View metadata, citation and similar papers at core.ac.uk

brought to you by CORE

provided by Boise State University - ScholarWorks

Boise State University
ScholarWorks

Physics Faculty Publications and Presentations

Department of Physics

4-18-2016

Selective-Area Growth of Heavily *n*–Doped GaAs Nanostubs on Si(001) by Molecular Beam Epitaxy

Yoon Jung Chang
UCLA

Paul J. Simmonds
Boise State University

Brett Beekley
UCLA

Mark S. Goorsky
UCLA

Jason C.S. Woo
UCLA

Copyright (2016) American Institute of Physics. This article may be downloaded for personal use only. Any other use requires prior permission of the author and the American Institute of Physics. The following article appeared in *Applied Physics Letters, 108*(16), 163106 and may be found at doi: 10.1063/1.4947436

Selective-area growth of heavily *n*–doped GaAs nanostubs on Si(001) by molecular beam epitaxy

Yoon Jung Chang,[1,a)] Paul J. Simmonds,[2] Brett Beekley,[3] Mark S. Goorsky,[3] and Jason C. S. Woo[1]
[1]*Department of Electrical Engineering, UCLA, Los Angeles, California 90095, USA*
[2]*Departments of Physics/Materials Science and Engineering, Boise State University, Boise, Idaho 83725, USA*
[3]*Department of Materials Science and Engineering, UCLA, Los Angeles, California 90095, USA*

(Received 13 January 2016; accepted 12 April 2016; published online 20 April 2016)

Using an aspect ratio trapping technique, we demonstrate molecular beam epitaxy of GaAs nanostubs on Si(001) substrates. Nanoholes in a SiO_2 mask act as a template for GaAs-on-Si selective-area growth (SAG) of nanostubs 120 nm tall and ≤100 nm in diameter. We investigate the influence of growth parameters including substrate temperature and growth rate on SAG. Optimizing these parameters results in complete selectivity with GaAs growth only on the exposed Si(001). Due to the confined-geometry, strain and defects in the GaAs nanostubs are restricted in lateral dimensions, and surface energy is further minimized. We assess the electrical properties of the selectively grown GaAs nanostubs by fabricating heterogeneous p^+–Si/n^+–GaAs *p–n* diodes. *Published by AIP Publishing.*
[http://dx.doi.org/10.1063/1.4947436]

Heterogeneous integration of III–V semiconductors with silicon complementary metal-oxide-semiconductor (CMOS) platforms could enable high performance electronics, optoelectronics, and photonics, for radar communications and space-based detection systems.[1–3] Coupling the excellent electronic and optical properties of compound semiconductors like GaAs,[4,5] with the component density of Si VLSI technology would yield cheap, lightweight, and scalable multi-functional integrated circuitries. Integration of GaAs devices with Si CMOS requires defect-free epitaxial growth with uniform size, spatial distribution, and doping profiles. However, significant mismatch exists between the lattice constants, thermal expansion coefficients, and structural polarities of Si and GaAs.[6,7] These differences mean that heteroepitaxial GaAs on Si typically contains high defect densities, compromising any performance gain. Researchers have tried numerous approaches to reduce defect density in GaAs/Si films, including graded buffers, strained layer superlattices, thermal cycle annealing, migration-enhanced epitaxy, and two-step growth.[8–16] Despite reducing defect densities, these methods are often complex and time-consuming, while thick buffers are unsuitable for Si CMOS integration. Moreover, many approaches involve Si(111) substrates, whereas growth on Si(001) is required for CMOS compatibility.

Aspect ratio trapping (ART) is an alternative approach that enables selective-area growth (SAG) of lattice-mismatched materials inside high aspect ratio (>1), submicron openings patterned in a dielectric mask.[17–22] Dislocations originating at the heterointerface terminate at the dielectric sidewalls, resulting in defect-free growth above the defect-trapping region. By eliminating the need for a thick buffer, ART also mitigates thermal stress and cracking.

Most previous reports of GaAs/Si(001) using SAG-ART focused on metalorganic chemical vapor deposition (MOCVD) and chemical beam epitaxy.[23] Large differences in pyrolysis of the chemical precursors between the mask and bare substrate enhance growth selectivity. An example is template-assisted selective epitaxy, where MOCVD is used to grow III-V/Si(001) nanowires.[24] However, much research into MOCVD-SAG has focused on trenches where defects still propagate along the channel.[25–31] In ART, nanoscale openings prevent lateral defect propagation, but few studies measured the GaAs/Si(001) electrical properties, and none looked specifically at the electrical behavior of the heterointerface.[24,30]

There are instances where growth by molecular beam epitaxy (MBE) rather than MOCVD may be preferred, for example, where ultrahigh material purity, or monolayer-level control over interface abruptness and layer thickness is essential. However, MBE is a physical deposition technique meaning that unless growth conditions are precisely controlled, Ga adatoms are equally likely to stick to the dielectric mask as to the Si. As a result, obtaining complete selectivity in MBE-based GaAs SAG is challenging.[32,33] MBE-based GaAs/Si SAG requires that: (1) migration length on the dielectric mask must be sufficiently large for Ga adatoms to reach the nearest hole (Figure 1(a)); (2) Ga adatom sticking coefficient must be lower on the dielectric than Si (Figure 1(b)).

Because of lower surface/interface energies, MBE-based SAG research has often focused on Si(111) substrates.[34–38] However, it is Si(001) that underpins the semiconductor industry, so GaAs integration on this surface is arguably more important. GaAs/Si(001) SAG research has typically been limited to masks with micron-sized patterns[39–42] and Au-assisted nanowire synthesis.[34] Only two reports demonstrate MBE SAG-ART of GaAs/Si(001) nanostubs but analysis of the GaAs/Si heterointerface is still needed to gauge its suitability for future devices.[43,44] To obtain high quality GaAs/Si(001) by MBE, we must understand this interface by investigating the initial stages of growth, and resulting crystal structure, as a function of growth conditions. In summary, a pressing need exists for a detailed study of nanoscale GaAs/Si(001) integration by MBE-based SAG-ART.

[a)]Author to whom correspondence should be addressed. Electronic mail: shyj13@ucla.edu

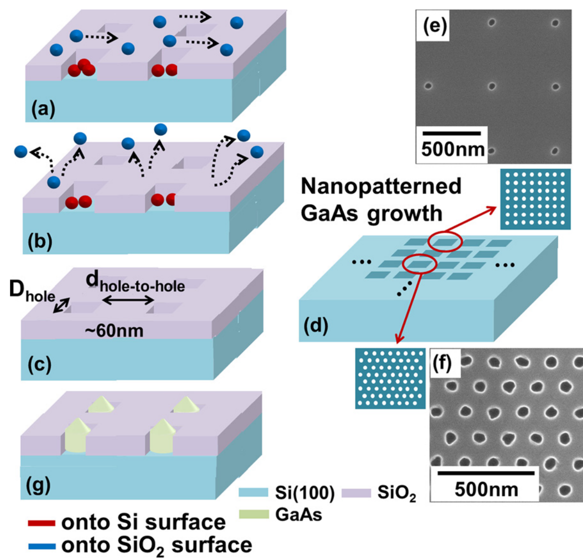

FIG. 1. (a) and (b) Process flow for MBE SAG of n^+–GaAs nanostubs on nanopatterned SiO_2/Si(001): (c) nanohole patterning using e-beam lithography/RIE etching, (d) nanopatterned SiO_2-matrix: example SEM images of 50 nm diameter nanoholes in (e) a square array (hole-to-hole distance 500 nm) and (f) a hexagonal array (hole-to-hole distance 100 nm), (g) SAG of GaAs/Si nanostubs.

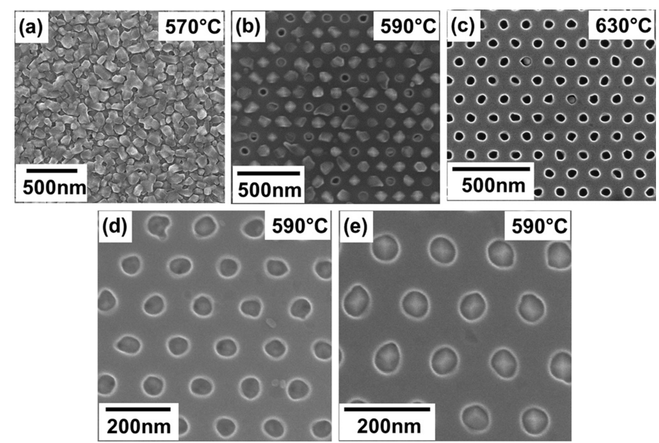

FIG. 2. FESEM image of GaAs nanostubs on nanopatterned SiO_2/Si(001) at T_{SUB} = (a) 570 °C, (b) 590 °C, (c) 630 °C. Optimized GaAs nanostub growth after (d) 15 min and (e) 30 min deposition (hole diameter: 50 nm, hole-to-hole distance: 100 nm).

In this letter, we demonstrate MBE-based ART of zinc-blende n^+–GaAs/Si(001) nanostubs with diameters <100 nm, and complete selectivity. We detail how MBE growth parameters affect GaAs/Si(001) SAG, particularly close to the heterointerface, and the origins of defect formation. Initial electrical performance data for n^+–GaAs/Si(001) *p*–*n* junctions suggests their promise for future devices based on heterogeneous integration.

We created dielectric masks by thermally growing 60 nm SiO_2 onto 1 cm^2 *p*–Si(001) substrates. Using e-beam lithography and RIE (Figure 1(c)), we defined a matrix of square and hexagonal arrays of circular nanoholes with a range of diameters (50–200 nm) and hole-to-hole distances (100–1000 nm) (Figures 1(d)–1(f)). Each pattern covered an area of 10 000 μm^2. Since we are particularly interested in nucleation and initial growth, we designed our nanoholes with an aspect ratio of 1.2 to simplify the microscopy. It is our intention in future work to focus on the aspect ratios >1.4 that can fully filter {111}-oriented stacking faults (SFs) above the defect-trapping region. After standard solution-based cleaning, we heated substrates to >800 °C *in vacuo* to remove any oxide formed during loading. This step was crucial for achieving complete SAG. We initiated SAG by cycling short depositions of n^+–GaAs with growth interruptions under As_2. This migration-enhanced approach gives Ga adatoms on the mask time to reach the nanoholes, and promotes desorption of residual Ga from the mask for complete selectivity (Figure 1(g)).

We studied nanostub structure and crystal quality using field-emission scanning electron microscopy (FESEM) and cross-sectional transmission electron microscopy (XTEM). We characterized the electrical response of the heterointerface via I-V measurements of a p^+–Si/n^+–GaAs diode.

We grew GaAs/Si nanostubs at substrate temperature (T_{SUB}) = 570–630 °C to find the optimum for highly selective growth (Figures 2(a)–2(c)). During this T_{SUB} variation study, the V/III beam equivalent pressure (BEP) ratio was ∼20 and GaAs growth rate was ∼120 nm/h. At 570 °C, there was no growth selectivity (Figure 2(a)). Highly defective, polycrystalline GaAs grew both on the mask and in the nanoholes.[45]

Increasing T_{SUB} to 590 °C (Figure 2(b)) resulted in complete selectivity without parasitic growth on the mask. The single-crystal nanostubs have four top facets, consistent with (001)-oriented zinc-blende GaAs, and are 120–140 nm tall. Figure 2(b) shows some non-uniformity in nanostub shape and size, and ∼10% of the nanoholes are empty. These effects were due to incomplete pre-growth substrate cleaning. GaAs growth was inhibited in nanoholes where native oxide was not fully removed. As discussed below, by correcting this issue we achieved uniform nanostub growth in 100% of nanoholes (Figures 2(d) and 2(e)).

At T_{SUB} = 630 °C (Figure 2(c)), only 2% of nanoholes contained GaAs nanostubs. Increased adatom desorption from the SiO_2 mask at higher T_{SUB} means Ga adatoms have less time to reach the nearest nanohole.[46,47]

Using the optimized T_{SUB} of 590 °C, we varied V/III BEP ratio and GaAs growth rate. Reducing V/III ratio to ∼10 for a growth rate of ∼120 nm/h resulted in 83% nanohole filling. Lower V/III ratio means Ga adatoms inside a nanohole are less likely to encounter As adatoms, resulting in GaAs nanostubs with lower crystal quality (evidenced by the absence of top four facets) than those grown at higher V/III ratio. Although lower growth rate could compensate for this by increasing Ga migration length, reducing growth rate to ∼70 nm/h (V/III ratio ∼20) led to ≤3% filling of nanoholes. This implies that under these conditions, Ga desorption occurs before GaAs formation. Therefore, our initial optimized MBE conditions for GaAs/Si SAG were: T_{SUB} = 590 °C; V/III BEP ratio = 20; and growth rate = 120 nm/h.

We studied nanostub nucleation under these conditions; 15 min GaAs deposition resulted in Volmer-Weber island nucleation at nanohole edges (Figure 2(d)). As growth proceeded, the GaAs islands increased in size, until after 30 min, uniform single-crystal GaAs nanostubs with clear top and sidewall facets had formed (Figure 2(e)). Longer deposition times led to 100% filling of the nanoholes, with complete selectivity.

GaAs nanostub morphology and coverage was independent of nanohole diameter, hole-to-hole distance and geometry

over the ranges we studied: 50–200 nm and 100–1000 nm, respectively, and square/hexagonal arrays (Figures 1(d)–1(f)).

The black dashed box in Figure 3 summarizes the MBE growth window for SAG of GaAs/Si nanostubs. Red and blue dots outside this box indicate conditions resulting in a lack of selectivity due to incomplete nanohole filling and polycrystal formation, respectively. We fine-tuned T_{SUB} within this window between 590 and 620 °C, at ∼120 nm/h growth rate, raising V/III ratio to compensate for increased As desorption at higher temperature.

We extracted TEM samples containing a single row of nanostubs, with a zone axis of [110]. Uniform GaAs/Si nanostubs, with clear top/side facets and stacking faults (SFs) at the base, grow across the whole array of nanoholes at 590 °C (Figure 3(a)). GaAs/Si nanostubs grown at $T_{SUB} = 605$–620 °C were identical to those grown at 590 °C (Figures 3(b) and 3(c)), confirming that increased V/III ratio maintains GaAs stoichiometry and crystal quality.

Figures 4(a) and 4(b) show the Si/GaAs heterointerface of a nanostub grown at 620 °C (V/III ratio = 50, growth rate = 120 nm/h). Figure 4(b) reveals the GaAs/SiO_2 sidewall interface is a few nanometers wide, and that the GaAs/Si interface follows a 10 nm-deep recess in the Si surface. Similar observations were made for nanostubs grown at 590–605 °C (not shown). Fast Fourier transform (FFT) analysis of the area marked (c) in Figure 4(b) shows the single-crystal Si(001) substrate.

FFT analysis of the GaAs/Si heterointerface (area (d) in Figure 4(b)) reveals streaking in the [−111] direction, consistent with SFs aligned along the preferred {111} plane.[26,28] HRTEM images of nanostubs from various locations on the samples consistently showed SFs that begin either at the GaAs/Si or GaAs/SiO_2 sidewall interfaces. Two SFs sometimes meet and annihilate. Additional spots in the FFTs also indicate ABCBACABCBA nanotwin stacking. However, no threading dislocations are observed, consistent with nanostructure ART-SAG in the literature.[18] Above the defect-trapping region (area (e) in Figure 4(b)), the FFT shows the FCC stacking of defect-free single-crystal zinc-blende GaAs. SAG via ART effectively suppresses SF penetration into upper regions of the nanostubs.

Our approach offers an additional benefit. As noted above, RIE creates shallow Si recesses at the bottom of each nanohole during mask patterning. The high temperature bake before growth can produce double-height atomic steps in these pits, helping to eliminate the anti-phase disorder prevalent in bulk GaAs/Si(001) heteroepitaxy.[29,48]

We calculated GaAs nanostub strain by measuring lattice parameters from the HRTEM FFTs in Figures 4(c) and 4(e), and found the GaAs is ≥99% relaxed in the in-plane direction. Plan-view TEM is often used to estimate defect density inside heteroepitaxial films, but in our case the tiny surface area of the GaAs nanostubs makes this difficult. We hence used two alternative methods to statistically quantify defects. The first considers the defects in terms of cross-sectional area. In Figure 4(f), the red dashed-dotted line marks the total cross-sectional area of a single nanostub, while the region containing SFs is bounded by a yellow square-dotted line. Analysis of the three samples in Figure 3 showed SFs and/or nanotwins occupy on average ≤40% of total nanostub cross-sectional area (std. dev. = 17.5%). The second method counts defects propagating to the top facets. The red dotted lines in Figure 4(g) shows the total facet perimeter, defined as the sum of the lengths of a nanostub's two top facets. The yellow square-dotted lines highlight the places where SFs intersect these facets. We define the length fraction of defects as the ratio between the length of the yellow lines to the total facet perimeter. For the same three

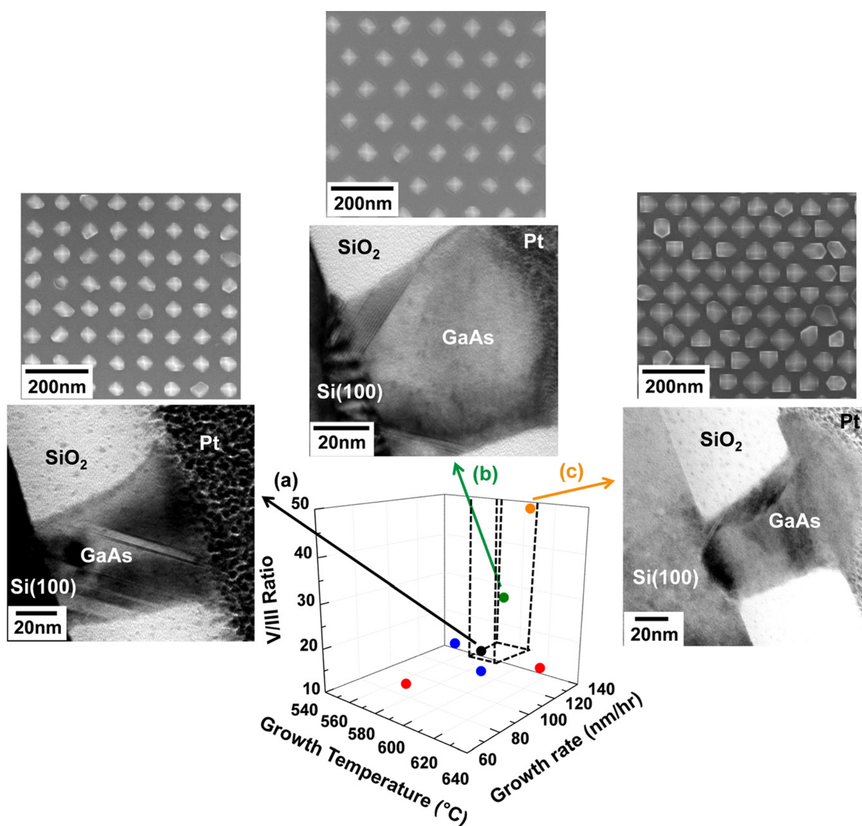

FIG. 3. 3D optimization window for GaAs/Si nanostub SAG: (a) $T_{SUB} = 590$ °C/V/III = 20, (b) $T_{SUB} = 605$ °C/V/III = 30, and (c) $T_{SUB} = 620$ °C/V/III = 50 (hole diameter: 50 nm, hole-to-hole distance: 100 nm). FESEM (upper) and bright-field XTEM (lower) images are shown for each sample.

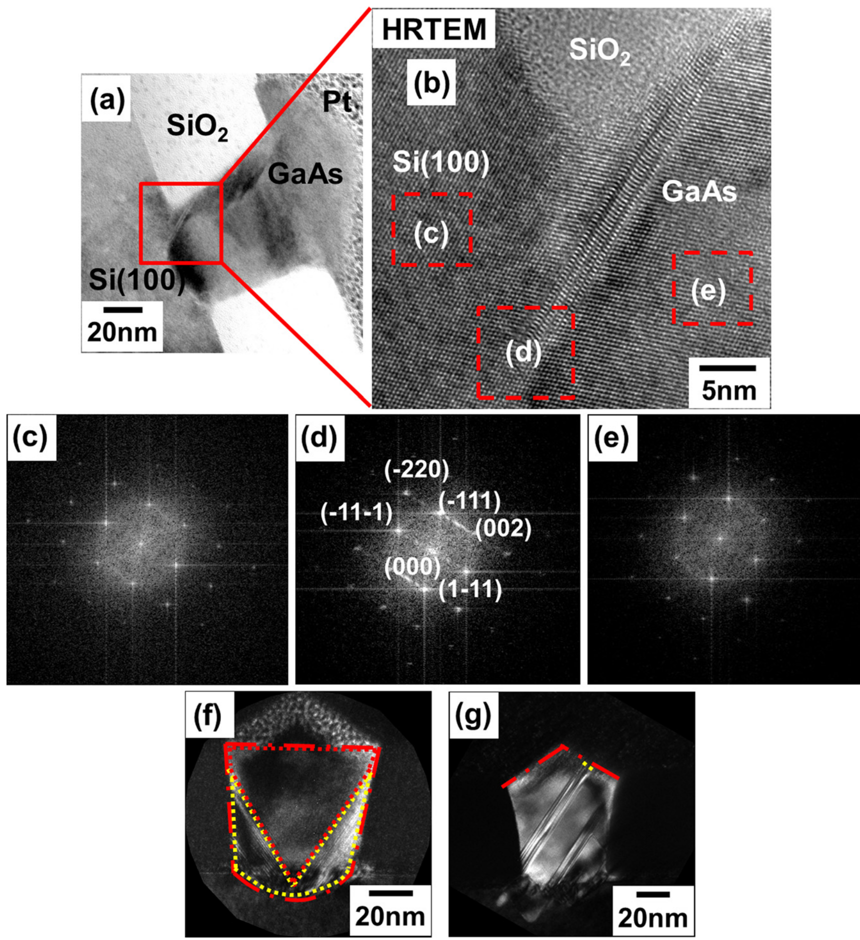

FIG. 4. GaAs nanostub SAG on Si(001): (a) Bright-field XTEM image and (b) HRTEM image near Si/GaAs interface; FFTs of (c) Si, (d) a region of SFs at heterointerface, and (e) defect-free GaAs. (f) Dark-field (DF) XTEM image for defect quantification method 1; (g) DF XTEM image for defect quantification method 2 (hole diameter: 50 nm, hole-to-hole distance: 100 nm).

samples, SFs constitute on average $\leq$10% of the top facet perimeter (std. dev. = 8.6%), calculated from more than 10 nanostubs on each sample. We attribute these low defect densities to the *necking effect* that encourages SF annihilation at GaAs/SiO_2 sidewalls.[23,24]

To the origin of SFs and nanotwins, we compared areal and linear fractions of defects in nanostubs grown at 590–620 °C. There was no distinct correlation between defect density and T_{SUB}, ruling out SF/nanotwin generation due to thermal mismatch during cool down. Instead, we observed different defect densities in GaAs nanostubs grown at the same T_{SUB}. This suggests that as the initial GaAs islands merge into a single nanostub, FCC stacking is stochastically disrupted, resulting in SF/nanotwin formation at the GaAs/Si interface.[49,50] This is likely due to different Si surface planes created during RIE. SFs originating at GaAs/SiO_2 sidewalls are likely due to roughness generating local stress in the nanostub. Our strain/defect density calculations confirmed that more SFs resulted in increased strain relaxation.

We performed I–V measurements on heterogeneous Si/GaAs *p–n* diodes, consisting of n^+–GaAs nanostubs with a range of diameters grown on p^+–Si(001) by SAG-ART (Figure 5(b) inset, left). We used e-beam evaporation of Ge/Ni/Ge/Au and Al to form ohmic contacts to GaAs and Si, respectively. The SiO_2 mask insulates the top contact from the Si. Reducing nanostub diameter from 100 to 55 nm improves diode performance by reducing the distance that dislocations have to glide before termination on a sidewall. However, even though our GaAs/Si(001) nanostubs are dislocation-free, reverse leakage current (Figure 5(b)) is higher than was reported for a selectively grown GaAs/Si(111) *p–i–n* solar cell.[38] We believe that the lower surface/interface energies of Si(111) result in superior film quality and heterointerfaces compared to the growth on Si(001). To reduce the leakage current in future, we will use nanoholes

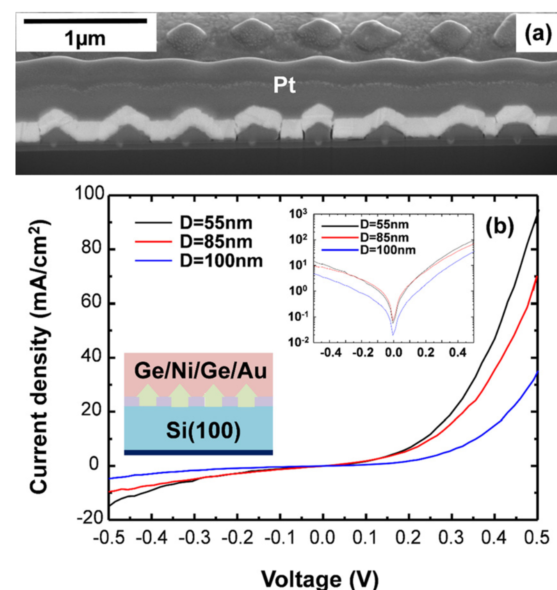

FIG. 5. (a) Cross-sectional FESEM image and (b) current-voltage electrical measurement plot of heterogeneous p^+-Si/n^+-GaAs *p-n* diode (T_{SUB} = 605 °C/V/III = 30/growth rate = 120 nm/h).

with aspect ratios >1.4 to increase the defect-trapping efficiency. Furthermore, surface treatment and/or removal of RIE surface damage could also help improve the material quality, and hence electrical performance.

In conclusion, we have demonstrated single-crystal GaAs/Si(001) nanostubs <100 nm in diameter using an MBE-based ART technique. Despite our chosen aspect-ratio being just below the minimum value of 1.4, the GaAs is ≥99% strain relaxed without the threading dislocations prevalent in bulk GaAs/Si(001) heteroepitaxy. Only a few stacking faults originating from the GaAs/Si interface reach the top facets. I–V measurements on p^+–Si/n^+–GaAs diodes show the promise of this approach for future nanoscale integrated device heterostructures.

The authors acknowledge the support of the Integrated NanoMaterials Laboratory MBE user facility at the California NanoSystems Institute, UCLA. This material is based upon work supported by U.S. Navy Space and Naval Warfare Systems Center (SSC) Pacific under Award No. N66001–13–1–4013.

[1]D. L. Mathine, IEEE J. Quantum Electron. **3**, 952 (1997).
[2]T. E. Kazior, Philos. Trans. R. Soc. A **372**, 20130105 (2014).
[3]Y. Halioua, A. Bazin, P. Monnier, T. J. Karle, G. Roelkens, I. Sagnes, R. Raj, and F. Raineri, Opt. Express **19**, 9221 (2011).
[4]Y. Q. Wu, M. Xu, P. D. Ye, Z. Cheng, J. Li, J.-S. Park, J. Hydrick, J. Bai, M. Carroll, J. G. Fiorenza, and A. Lochtefeld, Appl. Phys. Lett. **93**, 242106 (2008).
[5]B. Hua, J. Motohisa, Y. Ding, S. Hara, and T. Fukui, Appl. Phys. Lett. **91**, 131112 (2007).
[6]S. F. Fang, K. Adomi, S. Iyer, H. Morkoc, H. Zabel, C. Choi, and N. Otsuka, J. Appl. Phys. **68**, R31 (1990).
[7]S. M. Ting and E. A. Fitzgerald, J. Appl. Phys. **87**, 2618 (2000).
[8]J. A. Carlin, S. A. Ringel, E. A. Fitzgerald, M. Bulsara, and B. M. Keyes, Appl. Phys. Lett. **76**, 1884 (2000).
[9]G. Vanamu, A. K. Datye, R. Dawson, and S. H. Zaidi, Appl. Phys. Lett. **88**, 251909 (2006).
[10]Y. Takano, M. Hisaka, N. Fujii, K. Suzuki, K. Kuwahara, and S. Fuke, Appl. Phys. Lett. **73**, 2917 (1998).
[11]N. Chand, R. People, F. A. Baiocchi, K. W. Wecht, and A. Y. Cho, Appl. Phys. Lett. **49**, 815 (1986).
[12]G. Radhakrishnan, O. McCullough, J. Cser, and J. Katz, Appl. Phys. Lett. **52**, 731 (1988).
[13]N. Hayafuji, M. Miyashita, T. Nishimura, K. Kadoiwa, H. Kumabe, and T. Murotani, Jpn. J. Appl. Phys., Part 1 **29**, 2371 (1990).
[14]W. Stolz, M. Naganuma, and Y. Horikoshi, Jpn. J. Appl. Phys., Part 2 **27**, L283 (1988).
[15]K. Ishida, Mater. Res. Soc. Symp. Proc. **91**, 133 (1987).
[16]Y. J. Mii, T. L. Lin, Y. C. Kao, B. J. Wu, K. L. Wang, C. W. Nieh, D. N. Jamieson, and J. K. Liu, J. Vac. Sci. Technol., B **6**, 696 (1988).
[17]T. A. Langdo, C. W. Leitz, M. T. Currie, E. A. Fitzgerald, A. Lochtefeld, and D. A. Antoniadis, Appl. Phys. Lett. **76**, 3700 (2000).
[18]Q. Li, S. M. Han, S. R. J. Brueck, S. Hersee, Y.-B. Jiang, and H. Xu, Appl. Phys. Lett. **83**, 5032 (2003).
[19]J.-S. Park, J. Bai, M. Curtin, B. Adekore, M. Carroll, and A. Lochtefeld, Appl. Phys. Lett. **90**, 052113 (2007).
[20]J. Bai, J.-S. Park, Z. Cheng, M. Curtin, B. Adekore, M. Carroll, A. Lochtefeld, and M. Dudley, Appl. Phys. Lett. **90**, 101902 (2007).
[21]J. G. Fiorenza, J.-S. Park, J. M. Hydrick, J. Li, J. Z. Li, M. Curtin, M. Carroll, and A. Lochtefeld, ECS Trans. **33**(6), 963 (2010).
[22]M. J. H. van Dal, G. Vellianitis, B. Duriez, G. Doornbos, C.-H. Hsieh, B.-H. Lee, K.-M. Yin, M. Passlack, and C. H. Diaz, IEEE Trans. Electron Devices **61**, 430 (2014).
[23]C.-W. Hsu, Y.-F. Chen, and Y.-K. Su, Nanotechnology **23**, 495306 (2012).
[24]H. Schmid, M. Borg, K. Moselund, L. Gignac, C. M. Breslin, J. Bruley, D. Cutaia, and H. Riel, Appl. Phys. Lett. **106**, 233101 (2015).
[25]J. Z. Li, J. Bai, J.-S. Park, B. Adekore, K. Fox, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, Appl. Phys. Lett. **91**, 021114 (2007).
[26]S. F. Cheng, L. Gao, R. L. Woo, A. Pangan, G. Malouf, M. S. Goorsky, K. L. Wang, and R. F. Hicks, J. Cryst. Growth **310**, 562 (2008).
[27]W. Guo, L. Date, V. Pena, X. Bao, C. Merckling, N. Waldron, N. Collaert, M. Caymax, E. Sanchez, E. Vancoille, K. Barla, A. Thean, P. Eyben, and W. Vandervorst, Appl. Phys. Lett. **106**, 062101 (2014).
[28]Y. He, J. Wang, H. Hu, Q. Wang, Y. Huang, and X. Ren, Appl. Phys. Lett. **106**, 202105 (2015).
[29]T. Orzali, A. Vert, B. O'Brien, J. L. Herman, S. Vivekanand, R. J. W. Hill, Z. Karim, and S. S. Papa Rao, J. Appl. Phys. **118**, 105307 (2015).
[30]N. Waldron, G. Wang, N. D. Nguyen, T. Orzali, C. Merckling, G. Brammertz, P. Ong, G. Winderickx, G. Hellings, G. Eneman, M. Caymax, M. Meuris, N. Horiguchi, and A. Thean, ECS Trans. **45**(4), 115 (2012).
[31]R. Cipro, T. Baron, M. Martin, J. Moeyaert, S. David, V. Gorbenko, F. Bassani, Y. Bogumilowicz, J. P. Barnes, N. Rochat, V. Loup, C. Vizioz, N. Allouti, N. Chauvin, X. Y. Bao, Z. Ye, J. B. Pin, and E. Sanchez, Appl. Phys. Lett. **104**, 262103 (2014).
[32]H. P. Lee, S. Wang, Y.-H. Huang, and P. Yu, Appl. Phys. Lett. **52**, 215 (1988).
[33]H. P. Lee, X. Liu, and S. Wang, Appl. Phys. Lett. **56**, 1014 (1990).
[34]S.-G. Ihn, J.-I. Song, Y.-H. Kim, J. Y. Lee, and I.-H. Ahn, IEEE Trans. Nanotechnol. **6**, 384 (2007).
[35]G. E. Cirlin, V. G. Dubrovskii, I. P. Soshnikov, N. V. Sibirev, Y. B. Samsonenko, A. D. Bouravleuv, J. C. Harmand, and F. Glas, Phys. Status Solidi RRL **3**, 112 (2009).
[36]J. H. Paek, T. Nishiwaki, M. Yamaguchi, and N. Sawaki, Phys. Status Solidi C **6**, 1436 (2009).
[37]G. E. Cirlin, V. G. Dubrovskii, Y. B. Samsonenko, A. D. Bouravleuv, K. Durose, Y. Y. Proskuryakov, B. Mendes, L. Bowen, M. A. Kaliteevski, R. A. Abram, and D. Zeze, Phys. Rev. B **82**, 035302 (2010).
[38]C.-P. Chu, S. Arafin, T. Nie, K. Yao, X. Kou, L. He, C.-Y. Wang, S.-Y. Chen, L.-J. Chen, S. M. Qasim, M. S. BenSaleh, and K. L. Wang, Cryst. Growth Des. **14**, 593 (2014).
[39]N. Yamamoto, N. Kondo, and Y. Nanishi, J. Cryst. Growth **96**, 705 (1989).
[40]T. Shibata, N. Kondo, Y. Nanishi, and M. Fujimoto, Mater. Res. Soc. Symp. Proc. **160**, 487 (1989).
[41]Y. C. Kao, E. A. Beam III, J. Y. Yang, and D. J. Sesler, J. Electron. Mater. **20**, 471 (1991).
[42]C.-P. Chu, S. Arafin, G. Huang, T. Nie, Y. Wang, J. Zou, S. M. Qasim, M. S. BenSaleh, and K. L. Wang, J. Vac. Sci. Technol., B **32**, 02C111 (2014).
[43]S. C. Lee, L. R. Dawson, S. H. Huang, and S. R. J. Brueck, Cryst. Growth Des. **11**, 3673 (2011).
[44]Z. Zhao, K. Yadavalli, Z. Hao, and K. L. Wang, Nanotechnology **20**, 035304 (2009).
[45]S. C. Lee and S. R. J. Brueck, Appl. Phys. Lett. **94**, 153110 (2009).
[46]S. C. Lee, K. J. Malloy, L. R. Dawson, and S. R. J. Brueck, J. Appl. Phys. **92**, 6567 (2002).
[47]M. Heiß, E. Riedlberger, D. Spirkoska, M. Bichler, G. Abstreiter, and A. Fontcuberta i Morral, J. Cryst. Growth **310**, 1049 (2008).
[48]R. Loo, G. Wang, T. Orzali, N. Waldron, C. Merckling, M. R. Leys, O. Richard, H. Bender, P. Eyben, W. Vandervorst, and M. Caymax, J. Electrochem. Soc. **159**(3), H260 (2012).
[49]F. Ernst and P. Pirouz, J. Appl. Phys. **64**, 4526 (1988).
[50]K. Volz, A. Beyer, W. Witte, J. Ohlmann, I. Németh, B. Kunert, and W. Stolz, J. Cryst. Growth **315**, 37 (2011).