DUAL-INPUT DC-TO-DC CONVERTER TOPOLOGIES AND CONTROL SCHEMES

by

Shaun Alan Stickel

A thesis

submitted in partial fulfillment

of the requirements for the degree of

Master of Science in Electrical Engineering

Boise State University

December 2015

BOISE STATE UNIVERSITY GRADUATE COLLEGE

DEFENSE COMMITTEE AND FINAL READING APPROVALS

of the thesis submitted by

Shaun Alan Stickel

Thesis Title: Dual-Input DC-to-DC Converter Topologies and Control Schemes

Date of Final Oral Examination: 15 October 2015

The following individuals read and discussed the thesis submitted by student Shaun Alan Stickel, and they evaluated his presentation and response to questions during the final oral examination. They found that the student passed the final oral examination.

Said Ahmed-Zaid, Ph.D.	Chair, Supervisory Committee
Vishal Saxena, Ph.D.	Member, Supervisory Committee
Kurtis Cantley, Ph.D.	Member, Supervisory Committee

The final reading approval of the thesis was granted by Said Ahmed-Zaid, Ph.D., Chair of the Supervisory Committee. The thesis was approved for the Graduate College by John R. Pelton, Ph.D., Dean of the Graduate College.

ACKNOWLEDGEMENTS

Dr. Said Ahmed-Zaid

Dr. Vishal Saxena

Dr. Kurtis Cantley

AUTOBIOGRAPHICAL SKETCH OF AUTHOR

Shaun Stickel attended Oregon State University from 2004 through 2010 and received two bachelor's degrees. His first degree in electrical engineering emphasized analog circuit design and power electronics, and the second in computer engineering with a minor in computer science emphasized embedded systems. While at Oregon State University, Shaun participated in the MECOP program, which included two internships. The first internship was at Micro Power Electronics from April 2007 to September 2007, developing battery management PCBAs for medical applications. His second internship was at Intel Corporation developing test hardware for video products from June 2008 to January 2009.

In June of 2010, Shaun started at Micron Technology as a product engineer working on the development of enterprise PCIe SSDs. During his first year at Micron, his responsibilities were focused on test script development and automation of performance testing. In 2011, Shaun moved to the SSD hardware design group at Micron and since then has lead the design of multiple enterprise PCIe SSDs including the Micron P420m.

In August of 2010, Shaun started his master's program at Boise State University, pursuing a master's of engineering in electrical engineering. The first four years consisted of coursework focused on analog circuit design, high speed interface design, and digital systems. In 2014, work on his master's thesis began based upon previous work done investigating the viability of dual input power supplies.

ABSTRACT

Dual-input DC-to-DC converters are power supplies that draw power from two sources simultaneously and deliver power to a single load, the ratio of power drawn from each source and be held constant with changes in the load. Applications for dual-input power supplies are computer systems, mobile systems using energy harvesting, and systems needing redundant power supplies. This writing covers the operation and control of dual-input DC-to-DC converters that implement a non-inverting buck-boost function and utilize only a single power path.

Traditionally, a dual-input power supply is created by placing two standard power paths in parallel. This adds considerable control complexity associated with synchronizing the two converters. Four new power path topologies are presented: dual-input four-FET buck-boost, dual-input zeta, dual-input SEPIC, and alternate dual-input SEPIC. The single power path approaches require fewer components than the traditional approaches, however, the efficiency is slightly lower.

These converters can be controlled using any of the standard power supply control approaches, including: voltage mode, current mode, and constant on-time. Each control method does need to be modified slightly. The biggest difference in the control of these converters is in the logic that is used to control the switches in the power path. The ratio of current drawn from each input source can be held constant and can be adjusted in an open loop fashion if some variability is allowed, otherwise a sensor and feedback control can be implemented to fix the input current or input power ratio.

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LIST OF ABBREVIATIONS

MECOP	Multiple Engineering Co-Op Program
DC	Direct Current
SEPIC	Single Ended Primary Inductance Converter
AT	Advanced Technology
ATX	Advanced Technology Extended
HDD	Hard Disk Drive
SSD	Solid State Drive
PCIe	Peripheral Component Interconnect Express
SAS	Serial Attached SCSI
SCSI	Small Computer System Interface
DRAM	Dynamic Random Access Memory
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
JFET	Junction Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
MTTF	Mean Time To Failure
PWM	Pulse Width Modulator
OTA	Operational Transconductance Amplifier
LDO	Low Dropout Regulator
SW	Switch

CHAPTER ONE: INTRODUCTION TO DUAL-INPUT DC-TO-DC CONVERTERS

Topic Overview

The goal of a dual-input power supply in the context of this writing is to provide power to a single load from two input power sources either simultaneously or alternately. This objective can be met using simple diodes or paralleled low dropout regulators (LDOs) with some control logic, however, as the power requirements of the load increase, these approaches can become highly inefficient or inviable.

A DC-to-DC converter is typically employed when the requirements for power and or efficiency are such that simpler topologies are not sufficient to meet these requirements. The complexities associated with the design of DC-to-DC converters make it difficult to design dual-input converters using those topologies. Currently the most common strategy used to design dual-input DC-to-DC converters is to place multiple converters in parallel and to synchronize them using complex analog control loops.

As shown in Figure 1 a dual-input power supply has two inputs or power sources and a single output also called a load. The output typically has a regulated voltage set by the power supply itself and current is supplied to the load on demand. The inputs are typically a loosely fixed voltage and may or may not be the same as the output voltage; current drawn from these inputs is determined by the power supply itself. In a dual-input power supply the current or power drawn from the inputs is drawn from both sources either simultaneously or alternately.

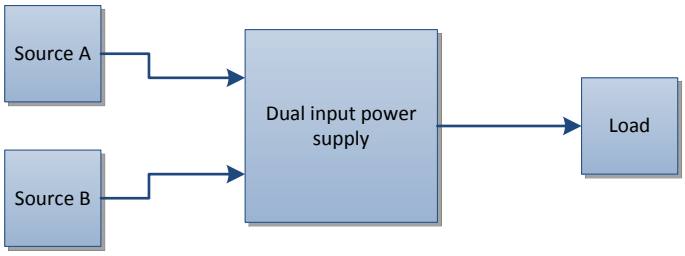

Figure 1. Dual-Input Power Supply

As an example, consider that the power supply shown in Figure 1 is an ideal (100% efficiency) power supply and is supplying power to the load with a regulated voltage of 5V. The input source A is supplying power at 5V and input source B is supplying power at 15V. Consider that the load is drawing 5A. In this example the load power is 25W. By definition the power being delivered to the load by the power supply must be drawn from the available sources A and or B as shown in Equation (1) which applies for ideal power supplies. With the load drawing 25W, the sources must together be supplying 25W to the power supply.

$$P_{load} = P_{sourceA} + P_{sourceB} \quad (1)$$

It is up to the power supply to decide how much of the 25W will be drawn from each of the available input power sources. The power supply may decide to draw an equal current from both sources, in which case 1.25A would be drawn from each source and source A would be supplying 6.25W while source B would be supplying 18.75W. The power supply may also decide to draw an equal amount of power from both sources, in which case each source would be supplying 12.5W and source A would be supplying 2.5A while source B would be supplying 0.833A. The actual ratio of current or power drawn from the sources is arbitrary and is typically dictated by the design constraints for the power supply and for the system as a whole.

Applications for Dual-Input DC-to-DC Converters

The idea for a dual-input DC-to-DC converter was initially conceived of while working on a product design for a PCIe add-in card (i.e. a video card or solid state drive) for which there were two input power sources available shown in Figure 2. Taken together each input power source could supply instantaneously 35W of power. Due to mechanical limitations the average power consumed could be not more than 25W. The peak power that could be drawn from one of the input sources was 25W, the other could supply an additional 10W.

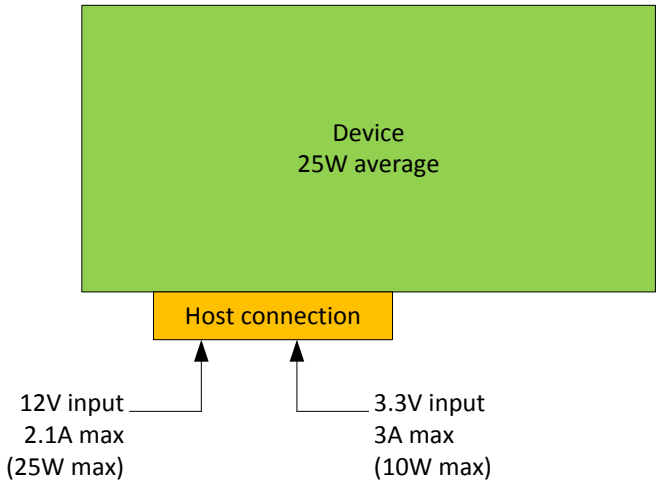

Figure 2. PCIe Add-In Card Application Example

Being limited to a single input source in this case limits the peak power to 25W. The thermal limitation was only for average power. As a result of this limitation the device would need to reduce its average power to below 25W to keep the peak power at or below 25W as shown in Figure 3. The consequence of this being reduced performance as the devices average power would need to be limited to something less than 25W in order to guarantee that the peak power does not exceeded 25W. Exceeding the 25W limit while using only the 12V input would exceed the 2.1A current limit on that input source. Making use of the second input source would allow the instantaneous power limit to be

raised to 35W while keeping the average power at or under 25W to satisfy mechanical requirements.

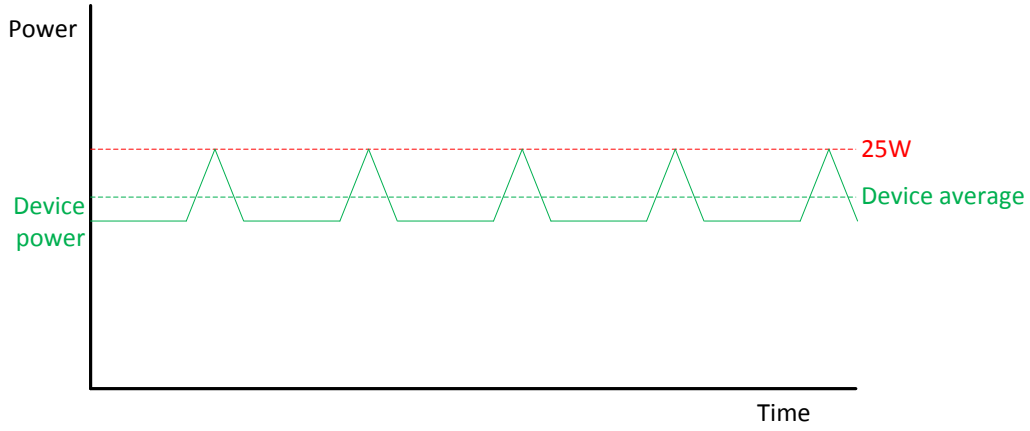

Figure 3. PCIe Add-In Card Application Example with Power Limited to 25W Peak

Dual-input converters are useful in applications where there is more than one power source and there is a benefit in drawing power from multiple sources either simultaneously or alternately. This benefit can take the form of improved energy efficiency, an increase in the maximum average or peak energy that can be consumed, or in reducing the current being drawn through each input connection to the system. There can also be benefits in terms of redundancy or in mobile systems that may use multiple sources for operation and for battery charging.

Computer System Applications for Dual-Input DC-to-DC Converters

Computer systems conforming to the various derivatives of the AT specification contain a variety of examples where multiple power sources are provided to computer components such as hard drives, video cards, and memory. The most common derivative of AT is ATX, which supplies 12V, -12V, 5V, and 3.3V as well as a low power 5V auxiliary source supplying power to the components of a computer system. Some interfaces such as PCIe step the 5V auxiliary input down to a 3.3V auxiliary supply.

Table 1 shows a breakdown of the power rails and common sources in ATX based computer systems.

Table 1. Based System Power Utilization by Interface

Source	SATA	SAS	PCIe	DRAM	SFF-8639
12V		√	√		√
5V	√	√			√
3.3V	√		√		√
1.5V/1.35V				√	
5V/3.3V auxiliary			√	√	√

SATA and SAS hard disk drives (HDDs) and more recently solid state drives (SSDs) are supplied with both 5V and 3.3V with a power limit of about 9W. SAS storage devices especially are often required to use each input (12V and 5V) equally either in terms of current or power in order to reach their maximum power with minimal loading on both supplies.

PCIe cards are allowed to draw up to 25W unless an additional 12V input is provided through a dedicated connector other than the primary hot connector. This power limit is however an average and the peak current allowed on the 12V input is 2.1A, which puts a peak power limit on PCIe cards of 25W, and puts the average power somewhat below this. If some power is drawn from the 3.3V input if it is present, then the average would truly be at 25W with peaks above 25W without violating the maximum current limit on the input power sources.

High power PCIe cards can draw 150W or even 350W as of the third generation of PCIe. These power demands are met by supplying additional power to the card through an additional 12V input power source from an auxiliary connector that is explicitly stated cannot be shorted to the 12V input source on the edge connector.

Because these two power sources are often both used by video cards to reach their full performance and they cannot be tied together some form of dual-input power supply is required.

Other interfaces exist as well which have multiple power inputs such as the SFF-8639 connector and DRAM modules. In all of these types of devices there are some common benefits to using multiple input power sources. By using two sources, the input current stress on connector contacts can be reduced, the loading on each rail of the host power supply can be reduced, and in some cases the peak power that the component is allowed to use can be increased.

Battery Equipped System Applications for Dual-Input DC-to-DC Converters

In mobile systems there are often at least two power sources for a device, its internal battery, and an external charger. In some mobile systems there is more than one external power source, for example an electric vehicle may use solar power, regenerative breaking, an on-board generator, and external power as a means of charging the internal battery. In most of these systems only one input power source at a time is used to power the device, such as in a cell phone where either the battery or an external charger is used to power the device, but never both.

When there are multiple input power sources, it may be useful to power the device from both sources simultaneously to minimize the loading on each source, especially if one source is susceptible to brown-out due to overloading. In such an application a dual-input DC-to-DC converter could be used to control the amount of power drawn from each input source in order to either minimize loading on sensitive power sources, or to maximize efficiency.

Another possibility is in systems with two batteries which may not have the same capacity or state of health. In such a system it may be advantageous to draw the full system power from both batteries at the same time with a given ratio of power from each battery in order to either reduce loading on a failing battery to extend its life or to load both batteries in such a way that the system can operate at full power for as long as possible.

Some mobile devices such as calculators and wearable devices, use various forms of energy harvesting to supplement battery power and extend the functional life of the device when operating without an external power supply. In this application some type of dual-input DC-to-DC power supply would be needed in order to draw as much power as possible from external sources such as solar, and draw the minimum possible amount of power from the devices internal battery.

Redundant Power Source Applications for Dual-Input DC-to-DC Converters

Some systems use multiple input power sources for redundancy. In these systems, it is common to use only one of the input sources at a time. When one fails the other is activated as a backup. It may be beneficial for systems with multiple redundant power sources to use both supplies simultaneously.

If each supply can source 100% of the system power demand, then the system could draw 50% of its power from each source thereby increasing the lifetime (reducing the MTTF) of each source by reducing the loading on each power source. In the event of a failure of one of the sources 100% of the power can then be drawn from the other source. Switching from one power source to another can sometimes cause the system

power to brown out. Having a dual-input DC-to-DC converter with a single power path reduces the chance of this occurring.

Thesis Scope

This writing will discuss topologies of DC-to-DC converters which can draw power from two sources using a single power path and will compare with more traditional approaches using two power paths. The power paths discussed will be buck-boost types, meaning that the output voltage is not bounded by either of the input voltages. Details of the power paths, their operation, and control schemes will be presented. Operational modes for the proposed dual-input power paths will be in-cycle and cycle-by-cycle. Control schemes discussed will be voltage mode, current mode, and constant on-time. Finally a simulation of a real-world design will be shown to illustrate how such a device might perform if implemented.

Definitions and Terminology

The term DC-to-DC converter is used here to define any type of energy converter that draws energy from one or more sources and delivers that energy to one or more loads by way of using an inductor as an energy storage and release mechanism. A “buck boost” converter is any type of DC-to-DC converter which can generate a fixed output voltage that is not bounded by the input voltage(s). The power path of a DC-to-DC converter is the components through which the energy flows from source(s) to load. The operating mode of a dual-input converter is the method in which the power path switches are controlled so as to draw energy from two input sources simultaneously. The control scheme of the converter is the concept and circuits that control the converters switches in order to achieve a stable output voltage.

The term “switch” in this writing will generally be assumed to mean a MOSFET type device. In general a switch could also be a MOSFET, IGBT, JFET, bipolar transistor, or other type of device which can have a low resistance “on” state and a high resistance “off” state.

It is assumed in this writing that the reader knows all of the units of measure contained within such as the volt, ohm, and watt among others.

CHAPTER TWO: BACKGROUND ON DC-TO-DC CONVERTERS

Theory of Operation

A DC-to-DC converter operates primarily by charging and discharging an energy storage device, typically an inductor, in such a way as to control the voltage going to a load while supplying the amount of current (or power) that is demanded by that load. In an ideal lossless DC-to-DC converter the power supplied to the load is the same as the power drawn from the source.

To illustrate the operation of a DC-to-DC converter a buck converter will be used as an example. A diagram of a typical buck converter is shown in Figure 4 The power path highlighted in red is the portion of the circuit that actively transfers power from the input power source to the load and performs the voltage translation to the fixed output voltage. The control portion highlighted in blue is the portion of the circuit which controls the turn-on and turn-off of the power switches in such a way that the converter maintains a constant output voltage; it does this by sensing the output voltage and comparing it with a reference voltage.

For the context of this writing, only synchronous DC-to-DC converters are considered. Asynchronous converters use a diode in place of one of the FETs in order to simplify the design. As a result their power handling capability is limited. In synchronous converters power can actually move either from output to input or from input to output as they are bidirectional. Asynchronous converters can only move power from input to output.

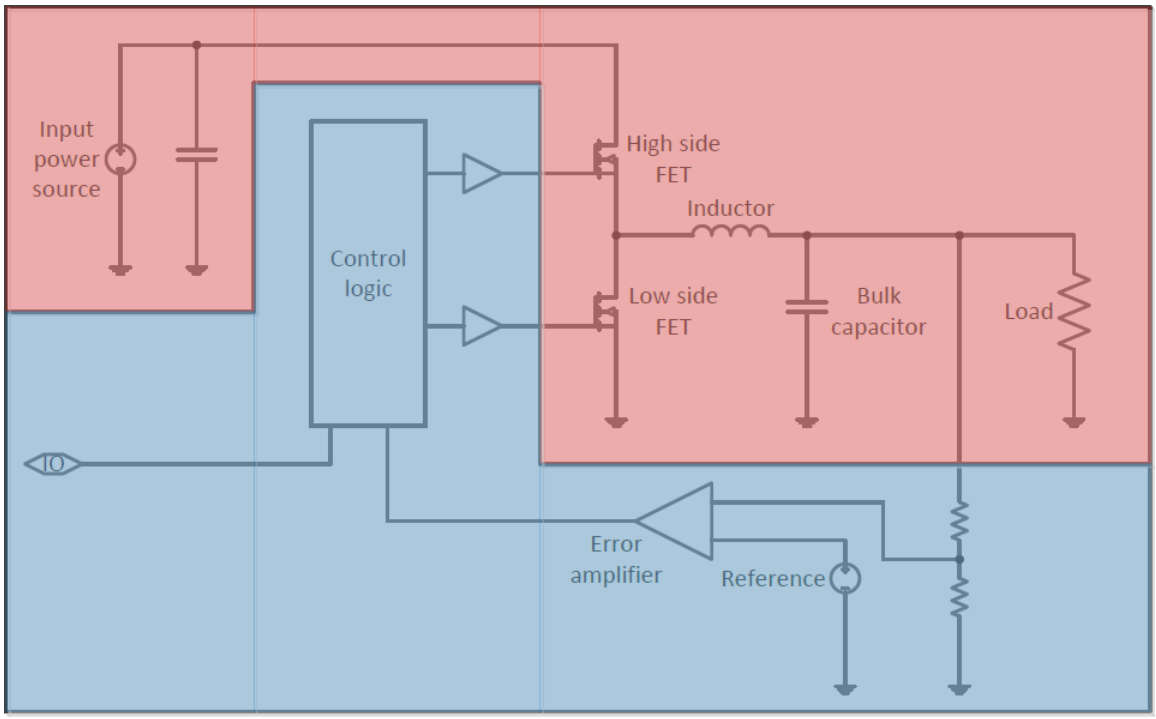

Figure 4. Typical Buck Converter Schematic

Energy is moved from the input power source to the output by storing it in an inductor and then subsequently discharged to the output. The ratio of time between energy being stored in the inductor and energy being released to the load will determine the output voltage.

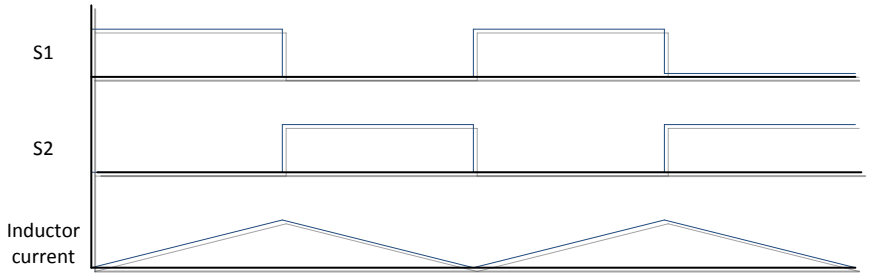

Figure 5. Graphs of DC-to-DC Converter Operation

In the buck converter the high side switch in the Figure 1 charges the inductor as shown in the graph above, the inductor current grows because the input voltage is greater than the output voltage. When the low side switch is activated and the high side switch

deactivated the inductor current begins to decrease as stored energy is released to the load.

In an ideal DC-to-DC converter the Equation that governs the output voltage is Equation (2) where D is the duty cycle of the high side switch S1 which can be expressed as Equation (3) where T_{S1} is the on-time for S1 and T_{S2} is the on-time for S2. For non-deal DC-to-DC converters the duty ratio must be adjusted slightly (higher than for an ideal converter) to compensate for losses within the converter.

$$V_{OUT} = D * V_{IN} \tag{2}$$

$$D = \frac{T_{S1}}{T_{S1} + T_{S2}} \tag{3}$$

Figure 6 shows how currents flow through the power path of a DC-to-DC converter. The output capacitor is charged while S1 is turned on, and discharged while S2 is turned on. It is intended to stabilize the output voltage and reduce voltage ripple.

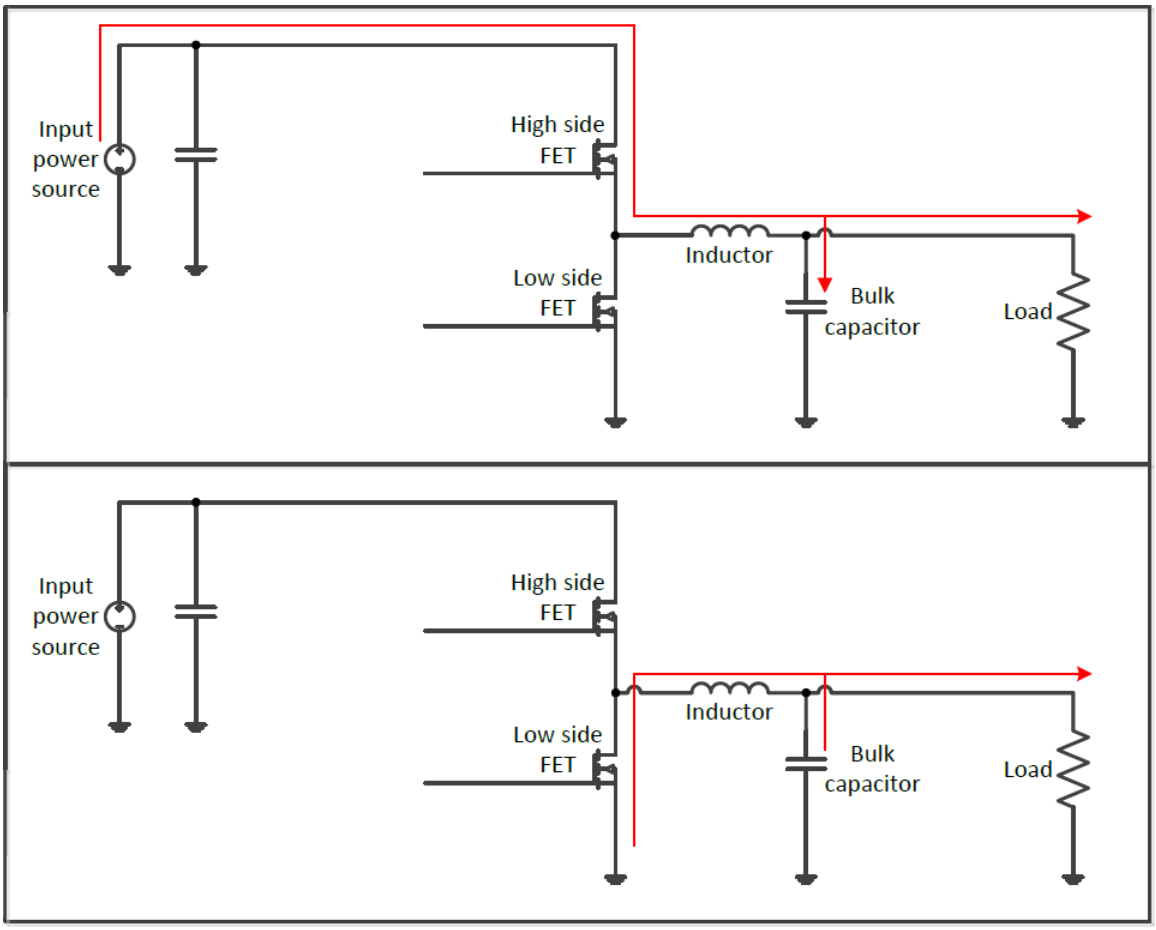

Figure 6. DC-to-DC Converter Power Path Current

Power Path

This writing will focus on three topologies which have the same input to output voltage relationship: the four-FET buck-boost, SEPIC, and ZETA DC-to-DC converter topologies. Each of these has the property that both the input and output voltage be positive, but the output voltage may be greater than, less than, or equal to the input voltage. To simplify the efficiency Equations below, it is assumed that all switches are FETs with the same properties of on state resistance and gate charge and all inductors are the same with identical DC resistances.

The Four-FET Buck-Boost Converter

The four-FET buck-boost converter is actually a hybrid of the buck and boost converter topologies. It consists of four FETs and a single inductor in its power path in addition to the usual input and output bulk capacitors. In this topology the switch node SW1 experiences voltages from ground to the input voltage, and the second switch node SW2 experiences voltages from ground to the output voltage; this is an advantage of this topology over the SEPIC and ZETA topologies.

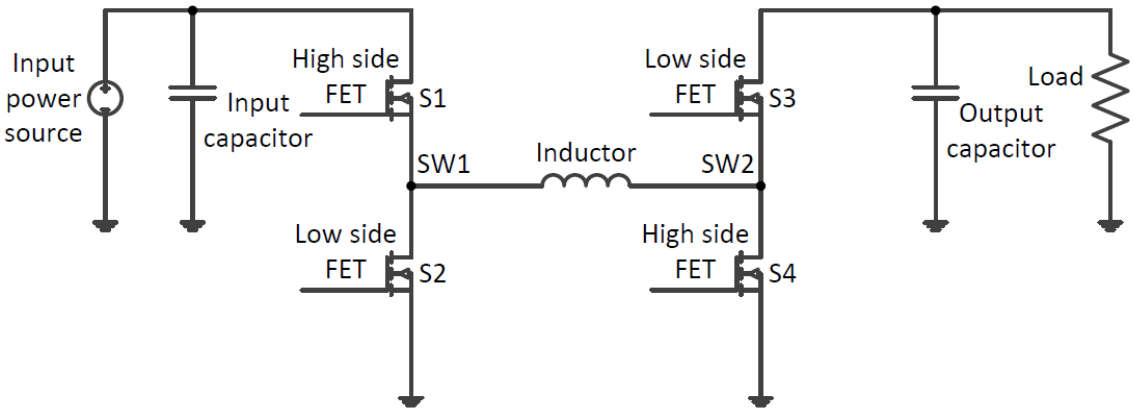

Figure 7. Four-FET Buck-Boost DC-to-DC Converter Power Path

In the four-FET buck-boost converter there are two ways that the converter can be operated. The first way is as a full buck-boost converter wherein all four switches are being switched all the time. The second way is a hybrid buck or boost wherein only two of the switches are being actuated at any given time depending on whether or not the input voltage than is greater or less than the input voltage.

When operated as a full buck-boost converter the relationship between duty ratio and output voltage is as shown by Equation (4) which means that for a duty ratio of ½ the input and output voltages are equal, for $D < 0.5$ the output voltage is less than the input voltage and for $D > 0.5$ the output voltage is greater than the input voltage. A big

advantage of this mode is that there is no distinction between buck and boost mode as there is in the hybrid mode which simplifies control loop design.

$$V_{OUT} = V_{IN} * \frac{D}{1 - D} \tag{4}$$

Figure 8 shows the flow of current through the four-FET converter in this mode of operation. The top half of Figure 8 shows the flow of current when the inductor is being charged through S1 and S4. The bottom half shows the flow of current when the stored energy in the inductor is being discharged to the load through S2 and S3.

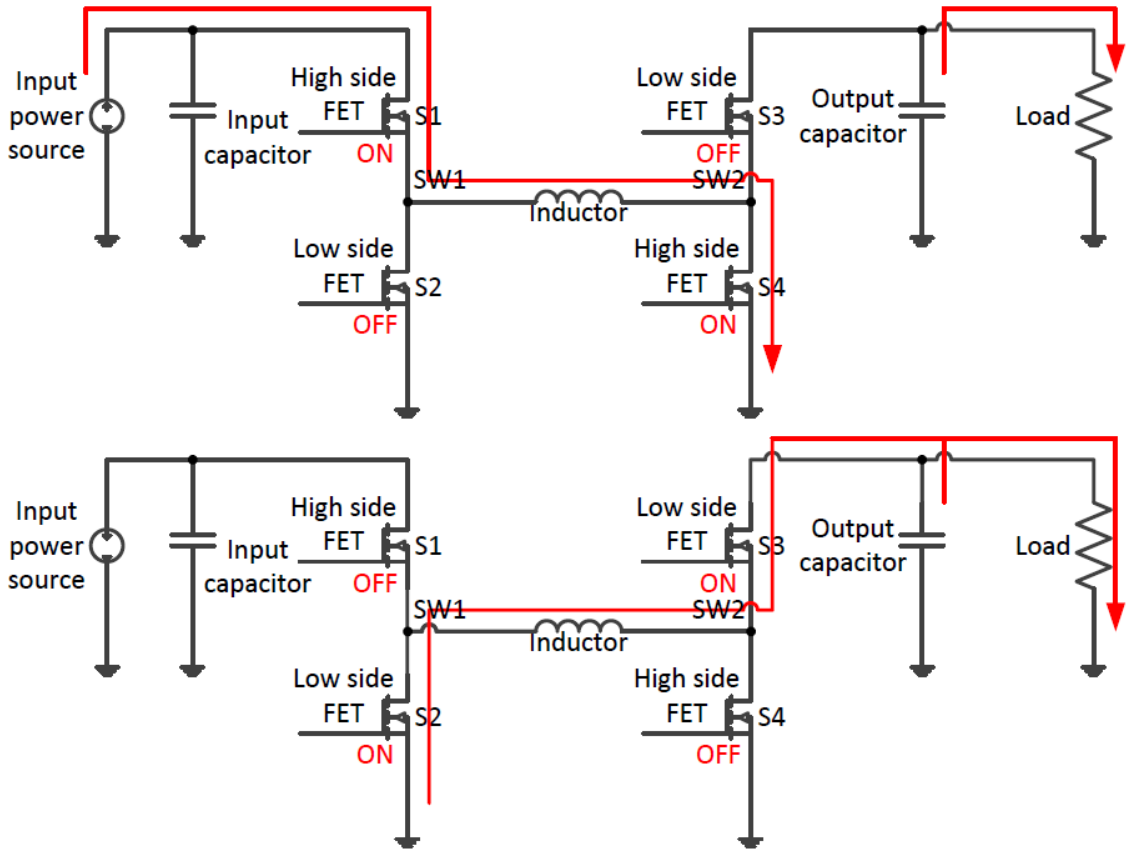

Figure 8. Current Flow in Full Buck-Boost Mode Four-FET Buck-Boost DC-to-DC Converter

In the full buck-boost mode of operation the power path losses are contributed to primarily by the inductor series resistance, on resistance of all four FETs, and the gate charge of all four FETs. The inductor losses can be estimated as Equation (5) where I_L is

the average inductor current and R_L is the series resistance of the inductor, for the full buck-boost the magnitude of the average inductor current I_L is actually the sum of the average input and output currents which can be expressed as Equation (6) The losses due to the on state resistance of the FETs can be expressed as Equation (7) where R_{FET} is the on state resistance of the FETs; this is because the current through the power path is at any given time flowing through two of the FETs. The FETs also dissipate energy due to their gate charge which is a representation of the energy required to turn the FETs on and off, this power dissipation can be expressed as Equation (8) where f is the switching frequency in Hz of the converter and Q_G is the gate charge of the FETs in coulombs (C).

$$P_L = I_L^2 * R_L \tag{5}$$

$$I_L = I_{IN} + I_{OUT} \tag{6}$$

$$P_{FET} = 2 * I_L^2 * R_{FET} \tag{7}$$

$$P_{FETSW} = V_{IN} * f * 2 * Q_G \tag{8}$$

There are additional sources of loss such as conduction during the transition between the on and off states of the FETs, FET off-state leakage, and magnetic saturation of the inductor at high currents which contribute to losses in the power path of a converter. To keep the analysis of the losses simple enough for comparison sake these additional losses will not be analyzed in this writing. Table 2 shows the Equations for losses in the four-FET converter running in full buck-boost mode which are covered in this writing.

Table 2. Equations for Losses in Four-FET Buck-Boost DC-to-DC Converter in Full Buck-Boost Mode

Source	Equation
Inductor series resistance	$P_L = I_L^2 * R_L$
FET on state resistance	$P_{FET} = 2 * I_L^2 * R_{FET}$
FET gate charge	$P_{FETSW} = V_{IN} * f * 2 * Q_G$

When operated in the hybrid buck or boost mode the four-FET converter is operated as either a buck converter when the output voltage is less than the input voltage or as a boost converter when the output voltage is greater than the input voltage. This mode has the benefit of improved efficiency as the losses are reduced from the full buck-boost mode. However, it has an issue when the input and output voltages are equal to one another. The converter can thrash between modes causing an increase in output noise.

Figure 9 shows the flow of current in this power path in buck mode and Figure 10 shows the flow of current in boost mode. This converter essentially puts the un-used FETs in a fixed state and only actuates the FETs that are needed during either buck or boost mode.

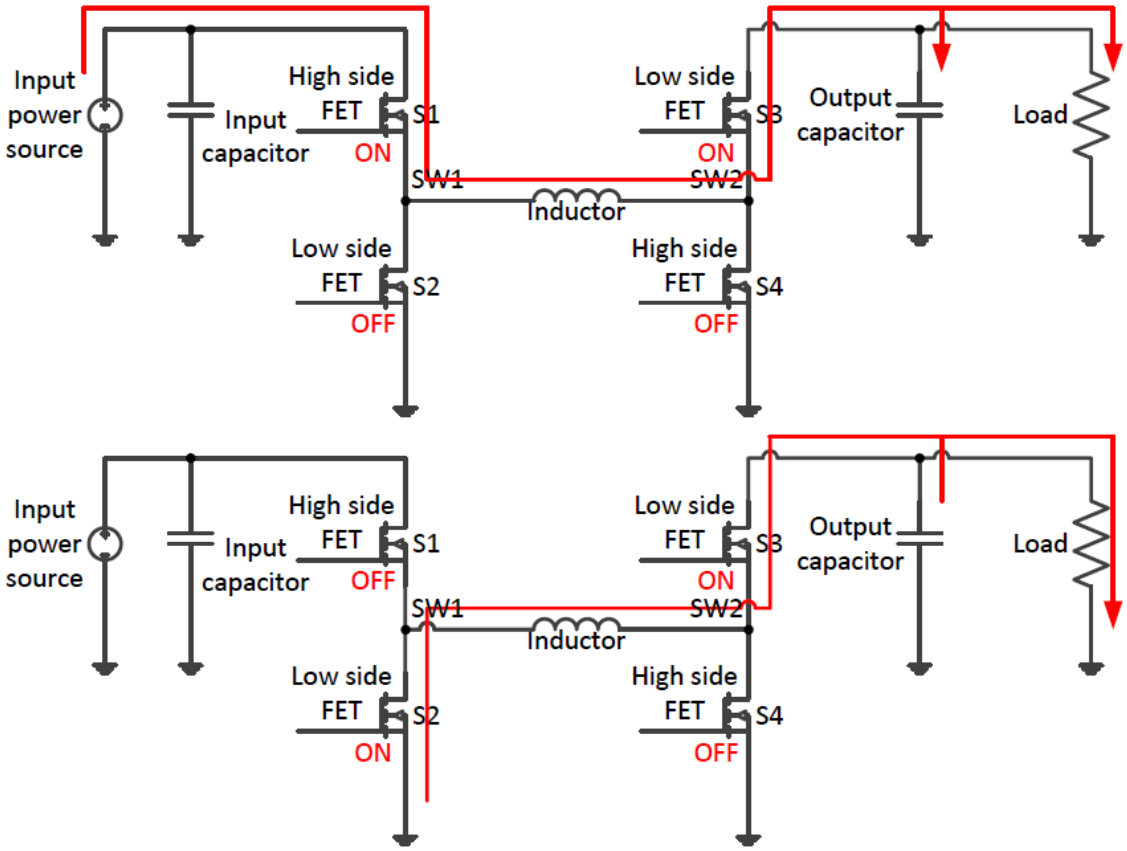

Figure 9. Current Flow in Buck Mode Four-FET Buck-Boost DC-to-DC Converter

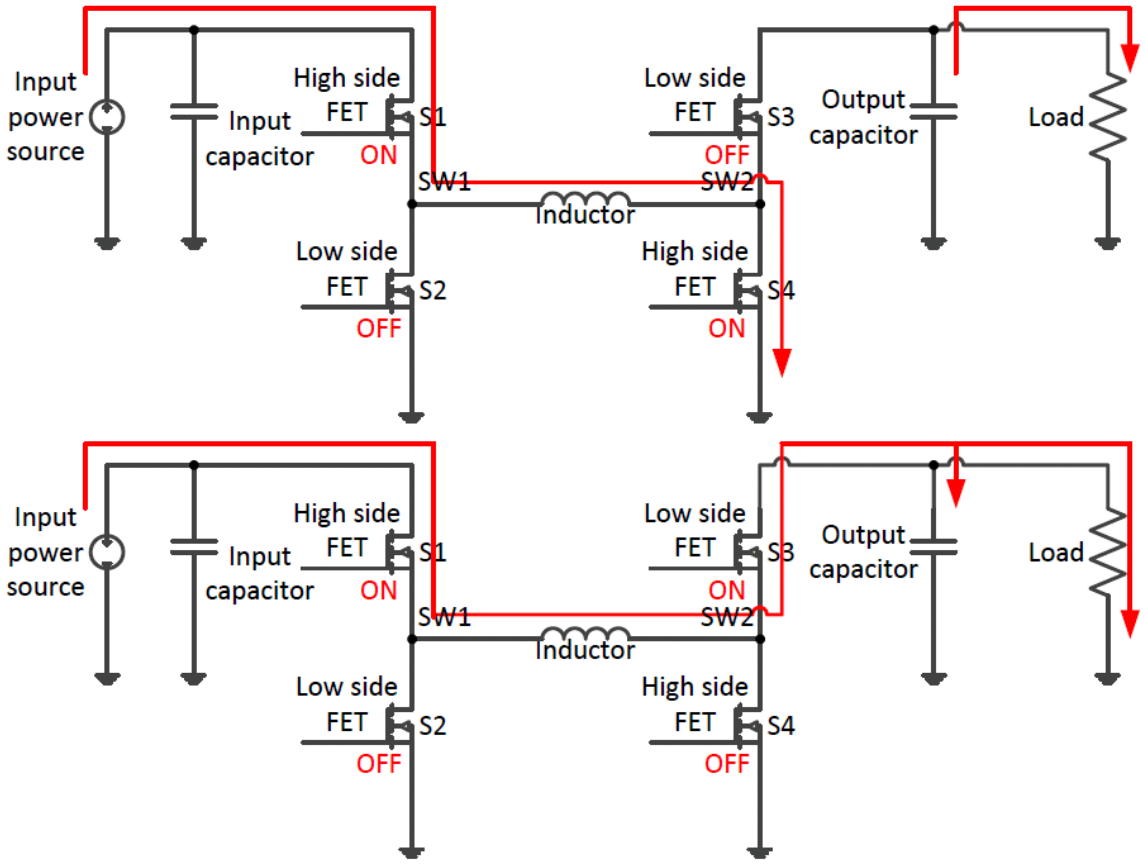

Figure 10. Current Flow in Boost Mode Four-FET Buck-Boost DC-to-DC Converter

In buck mode only S1 and S2 are actuated, S3 is left on and S4 is left off, making the converter appear very similar to a buck converter with an input to output relationship given as Equation (2) In boost mode only S3 and S4 are switched, S1 is left on and S2 is left off, making the converter look very much like a boost converter with an input to output relationship given by Equation (9) efficiency of the four-FET buck boost when operated this way is the same in either buck or in boost mode. Table 3 shows the equations for the losses of efficiency of the four-FET buck-boost DC-to-DC converter when operated in hybrid buck or mode. The key difference is that with ½ of the switches actually switching at any given time, the losses due to gate charge are cut in half. This especially come in to play during low current (low power) operation.

$$V_{OUT} = V_{IN} * \frac{1}{D} \tag{9}$$

Table 3. Equations for Losses in Four-FET Buck-Boost DC-to-DC Converter in Hybrid Buck or Boost Mode

Source	Equation
Inductor series resistance	$P_L = I_L^2 * R_L$
FET on state resistance	$P_{FET} = 2 * I_L^2 * R_{FET}$
FET gate charge	$P_{FETSW} = V_{IN} * f * Q_G$

The SEPIC Converter

A SEPIC converter has the same transfer function as a four-FET buck-boost converter with only two switches but two inductors and a DC blocking capacitor. With this type of converter, there is only one way to operate the converter unlike the four-FET design. The main drawback of this converter over the four-FET design is that the switch nodes SW1 and SW2 experience a greater range of voltages and the FETs must be able to withstand much higher voltages than they would in a four-FET configuration. In the SEPIC configuration SW1 must withstand voltages from ground to the sum of the input and output voltages, the second switch node SW2 must withstand a voltage range from the negative of the input voltage to the output voltage. The reason for this is that the average voltage across both inductors must be zero. Node SW1 experience a voltage of 0V for time $D * T$ and in order to keep the average at 0 by Equation (10) the voltage V_{SW1} must equal $V_{out} + V_{in}$ when substituting Equation (11). The same logic can be applied to show that the voltage swing on SW2 goes from $-V_{in}$ to V_{out}. Figure 11 shows the power path of the SEPIC converter.

$$\frac{D * (V_{in} - 0) + (1 - D) * (V_{in} - V_{sw1})}{2} = 0 \tag{10}$$

$$D = \frac{V_{out}/V_{in}}{1 + V_{out}/V_{in}} \tag{11}$$

Another design consequence of the SEPIC converter which also applies to the ZETA converter is that, for switch S2, floating drivers must be used if S2 is an n-channel FET, or a p-channel FET must be used in order to be able to turn this switch on and off. In the case of a zeta converter this is true for S1. The drawings of both the SEPIC and zeta converters in this chapter show a p-channel for S2 in the SEPIC converter and for S1 in the zeta converter.

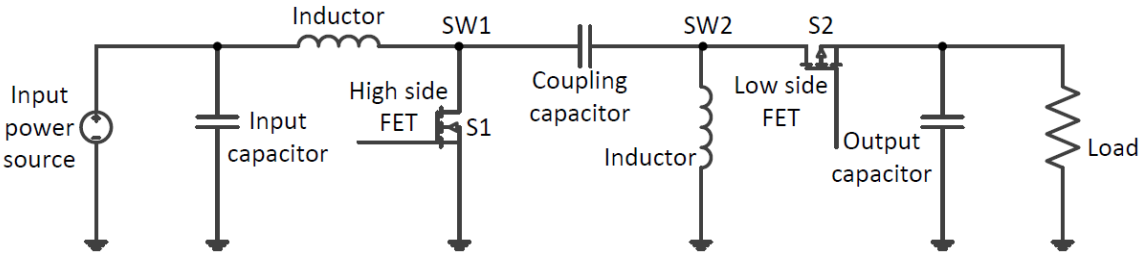

Figure 11. SEPIC Converter Power Path

The SEPIC converter always operates in full buck-boost mode and its transfer function and characteristics are otherwise the same as for the four-FET buck-boost when operated in full buck-boost mode. One design constraint of the SEPIC is that the coupling capacitor must be sized sufficiently large in order to prevent oscillations of the output voltage. Another design note about this converter is that the two inductors may be coupled for improved response time when designing the control circuits.

The current flow in a SEPIC converter is somewhat non-intuitive due to the DC blocking capacitor. The SEPIC converter operates in two phases; in the first phase energy is taken from the input power source and stored in the inductors, in the second phase that energy is released to the load. Bulk capacitors supply energy to the load during the first phase. During the first phase, S1 is on and current is flowing to ground through S1 from

the first inductor and the DC blocking capacitor. Output current is being supplied by the output bulk capacitor. During the second phase, S2 is on and current is flowing from input to output and from ground to output through the second inductor. Figures 12 and 13 shows the current flows in a SEPIC converter. Note that the input current in the SEPIC is being drawn during both phases.

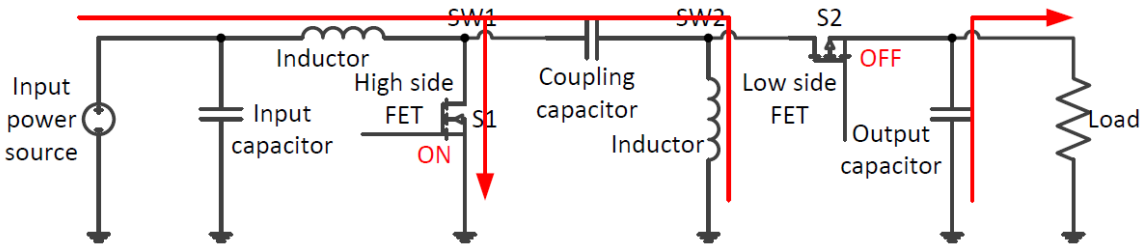

Figure 12. SEPIC Converter Current Flow During Phase 1

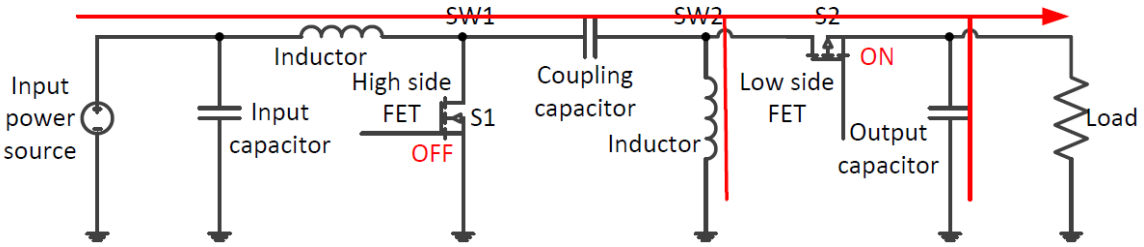

Figure 13. SEPIC Converter Current Flow During Phase 2

Sources of power loss in the SEPIC power path are the same as those for a four-FET converter with the addition of the coupling capacitor; the Equations are however somewhat different due to the different number of FETs and inductors. The losses in the inductors follow the same Equation as for the inductor in the four-FET buck-boost converter with the exception that there are two inductors. The FETs also follow the same Equations with the exception that there are just two FETs. The losses in the coupling capacitor are less straightforward as they depend on the capacitance of the coupling capacitor and the RMS current through the capacitor. Typically the losses in the coupling

capacitor are less than those of the other components in the system. Table 4 shows the Equations for loss in a SEPIC converter.

Table 4. Losses in a SEPIC Converter

Source	Equation
Inductor series resistance	$P_{L1} = 2 * I_{L1}^2 * R_{L1}$ $P_{L2} = 2 * I_{L2}^2 * R_{L2}$
FET on state resistance	$P_{FET1} = I_{L1}^2 * R_{SW1}$ $P_{FET2} = I_{L2}^2 * R_{SW2}$
FET gate charge (applies to each FET)	$P_{FETSW} = \frac{1}{2} * V_{IN} * f * Q_G$

Typically, if the same inductors and FETs are used, a SEPIC converter will be slightly more efficient than a four-FET buck-boost converter due to only having two FETs which saves power in both FET resistances and reduces switching losses.

The Zeta Converter

The zeta converter is the inverse of the SEPIC converter. It is a consequence of the fact that the SEPIC converter is bi-directional and as such the zeta converter can be thought of as a SEPIC converter with the input and output swapped and the high side and low side FET assignments reversed. All of the characteristics of losses shown in Table 4 and the transfer function for the SEPIC converter apply to the zeta converter as well. Figure 14 shows the power path of the zeta converter.

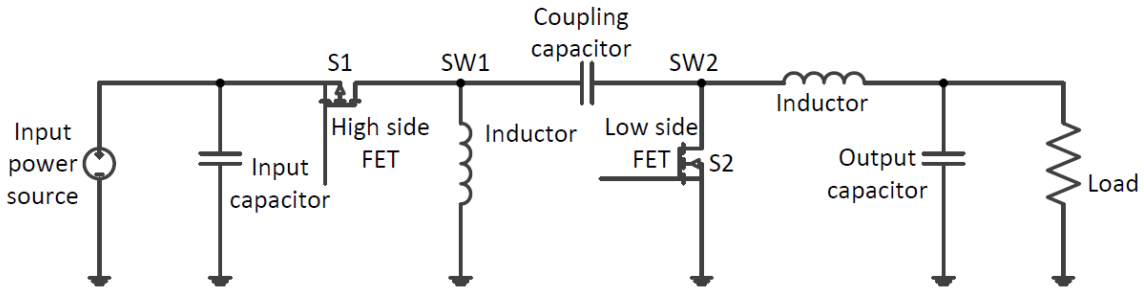

Figure 14. Zeta Converter Power Path

The chief difference between the zeta and SEPIC converters has to do with the nature of the current at the input versus the output. The SEPIC converter has an inductor in series with the input which provides a filter for the input current and reduces the switching noise radiated to the input. The zeta converter has the series inductor at the output which provides the same filtering but on the output side.

Operation of a zeta converter is similar to a SEPIC. The high side and low side FETs are reversed along with the circuit direction: low side FET is on the left and high side FET is on the right. The relationship between duty cycle, input voltage, and output voltage is the same as for a SEPIC converter. The operation of a zeta converter is in two phases, the first phase is a charging phase where energy is taken from the input power source and stored in the two inductors. The second phase is where the energy is then delivered to the output load. A bulk capacitor acts to supply energy to the output load during the first phase. Figures 15 and 16 show the flow of current in the zeta converter during phase 1 and phase 2 respectively. During the first phase current flows from the input power source through S1 into both the left side inductor and DC blocking capacitor and right side inductor to the load. During the second phase the input current is cut off and S2 is closed, current then flows from ground through S2 into the DC blocking capacitor (moving right to left now) and also through the right side inductor to the load. One feature of the Zeta converter is that the output current is not interrupted which can reduce output noise.

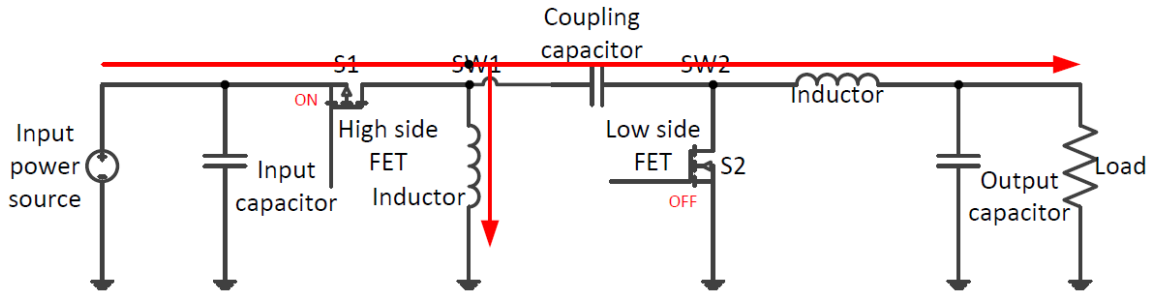

Figure 15. Current Flow in a Zeta Converter During Phase 1

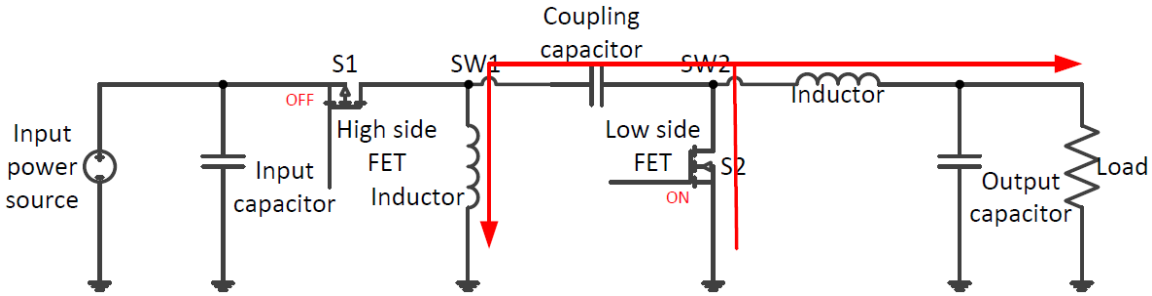

Figure 16. Current Flow in a Zeta Converter During Phase 2

Control Scheme

The control portion of a DC-to-DC converter is primarily responsible for regulating the output voltage of the converter as well as a number of secondary functions. Some of the secondary functions include soft start, an output power-good indicator, and an input under voltage lockout. This chapter is only concerned with the primary responsibility of the control which is regulation of the output voltage. There are three types of control circuits commonly used in DC-to-DC converters; voltage mode, current mode, and constant on-time.

The basic constituents of a regulator control loop are the reference voltage, the error amplifier, and the PWM/logic circuit. The reference voltage is used as a fixed known reference to compare the output voltage against. The error amplifier performs the comparison of the output voltage or a scaled version of it by way of a resistor divider to the reference voltage and provides a signal to the PWM/logic circuit. In the constant on-

time control scheme the error amplifier is actually a comparator instead of an amplifier. The PWM/logic circuit controls the power path FETs through some FET drivers based on input from the error amplifier. Figure 17 shows a generic control loop for a DC-to-DC converter with the components mentioned above.

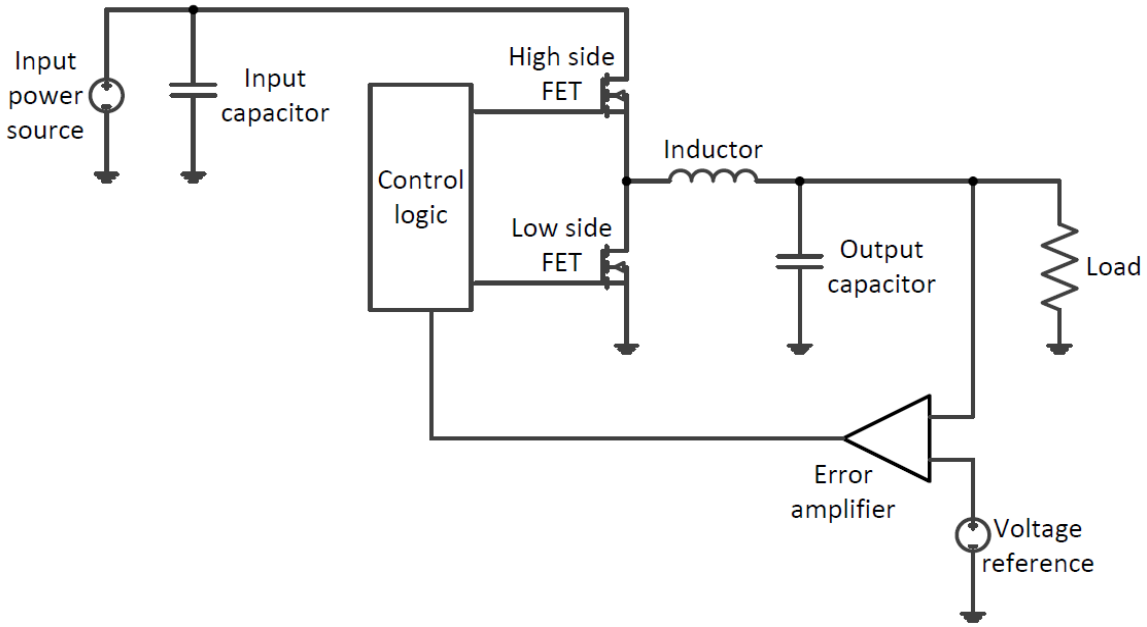

Figure 17. Diagram of a Generic Control Loop for a DC-to-DC Converter

This writing does not focus heavily on DC-to-DC converter control loops; however, they are shown to illustrate how dual-input DC-to-DC converters can be controlled and then highlight the challenges associated with controlling them in various configurations with a few common control loop types.

Voltage Mode Control

Voltage mode control is the simplest method for controlling the output voltage of a DC-to-DC converter. The voltage mode control loop uses an integrator for the error amplifier which can be built from an opamp or an operational transconductance amplifier (OTA). The integrator compares the feedback voltage with a reference and based on the

error polarity and magnitude the output, also known as the control voltage, will track up or down to compensate for error in the output with respect to the reference voltage. The control voltage is compared with a PWM saw-tooth waveform which produces a digital signal much like a clock whose duty cycle is controlled by the magnitude of the control voltage. The duty cycle of this clock signal is the duty cycle of the high side and low side FETs in the converter power path. The clock signal is an input either directly to the power path FETs or to FET drivers which turn the power path FETs on and off.

Current Mode Control

Current mode control adds a second and inner control loop to the basic voltage mode control scheme which senses the inductor current and feeds that information to the error amplifier. This has the effect of turning the inductor into a current source in the control loop transfer function which improves stability and eases the requirements on compensation.

Constant On-Time Control

Constant on-time control works in a very different fashion that the more traditional voltage and current mode control schemes. This control mode replaces the error amplifier with a comparator which compares the converter output voltage with a reference voltage. Any time the output voltage goes below the reference level the comparator changes its output state which triggers the control logic to switch on the high side FET for a fixed on-time, otherwise the low-side FET is turned on unless discontinuous current mode is used. This control mode often does not require compensation, however, the logic behind it can be far more complicated than in voltage and current mode converters. Another advantage of the control scheme is that it offers a

faster transient response than the others as the converter can compensate for loading changes on a cycle-by-cycle basis.

CHAPTER THREE: DUAL-INPUT DC-TO-DC CONVERTER POWER PATHS

In most applications where two power sources are being used to supply power to a single load, a pair of DC-to-DC converters will be placed in parallel. The subject of this chapter is to show alternative topologies for achieving this using a single power path. These alternate topologies include a dual-input four-FET buck-boost converter, two types of dual-input SEPIC converters, and a dual-input zeta converter.

The general theory of operation for these converters is that power is drawn alternately from each input power source. In a traditional DC-to-DC converter there are two phases: one where energy is drawn from the input and stored in an inductor: and a second where that energy is released from the inductor to the load as shown in Figure 18. In these topologies a third phase is added where power is drawn from the second input power source. Figure 19 shows the addition of a third phase for the dual-input converter. During the phase where power is being drawn from the input power source(s) a bulk capacitor at the load supplies power to the load, this is shown in the detailed schematics that follow.

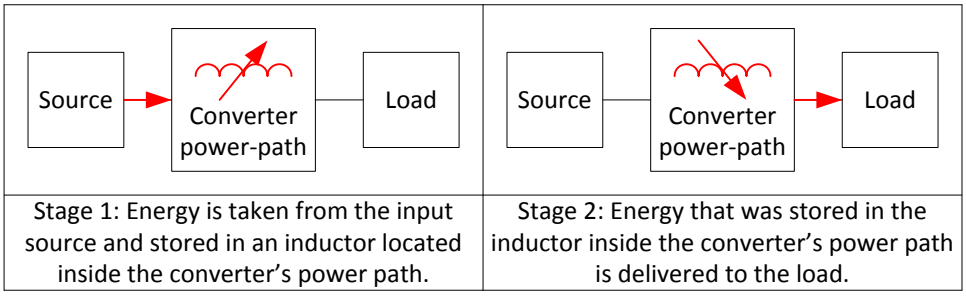

Figure 18. Charge and Discharge Stages in a Typical DC-to-DC Converter

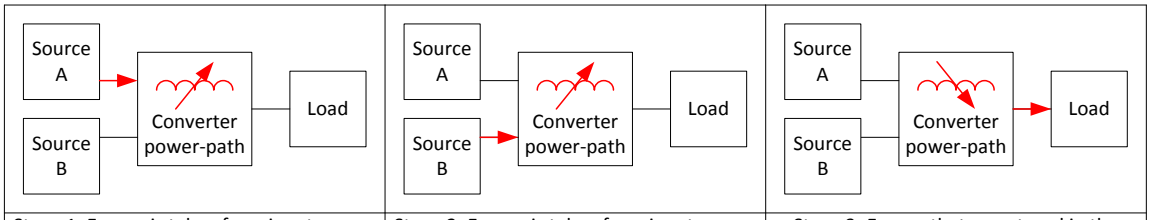

Figure 19. Charge and Discharge Stages in a Dual-Input DC-to-DC Converter

Because there are three phases of operation there are two ways in which they can be combined during the cyclic operation of a DC-to-DC converter. One way is to draw the input power from both sources during the same cycle which will be referred to as in-cycle operation. The other way is to draw energy from each source every other cycle, this will be referred to as cycle-by-cycle operation. Table 5 shows the sequences of these phases for the dual-input DC-to-DC converters covered in this writing. Each series of phases repeats continuously as shown during operation of the converter.

Table 5. Table of Operation for Dual-Input DC-to-DC Converters

In-cycle operation	
1. Input A	Energy is drawn from input source A and stored in the inductor(s)
2. Input B	Energy is drawn from input source B and stored in the inductor(s)
3. Output	Energy is discharged from the inductor(s) to the load
Cycle-by-cycle operation	
1. Input A	Energy is drawn from input source A and stored in the inductor(s)
2. Output	Energy is discharged from the inductor(s) to the load
3. Input B	Energy is drawn from input source B and stored in the inductor(s)
4. Output	Energy is discharged from the inductor(s) to the load

In-cycle operation has the advantage of moving the fundamental frequency of the current noise radiated to the input source to a higher frequency than in cycle-by-cycle operation. This is because in-cycle operation pulls a pulse of current from the source at

the same frequency that the converter is operating, whereas cycle-by-cycle operation pulls current as one half of the frequency of operation of the converter. The advantage for out-of-cycle control is that there are only two phases used per cycle which causes fewer off-on and on-off transitions per cycle which leads to improved efficiency due to lower switching losses when compared to in-cycle operation.

To make the comparison between each one, all simulations are done with the same assumptions about the characteristics of the converters; those assumptions are listed below in Tables 6 and 7. Each converter has been designed around a common set of input and output requirements in order to provide a fair comparison of each topology. These requirements are that the inputs are 12V and 5V, the output is 3.3V, and approximately half of the input current is drawn from each source.

The FET gate charge is included for the power path simulations to capture its impact on efficiency between in-cycle and cycle-by-cycle operation. The gate charge is modeled by placing a constant current load in the 12V input to the converter with a current draw that matches the power draw of the FET gate charge for the number of FETs, switching pattern, and switching frequency of each power path. The Equation used to determine this current is shown in Equation (12) where N_{SW} is the number of FETs that switch in a given cycle, F_{SW} is the switching frequency, and Q_G is the gate charge of each FET.

$$I_{CHG} = N_{SW} * F_{SW} * Q_G \tag{12}$$

Table 6. Assumptions for Component Properties

Inductor inductance	2µH
DC blocking capacitor capacitance	220µF
Input capacitor capacitance	47µF
Output capacitor capacitance	100µF

Table 7. Assumptions for Component Parasitic Properties

FET on resistance	10mΩ
FET off resistance	100MΩ
FET body diode on resistance	10mΩ
FET body diode forward voltage	350mV
FET body diode off resistance	100MΩ
FET gate charge	20nC, modeled with constant load
Inductor DC resistance	10mΩ
DC blocking capacitor series resistance	10mΩ
Input capacitor series resistance	1mΩ
Output capacitor series resistance	1mΩ

Traditional Approach

Typically when a load must draw power simultaneously from two power sources the solution is to take two independent DC-to-DC converters and run them in parallel. In the case of buck-boost regulators which are the focus of this writing, the configuration would look like what is shown in Figure 20 implemented with four-FET buck-boost converters. Because the two converters are synchronous (power can flow in either direction) care must be taken that one converter does not begin to conduct in the reverse direction. This reverse flow can happen if one converter is trying to move the output voltage even slightly higher than the other. As the higher output voltage converter sources current from the input power supply to raise the voltage, the other converter will sink current back to its input power supply to lower the output voltage. Preventing

reverse conduction in this situation can require complex current sensing circuitry at the output of one or both converters.

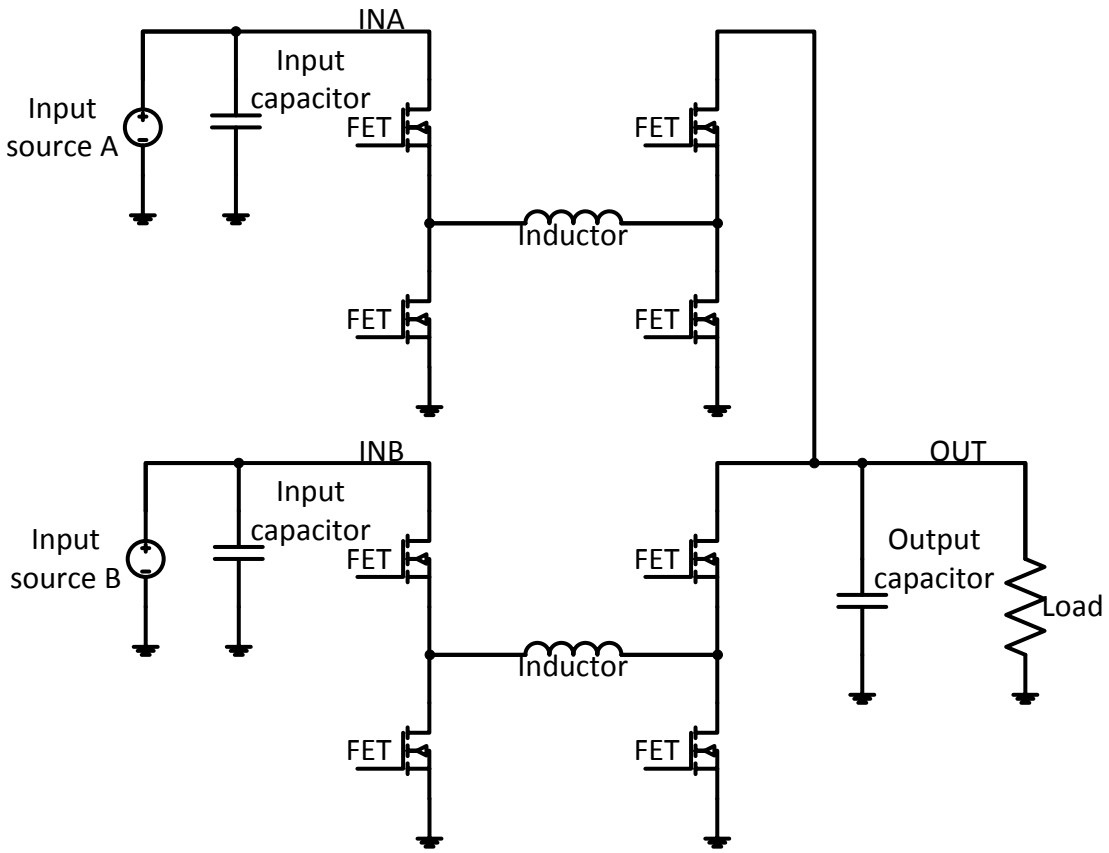

Figure 20. Two Four-FET Buck-Boost DC-to-DC Converters in Parallel

In the traditional approach, the operation of the two converters does not need to be synchronized. There are, however, benefits to synchronizing both converters. If each converter operates out of phase with the other (one is pulling energy from the input power source while the other is pushing energy out to the load), the output voltage ripple can be greatly reduced. This type of operation is sometimes referred to as dual phase operation. Depending on the control scheme used to prevent reverse current, synchronization of the converters may be beneficial or even necessary for the operation of the control loop that regulates the output current.

The traditional approach of paralleling multiple converters can also be achieved using SEPIC and zeta converters as shown in Figures 21 and 22, respectively. These configurations share the same concerns with reverse current flows as mentioned previously. The differences in the design considerations between using two four-FET buck-boost converters and two SEPIC or zeta converters are the same as those for single input converters. Most commonly, however, the configuration of two four-FET buck-boost converters is chosen for the applications mentioned in this writing for the simplicity of FET drivers required to drive the four-FET buck-boost compared to the SEPIC and zeta converters.

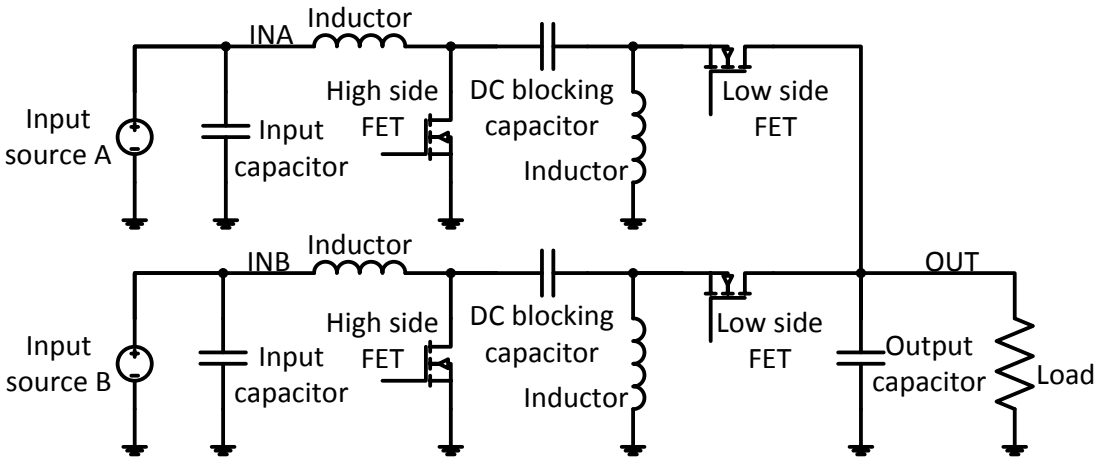

Figure 21. Two SEPIC DC-to-DC Converters in Parallel

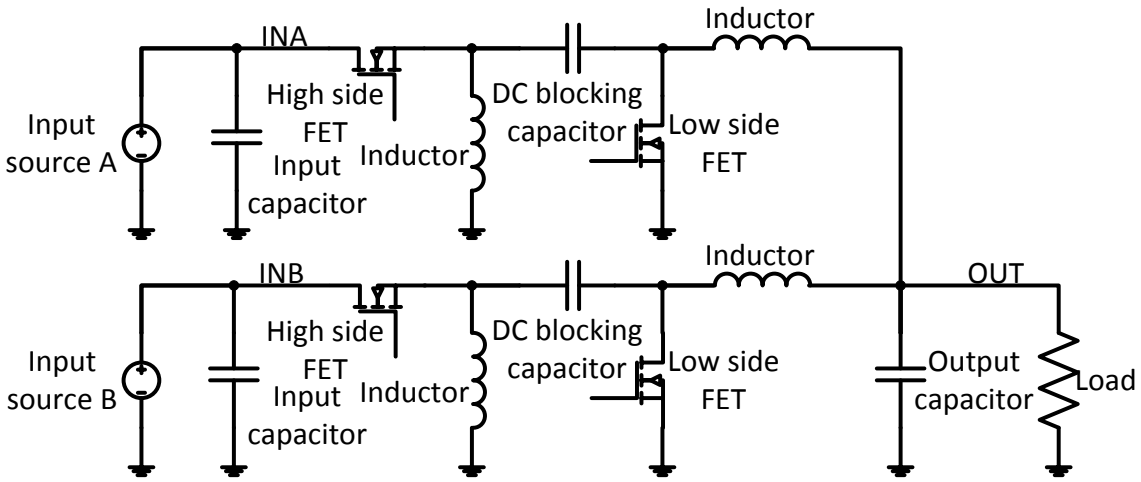

Figure 22. Two Zeta DC-to-DC Converters in Parallel

One advantage of the traditional approach that is not shared by the dual-input converter is that there is no penalty for supporting either input voltage being greater than the other. This is because each input is tied to an independent power path and is therefore fully isolated from the other input so long as reverse current flow does not occur. The dual-input topologies as explained below do have a penalty if supporting the characteristic that either input power source may be at a higher voltage than the other source.

Dual-Input Four-FET Buck-Boost

The dual-input four-FET buck boost converter achieves the dual-input function using a single power path as opposed to the traditional approach which uses two power paths. The power path for a dual-input four-FET buck-boost converter is shown in Figure 23 The difference from the single input four-FET buck boost is the addition of the extra input transistor(s) to connect the second input power source.

The purpose of the dual FETs SW1 and SW2 are to provide reverse blocking during the time when SW1 and SW2 are disabled and SW3 is enabled, at this time the voltage at node SW1 is the same as that of node INA, if the voltage at INA is greater than

the voltage at INB then a single FET in place of SW1 and SW2 would be reverse biased and would begin to conduct through its body diode. This would effectively shunt current from the input source with the higher voltage to the input source with the lower input voltage which would potentially damage the input sources and the converter. By using back to back FETs connected as shown the body diodes are opposing each other and reverse conduction when the FETs are turned off is prevented; additionally by having dual FETs on input B, the voltage of input A may be the same or higher than the voltage of input B. If back to back FETs were used on both input A and input B, then either input could be higher than the other. The drawback of using back to back FETs in that they will contribute to higher conduction losses due to on-state resistance and higher switching losses due to the increase in gate charge.

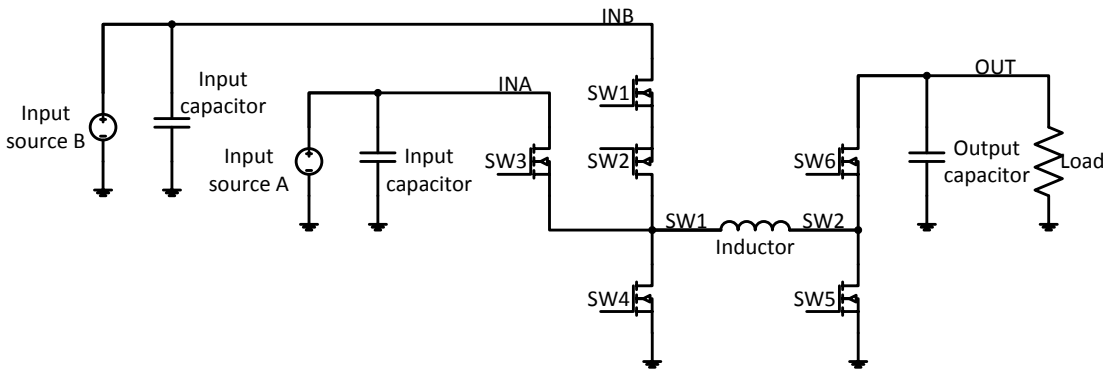

Figure 23. Dual-Input Four-FET Buck-Boost Converter

This converter operates by storing energy from each of the two input sources in the inductor and releasing that energy to the output load. Figures 24, 25, and 26 show the flow of current through the converter during the three states of the converter: charging from input A, charging from input B, and discharging to the output load. Either cycle-by-cycle or in-cycle operation may be used as described earlier in this chapter.

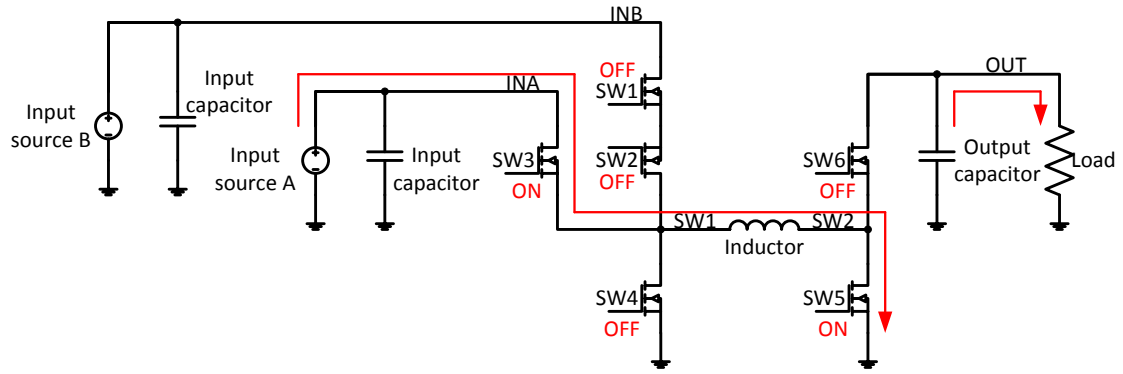

Figure 24. Dual-Input Four-FET Buck-Boost Charging From Input A

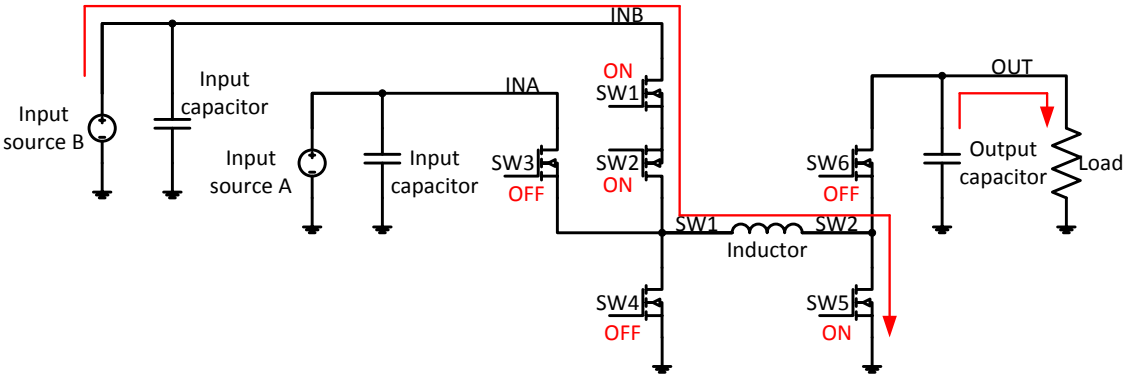

Figure 25. Dual-Input Four-FET Buck-Boost Charging From Input B

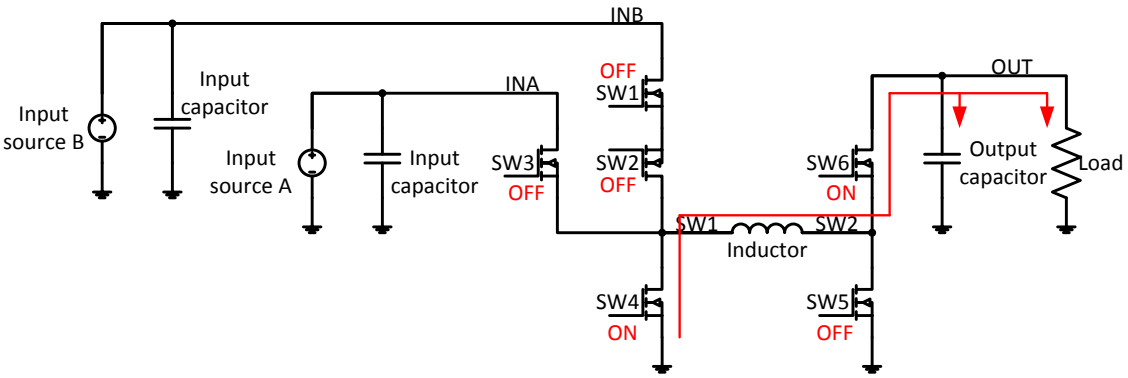

Figure 26. Dual-Input Four-FET Buck-Boost Discharging to the Output Load

Operational waveforms of this converter are shown in Figure 27 detailing what operation would look like for in-cycle mode operation. Figure 28 shows cycle-by-cycle operation. During a charging phase from either input source the voltage across the inductor will cause the current to steadily increase, during this time energy is being stored in the magnetic field of the inductor. During an output phase the voltage across the

inductor is reversed and the current begins to decrease as the stored energy is released to the output load.

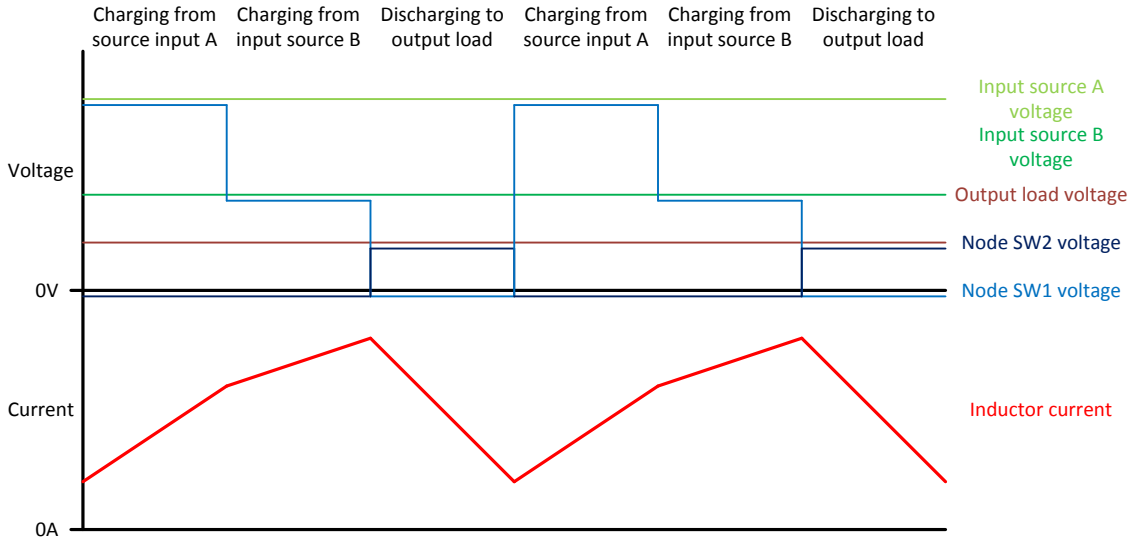

Figure 27. Dual-Input Four-FET Buck-Boost In-Cycle Operational Waveforms

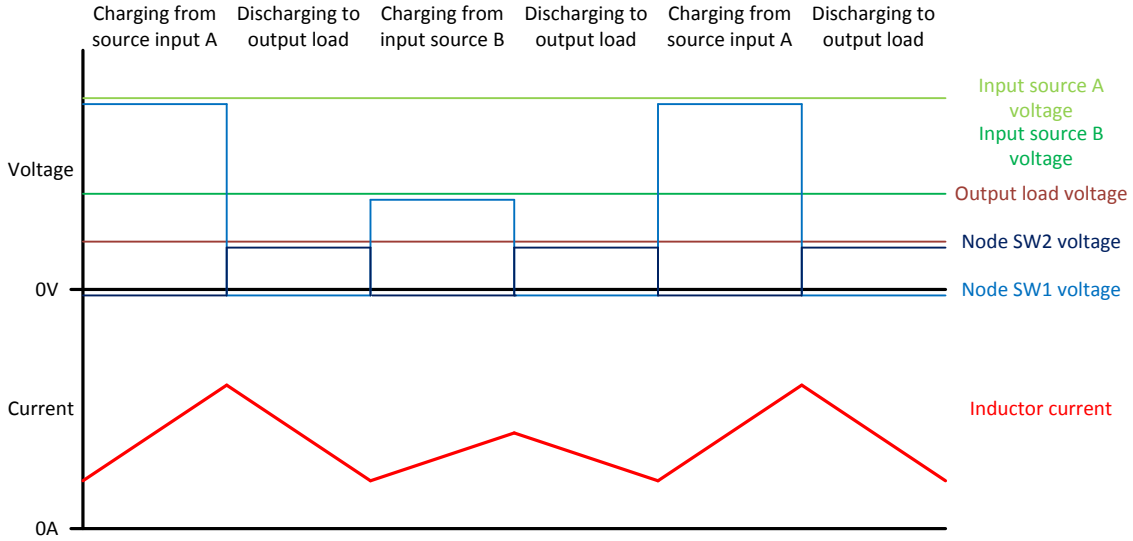

Figure 28. Dual-Input Four-FET Buck-Boost Cycle-By-Cycle Operational Waveforms

Operational demonstration of the dual-input four-FET buck-boost converter is done using LTSpice as a circuit simulation engine. Figure 29 shows the SPICE schematic used to prove operation of the converter with 12V and 5V inputs supplying ~3.26V to a

2.728A load. This simulation demonstrates in-cycle operation of the dual-input four-FET buck-boost converter. Ideal circuit elements are combined with some parasitic values to create a semi-realistic simulation of the power path of the converter as if constructed using MOSFETs. In-cycle operation is used for the purposes of this simulation. The resulting efficiency for this power path (neglecting gate charge effects) is approximately 95% with an output load of 2.728A (8.89W).

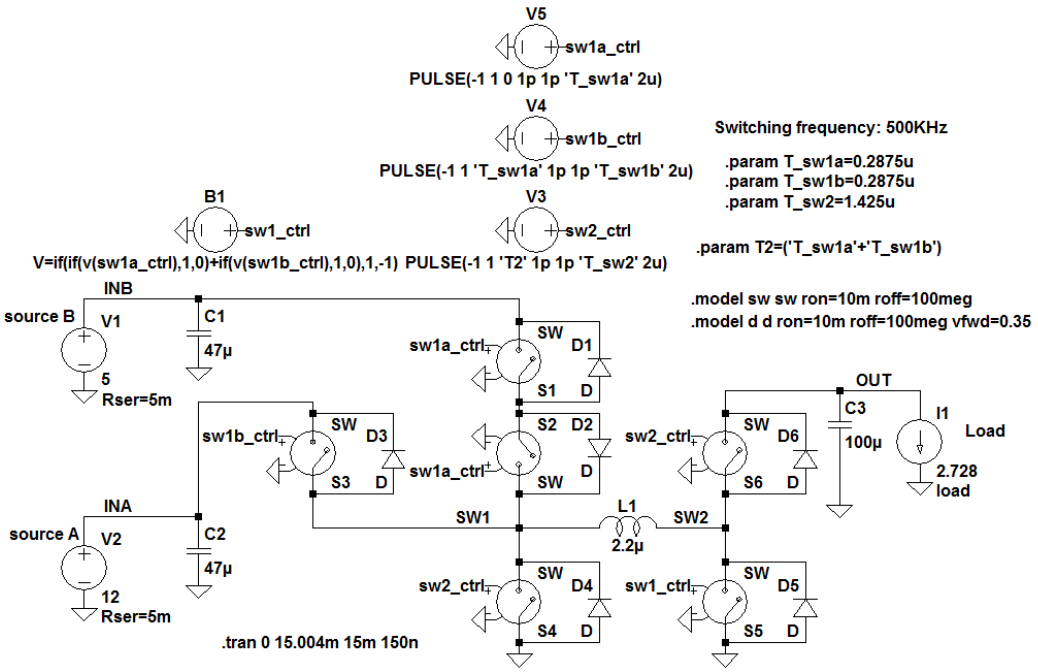

Figure 29. SPICE Circuit for Conceptual Verification of Dual-Input Four-FET Buck-Boost Converter

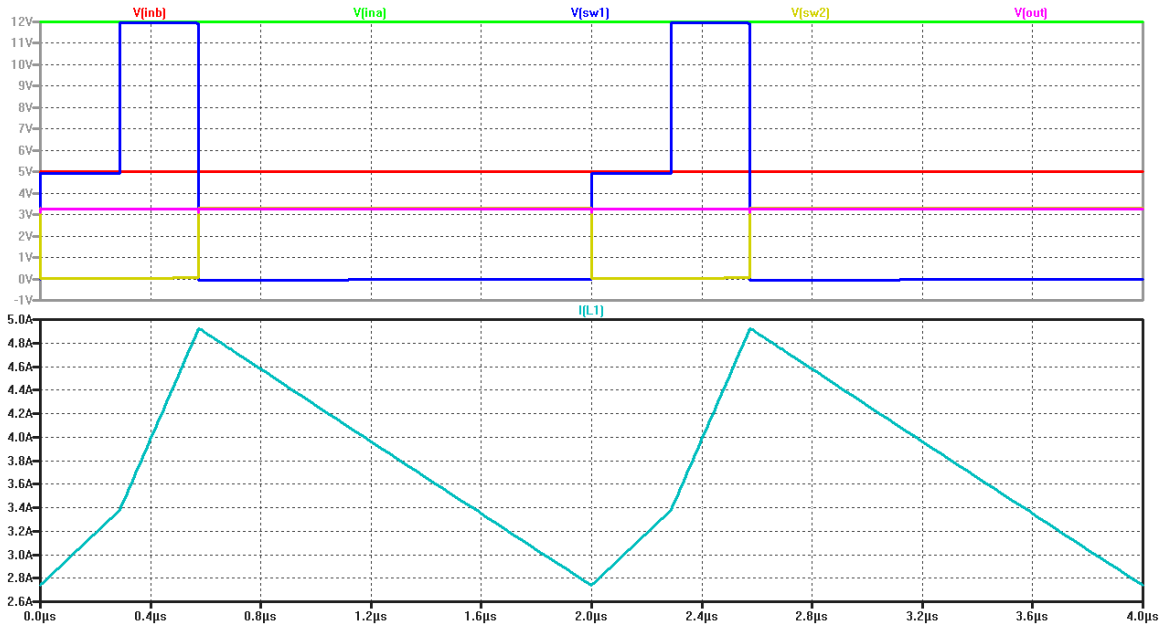

Figure 30. SPICE Waveforms for Conceptual Verification of Dual-Input Four-FET Buck-Boost Converter

An additional simulation is done to demonstrate that the converter continues to regulate the output voltage and maintains the input current sharing ratio across different loads. The simulation is done using cycle-by-cycle operation and a voltage mode control loop regulates the output voltage. Figure 31 shows the results of this simulation. Simulation conditions are the same as in the previous simulation with the difference being that the load steps from 1A to 5A in 1A steps each lasting 1ms. Figure 31 shows the output voltage of the dual-input four-FET converter during this test, the graph does show that the control loop used for this test is not precisely tuned, however, this does not impact the results for the power paths efficiency or it's input current sharing.

Table 8. Dual-Input Four-FET Regulation Test Results

Output current (A)	Output voltage (V)	Input current A (A)	Input current A	Input current B (A)	Input current B	Efficiency
1	3.299	0.198	50%	0.199	50%	98%
2	3.298	0.397	49%	0.412	51%	95%
3	3.298	0.616	50%	0.618	50%	94%
4	3.298	0.837	50%	0.839	50%	93%
5	3.298	1.053	49%	1.083	51%	90%

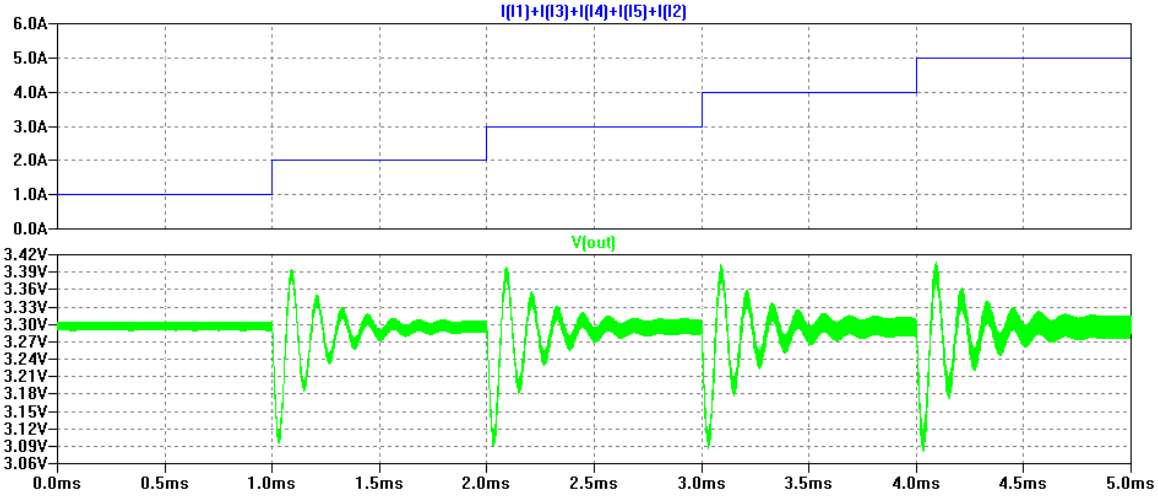

Figure 31. Dual-Input Four-FET Regulation Test Output Voltage Waveform

Dual-Input Zeta Converter

The zeta converter can be converted to a dual-input converter by using the same principles as those applied to the four-FET buck-boost. A second input FET path is added to connect an additional input power source. Figure 32 shows the dual-input zeta converter power path. Due to the inherent buck-boost nature of the zeta (and SEPIC) converter there is no distinction between buck or boost and buck-boost operation for this type of converter which simplifies the control requirements when using this power path topology.

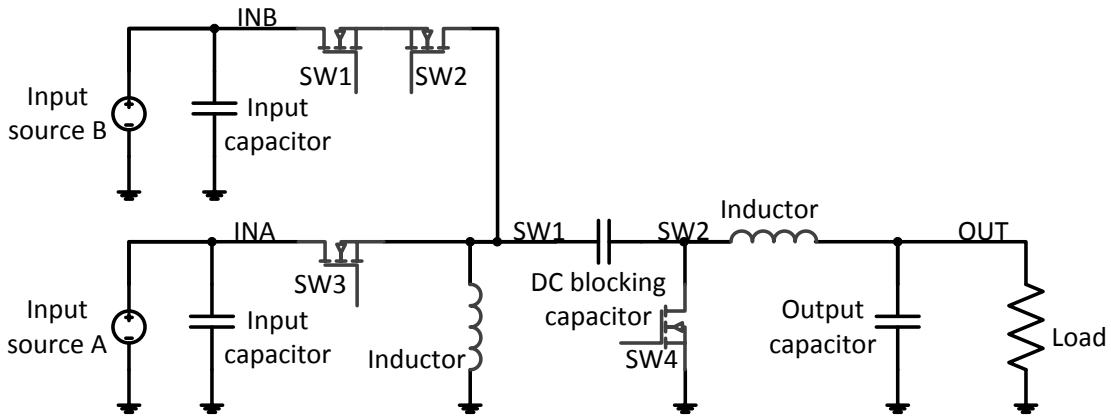

Figure 32. Dual-Input Zeta Converter

Input source A in this example may be the same as or higher voltage than input source B. For the same reasons as described in the section on the dual-input four-FET buck-boost converter, a second FET is added to one of the input legs to prevent current from flowing from input source A to input source B. To remove the input voltage restriction a second FET can be added in line with input source A (next to SW3).

Operation of the dual-input zeta is the same as for the dual-input four-FET buck-boost. There are three possible states or phases of operation. Charging from input source A, charging from input source B, and discharging to the output load. Figures 33, 34, and 35 show the flow of current in the power path during these phases of operation.

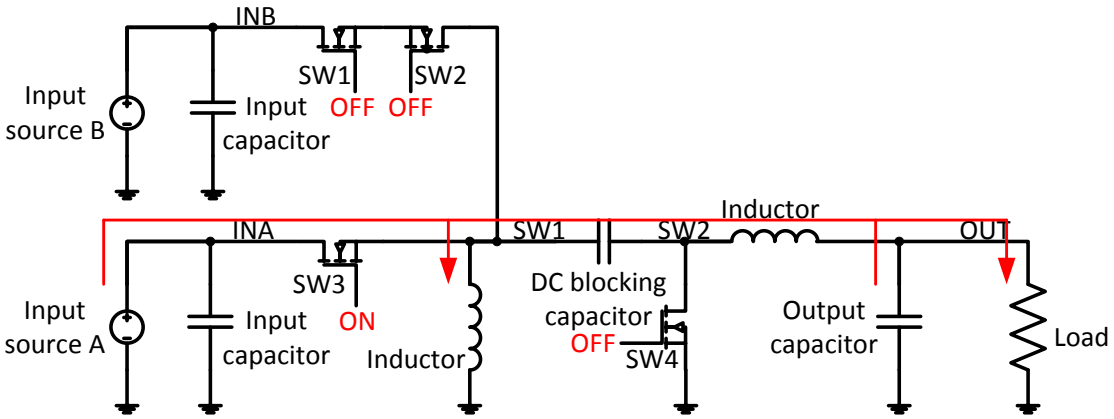

Figure 33. Dual-Input Zeta Current when Charging From Input Source A

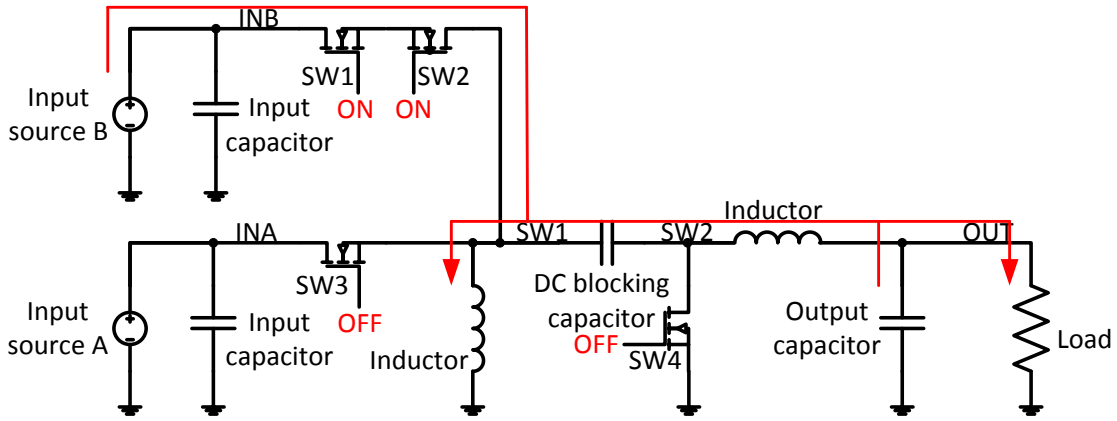

Figure 34. Dual-Input Zeta Current when Charging From Input Source B

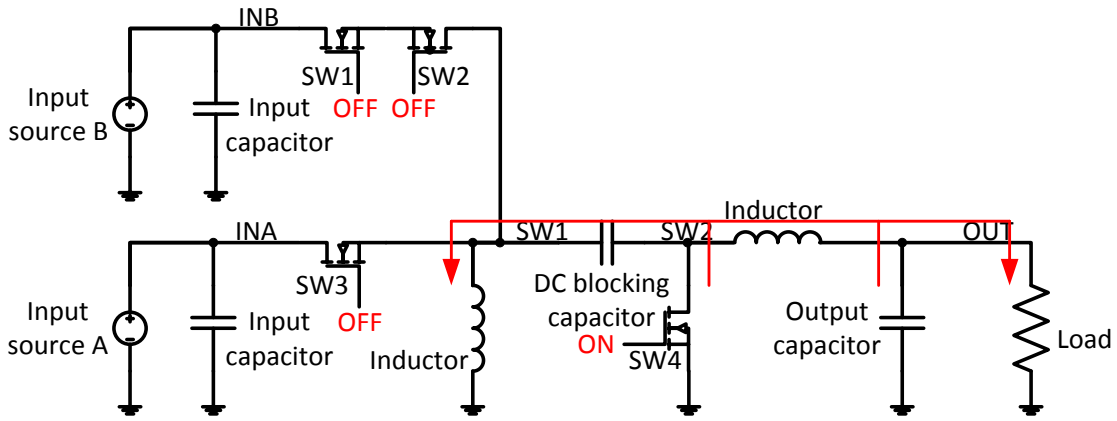

Figure 35. Dual-Input Zeta Current when Discharging to Output Load

The dual-input zeta converter has the same current flow characteristics in its two inductors as the single input zeta does. The input side inductor (connected to node SW1) always has current flowing towards ground and the output side inductor (connected to node SW2) always has current flowing towards the output load. Waveforms for the dual-input zeta converter are shown in Figure 36 for in-cycle operation and Figure 37 for cycle-by-cycle operation. The inductors of a zeta converter will typically have the same AC current. The DC current of the input inductor will be equal to the sum of the average input currents and the output inductors DC current will be equal to the average output current. For simplicity only one waveform is shown which represents the inductor current.

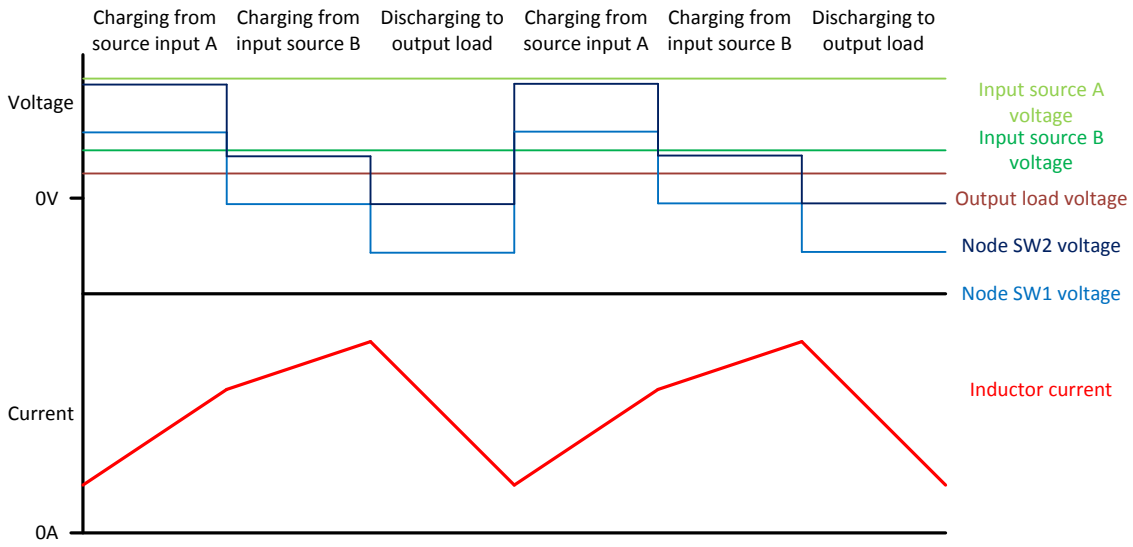

Figure 36. Dual-Input Zeta Waveforms for In-Cycle Operation

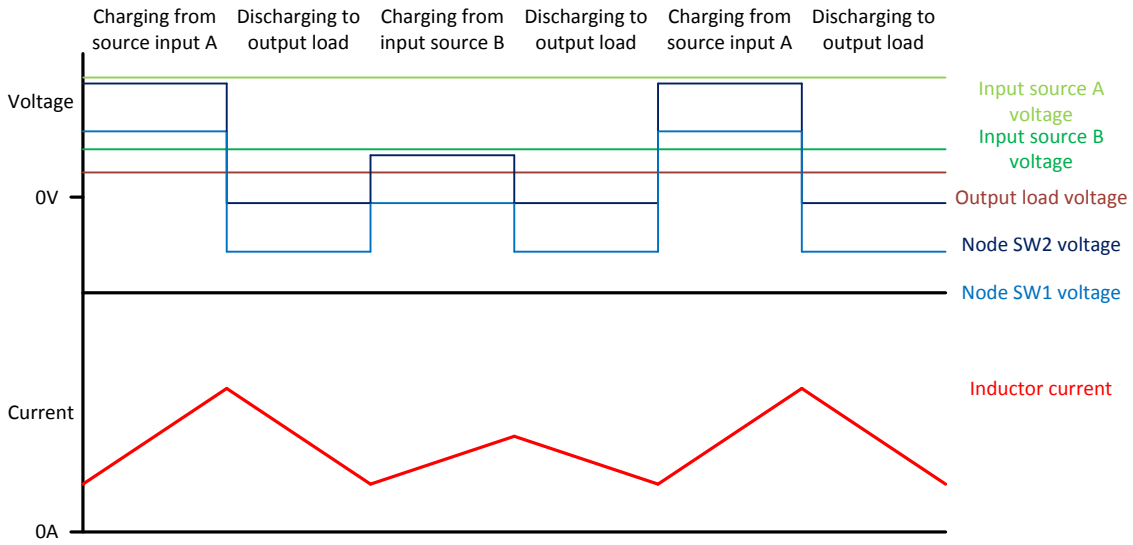

Figure 37. Dual-Input Zeta Waveforms for Cycle-By-Cycle Operation

To verify the operation the dual-input zeta an LTSpice simulation is done using the same methods as is done for the dual-input four-FET buck-boost converter. The simulation conditions are input voltages of 12V and 5V and the output voltage is approximately 3.33V. Figure 38 shows the SPICE schematic and Figure 39 shows the resulting waveforms. The resulting efficiency for this power path (neglecting gate charge effects) is approximately 97% with an output load of 2.728A (9.08W).

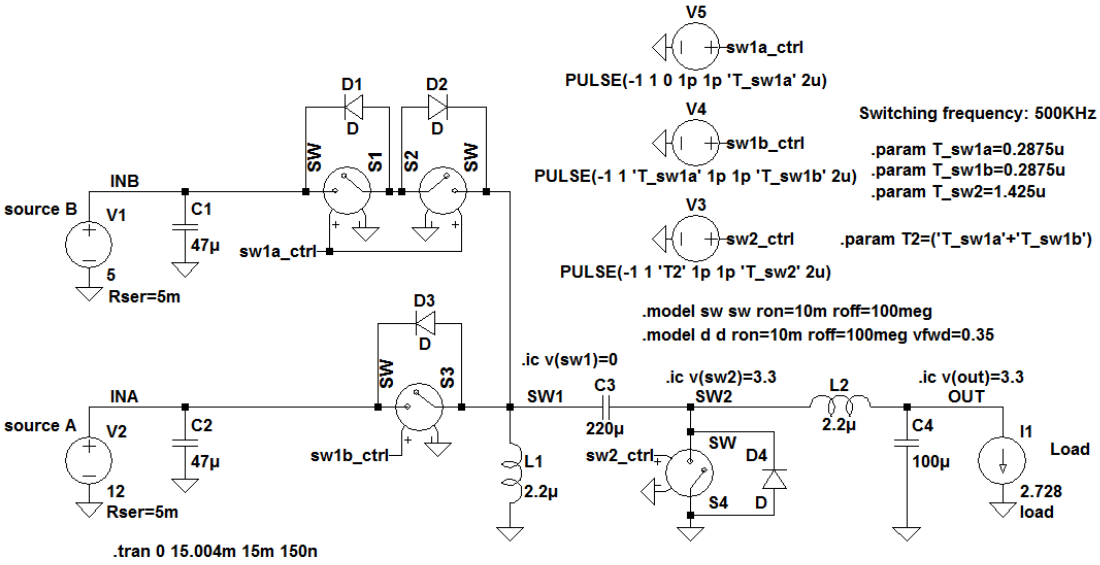

Figure 38. SPICE Circuit for Conceptual Verification of Dual-Input Zeta Converter

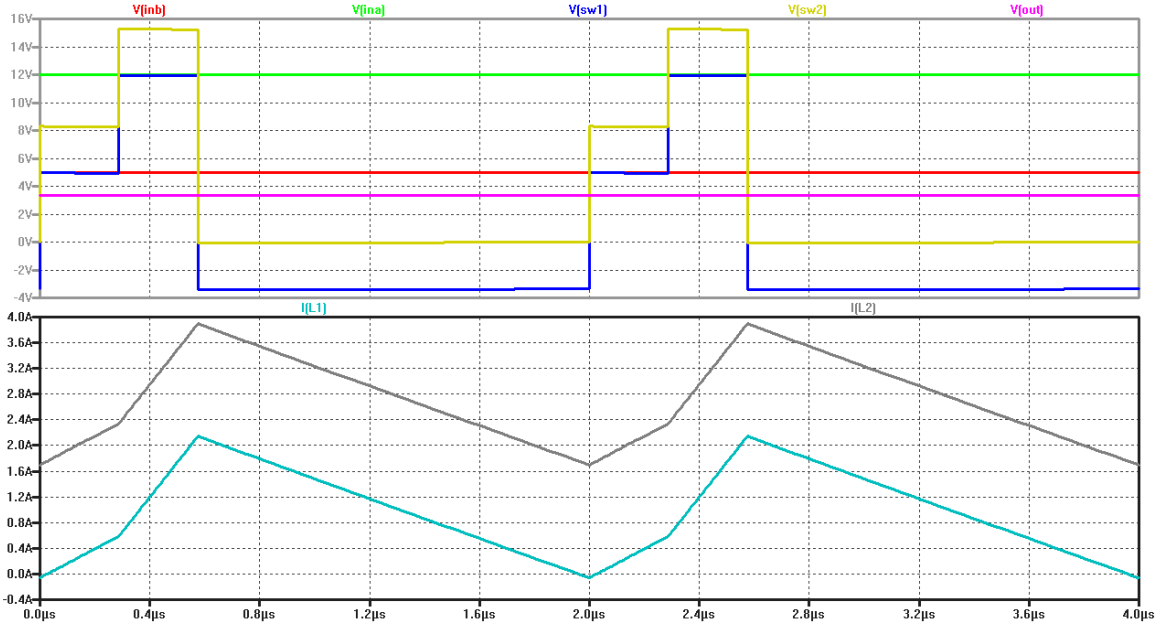

Figure 39. SPICE Waveforms for Conceptual Verification of Dual-Input Zeta Converter

An additional simulation is done to demonstrate that the dual-input zeta converter continues to regulate the output voltage and maintains the input current sharing ratio across different loads. As with the dual-input four-FET converter the simulation is done

using cycle-by-cycle operation and a voltage mode control loop regulates the output voltage. Table 9 shows the results of this simulation. Simulation conditions are the same as in the previous simulation with the difference being that the load steps from 1A to 5A in 1A steps each lasting 1ms. Figure 40 shows the output voltage of the converter during the test, there is some oscillation due to the voltage mode control loop not being precisely tuned for this test.

Table 9. Dual-Input Zeta Regulation Test Results

Output current (A)	Output voltage (V)	Input current A (A)	Input current A	Input current B (A)	Input current B	Efficiency
1	3.299	0.196	49%	0.201	51%	97%
2	3.299	0.402	50%	0.396	50%	98%
3	3.299	0.600	50%	0.609	50%	96%
4	3.299	0.809	50%	0.821	50%	95%
5	3.299	1.024	50%	1.037	50%	94%

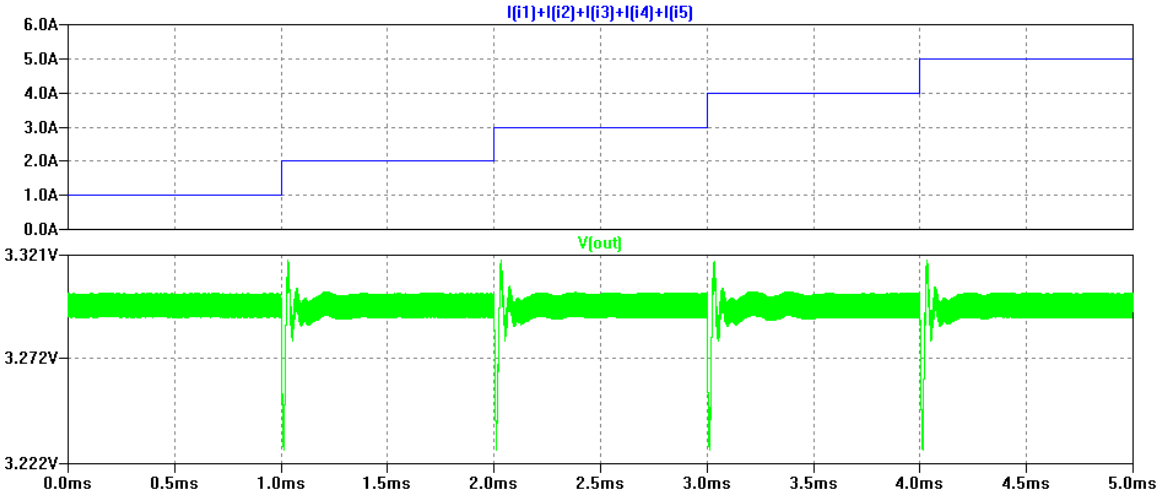

Figure 40. Dual-Input Zeta Regulation Test Output Voltage Waveform

Dual-Input SEPIC Converter

In order to achieve the dual-input functionality the SEPIC converter could not be modified in the same way as the four-FET buck-boost and the zeta converter. The reason for this is that in the SEPIC converter there is an inductor in series with the input power

source instead of a FET. As a result two topologies are considered to convert the SEPIC power path into a dual-input power path. The first option shown in Figure 41 functions very much like the dual-input zeta converter and will be referred to as a dual-input SEPIC converter. The second topology shown in Figure 42 is slightly smaller and more efficient but operates differently than the other dual-input power paths covered in this writing. It will be referred to as an alternate dual-input SEPIC converter.

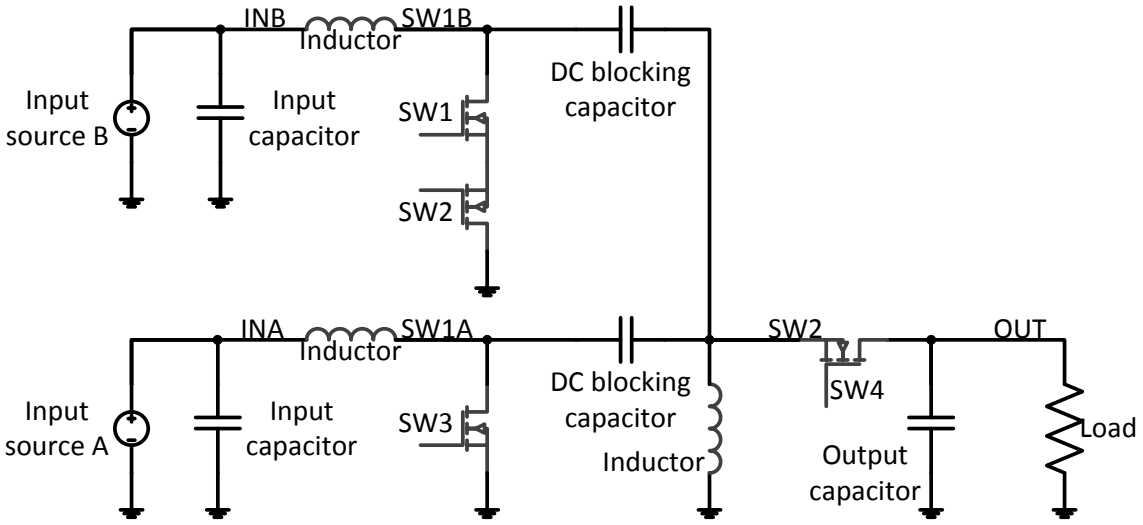

Figure 41. Dual-Input SEPIC Converter

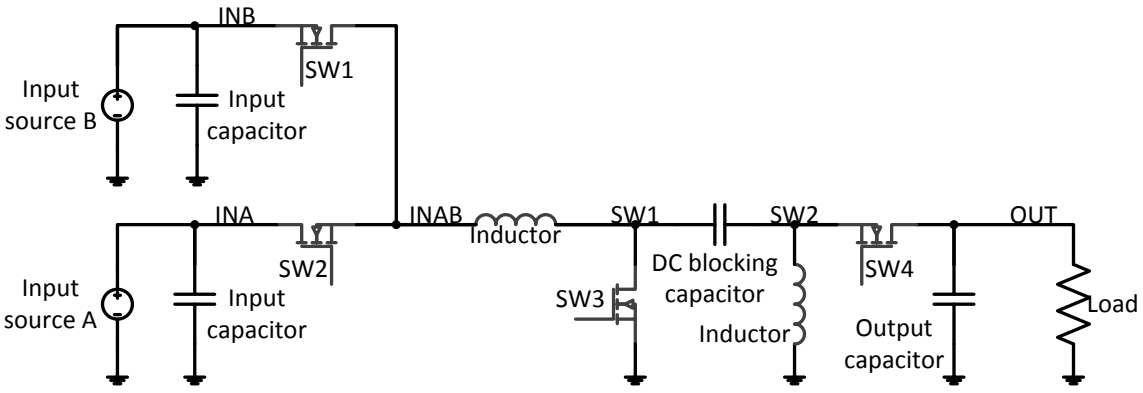

Figure 42. Alternate Dual-Input SEPIC Converter

The dual-input SEPIC converter operates very similarly to the dual-input zeta converter. The power path is somewhat more complicated in this case because adding a

second input power inductor to another input power source would short the two input power sources together, the solution to this is to duplicate the first half of the power path and merge them after the DC blocking capacitor. Figures 43, 44, and 45 show how current flows in the converter during each phase of operation.

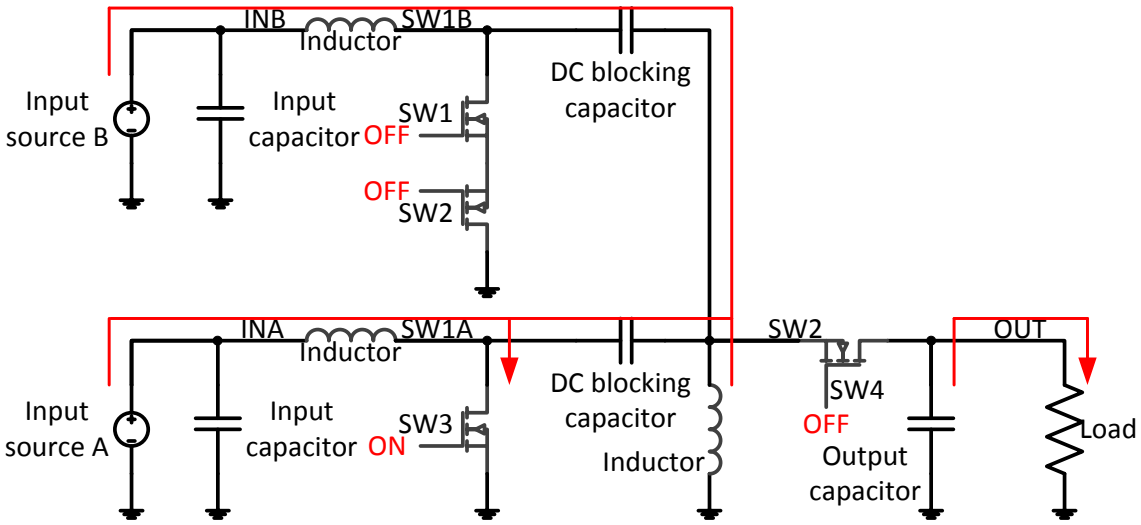

Figure 43. Dual-Input SEPIC Converter Current Flow when Charging from Input Source A

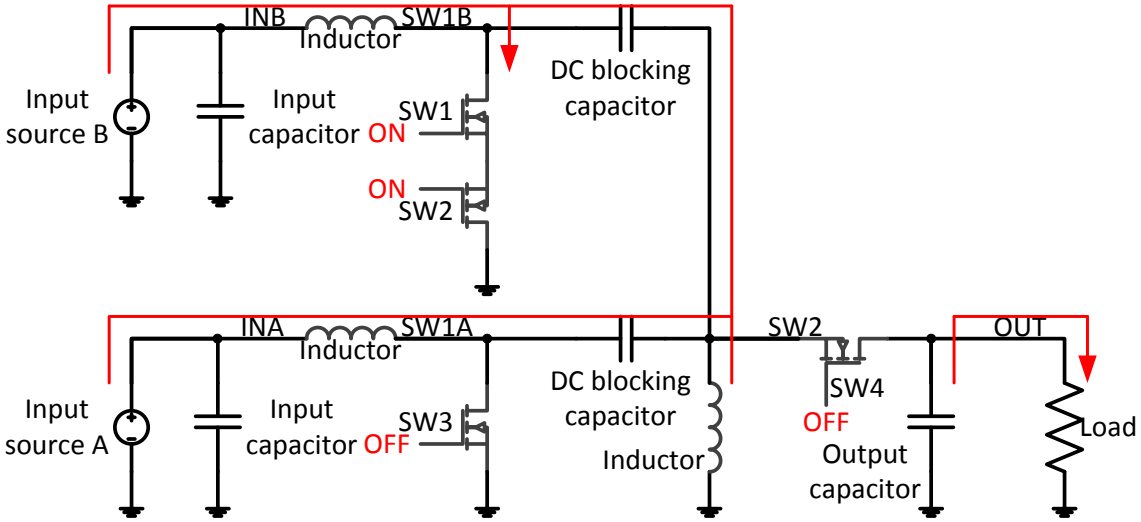

Figure 44. Dual-Input SEPIC Converter Current Flow when Charging from Input Source B

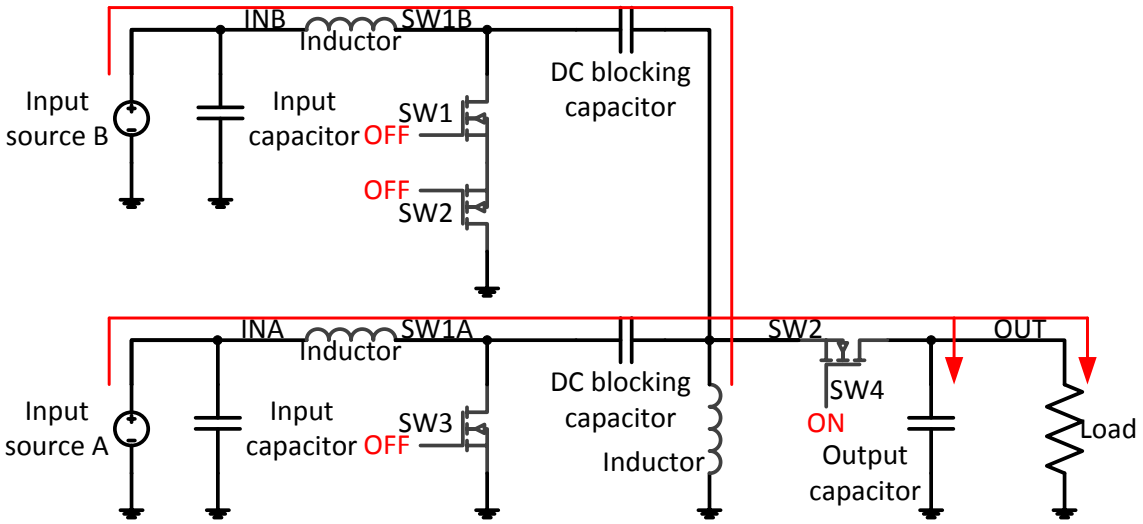

Figure 45. Dual-Input SEPIC Converter Current Flow when Discharging to the Output Load

Although it seems that the nodes SW1A and SW1B are separated there is still a potential for current to backflow through the FET body diodes if one input voltage source is at a higher voltage than the other. This is caused by the DC coupling effects of the DC coupling capacitors which transfer the voltage from one switch node to the other. In this configuration the voltage on input source A must be the same as or greater than the voltage on input source B to avoid forward biasing the body diode on SW3 while SW1 and SW2 are on. This restriction can be removed by adding a second FET in series with FET SW3 this is also referred to as implementing back to back FETs.

During the charging phase from either input source the inductor current in the two input inductors remains the same as both are discharging either into the FET SW3 or into one of the DC blocking capacitors. As the input side inductors are being charged from the input power source their current increases. Then their current decreases during a discharge phase to the output load. The input switch nodes SW1A and SW1B track each other with a fixed DC offset. The output switch node SW2 also tracks the input switch nodes with a fixed DC offset. Figures 46 and 47 present a graphical representation of the

waveforms of a dual-input SEPIC converter during each of the three phases of operation. The inductor current shown is a representation of the output inductor which will have the same average current as the load. The input inductors of the dual SEPIC converter will have an average current matching the average current of their associated input sources.

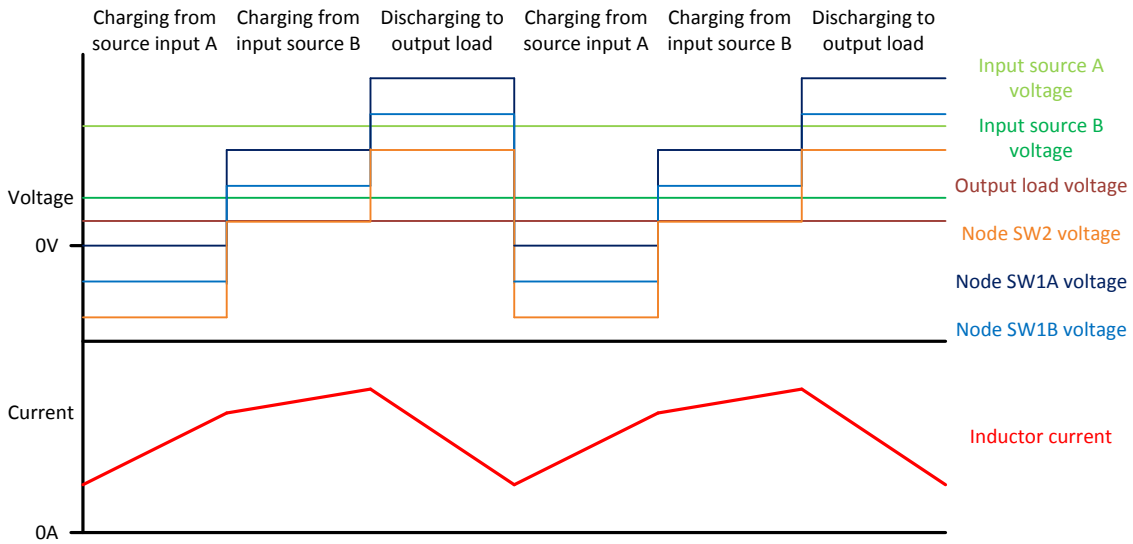

Figure 46. Dual-Input SEPIC Converter Waveforms for In-Cycle Operation

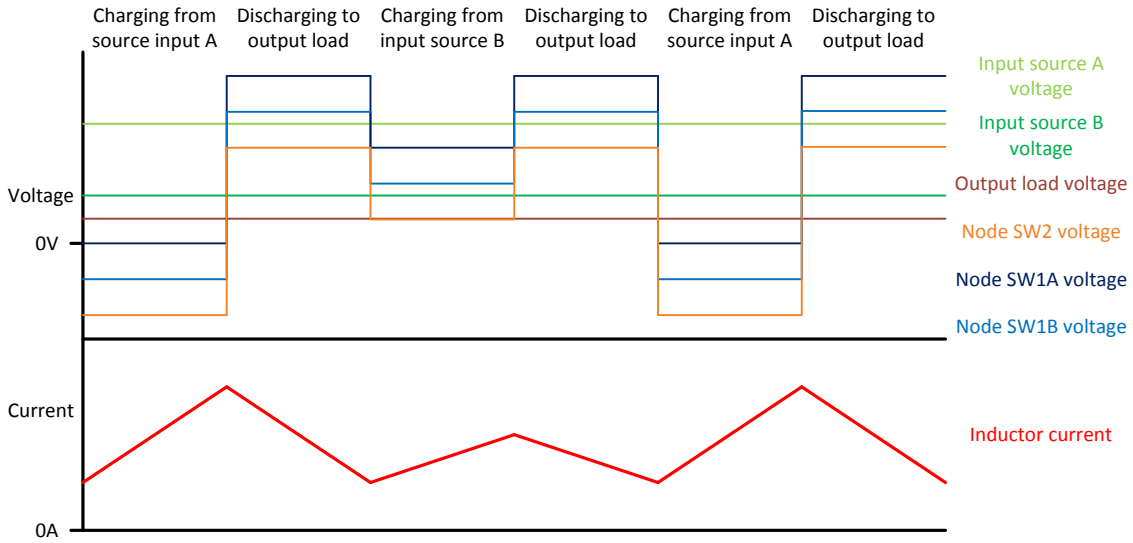

Figure 47. Dual-Input SEPIC Converter Waveforms for Cycle-By-Cycle Operation

Just as with the dual-input zeta, the dual-input SEPIC is demonstrated in LTSpice using the schematic shown in Figure 48 with the resulting waveforms in Figure 49 The resulting efficiency for this power path (neglecting gate charge effects) is approximately 96% with an output load of 2.728A (9.06W).

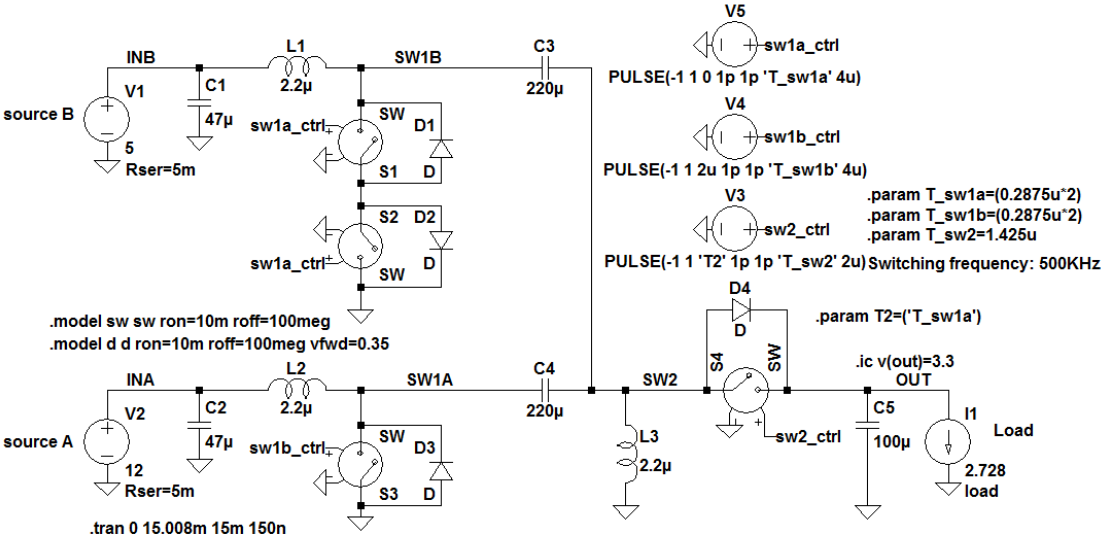

Figure 48. SPICE Circuit for Conceptual Verification of Dual-Input SEPIC Converter

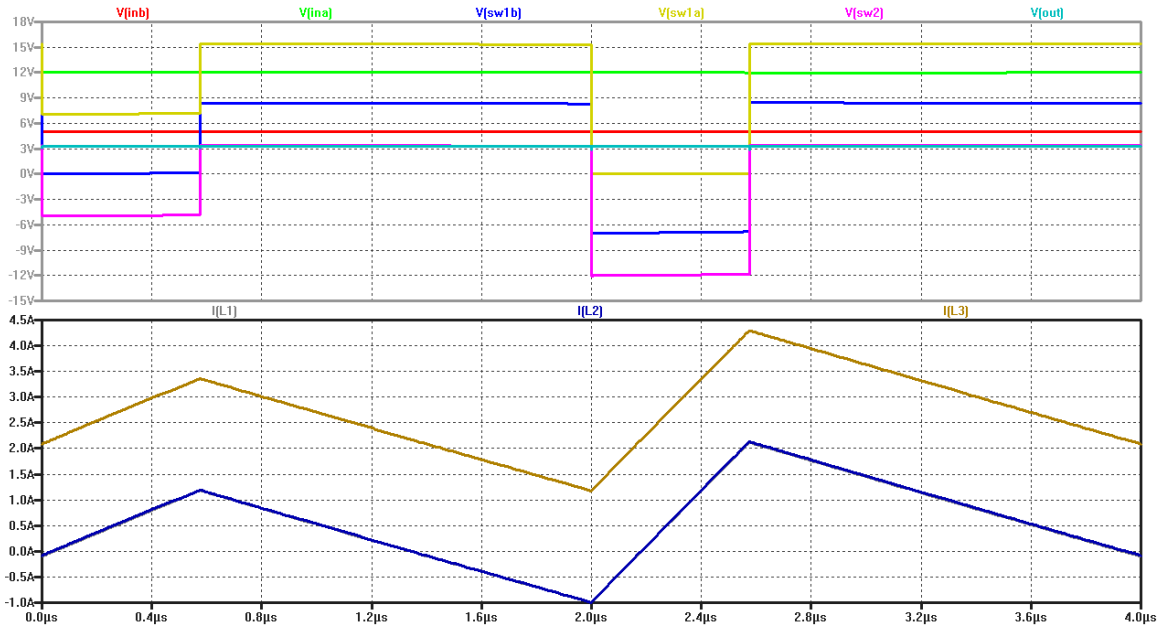

Figure 49. SPICE Waveforms for Conceptual Verification of Dual-Input SEPIC Converter

As with the previous converters, an additional simulation is done to demonstrate that the dual-input SEPIC converter continues to regulate the output voltage and maintains the input current sharing ratio across different loads. Simulation is done using cycle-by-cycle operation and a voltage mode control loop regulates the output voltage. Table 10 shows the results of this simulation. Figure 50 shows the output voltage of the converter during the test.

Table 10. Dual-Input SEPIC Regulation Test Results

Output current (A)	Output voltage (V)	Input current A (A)	Input current A	Input current B (A)	Input current B	Efficiency
1	3.299	0.197	49%	0.205	51%	96%
2	3.300	0.398	49%	0.413	51%	95%
3	3.300	0.594	49%	0.615	51%	96%
4	3.299	0.802	49%	0.830	51%	94%
5	3.299	1.010	49%	1.045	51%	94%

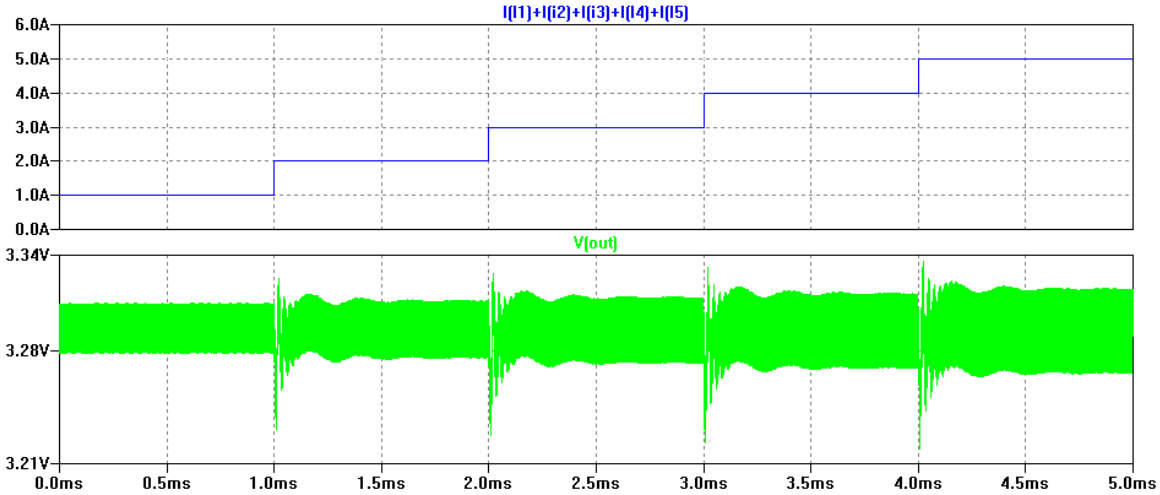

Figure 50. Dual-Input SEPIC Regulation Test Output Voltage Waveform

Alternate Dual-Input SEPIC Converter

An alternate dual-input SEPIC converter can be designed as shown in Figure 51 This SEPIC converter power path takes advantage of the fact that there is an inductor in series with the input to the converter which will act to keep the input current roughly

constant. Adding a pair of “selector switches” to the input side of the FET before this inductor allows the designer to select when the converter input current is being drawn from each of the input power sources. By alternating the selection of the input power sources rapidly with some duty cycle, a ratio of current can be drawn from the two sources. The SEPIC converter after the input selector switches can operate as a single input SEPIC converter. The switching frequency and duty ratio of the input selector switches can be controlled independently of the rest of the converter in this case, which is different from the other dual-input power paths discussed in this writing.

Because node INAB will only ever be at the voltage of input source A or input source B, the input selector does not need to be built using series (reverse blocking) FETs which improves the efficiency of this topology. Another benefit is that only a single inductor and a single DC blocking capacitor are needed.

To illustrate the operation of this topology an assumption of cycle-by-cycle style control will be made. Assuming that the converter selects each input power source for a full cycle of SW3 and SW4 and that each input source is selected every other cycle, Figures 51, 52, 53, and 54 represent the flow of current in the alternate dual-input SEPIC converter. Given the assumed operation of this power path Figure 55 shows an approximation of what the waveforms of the converter would look like.

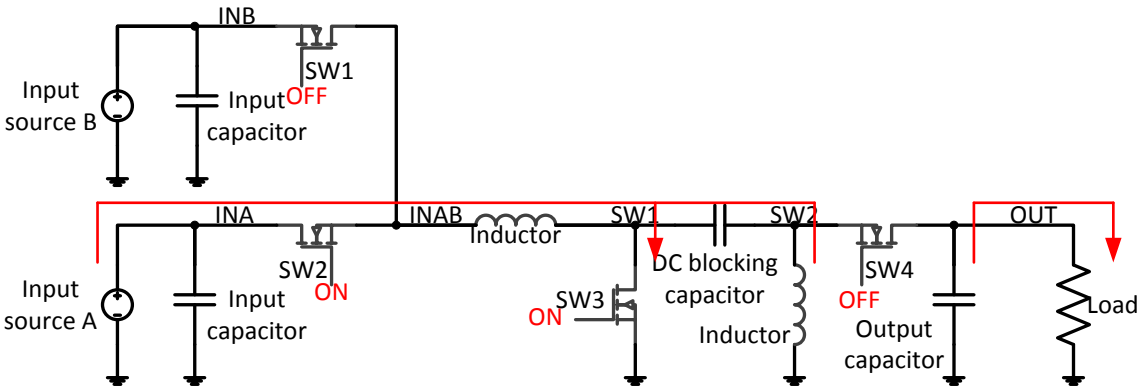

Figure 51. Flow of Current in Alternate Dual-Input SEPIC Converter when Charging while Drawing Power from Input Source A

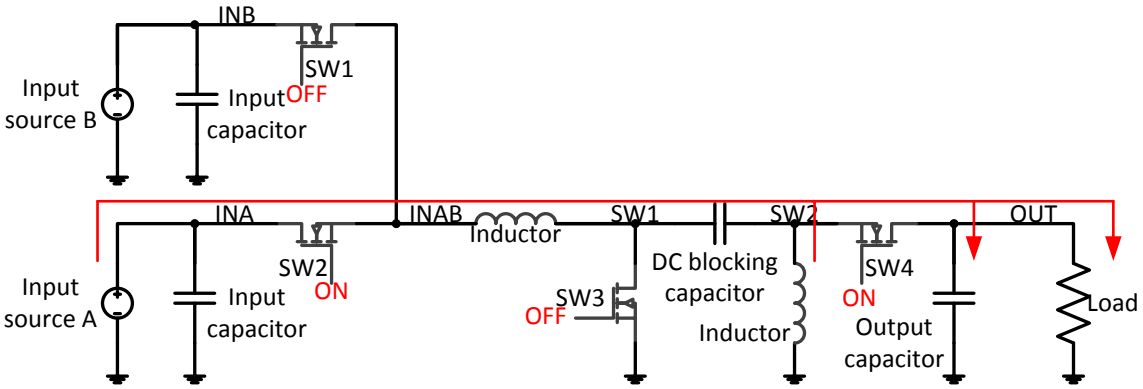

Figure 52. Flow of Current in Alternate Dual-Input SEPIC Converter when Discharging while Drawing Power from Input Source A

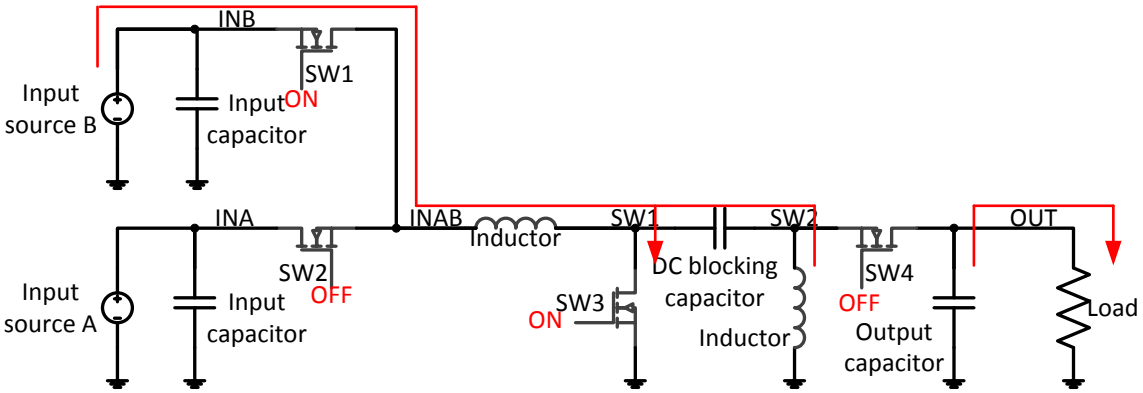

Figure 53. Flow of Current in Alternate Dual-Input SEPIC Converter when Charging while Drawing Power from Input Source B

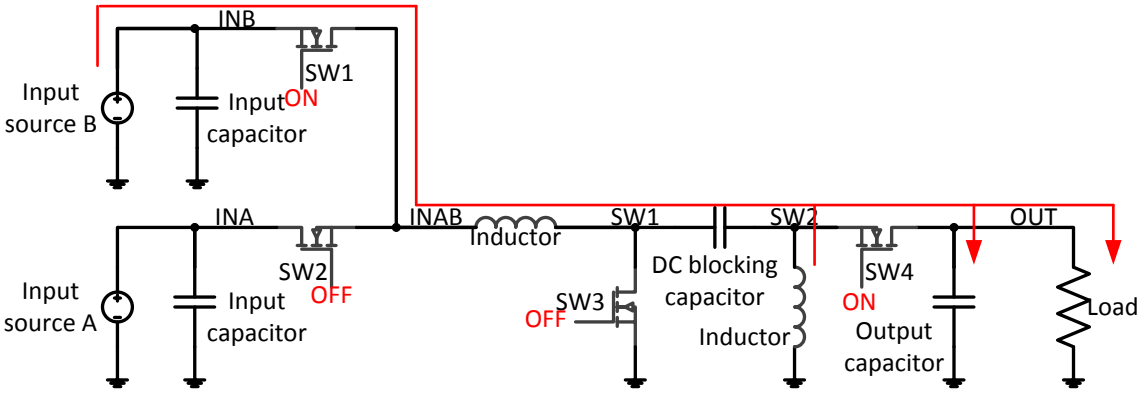

Figure 54. Flow of Current in Alternate Dual-Input SEPIC Converter when Discharging while Drawing Power from Input Source B

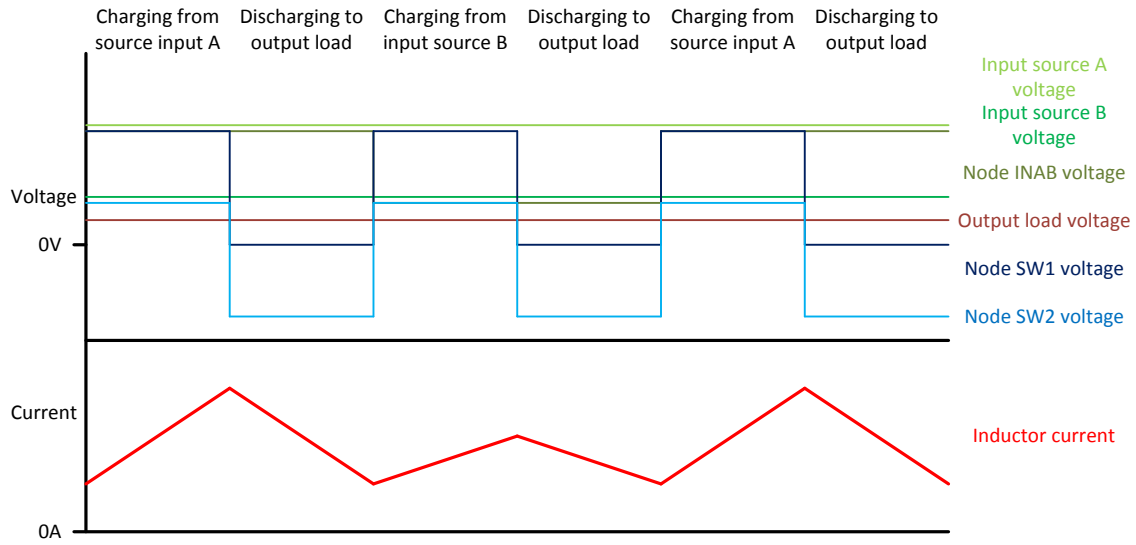

Figure 55. Operational Waveforms for Alternate Dual-Input SEPIC Converter

Having the input source selector switches able to run independently means that power could be saved by having them run slower than the rest of the converter, this would have the drawback of providing a noisier load current to each input source which would mean they may see higher current spikes. Conversely the input selector switches could be run faster to smooth out the input current to each input source. This would have the drawback of reducing the efficiency of the converter.

Operation of this power path is simulated with LTSpice using the same conditions as the other dual-input power paths. Input conditions are 12V and 5V and output

condition is approximately 3.3V at 2.728A (~9W), the resulting efficiency for this power path neglecting gate charge effects is 96%. Figure 56 shows the Spice circuit and Figure 57 shows the resulting waveforms.

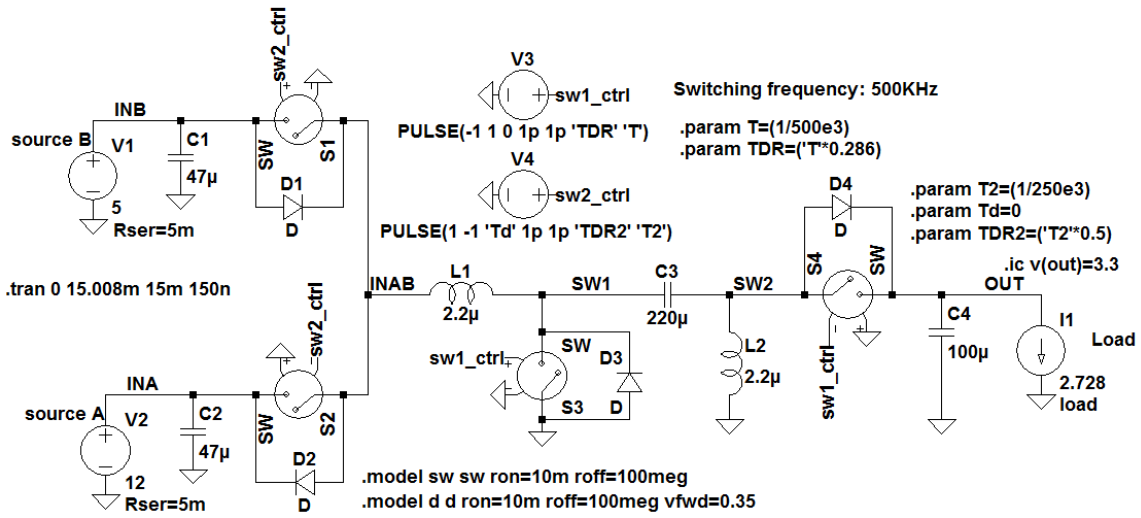

Figure 56. SPICE Circuit for Conceptual Verification of Alternate Dual-Input SEPIC Converter

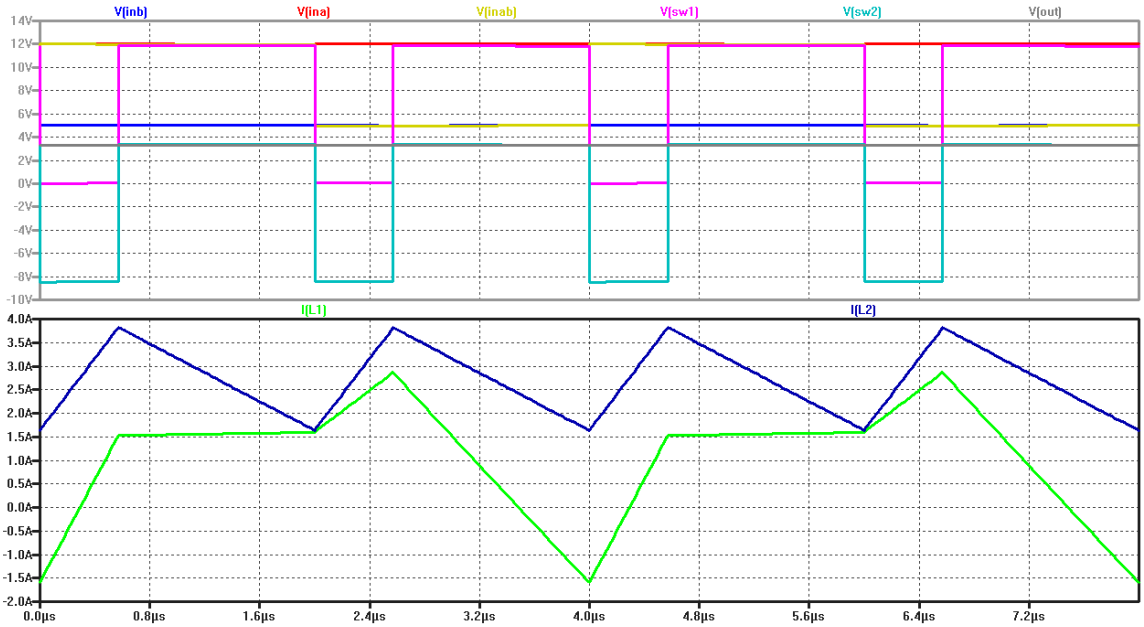

Figure 57. SPICE Waveforms for Conceptual Verification of Dual-Input SEPIC Converter

As with the previous converters, an additional simulation is done to demonstrate that the alternate dual-input SEPIC converter continues to regulate the output voltage and maintains the input current sharing ratio across different loads. Simulation is done using cycle-by-cycle operation and a voltage mode control loop regulates the output voltage. Table 11 shows the results of this simulation. Figure 58 shows the output voltage of the converter during the test.

Table 11. Alternate Dual-Input SEPIC Regulation Test Results

Output current (A)	Output voltage (V)	Input current A (A)	Input current A	Input current B (A)	Input current B	Efficiency
1	3.299	0.239	55%	0.196	45%	93%
2	3.299	0.437	53%	0.391	47%	96%
3	3.299	0.641	52%	0.596	48%	96%
4	3.299	0.844	51%	0.817	49%	94%
5	3.299	1.066	51%	1.021	49%	94%

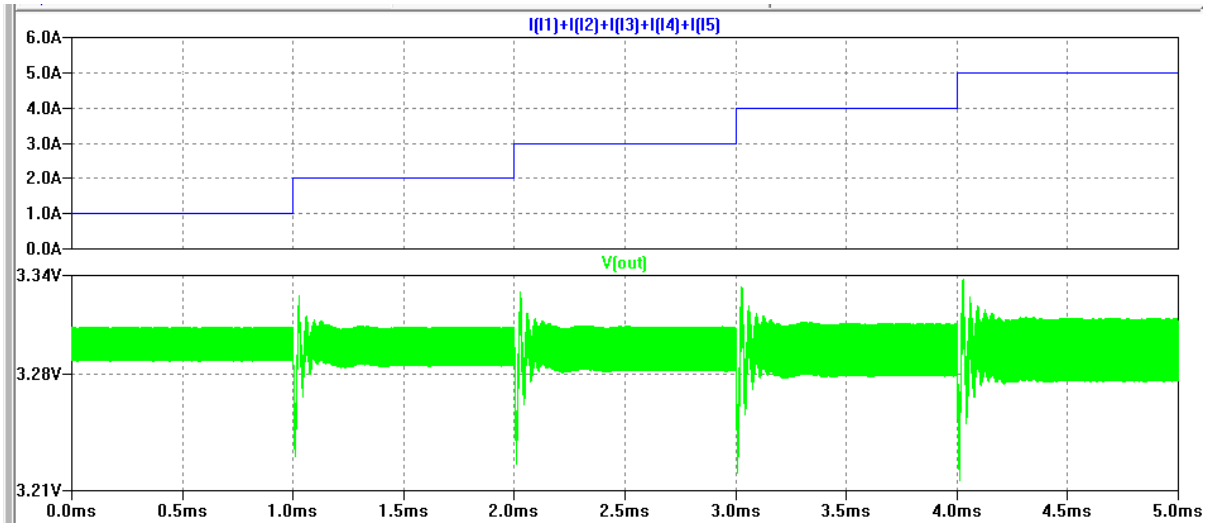

Figure 58. Alternate Dual-Input SEPIC Regulation Test Output Voltage Waveform

Power Path Comparison

Each dual-input converter presents different characteristics in terms of component count and efficiency. These metrics are common figures of merit in power supply design.

Table 12 shows the differences in component makeup of each power path. The first three rows are the traditional approaches and the last four rows are the single power path dual-input topologies being considered in this writing. Inductors are typically the largest items in a voltage regulator power path, with FETs being the next largest and DC blocking capacitors are typically not as large. Table 13 is rearranged to show the relative ranking of each converter based on prioritizing fewer inductors over fewer MOSFETs and fewer MOSFETs over fewer DC blocking capacitors. By this analysis the most size efficient converters would be the dual-input four-FET, dual-input zeta, and alternate dual-input SEPIC topologies.

Table 12. Regulator Power Path Component Makeup

	Inductors	MOSFETs	DC blocking capacitors
Dual four-FET buck-boost	2	8	0
Dual SEPIC	4	4	2
Dual zeta	4	4	2
Dual-input four-FET buck-boost	1	5	0
Dual-input zeta	2	4	1
Dual-input SEPIC	3	4	2
Dual-input SEPIC alternate topology	2	4	1

Table 13. Regulator Power Path Component Makeup Rearranged

	Inductors	MOSFETs	DC blocking capacitors
Dual-input four-FET buck-boost	1	5	0
Dual-input zeta	2	4	1
Dual-input SEPIC alternate topology	2	4	1
Dual four-FET buck-boost	2	8	0
Dual-input SEPIC	3	4	2
Dual-SEPIC	4	4	2
Dual zeta	4	4	2

Efficiency is compared for each converter using LTSpice simulations. Traditional two power path designs are simulated assuming each power path is running independently. The dual-input four-FET, zeta, and SEPIC converters are simulated assuming both in-cycle and cycle-by-cycle operation. Lastly, the alternate dual-input SEPIC is simulated assuming only cycle-by-cycle operation. The conditions for the efficiency simulations are shown in Table 14 Losses modeled include MOSFET gate charge and DC resistance, inductor DC resistance, capacitor equivalent series resistance, and MOSFET parasitic diode losses. The efficiency of the four-FET converter would be greater if operated in buck or boost mode, this is not accounted for in this analysis.

Then simulations determined efficiency by running the circuit until steady state is reached after a fixed time of 4ms. After steady state is reached an additional 100us of data is gathered and used for computing efficiency. The efficiency of these circuits is

determined by taking the average output power and dividing by the sum of the average input powers from the two input power sources.

Table 14. Converter Efficiency Simulation Conditions

Input voltages	5V and 12V
Output voltage	3.3V
Output current range	1A – 15A
Input current sharing ratio	50% from each source

Figures 59 through 61 show the schematics used in simulating the efficiency of the traditional approaches for dual-input power supplies: dual four-FET buck-boost, dual zeta, and dual SEPIC converter. The two power path simulations are done using two independent power paths each supplying power to a load drawing 50% of the same load current drawn by a single dual-input power path. This is done to simplify the simulated control scheme which is needed in order to achieve stable simulation. Following those are Figures 62 through 68 which show the schematics used in simulating the efficiency of the topologies under investigation in this writing. Simulations of all power paths are done with voltage mode control for simplicity.

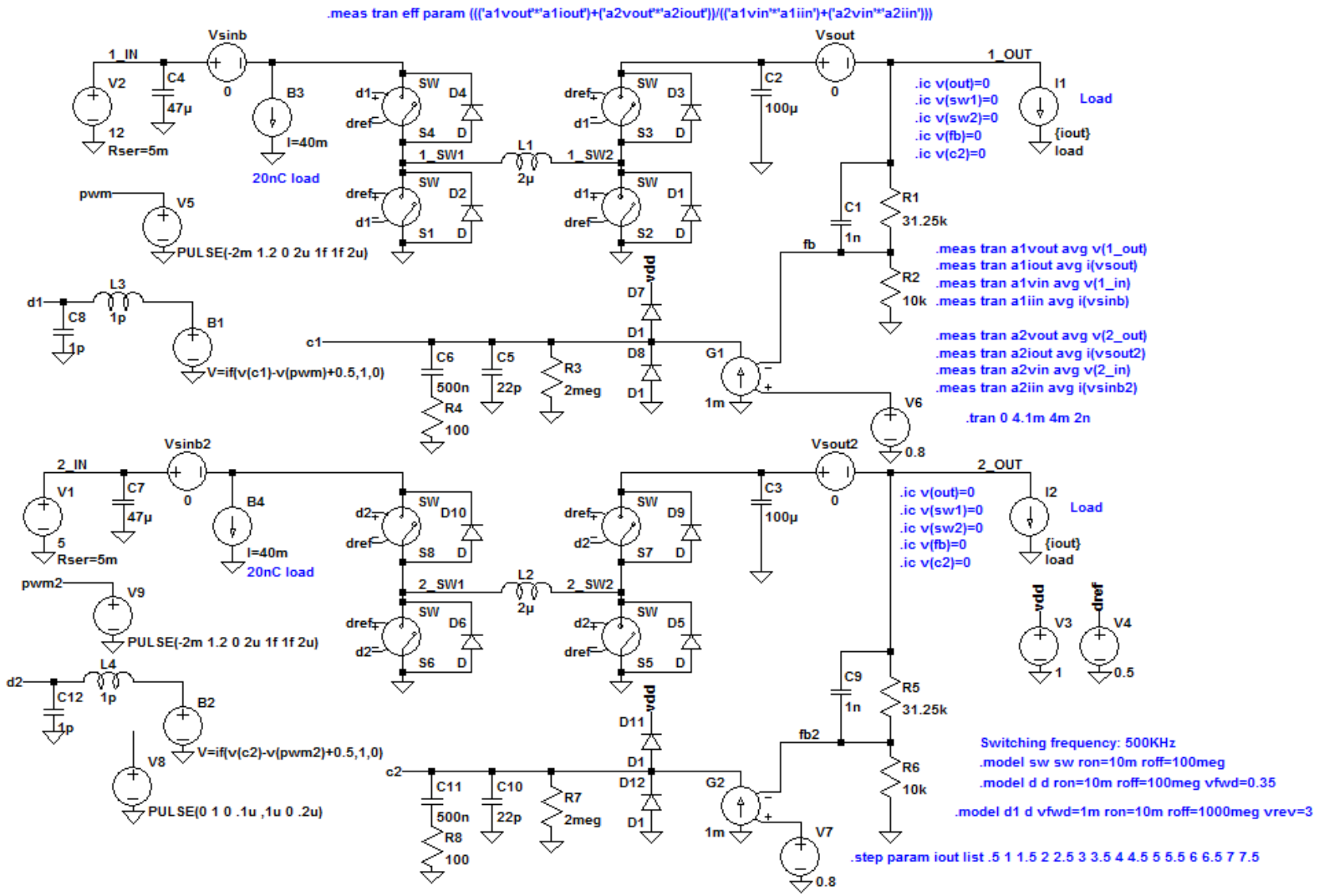

Figure 59. SPICE Circuit for Simulating the Efficiency of Dual Four-FET Buck-Boost Converter Topology

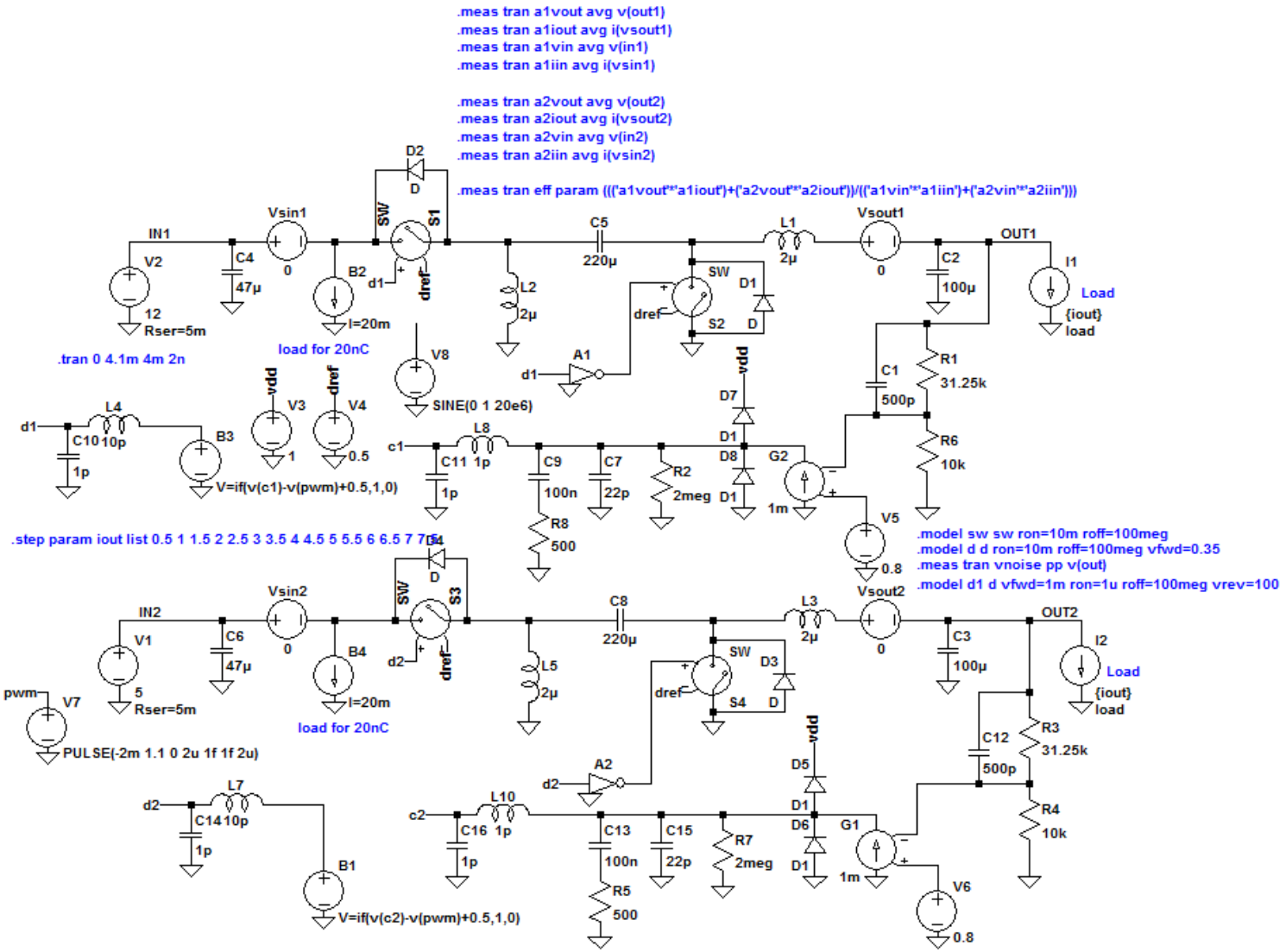

Figure 60. SPICE Circuit for Simulating the Efficiency of Dual Zeta Converter Topology

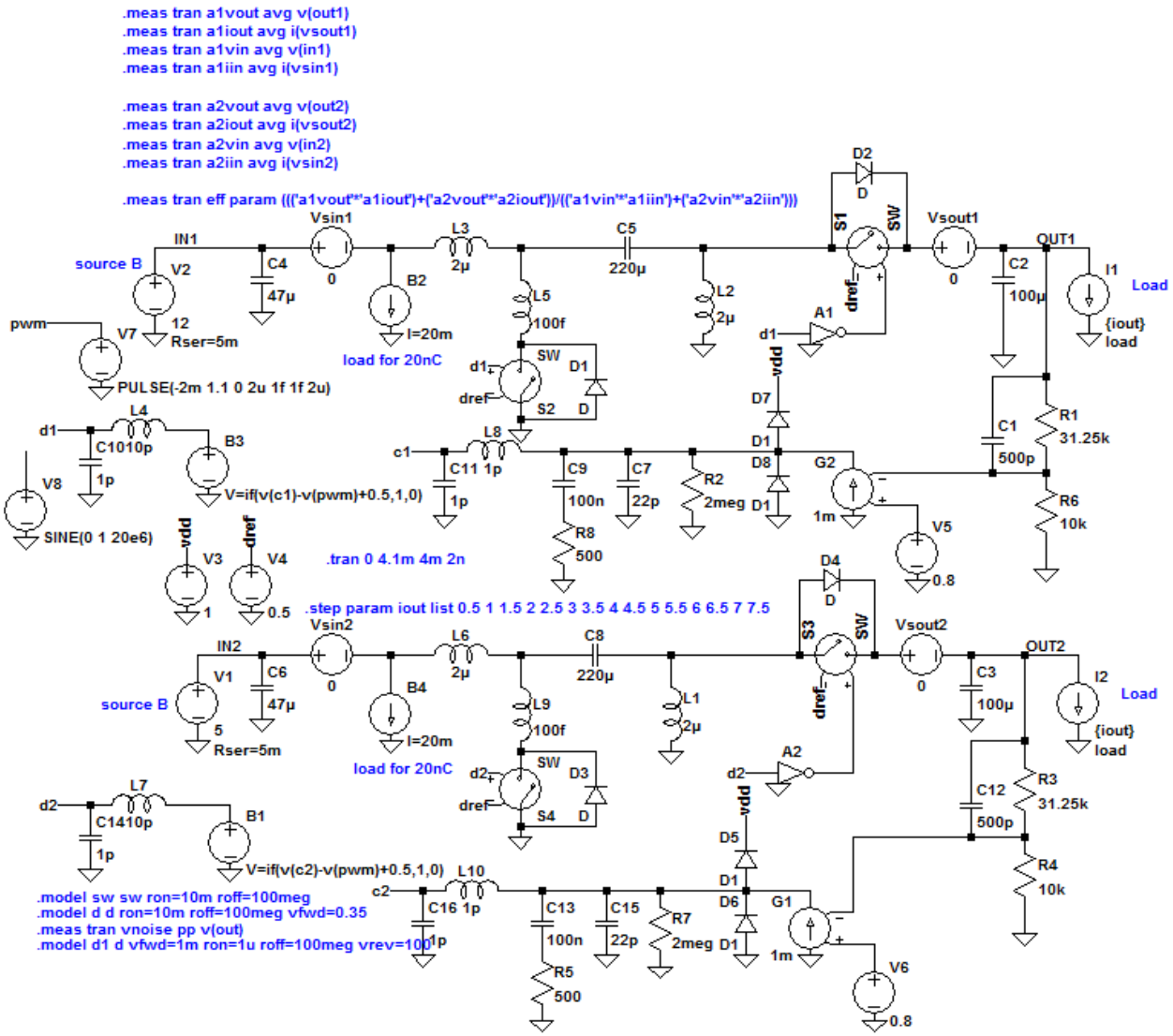

Figure 61. SPICE Circuit for Simulating the Efficiency of Dual SEPIC Converter Topology

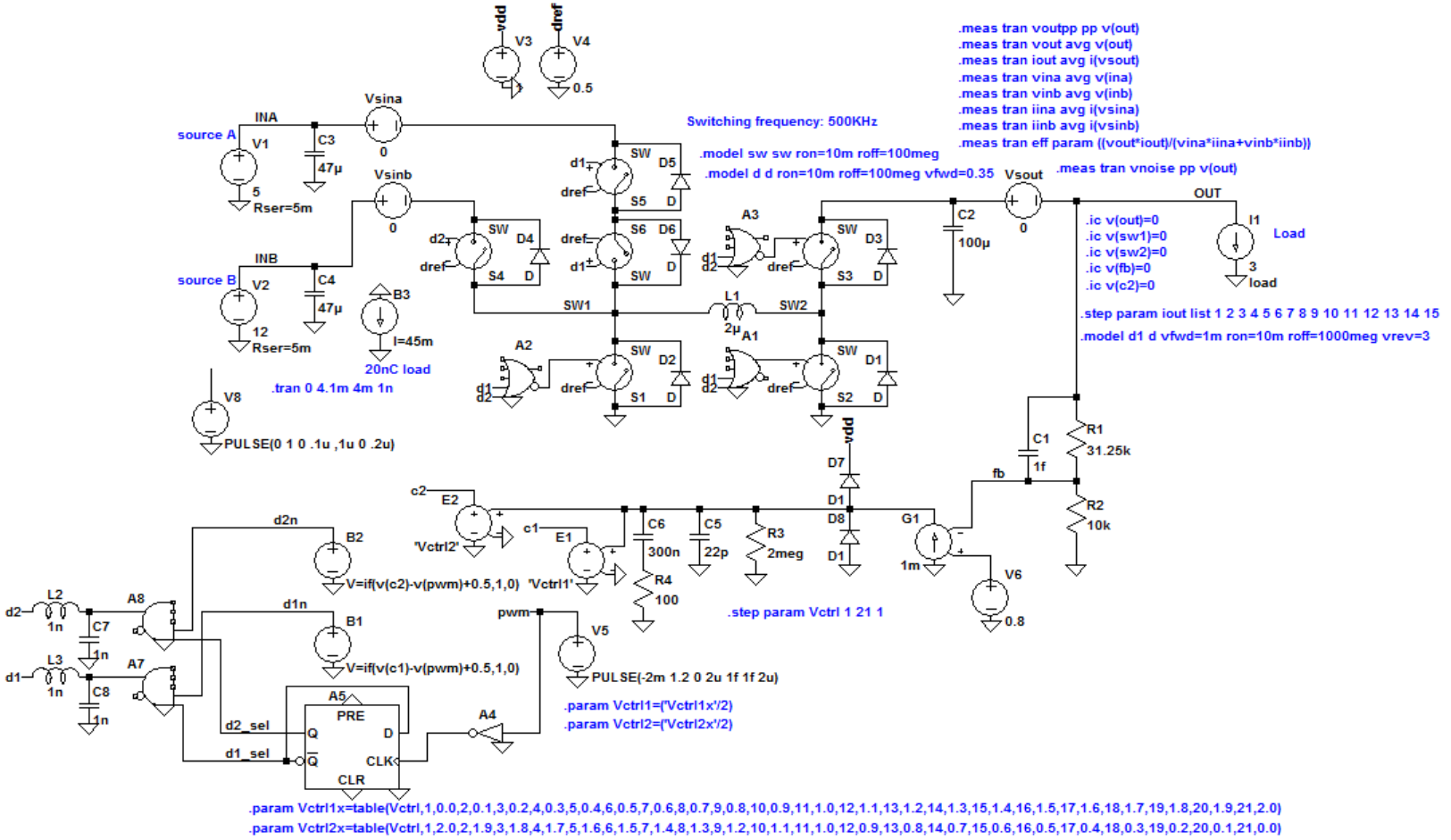

Figure 62. SPICE Circuit for Simulating the Efficiency of Dual-Input Four-FET Buck-Boost Converter Topology with Cycle-By-Cycle Operation

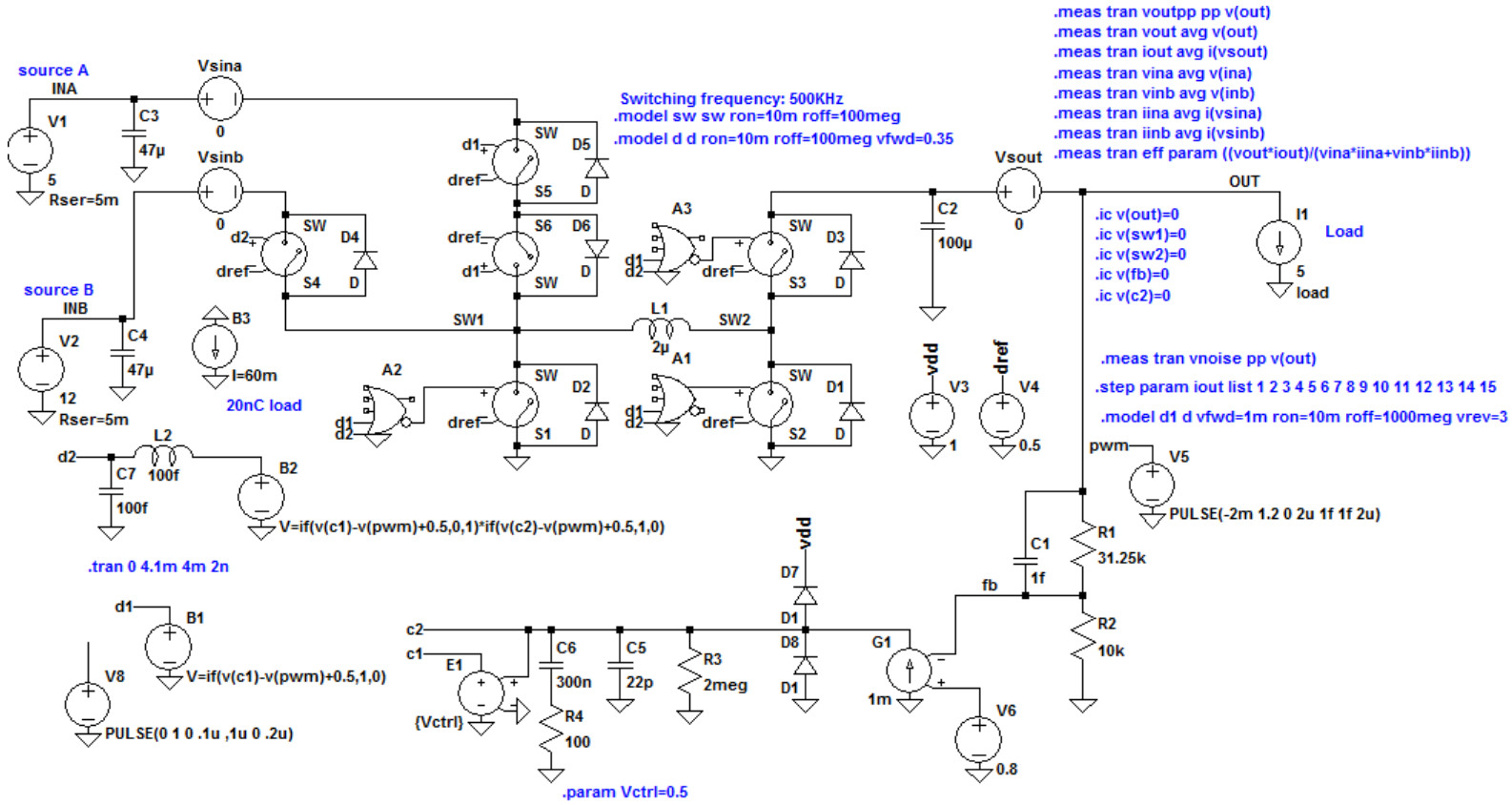

Figure 63. SPICE Circuit for Simulating the Efficiency of Dual-Input Four-FET Buck-Boost Converter Topology with In-Cycle Operation

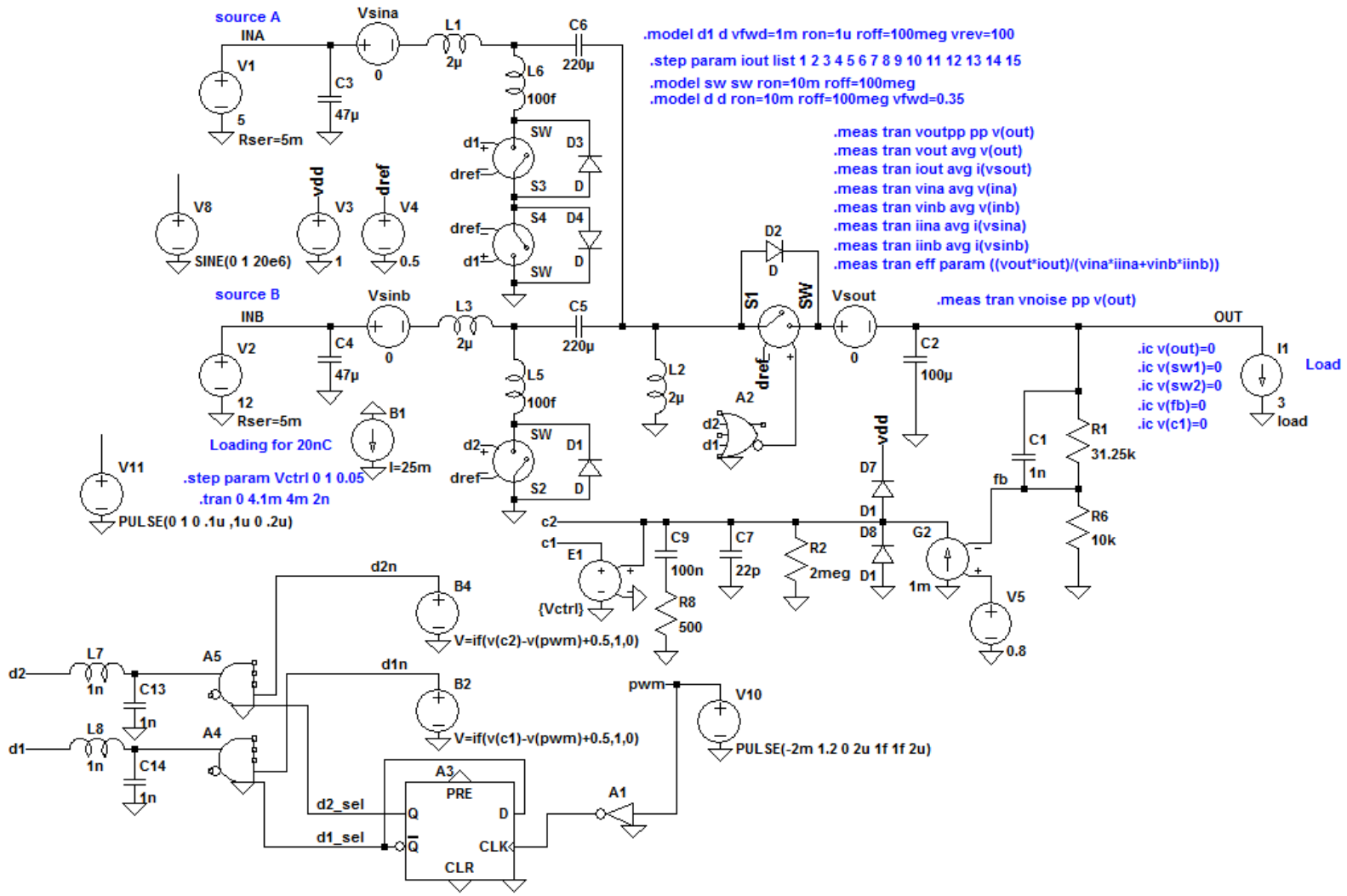

Figure 64. SPICE Circuit for Simulating the Efficiency of Dual-Input SEPIC Converter Topology with Cycle-By-Cycle Operation

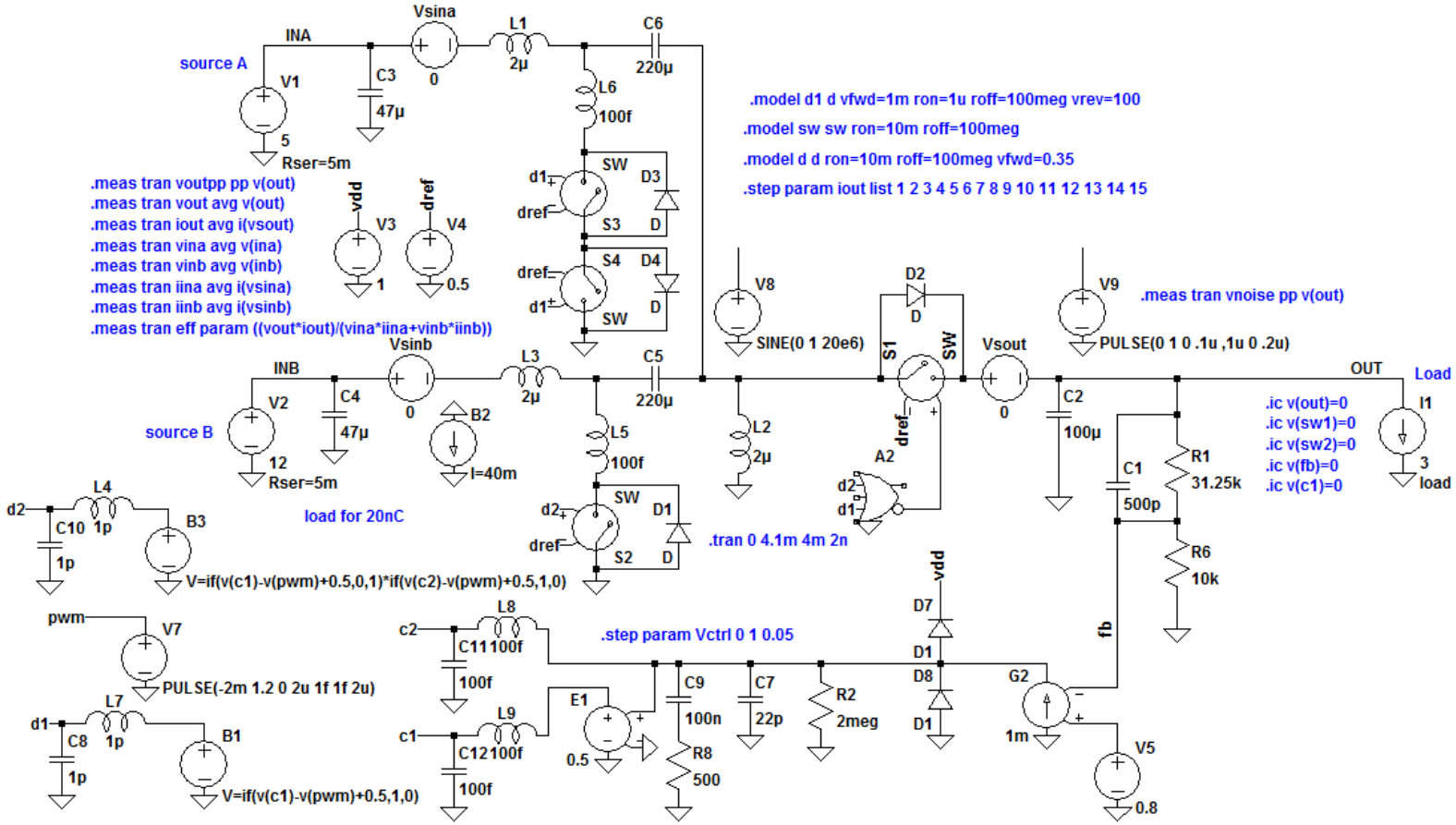

Figure 65. SPICE Circuit for Simulating the Efficiency of Dual-Input SEPIC Converter Topology with In-Cycle Operation

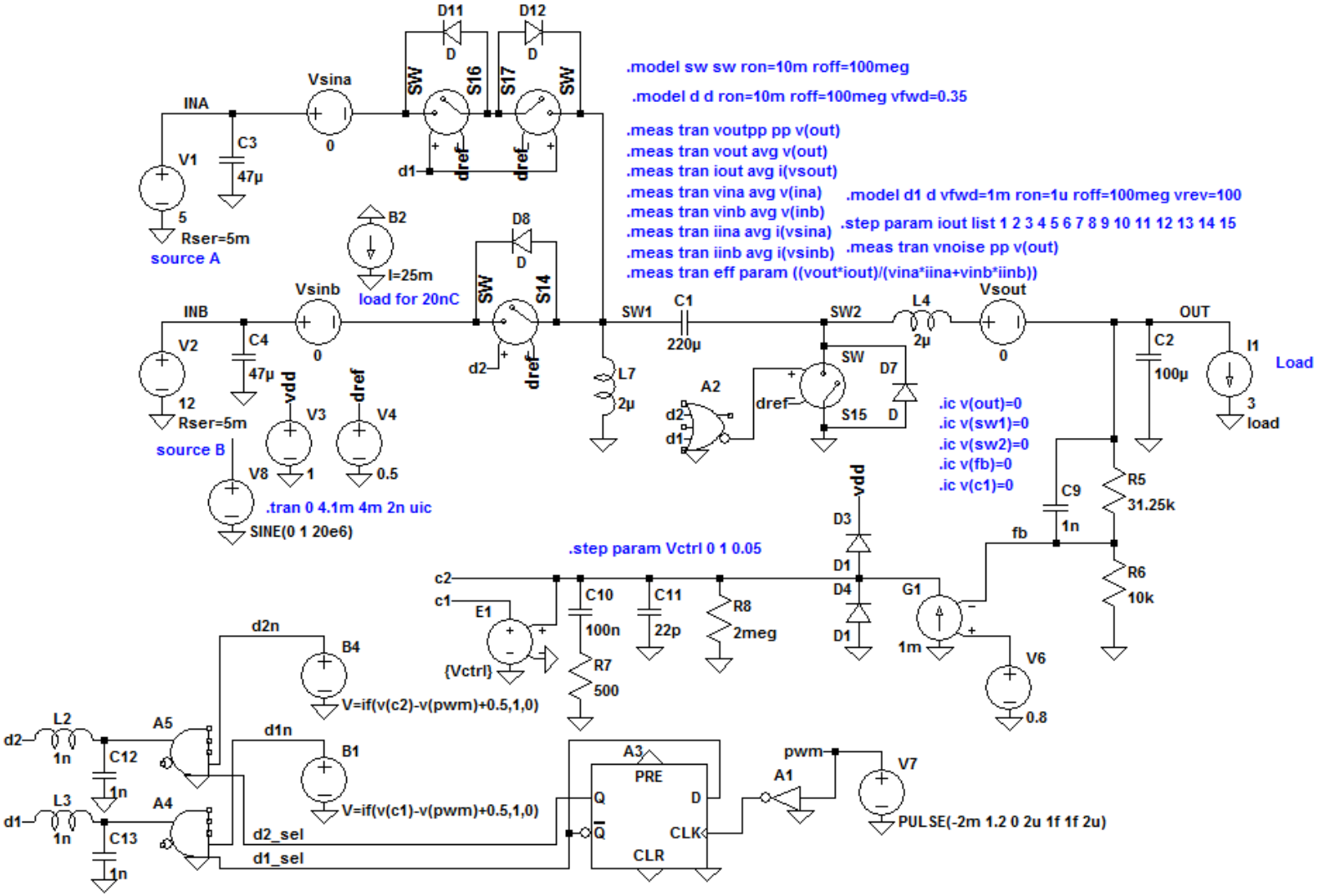

Figure 66. SPICE Circuit for Simulating the Efficiency of Dual-Input Zeta Converter Topology with Cycle-By-Cycle Operation

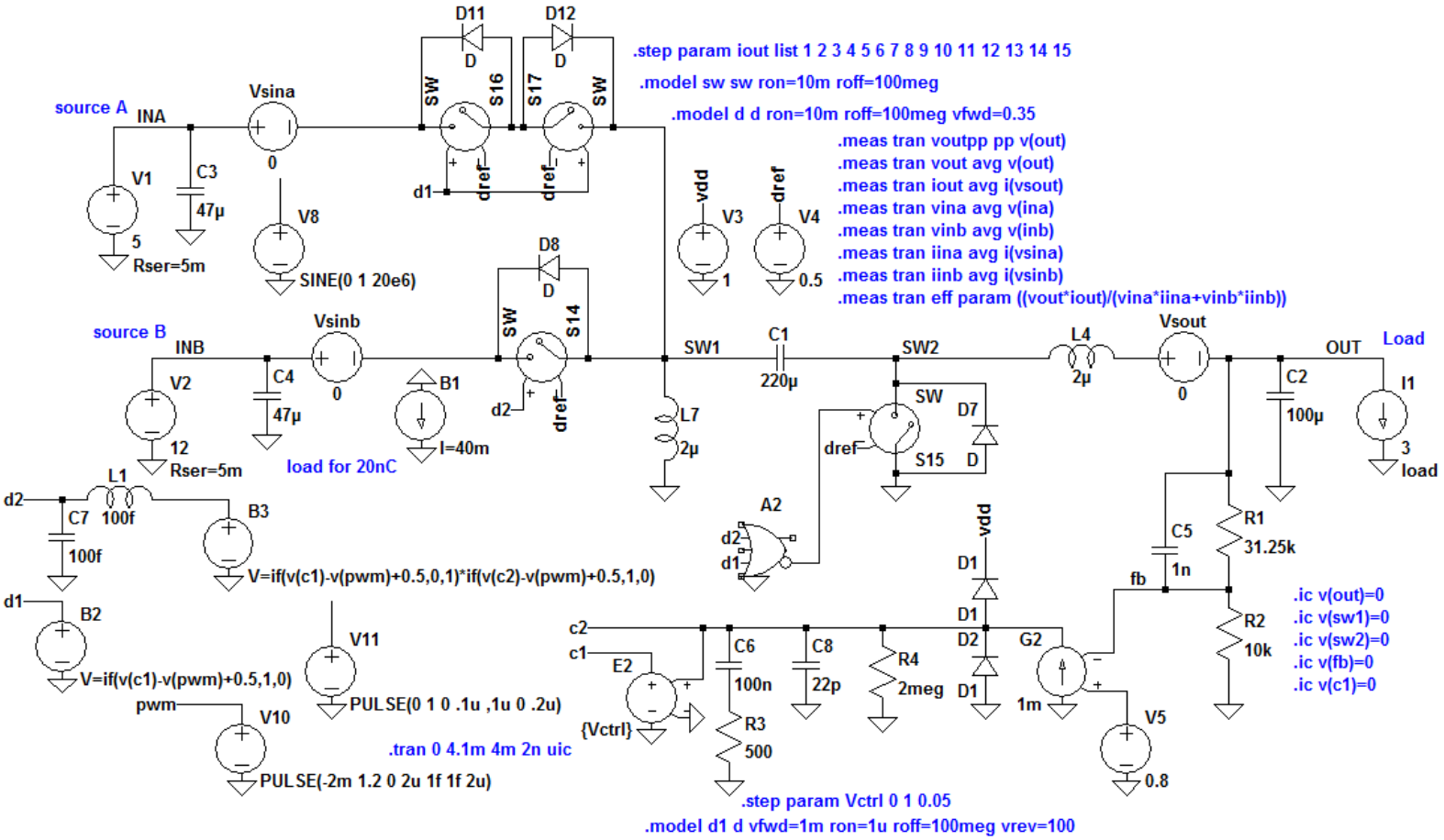

Figure 67. SPICE Circuit for Simulating the Efficiency of Dual-Input Zeta Converter Topology with In-Cycle Operation

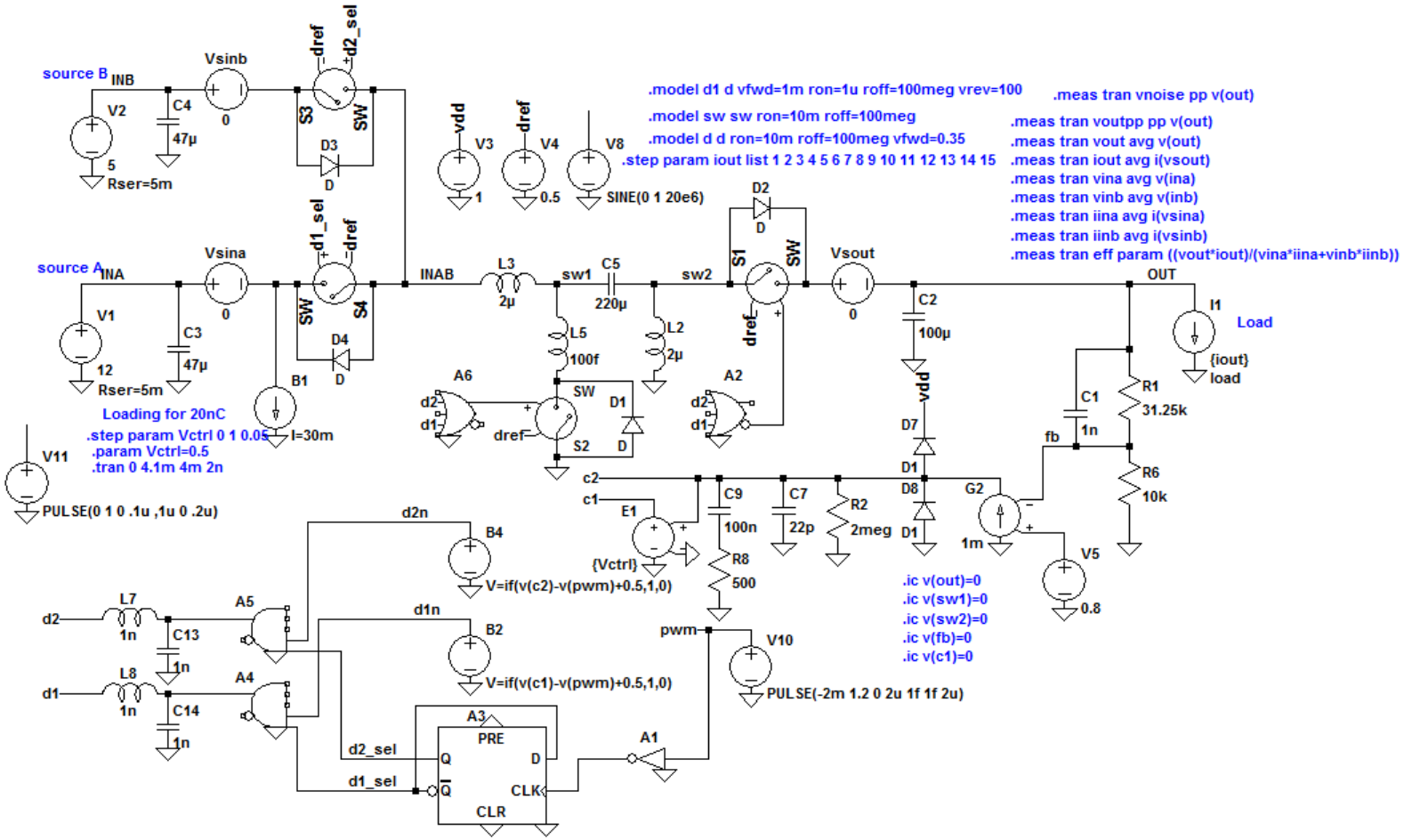

Figure 68. SPICE Circuit for Simulating the Efficiency of Alternate Dual-Input SEPIC Converter Topology with Cycle-By-Cycle Operation

Raw data results for the efficiency simulations are shown in Table 15 below followed by a list identifying which lines are associated with which power paths in Table 16. The dual power path approaches have higher efficiencies than the dual-input single power path topologies, but at the cost of increased size and complexity.

Table 15. Converter Efficiency Simulation Results

	1A	2A	3A	4A	5A	6A	7A	9A	10A	11A	12A	13A	14A	15A
1	82	89	91	91	91	91	90	90	89	88	88	87	86	85
2	89	93	94	95	95	95	94	94	94	93	93	92	92	91
3	89	93	94	95	95	94	94	94	93	93	92	92	91	91
4	81	87	89	88	88	87	85	84	83	81	80	79	77	76
5	84	89	90	89	88	87	86	84	83	81	80	78	77	75
6	85	91	92	92	92	92	91	90	89	88	88	87	86	85
7	86	91	92	93	92	92	91	90	90	89	88	87	86	86
8	88	92	93	93	92	92	91	90	89	88	87	86	86	85
9	86	91	92	92	92	91	91	90	89	88	87	86	85	84
10	89	93	93	93	93	92	91	91	90	89	88	87	86	85

Units are in %, actual data gathered with 2 decimal places of accuracy

Table 16. Converter Efficiency Simulation Results Line Meaning List

1	Dual four-FET buck boost
2	Dual SEPIC
3	Dual zeta
4	Dual-input four-FET buck-boost in-cycle operation
5	Dual-input four-FET buck-boost cycle-by-cycle operation
6	Dual-input SEPIC in-cycle operation
7	Dual-input SEPIC cycle-by-cycle operation
8	Alternate dual-input SEPIC
9	Dual-input zeta in-cycle operation
10	Dual-input zeta cycle-by-cycle operation

An analysis of the efficiency simulation results is shown in Table 17 and Table 18 rearranges the list from most efficient to least efficient on average. On the whole the four-FET topologies fared the worst in terms of efficiency compared to all other topologies. The most efficient are the dual SEPIC and dual zeta topologies, followed by the dual-

input SEPIC and dual-input zeta operated in cycle-by-cycle mode. Figure 69 shows a graph of the efficiency of each of these converter topologies with respect to load current. Given the increased size of the dual power path designs, it is entirely possible that if the single power path designs are scaled up to the same size that the efficiencies would become the same or better for the dual-input single power path topologies.

Table 17. Converter Efficiency Simulation Results Summary

	Average	Peak
Dual four-FET buck boost	88.09%	91.29%
Dual SEPIC	92.88%	94.78%
Dual zeta	92.77%	94.74%
Dual-input four-FET buck-boost in-cycle operation	82.58%	88.64%
Dual-input four-FET buck-boost cycle-by-cycle operation	83.01%	89.67%
Dual-input SEPIC in-cycle operation	88.78%	92.31%
Dual-input SEPIC cycle-by-cycle operation	89.26%	92.56%
Alternate dual-input SEPIC	89.01%	92.82%
Dual-input zeta in-cycle operation	88.62%	92.37%
Dual-input zeta cycle-by-cycle operation	89.60%	93.30%

Table 18. Converter Efficiency Simulation Results Summary Sorted by Average Efficiency

	Average	Peak
Dual SEPIC	92.88%	94.78%
Dual zeta	92.77%	94.74%
Dual-input zeta cycle-by-cycle operation	89.60%	93.30%
Dual-input SEPIC cycle-by-cycle operation	89.26%	92.56%
Alternate dual-input SEPIC	89.01%	92.82%
Dual-input SEPIC in-cycle operation	88.78%	92.31%
Dual-input zeta in-cycle operation	88.62%	92.37%
Dual four-FET buck boost	88.09%	91.29%
Dual-input four-FET buck-boost in-cycle operation	82.58%	88.64%
Dual-input four-FET buck-boost cycle-by-cycle operation	83.01%	89.67%

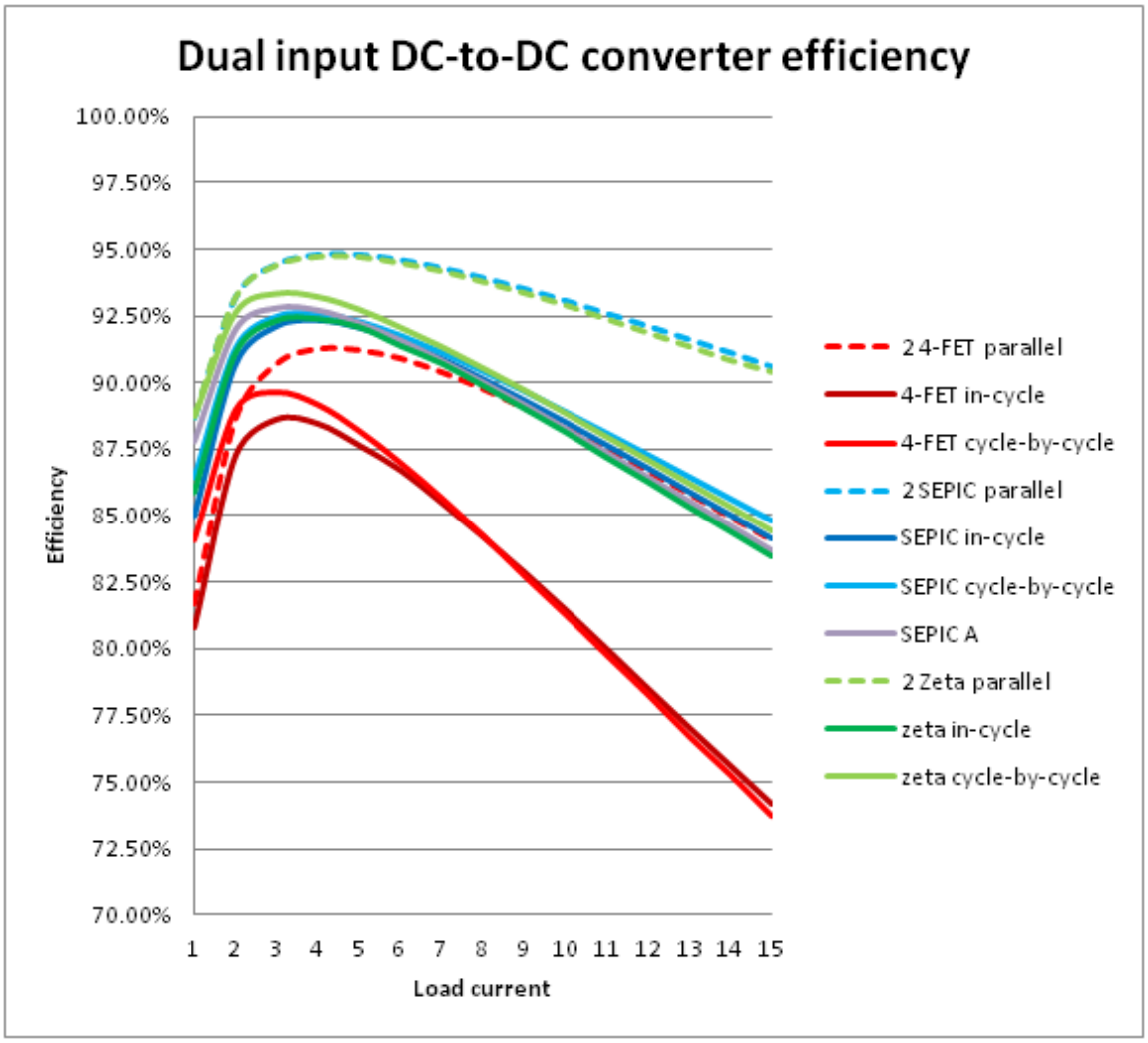

Figure 69. Dual-Input DC-to-DC Converter Power Path Efficiency with Respect to Input Current

CHAPTER FOUR: DUAL-INPUT DC-DC CONVERTER CONTROL SCHEMES

All of the common control schemes for DC-to-DC converters can be applied to dual-input converters with some modifications. For each implementation discussed in this paper there are alternate or more complex variations available with their own individual advantages and disadvantages. The objective of this chapter is to discuss methods of setting and controlling the input current ratio and to highlight how these types of converters can be controlled using voltage, current, and constant on-time control. Regulation of the output voltage is not substantially different that of from single-input converters with the primary difference being that the output of the control section includes information about when to turn on and turn off an extra switch for the two input power sources.

Input Current Ratio Control

This section focuses on how both in-cycle and cycle-by-cycle operation can control the input current ratio of the dual-input converter, and how the output voltage can be regulated using traditional control techniques such as voltage mode, current mode, and constant on-time control. The basic principles are independent of the chosen power path.

For each dual-input power path there are two input paths and a single output power path. The input switches are activated separately and conduction through each input state is a mutually exclusive event, which means that conduction through both input paths simultaneously is not allowed.

During the time when each input switch is turned on, current flows through that input leg and is drawn from the corresponding input power source. By controlling the

proportion of time during which one input switch is turned on versus the other input power switch, the ratio of input currents may be controlled. For the most part, the ratio of input currents between input legs is not dependent on the total output load current so long as the duty cycle control of the converter scales the two input current times in such a way that the ratio of input A to input B is maintained constant.

Figure 70 shows the input, inductor, and output current for a dual-input DC-to-DC converter with in-cycle operation, the concepts discussed here apply equally to cycle-by-cycle operation. The output voltage is controlled by the ratio shown by Equation (13) which is commonly referred to as the "duty cycle" or "duty ratio." To keep the ratio of average input currents roughly constant the ratio of input currents from input A and input B in Equation (14) should be kept constant. Should more precise control of the input current ratio be desired, a feedback loop can be included to adjust the ratio in Equation (14) to compensate for inefficiencies and more precisely keep the input current ratio constant.

$$D = \frac{T_{in}}{T_{out} + T_{in}} \tag{13}$$

$$Input\ Ratio = \frac{T_{in\_A}}{T_{in\_B}} \tag{14}$$

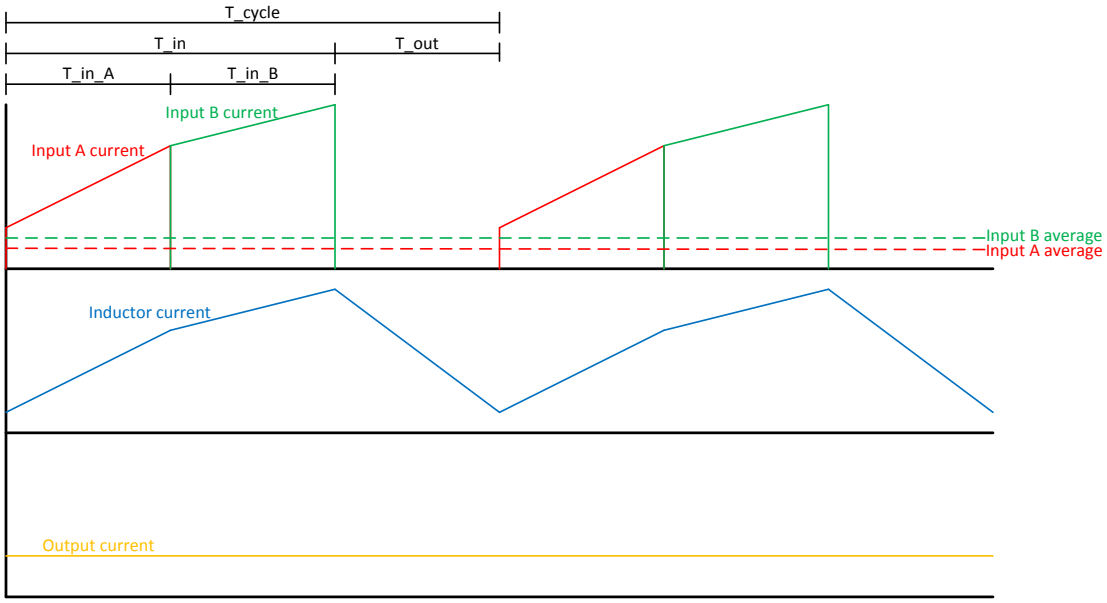

Figure 70. Dual-Input DC-to-DC Converter Current Waveforms for In-Cycle Operation

Cycle-by-cycle operation presents some different timing considerations but the underlying principles are the same. The total cycle time is defined as T_{cycle}. The duty ration, however, is now a composite quantity which can be represented as in Equation (15). For simplicity the control algorithm may set T_{offa} to equal T_{offb}. Keeping the ratio of T_{ina} to T_{inb} constant will keep the input current roughly constant. Measuring the input currents and adjusting to compensate for inaccuracies or inefficiencies can further improve control over the input current ratio. The output voltage is then regulated by varying the duty ratio which can be done without altering the input current ratio. Figure 71 below shows the timing waveforms described for a cycle-by-cycle operation.

$$D = \frac{T_{ina} + T_{inb}}{T_{offa} + T_{offb} + T_{ina} + T_{inb}} \tag{15}$$

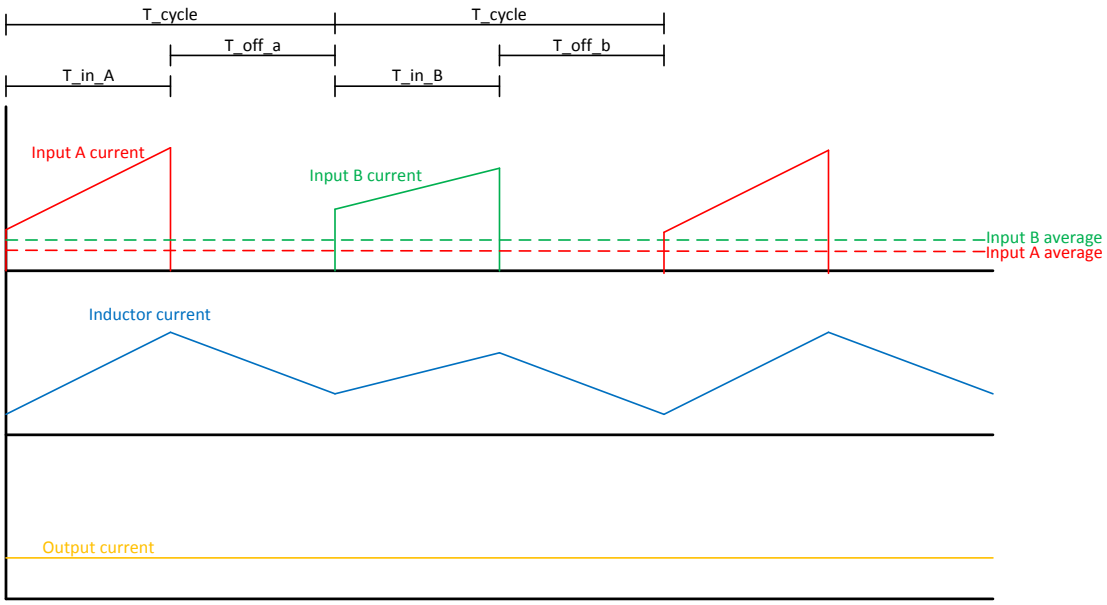

Figure 71. Dual-Input DC-to-DC Converter Current Waveforms for Cycle-By-Cycle Operation

Simulations are done to demonstrate how closely the input current ratio follows the on-time ratio for both in-cycle and cycle-by-cycle control modes. The dual-input four-FET buck-boost topology is used in voltage mode control for this example. Three different on-time ratios are used (25%/75%, 50%/50%, and 75%/25% for 5V/12V), and the output current is swept from 1A to 15A in 1A steps. Figures 72, 73, and 74 show the results for in-cycle control and Figures 77, 78, and 79 show the results for cycle-by-cycle control. The graphs below show the two input currents plotted as a function of load current along with the target current ratio as set by the ratio of on-times between the two inputs.

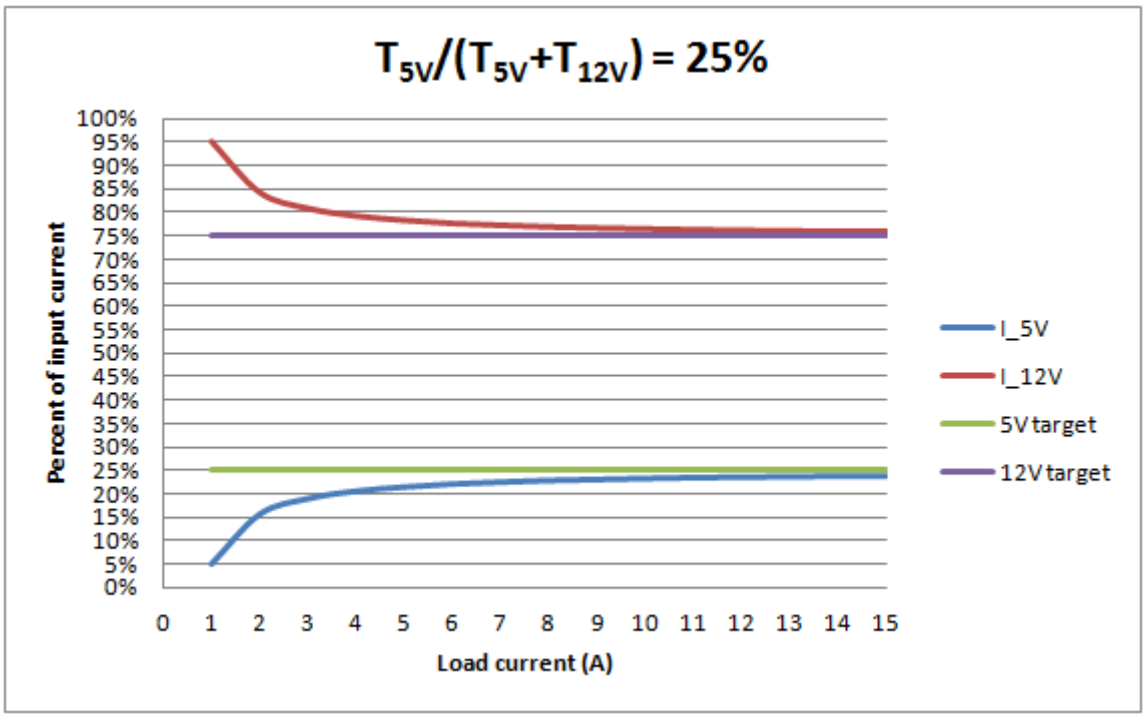

Figure 72. Input Current Sharing Results for In-Cycle Mode 25% from 5V and 75% from 12V

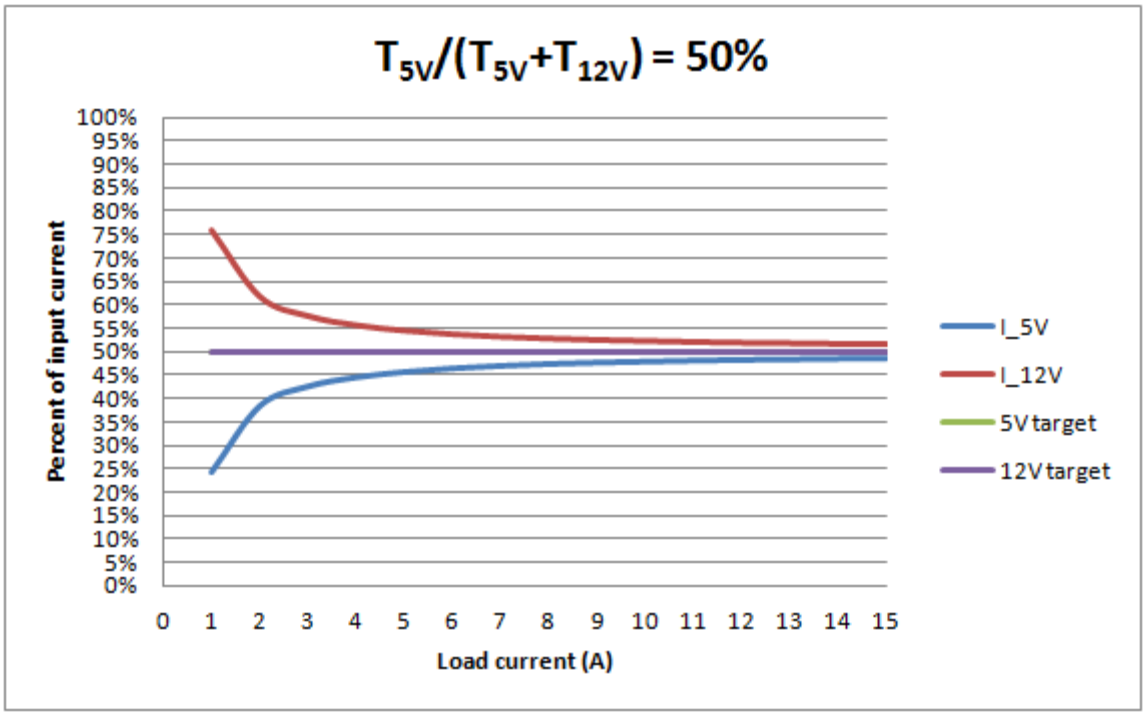

Figure 73. Input Current Sharing Results for In-Cycle Mode 50% from 5V and 50% from 12V

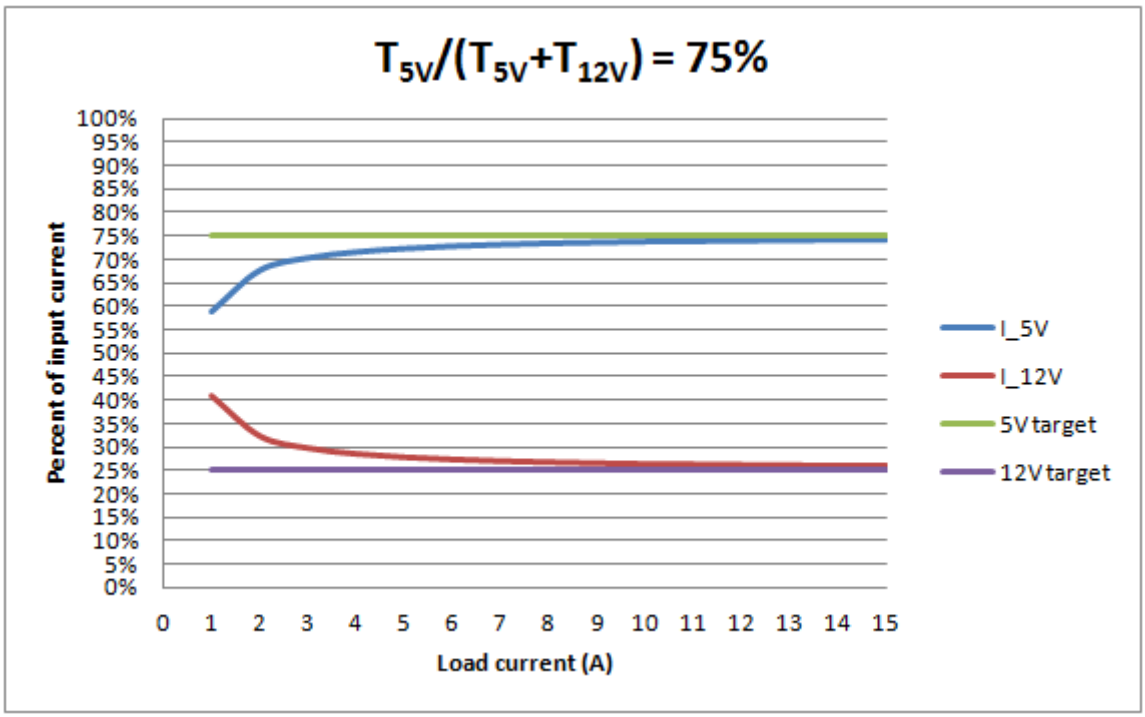

Figure 74. Input Current Sharing Results for In-Cycle Mode 75% from 5V and 25% from 12V

For in-cycle operation the accuracy of the actual input current ratio is within 5% for currents above 3A to 4A. For applications which only care about having accurate input current sharing ratios at the maximum current, this may be acceptable. The addition of a control loop that senses the input current ratio and offsets the on-time ratio to compensate for this error would greatly improve the accuracy of input current sharing when using in-cycle operation.

The reason for this error with in-cycle operation is that the input current waveform is not symmetrical between the A and B inputs as a result of not having a discharge cycle between them as is the case for cycle-by-cycle operation. Figure 75 demonstrates this. Even though the on-time for each input is the same, the average current for the B input will be greater than for the A input. Figure 76 shows how this offset is not present when using cycle-by-cycle control as there is an inductor discharge

cycle between each input cycle, which causes the average input currents to more closely match.

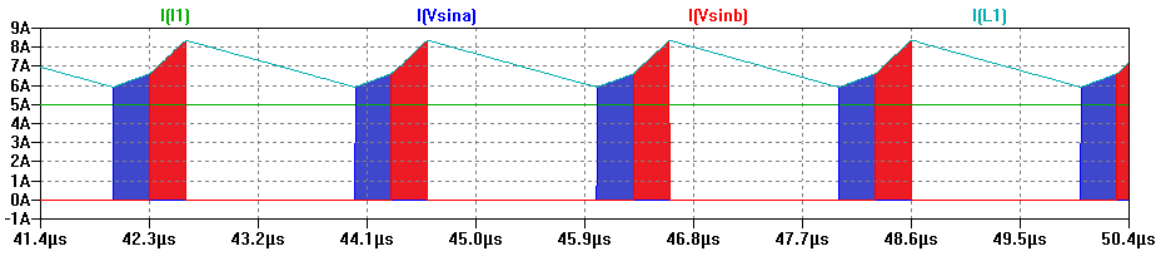

Figure 75. Input Current Sharing Offset for In-Cycle Operation

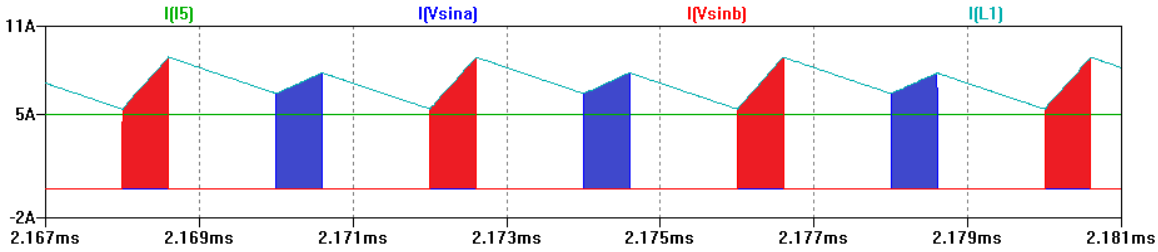

Figure 76. Input Current Sharing Offset for Cycle-By-Cycle Operation

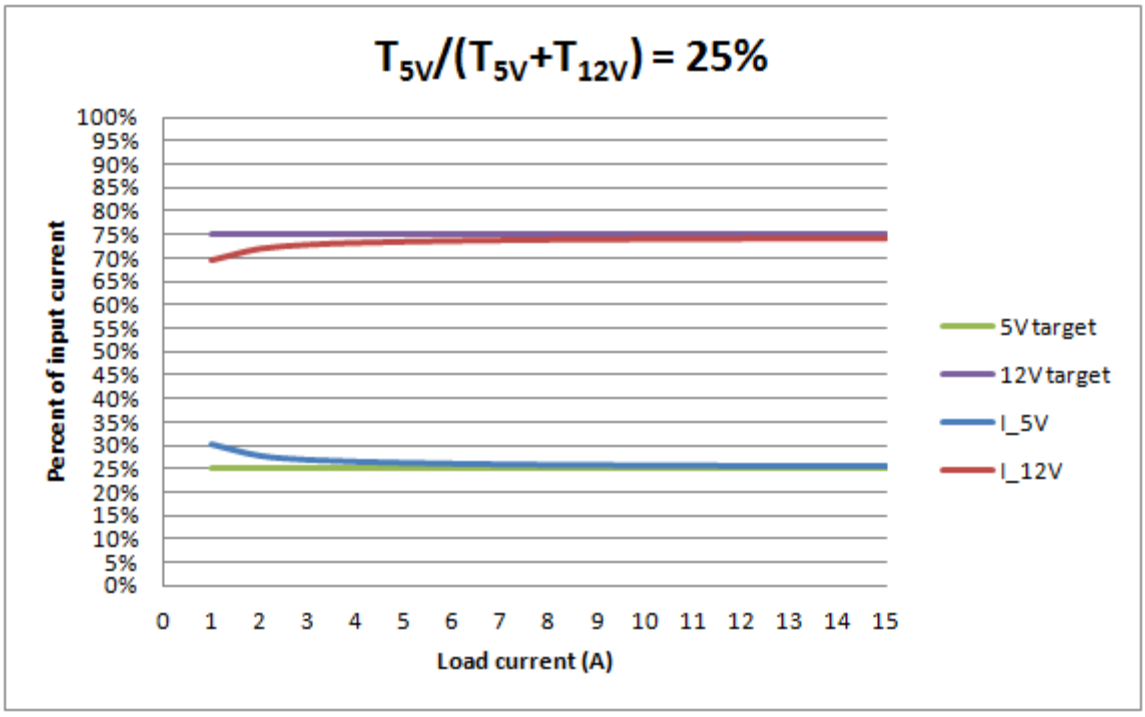

Figure 77. Input Current Sharing Results for Cycle-By-Cycle Mode 25% from 5V and 75% from 12V

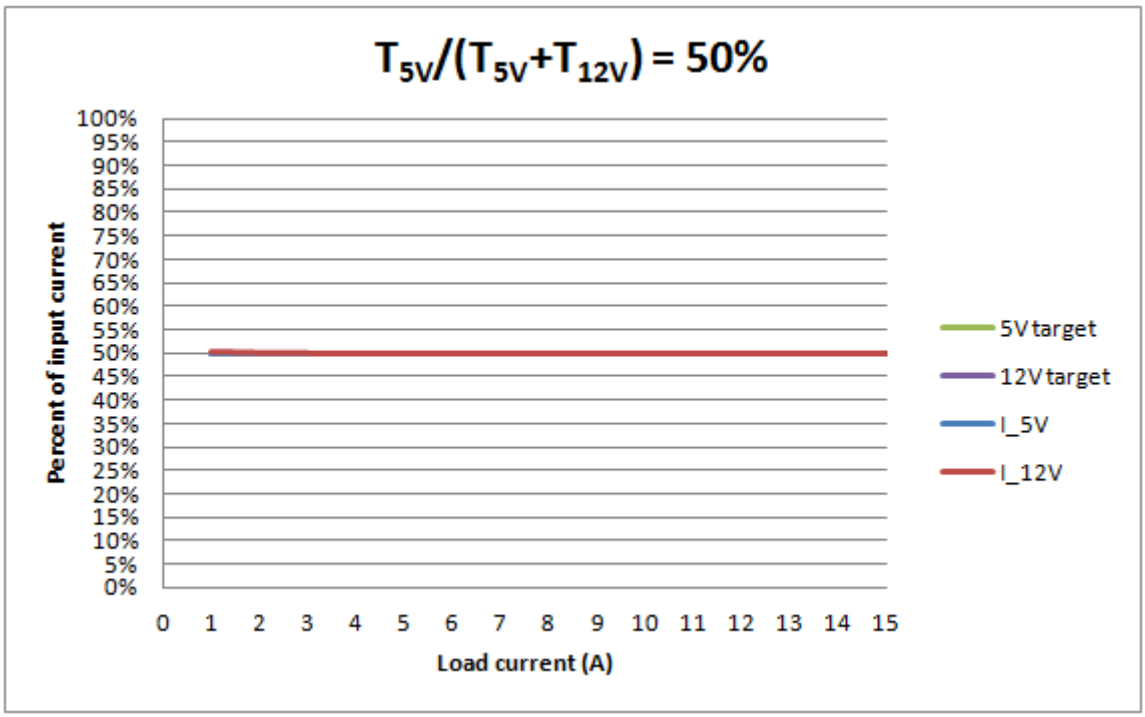

Figure 78. Input Current Sharing Results for Cycle-By-Cycle Mode 50% from 5V and 50% from 12V

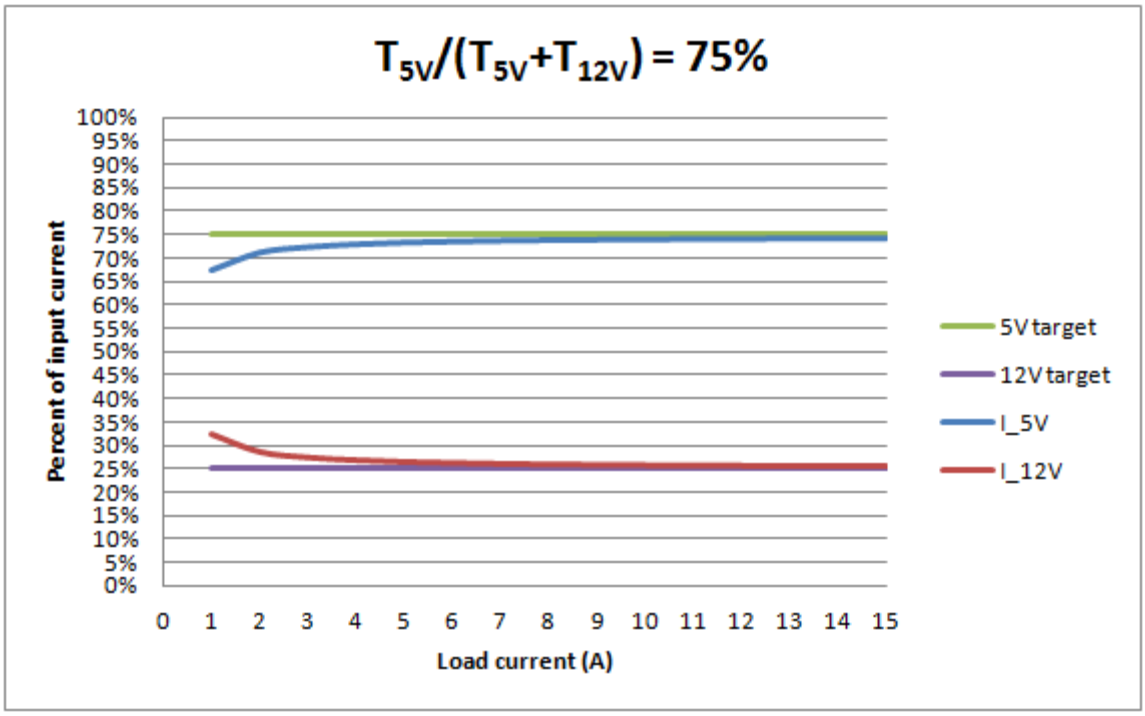

Figure 79. Input Current Sharing Results for Cycle-By-Cycle Mode 75% from 5V and 25% from 12V

In the case of cycle-by-cycle operation the input current sharing very closely matches the on-time ratio of the inputs for currents above 2A. For ratios near 50/50 the sharing is good down to very low currents, and the error at low currents tends to skew the current sharing towards a 50/50 ratio. As with the in-cycle case, the addition of input current sensors and a control loop to adjust the on-time ratio could further improve the accuracy of setting the input current ratio.

To demonstrate the linearity of the control over the input current ratio provided by adjusting the on-time ratio for each input power source a simulation sweep is done where the load current is kept constant and the on-time ratios were varied. For this simulation the dual-input four-FET buck-boost topology is again used with a fixed 3A load current. The results in Figures 80 and 81 show a mostly linear response with the same offset seen in the above simulations when using in-cycle operation.

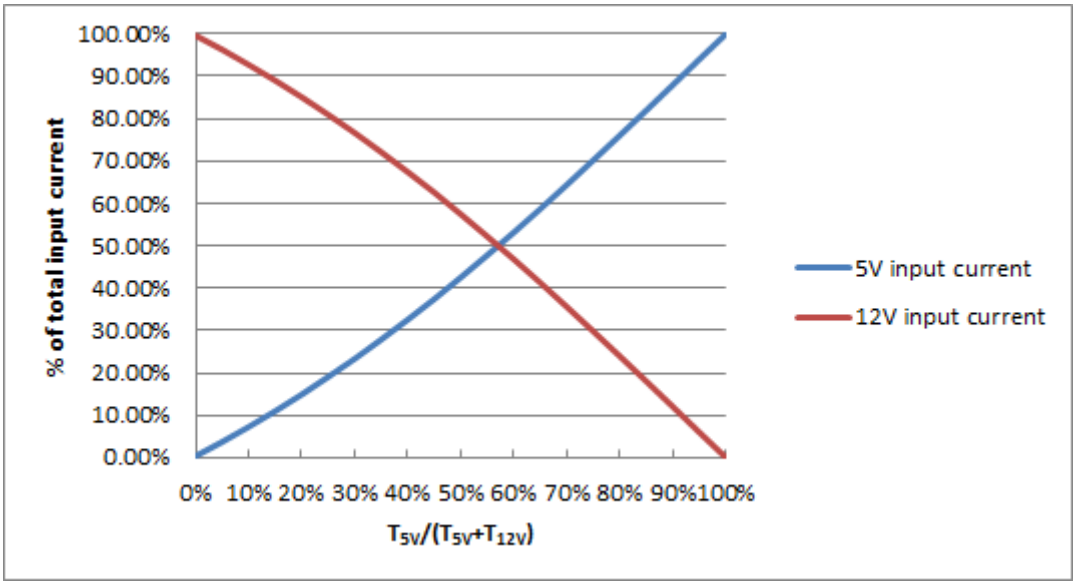

Figure 80. Input Current Sharing Control Linearity for In-Cycle Mode

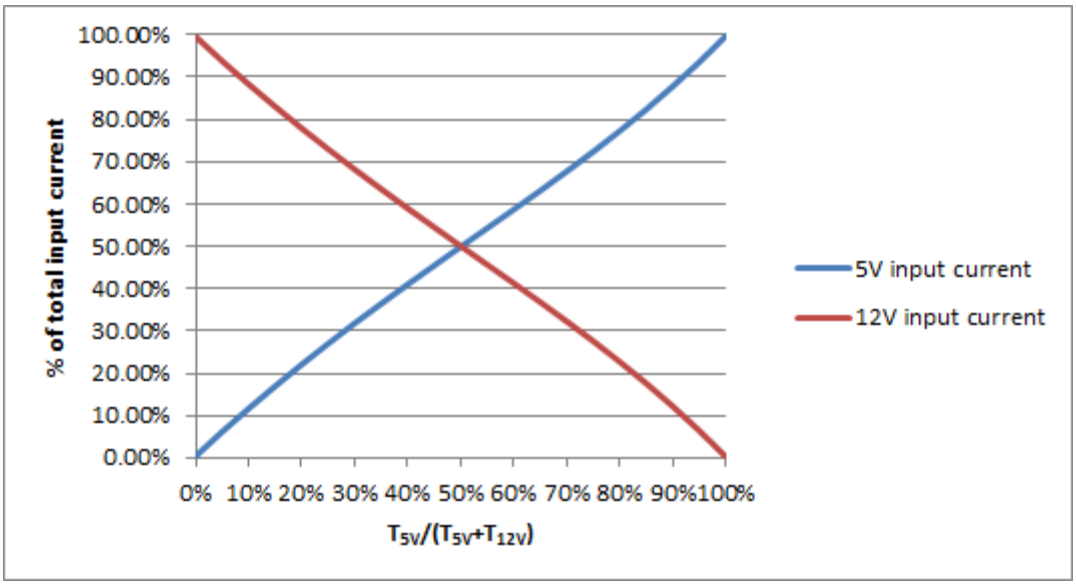

Figure 81. Input Current Sharing Control Linearity for Cycle-By-Cycle Mode

The input power is a function of both voltage and current. So long as the input voltage remains relatively constant the input power ratio can be set in the same way. If the input voltage varies such as in a battery-driven application the input power ratio may tend to shift excessively without the aid of a sense and control scheme to compensate for changes in the input voltage.

Voltage Mode Control

Voltage mode control can be achieved for a dual-input DC-to-DC converter much the same way as for single-input converters. Figure 82 presents an example implementation of voltage mode control of a dual-input converter with open-loop control over the input current ratio. The power path shown as a generic block as this example can apply to any power path topology although the compensation requirements may vary. The logic block is shown as a generic block as well because the implementation of the logic portion of the control can vary depending on the power path and other features being implemented such as soft-start and enable functions.

A single set of feedback resistors senses the output voltage and feeds this into an error amplifier which compares this feedback voltage to a fixed reference just as in the single-input converter case. The output of the error amplifier is split by two voltage dividers. The output of each divider is fed into a comparator which compares them to a common sawtooth wave. By doing this, the resistor dividers may be adjusted such that one comparator will output a different duty ratio than the other for a given output level of the error amplifier. As the output of the error amplifier moves up and down, the ratio of the pulse widths created by the comparators will be kept constant, thus providing open-loop control over the input current.

Compensation is not shown in Figure 82. However, it would typically be placed on the output of the error amplifier and sometimes an additional feedforward capacitor is placed in parallel with the top feedback resistor labeled FBR1 in Figure 82. Given the resistor dividers hanging off of the output, a buffer (voltage follower) amplifier may be added in series to prevent the resistor dividers from loading the error amplifier and thereby impacting the compensation.

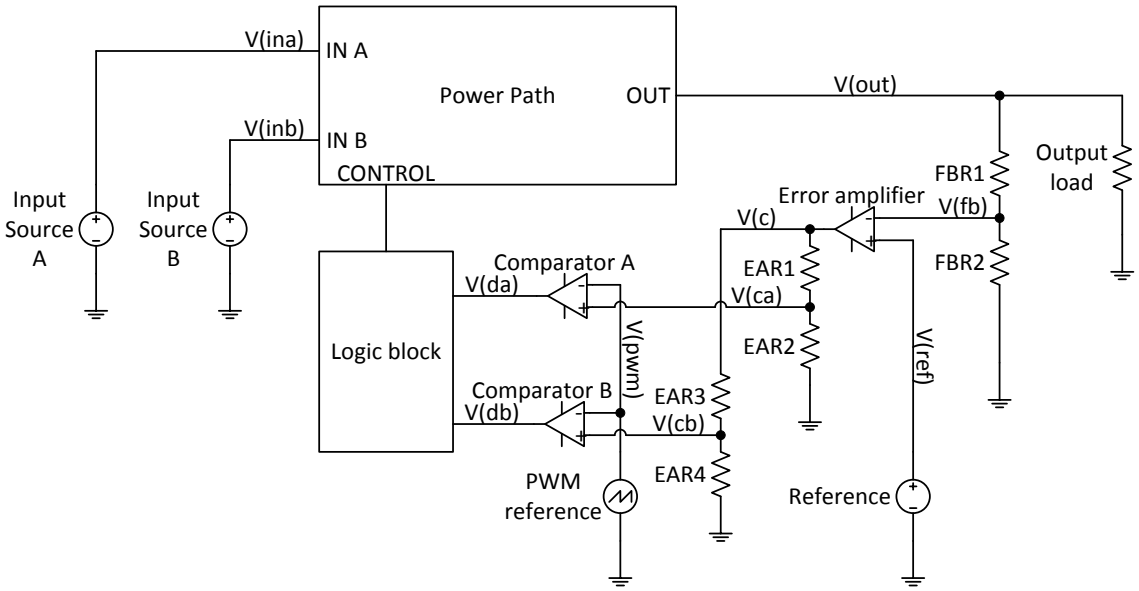

Figure 82. Example of Voltage Mode Control of a Dual-Input DC-to-DC Converter

To demonstrate voltage mode control in a dual-input converter a simulation is done on the dual-input zeta converter using cycle-by-cycle operation. This is the same simulation done to verify the operation of the zeta converter power path with the difference being that the load step conditions have changed. A load of 2A is placed on the output of the converter, it is transitioned to 4A and then back to 2A to show how the output voltage is effected. The converter compensation has been adjusted to reduce the deviation of the output voltage. Figure 83 shows a diagram of the control loop and Figure 84 shows the resulting output waveforms. In this example the buffers both being one-to-one will result in the input current sharing ratio being fifty/fifty. If a scaling other than one-to-one is introduced into the buffers the input current sharing ratio would be changed. The peak-peak output voltage for this example is 183mV.

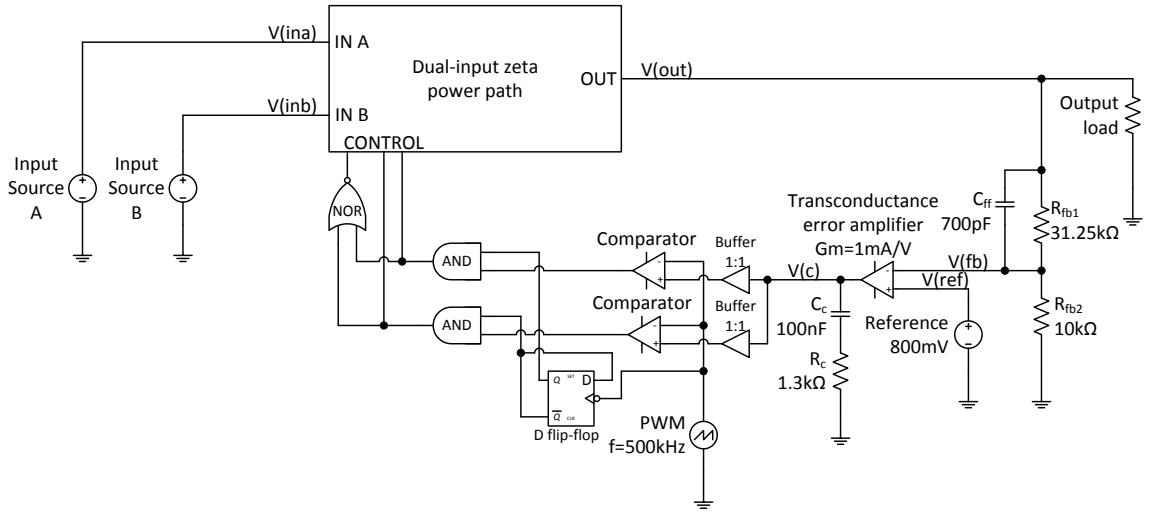

Figure 83. Example Voltage Mode Control Diagram

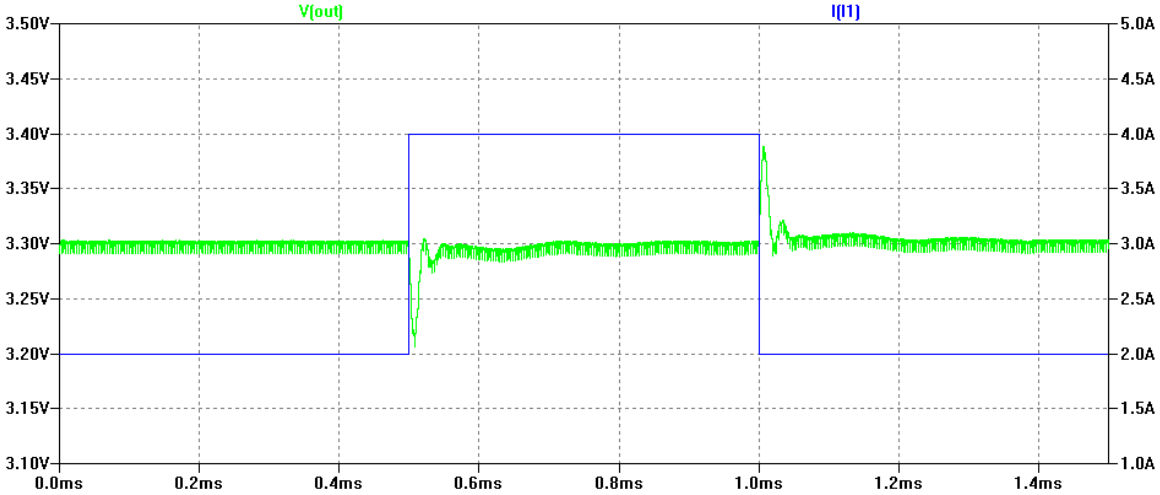

Figure 84. Example Voltage Mode Control Waveforms

Current Mode Control

The primary difference between voltage and current mode control is the addition of an inner current feedback loop within the overall voltage mode feedback loop. Using the example from Figure 82, a current sense output from the power path can be added and that feedback taken to the PWM comparators which must be changed to three input comparators. This creates the peak current mode control regulator shown in Figure 85

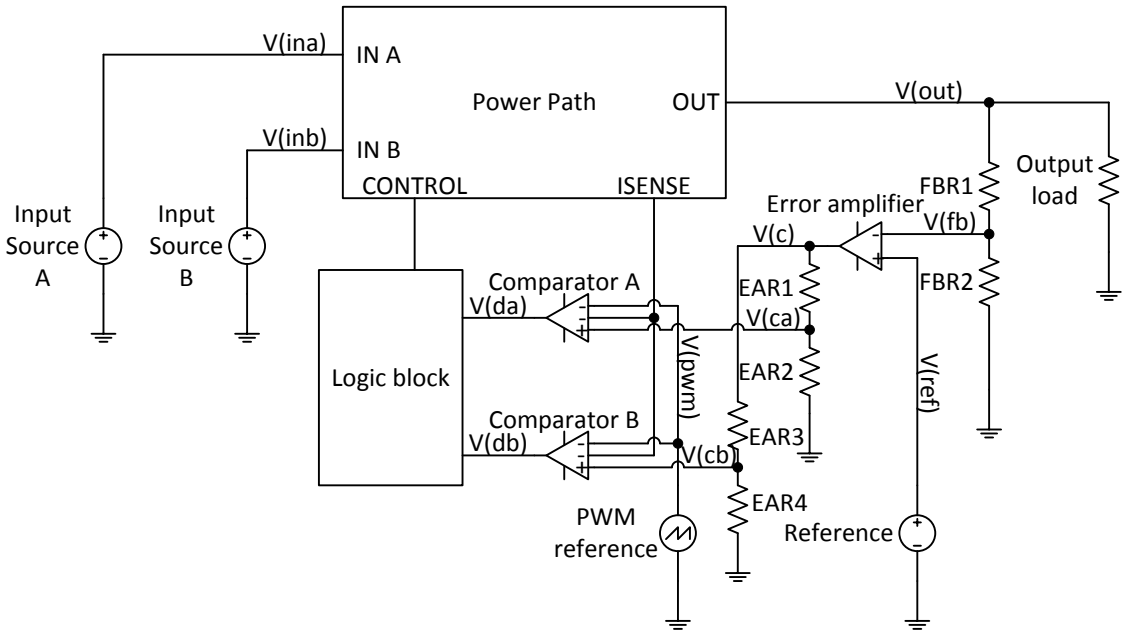

Figure 85. Example of Current Mode Control of a Dual-Input DC-to-DC Converter

As an example of current mode control, the voltage mode example is modified with an extra control loop to become a current mode design. The added sense connection from the power path is a current sensor placed in series with the output inductor. Figure 86 shows this design and Figure 87 shows the resulting transient response. The ratio of the input currents in this design is not set by the gain ratio of two buffers, but by the spacing of the pulses in the 500kHz pulse generator. When the pulses are all evenly spaced the ratio is 50/50. If the pulses spacing is made to alternate between two different times then the ratio of those times would set the ratio of the input currents. In this case the peak-peak output voltage is reduced to 90mV compared to 183mV with voltage mode control.

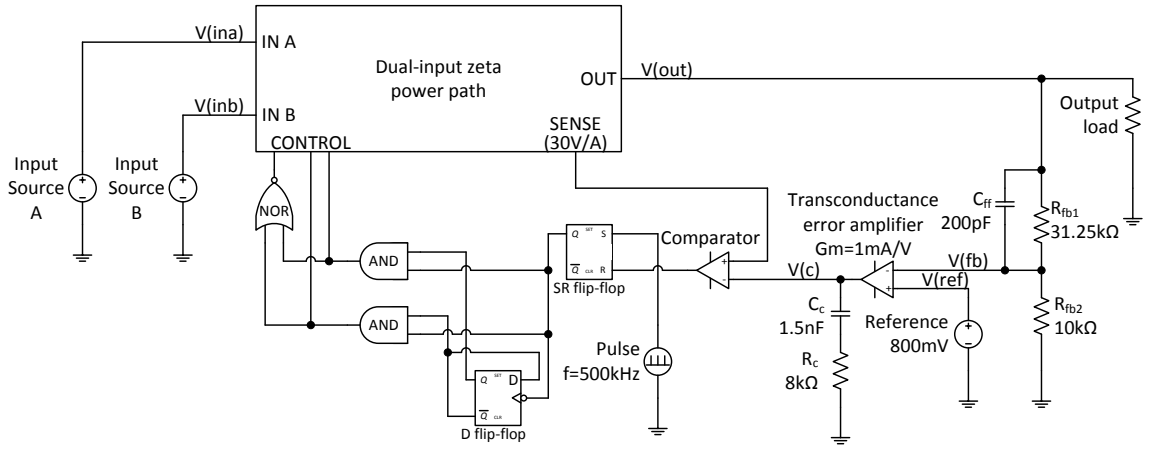

Figure 86. Example Current Mode Control Diagram

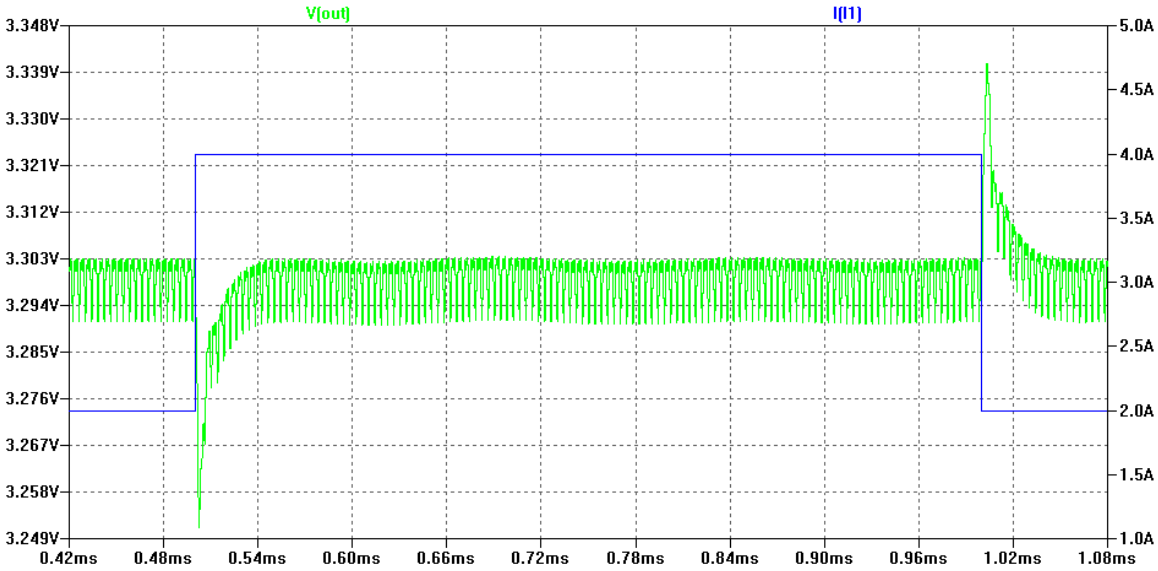

Figure 87. Example Current Mode Control Waveforms

Constant On-Time Control

Constant on-time control is different than voltage or current mode control in that the error amplifier is replaced with a comparator. The output of this comparator signals whether the output is above or below the setpoint.

The output of the comparator is essentially a digital signal and as such many schemes of using this information can be envisioned. For example, to implement cycle-by-cycle operation current can be drawn from each power source every other cycle, a pair

of resistors could theoretically be used to tune the on-time for each input source and thereby control the ratio of the input currents. Figure 88 shows this example implementation.

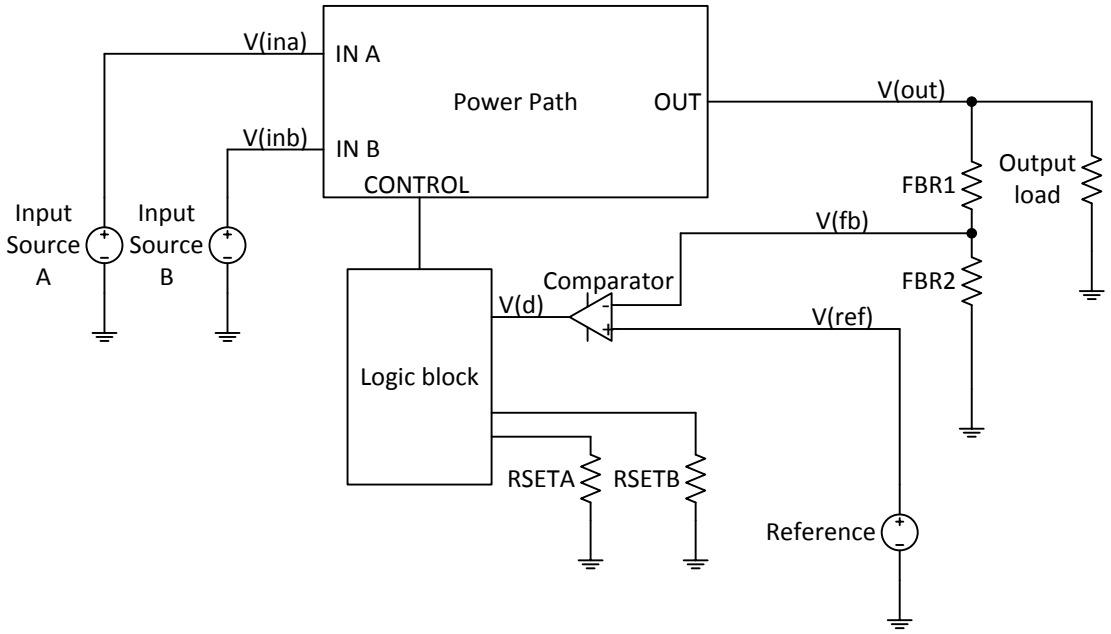

Figure 88. Example of Constant On-Time Control of a Dual-Input DC-to-DC Converter

To illustrate the operation of constant on-time control compared with voltage and current mode control, an example simulation with the same zeta converter as used previously is shown in Figure 89 with corresponding waveforms shown in Figure 90. A connection from SW2 is provided on the power path block showing where the R1 and C1 network is placed across the output inductor of the zeta converter. This design is only capable of an input current sharing ratio of fifty/fifty, the circuit would become substantially more complicated if other ratios were required. The resulting noise for this converter is only 75mV. Table 19 shows a comparison of the three control scheme examples.

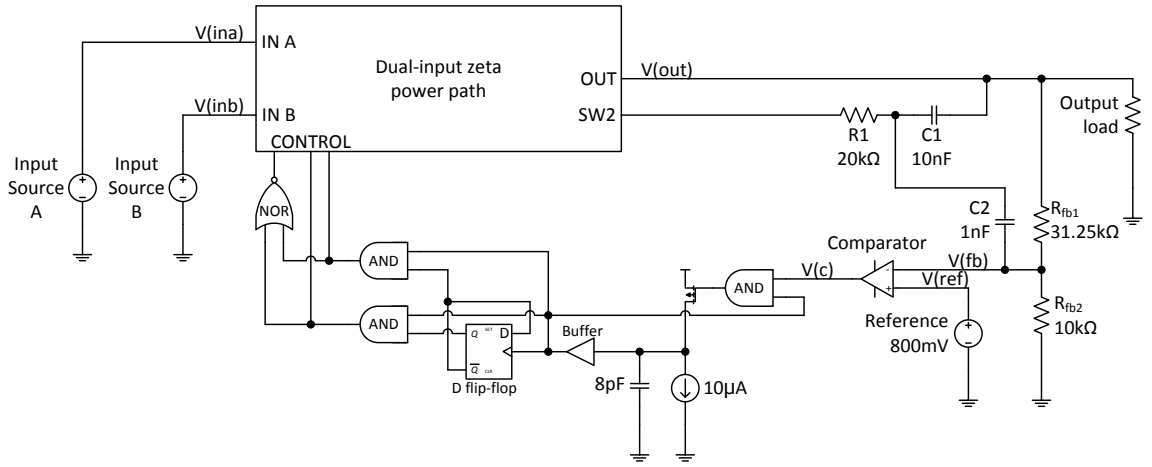

Figure 89. Example Constant On-Time Control Diagram

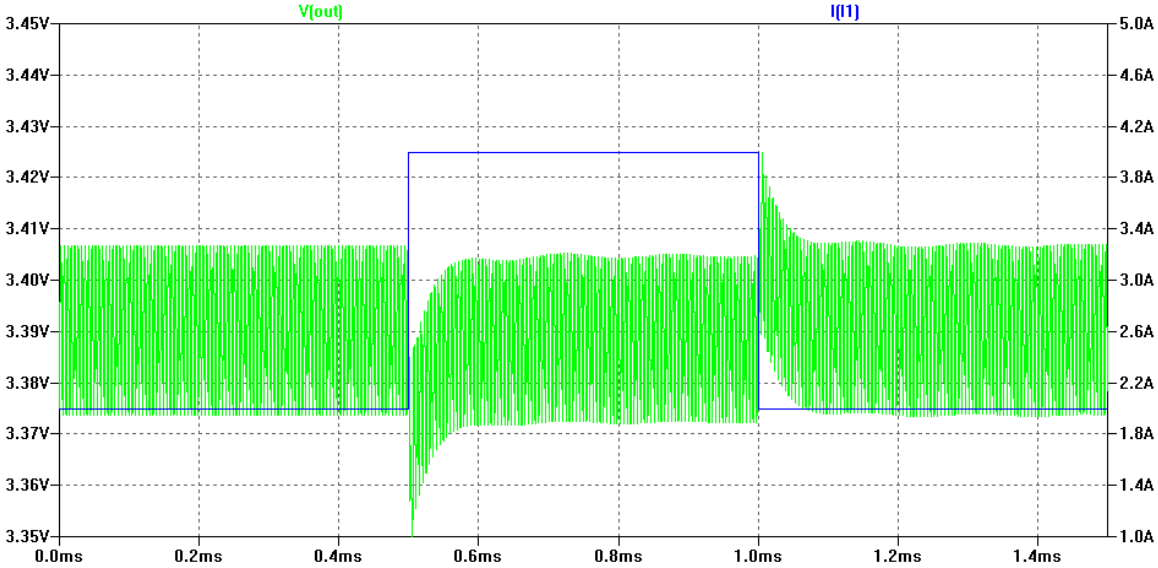

Figure 90. Example Constant On-Time Control Waveforms

Table 19. Example Control Comparison

	Ripple (Vpp)	Noise (Vpp)
Voltage mode	11mV	183mV
Current mode	12mV	90mV
Constant on-time	34mV	75mV

The results in Table 19 show that the overall noise is lowest for the constant on-time converter and highest for the voltage mode converter, which is in line with conventional wisdom for these converters. Overall noise is considered to be the peak to

peak total voltage variation during the load step test, and therefore includes both the ripple voltage and the under-shoot and over-shoot effects. The ripple should be the same for all three control schemes. However, a bug in the constant on-time design used for this proof of concept resulted in a higher ripple voltage which may have added an extra 20mV to the total noise result.

CHAPTER FIVE: DESIGN EXAMPLE

Design Overview

To illustrate the operation of a dual-input converter one of the previously discussed converters is simulated in LTSpice using SPICE models of real-world components. The power path itself and digital control are simulated using real component models, while the analog feedback error amplifier and comparators are simulated using ideal models to reduce simulation time. The selected converter is a dual-input zeta converter with voltage mode control operated in cycle-by-cycle mode. Real-world components selected for this design example have properties similar to those in the previous chapter.

Exploring the performance of the design includes looking a number of performance parameters. The efficiency is looked at across the full range of loads and different input current ratios. Output noise is broken down into voltage ripple and dynamic noise where voltage ripple noise is measured across the full range of load currents. Dynamic noise is measured by a load transient which switches between the minimum and maximum load current. The input current ratio is tested across multiple settings and a range of load currents.

Requirements

To demonstrate how a dual-input converter can take input voltages both above and below the output voltage the input voltages are selected at 12V and 5V while the output voltage is set at 5V. The load current ranges from 0A to 10A. These and other

requirements are detailed in Table 20 Additionally the design is restricted to components that can purchased at the time of this writing and which are surface-mount parts.

Table 20. Converter Example Design Requirements

Requirement	Spec
Input source 1 voltage	12V
Input source 2 voltage	5V
Output voltage	5V
Output current range	0A – 5A
Output noise Vpp	10%

Power Path

The power path topology is a dual-input zeta converter using P-channel MOSFETs for the input switches and an N-channel MOSFET for the output switch. Low-side MOSFET drivers were used to turn the switches on and off. Table 21 shows the components selected for the power path and Figure 91 shows a diagram of the power path for reference. Figure 92 shows the actual schematic of the example design and Figure 93 shows the waveforms of the power path portion of the converter. The voltage on input one is 12V and the voltage on input two is 5V.

Table 21. Converter Example Design Power Path Components

Part	Vendor	MPN	Quantity
N-channel MOSFET	International Rectifier	IRF8721	1
P-channel MOSFET	International Rectifier	IRFHM9391	4
Diode	NXP Semiconductor	PMEG3010	5
MOSFET driver	Linear Technology	LTC4440	3
Inductor	Wurth Electronics	7443340150	2
Capacitor	Murata Electronics	GRM32ER71E226ME15	24

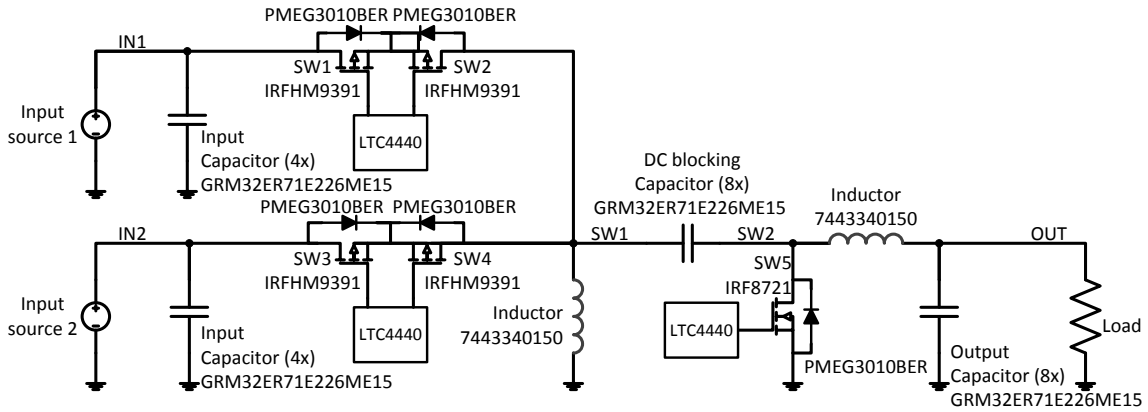

Figure 91. Dual-Input Converter Example Power Path Design

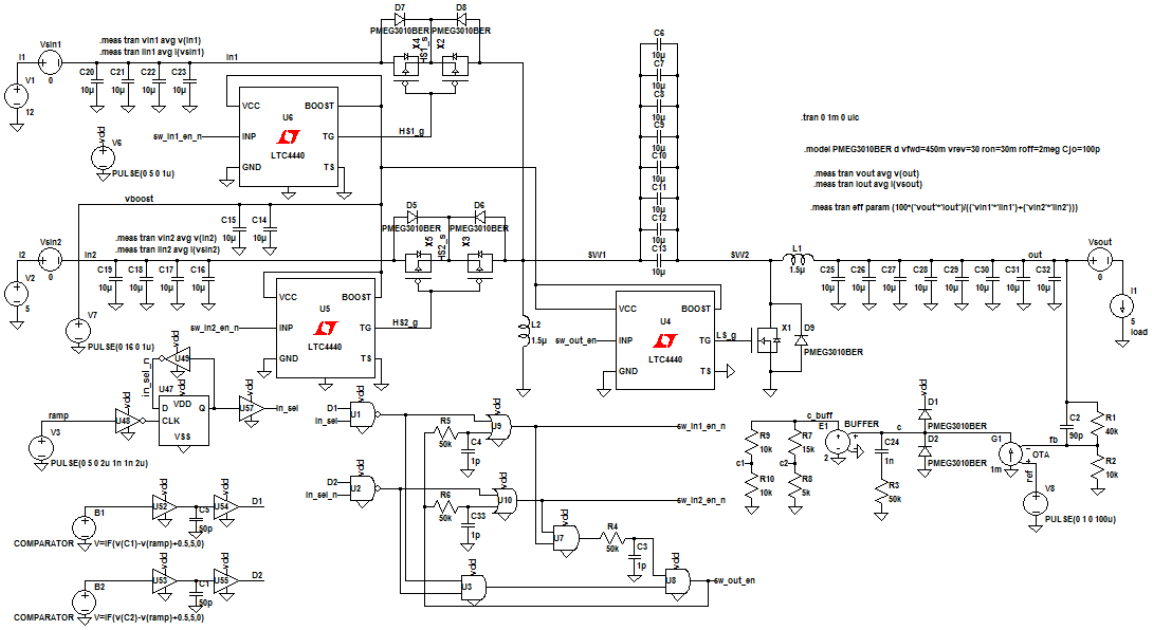

Figure 92. Dual-Input Converter Example LTSpice Schematic

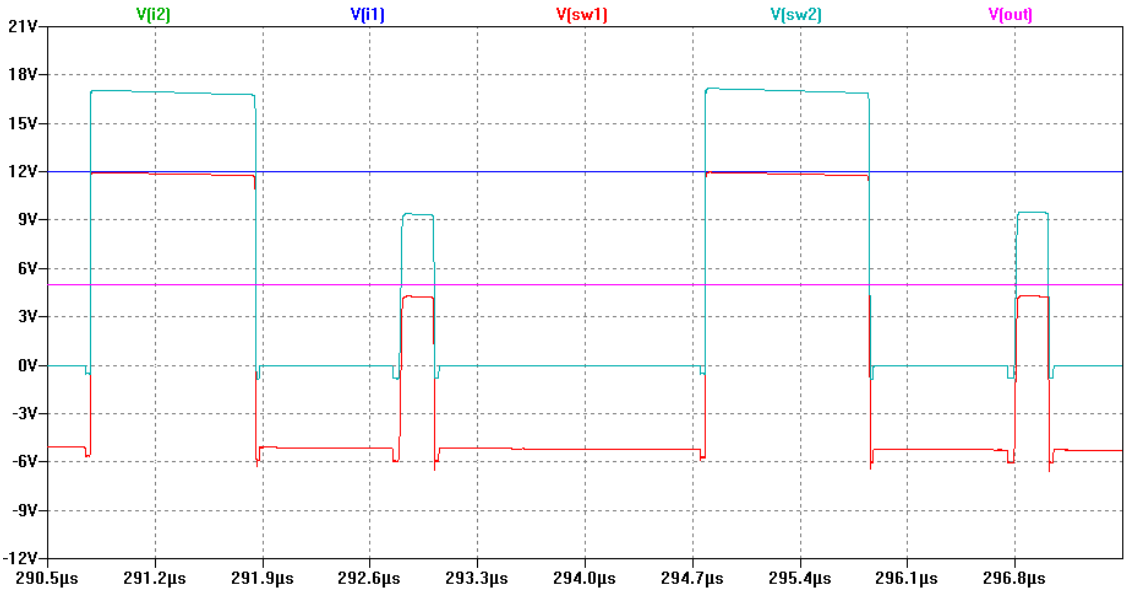

Figure 93. Dual-Input Converter Example Power Path Waveforms

Back-to-back FETs were implemented on both inputs to provide an additional degree of blocking to prevent reverse currents from flowing into the input power sources. The MOSFET drivers in this design require a bootstrap voltage to operate which is supplied by a 16V bootstrap supply modeled by an ideal voltage source in this simulation. In a real implementation the 16V bootstrap supply could be provided by a low power charge pump IC. Table 22 shows each components properties compared with the assumptions made in previous chapters and Table 23 shows the same for the components parasitic properties. The ideal value column is for the values from previous chapters, the design value column is for the components used in this design example. The equivalent design values for capacitors takes into account the number of capacitors placed in parallel in the design. MOSFET properties are listed per device.

Table 22. Converter Example Design Component Properties

Parameter	Ideal value	Design value
Inductor inductance	2µH	1.5µH
DC blocking capacitor capacitance	220µF	176µF
Input capacitor capacitance	47µF	88µF
Output capacitor capacitance	100µF	176µF

Table 23. Converter Example Design Component Parasitic Properties

Parameter	Ideal value	Design value
FET on resistance	10mΩ	N-channel: 6.9mΩ P-channel: 11.7mΩ
FET off resistance	100MΩ	N-channel: 25MΩ P-channel: 25MΩ
FET gate charge	20nC	N-channel: 8.3nC P-channel: 32nC
Diode on resistance	10mΩ	30mΩ
Diode forward voltage	350mV	450mV
Diode off resistance	100MΩ	2MΩ
Inductor DC resistance	10mΩ	4.4mΩ
DC blocking capacitor series resistance	10mΩ	1.25mΩ
Input capacitor series resistance	1mΩ	2.5mΩ
Output capacitor series resistance	1mΩ	1.25mΩ

Shoot-through current must be accounted for in this design which is not an issue when working with switch models that have instantaneous turn-on and turn-off times as in the previous chapters. This happens as a result of the switches having both a delay in the transition from on state to off state, and having a gradual turn-on or turn-off time rather than an instantaneous one. If not accounted for there can be a brief time during which both a high side (input) switch and a low side (output) switch are turned on to some degree which results in a momentary short circuit between the input power source and ground. This is accounted for by inserting a time in the cycle during which all switches are turned off and which allows one switch to finish turning off before the next turns on. This is described in the logic block section.

Logic Block

The logic block in this design controls the MOSFET switches according to the output of a PWM generator which is controlled by the error amplifier. For this design the

logic block implements cycle-by-cycle control and adds dead time between the turn on of input and output switches.

Simulation of the logic block is done using MOSFET level models of off the shelf PCB mounted logic gates. Figure 94 shows the logic section of the design. The MOSFET drivers inputs are active high, however, because the input side MOSFETs are P-channel a high level on the gate turns them off. Therefore the output signals of the logic block are active low for the input MOSFETs and active high for the output MOSFET. The inputs to the logic block are the two control signals put out by the error amplifier.

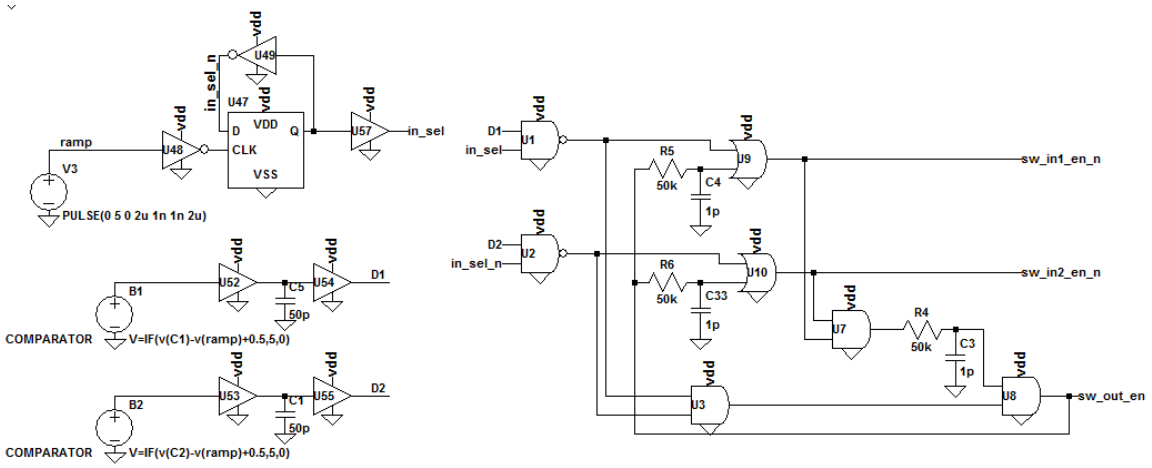

Figure 94. Dual-Input Converter Example Logic Block Schematic

The voltage source V3 represents a ramp generator which in a real design could be implemented with a 555 timer circuit. Two behavioral voltage sources B1 and B2 are used to represent comparators which compare the control signals from the error amplifier against the output of the ramp generator generate the PWM signal. As this is a cycle-by-cycle implementation, a select signal alternates between ramp cycles which is used to determine which input power source is being used during a given cycle. Some buffers are then used delay match the D1 and D2 signals to line up with the in_sel signal.

To generate the proper logic levels for the MOSFET drivers and insert some dead time, a network of logic gates takes in the D1, D2, and in_sel_n signals and generates the output signals to the MOSFET drivers. There are internal feedback loops in this circuit with built-in delays that insert a dead time which prevents shoot-through. Figure 95 shows the waveforms of this circuit in operation.

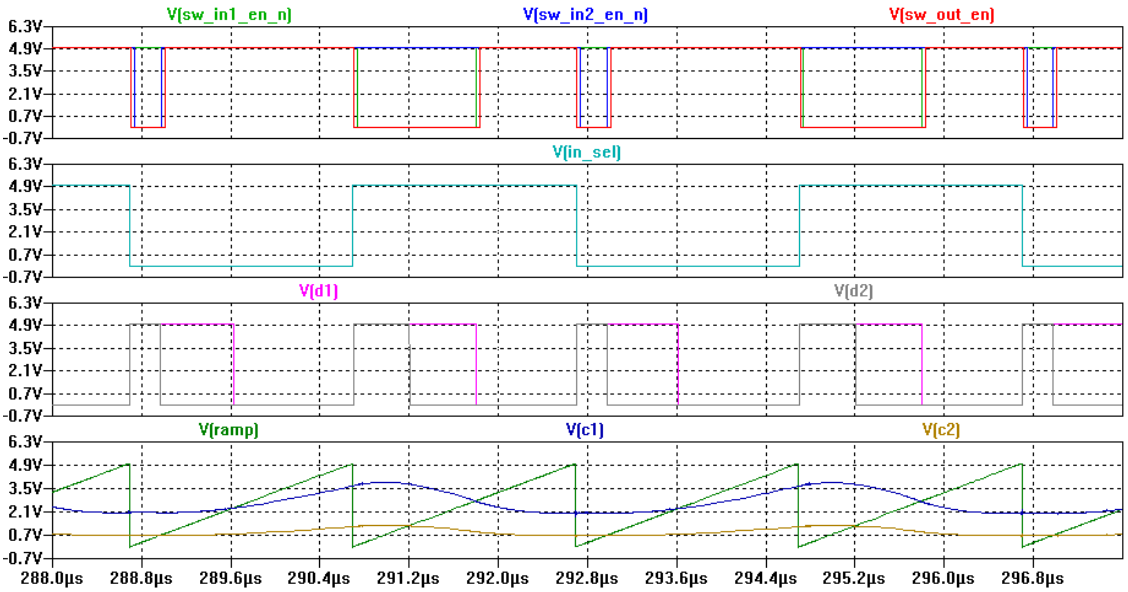

Figure 95. Dual-Input Converter Example Logic Block Simulation Waveforms

Analog Control

An error amplifier shown in Figure 96 is used to compare the output voltage of the converter with a reference voltage which is modeled as an ideal voltage source. In a real design this would be either a piece of silicon IP or a dedicated reference IC. The voltage-controlled current source G1 represents an OTA which is the error amplifier for this design. The capacitive load on its output forms an integrator providing the system with a very high overall gain at low frequencies. The output of the error amplifier is buffered before being divided down into two separate ratios. This is done to prevent the resistor dividers from interfering with the output impedance seen by the error amplifier.

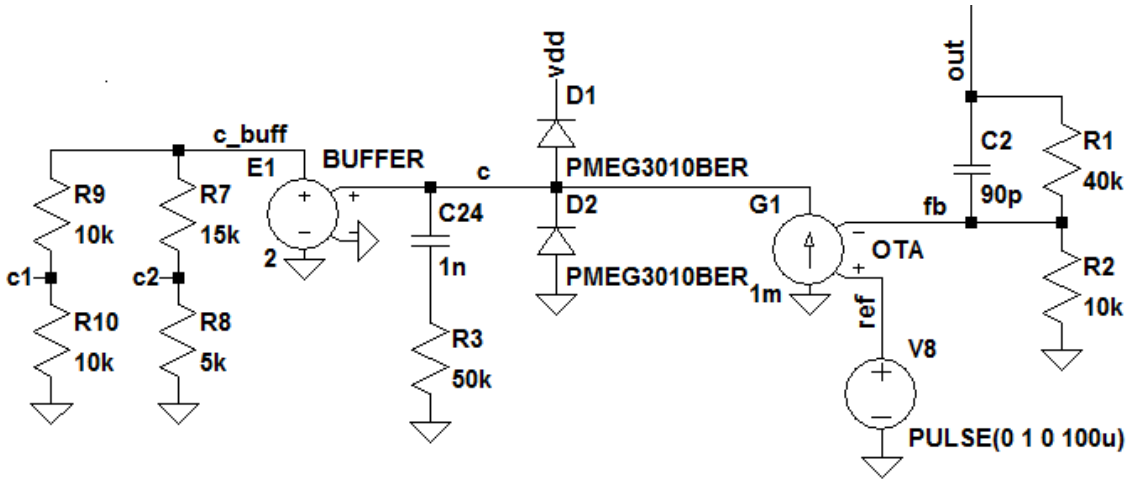

Figure 96. Dual-Input Converter Example Analog Control Schematic

The two divider ratios formed by divider R9 and R10 and divider R7 and R8 create a constant ratio of the control voltages C1 and C2. The ratio of the control voltages being fixed and allowing them to move together is important to the operation of the converter, as this ratio sets the input current ratio between the two input power sources, moving them up and down together allows the duty cycle to be adjusted for different output load cases and when compensating for load transients. Diodes D1 and D2 were used to bound the output of the OTA for simulation purposes only.

Compensation for the feedback loop of the converter is provided by C24, R3, and C2. This compensation scheme includes both the output compensation for the OTA and a feedforward capacitor across the resistor divider at the input of the OTA. Figure 97 shows simulation results for a transient load step at the output of the converter from 0A to 5A and back to 0A. Figure 98 shows simulation results of the waveforms for the analog control section during steady state operation at 5A. The example design is compensated to be stable with a fast transient response while allowing for some oscillation due to a low frequency pole introduced by the DC blocking capacitor interacting with the inductors in the power path.

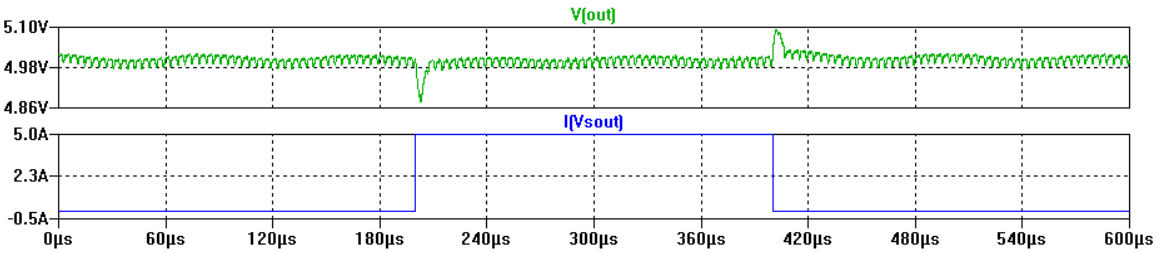

Figure 97. Dual-Input Converter Example Transient Response

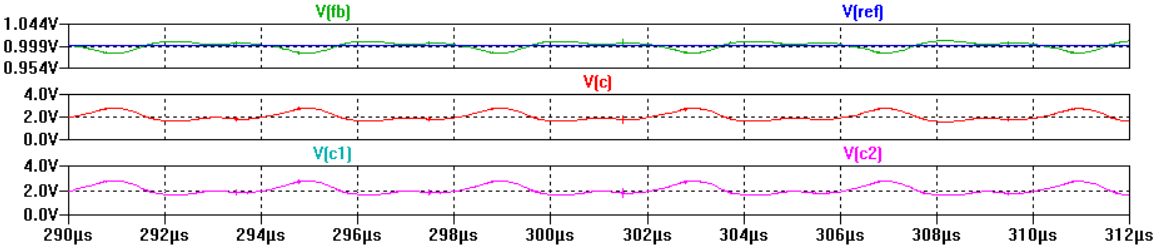

Figure 98. Dual-Input Converter Example Analog Control Waveforms

Characterization Results

An experiment to characterize the efficiency, static noise, and input current ratio is shown first. The load current is swept from 0A to 5A in 1A steps for five different input current ratio settings. The outputs of this characterization are the converters overall efficiency, the static output noise of the converter, the actual ratio of the input currents, and the average output voltage. The input current ratios tested are 90/10, 75/25, 50/50, 25/75, and 10/90 where the format is input 1 / input 2.

Figure 99 shows the percentage of the total input current being drawn from input 1 and Figure 100 shows that same information for input 2. In both figures the legend shows the ratios in the format of input 1 / input 2. The graphs show that compared to the set point there is a bias towards input 1 which is at a higher voltage compared to input 2. For any given set point the actual ratio of input currents seems to be biased towards drawing more current from input 1. This is likely due to a combination parasitic losses and inaccuracies introduced by the inserted dead time. Additionally there is a tendency for the actual input current sharing ratio to move closer to 50/50 under light loads.

In the 10/90 case where ideally only 10% of the current is being drawn from the 12V input source there is an issue in the design which causes the power to be drawn primarily from the 5V input. This is because the steep and narrow pulses from 0V to 12V on the switch nodes cause issues with the power path. A solution to this problem would be a more complex on-time and dead time management scheme. As a result of this issue the results for the 10/90 case do not line up with the results for the other cases.

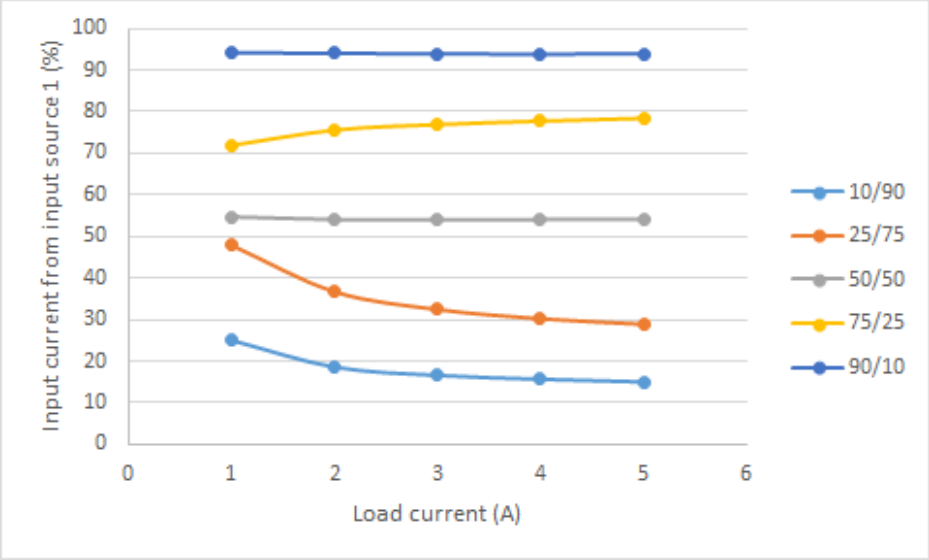

Figure 99. Percentage of Input Current Drawn from Input 1

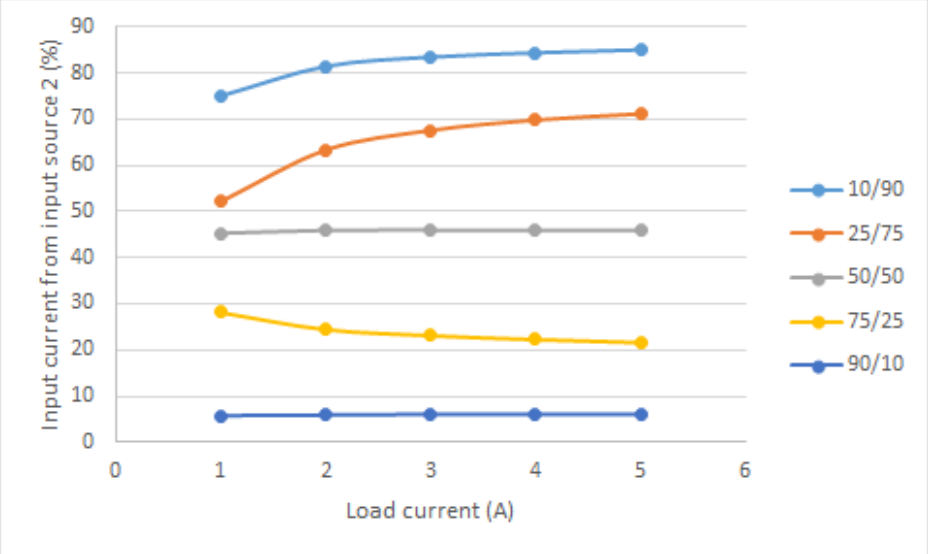

Figure 100. Percentage of Input Current Drawn from Input 2

Figure 101 shows the efficiency of the converter for each case. For all cases except 10/90 a typical distribution is seen with a peak efficiency around one to two thirds of the range of load currents. Under maximum load the higher efficiencies are seen when input 1 is favored. Under light loads a clear pattern is not present. The overall efficiency of the converter is above 80% for most cases which is typical for PCB level converters in this power range.

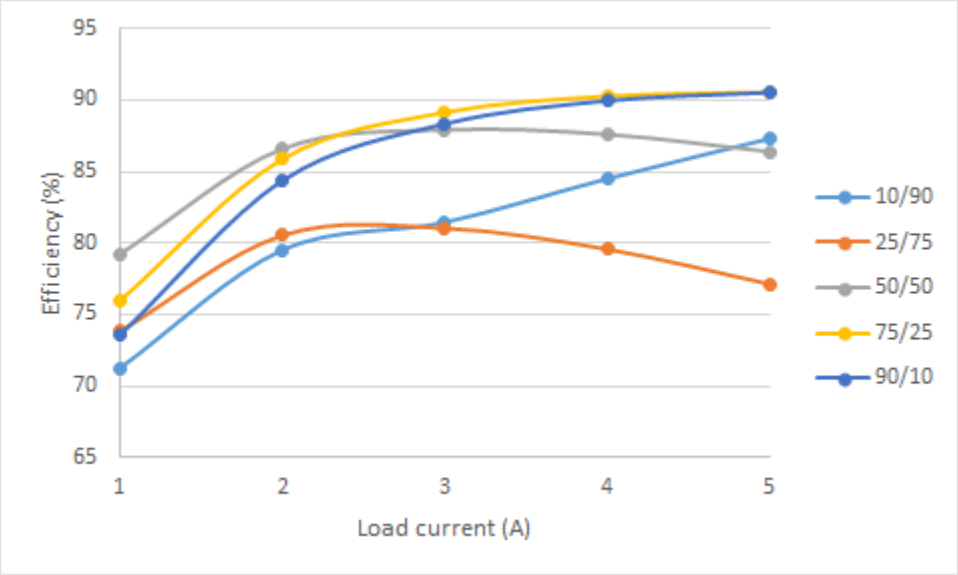

Figure 101. Example Converter Efficiency

In Figures 102 and 103 the DC output voltage and output voltage ripple are shown. Ripple voltage is measured as the peak-to-peak output voltage noise of the converter when operated in steady state with a static load. This data is also summarized in Tables 24 and 25. In all cases the average output voltage is within 20mV of the intended output voltage of 5V which represents a maximum set point error of 0.4%. The output voltage ripple increased with the load current for all cases which is consistent with what is generally understood about DC-to-DC converters. The maximum output voltage ripple, also known as output ripple, is approximately 180mV or 3.6%.

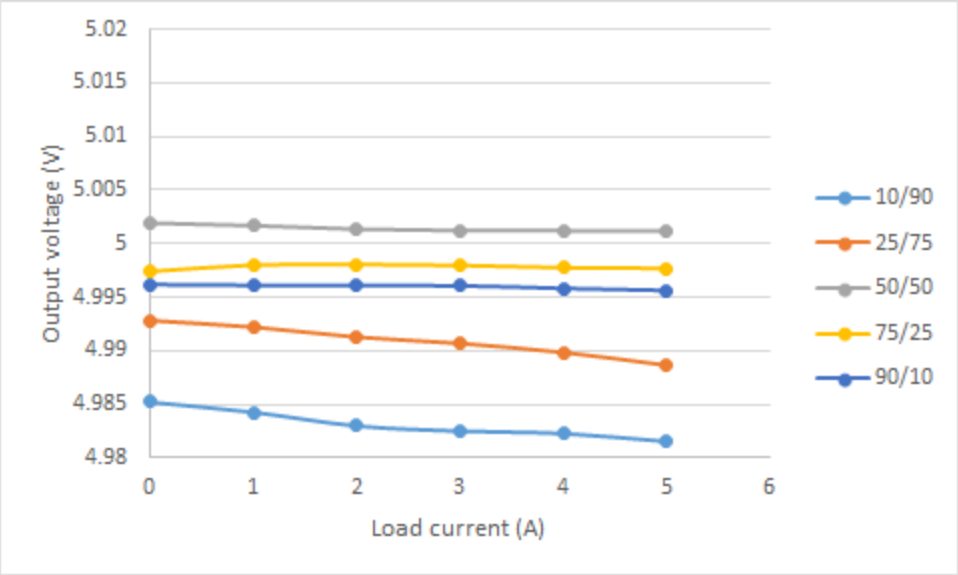

Figure 102. Example Converter DC Output Voltage

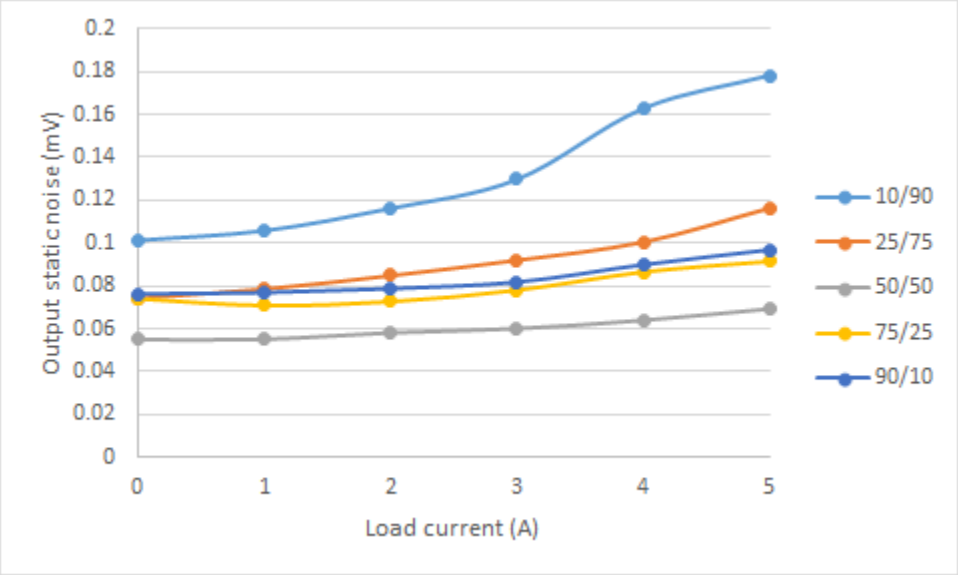

Figure 103. Example Converter Output Voltage Ripple

Table 24. Example Converter DC Output Voltage Results

Load (A)	10/90 (V)	25/75 (V)	50/50 (V)	75/25 (V)	90/10 (V)
0	4.985	4.993	5.002	4.997	4.996
1	4.984	4.992	5.002	4.998	4.996
2	4.983	4.991	5.001	4.998	4.996
3	4.982	4.991	5.001	4.998	4.996
4	4.982	4.990	5.001	4.998	4.996
5	4.982	4.989	5.001	4.998	4.996

Table 25. Example Converter Output Voltage Ripple Results

Load (A)	10/90 (mV)	25/75 (mV)	50/50 (mV)	75/25 (mV)	90/10 (mV)
0	101	74	55	74	76
1	106	79	55	71	77
2	116	85	58	73	79
3	130	92	60	78	82
4	163	100	64	87	90
5	178	116	69	92	97

A second characterization experiment is intended to capture the full dynamic noise and transient behavior of the design under the same conditions as the previous experiments. Each test case is given 400µs to stabilize, then run for 400µs with a load that switches from 0A to 5A and back with a 50µs period and a 50% duty cycle. Figure 104 shows the simulation results from a test run on the 50/50 case. Table 26 shows the results for total noise across all 5 cases. The total output voltage noise is less than 8% for all cases. The total output noise includes both the ripple voltage and the transient response.

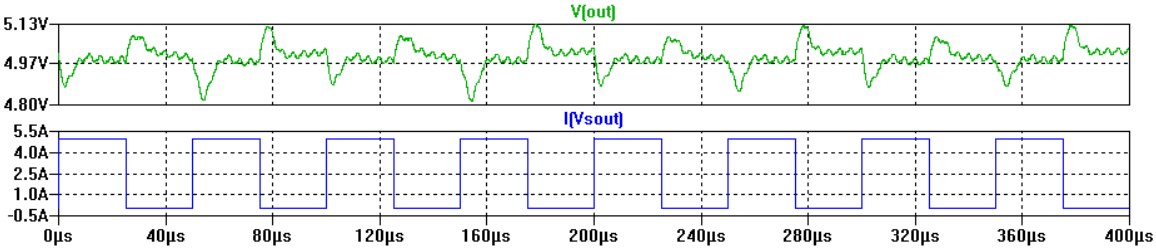

Figure 104. Example Converter Output Voltage Total Noise

Table 26. Example Converter Total Output Voltage Noise Results

Case	Noise (mV)
10/90	397
25/75	311
50/50	209
75/25	315
90/10	370

CHAPTER SIX: CONCLUSION

Dual-input DC-to-DC converters allow power to be drawn from multiple input sources and delivered to a single load. The applications for dual-input DC-to-DC converters include PC systems, mobile systems, energy harvesting applications, and systems with redundant power sources. The primary advantages of using a single power path for a dual-input DC-to-DC converter is smaller size and cost and reduced complexity. An opportunity for future research exists in examining the cost versus size versus efficiency tradeoffs in more detail based on modern semiconductor technology.

Of the four single power-path DC-to-DC converters analyzed in this thesis, the most advantageous is the dual-input zeta having a higher overall efficiency than the other single power path approaches and in some cases higher than the dual power path options as well. The dual-input zeta also has the lowest overall component count. One particular challenge with the zeta and SEPIC topologies in general which may sway designers towards the four-FET topologies is that the switch nodes in the zeta and SEPIC power paths can swing to negative voltages with respect to ground. This voltage swing complicates the design of power MOSFET drivers for those topologies. One solution to this problem is to use P-channel power MOSFETs for the high side switches, the cost of this being slightly higher losses as N-channel power MOSFETs tend to have lower losses.

All three of the common control methods were shown to be effective in regulating the output voltage of the single power-path dual-input DC-to-DC converters. As the topologies covered in this writing are buck-boost type converters, the advantages of

current mode and constant on-time control make those more attractive options than voltage mode control.

The overall power path of the example converter functions well in simulation. The main difference between this design example and the proofs of concept used in previous chapters is the need for dead time to be inserted to account for the turn-on and turn-off time of the MOSFETs. Having an efficiency that is generally above 80% is satisfactory for a small and relatively low-power voltage regulator. Some optimizations could be made to improve the efficiency including removing one of the series input MOSFETs from the higher voltage input, minimizing the dead time for each state transition, and selecting lower loss components.

The control block used in this design is similar to the control block used in the proof of concept simulations. Having realistic logic gate models serves to add realism to the simulation, however, it does not substantially impact the results. For more complex control schemes a CPLD or even a microcontroller could be used.

Design of a real control loop is a substantial undertaking, and if this were a design to be implemented, then a more complex control method such as current mode or constant on-time would likely be used. It is very common for compensation of these control loops to be done in the lab on hardware rather than in simulation.

One area that could be greatly improved upon is the current sharing accuracy. In this design the current sharing ratio is not controlled in a closed-loop fashion and therefore changes with load current in addition to having an offset. Adding a current sense and control loop to correct for this would greatly improve the accuracy if such improvement are needed.

Some additional opportunities for future research include looking at how these converters could be implemented on silicon as monolithic DC-to-DC converters where the power MOSFETs are integrated onto the same silicon as the logic and control circuits. Another opportunity for future research would be the development of hardware prototypes of these converters for additional proof of concept.

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