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Richard G. Southwick III
Boise State University

Justin Reed
Boise State University

Christopher Buu
Boise State University

Hieu Bui
Boise State University

Ross Butler
Boise State University

See next page for additional authors

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Temperature (5.6-300K) Dependence Comparison of Carrier Transport Mechanisms in HfO_2/SiO_2 and SiO_2 MOS Gate Stacks

Richard G. Southwick III[1], J. Reed[1], C. Buu[1], H. Bui[1], R. Butler[1], G. Bersuker[3], and W.B. Knowlton[1,2]

[1]Dept. of Electrical and Computer Engineering,
[2]Dept. of Materials Science and Engineering; Boise State University; 1910 University Dr.; Boise, ID 83725 USA
208-426-5705; fax: 208-426-2470; e-mail: bknowlton@boisestate.edu
[3]SEMATECH; Austin, TX 78741 USA

ABSTRACT

Temperature dependent measurements have been used to examine transport mechanisms and energy band structure in MOS devices. In this study, a comparison between high-*k* HfO_2 dielectrics and conventional SiO_2 dielectrics is made to investigate dielectric specific thermally activated mechanisms. Temperature dependent measurements on large area n/pMOSFETs composed of SiO_2 and HfO_2/SiO_2 gate dielectrics were performed from 5.6K to 300K. A large increase in the gate leakage current is observed at the formation of the minority carrier channel. The data indicate that gate leakage current prior to the formation of the minority channel is carrier rate limited while gate leakage current is tunneling rate limited above the threshold voltage. Gate leakage current measurements show two distinct Arrhenius transport regimes for both SiO_2 and HfO_2 gate dielectrics. The Arrhenius behavior of the gate leakage current is characterized by a strong temperature dependent regime and a weak temperature dependent regime. The activation energy of the strong temperature regime is found to vary with the applied gate voltage. Frenkel-Poole or other electric field models are able to explain the gate voltage dependence of the gate leakage current for the low-temperature/voltage regime investigated. The data suggest that the variation of the activation energy for the Arrhenius behavior is weakly electric-field driven and strongly voltage, or Fermi energy level, driven. The weak electric field and strong voltage dependence of the thermal characteristics of the gate leakage current may point to trap densities within the HfO_2 that vary in energy (hence applied voltage) as responsible for the observed activation energies. Trap assisted tunneling (or hopping) could be implicated as the transport mechanism.

INTRODUCTION

Understanding carrier transport is critical to development of reliability models of metal oxide semiconductor field effect transistors (MOSFETs). Identifying carrier transport (e.g., Fowler-Nordheim, Frenkel-Poole, etc.) provides reliability models with a physical basis to enhance the understanding of device limitations and potential solutions. A detailed knowledge of carrier transport can give insight to defects that are present in the oxide (a defect mediated transport), in which energy is deposited and transport of transient charges give rise to threshold instabilities. Temperature dependent measurements of the gate leakage current have been used extensively to understand carrier transport through many different gate dielectrics such as silicon nitride [1, 2], titanium oxide [3], aluminum oxide [4], europium oxide [5], zirconium oxide [6], and others. With the emergence of hafnium oxide (HfO_2) as the next gate dielectric to replace silicon dioxide (SiO_2), it is not unexpected that temperature dependent measurements have been made to assess its electrical properties [7-11].

Temperature dependent measurements on HfO_2 have reported Frenkel-Poole conduction with various trap depths between 0.35eV and 1.5eV below the conduction band [7, 8, 11]. Temperature dependent charge trapping experiments have been performed and indicate a large presence of charge traps around 0.35eV which contribute to threshold instabilities [12]. Band offsets have been measured using Schottky emission [11] and transient and steady state currents have been measured and modeled [9, 10], demonstrating the advantage of temperature dependent measurements.

Despite the large amount of temperature dependent work for understanding carrier transport in HfO_2, the majority of the work has focused on above room temperature measurements with few studies analyzing transport below room temperature and even fewer at cryogenic temperatures below 77K.

Although 77K reduces thermal smearing of the Fermi energy level (E_f) relative to room temperature, it is clear that temperatures much closer to 0K provide an appreciably sharper energy probe (Fig. 1). This work attempts to provide a clearer understanding of the trends observed in carrier transport of HfO_2 by investigating gate leakage currents in the low temperature regime ranging from 5.6K to 300K. Two different gate stacks of $TiN/HfO_2/SiO_2/Si$ and a $TiN/SiO_2/Si$ are measured and both nMOSFETs and pMOSFETs are used. A comparison between the HfO_2/SiO_2 and SiO_2 gate stack allows temperature specific trends of the HfO_2 to be identified. Low temperatures and finer temperature increments minimize thermal smearing and can reveal convoluted or competing mechanisms providing further insight to carrier transport in HfO_2/SiO_2 gate stacks.

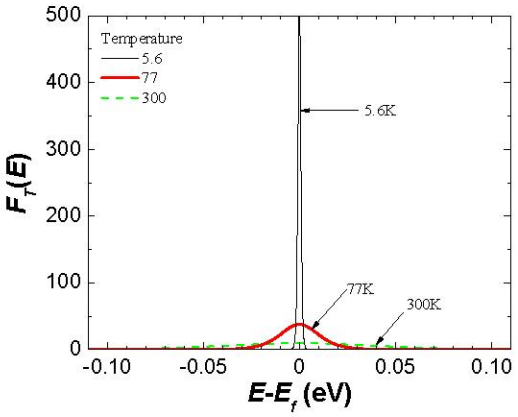

Fig. 1: Thermal broadening function, $F_T(E) = \partial_E f(E)$, as a function of E-E_f at 5.6K, 77K and 300K. The energy distribution at 5.6K is significantly narrower allowing the E_f position to be known much more accurately.

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This paper is presented as follows. First, the test devices and experimental procedure are presented. Next, general observations in the behavior of the gate leakage current, over a broad temperature range, are illustrated. The Arrhenius behavior of the gate leakage current is then described followed by an analysis of the activation energies and approaches used to correct for electric field dependence.

TEST DEVICES AND EXPERIMENTAL PROCEDURE

Devices used in this study are MOSFETs fabricated using a standard CMOS process flow including 1000°C/10s dopant activation and 480°C forming gas anneals. The gate stack of each MOSFET consists of a titanium nitride (TiN) metal gate and a dielectric bi-layer of 3nm of ALD HfO_2 on a 1.1nm chemically grown SiO_2 IL. A more detailed fabrication description is presented in [13]. A control wafer composed of 2nm SiO_2 is used as a base to compare the HfO_2 samples. Test devices are large 30µm/30µm (width/length) and 50µm/50µm MOSFETs to increase the signal to noise ratio of the gate leakage current. A Janis custom built variable range probe station (5.6-450K) with actively cooled Kelvin probes combined with a Keithley 4200SCS with remote pre-amps was used in the measurements.

RESULTS AND DISCUSSION

Gate leakage currents for nMOSFETs and pMOSFETs composed of HfO_2/SiO_2 and SiO_2 are shown in Figs. 2 and 3, respectively. For both n- and pMOSFETs, the HfO_2/SiO_2 gate stack shows a larger increase in gate leakage current with temperature than the SiO_2 gate stacks. For positive gate biases of 1V, the high-*k* gate nMOSFET shows over an order of magnitude increase in gate leakage current with the pMOSFET showing over three orders of magnitude increase. While the increase in gate leakage current for -1V gate biases is lower than 1V gate biases, it is still higher than SiO_2. Since equivalent oxide thicknesses, EOTs, are relatively similar ($EOT_{high\text{-}k}$ = 1.3nm and EOT_{SiO2} = 2nm), the HfO_2/SiO_2 gate leakage current data differ from the SiO_2 data most likely because of the HfO_2 defects, phonon modes, and perhaps carrier transport modes.

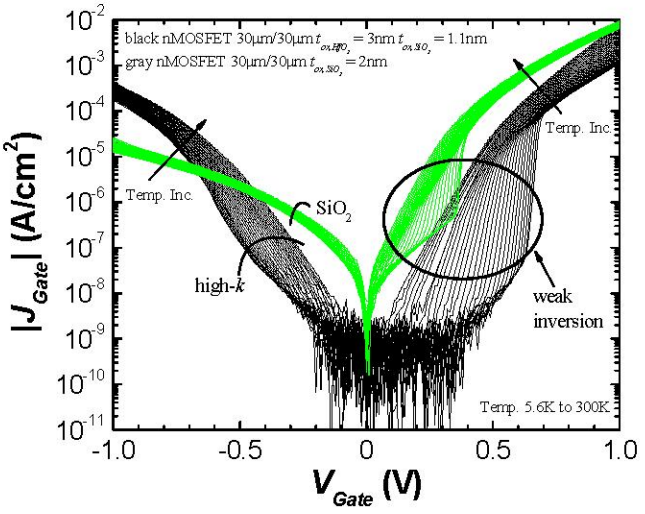

Fig. 2: Gate leakage current for nMOSFETs composed of a HfO_2/SiO_2 gate dielectric and a SiO_2 gate dielectric for temperatures ranging from 5.6K to 300K. The encircled region marks the weak inversion regime of MOS operation and shows a large increase gate leakage current.

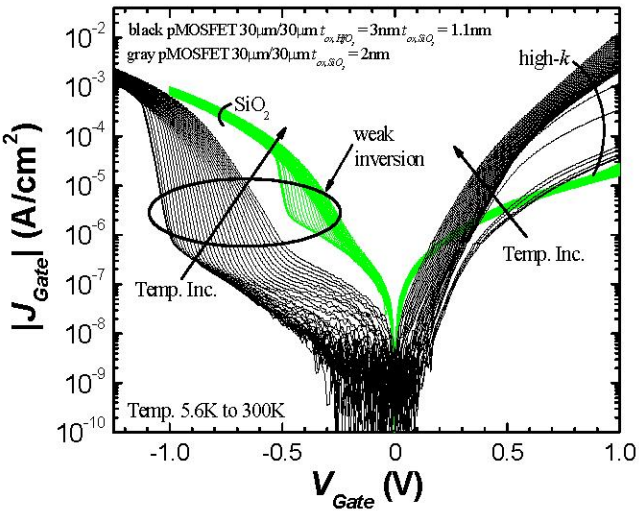

Fig. 3: Gate leakage current for pMOSFETs composed of a HfO_2/SiO_2 gate dielectric and a SiO_2 gate dielectric for temperatures ranging from 5.6K to 300K. The encircled region marks the weak inversion regime. For accumulation (positive voltages), the gate leakage current decreases dramatically at very low temperatures ~25K.

General Temperature Observations

The gate current versus gate voltage (I_G-V_G) temperature dependent curves for both n- and pMOSFETs show similar trends in three different regimes. These regimes are: 1) weak inversion – see encircled region in Figs. 2 and 3; 2) relatively large positive gate biases (0.7V to 1V); and 3) relatively large negative biases (~-1V). The following subsections propose qualitative explanations for the temperature increases for the three regimes.

Weak Inversion – For both n- and pMOSFETs composed of HfO_2/SiO_2 and SiO_2 gate dielectrics, a large increase in the gate leakage current, $J_{gate\text{-}leak}$, is observed during weak inversion, the encircled region in Figs. 2 and 3. As the temperature increases, the slope of the sudden increase in the $J_{gate\text{-}leak}$ decreases following temperature dependent trends in sub-threshold slope [14]. Applying a $3k_BT$ bias between the source and drain [14] to measure the presence of inversion charge reveals the sudden increase in $J_{gate\text{-}leak}$ corresponds to the sudden increases of minority carriers in the channel (Fig. 4).

The data of Figs. 4 and 5 suggest *carrier-limited* and *tunneling-limited* regimes. Consider Fig 5, the data indicate the first carriers that enter the channel from the source and drain do not flow from the source to the drain (i.e., source and drain current are asymmetric across the voltage axis), but from the source and drain through the gate thereby increasing the $J_{gate\text{-}leak}$. Prior to the threshold voltage, depletion/weak inversion, the gate leakage current is *carrier-limited*, due to the absence of minority carriers, labeled in Fig. 4. It appears that the $J_{gate\text{-}leak}$ then saturates even as the inversion charge continues to increase exponentially before losing its exponential dependence with the gate bias. Since carrier concentration is increasing but carrier transport (i.e., tunneling) is saturating, tunneling is self-limiting indicating a *tunneling-limited* mechanism, labeled in Fig. 4. As temperatures increase, the transition between *tunneling-limited* and *carrier-limited* tunneling occurs at lower voltages due to the increased number of minority carriers as temperatures increase. Above the threshold voltage however, enough minority carriers are

present so that the tunneling current is *tunneling-limited* over the temperature range investigated.

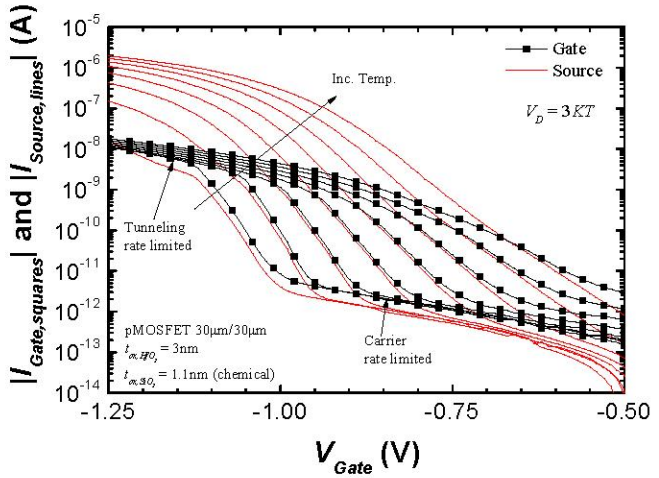

Fig. 4: A comparison of source current, a measure of the inversion charge, to the gate leakage current. The slope in the increase of the gate leakage current matches the sub-threshold slope in the source current. Current is tunneling rate limited above the threshold voltage (V_{TH}) and carrier rate limited below ~V_{TH} at low temperatures.

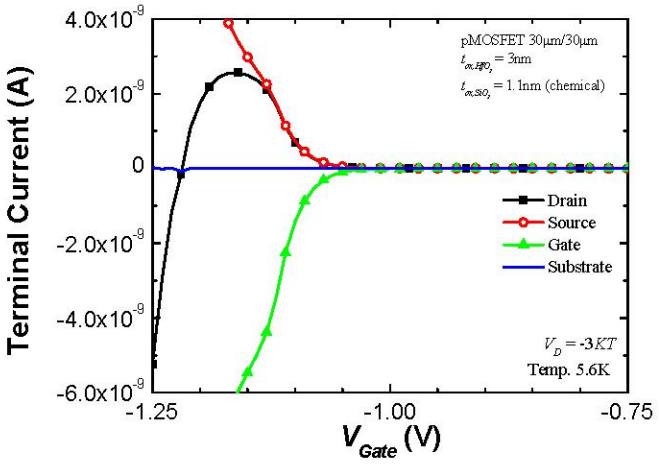

Fig. 5: A plot of all four terminal currents in a HfO_2/SiO_2 pMOSFET. Tunneling current (i.e., gate current) is carrier starved as observed by the increase in the gate leakage current corresponding to the presence of minority carriers flowing from the source and drain to the gate.

Relatively Large Positive Gate Biases: V_{Gate} 0.7V to 1V – As the gate bias increases, the Fermi energy level in the silicon moves closer to the conduction band of the HfO_2, Fig. 6a. Nevertheless, at low temperatures (i.e., minimal thermal broadening – Fig. 1) and low voltages, the Fermi level is not close enough to access defect states near the HfO_2 conduction band. As the temperature increases, the thermal energy distribution broadens (Fig. 1) allowing electrons to occupy higher energy levels in the silicon that have a greater probability to coincide with defect levels in the HfO_2, Fig. 6a. The combined qualitative result is the temperature dependence of the gate leakage current increases as the gate voltage increases.

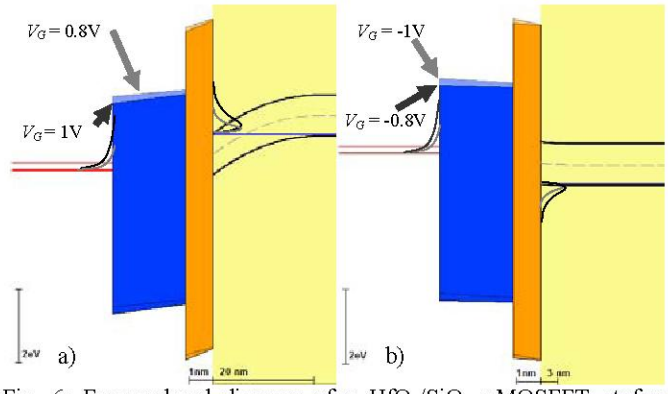

Fig. 6: Energy band diagram of a HfO_2/SiO_2 nMOSFET at four different gate biases, a) 0.8V and 1V and in b) -0.8V and 1V. As indicated in a), the HfO_2 conduction band becomes closer to the silicon Fermi energy with increasing positive gate bias. Conduction electrons in the silicon are moved even closer in energy to the HfO_2 conduction band with temperature for positive gate bias, part a). In b) as the voltage becomes more negative, the silicon Fermi energy level is further away from defects near the HfO_2 conduction band. Created using [15].

Examining the relative increase in $J_{gate\text{-}leak}$, ($\Delta J_{gate}/J_{5.6K,gate}$), in Fig. 7., it is observed that as the gate voltage increases so does the relative $J_{gate\text{-}leak}$. The relative $J_{gate\text{-}leak}$ increase at 300K for a gate bias of 1V is 6 fold. This increase in gate leakage current is much higher than the theoretical increase based on the work of Ling-Feng Mao which shows only a 0.2 fold increase at a gate bias of 1V [10]. In Mao's work, changes in tunneling currents due to changes in effective mass are calculated for various temperatures. When applied to this work, a large gate leakage current composed of defect mediated leakage current may explain the higher relative gate leakage current increase in Fig. 7. The relative increase in $J_{gate\text{-}leak}$ for the SiO_2 samples is not as large as the high-k samples but is also higher than what is predicted in [10]. It is important to note that the work done by Mao was for HfSiO not HfO_2 which also may account for some differences.

Relatively Large Negative gate Biases: V_{Gate} ~ -1V – For high-*k* samples, when the gate bias increases in the negative voltage direction, the Fermi energy level in the silicon moves further away from defects near the HfO_2 conduction band, Fig. 6b. This results in the temperature dependence of the relative gate leakage current decreasing as the voltage decreases. This is observed in Figs. 2 and 3 near V_{Gate} = -1V; as the gate voltage decreases the spread of the gate leakage current decreases. The relative gate leakage current for the negative bias regime (not shown) shows the opposite trend for positive gate biases, Fig. 7. Comparing to the theoretical work by Mao, the relative gate leakage current should not decrease with increasing voltage. This may further point to defect mediated tunneling as the primary component for the temperature dependence of the gate leakage current. As the gate voltage is decreased for negative voltages, fewer defects are being accessed which contribute less to the temperature dependence. As was seen in the positive bias regime, the negative bias regime also shows a significantly smaller temperature dependent increase for SiO_2 compared to HfO_2. Thus, increases in the direct tunneling current due to thermal broadening of carriers (Fig. 1) in the TiN metal gate and silicon substrate are thought to have a smaller impact on the large increase in the temperature dependence of the HfO_2 gate leakage current.

As the gate voltage continues to increase in the negative direction beyond -1V, the Fermi energy level in the TiN metal gate becomes closer to the defects near the HfO_2 conduction band. It can be

expected then, in a gate leakage current dominated by defect mediated tunneling, that the relative increase in the gate leakage current should increase at these higher voltages. Figure 8. shows the gate leakage current for -1V and -2V. As indicated, the relative gate leakage current increases from 1.21 and -1V to 2.55 at -2V consistent with the proposed mechanism.

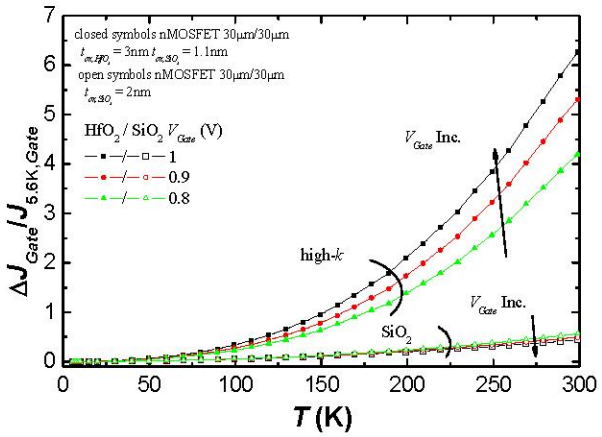

Fig. 7: Plot of the relative gate leakage current increase over the temperature range of 5.6K to 300K for gate voltages of 0.8, 0.9, and 1V. The relative increase in gate leakage current for HfO_2/SiO_2 gate dielectric is much higher than SiO_2 and the theoretical analysis done in [10]. Defect mediated tunneling in the HfO_2 devices may account for the difference.

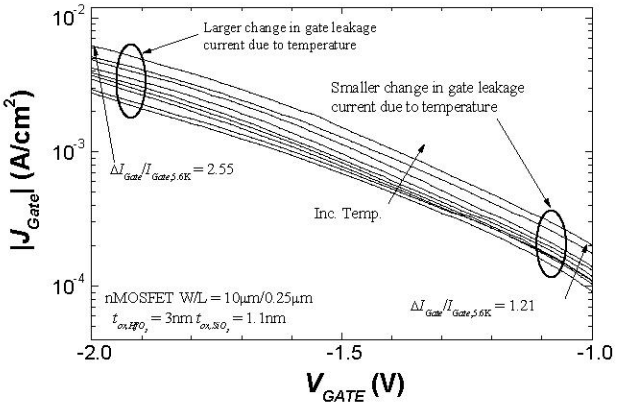

Fig. 8: Plot of the gate leakage current for voltages from -1V to -2V. As the temperature increases at these higher voltages, the change in J_{gate} increases indicating an increased temperature dependence. An increase in J_{gate} with temperature is consistent with electrons from the TiN metal gate accessing defect levels in near the HfO_2 conduction band.

Arrhenius Behavior

The Arrhenius behavior of the $J_{gate\text{-}leak}$ reveals two different transport regimes for both HfO_2/SiO_2 and SiO_2 MOSFETs (Fig. 9) with the exception of HfO_2 pMOSFETs in accumulation. The two different transport regimes can be characterized by a weak temperature sensitive regime (5.6K to 50K) with μeV activation energies and a strong temperature regime (~150K to at least 300K) with a very wide temperature transition regime. Two transport regimes were also observed by Compagnoni *et al.* [9]. They report activation energies ~87meV for temperatures higher than 165K and 5meV for the lower temperature regime in experiments performed to a minimum temperature of 77K. In this study, a lower activation energy of ~30μeV is found, indicating a very weak temperature dependence. The inset of Fig. 9 shows the data of this study in a temperature regime down to which Compagnoni *et al.* investigated (i.e., 77K). In this regime, an activation energy of 4.5meV is determined, which is consistent with the activation energy reported by Compagnoni *et al.* (Fig. 9 inset). The much larger activation energy of 4.5meV is explained by realizing that the range of temperature used down to 77K to calculate the activation energy is in a transition region which is not linear (Fig. 9).

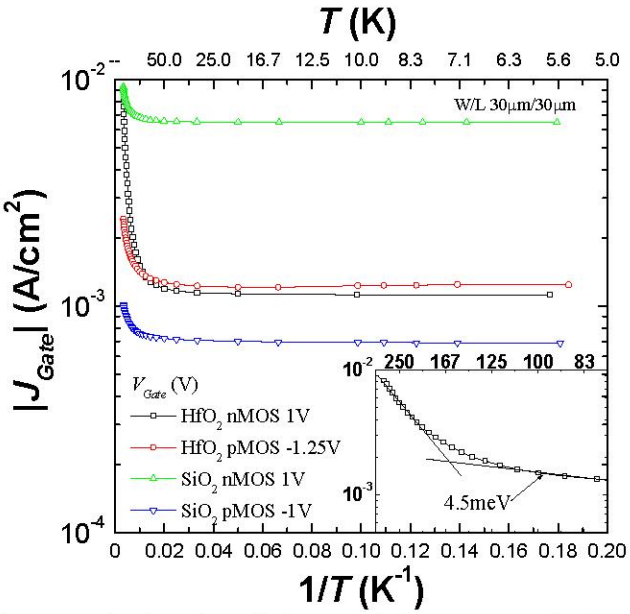

Fig. 9: Arrhenius plot of the gate leakage current density for HfO_2/SiO_2 and SiO_2 MOSFETs showing two different transport regimes, a weak temperature dependent ~30μeV regime and a highly temperature dependent regime. For gate leakage currents from ~125K to 77K which appears linear (inset), the weak temperature regime has and activation energy of 4.5meV. As the measurements continue to 5.6K, ~125K to 77K is in a transition region and not linear.

Four different transport regimes can be seen in HfO_2/SiO_2 pMOSFETs in accumulation (Fig. 10). Transport regimes labeled *1* and *2* in Fig. 10 are similar in activation energy and transition temperature as HfO_2/SiO_2 nMOSFETs. In addition, the pMOSFETs show transports regimes labeled *3* and *4*. The activation energy calculated for regime *3* is approximately ~4meV. A transition between *3* and *2* occurs at temperature of about 25K. Transport regime *4* exists below ~9K and is weakly temperature dependent. It is unclear at this point what might cause such a response. The Fermi energy level in the silicon for similar biases in HfO_2/SiO_2 nMOSFETs and pMOSFETs are aligned to relatively the same energy level in the HfO_2 so it is unlikely that a different energy range is accessed in the pMOSFET.

The slopes of the transport regimes (i.e., activation energy, E_A) change with gate voltage for both HfO_2/SiO_2 and SiO_2, Fig. 11. The SiO_2 range of activation energies are lower than the high-*k* range of E_As, and vary from 10meV to 40meV. The E_As for the high-*k* samples range from 20meV to 90meV depending on the gate bias. The high-*k* E_As are somewhat low as compared to [12]. This may be because the E_As have not been corrected for the electric field effect on the trap [12, 16] or that the E_A extracted from [12] was using threshold voltage shift data. Rough correction calculations using [16], show that the E_As would increase by ~200meV towards that of [12]. Both the HfO_2/SiO_2 and SiO_2 samples exhibit a transport regime that is

nearly independent of temperature in the low temperature range probably due to a low phonon density.

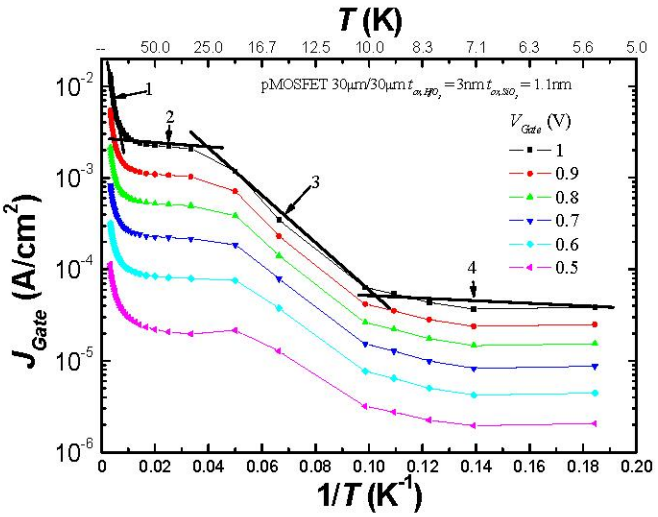

Fig. 10: Arrhenius plot of HfO_2/SiO_2 pMOSFET in accumulation ($+V_{Gate}$). Four different transport regimes are observed and indicated by arrows and numbers. The lines are only used to show trends for regions 1-4.

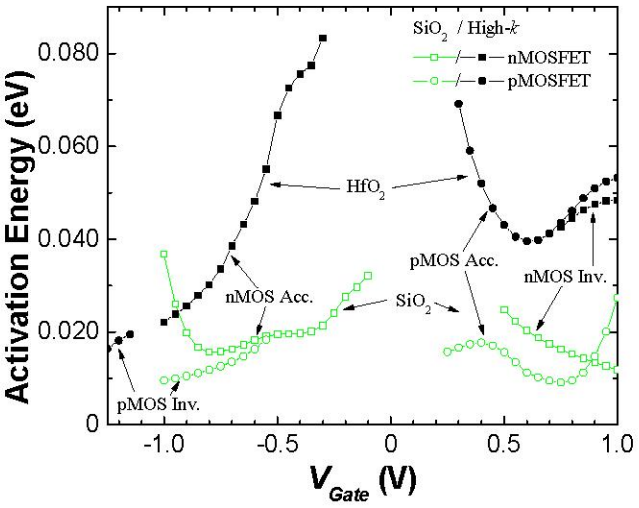

Fig. 11: Plot of the E_A for transport regime above 150K for both HfO_2/SiO_2 and SiO_2 dielectrics. The E_A for SiO_2 is lower than the HfO_2/SiO_2 dielectric. Both the SiO_2 and HfO_2/SiO_2 E_A's depend on the applied gate voltage.

Consider the range of temperatures in which a transition between carrier transport regimes occurs. Within a given transition range of temperatures, there exists a midpoint temperature which we shall define as the "center transition temperature". The center transition temperature for the transition regime between the highly dependent temperature regime (T > ~200K) and the weakly temperature dependent regime (T < ~50K) is plotted as a function of V_{gate} in Fig. 12. The HfO_2/SiO_2 MOSFETs on average show a lower center transition temperature than the SiO_2 MOSFETs. Although HfO_2 and SiO_2 both display two carrier transport regimes, the higher center transition temperature coupled with the lower activation energy in SiO_2, may explain the small gate leakage current temperature dependence observed in Figs. 2 and 3. The smaller E_A and higher center transition temperature in SiO_2 indicates a significant difference in the carrier transport in SiO_2 compared to HfO_2.

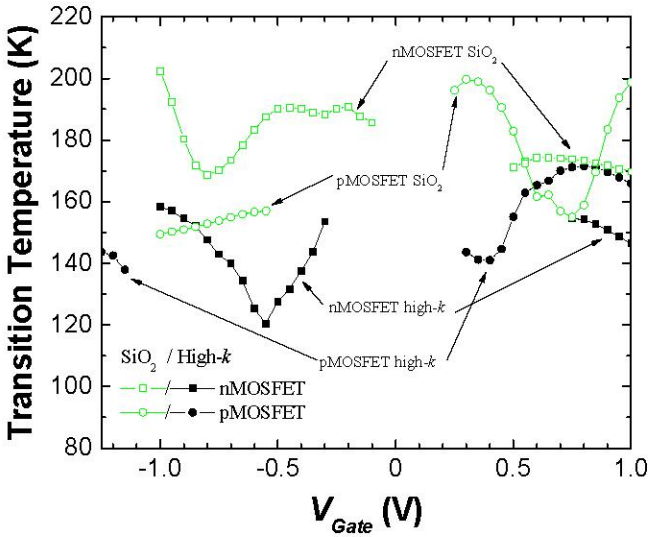

Fig. 12: Plot of the center transition temperature for HfO_2/SiO_2 and SiO_2 MOSFETs. SiO_2 MOSFETs have a higher transition temperature than HfO_2/SiO_2 MOSFETs. The transition temperature varies with gate voltage.

Electric Field Correction Factors

As was alluded to in the previous section, a common correction factor to E_As is the electric field. A typical electric field correction factor is Frenkel-Poole [17]. In Frenkel-Poole conduction, the amount of energy required for an electron to move from the localized trap to the conduction band is reduced in the presence of an electric field (E_{ox}) [18-20]. The higher the electric field, the less energy is needed for the electron to escape. This results in lower activation energies at higher electric fields. The equation describing Frenkel-Poole conduction (J_{FP}) is given as:

$$J_{FP} \approx E_{ox} e^{\frac{-\left(\phi_B - \beta_{FP} E_{ox}^{1/2}\right)}{k_B T}} \quad (1)$$

where $\beta_{FP} = \sqrt{q/4\pi\varepsilon_0 k}$,

k_B is Boltzmann's constant (eV/K), ϕ_B is the trap depth from the conduction band, q is the charge of an electron, ε_0 is the permittivity of free space, and k is the dielectric constant. From (1), the dependence on the electric field is seen in the pre-exponential and as a modifier to the numerator of the exponent, or the activation energy. It is therefore important to accurately extract the electric field. Below are several methods of calculating the electric field.

$$E_{ox} = \frac{V_{Gate} - V_{FB}}{t_{ox}} \quad (2)$$

$$E_{ox,HfO_2} = \frac{V_{Gate} - V_{FB}}{t_{ox,HfO_2}} \frac{C_{ox,SiO_2}}{C_{ox,HfO_2} + C_{ox,SiO_2}} \quad (3)$$

$$E_{ox,HfO_2} = \frac{V_{Gate} - V_{FB} - \phi_s(V_{Gate})}{t_{ox,HfO_2}} \frac{C_{ox,SiO_2}}{C_{ox,HfO_2} + C_{ox,SiO_2}} \quad (4)$$

where V_{FB} is the flat-band voltage, $C_{ox,SiO2}$ is the SiO_2 layer capacitance, $C_{ox,HfO2}$ is the HfO_2 layer capacitance, t_{ox} is the dielectric thickness, and ϕ_s is the surface potential in the silicon which is a function of gate voltage. In (2) the voltage across the oxide is approximated as the difference in the gate voltage and flat-band

voltage and is converted to an electric field through the dielectric thickness. For a two dielectric gate stack and assuming the traps are located in the HfO_2 dielectric, the voltage across the HfO_2 dielectric is modified by the capacitances of each dielectric layer as shown (3).

At low voltages, the surface potential in the silicon accounts for a large part of the total gate voltage drop and cannot be ignored. Accounting for the surface potential drop in the silicon, $\phi_s(V_{Gate})$, which reduces the voltage across the HfO_2 is done in (4). Using SILVACO, the electric field in the HfO_2 layer for various voltages was simulated for temperatures ranging from 10K to 300K. Results indicate that the electric field changes little with temperature and are closely approximated with [15] (Fig. 13). A plot of the four ways discussed to calculate the electric field is shown in Fig. 13. A significant difference in the manner the electric field through the HfO_2 is calculated is observed, particularly in inversion. Substantial error can occur when performing an electric field correction if an insufficient method is used to calculate the electric field through the HfO_2.

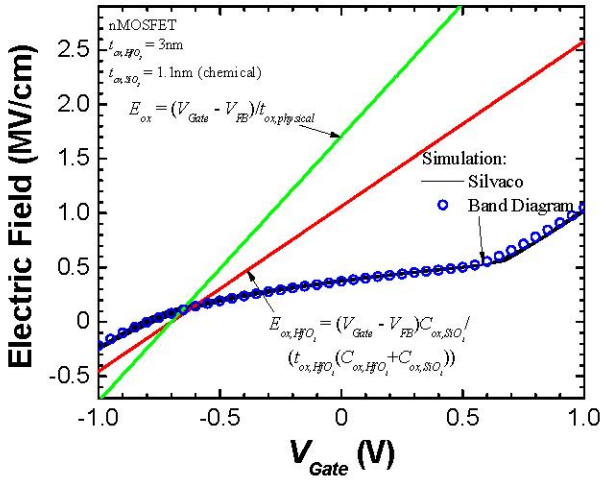

Fig. 13: Plot of the electric field calculated three different ways using equations (2) – (4). The extracted electric field at low voltages depends greatly on the chosen method. The electric field was calculated for temperatures ranging from 10K-300K using SILVACO and are observed to vary little. $E_{ox,HfO2}$ can be approximated to SILVACO using the band diagram program [15].

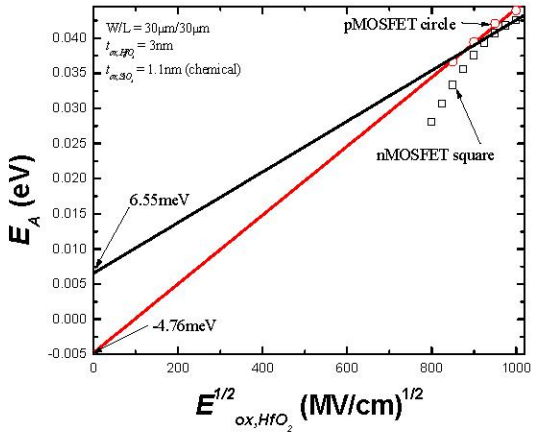

Fig. 14: Frenkel-Poole analysis of the gate leakage current in the high temperature transport regime (T < 150K). The activation energy increases as the electric field in the HfO_2 increases which is nonsensical.

Following Frenkel-Poole analysis and determining the activation energy of $J_{Gate}/E_{ox,HfO2}$, at different electric fields results in Fig. 14. Using a linear fit, the trap depth at flat-band is near 0eV and, depending on where the linear fit is taken, may be negative which doesn't make sense. Also observed in Fig. 14 is an increase in the activation energy as the electric field increases. The increase in E_A as $E_{ox,HfO2}$ increases does not follow Frenkel-Poole theory which states that E_A should decrease with electric field. Possible reasons for why Frenkel-Poole analysis fails here, but has been successful in explaining the temperature dependence in the work of many others, may be due to the low voltage and low temperature regime discussed here. That is, it is reasonable to expect that traps in the HfO_2 are more easily accessed at high voltages and temperatures. Frenkel-Poole transport has been shown in similar samples for higher gate voltages from 1 to 2V [21].

Examining E_A as a function of gate voltage, Fig. 11, the activation energy decreases *and* increases, as the gate voltage increases. A more plausible explanation to the varying E_As maybe due to the position of the Fermi energy level and different temperature dependent transport traps being accessed as the gate voltage changes. We suspect that as the Fermi energy level begins to coincide with a high density of defect states that the E_A should decrease. Conversely, the further in energy the Fermi energy level is from traps, the great E_A should be.

SUMMARY

Carrier transport mechanisms at low temperatures and low voltages are not well understood in HfO_2 gate dielectrics. By comparing the temperature dependence of the gate leakage current in HfO_2 to SiO_2, a better understanding of the transport mechanism specific to HfO_2 can be realized. Gate leakage current measurements on HfO_2/SiO_2 gate dielectrics and SiO_2 gate dielectrics were made for temperatures ranging from 5.6K to 300K. Results indicate a strong increase in the gate leakage current for both HfO_2/SiO_2 and SiO_2 dielectrics in the weak inversion regime which is attributed to the increase in minority carriers in the channel. HfO_2/SiO_2 dielectrics show a large temperature dependence compared to SiO_2. In HfO_2/SiO_2 for positive voltage ~1V, the temperature dependence increases with gate voltage, this is thought to occur due to increased interaction of electrons with defects near the HfO_2 conduction band. For HfO_2/SiO_2 operating near -1V, the temperature dependence decreases as the gate voltage becomes more negative, and is attributed to traps nears in HfO_2 the conduction band becoming inaccessible. Both HfO_2/SiO_2 and SiO_2 dielectrics show two transport regimes on an Arrhenius graph with pMOSFET HfO_2/SiO_2 dielectrics showing four in accumulation. The activation energy for the transport regime for T > ~150K varies with gate voltage and cannot be modeled with a Frenkel-Poole or electric field approach. Care must be taken when calculating the electric field at low gate voltages (e.g., close to use conditions) as band bending in the silicon consumes a significant portion of the applied gate voltage. Variations in the activation energy with respect to gate voltage indicate a weak electric field dependence and are probably more dependent on the Fermi energy level alignment with defects in the HfO_2.

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Questions and Answers

Q: Does your electric field equation include the effects of charge trapping?

A: No, the electric field equation assumes no charge trapping.

Q: Have you ever tried to solve for electric field using the continuity of conductance?

A: No, we have not. All of the electric field calculations used so far assume no current transport through the dielectrics.