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Jim Jozwiak
Boise State University

Richard G. Southwick III
Boise State University

Vaughn N. Johnson
Boise State University

William B. Knowlton
Boise State University

Amy J. Moll
Boise State University

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Integrating Through-Wafer Interconnects With Active Devices and Circuits

Jim Jozwiak, Richard G. Southwick, III, *Member, IEEE*, Vaughn N. Johnson, William B. Knowlton, *Member, IEEE*, and Amy J. Moll

***Abstract*—Through wafer interconnects (TWIs) enable vertical stacking of integrated circuit chips in a single package. A complete process to fabricate TWIs has been developed and demonstrated using blank test wafers. The next step in integrating this technology into 3-D microelectronic packaging is the demonstration of TWIs on wafers with preexisting microcircuitry. The circuitry must be electrically accessible from the backside of the wafer utilizing the TWIs; the electrical performance of the circuitry must be unchanged as a result of the TWI processing; and the processing must be as cost effective as possible. With these three goals in mind, several options for creating TWIs were considered. This paper explores the various processing options and describes in detail, the final process flow that was selected for testing, the accompanying masks that were designed, the actual processing of the wafers, and the electrical test results.**

***Index Terms*—Integrated circuit (IC) packaging, interconnects.**

I. Introduction

MOORES's law has driven the semiconductor industry for 40 years, with each generation of devices requiring new processes and new materials. Although the pace of introduction of new processes and new materials has continually accelerated, innovations, such as low-k dielectrics, are presenting processing challenges and have not been easily integrated [1]. Hence, other alternatives—such as advanced packaging—are being explored to continue the drive for increased functionality in less space [2].

Three-dimensional packaging using stacked chips for high density has received a considerable amount of attention over the last few years [3]. The evolution of semiconductor technology has reached a point where the package now plays an important role in the overall performance of the device. In MEMs devices, the package is often more than 75% of the cost and has a significant impact in the overall size. Off-chip interconnects are now becoming a limiting factor in the overall performance of an integrated circuit (IC).

Stacked chip packages have been integrated into commercial applications over the last five years in cell phones, PDAs, and laptops [4], [5]. In these high volume applications, wire-bonding is typically used for the off-chip connections. Other alternatives have been explored including stacked packages, folding packages, chips embedded in polymer, and metal traces on the side of the die [6]–[8]. In these technologies, multichip packages compete with the concept of a system on a chip. Separating system functions into more than one die allows each die to be fabricated utilizing the optimal processes for the given materials system and technology.

Through wafer interconnects (TWIs) have distinct advantages to other advanced 3-D packaging schemes [9]. Additional miniaturization, increased interconnection density, and higher performance are possible by stacking die with TWIs [10]. Power consumption can be reduced by shortening the overall wire lengths [11], while also providing thermal vias for heat removal. Key technologies for creating TWIs are the ability to create a via through the silicon wafer, dielectric isolation of the via metal from the substrate, and filling or coating the via with a conducting material [12].

Through wafer interconnects are of particular interest in microelectromechanical systems (MEMs) and sensor packaging [13]–[15]. TWIs address two challenges in MEMs packaging—cost and size. In a MEMS system, the package is often 75%–95% of the cost. The package size may also be significantly larger that the actual die. These issues have reduced the market for MEMS applications. TWIs have many potential advantages over wirebonding and other interconnect technologies for MEMs packaging [16], [17]. Use of TWIs with MEMS devices will provide device-scale packaging and compatibility with flip chip assembly. In one MEMS application, TWIs have been used in the development of a two dimensional cantilever array allowing for the electrical wiring and wire bonds to be on the backside of the wafer away from the sensors [13]. In millimeter-wave and radio-frequency (RF) applications, TWIs have been incorporated in order to improve the high-frequency operation of the radio-frequency integrated circuit (RFIC) [18], [19] and reduce extrinsic parasitics. TWIs can be used to replace bond wires that add parasitics to the RF devices and are incompatible with standard CMOS processing.

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J. Jozwiak was with the Selland College of Applied Technology, Boise State University, Boise, ID 83725 USA. He is now with Micron Technology, Boise, ID 83707 USA (e-mail: jjozwiak@micron.com).

R. G. Southwick, III is with the Electrical and Computer Engineering Department, Boise State University, Boise, ID 83725 USA (e-mail: rickisouthwickiii@boisestate.edu).

V. N. Johnson was with the Electrical and Computer Engineering Department, Boise State University, Boise, ID 83725 USA. He is now with Micron Technology, Boise, ID 83707 USA (e-mail: vnjohnson@micron.com).

W. B. Knowlton is with the Electrical and Computer Engineering Department and the Materials Science and Engineering Department, Boise State University, Boise, ID 83725 USA (e-mail: bknowlton@boisestate.edu).

A. J. Moll is with the Materials Science and Engineering Department, Boise State University, Boise, ID 83725 USA (e-mail: amoll@boisestate.edu).

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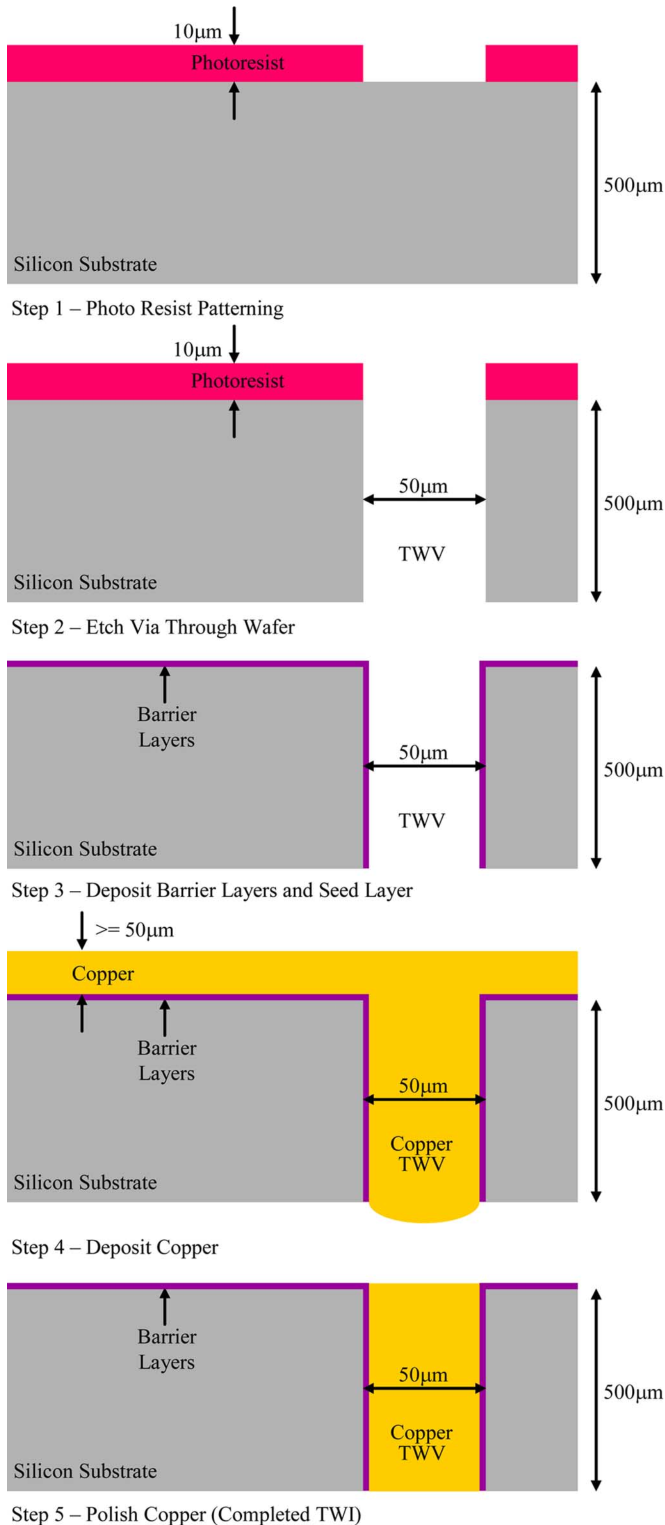

Fig. 1. TWI process on bare silicon wafers.

In order for TWIs to be incorporated into a 3-D package, the fabrication and processing must be compatible with active device wafers. The creation of a TWI cannot change the electrical behavior of the device or impact the reliability of the devices. In this study, the TWI process integration used to provide electrical contact to active devices from the device-side to the wafer backside is detailed. The effect of the TWI process on device performance and functionality is described.

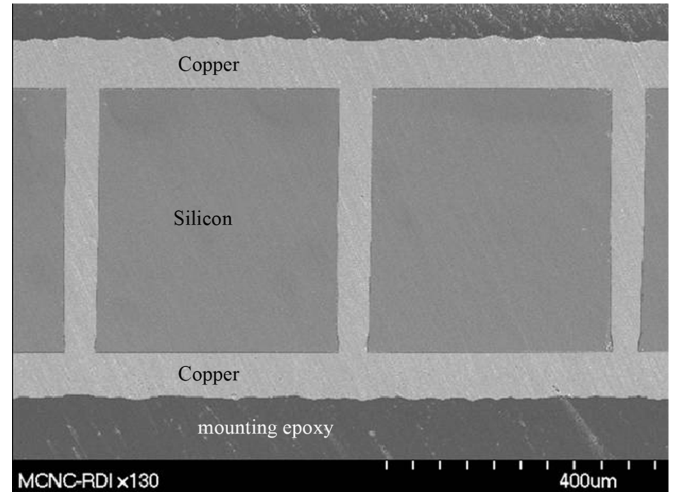

Fig. 2. Scanning electron micrograph of cross section of TWI in blank Si wafer before CMP to remove copper on top and bottom of wafer.

II. Fabrication Process Steps

Our initial work on the development of TWIs has focused on the optimization of the process using blank Si wafers. TWIs with a 10:1 aspect ratio have been demonstrated on 500-μm-thick wafers. The size of these TWIs are optimized for incorporation into existing bond pads in current circuit designs. One potential application is the stacking of existing memory chips without any need to change the design. Other groups are pursuing much smaller (e.g., less than 5-μm in diameter) TWIs as part of new IC designs and applications which incorporate 3-D packaging in the initial design [20]. Complete details of the processing steps for the fabrication of through wafer interconnects have been presented elsewhere [21]. Processing steps are summarized below and in Fig. 1 for 50-μm-diameter vias in 500-μm-thick wafers. A cross section of a completed TWI in a blank wafer is shown in Fig. 2.

Step 1—Photoresist Patterning: Very high-viscosity positive photoresist is spun onto the wafer to a thickness of at least 10 μm. The thick resist is required in order to provide sufficient protection for the etching of the vias. Exposure takes place through a dark-field mask with 50-μm-diameter holes where each TWI is to be located. Holes in the resist are developed using a TMAH-based developer solution.

Step 2—Etch Via Through Wafer: An inductively-coupled plasma etcher utilizing the Bosch process [22] is used to etch an anisotropic hole through the entire thickness of the silicon wafer. The Bosch process consists of a short etch step, utilizing SF_6, followed by a sidewall passivation step utilizing C_4F_8. This sequence is repeated between 500–600 times until the via extends through the entire wafer. Following the etch process, the photoresist is stripped.

Step 3—Deposit Barrier Layers and Seed Layer: An organic insulating film, parylene, is deposited using a thermal deposition process to a thickness of 1 μm. The second film is a thin (200 nm) layer of titanium nitride. The TiN prevents diffusion of the copper from the via into the silicon. The last film is seed layer of copper approximately 1 μm thick.

Step 4—Electroplate Copper: The vias are filled with electroplated copper. Copper also coats the both the front and the back of the wafer, with raised hillocks where the vias are located.

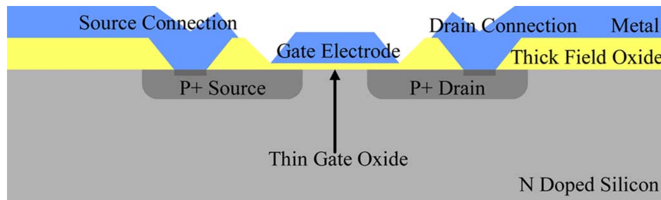

Fig. 3. Cross-sectional diagram of pMOS transistor.

Step 5—Polish Copper: The surface copper is removed using chemical mechanical planarization (CMP). A two-step process is used in order to remove the thick layer of copper and planarize the surface [23]. The TiN is also removed by CMP. The surface barrier layers are removed using wet chemistry, and the TWI's are completed.

TWIs with a 50 μm diameter have been demonstrated on a 500-μm-thick wafer. Electrical testing indicated the TWIs have an average resistance of 6 mΩ [24]. Electrical characteristics of the individual interconnects did not change following a reliability test for moisture sensitivity (24 h bake at 90 °C, 24 h bake at 125 °C, seven day soak: 85 °C/85% relative humidity, and 3 times through the 260 °C reflow cycle) and a thermal cycling test (1000 cycles of -65 °C for 15 min and 150 °C for 15 min, air to air) [24].

III. Integration of Through Wafer Interconnects With Active Circuitry

Integration with active devices and circuitry requires the TWI to be formed and electrically connected to the circuit. Optimization of the design would incorporate TWIs in a way that results in the highest density for the entire package. Design would be dependent on the specific application. For this study, an existing device was used with the TWI connection made to the existing bond pads. Bond pads are similar in dimension to the TWI and utilizing them for the connection allows the demonstration of TWIs on existing designs.

The test vehicle is a simple p type metal oxide semiconductor (pMOS) test chip, chosen for its large dimensions, robustness, and relative simplicity. Both the process and the circuit designs for the pMOS test chip were developed at the Rochester Institute of Technology Microelectronics Center, Rochester, NY [25]. The chip consists of several pMOS field effect transistors (pMOSFET) of varying dimensions of both width (W) and length (L). The SiO_2 gate oxide thickness is 70 nm. These transistors exist separately, or are configured into simple digital circuits such as inverters and flip flops. Other devices are also present, such as serpentine resistors and Kelvin structures. The entire process consists of only one doping operation, where p type regions are created in an n-type substrate, one metal layer and four patterning operations: diffusion, gate oxide, contact, and metal interconnect. A 1-μm layer of oxide passivation is added for device protection. The completed pMOSFET cross-sectional diagram is shown in Fig. 3.

Successful fabrication of TWIs must result without significant impact to the electrical performance of the previously existing devices or circuits. In this study, following the creation of the TWI devices were tested from the back side. In addition, electrical tests were conducted before and after BOSCH etch on a second set of wafers. The BOSCH etch process significantly deviates from typical processing and plasma processes have caused reliability issues. These results are summarized in a later section of this paper.

Three process sequences were considered for the integration of TWIs with the previously existing circuitry. These options are summarized as follows.

1) Approach the completed bond pad from beneath, performing all major TWI processing from the wafer backside ("Backside Process," Fig. 4).
2) Fabricate the TWIs from the wafer frontside prior to deposition and patterning of the bond pad (top) metal layer ("Insertion Process," Fig. 5).
3) Fabricate the TWIs from the wafer frontside following the deposition and patterning of the bond pad metal layer. Then build a metal "bridge" from the TWI to the bond pad ("Bridge Process," Fig. 6).

These processes are discussed relative to the simple pMOS wafers used in this study with some consideration of how the processes could be incorporated into the fabrication of more complex integrated circuit wafers.

A. Option #1—Backside Process

The fabrication of TWIs on a wafer exposes the existing circuitry to additional process steps. Relative to potential damage to the existing devices, two process steps are of primary concern: Bosch etch and Cu CMP. In order to minimize damage to the devices, backside-only processing was investigated. By performing the process steps on the wafer backside, the potential damage to the devices could be minimized. This methodology could also be very cost effective, because it only requires eight additional processing steps and one additional photomask. The proposed methodology is summarized in Fig. 4.

Several areas of concern arise in this processing scheme. When the via is etched what remains behind is a thin metal layer—the bond pad that is less than 1 μm thick, stretched over a hole that is 50 μm in diameter. The mechanical stability of a thin metal layer is of concern, and it is likely that this would collapse before the TWI was filled with copper.

The second concern is that the Bosch etch process is configured for silicon etching only. In order to make electrical contact with the bond pad, the field oxide underneath must also be removed. Wet etching of this film would be impractical due to high aspect ratio of the via (in this study, 500 μm deep and 50 μm wide). It is unlikely that etch byproducts and residues could be removed from the bottom of such a deep hole. In addition, in a more complex device, many additional layers would exist between the substrate and the bond pad, all of which would need to be removed from the bottom of the via. The final concern with this process is the fact that the organic insulator is deposited prior to copper deposition. Without a practical way to remove the insulator from the bottom of the via, the insulating film would prevent conductivity between the copper and bond pad.

Based on the multiple concerns described above, this option was not further considered.

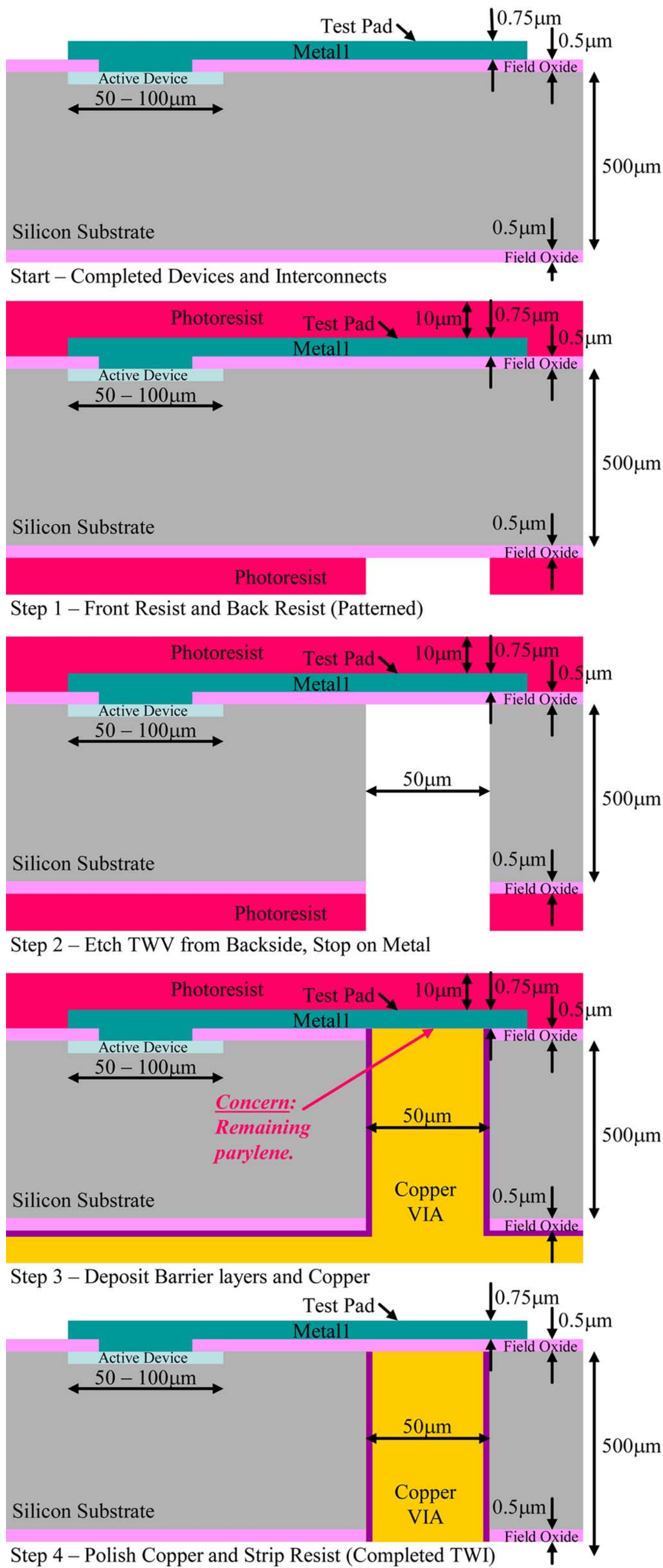

Fig. 4. Backside process.

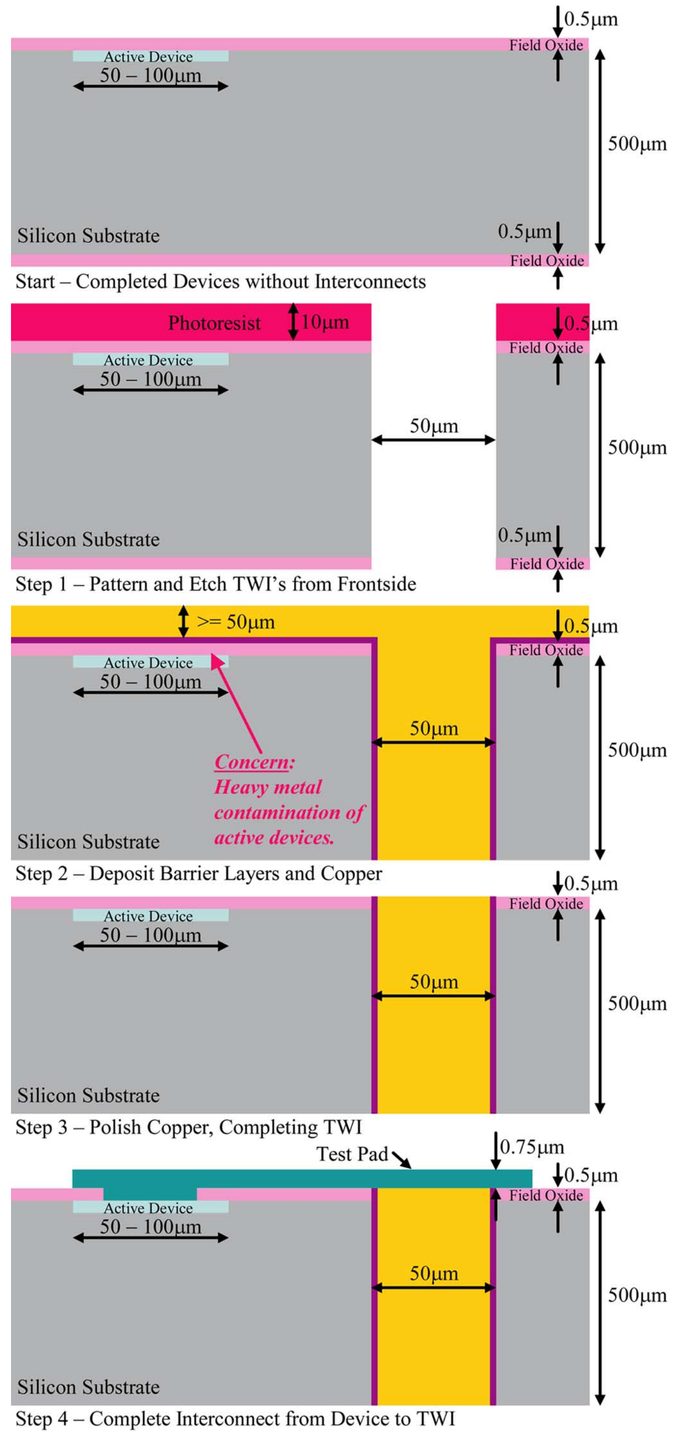

Fig. 5. Insertion process.

B. *Option #2—Insertion Process*

The next approach considered was to fabricate the TWIs from the wafer frontside prior to the deposition and patterning of the bond pad metal layer. The main reason for considering this approach was cost effectiveness, as it requires only eight additional processing steps and one additional mask layer. This process is summarized in Fig. 5.

Examination of the cross-sectional diagrams clearly demonstrates that there is very little protection between the active devices and a significant source of copper contamination, the frontside electroplated copper layer. Although the TiN layer is designed to prevent diffusion of copper, the layer is thin and the possibility of contamination is high. In addition, it is relatively impractical to insert a packaging process into the middle of the chip processing. Since processes required for packaging

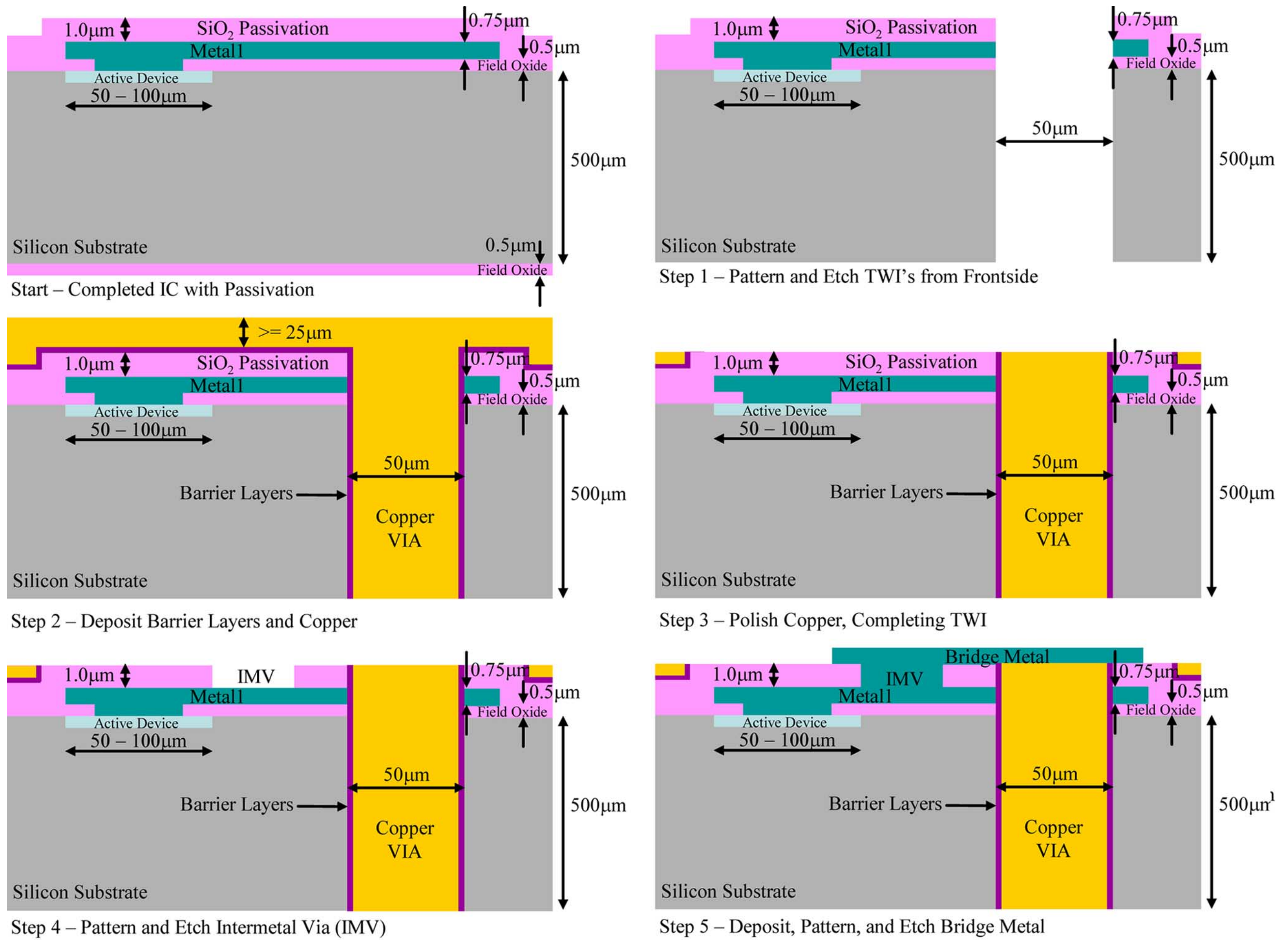

Fig. 6. Bridge process.

are typically conducted on a different production line and often in a different location, the industry would be resistive to this change. In some applications, the processing for the TWI could be incorporated into back end of the line processing with adequate protection of the devices.

C. Option #3—Bridge Process

The final option considered was to process the TWIs from the frontside of the wafer (following all device processing), and then construct a metal bridge to electrically connect the TWIs to the bond pads. This approach alleviates the concerns from the previous two approaches. The processing is designed so that the devices are protected from metal contamination as well as potentially damaging process steps. The tradeoff is in complexity and cost effectiveness. This approach requires more processing steps (12 total), including an additional metal layer, and two additional masking operations (three total). This option was selected for further experimentation. The process is summarized in Fig. 6 with each step described below.

Step 1—Photoresist Patterning: The TWIs are fabricated in the center of the bond pads. Therefore, the first mask (TWI) is aligned to the bond pads. Photoprocessing is identical to that described earlier.

Step 2—Surface Layer Removal: Following photoresist patterning, the surface layers, including the bond pad metal, oxide, and other metal layers are etched away to the underlying substrate. For the wafers in this study, the layers removed include silicon dioxide and aluminum.

Step 3—Etch via Through Wafer: The exact effect of the harsh plasma environment on the active devices is unknown. Electrical testing is done following this step to look for any plasma induced damage to the devices.

Step 4—Deposit Barrier Layers, Seed Layer, and Bulk Copper: As previously described.

Step 5—Polish Copper, Remove Insulator and Barrier Layer: Copper on the surface of the wafer is completely removed. The insulator layers and barrier layers deposited in the vias are also present on the surface and are removed. Following the filling and polishing of the copper via, the barrier layers prevent electrical connection between the TWI and the bond pad metal. For this reason, a metal bridge is now constructed.

Step 6—Pattern and Etch IMV: Before constructing the bridge, another via is opened in the passivation layer exposing the bond pad metal layer. This second photomask is called intermetal via (IMV). The IMV must be centered on the metal interconnect leading to the bond pad.

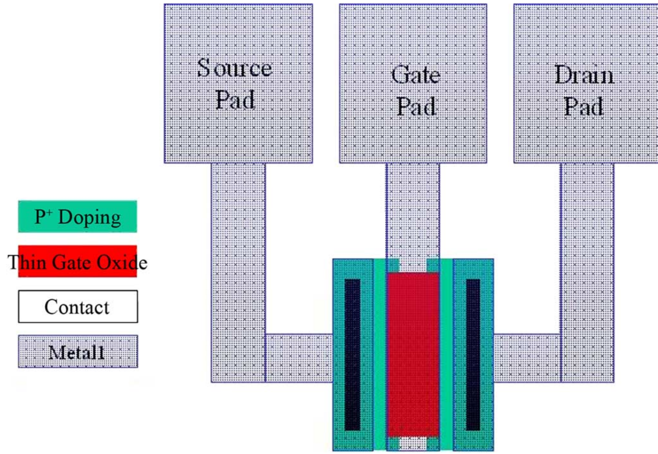

Fig. 7. pMOS transistor composite layout—Before TWI processing.

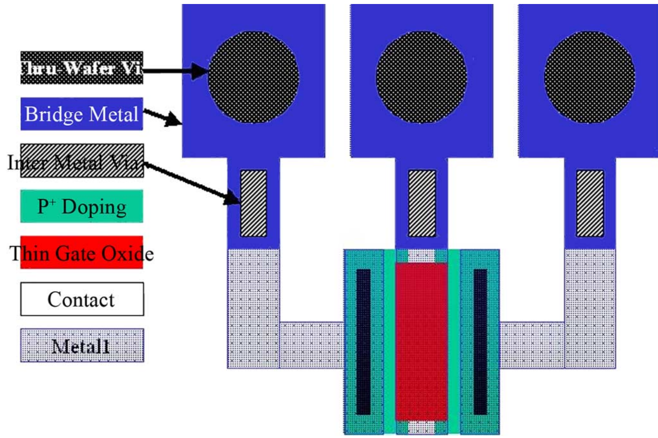

Fig. 8. pMOS transistor composite layout—Including TWI layers.

Step 7—Deposit and Pattern Metal Bridge: The bridge metal layer is deposited, and patterned. The final patterning operation is called the bridge mask (BRDG). The bridge overlays both the TWI and IMV.

D. Photomasks to Accompany the Bridge Process

Three photomasks were designed for the TWI bridge process. Fig. 3 is the cross-sectional view of the pMOS transistor. Fig. 7 shows a composite layout diagram of a single pMOS transistor prior to TWI processing (four masks total). Fig. 8 shows the same composite layout with the three additional mask layers required for the TWI bridge process superimposed. For simplicity, the 50-μm TWIs were located in the center of each 100-μm bond pad on the test chip. The IMVs are much smaller (10 μm was chosen due to the wet etch processing being used) and could be placed anywhere directly over the metal interconnect in near proximity to the TWI. Finally, the bridge metal must overlap both the IMV and the TWI with sufficient margin for alignment error. Optical micrographs of 80 μm/20 μm and 30 μm/90 μm (width/length) pMOS transistors both before TWI processing and after the vias have been etched through the center of the bond pad are shown in Fig. 9.

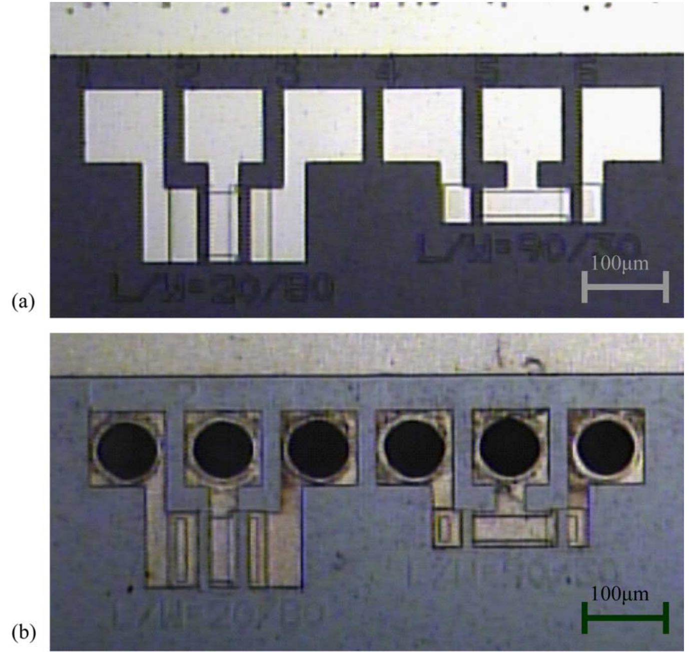

Fig. 9. Optical micrographs of 20 μm/80 μm (left) and 90 μm/30 μm (right) pMOS transistors both (a) before TWI processing and (b) after the vias has been etched through the center of the bond pad.

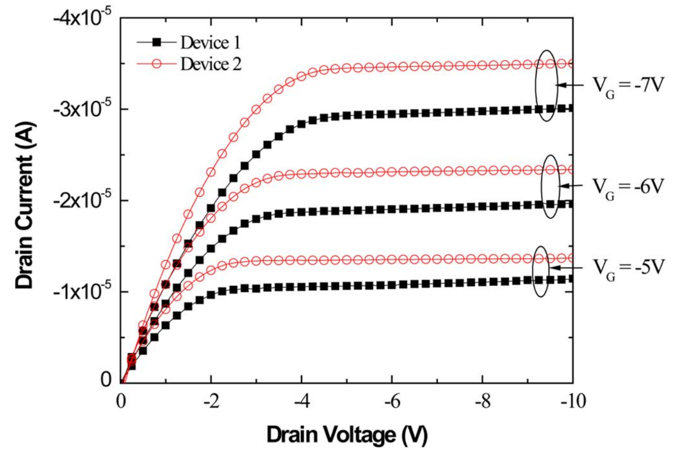

Fig. 10. Drain current versus drain voltage for two pMOSFET devices addressed from the backside of the wafer following full processing.

IV. Electrical Characterization of TWI-Accessed Devices

A. Initial Results From Full Process

To assess electrical continuity of the TWI to the MOSFET and device functionality, electrical characteristics of the device were measured following the full process. Measurements were obtained by probing the TWI from the backside of the wafer. Data are presented that were acquired from devices addressed by probing the TWIs from the backside of the wafer. In addition, statistical data obtained from before processing is shown. Fig. 10 shows the drain current as a function of drain voltage at several gate voltages for two pMOSFETs addressed from the

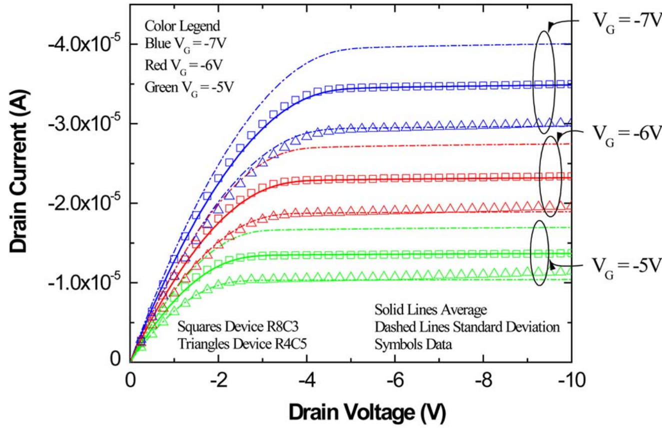

Fig. 11. Drain current versus drain voltage for pMOSFET devices both before (average and standard deviation lines) and after TWI processing (symbols).

backside of the wafer. These data clearly demonstrate that following the full process the devices can be electrically addressed from the back side of the wafer and are functional. Electrical results for several devices on the same wafer are compared with the statistical data of devices before processing in Fig. 11. The performance of the devices after formation of the TWI is within the range of the behavior prior to processing. This result establishes that TWIs can be incorporated into an active device wafer allowing this technique to be used for 3-D packaging of integrated circuits.

B. Investigation of Plasma Induced Damage

Since the initial results were encouraging, a second set of wafers were processed where the effects of TWI processing were more fully characterized. One of the primary concerns with the bridge metal process is damage to the gate oxide of the pMOSFET devices when etching through the wafer to form the via. The etch procedure is a plasma process which can result in plasma induced damage (PID) of the gate oxide [26]–[28]. Since the etch is from the top side of the wafer, charged particles that collect on the gate electrode create a voltage drop across the gate oxide. If the electrical field is significant enough, damage occurs to the gate oxide severely affecting the MOSFET performance. In this study, the devices have a 1-μm oxide passivation layer to help minimize PID.

To determine if the Bosch etch process is causing PID, MOSFET characteristics were taken at several stages during the process, before and after the etch process including the first electrical characterization step, and the second electrical characterization step, as shown in the process flow chart in Fig. 12. In order to contact the device for the second electrical characterization step, a portion of the oxide over the aluminum bond pad was removed. Two different pMOSFET devices, 30 μm/90 μm and 80 μm/20 μm, both with a gate oxide thickness of 70 nm were investigated. The device parameters examined were gate oxide leakage current $(I_G - V_G)$, on-current $(I_{\rm ON})$, off-current $(I_{\rm OFF})$, threshold voltage $(V_{\rm THP})$, and family of curves $(I_D - V_D)$. The test conditions for each of these test are summarized Table I and typical results from these tests are discussed and presented.

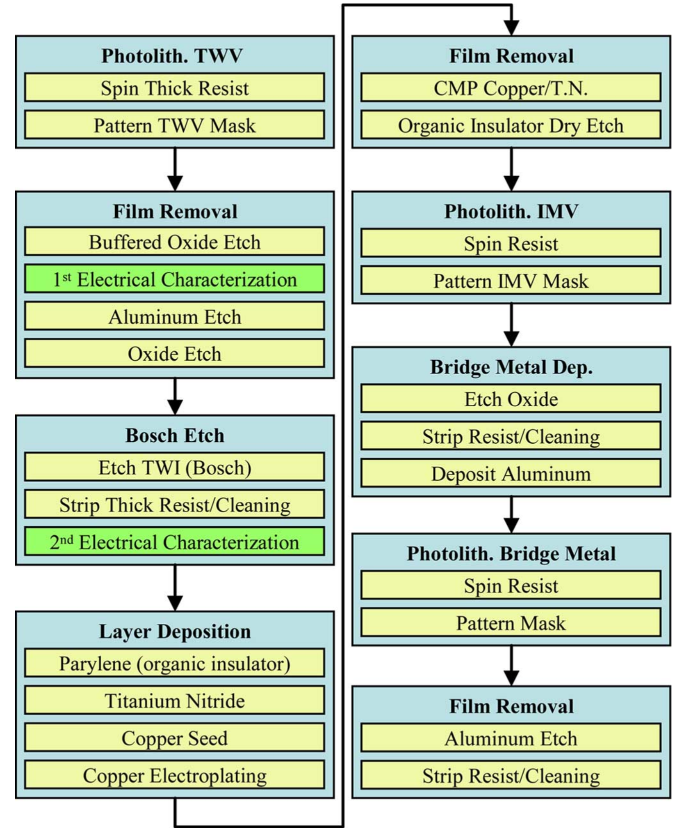

Fig. 12. Process flow for creation of TWI with additional electrical characterization points indicated.

TABLE I
pMOSFET MEASURED PARAMETERS AND TERMINAL BIAS CONDITIONS

Parameter	Source (V)	Drain (V)	Substrate (V)	Gate (V)	Voltage Steps
I_G-V_G	G	G	G	5 to -5	50 mV
I_{on} and I_{off}	G	-5	G	0 to 5	50 mV
V_{THP}	G	0.1	G	0 to -5	50 mV
I_D-V_D	G	0 to -10	G	-3 to -7	Drain: 50 mV Gate: -1V

G = ground

Of the 48 devices tested before and after the Bosch process, 44, or 91.6%, of the devices survived. An increase in gate leakage current (Fig. 13) was observed following the etch process ranging from $\sim 10^{-12}$ A to $\sim 10^{-7}$ A. An overall decrease in the on-current was observed (Fig. 14) ranging from 4% to 23% while in several cases off-current improved (this result is likely due to the simple pMOSFET device). Fig. 15 shows a threshold shift increasing between 1% to 14%. A decrease in the drive current is exhibited in the family of curves for all gate voltages. (Fig. 16). At the greatest applied gate voltage, the drive current decrease within a range of 4%–23%.

In addition to monitoring MOSFET device characteristics as an indication of PID, time zero dielectric breakdown (TZDB) tests [29], to determine the dielectric voltage breakdown strength of the devices, were performed before and following the plasma process. The ramp rate of the TZDB test is 1 MV/cm$\cdot$s. If the gate oxide is damaged due to the Bosch process, a lower breakdown strength of the oxide would be expected. Of the total 20 pMOSFET 30 μm/90 μm devices tested

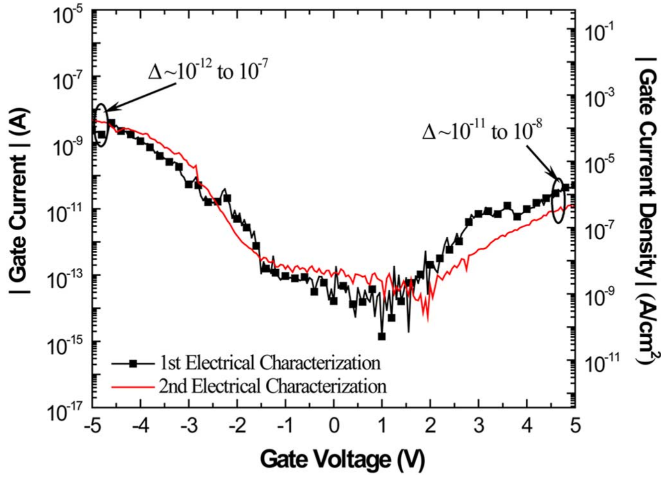

Fig. 13. Typical gate oxide leakage current before the Bosch etch process (first *Electrical Characterization*) and after the Bosch etch process (second *Electrical Characterization*) (PID study).

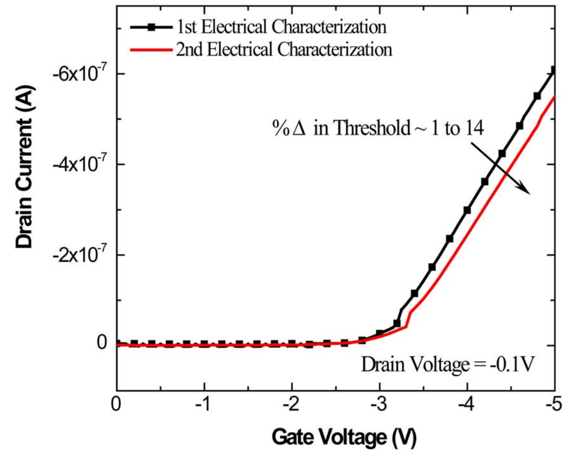

Fig. 15. Threshold Voltage measurement before the Bosch etch process (first *Electrical Characterization*) and after the Bosch etch process (second *Electrical Characterization*) (PID study).

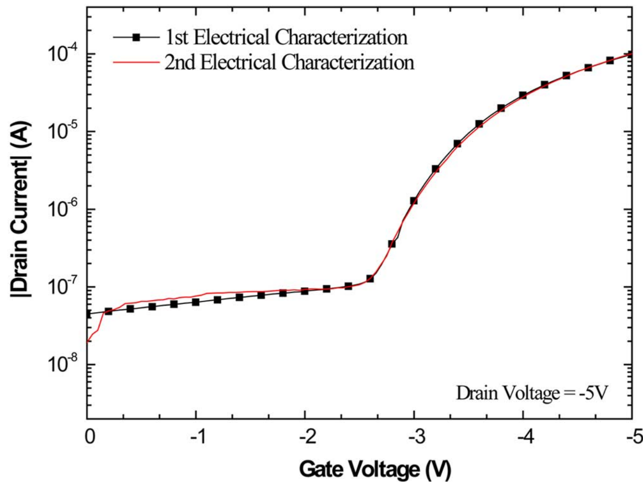

Fig. 14. On-current and off-current before the Bosch etch process (first *Electrical Characterization*) and after the Bosch etch process (second *Electrical Characterization*) (PID study).

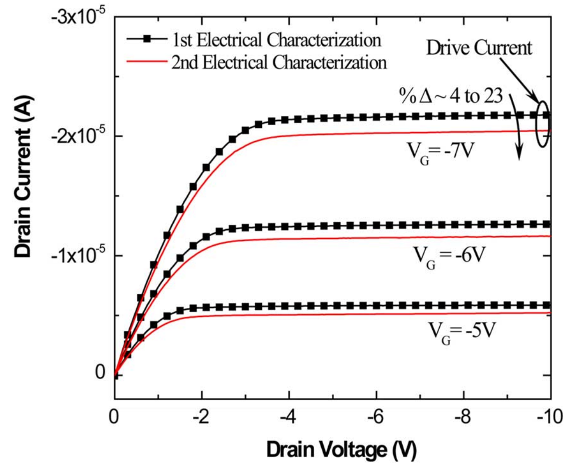

Fig. 16. Family of Curves measurement before the Bosch etch process (first *Electrical Characterization*) and after the Bosch etch process (second *Electrical Characterization*) (PID study).

before the Bosch process, the average breakdown strength was −13.65 V with a standard deviation of 1.98 V. The average breakdown strength after the Bosch process was −13.12 V with a standard deviation of 1.90 V which is not a significant change. The same holds true of the 80 μm/20 μm pMOSFETs for which the breakdown strength before the Bosch process was −14.22 V with a standard deviation of 1.31 V and the breakdown strength after was −14.59 V and a standard deviation of 1.02 V. Plotting the voltage at breakdown (V_{bd}) for both devices tested before and after the Bosch process using a Weibull distribution also indicates no significant change (Fig. 17, only 80 μm/20 μm devices are shown). If a change had occurred, one would expect a unilateral shift to the left in the breakdown strength of gate dielectric. These results indicated that the gate oxide did not suffer significant damage from the Bosch process, an important step in creating TWIs.

Since the Bosch etch is the one process step that deviates significantly from current processing techniques applied to active

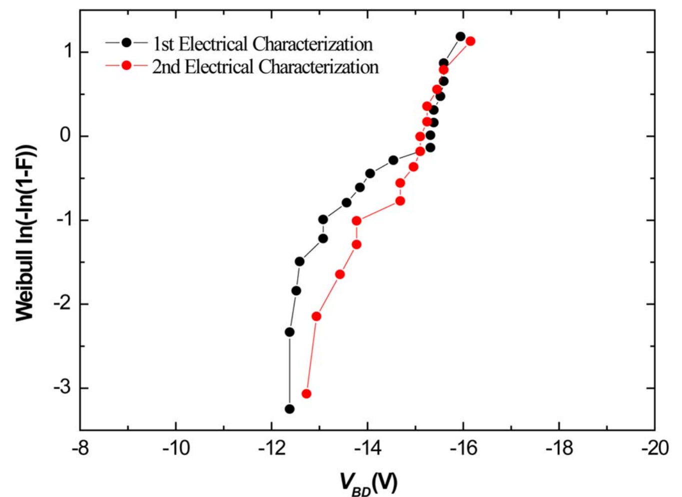

Fig. 17. Weibull Analysis of RVS results comparing the dielectric strength of devices before the Bosch etch process (first *Electrical Characterization*) and after the Bosch etch process (second *Electrical Characterization*) for the 80μm/20 μm pMOSFET devices.

device wafers, extra attention was given to the electrical characterization of the devices following etch. After testing of the specific devices, these wafers did not continue through the rest of the process.

V. Conclusion

Three different process flows were investigated to incorporate TWIs in wafers with active devices allowing for 3-D stacking of chips. Of the three process flows discussed, the bridge process has the fewest concerns with regard to the integrity of the preexisting microcircuitry, and therefore, it was the one selected for the active device test. TWI's were fabricated in wafers with pMOSFET devices. Following processing, the devices were accessed from the backside of the wafer and the performance of the devices was shown to be similar to the performance before processing. Time zero dielectric breakdown tests revealed little change in the gate oxide voltage breakdown strength. This work demonstrates the feasibility of stacking chips using TWIs for the electrical connection between chips and to the underlying substrate.

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Jim Jozwiak was born in South Bend, IN, on March 27, 1964. He received the B.S. and M.S. degrees in electrical engineering from Purdue University, West Lafayette, IN, in 1986 and 1987, respectively, and the M.S. degree in adult education from the University of Idaho, Boise, in 2004.

In 1987, he joined Intel Corporation where he worked as a process engineer, and subsequently a process engineering group leader, in chemical vapor deposition and photolithography for submicron logic processing. In 1999, he joined Boise State University, Boise, IN, as a faculty member in the Electronics Department. He was subsequently appointed to head the Semiconductor Technology program at Boise State University. In 2006, he joined Micron Technology, Inc., Boise, ID, as a workforce development engineer. In this position, he is currently working as a technical trainer in advanced research and development. He has one published paper in a refereed journal. He has written, or cowritten, five modules for technical training in semiconductor processing under a grant from the National Science Foundation, and he has presented at three technical conferences.

Mr. Jozwiak was recognized with the Motorola Educator of the Year award, in 2002.

Richard G. Southwick, III (M'04) was born in Cedar City, UT, on March 22, 1981. He received the B.S. degree in electrical engineering, in 2004, from Boise State University, Boise, ID, where he is currently working toward the M.S. degree. He has been accepted into the Ph.D. program in electrical engineering at Boise State University.

His research interests include gate oxide reliability studies and alternative gate oxide dielectrics.

Vaughn N. Johnson was born in Taos, NM, on January 9, 1974. He received the B.S. degree in electrical engineering from Boise State University, Boise, ID, in 2002.

In 2005, he joined Micron Technology, Inc., Boise, ID, as a Product Engineer. Currently, he works on PSRAM research and development.

William B. Knowlton (M'00) was born in Sewart Air Force Base, TN, on June 15, 1960. He received the B.S., M.S., and Ph.D. degrees in materials science and engineering from the University of California, Berkeley, in 1992, 1995, and 1998, respectively. His doctoral work included the study of point defects and modeling diffusion in silicon and the development, fabrication, characterization of dark matter particle detectors, X-ray detectors, and far-infrared resonant detectors.

In 1997, he joined Hewlett Packard Laboratories where he studied dislocations and structural properties in heteroepitaxial grown thin film and bulk grown GaN materials systems to optimize light output in LEDs. He joined Insight Analytical Laboratories in 1998 where he consulted and performed electromigration and dielectric reliability studies. In 2000, he joined the faculty in Electrical and Computer Engineering at Boise State University, Boise, ID. He has codeveloped five new programs and a Department in Materials Science and Engineering where he is the Program Coordinator for Graduate Studies and holds a joint appointment. He has published over 30 papers in peer reviewed journals or conferences. His research activities include device and simple circuit reliability physics, materials characterization, nanofabrication of materials, biomaterials, and molecular electronic devices.

Prof. Knowlton is a member of the Materials Research Society and the American Physical Society. From 2002 to 2005, he has been a member of the organizing committee for the IEEE International Integrated Reliability Workshop.

Amy J. Moll received the B.S. degree in ceramic engineering from University of Illinois, Urbana, in 1987, and the M.S. and Ph.D. degrees are in materials science and engineering from University of California, Berkeley, in 1992 and 1994, respectively.

Following graduate school, she worked for Hewlett Packard/Agilent Technologies for six years in several roles including Research and Development Engineer and Production Manager for the Optoelectronics Division in San Jose, Process Engineering Manager for the Colorado Springs Technology Center, and Project Manager for corporate procurement. She was an Adjunct Professor at San Jose State University from 1996 to 1998. In 2000, she joined the faculty of Mechanical Engineering at Boise State University, Boise, ID, where she has codevelop five new programs and is the Chair of the new Department of Materials Science and Engineering. She has published over 15 papers in peer reviewed journals or conferences. Her research has focused on microelectronic processing, in particular in through-wafer interconnects, advanced packaging issues, and the development of MEMs devices in multilayer ceramic materials. She has been involved in several conferences and workshops on materials science and engineering education.

Prof. Moll is a member of the Materials Research Society, the Society of Women Engineers, and the American Society for Engineering Education.