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Conditions for Capacitor Voltage Regulation in a Five-Level Cascade Multilevel Inverter: Application to Voltage-Boost in a PM Drive

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***Abstract*— A cascade multilevel inverter is a power electronic device built to synthesize a desired AC voltage from several levels of DC voltages. Such inverters have been the subject of research in the last several years, where the DC levels were considered to be identical in that all of them were either batteries, solar cells, etc. Similar to previous results in the literature, the work here shows how a cascade multilevel inverter can be used to obtain a voltage boost at higher speeds for a three-phase PM drive using only a single DC voltage source. The input of a standard three-leg inverter is connected to the DC source and the output of each leg is fed through an H-bridge (which is supplied by a capacitor) to form a cascade multilevel inverter. A fundamental switching scheme is used, which achieves the fundamental in the output voltage while eliminating the fifth harmonic. A new contribution in this paper is the development of explicit conditions in terms of the power factor and modulation index for which the capacitor voltage of the H-bridges can be regulated while simultaneously maintaining the aforementioned output voltage. This is then used for a PM motor drive showing the machine can attain higher speeds due to the higher output voltage of the multilevel inverter compared to using just a three-leg inverter.**

I. Introduction

The work here shows how a cascade multilevel inverter (CMLI) using only a *single* DC voltage source can be used to obtain a voltage boost at higher speeds for a three-phase PM drive compared to a standard three-leg inverter with the same DC source. Figure 1 shows one leg of a standard three-leg inverter connected to a DC source with output of the leg fed through an H-bridge supplied by a capacitor, to form the CMLI. A fundamental switching scheme is used and it is chosen so that the output voltage waveform achieves the desired fundamental while eliminating the fifth harmonic. Explicit conditions are given in terms of the power factor and modulation index to characterize when the capacitor voltage of the H-bridges can be regulated to a desired constant value, while simultaneously having the CMLI maintain the desired output voltage.

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II. Multilevel Inverter Architecture and Operation

A cascade multilevel inverter is a power electronic device built to synthesize a desired AC voltage from several levels of DC voltages. Such inverters have been the subject of research in the last several years [1][2][3][4], where the DC levels were considered to be identical in that all of them were either batteries, solar cells, etc. In [5], a multilevel converter was presented in which the two separate DC sources were the secondaries of two transformers coupled to the utility AC power. Corzine et al [6] have proposed using a single DC power source and capacitors for the other DC sources. A method was given to transfer power from the DC power source to the capacitor in order to regulate the capacitor voltage. A similar approach was later (but independently) proposed by Du et al [7]. These approaches required a DC power source for each phase. Similar methods have also been proposed by Veenstra and Rufer [8][9].

The approach here is similar to that of Corzine et al [6] and Du et al [7] with the important exception that only a single standard 3-leg inverter is required as the power source (one leg for each phase) for the three phase multilevel inverter [10]. A significant contribution of this paper is the development of explicit conditions in terms of the modulation index and power factor for when such a topology can be used to boost the output voltage compared to a standard three-leg inverter.

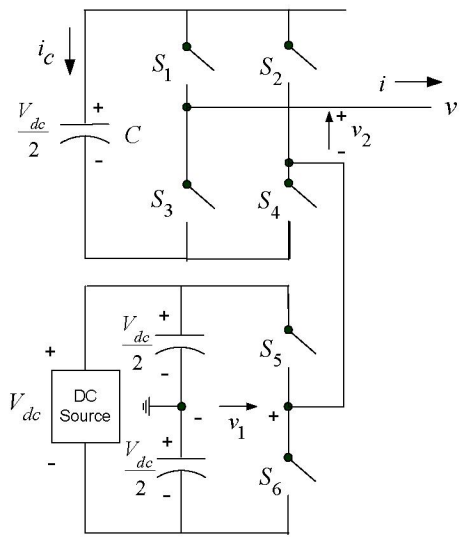

Fig. 1. One leg of a 3-leg inverter connected to a full H-bridge with a capacitor DC source.

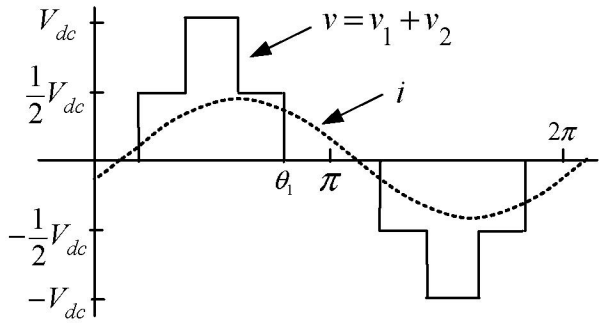

Fig. 2. Output waveform

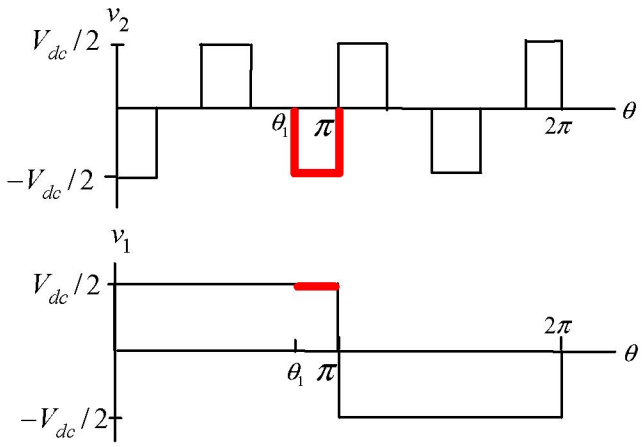

Fig. 3. One way to make the output voltage zero for $\theta_1 \leq \theta \leq \pi$ is to set $v_1 = +V_{dc}/2$ and $v_2 = -V_{dc}/2$.

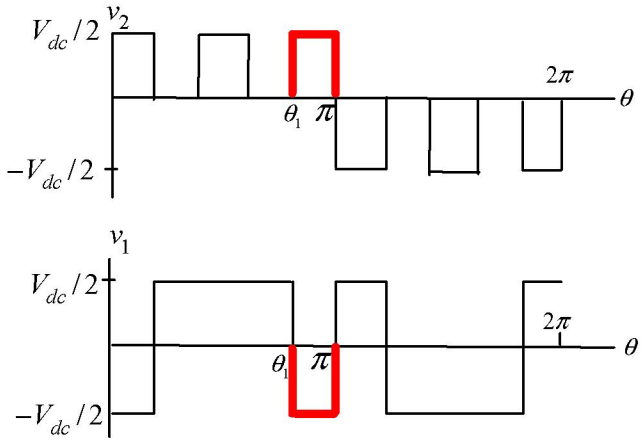

Fig. 4. Another way to make the output voltage zero for $\theta_1 \leq \theta \leq \pi$ is to set $v_1 = -V_{dc}/2$ and $v_2 = +V_{dc}/2$.

To proceed, consider the left-side of Figure 1, which shows a DC source connected to a single leg of a standard 3-leg inverter. The output voltage v_1 of this leg (with respect to the ground) is either $+V_{dc}/2$ (S_5 closed) or $-V_{dc}/2$ (S_6 closed). This leg is connected in series with a full H-bridge, which in turn is supplied by a capacitor voltage. If the capacitor is kept charged to $V_{dc}/2$, then the output voltage of the H-bridge can take on the values $+V_{dc}/2$ ($S_1\&S_4$ closed), 0 ($S_1\&S_2$ closed or $S_3\&S_4$ closed), or $-V_{dc}/2$ ($S_2\&S_3$ closed). An example output waveform that this topology can achieve is shown in Figure 2.

When the output voltage $v = v_1 + v_2$ is required to be zero, one can either set $v_1 = +V_{dc}/2$ and $v_2 = -V_{dc}/2$ as in Figure 3 or $v_1 = -V_{dc}/2$ and $v_2 = +V_{dc}/2$ as in Figure 4. It is this flexibility in choosing how to make the output voltage zero that is exploited to regulate the capacitor voltage. As an example, in Figure 2, in the interval $\theta_1 \leq \theta \leq \pi$, the output voltage is zero and the current $i > 0$. If $S_1\&S_4$ are closed (so that $v_2 = +V_{dc}/2$) along with S_6 closed (so that $v_1 = +V_{dc}/2$), then the capacitor is *discharging* ($i_c = -i < 0$) and $v = v_1 + v_2 = 0$. On the other hand, if $S_2\&S_3$ are closed (so that $v_2 = -V_{dc}/2$) and S_5 is also closed (so that $v_1 = +V_{dc}/2$), then the capacitor is *charging* ($i_c = i > 0$) and $v = v_1 + v_2 = 0$.

The case $i < 0$ is accomplished by simply reversing the switch positions of the $i > 0$ case for charge and discharge of the capacitor. Consequently, the method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output, either the switches S_1, S_4, and S_6 are closed or the switches S_2, S_3, and S_5 are closed depending on whether it is necessary to charge or discharge the capacitor.

III. Conditions for Capacitor Voltage Regulation

As Figure 2 illustrates, the ability to regulate the capacitor voltage depends on the power factor. Let

$$\begin{aligned} v_f(\theta) &= V\sin(\theta) \\ i(\theta) &= I\sin(\theta - \varphi) \end{aligned}$$

where $v_f(\theta)$ is the fundamental component of the output voltage, $i(\theta)$ is the current, and φ is the power factor angle (phase angle of the current with respect to the voltage). The objective here is to compute the conditions on switching angles θ_1 and θ_2, and the power factor angle φ to ensure the capacitor can be regulated to a desired value.

A. Case 1 $0 < \varphi < \theta_1$

Consider the case where $0 < \varphi < \theta_1$ as illustrated in Figure 5.

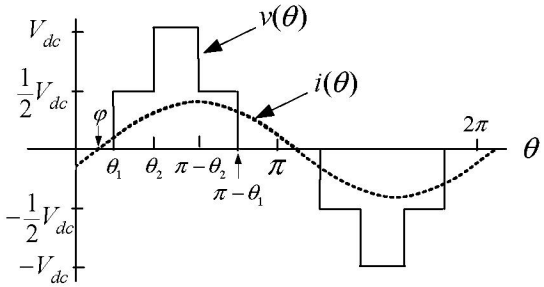

Fig. 5. $0 < \varphi < \theta_1$

During the interval $\theta_2 < \theta < \pi - \theta_2$, the capacitor loses the amount of charge $\int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta$ while during the intervals $0 < \theta < \theta_1$ and $\pi - \theta_1 < \theta < \pi$ the capacitor can be recharged (by choosing the switch positions appropriately) by the amounts $\int_0^{\varphi} I\,|\sin(\theta-\varphi)|\,d\theta + \int_{\varphi}^{\theta_1} I\sin(\theta-\varphi)d\theta$ and $\int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta$, respectively. In this case, keeping the capacitor charged requires

$$\int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta \le \int_0^{\varphi} I\,|\sin(\theta-\varphi)|\,d\theta + \int_{\varphi}^{\theta_1} I\sin(\theta-\varphi)d\theta + \int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta$$

which reduces to

$$\cos(\varphi) \le \frac{1}{\cos(\theta_1)+\cos(\theta_2)} \tag{1}$$

B. Case 2 $\theta_1 < \varphi < \pi/2$

Consider the case $\theta_1 < \varphi < \pi/2$ as shown in Figure 6.

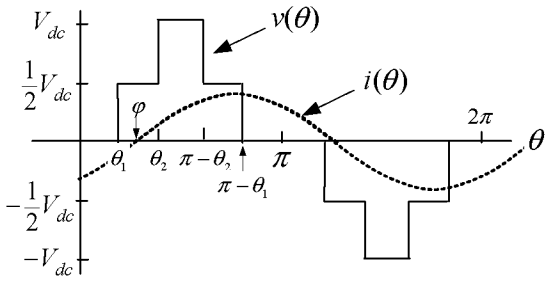

Fig. 6. $\theta_1 < \varphi < \pi/2$

During the interval $\theta_2 < \theta < \pi - \theta_2$, the capacitor loses the amount of charge $\int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta$ while during the intervals $0 < \theta < \theta_1$ and $\pi - \theta_1 < \theta < \pi$ the capacitor can be recharged (by choosing the switch positions appropriately) by the amount $\int_0^{\theta_1} I\,|\sin(\theta-\varphi)|\,d\theta + \int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta$. Thus keeping the capacitor voltage regulated requires

$$\int_{\theta_2}^{\pi-\theta_2} I\sin(\theta-\varphi)d\theta \le \int_0^{\theta_1} I\,|\sin(\theta-\varphi)|\,d\theta + \int_{\pi-\theta_1}^{\pi} I\sin(\theta-\varphi)d\theta$$

which reduces to

$$\frac{\cos(\theta_2)}{\sin(\theta_1)} \le \tan(\varphi). \tag{2}$$

In summary, the conditions for capacitor voltage regulation in terms of the switching angles θ_1 and θ_2, and the power factor φ are $\left(m \triangleq \cos(\theta_1)+\cos(\theta_2) = V_1/\left(\frac{4}{\pi}\frac{V_{dc}}{2}\right)\right)$

$$\begin{aligned} &0 < \varphi < \theta_1 \quad \text{for} \quad \varphi \ge \cos^{-1}(1/m) \\ &\theta_1 < \varphi < \pi/2 \quad \text{for} \quad \varphi \ge \tan^{-1}\left(\frac{\cos(\theta_2)}{\sin(\theta_1)}\right). \end{aligned} \tag{3}$$

Notice the two conditions are identical at the boundary where $\varphi = \theta_1$. In order to achieve the fundamental in the desired output voltage while eliminating the fifth-harmonic (Only one harmonic can be eliminated using this switching scheme and the fifth is typically significant in a three-phase system), the switching angles must satisfy

$$\begin{aligned} \cos(\theta_1)+\cos(\theta_2) &= m \\ \cos(5\theta_1)+\cos(5\theta_2) &= 0 \end{aligned} \tag{4}$$

Figure 7 is a plot of θ_1 and θ_2 (in degrees) that solve (4) versus m (the modulation index is $m/2$).

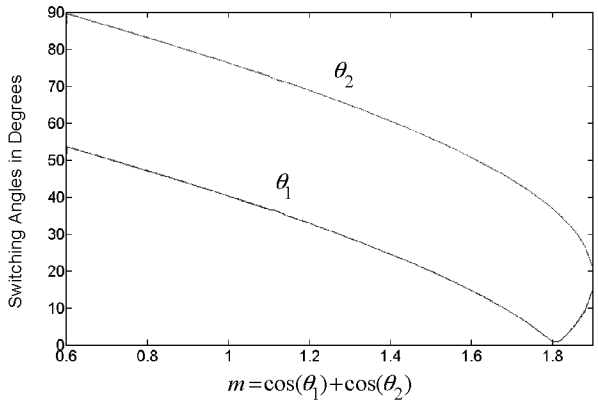

Fig. 7. θ_1 and θ_2 versus m.

Thus, for any given value of m and φ, the values of θ_1 and θ_2 are found via Figure 7 and thus whether or not the capacitor voltage can be regulated is straightforwardly checked using the conditions (3). What these conditions say is, for any given value of m in the interval $0.6 \le m \le 1.909$ (i.e., where conditions (4) have a solution), the capacitor voltage can be regulated provided the power factor angle is large enough. Note that both m and φ increase as the motor speed goes up.

IV. Fundamental Frequency Switching

In the simulations presented here, the DC link voltage V_{dc} was set to 200 V (so that the 3-leg inverter produces ± 100 V), the capacitors were regulated to 100 V, the motor's inertia is $J = 0.1$ kg-m^2, the motor has $n_p = 4$ pole-pairs, the stator resistance is $R_S = 0.065$ Ohms, the stator inductance is $L_S = 3$ mH, the torque/back-emf constant $K_T = K_b = 0.37$ Nm/A (V/rad/sec), and the load torque $\tau_L = 19$ Nm at peak speed. The capacitor value for the H-bridges is $C = 0.01$ F.

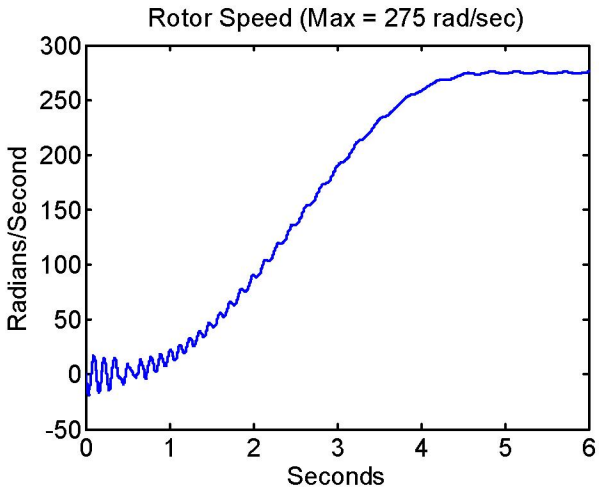

Fig. 8. Rotor speed in rad/sec versus time in seconds.

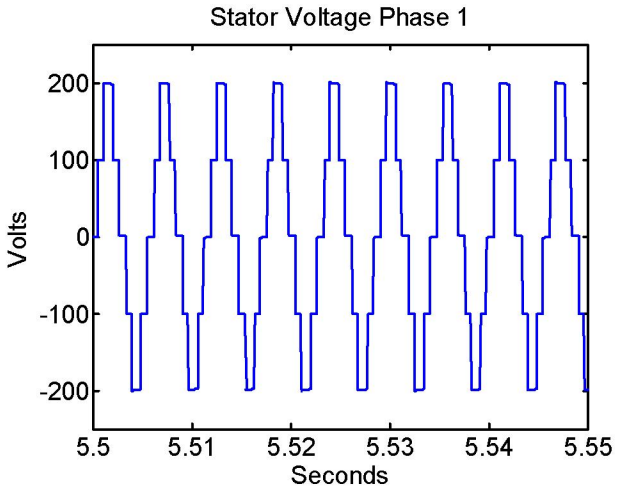

Fig. 9. Enlarged view of the phase 1 voltage in Volts vs time in sec.

The motor was run open-loop with the magnitude of the fundamental of the stator voltage ramped from 90 V to 180 V during the time interval from 0 to 3 seconds (Note that the three-leg inverter produces ± 100 V so the capacitor sourced H-bridges provide the boost up to ± 190 V). The stator electrical frequency f_S was brought up smoothly from 0 to 175 Hz in 5 seconds resulting in a peak speed of $2\pi f_S/n_p = 275$ rad/sec. The resulting speed response is shown in Figure 8, which is somewhat oscillatory due to the open-loop control. A viscous friction load torque was used with the viscous friction coefficient chosen to be $f = 0.07$ (quite large) so that at maximum speed the load torque was $f\omega_{\max} = f(2\pi f_S/n_p) = (0.07)(275) = 19$ Nm. An enlarged section of the inverter output voltage of phase 1 is given in Figure 9 illustrating the fundamental switching scheme for a stator frequency of $f_S = 175$ Hz. The capacitor voltage for one of the H-bridges is shown in Figure 10 showing that the scheme regulates the voltage within 3 volts of the nominal value. The value of the capacitance is $C = 0.01$ F. An enlarged view of the capacitor voltage for $5.5 \leq t \leq 5.525$ is shown in Figure 11.

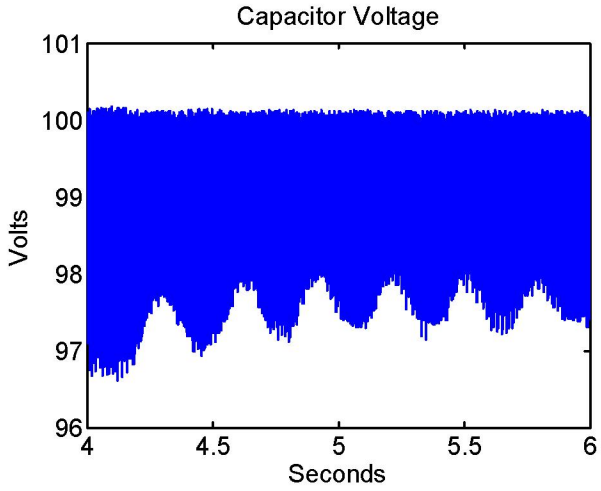

Fig. 10. Capacitor voltage versus time.

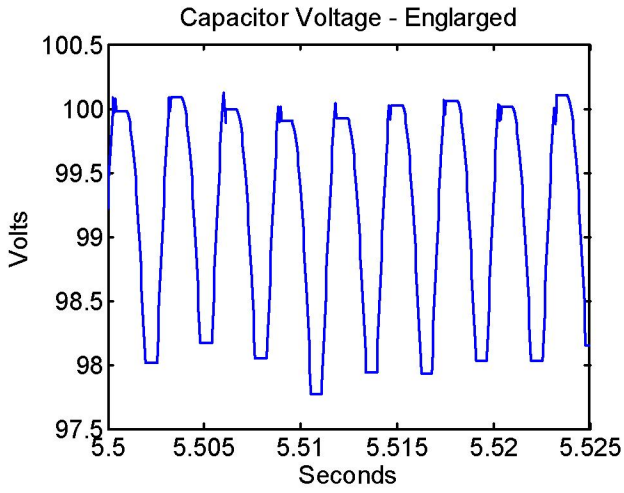

Fig. 11. An enlarged view of the capacitor voltage versus time.

The stator current, the stator voltage, and a scaled version of the capacitor voltage are shown in Figure 12.

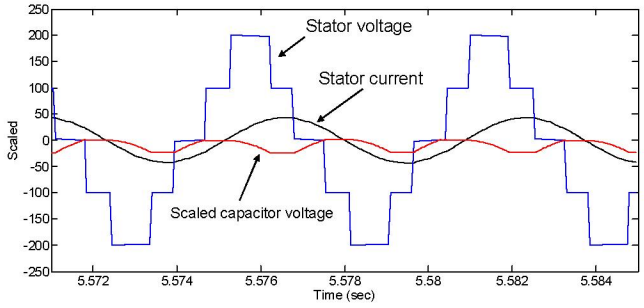

Fig. 12. Scaled capacitor voltage (V), stator current (A), and stator voltage (V) vs time.

Note that the capacitor discharges when the inverter is supplying ± 200 V, stays constant when the inverter is supplying ± 100 V, and recharges when the inverter is supplying 0 V. For example, at about $t = 5.575$ seconds, the stator current becomes positive, the CMLI inverter is supplying 200 V, and the capacitor voltage is decreasing. Following this, the CMLI inverter is supplying 100 V and the capacitor voltage is constant. Next, the CMLI inverter is supplying 0 V and the capacitor is charging so that its voltage increases.

For comparison purposes, the simulation was rerun using just a standard three-leg inverter supplying ± 100 V (In this case, closed-loop vector control of the PM machine was used so that there is no oscillatory behavior in the response). The maximum speed possible was only 212 rad/sec, which is shown in Figure 13 and is due to the voltage limitation. Figure 14 shows one of the stator phase voltages goes into saturation just to obtain this speed. This should be contrasted with the maximum speed of 275 rads/sec obtained using the same DC source and a multilevel inverter (see Figure 8).

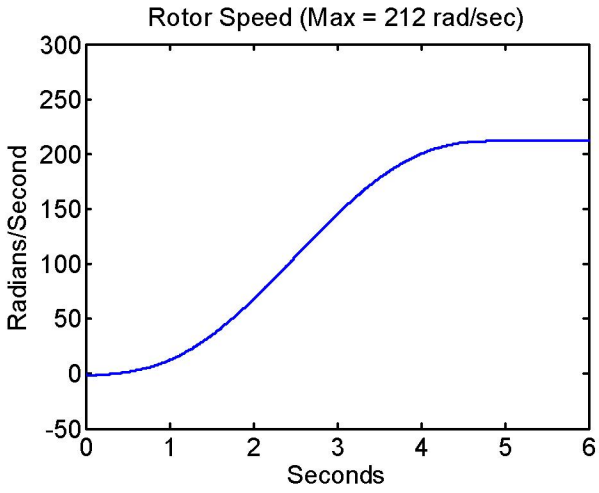

Fig. 13. Rotor speed using a standard 3-leg inverter supplying ± 100 V

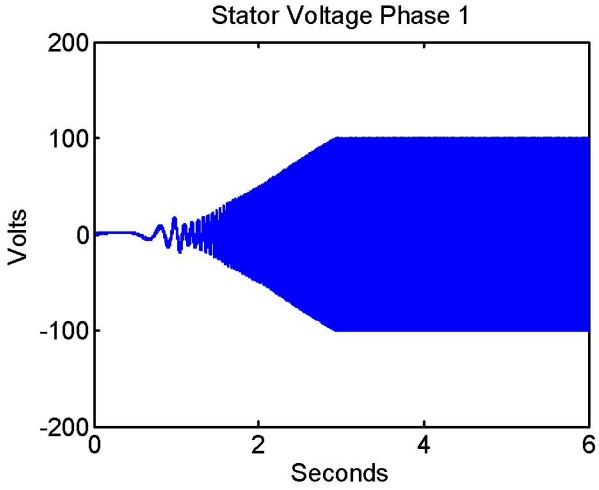

Fig. 14. Stator voltage using a standard 3-leg inverter supplying ± 100 V

V. Conclusions

A cascade multilevel inverter topology has been proposed that requires only a single standard 3-leg inverter and capacitors as the power sources. The capacitors obtain their power from the 3-leg inverter allowing the cascade multilevel inverter to supply significantly more voltage from a given DC power source than just a three leg inverter alone. Simulation results were presented using a fundamental frequency switching scheme. Finally, subject to conditions in terms of the power factor and modulation index [$= m/2$ see (4)], it was shown that the capacitor voltages could be regulated.

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