A RELIABILITY PREDICTION METHOD FOR PHASE-CHANGE DEVICES USING OPTIMIZED PULSE CONDITIONS

by

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DEDICATION

To my wife Jacque, my parents Martin and Judy, my children and family.

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ABSTRACT

Owing to the outstanding device characteristics of Phase-Change Random Access Memory (*PCRAM*), such as high scalability, high speed, good cycling endurance, and compatibility with conventional complementary metal-oxide-semiconductor (*CMOS*) processes, *PCRAM* has reached the point of volume production. However, due to the temperature-dependent nature of the phase-change memory device material and the high electrical and thermal stresses applied during the programming operation, the standard methods of high-temperature (Temperature > 125 °C) accelerated retention testing may not be able to accurately predict bit sensing failures or determine slight pulse condition changes needed if the device were to be programmed at an elevated temperature several times, in an environment where the ambient temperature is between 25 and 125 °C. In this work, a new reliability prediction method, different than standard *PCRAM* reliability methods, is presented. This new method will model and predict a single combination of temperature and pulse conditions for temperatures between 25 and 125 °C, giving the lowest Bit Error Rate (*BER*). The prediction model was created by monitoring the cell resistance distributions collected from sections of the *PCRAM* 1Gigabit (Gb) array after applying a given RESET or SET programming pulse shape at a given temperature, in the range of 25 to 125 °C. This model can be used to determine the optimal pulse conditions for a given ambient temperature and predict the *BER* and/or data retention loss over large arrays of devices on the Micron/Numonyx 45nm *PCRAM* part.

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LIST OF ABBREVIATIONS

BER	Bit Error Rate
BL	Bit Line
CCD	Central Composite Design
CDF	Cumulative Distribution Function
CFR	Constant Failure Rate
CKB	Checkerboard
CMOS	Complementary Metal Oxide Semiconductor
DFR	Decreasing Failure Rate
DMA	Direct Memory Access
DOE	Design of Experiment
E_a	Activation Energy
eV	ElectronVolt
F	Feature Size (half-pitch)
FeRAM	Ferroelectric Random-Access Memory
Gb	Gigabit
H_a	Alternative Hypothesis

H_o	Null Hypothesis
IFR	Increasing Failure Rate
I_{th}	Threshold Current
LPDDR2	Low-Power Double Data Rate synchronous DRAM
μM	MicroMate
MTTF	Mean Time To Failure
NVM	Non-Volatile Memory
PCRAM	Phase-Change Random Access Memory
PDF	Probability Density Function
Qs	SET Quench
RRAM	Resistive Random Access Memory
SoC	System on a Chip
SR	Structural Relaxation
STT- RAM	Spin-Transfer Torque – Random Access Memory
STI	Shallow Trench Isolation
T_g	Glass Transition Temperature
t_{life}	Lifetime (of a device)
T_m	Melting Temperature
$t_{mission}$	Mission Time (of a device)

t_Q	Quenching Time
t_{*set}	Time to SET
t_{50}	Time to 50% (cumulative failure)
T_s	System Temperature (in degrees Kelvin)
T_t	Test Temperature (in degrees Kelvin)
Vr	RESET Voltage
Vread	READ Voltage
Vs	SET Voltage
V_{th}	Threshold Voltage
WL	Word Line
λ	Hazard Rate
λ_s	System Temperature Failure Rate
λ_t	Test Temperature Failure Rate

CHAPTER 1: INTRODUCTION

1.1 Introduction and Motivation

Non-Volatile Memory (*NVM*) data storage technologies play a fundamental role in the semiconductor memory market due to the wide spread use of portable devices such as smart phones, tablet PCs, digital cameras, MP3 players, and personal computers, which require ever increasing memory capacity to improve their performance. Flash memory is the dominant semiconductor *NVM* storage technology; however, with the aggressive scaling (aimed at reducing the cost per bit), the floating-gate storage method is on the verge of reaching its technological limit, for conventional two-dimensional (*2D*) Flash memories [1], [2]. In fact, data retention and reliability of *2D* Flash memory has pushed the semiconductor industry to invest in three-dimensional (*3D*) Flash memory and in alternative emerging memories [3]–[5], such as Spin-Transfer Torque Random-Access Memory (*STT-RAM*) [6]–[8], Ferroelectric Random-Access Memory (*FeRAM*) [9]–[11], Resistive switching Random-Access Memory (*RRAM*) [12], and Phase Change Random-Access Memory (*PCRAM*) [13], [14].

1.2 Phase-Change Random Access Memory (*PCRAM*)

Chalcogenide-based *PCRAM* is one of the most promising non-volatile memory candidates for the next generation of portable electronics, due its excellent scalability [15]–[17], extremely high switching speed [18], and low-power operation [19].

1.2.1 Chalcogenide Glasses

Chalcogenide glasses are a class of materials, which contain Sulfur (S), Selenium (Se), and/or Tellurium (Te), or combinations thereof (shown in Figure 1.1). These materials are attracting much attention due to their potential use in Non-Volatile Memory (*NMV*) technology and the high demand for portable media, which use this type of memory.

14 IVA	15 VA	16 VIA	17 VIIA
6 12.011 C CARBON	7 14.007 N NITROGEN	8 15.999 O OXYGEN	9 18.998 F FLUORINE
14 28.086 Si SILICON	15 30.974 P PHOSPHORUS	16 32.065 S SULPHUR	17 35.453 Cl CHLORINE
32 72.64 Ge GERMANIUM	33 74.922 As ARSENIC	34 78.96 Se SELENIUM	35 79.904 Br BROMINE
50 118.71 Sn TIN	51 121.76 Sb ANTIMONY	52 127.60 Te TELLURIUM	53 126.90 I IODINE
82 207.2 Pb LEAD	83 208.98 Bi BISMUTH	84 (209) Po POLONIUM	85 (210) At ASTATINE

Figure 1.1 Chalcogenide glass materials are alloys with an element from group VI of the periodic table. Chalcogenic Elements marked in square.

The conduction characteristic of chalcogenide glasses, meaning the reversible change in electrical resistivity upon a change in the phase of the chalcogenide glass material, was first published in 1968 by Stanford Ovshinsky using a 500 nm thick film composed of Tellurium (Te), Arsenic (As), Silicon (Si), and Germanium (Ge) [20], laying the path for future development for applications such as Phase-Change Random Access Memory (*PCRAM*). *PCRAM* is a resistance-based *NVM* technology, where the state of the memory bit is defined by the resistance of the chalcogenide glass material; the resistance state depends on the microstructure of the material [18]. The most commonly

used chalcogenide material for *PCRAM* is $Ge_2Sb_2Te_5$ (or *GST*) [21]. In this study, *GST* was used as the chalcogenide material. A typical cross-section of a *GST* phase-change device (or cell) is shown in Figure 1.2. Although there are a number of possible geometries for *PCRAM* cells [22], the geometry that was used is the "mushroom" structure shown (amorphous region marked by the * in Figure 1.2, left) [22].

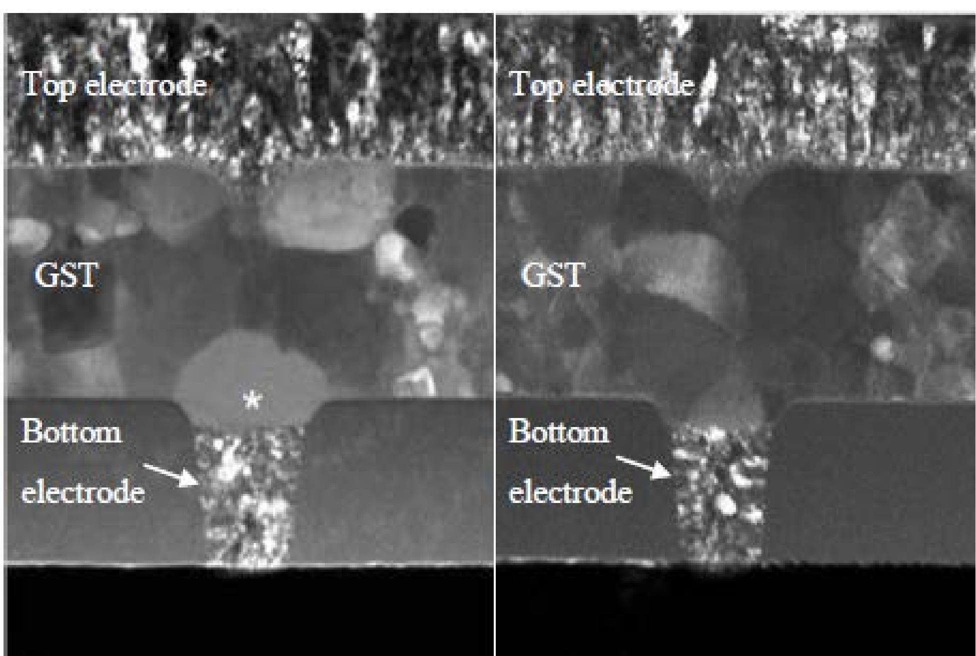

Figure 1.2 Representation of a cross-section for a *GST* phase change device. Left: After RESET (mushroom structure); Right: After SET. Amorphous *GST* region marked by * in RESET image (LEFT image). TEM images courtesy of Micron Technology.

<u>1.2.2 Operation</u>

In the mushroom structure geometry (shown in Figure 1.2), the phase-change material (*GST*) is sandwiched between two electrodes: 1) a bottom electrode, often called a "heater element" typically made of TiN, Tungsten (W), or a silicide, to lower the current needed to program the phase-change material and improve heating efficiency [23], and 2) a top electrode, which typically has a larger contact area than the bottom electrode [21]. Due to the contact area asymmetry, the current is confined near the bottom

electrode. The small size of the bottom electrode is needed to promote the region around the bottom electrode to reach the highest temperature during operation in order to change the phase of the material. This region is sometimes referred to as the "active" or "melt" region of the *PCRAM* cell. Information is stored by exploiting two different solid-state phases (namely, the amorphous and the crystalline phase) of a chalcogenide alloy, which have different electrical resistivity. The amorphous (high-resistance) phase of the chalcogenide glass has a disordered microstructure with little to no atomic order, and as a result the resistance range of the amorphous phase is between 1–10 MΩ, which is often 2 orders of magnitude higher than the crystalline (low-resistance) phase of the chalcogenide glass, which has a resistance range between 10 -100 kΩ [22]. The change in the solid-state phase from the amorphous phase to the crystalline phase is based on the thermally-induced change in the active region of the chalcogenide *GST* layer [22], [24].

The phase-change of the *PCRAM* device to a highly resistive amorphous chalcogenide material is accomplished when a voltage higher than the threshold voltage (V_{th}) is applied across the bit, driving a brief, intense current pulse through the device. The RESET and SET pulses mentioned are illustrated in Figure 1.3, as a function of electrical current (I) and Time, with dotted lines representing the RESET and SET regions [25]. When the RESET pulse is applied, this raises the temperature of the chalcogenide material above the melting temperature (i.e., I_{melt} which corresponds to $T \sim 600°C$ for the *GST* alloy, shown in Figure 1.3) through Joule heating [26]. Once the melting temperature is achieved, the rapidly falling edge of the current pulse quenches the temperature of the material. This places the chalcogenide film in an amorphous (high-resistance) state, which is a "RESET" state for the device.

The RESET operation creates the amorphous dome-shaped region (marked by the * in Figure 1.2, left) with a resistivity several orders of magnitude higher than that of the poly-crystalline region of the device, placing the device in a RESET state. To "SET" the device or recover the crystalline phase, an extended (longer duration: 100 ns – 1 μs range), low intensity, current pulse is applied to the phase-change material heating the device above the glass transition temperature (I_{cry}, shown in Figure 1.3). The device is then cooled more slowly, changing the phase of the material to a poly-crystalline (low-resistance) state [27]. It should be noted that the crystalline phase or SET state can also be achieved by annealing the amorphous *GST* at elevated temperatures. This is accomplished through thermally-accelerated nucleation and/or growth of crystalline grains during the sub-melting annealing [18], which will be discussed further in Chapter 2.

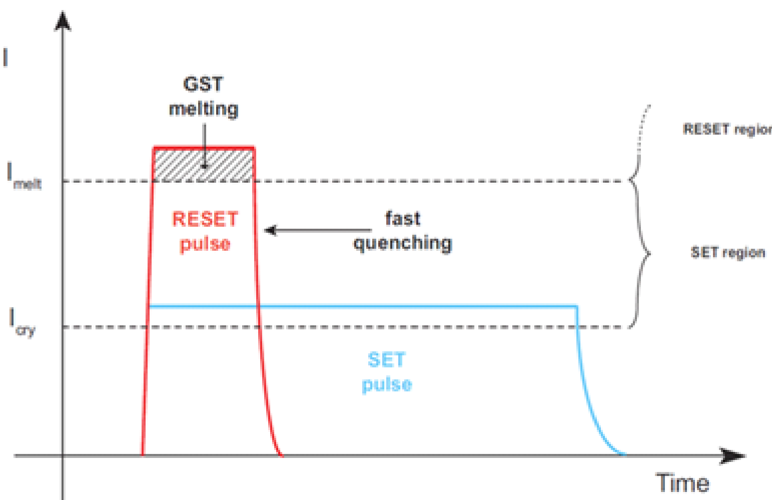

Figure 1.3 Diagram of standard current pulses for *PCRAM* programming during writing (SET or logic 1) and Erasing (RESET or logic 0). I_{melt} refers to the current pulse amplitude needed to achieve the melting temperature and I_{cry} refers to current pulse amplitude where the crystallization temperature occurs or the glass transition temperature [25].

Finally, to READ the state of the bit, a predetermined READ voltage is applied to the cell; and the current flowing through the device, referred to as the READ current, is sensed (current sensing approach). The READ voltage must be low enough to avoid unintentional modifications of the cell contents due to unintended heating during readout.

During the SET operation, there is a point where the resistance of the phase-change material drops suddenly. This phenomenon takes place at the threshold voltage (V_{th}) of the material and is often referred to as "snap-back," "threshold switching," or "switching effect" of the device, due to the change in the current-voltage (*I-V)* trace. Figure 1.4 shows a typical *I-V* trace for the SET and RESET state. The *I-V* curve of the cell in its amorphous (or RESET) state shows an S-shaped behavior at about 1.2 V, which is the V_{th} for the measured device or the point where the conductivity of the cell changes and becomes comparable to that of the SET state. This effect is due to the threshold switching phenomenon [20], [21], [24], which consists of a sudden drop in the amorphous chalcogenide resistivity as the voltage reaches the threshold voltage (V_{th}) or equivalently when the current flowing through the cell exceeds the threshold current value (I_{th}). From an application point of view, threshold switching plays an essential role in the operation and performance of *PCRAM* cells; V_{th} defines the boundary between the voltage ranges for the READ and write (SET/RESET) pulse amplitudes in the memory cell [22]. Threshold switching is attributed to a voltage-current instability due to electronic excitation at high electric fields [28]–[32]. It should be noted that in some chalcogenide glasses, including *GST*, the threshold switching usually results in a transition from the amorphous to crystalline phase, while for other materials the switching process leaves the phase unaltered [33]. This difference can be explained by

the Joule heating, resulting from the large current increase at switching, which for sufficiently long electrical pulses can contribute to the transition to the crystalline phase for glasses with low crystalline point [22],[34].

The programming operation of the *PCRAM* cell takes place in the high current regime of the SET and RESET trace, which is the location in Figure 1.4 where the amorphous (RESET) and crystalline (SET) *I-V* trace characteristics are almost indistinguishable (*I* = ~300 µA) [35].

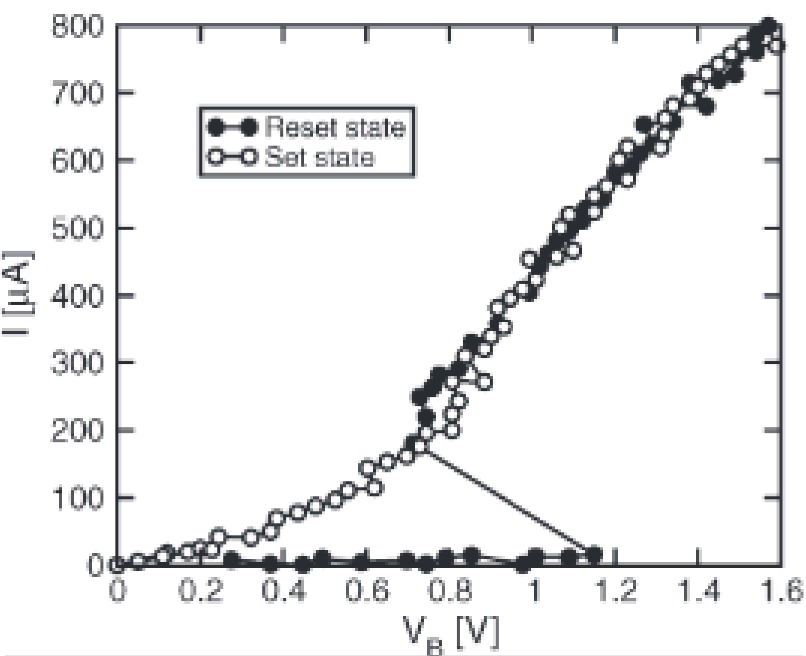

Figure 1.4 Measured *I-V* curves for the crystalline (SET state) and amorphous (RESET state) chalcogenide [35].

1.2.3 Technology Development

The operation properties of *PCRAM* technology provide the characteristics to allow a drop-in replacement in a broad base of applications, while providing significant added value in: 1) wireless systems; 2) embedded applications (as a Flash replacement); 3) solid state storage subsystem; and 4) computing platforms [36]. Moreover, as has been

mentioned in Section 1.2, *PCRAM* offers the possibility of improved scalability; the current state of the art is at the 20 nm technology node (cell half-pitch, F = 20 nm) with a cell size of 4 F^2 (i.e., cell size = 4*(20 nm)^2), as shown in Figure 1.5. Technology nodes are used to define the ground rules of device fabrication processes, governed by the smallest feature printed in a repetitive array [37].

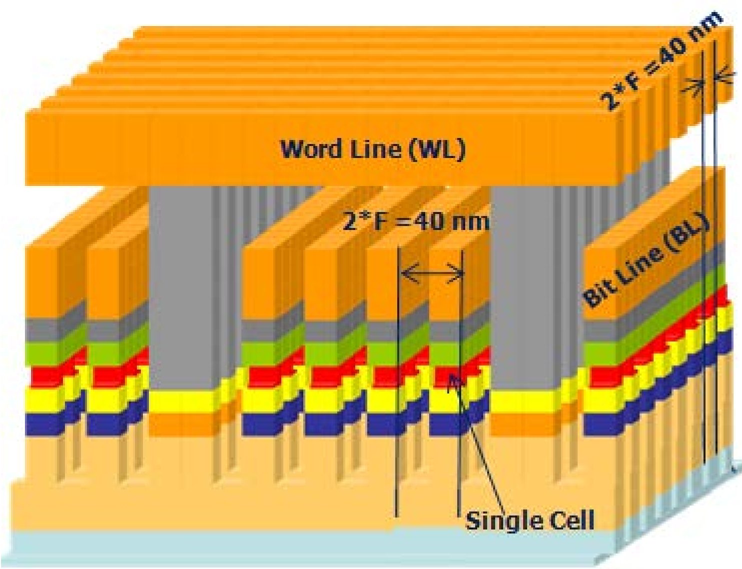

Figure 1.5 Schematic of a memory cell array showing the cell size as 4 F^2. Schematic image courtesy of Micron Technology.

When comparing the technology node of *PCRAM* to Flash, *FeRAM*, and/or *STT-RAM* in Table 1.1, it is apparent that *PCRAM* shows a significant improvement in terms of scaling (or shrinking) of the device. Furthermore, it should be noted that *PCRAM* has much lower programming read and write voltages than the other technologies, not to mention "direct overwriting" capabilities, meaning that the programming operation can be completed in one pass without having to erase the existing state of the bit first; *NOR* and *NAND* Flash do not have direct overwriting capabilities. Finally, for *PCRAM*, a reduced number of photo-lithography levels or "mask steps" are needed, due to fewer

device manufacturing or processing steps when compared to *NAND* and *NOR*. Moreover, the processing flow for *PCRAM* does not require the integration of ferroelectric and/or magnetic materials with the *CMOS* process flow, unlike *FeRAM* and *STT-RAM*.

Table 1.1 Comparison of non-volatile memories characteristics [8], [10], [38]–[40].

Metric	PCRAM	Flash NOR	Flash NAND	FeRAM	STT-RAM
Endurance(cycles)	$1x10^{12}$	$1x10^{5}$	$1x10^{5}$	$1x10^{16}$	$1x10^{14}$
Added mask steps	3-4	6-8	6-8	2	4
Direct Overwriting	Yes	No	No	Yes	Yes
Programming energy	Medium	High	Medium/High	Low	Medium
Read Voltage	0.4 V	2 V	5 V	1.5 V	3.3 V
Write Voltage	1 V	12 V	18 V	1.5 V	3.3 V
Technology	**20 nm**	**45 nm**	**19 nm**	**130 nm**	**54 nm**
Cell Size	**4 F^2**	**12 F^2**	**3b/cell**	**14.9 F^2**	**14 F^2**
Array Size	**8 Gb**	**1 Gb**	**128 Gb**	**128 Mb**	**64 Mb**
Write Speed	**~150 nsec**	**5 Mbps**	**18 Mbps**	**83 nsec**	**<15 nsec**
Read Speed	**100 nsec**	**80 ns**	**400 Mbps**	**43 nsec**	**< 20 nsec**
Vcc	**1.8 V**	**1.8 V**	**2.7-3.6 V**	**1.9 V**	**1.8 V**
Micrograph (not to scale)					
Note: Items in bold are State of the Art based on search from ISSCC and IEDM.	**ISSCC 2012 [39]**	**ISSCC 2008 [38]**	**ISSCC 2012 [40]**	**ISSCC 2009 [10]**	**IEDM 2010 [8]**

Among the companies that have invested in *PCRAM* technology, Micron is the first to supply high-volume availability of a 45 nm technology node, 1-Gigabit (Gb) *LPDDR2*, with an effective cell size of 5.5 F^2 [36], [41], [42], in a multichip package. The technology development road map for *PCRAM* is reported in Figure 1.6, showing the aggressive technology scaling with each generation between Samsung and Micron (formally Numonyx, STMicroelectronics).

The 180 nm technology node has been used as a vehicle to demonstrate and prove the viability of the technology, which for STMicroelectronics/Numonyx led to the development of both the 90 nm technology (the "Alverstone" technology) and on to the 45 nm technology, which is now commercialized by Micron [42].

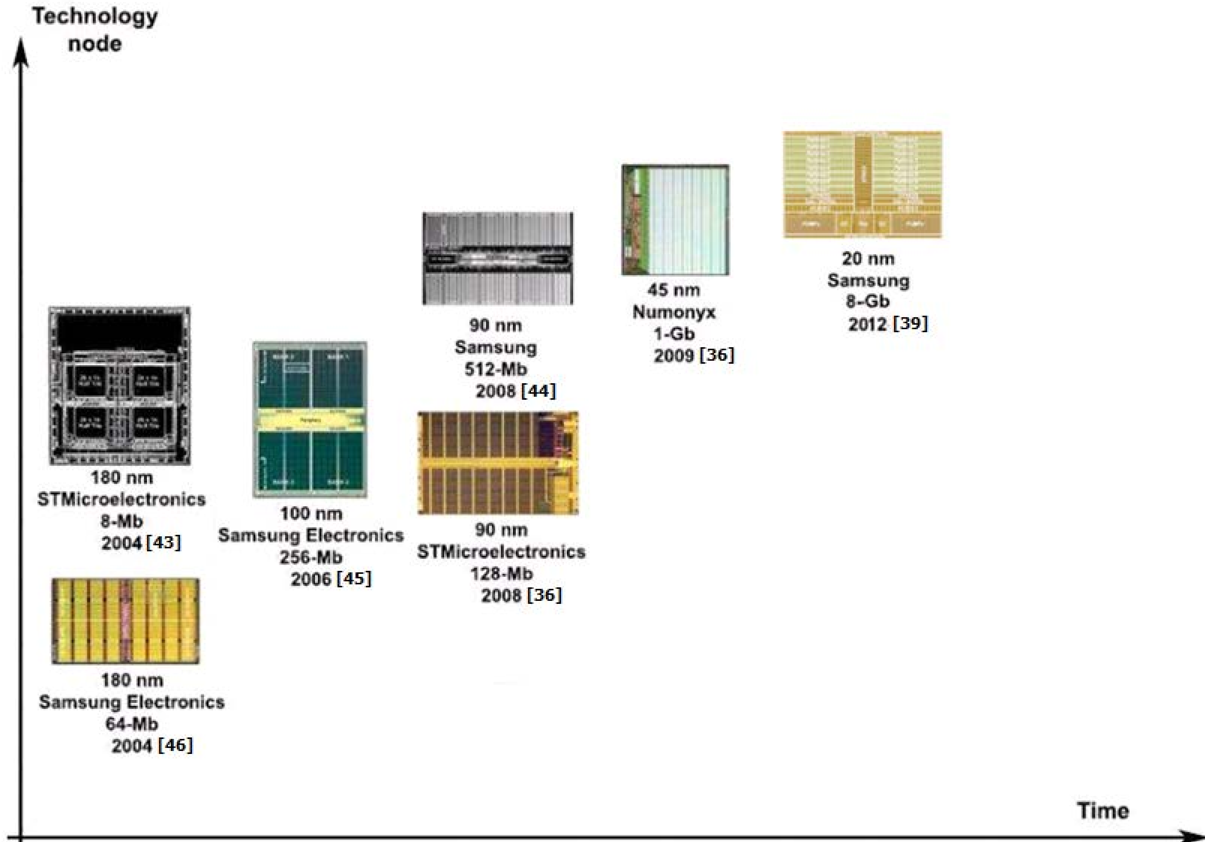

Figure 1.6 Technology development roadmap for *PCRAM* [36], [43]–[46].

1.3 Materials

In this study, 45 nm 1-Gigabit (*Gb*) *LPDDR2 PCRAM* engineering devices fabricated at Micron were used in determining the optimal pulse conditions and in developing the reliability prediction method, which will be discussed further in Chapter 2. Conceptually, the structure of the Micron 45 nm *PCRAM* cell architecture is simple, consisting of a top electrode, memory layer (*GST*), and the heater (as shown in Figure 1.7), which form the storage element.

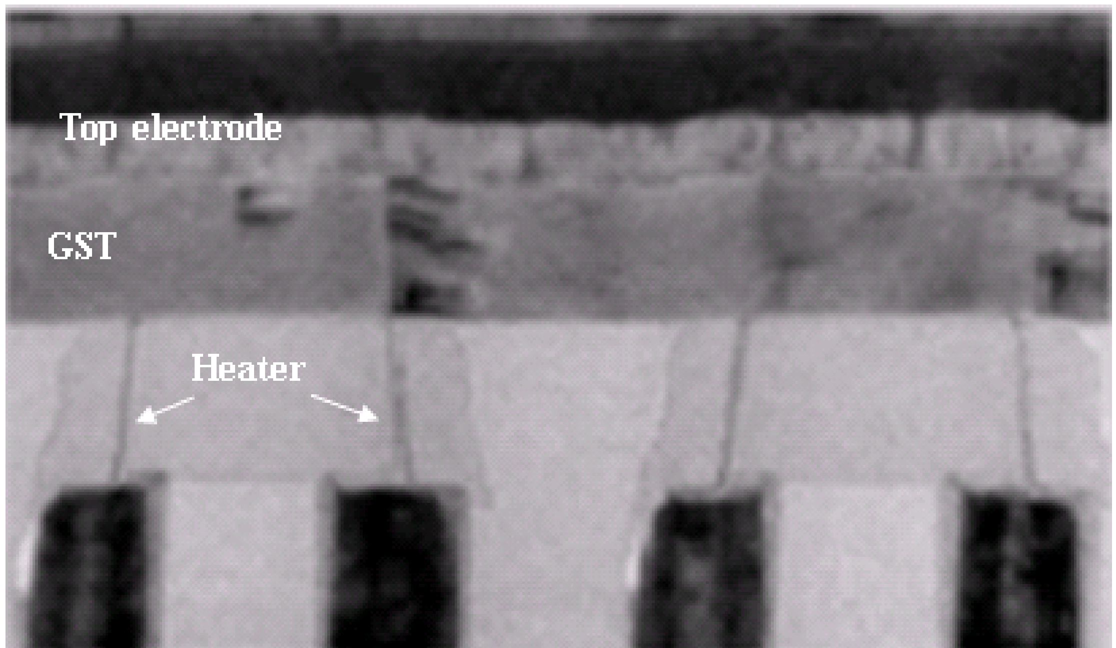

Figure 1.7 Representation of a cross-section of the Micron 45 nm storage element architecture [36].

Since the phase change material (or memory layer) in the storage element is programmable with the application of an applied electrical pulse, when programming an array of devices, a selecting device is required in order to decoded the correct storage element inside the 1-Gb array of devices [22]. Two primary solutions have been investigated for high-volume manufacturing: 1) vertical Bipolar Junction Transistor (*BJT*) and 2) planar metal-oxide-semiconductor field effect transistor (*MOSFET*) [22],[42], shown in Figure 1.8. Considering that the aim of process integration is to build a compact and efficient *PCRAM* storage element coupled with its selector, the *BJT*/Diode was considered to be an innovative solution for high density, high performance applications.

Planar *MOSFET* Selector **Vertical *BJT* Selector**

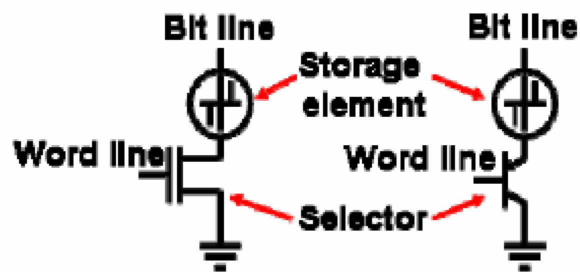

Figure 1.8 Schematic Depiction Single Transistor Per *PCRAM* Cell Structure: Left: Planar Metal-Oxide Semiconductor Field Effect Transistor (*MOSFET*), Selecting Device; Right: Vertical Bipolar Junction Transistor (*BJT*), Selecting Device [42].

A comparison of the process complexity, size, organization, application, and the schematic of the *MOSFET* vs. *BJT*/Diode is shown in Figure 1.9. In this comparison, one can see that the cell size of the *MOSFET* is ~20 F^2, while the *BJT*/Diode cell size was reduced to ~5 F^2. As a result of the smaller cell size, the *BJT*/Diode-selector has been chosen in the 45 nm commercialized *PCRAM* part, which allows for higher performance and density applications [21], [42].

	MOSFET	**BJT/Diode**
Process Complexity	No mask overhead for the selector	Dedicated steps for the p-n-p junction integration
Cell Size	Larger (~20F^2)	Smaller (~5F^2)
Memory Array Organization	Conventional	Innovative
Application	Embedded memory	High density, high performance
Schematic Cell Structure Cross-section	BL, GND, WL, n+, n+, STI, p-substrate	WL, BL, p+, n+, n-well, p-substrate

Figure 1.9 Comparison of the *MOSFET* and *BJT*/Diode selected *PCRAM* cell [42].

The *PCRAM* architecture was originally developed considering the small cell size requirements, the process cost, and the high performance characteristics, with the focus of obtaining fast random access-time typical of *NOR* Flash applications [22], [47]–[49]. The standard "µTrench" storage element fabrication steps proposed for the 90 nm technology platform is shown in Figure 1.10. For the standard "µTrench" storage element, one base-contact of the *BJT*/Diode is used for every emitter [36].

The active storage region is achieved at the intersection between the vertical thin-film metallic layer or heater (which is deposited inside an opening on a Tungsten (W) plug), and a thin layer of chalcogenide material (*GST*) capped with a TiN barrier (deposited inside a sub-lithographic trench or "µTrench"), as shown in Figure 1.10 [22],[42].

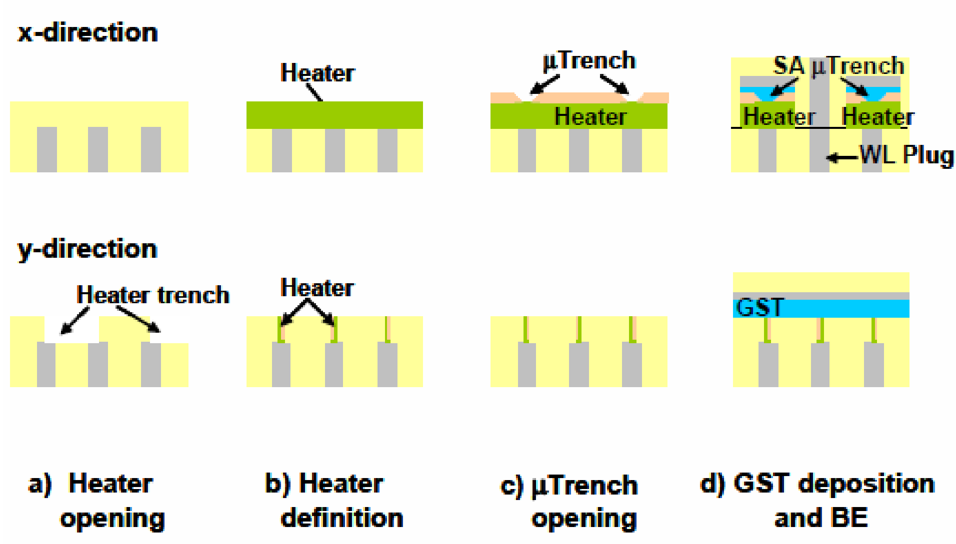

Figure 1.10 Schematic of the Self-aligned "µTrench" fabrication steps [42].

With the enablement of a working and reliable storage element, ongoing development led to a more effective cell using one base contact for every four emitters [36]. This approach has been adopted on the 45 nm technology to achieve a cell size of

5.5 F^2, leading to the design of the 1-Gb *PCRAM* product and "Wall" storage element, shown in Figure 1.11 [36].

Process module optimization, in particular an innovative double Shallow-Trench Isolation (*STI*) approach (used for isolation between adjacent emitters) and material improvements, have permitted the evolution of the cell from the "μTrench" (Figure 1.10) to the "Wall" structure (Figure 1.11), simplifying the overall storage element process integration and maintaining a very controlled low RESET current [36], [42]. The reliability results (discussed further in Chapter 2), using the new "Wall" cell have been very positive both in terms of retention and endurance; these results show that the technology is able to meet the reliability expectations for 90 nm, 45 nm, and future scaled technology nodes [36], [42].

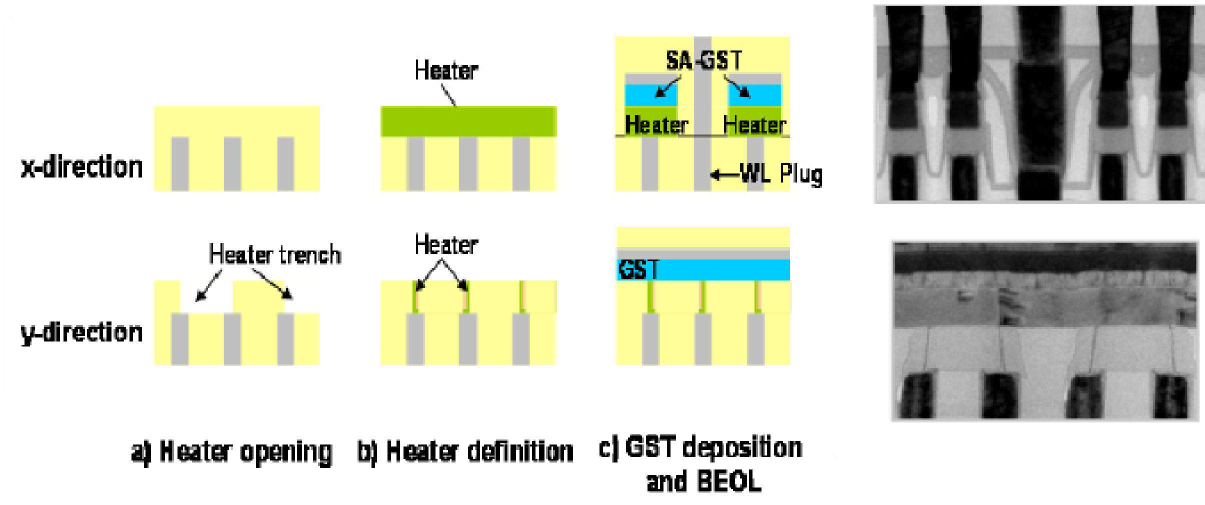

Figure 1.11 Schematic of the "Wall" storage element and related cross-sections [36].

1.4 Conclusions

In view of the need for new types of non-volatile memory (*NVM)* and with an understanding of *PCRAM* and where it fits when compared to other non-volatile

emerging memories, we now move into the investigation of *PCRAM* reliability presented in this dissertation. In Chapter 2, common methods used for reliability prediction will be reviewed. These methods lead to the objective of this dissertation which is to develop a reliability prediction method based on the pulse conditions, temperature, cycling data, and Bit Error Rate (*BER*). This new reliability prediction method presented in Chapter 2 is able to model and predict a single combination of temperature and pulse conditions, giving the lowest Bit Error Rate (BER), on a 1-Gigabit (Gb) array of experimental *PCRAM* devices, using the Micron/Numonyx *PCRAM* 45 nm cell architecture. In the following chapter (Chapter 3), an overview of the testing method, equipment used, and theory supporting the new reliability method will be covered. In Chapter 4, the Design of Experiments (DOEs) used for in modeling of the optimal pulse conditions are presented. Finally, in Chapter 5, the DOE used for the Bit Error Rate (*BER*) model is presented.

CHAPTER 2: RELIABILITY

2.1 Reliability and Failure Rate

Reliability is one of the most important factors used to determine if a device fulfills its required functions for the prescribed period under the conditions for which it was designed. Each device has a lifetime, which is the length of time that the device works as desired. The reliability indicates the probability for functioning correctly without failure until time (t_{life}), which is used as a random variable for the lifetime of a device in Equation 2.1. If the mission time ($t_{mission}$) of the device is not specified, the reliability of the device becomes a real-value function for $t_{mission}$. It should be noted that $t_{mission}$ is not a random variable. Then, the reliability function, $R(t_{mission})$, which is the probability that t_{life} is greater than $t_{mission}$, can be formulated as follows:

$$R(t_{mission}) = \Pr(t_{life} > t_{mission}) = \int_{t}^{\infty} f(\theta)d\theta, \quad (2.1)$$

where $f(\theta)$ is the probability density function (*pdf*) of t_{life} with respect to operating time θ.

Failures are counted in calculating reliability. In semiconductor engineering, failures can be classified into types according to the failure source. The failure rate of a device is often expressed using what is called the "bathtub" curve as shown in the “Observed Failure Rate” curve of Figure 2.1. The bathtub curve takes into account the failure rate from the standpoint of time and classifies failures into three types according to the failure source: 1) early failures or, Decreasing Failure Rate (*DFR*), 2) Constant

Failure Rate (*CFR*), and 3) wear out failures or Increasing Failure Rate (*IFR*) [50]–[53]. It should be noted that the failure rate of semiconductors shows a gradual decreasing failure rate with increased time similar to the early "Infant Mortality" failure curve in Figure 2.1; hence, the longer a particular semiconductor device is used, the more stable it will be. However, two points must be considered regarding the service life of a device: 1) the *CFR* region, and 2) *IFR* region or the wear out of the device.

If a failure is caused by unrevealed manufacturing defects, it is classified as an early failure in the *DFR* region. Defects that do not materialize into yield losses can grow to failures during operation depending on the quantity of external and internal stresses [50], [52], [54]. These early failures are usually screened by accelerated life testing and burn-in [50]–[52].

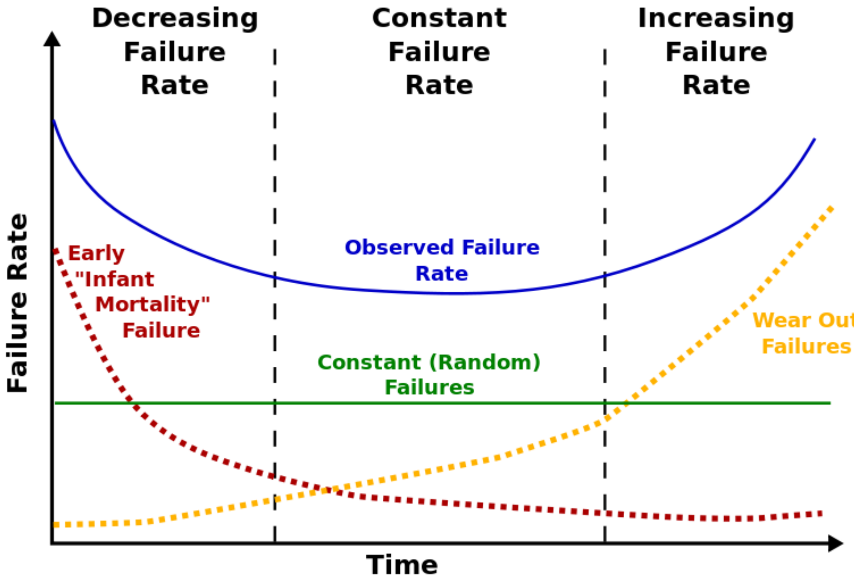

Figure 2.1 Typical "Bathtub" curve for semiconductor devices [55].

2.2 Accelerated Life Tests

Accelerated tests are typically used to find and identify potential failure mechanisms in semiconductor devices [50]. When performing accelerated tests for a

given failure mechanism, a common way of determining the presence of some stress (e.g., temperature cycling, electric field, current density) is through the acceleration factor. The mathematical relationship or equation commonly used for the acceleration factor due to changes in temperature for microcircuits and other semiconductor devices follows the format of the Arrhenius equation [50]. An example of the acceleration factor due to changes in temperature is shown in Equation 2.2:

$$A_T = \frac{\lambda_t}{\lambda_s} = \exp\left[\left(\frac{-E_a}{k}\right) * \left(\frac{1}{T_t} - \frac{1}{T_s}\right)\right], \tag{2.2}$$

where E_a is the activation energy (in electronvolts (eV)), k is Boltzmann's constant (8.62E-5 eV K^{-1}), T_t is the absolute temperature of the test (in Kelvin), T_s is the absolute temperature of the system (in Kelvin), λ_t is the failure rate at the test temperature, and λ_s is the failure rate at the system temperature. The acceleration factor can be calculated for electrical, mechanical, environmental, and other stresses when those stresses affect the reliability of a device [50]. With accelerated testing, caution should always be used since the relationship only holds if the failure rate is constant; however, very few practical situations exist in which the failure rate is truly constant. Nevertheless, the assumption of constant failure rate is still commonly used.

2.3 PCRAM Reliability

2.3.1 Design Constraints

When developing a memory chip used for high-performance applications, fast programming (SET/RESET) and READ times are necessary; however, consideration also needs to be taken into preserving data retention capabilities [22]. Among the failure mechanisms seen, retention loss of amorphous or RESET cells is most fundamental to

PCRAM [56], due to the instability of the amorphous *GST* [57], [22]. Early retention failures of the RESET bit have been related to pre-nucleation sites [56], which spur the rapid development of a conducting percolation path (shown in Figure 2.2), after a cell is RESET [18], [58].

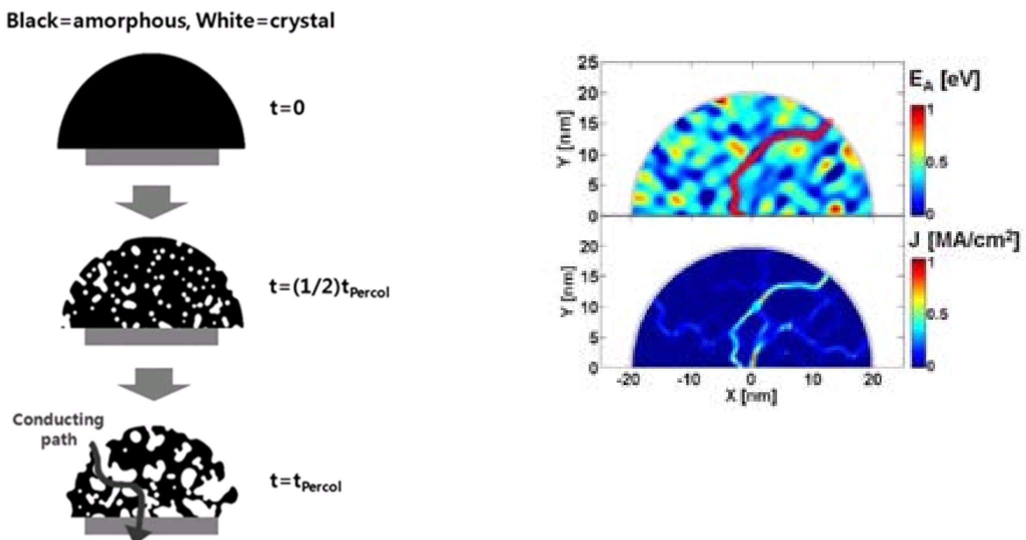

Figure 2.2 Conducting percolation path of *PCRAM*: left, simulation example of retention failure by the formation of conducting percolation path, from t=0 to the formation of the path [58]; right (top), percolation path highlighted (red), the channel is made by a continuous low-E_a path; right (bottom), corresponding current density profile, where the low-E_a path is the channel that brings the higher percentage of the total current [18].

When reviewing the retention of SET cells, it should be noted that insufficient pulse widths for the SET pulse can also cause a SET bit to be placed in a partial-RESET state, meaning that better retention capabilities implies longer SET programming pulses widths [22]. For example, in Figure 2.3, as the *PCRAM* cell transitions from the high resistance RESET state (amorphous phase) to the low resistance SET state (crystalline phase), one can see that complete crystallization is achieved with very long SET pulses widths (10 μsec), even at lower programming currents (~200 μA). However, as the pulse

width is reduced, the *GST* is not able to fully crystallize, resulting in a higher SET resistance, limiting the READ margin or reading window between the SET and RESET states [22], [59]. It should be noted that it is unacceptable for high-performance products to have a SET pulse width of 10 µsec, thus requiring shorter pulses to be used, resulting in a trade-off or compromise between the READ margin and shorter SET pulse widths and the possibility of a SET cell not being sensed correctly during the READ pulse.

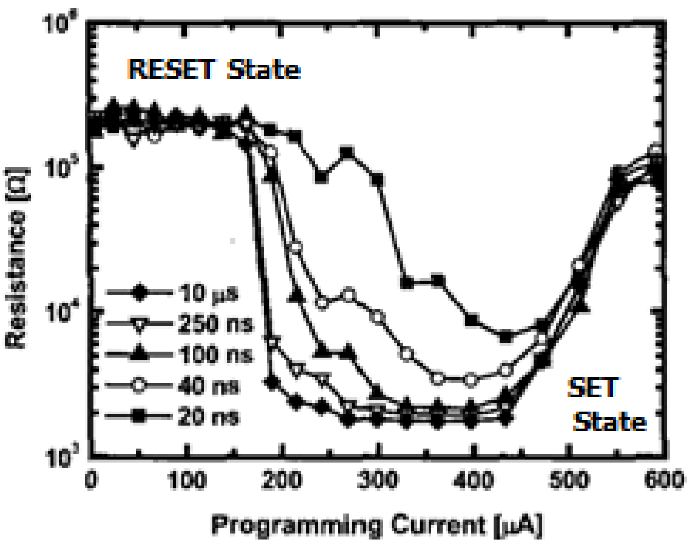

Figure 2.3 Programming curves of a *MOSFET*-selected *PCRAM* cell for different SET pulse widths [22],[59].

For the RESET pulse, shorter pulse widths have been found to be better, with advantages being seen in the *PCRAM* cell endurance, as shown in Figure 2.4. The theory behind the relationship between the cell endurance and the RESET pulse width is related to the overall time elapsed by the cell at higher temperatures during the RESET operation or the total energy dissipated inside the device [59]. It should be noted, that the experimental data in Figure 2.4 was fit using the power law.

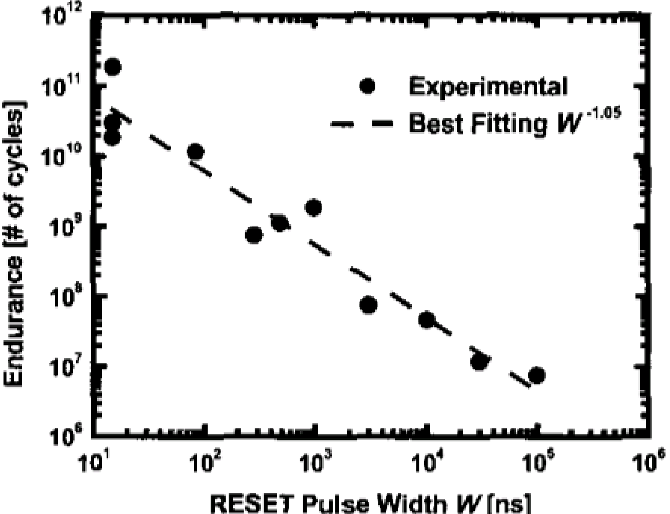

Figure 2.4 ***PCRAM* cell endurance as a function of the RESET pulse width [59].**

2.3.2 *PCRAM* Reliability Risks

The reliability risks of *PCRAM* can generally be grouped into three types: 1) data retention; 2) cycling endurance; and 3) data program and READ disturbs [56], [60], [61]. In Sections 2.3.2.1- 2.3.2.3, the standard methods used on the Micron 45 nm *PCRAM* devices to test the reliability risks are reviewed.

2.3.2.1 Data Retention

The major figure of merit for a non-volatile memory (*NVM*) is the capability of retaining the stored information for a long time period; the actual specification is 10 years [62]. To assess the *PCRAM* technology retention, accelerated bake testing on *PCRAM* cells are performed [56], [60]–[62]. However, these studies are generally limited in two ways: 1) to accelerate the data collection, the data is generally collected at very high temperatures (Temperatures > 180 °C), which requires a significant extrapolation when compared to the usable temperatures of the product and can affect the structure of the chalcogenide glass, and 2) the data collection is usually on a statistically small number of

cells, which likely does not expose possible defect failure modes that may be present/observed on a large array product [56]. For this reason, data retention needs to be examined at the part-per-million (*PPM*) level across a broad range of temperatures [56]. It should be noted that when the *PCRAM* device is subject to elevated temperatures, the resistance of the RESET *PCRAM* cell evolves with time as shown in Figure 2.5b [56], [57].

The behavior of the resistance shown in Figure 2.5 is mainly related to the unstable amorphous phase (RESET state) of the *PCRAM* cell, which is affected by two types of structural modifications: 1) the Structural Relaxation (*SR*) effect (Figure 2.5a), and 2) the crystallization process (Figure 2.5b) [57].

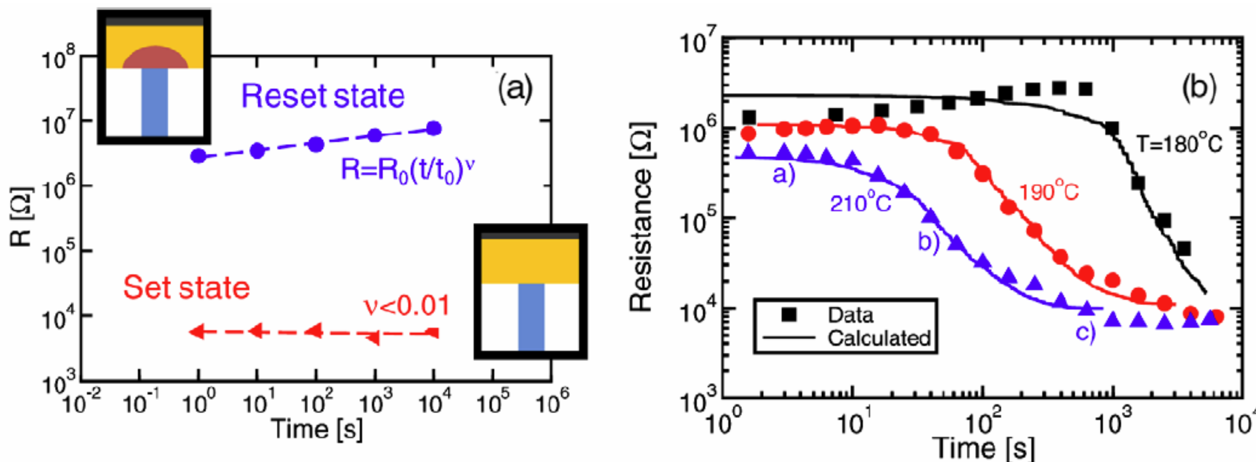

Figure 2.5 Resistance vs. time behavior during annealing, highlighting two possible structural phase modifications. (a) Structural relaxation at room temperature (T = 25 °C). (b) Drop in the RESET state cell resistance due to the nucleation and growth of a crystalline phase [57].

Both of these types of structural modifications affect resistance, which can lead to reliability issues for the *PCRAM* cell. In Figure 2.5b, the cell is initially RESET to ~1 MΩ, and the resistance is monitored at three different temperatures of 180 °C, 190 °C, and 210 °C [56]. Initially, the resistance in the cell increases due to resistance drift (a

phenomenon seen in amorphous chalcogenides) [56]; however, crystallization in the amorphous phase eventually sets in resulting in a drop in resistance and thereby, loss of data in the cell [56], [63].

The Structural Relaxation (*SR*) only affects the amorphous phase and has been explained by defect annihilation in the amorphous network, as shown in Figure 2.6 by the schematical annihilation process for a dangling bond as it transitions to a more stable state [57].

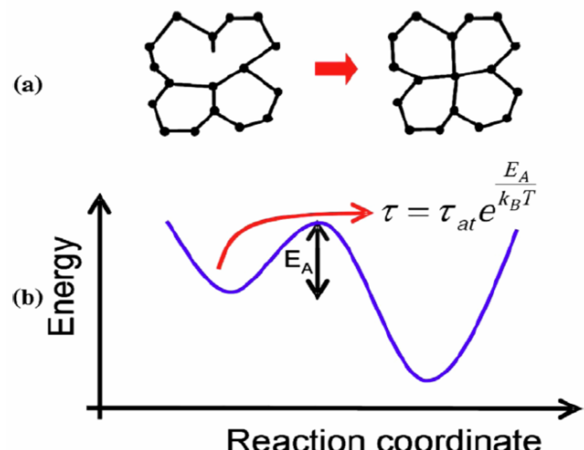

Figure 2.6 Schematic for the structural relaxation model in the amorphous chalcogenide material: (a) Structural defects (point defect such as a dangling bond); (b) The transition to the more stable state requires thermal excitation over an energy barrier E_A [57].

When multiple *PCRAM* cells are measured at the array level, a similar behavior is observed; however, the distribution of data retention failure times becomes broader. Figure 2.7 contains resistance distributions for an 512 Kb *PCRAM* array of RESET cells, which were run through successive high temperature bake steps [56]. The drift component is difficult to observe in this case due to the loss of measurement resolution above 1 MΩ; however, here a significant variation in % cell vs. resistance with increasing bake time across the distribution of cells can be observed. After the final bake, the

resistance of the cells ranges from essentially SET (Resistance < 10 kΩ) to fully RESET (Resistance=1 MΩ) [56], and the percentage of cells moving toward the SET resistance increases with increased bake time.

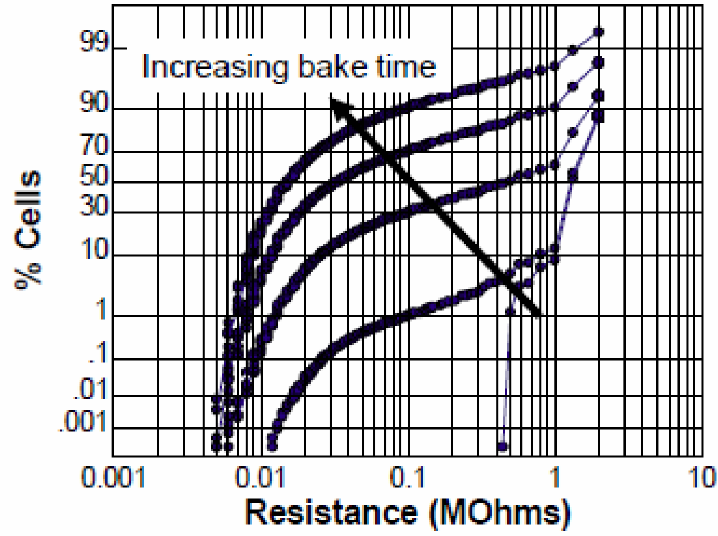

Figure 2.7 Resistance distributions of initially RESET *PCRAM* cells with increasing bake time at elevated temperature [56].

To estimate failure rates at product use conditions, an acceleration model for retention loss as a function of bake temperature is often used [56]. The experimental procedure consists of: 1) placing arrays of cells in a RESET state, and 2) baking the cells at elevated temperatures until retention loss is observed [56]. The *PCRAM* cells are considered fails once the resistance drops below a specified threshold (~100 KΩ), which is repeated at multiple temperatures on the same cells [56]. Temperatures between 125 °C and 160 °C have been found to be sufficient to describe the failure using this process [56]. Once the data is collected, it is then fit to the Arrhenius equation (Equation 2.3) to determine the data retention time [56].

$$t \propto exp\left[\frac{E_a}{kT}\right], \tag{2.3}$$

While more complex models have been developed to describe the crystallization process, the simple Arrhenius model is able to describe the failure process over a range of temperatures as shown in Figure 2.8 [56].

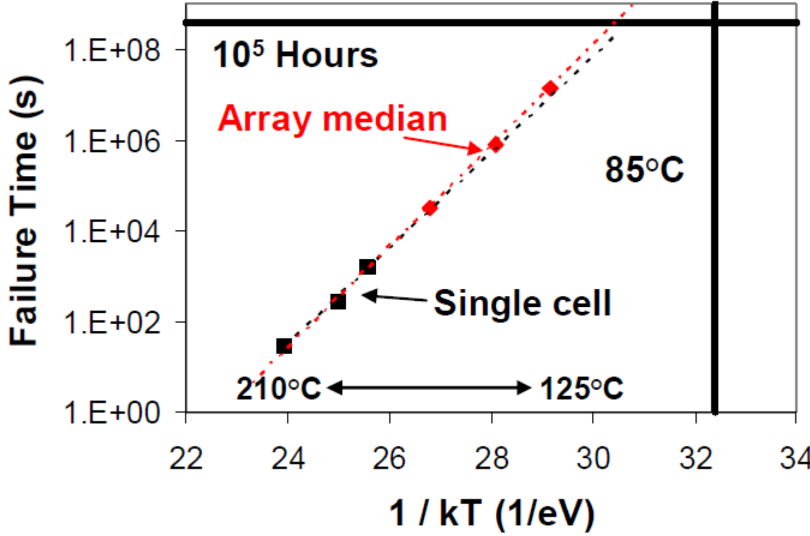

Figure 2.8 Arrhenius plot of Data Retention Failure Time vs. Temperature, including both array and single cell data [56].

2.3.2.2 Cycling Endurance

As with data retention, achieving high reliability for cycling endurance is very important and requires optimized device and pulse operation [60]. The cycling endurance tests can be conducted in three ways: 1) SET cycling, 2) RESET cycling, and 3) alternating SET and RESET cycling [61]. As shown in Figure 2.9, a resistance change of two orders of magnitude between the SET and the RESET state has been shown to be unchanged for more than 10^{11} programming cycles for a single *PCRAM* device with the alternating SET and RESET cycling [62].

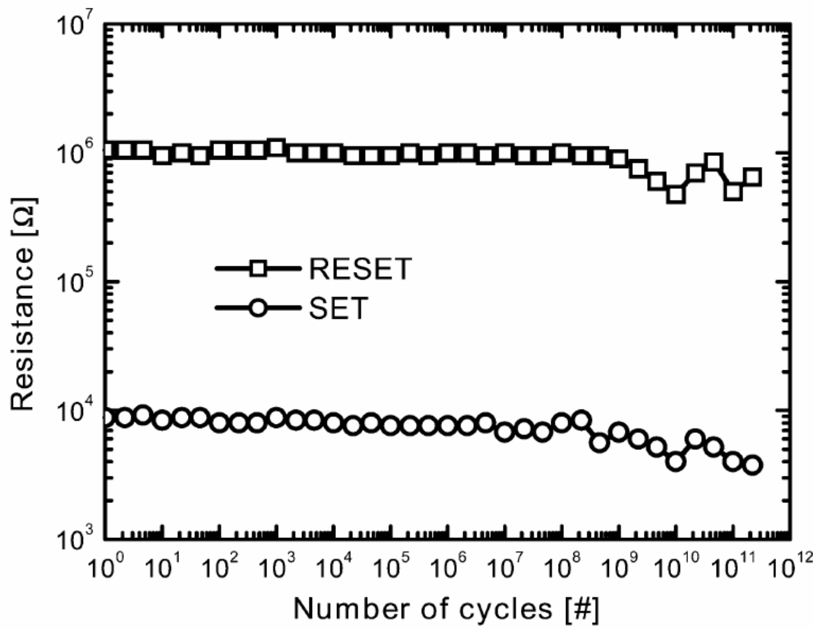

Figure 2.9 Cycling Endurance of a *PCRAM* cell [62].

When performing the cycling endurance tests, it should be noted that it is important that optimized programming pulses for SET and RESET be determined to ensure that the endurance of the device is maintained or improved [61]. It is also very important that the device is not over programmed as this can lead to early device failures such as: 1) "Stuck SET" or RESET fails, and 2) "Stuck RESET" or cell opens [60], [61]. In general, cells that get stuck in RESET after cycling show a higher threshold voltage, suggesting a failure mechanism related to the *GST* [60]. However, cells that get stuck in a SET state show a high resistance in the *I-V* curve at high current, suggesting that the failure mechanism is related to the heating element (or "heater element") [60].

2.3.2.3 Data Program and READ Disturbs

Since reading and programming device operations are based on the application of suitable voltage pulses, a major concern for every non-volatile memory technology is the ability of the cell to retain data when the writing and reading methods can cause various

disturb issues (related to the isolation between adjacent bits, shown in Figure 2.10), which can induce a transition from an amorphous state to a polycrystalline state in a *PCRAM* cell [62].

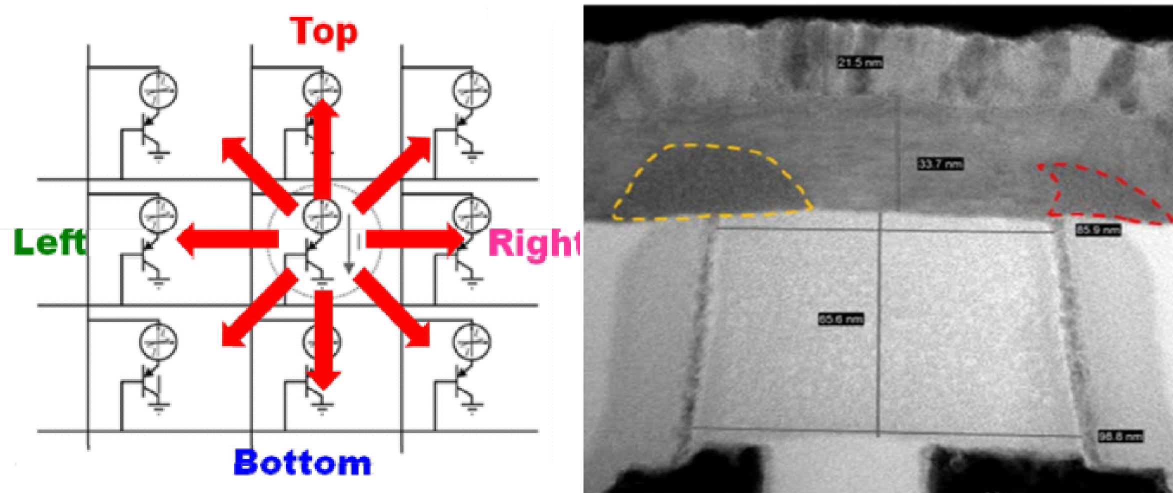

Figure 2.10 Left: Schematic description of the programming disturb phenomenon [62]; Right: TEM cross-section of aggressor (yellow) and disturbed cell (red); a portion of the amorphous *GST* dome is crystallized [64].

Disturbs are an intrinsic phenomena of the memory array [61]. There are two major disturb mechanisms: 1) thermal proximity disturb during programming, which are often referred to as "Data Programming Disturbs," and 2) READ disturbs [61], [62]. Data programming disturbs occur when reading or writing a certain *PCRAM* cell, which then can effect unwanted reading or writing at a nearest neighbor *PCRAM* cell, or at *PCRAM* cells connected to the same word-line/bit-line as shown in Figure 2.10 [62]. For the READ disturbs, this often involves the repetitive readout of a *PCRAM* cell in a RESET state, which eventually may cause a modification of its phase.

To test for data programming disturbs, the following tasks are usually performed: 1) all cells in the array are programmed into a RESET state, 2) selected cells in a checkerboard pattern across the array are then programmed up to 10^6 cycles, and 3) the

RESET state resistance before and after on the cells that were not cycled are then compared to determine the number of cells affected by the programming disturb [61].

2.3.3 Bit Error Rate and Array Reliability

In order to integrate *PCRAM* devices into large and yielding arrays, a large READ margin or "reading window" between the two memory logic states must exist and be maintained, with a probability of error or Bit Error Rate (*BER*) less than 10^{-6} (1 *PPM*) [65]. An example of the "reading window" can be seen in Figure 2.11 where a single-tile (4 Mb distributions) of SET and RESET resistances were collected on the µTrench *PCRAM* array [65]. While the SET distribution is log-normal with a resistance of 5 - 10 kΩ, the RESET distribution is only log-normal for resistances between 400 kΩ - 1 MΩ. Starting around the cell resistance of ~400 kΩ a pronounced tail or "RESET tail" is shown, which extends toward the low-resistance value of 20 kΩ and narrows the reading window between the SET and RESET states [65]. This RESET tail has been related to *PCRAM* cells that may have some abnormal material properties in or around the *GST* cell as a result of defects or processing issues that causes the *PCRAM* cell to behave differently to the applied electrical pulse [65]. It should be noted that this RESET tail and/or narrowing of the reading window is not a desirable characteristic; ideally the SET and RESET resistance distributions should have a large reading window between them so that the states of the cells can be easily distinguished. This means that out of all the *PCRAM* cells in a given memory array, the resistance of the cell with the highest SET resistance must be much lower than the resistance of the cell with the lowest RESET resistance.

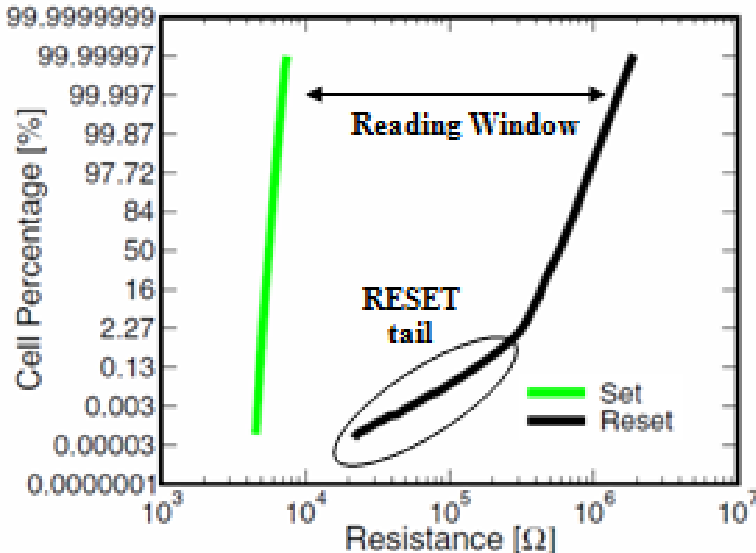

Figure 2.11 Array statistics for 4 Mb of SET and RESET resistances collected on a µ-trench *PCRAM* array [65].

Looking at the resistance distribution for the SET and RESET states by cell percentage of 4Mb from an array of *PCRAM* devices (shown in Figure 2.11), it is apparent that the single electrical programming pulse used for the RESET operation is able to RESET the majority of the *PCRAM* cells. However, for the anomalous or abnormal cells (within the lower 2.27% cell percentage), a different RESET pulse may be required to increase the RESET state resistance of these cells and improve the reading window between the SET and RESET states [65]. It has been found that an improvement of the RESET tail resistance distribution can be obtained by optimizing the RESET programming operation with a faster quenching time (t_Q) on the RESET electrical pulse as shown in Figure 2.12 and Figure 2.13, where t_Q is varied from a 60 ns RESET pulse width down to 20 ns [65].

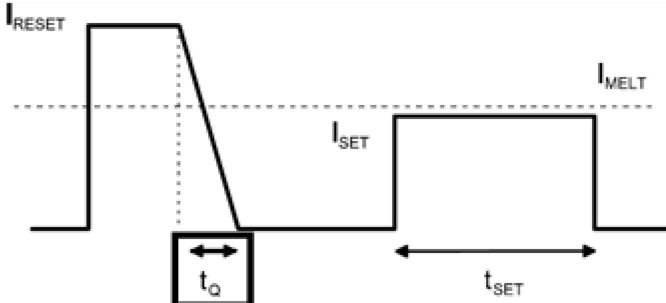

Figure 2.12 RESET and SET current pulses and significant parameters (highlighting t_Q or the quench time) [66].

With faster quenching time for the RESET pulse, the RESET tail becomes less apparent, meaning that the programming characteristics of the anomalous cells are now aligned with the intrinsic cell. This suggests that a faster quenching programming pulse is preventing the spontaneous crystallization of the *PCRAM* chalcogenide material, helping maintain the amorphous disordered state and high RESET resistance value [65].

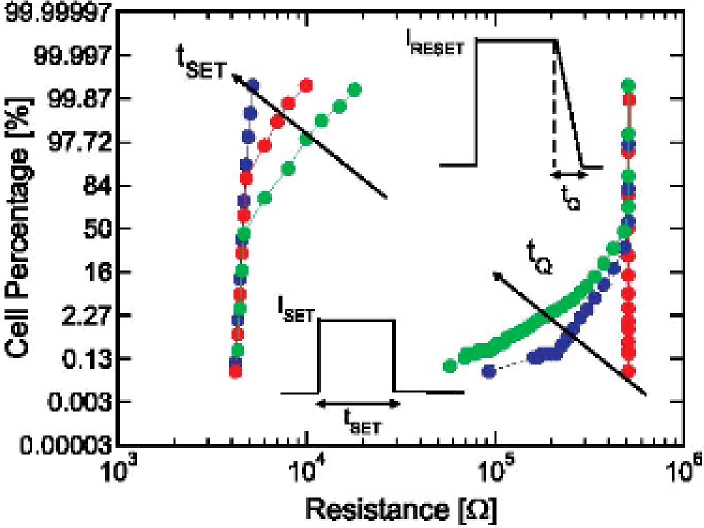

Figure 2.13 Resistance distribution improvements: RESET achieved with a faster quenching of the RESET pulse (Green: longer quench time; Orange: Short shorter quench time); SET achieved with longer pulse (Green: Short pulse; Blue: long pulse) [65], [66].

From a *PCRAM* reliability viewpoint, the characterization and understanding of the statistical spread of reliability parameters, such as the crystallization time and its

activation energy are extremely important [67]. Single-cell characterization only allows for the modeling of the intrinsic cell reliability with no insight into the reliability behavior of large arrays. The correlation between single cell performance and array performance still needs to be better understood. For example, a recent study was completed that compared the cumulative distribution of a single cell and array of cells (shown in Figure 2.14) [67]. In this comparison, two distributions of the time to SET (t^*_{set}), which was listed as the SET pulse-width required to reduce the cell resistance below 0.1 MΩ, were reviewed for: 1) The "Cell" distribution, which is a collection of multiple pulses on the same single cell, and 2) the "Array" distribution, which was obtained from a single SET pulse applied to multiple cells within the same array [67].

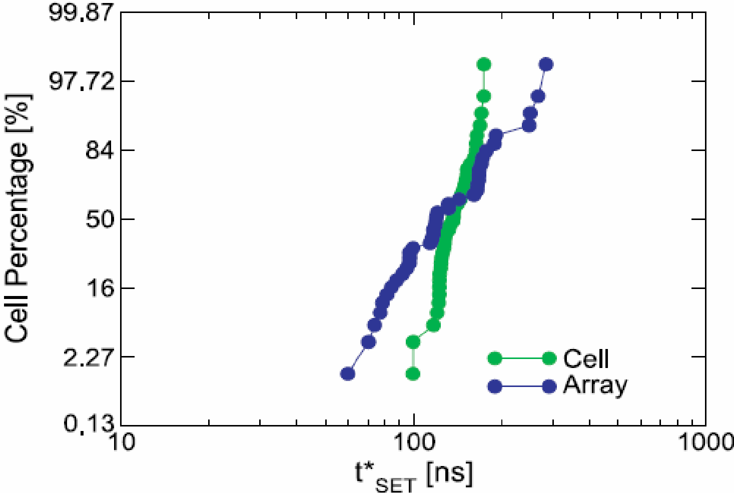

Figure 2.14 Cumulative distribution of measured set time t^*_{set} that is the pulse-width of the set pulse required for reducing the cell resistance below 10^5 Ω. A cell distribution (collected from many experiments on the same cell) and array distribution (collected from single experiments performed on many different cells within the array) are compared [67].

As shown in Figure 2.14, the single cell distribution displays a narrower spread than the array distribution. The statistical spread of the array data provides additional insight into the spread of crystallization parameters among the cells [67]. Moreover, it is

interesting to see how the single cell distribution supports the repeatability of the crystallization process for a single cell [67].

2.4 Failure Rate Prediction

Several different distributions can be used to model failure rate under appropriate circumstances such as the exponential, Weibull, and lognormal distributions. However, it should be noted that due to the window of operating conditions chosen in this research (to be defined in Chapter 3). The standard time-to-failure or lifetime prediction methods and distributions commonly used are not possible, since the 45 nm 1-Gb *PCRAM* chip is not sufficiently stressed to fail at the temperatures and voltages, which are used for determining the optimal pulse conditions for very long periods of time. For this reason, this reliability prediction method monitors the cell resistance distributions collected from sections of the *PCRAM* 1Gigabit (*Gb*) memory array and will predict a single combination of temperature and pulse conditions, giving the lowest Bit Error Rate (*BER*).

2.4.1 Exponential Distribution

An exponential distribution implies a constant failure rate. However, a constant rate does not occur if the product is insufficiently screened or improperly designed for reliability. It also does not occur if the product is past the bottom of the “bath tub” curve and into the wear-out phase. The exponential distribution is the least complex of all lifetime distribution models. The exponential distribution for the reliability function is defined in Equation 2.4,

$$R(t) = exp(-\lambda * t), \tag{2.4}$$

the cumulative distribution function (*CDF*) or failure distribution, is defined in Equation 2.5,

$$F(t) = 1 - \ exp(-\lambda * t), \tag{2.5}$$

and the probability distribution function (*PDF*), or the lifetime distribution model, which is obtained from the derivative (with respect to time) of the *CDF,* is defined in Equation 2.6,

$$f(t) = \lambda * exp(-\lambda * t), \tag{2.6}$$

where, t is time and λ is the failure rate or "hazard rate."

It should be noted that the mean time to failure (*MTTF*) of the exponential function is the inverse of the failure rate λ, which is defined in Equation 2.7.

$$MTTF \ = \ 1/\lambda, \tag{2.7}$$

In Figure 2.15-2.17, figures of the *CDF*, *PDF*, and hazard rate (λ), for the exponential distribution are shown.

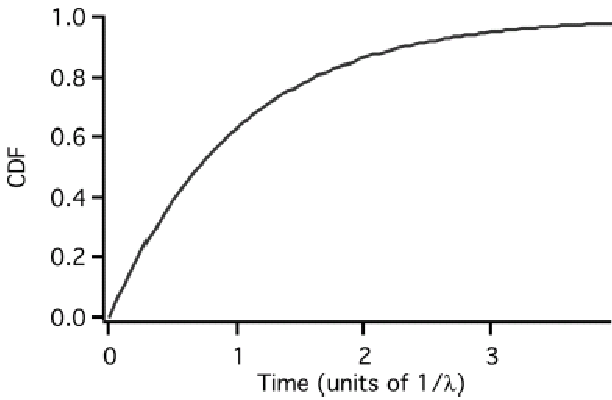

Figure 2.15 *CDF* or *F(t)* for exponential distribution [68].

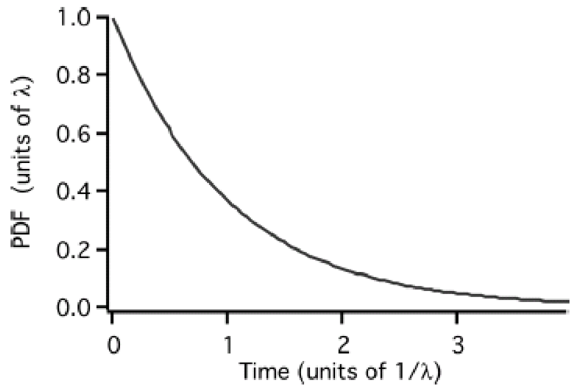

Figure 2.16 ***PDF* or *f(t)* for exponential distribution [68].**

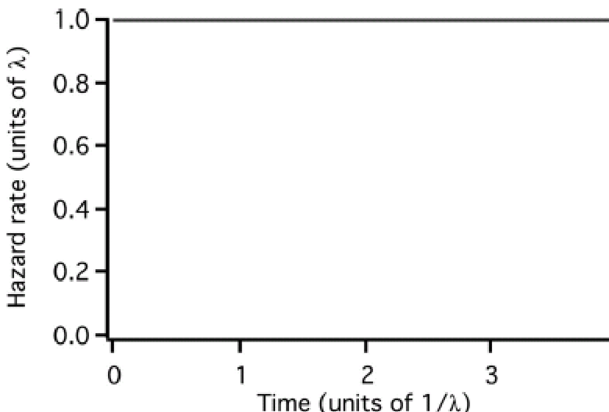

Figure 2.17 Exponential distribution hazard rate [68].

2.4.2 Weibull Distribution

A Weibull distribution can be used to model the "weakest link." The Weibull function can be expressed in multiple ways [68]. The two-parameter version derives a characteristic life, and a shape parameter, usually called β. The three-parameter version for Weibull retains the characteristic life and β, but adds a "delay time" corresponding to the time required to initiate defects. The difference between the two-parameter and three-parameter Weibull is whether or not failures start at time zero [68]. The equation of the three-parameter Weibull distribution shown in Equation 2.8 is the probability of survival between time zero and time t, or in other words the Weibull reliability function $R(t)$,

$$R(t) = \ exp\left[-\left(\frac{[t-\gamma]}{\alpha}\right)^{\beta}\right], \tag{2.8}$$

where, β is the shape parameter, γ is the location parameter, which is also referred to as the defect initiation time parameter, and α is the characteristic life or scale parameter [68]. If failures do not start at time zero, the defect initiation time parameter (also known as the location parameter) is zero, and the Weibull exponential expression is reduced to Equation 2.9,

$$R(t) = exp\left[-\left(\frac{t}{\alpha}\right)^{\beta}\right], \tag{2.9}$$

when $\beta = 1$, Equation 2.9 becomes the exponential model, with $\alpha = 1/\lambda$ or the *MTTF*. The *PDF* of the two parameter Weibull distribution is defined in Equation 2.10, a plot of the *PDF* is shown in Figure 2.19 for different values of β [68].

$$f(t) = \frac{\beta}{t}\left(\frac{t}{\alpha}\right)^{\beta} exp\left[-\left(\frac{t}{\alpha}\right)^{\beta}\right], \tag{2.10}$$

The *CDF* of the two-parameter Weibull is defined in Equation 2.11,

$$F(t) = 1 - exp\left[-\left(\frac{t}{\alpha}\right)^{\beta}\right], \tag{2.11}$$

which is shown in Figure 2.18, and its associated hazard function is shown in Figure 2.20.

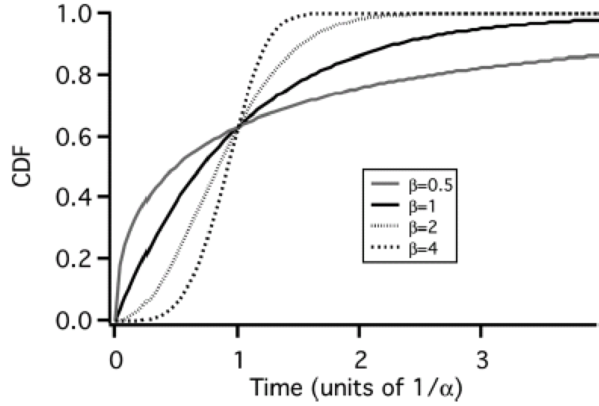

Figure 2.18 ***CDF* of Weibull function, varying β [68].**

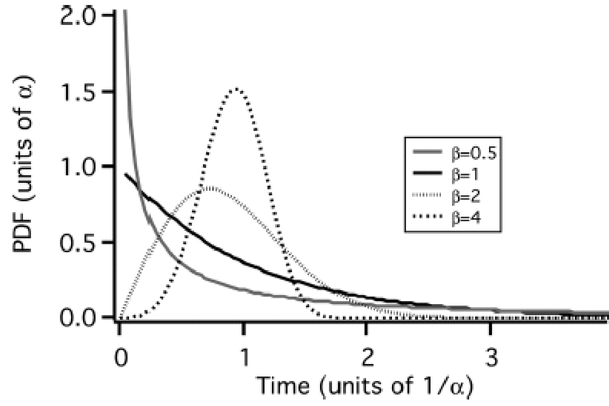

Figure 2.19 **Weibull function *PDF* in units of α, varying β [68].**

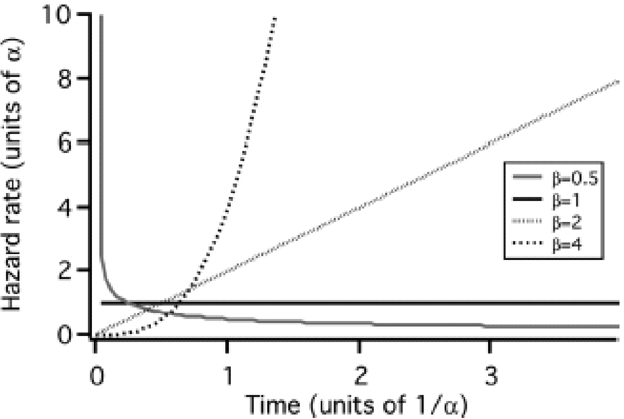

Figure 2.20 **Hazard rate for Weibull function, varying β [68].**

The cumulative failure rate of the two parameter Weibull model or so-called cumulative hazard rate is defined in Equation 2.12,

$$H(t) = \left(\frac{t}{\alpha}\right)^{\beta}, \tag{2.12}$$

with the instantaneous failure rate defined in Equation 2.13.

$$h(t) = \frac{\beta}{\alpha}\left(\frac{t}{\alpha}\right)^{\beta-1}, \tag{2.13}$$

2.4.3 Lognormal Distribution

The lognormal distribution is based on a normal distribution of failures vs. logarithm of time. The lognormal (also called Gaussian) distribution [68] for reliability function or survivor function is defined in Equation 2.14 as,

$$R(t) = 1 - \Phi\left(\frac{\ln(t) - \ln(t_{50})}{\sigma}\right), \tag{2.14}$$

where,

$$\Phi(z) = \frac{1}{2}\left[1 + Erf\left(\frac{z}{\sqrt{2}}\right)\right]. \tag{2.15}$$

The characteristic fitting parameters are the time to 50% cumulative failure (t_{50}) and sigma (σ), which is referred to as the shape parameter or the slope of the time to failure vs. the cumulative percent failure on a log scale and is a measure of the time dispersion of the failures [68]. The equation of the *CDF* for the lognormal distribution is shown in Equation 2.16.

$$F(t) = \Phi\left(\frac{\ln(t) - \ln(t_{50})}{\sigma}\right), \tag{2.16}$$

The probability distribution function (*PDF*), or the lifetime distribution model, is defined in Equation 2.17,

$$f(t) = \frac{1}{\sqrt{2\pi}t\sigma} * exp\left[-\frac{1}{2}\left(\frac{\ln(t) - \ln(t_{50})}{\sigma}\right)^2\right], \tag{2.17}$$

In Figure 2.21-2.23, figures of the *CDF*, *PDF*, and hazard rate, for the lognormal distribution are shown.

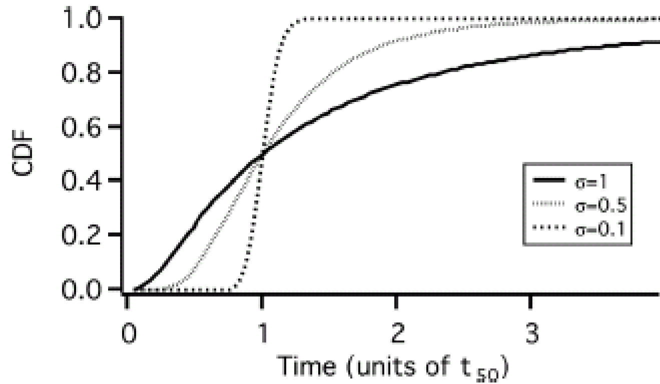

Figure 2.21 ***CDF*** **of lognormal function with varying σ [68].**

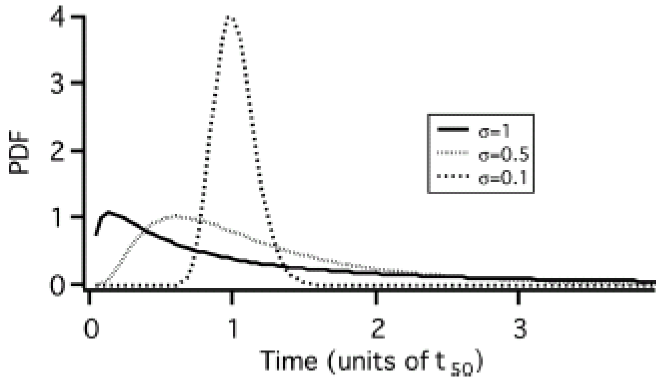

Figure 2.22 ***PDF*** **of lognormal function with varying σ [68].**

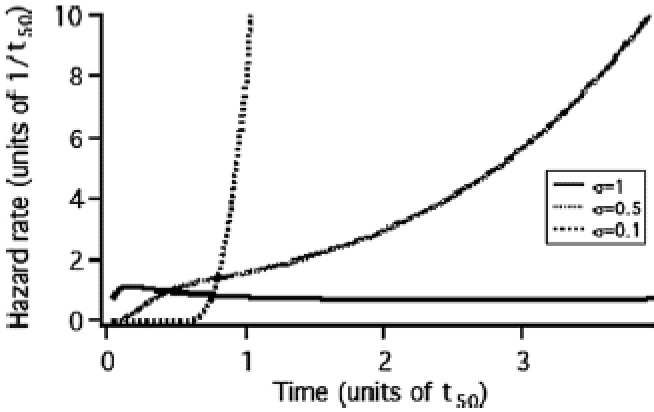

Figure 2.23 Hazard Rate of lognormal function with varying σ [68].

When performing reliability testing, the following points must be considered before implementing a reliability test: 1) in what applications will the device be used, 2) in what possible environments and operating conditions will the device be used, 3) what are the possible failure modes and mechanisms, 4) what level of reliability does the market require for the device, and 5) how long is the device expected to be in service. Once this is determined, there are multiple accelerated stresses that can be applied to devices such as: 1) temperature, 2) voltage, 3) temperature difference, and 4) current [51]. An important consideration in reliability testing is that the testing must contribute to the appropriate evaluation and improvement of semiconductor reliability [51].

2.5 Reliability Model Classification

Reliability models can be classified into two types: 1) physical models, and 2) statistical models. Physical models are used to explain the electrical and parametric behavior of semiconductor devices, whereas statistical models are used to understand statistical inference and the estimation of defect and failure rates. Due to the long lifetime and low failure rate requirements of semiconductor devices, test under actual usage conditions would require extensive test time and excessively large sample sizes. To

shorten the test time, accelerated tests on voltage, temperature, and humidity have been developed. In addition, statistical sampling is used [50]–[53]. However, in recent years, customer demand for shorter development-to-shipment times as well as the increasing advancement and complexity of semiconductor devices has made failure analysis extremely difficult. Consequently, the evaluations of basic failure mechanisms are now being studied when a device is in the development phase. Products are divided into different test element groups such as process and design [51].

2.6 Proposal

The Micron/Numonyx 45 nm technology *PCRAM* production part will be used in mobile devices, such as smart phone and/or tablet. Considering the environment and the operating conditions that a mobile device is exposed to, if the mobile device were to be left in an automobile on a summer day, how many bits are at risk of being sensed incorrectly during the READ operation? Using the standard retention test discussed in Section 2.3.2.1, the retention prediction shows that the mobile device could sit in the car for 10 years and retain the state of the bit, if the ambient temperature of the car is below 85 °C. However, what if a programming pulse or READ pulse were applied multiple times while the mobile device was at an elevated temperature? How many *PCRAM* cells within the array would be at risk of possible retention loss, or what would be the percentage of bits that would fall within the programming/reading window, which could possibly be sensed incorrectly? The market reliability requirement for the Bit Error Rate for an array of cells is 1 part-per-million (*PPM*). Would the current retention prediction model be adequate to predict a possible retention issue?

The hypothesis for this research is that a reliability prediction method that finds the optimal pulse conditions for an array of *PCRAM* devices (using ambient temperatures between 25 to 125 °C) and predicts the Bit Error Rate (*BER*) has the potential to predict reliability issues closer to the normal operating conditions for the device. In this work, the aim of this research is to develop a reliability prediction method, different than standard retention reliability methods, using lower ambient temperatures from 25 to 125 °C. This new method models and predicts a single combination of temperature and pulse conditions that give the lowest Bit Error Rate (*BER*) on a 1-Gigabit (*Gb*) array of experimental *PCRAM* devices, using the Micron/Numonyx *PCRAM* 45 nm cell architecture.

2.7 Conclusions

To support reliable large array products, *PCRAM* must be able to retain data over the life of the product [56]. The standard reliability prediction methods used on *PCRAM* and semiconductors have been reviewed, including the materials and geometries of the Micron/Numonyx 45 nm *PCRAM* experimental device, which was used in this study. The hypothesis for the research and aim of this dissertation has also been reviewed.

CHAPTER 3: EXPERIMENTAL SETUP AND OPTIMAL PULSE CONDITION STRATEGIES

3.1 Experimental Setup

In Chapter 3 the experimental setup used for developing the reliability prediction method is presented. This includes the screening of the voltage pulse amplitude and SET quench time, which is later used to determine the design space for the designed experiments. The prediction models are created for the optimal pulse conditions and Bit Error Rate (*BER*), which are then used to predict a single combination of temperature and pulse conditions giving the lowest Bit Error Rate (*BER*), on a 1-Gigabit (*Gb*) *PCRAM* array of Micron/Numonyx 45 nm *PCRAM* experimental devices.

3.1.1 Electrical Test Setup

In general, the most basic form of electrical testing for a single *PCRAM* device can be performed using a pulse generator (for programming the device) and an oscilloscope to determine the voltage drop across the device (through the use of a series load resistor) [69]. For the Micron/Numonyx 45 nm PCRAM experimental chip, in order to access the 1 Gigabit (*Gb*) array, a device specific probe card and tester capable of making array level measurements is needed. The probe card is specifically designed for the Micron/Numonyx 45 nm *PCRAM* experimental chip to collect the electrical measurement data. Also discussed in Chapter 2, the distribution of the resistances for the amorphous and crystalline phases (or RESET and SET states) over an array of *PCRAM*

devices depends on the shape of the programming pulse. For these reasons, all measurements were performed using the MicroMate (μM) tester (Figure 3.1), which is a Micron specific tool that consists of a self-contained module offering the combination of both single cell and array level electrical characterization.

Figure 3.1 MicroMate (μM) Tester.

Depending on the part, the bond pads or electrical contact points between the *PCRAM* device and the pins of the probe card can change. For this reason, the package part probe cards are interchangeable on the probe stations, allowing multiple part types to be tested on the same probe station.

As shown in Figure 3.2, the device specific probe card can be inserted into a probe station just above the thermal chuck. Built-in clamps on the probe station are used to hold the package part probe card securely in place. The thermal chuck is used to hold the wafer in place by applying a vacuum on the back-side of the wafer; the thermal chuck also has electrical coils within the chuck, allowing the wafer to be heated for the temperature measurement tests.

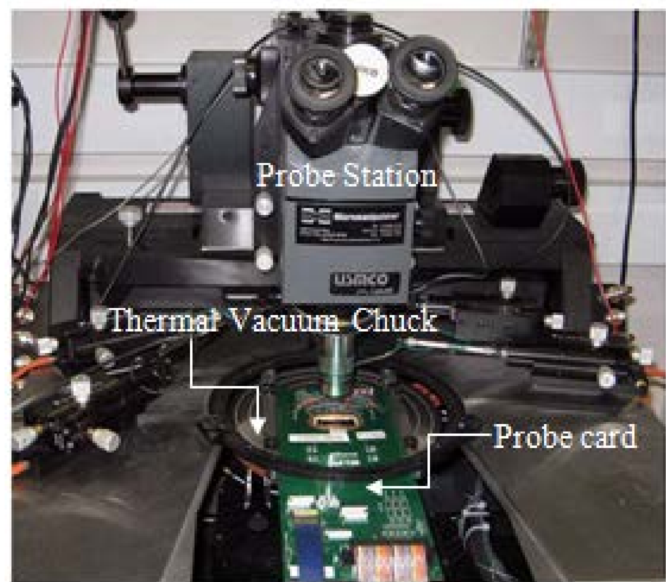

Figure 3.2 Probe station, showing package part probe card and thermal vacuum chuck (directly below the probe card).

As discussed in Chapter 1, each memory cell in the *PCRAM* array is referred to as a storage element. The storage element consists of a top electrode, memory layer (*GST*), and the heater storage element material. This storage element is connected to a *BJT* selection transistor, as discussed in Chapter 2 (shown in Figure 3.3, right). In the memory array, the base of all BJT select transistors is connected to the same row or “Word-Line,” while the top-electrode contacts the *PCRAM* cells belonging to the same column or “Bit-Line.” The memory cell is selected by means of row (or Word-Line) and column (or Bit-Line) decoders that generate the electrical control signals required for the READ and SET/RESET programming operations (shown in Figure 3.3, left).

It should also be noted that the Micron/Numonyx *PCRAM* 45 nm 1-Gb experimental wafers have trims available that can be used to switch the SET pulse from current mode (or *I*-force) to a voltage mode (or *V*-force), as shown in Figure 3.3, right. In the production part, the current mode (*I*-force) is used for the SET pulse and voltage

mode (*V*-force) is used for the RESET pulse. For this reason, the optimal pulse conditions for the SET pulse using voltage mode (*V*-force) are not well understood on the Micron/Numonyx 45 nm 1-Gb part. For all tests performed in the designed experiments (to be discussed), *V*-force is used for both the SET and RESET programming pulses.

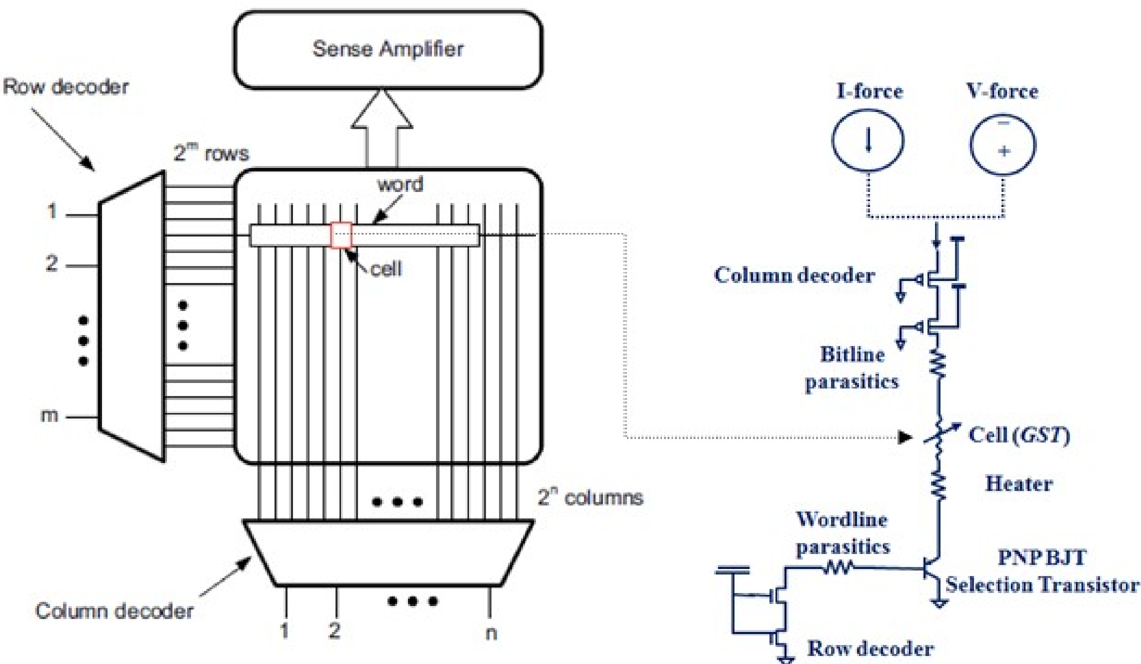

Figure 3.3 Left: Diagram of *PCRAM* array [25], [42]; Right: Circuit schematic of an individual memory cell in the *PCRAM* array, Parasitics, Heater, Select Transistor, and programming pulse source.

In voltage mode programming, the memory cell is biased by applying an adequate voltage level to the selected Bit-Line (*BL*) through the high-voltage *PMOS* transistors. The *BJT* is turned on by applying 0 V to the addressed Word-Line (*WL*), which is connected to the base of the *PNP-BJT*. The current flowing through the *PCRAM* cell is controlled by means of the *WL* voltage. The stored information is read-out by sensing the current flowing through the cell (which will be referred to as the READ current), when a suitable READ voltage is applied. To prevent unintentional programming of the *GST* state, the bit-line READ voltage is set to 1.20 V.

In order to measure the cell current of the SET and RESET state with high accuracy, the *PCRAM* array can be operated in direct memory access (*DMA*) mode, allowing the cell current (I_{cell}) to be sensed for a given bit within the array directly during the READ operation. The cell resistance (R_{cell}) is calculated as the ratio between the READ voltage (V_{read}), which is applied across the cell and the current sensed, which is flowing through the cell I_{cell} (i.e., $R_{cell} = V_{read} / I_{cell}$).

3.1.2 The SET and RESET Pulse

In beginning, the process of determining the optimal programming conditions for the SET and RESET programming pulses, a key aspect that needed to be considered was the shape of the RESET and SET programming pulses. As described in Chapter 1, a proper RESET pulse requires a rapid quenching of the chalcogenide material to place the *PCRAM* cell in the amorphous or RESET state. For this reason, a square pulse was chosen for the RESET pulse operation, with the RESET pulse width fixed at 45 nsec and a trailing edge or quench time set at 10 nsec. The quench time of 10 nsec is the fastest reproducible pulse that can be applied to the 1-Gb *PCRAM* array with this tester.

For the SET pulse, a gradual trailing edge has proven to be more efficient when programming an array of devices into the crystalline or SET state [70], allowing the atoms within the chalcogenide material more time to arrange into a crystalline phase. For this reason, a trapezoidal, or "set-sweep," form of pulse was implemented (shown in Figure 3.4). The set-sweep pulse is characterized by a maximum (V_M) and minimum (V_m) SET voltage, and the time before quench is labeled as T_s [70], which we will later refer to as the SET quench time (Q_s). In the literature, the set-sweep pulse of an array of *PCRAM* devices was programmed on an 8-Mb *BJT* selected array and found to have the advantage

of narrowing the SET distribution when programming multiple cells, due to the gradual change in the temperature profile [70].

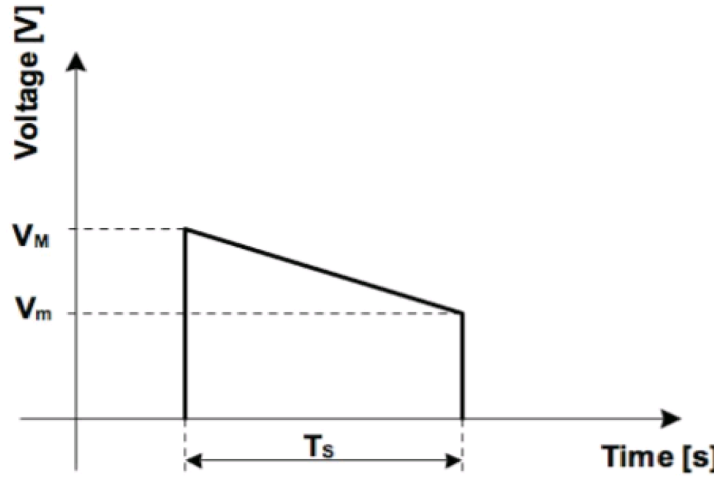

Figure 3.4 Set-Sweep program pulse [70].

The theory behind the set-sweep pulse is that each cell has a specific optimum SET voltage for a determined programming time [70]. By using a trapezoidal SET pulse, different optimum SET voltages can be applied to different cells being programmed simultaneously; hence, if the optimal program voltage of a cell is in the range of (V_M) to (V_m), the cell turns out to be programmed with optimum conditions [70].

Prior to conducting the designed experiments, initial screening of the RESET pulse amplitude (V_r) and the SET quench time (Q_s) were performed to determine the window of values to use for the optimal pulse conditions Design of Experiment (DOE). The initial screening was performed to determine the high and low levels, which would be used for the DOEs as represented in the cube plots in Figure 3.5. In the Cube Plot shown (Figure 3.5, left), the left half of the two-dimensional geometric figure represents the observations of the cell resistance (R_i) collected when the RESET voltage (V_r) pulse amplitude is set at its low level, and the right half represents the observations collected at

its high level. Likewise, the bottom half of the cube plot represents the observations when the SET quench time (Q_s) is set at its low level, and the top half represents the observations at the high level. When a third factor is introduced, an added dimension is created resulting in a three-dimensional geometric figure as shown in Figure 3.5, right. More than three factors can be used in a DOE; however, when monitoring the response, additional factors must be held constant while the three factor response is observed. Care needs to be used in creation of the treatment run combinations. If one of the corner points is going to result in failed product, then for the optimal conditions design, it is more beneficial to create a smaller design space inside the original design.

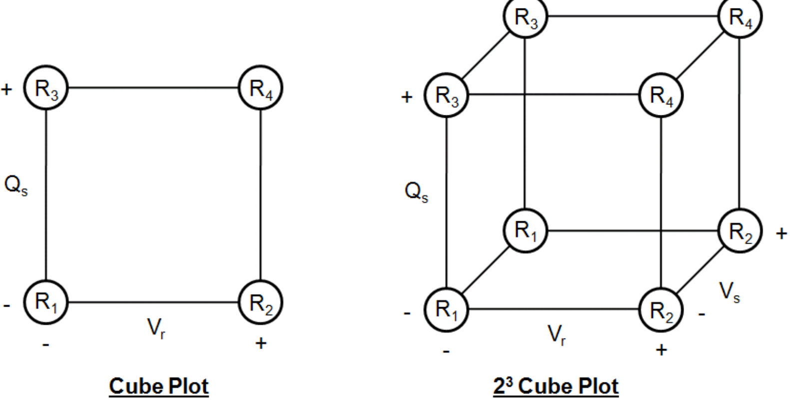

Figure 3.5 Design of Experiment Cube Plot (left) and 2^3 Cube Plot (right).

When setting up the design space window for modeling the optimal pulse conditions, consideration was taken to ensure that the window of pulse conditions and temperatures for the design space were large enough to capture the cell resistance response and determine the optimal conditions without causing over-programming of the *PCRAM* cell. In the initial testing, with the chosen RESET and SET pulse shapes presented, a “Program and Verify” technique was used for both the SET Quench time (Q_s), shown in Figure 3.6, and for the RESET pulse amplitude (V_r), shown in Figure 3.7,

used in determining the quench time window for the SET pulse and voltage pulse amplitude window for the RESET and SET pulses.

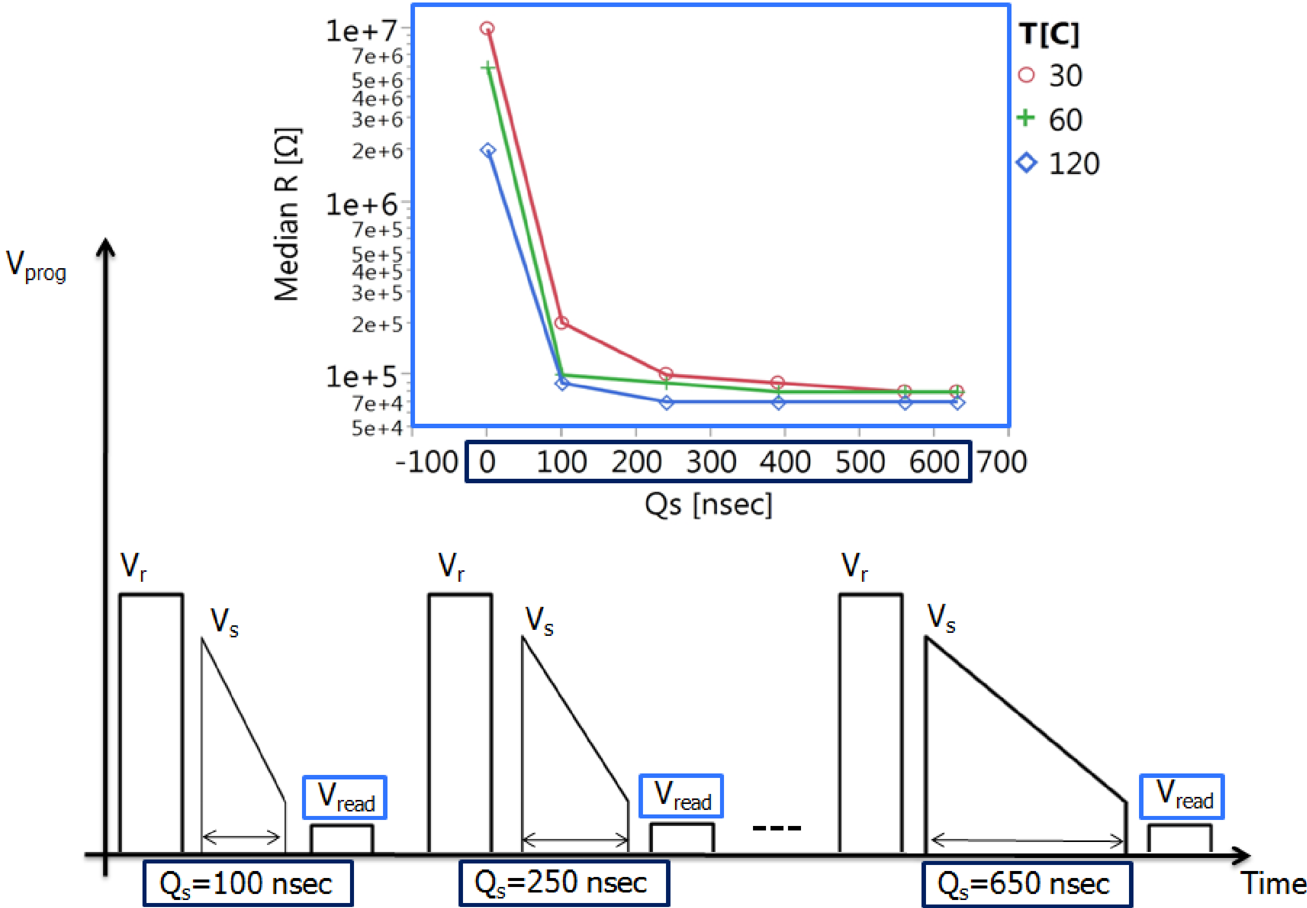

Figure 3.6 Sequence of programming and read pulses, showing the RESET-SET transition as a function of SET quench time (Q_s).

For the screening of the SET quench time (Q_s), sequences of increasing Q_s were applied to an array of cells, which were programmed into the amorphous or RESET state prior to the SET pulse. The median resistances of the 440 bits sampled from the 1-Gigabit *PCRAM* array is shown in Figure 3.6. As depicted, the pulse sequence consisted of first applying a RESET pulse (*Vr*) to place the partition of cells in an amorphous or RESET

state prior to applying the SET pulse with increasing quench time (Q_s), followed by a READ (*Vread*) pulse.

In this test, the SET quench time (Q_s) sample window was between 100 nsec and 650 nsec, while holding the SET pulse amplitude at 5 V for each applied SET pulses. To initialize the sequence, a 6 V RESET pulse is applied just prior to the SET pulse. After the SET pulse is applied, the READ current is sensed in *DMA* mode, and the cell resistance is calculated. The test was conducted at three different temperatures: 30 °C, 60 °C, and 120 °C. The READ points in Figure 3.6 are the median resistance values taken or READ after the SET and RESET voltage pulses were applied at a given temperature. As mentioned above, the sampled median resistance was obtained from 440 bits in the 1-Gigabit array of *PCRAM* experimental cells.

As shown in Figure 3.6, the RESET to SET transition shows a temperature dependence at lower values of Q_s. At higher values of Q_s the SET pulse is able to fully crystallize the active region above the heater, changing the phase of the active region from an amorphous phase to a crystalline phase. At 100 nsec, the SET pulse is marginal, showing overall higher median cell resistance than at higher values of Q_s, meaning that at ~100 nsec the SET pulse amplitude does not have sufficient time to cool after the programming pulse, which is needed to place the active area above the heater in a crystalline phase.

For the screening of the RESET voltage (V_r) pulse amplitude, sequences of increasing V_r amplitude were applied to an array of cells, which were programmed into the crystalline or SET state prior RESET pulse. The median resistances of the 440 bits sampled from the 1-Gigabit *PCRAM* array are shown in Figure 3.7. As depicted, the

pulse sequence consisted of first applying a SET pulse (*Vs*) to place the partition of cells in a crystalline or SET state prior to applying the RESET pulse (*Vr*) and subsequent READ (*Vread*) pulse.

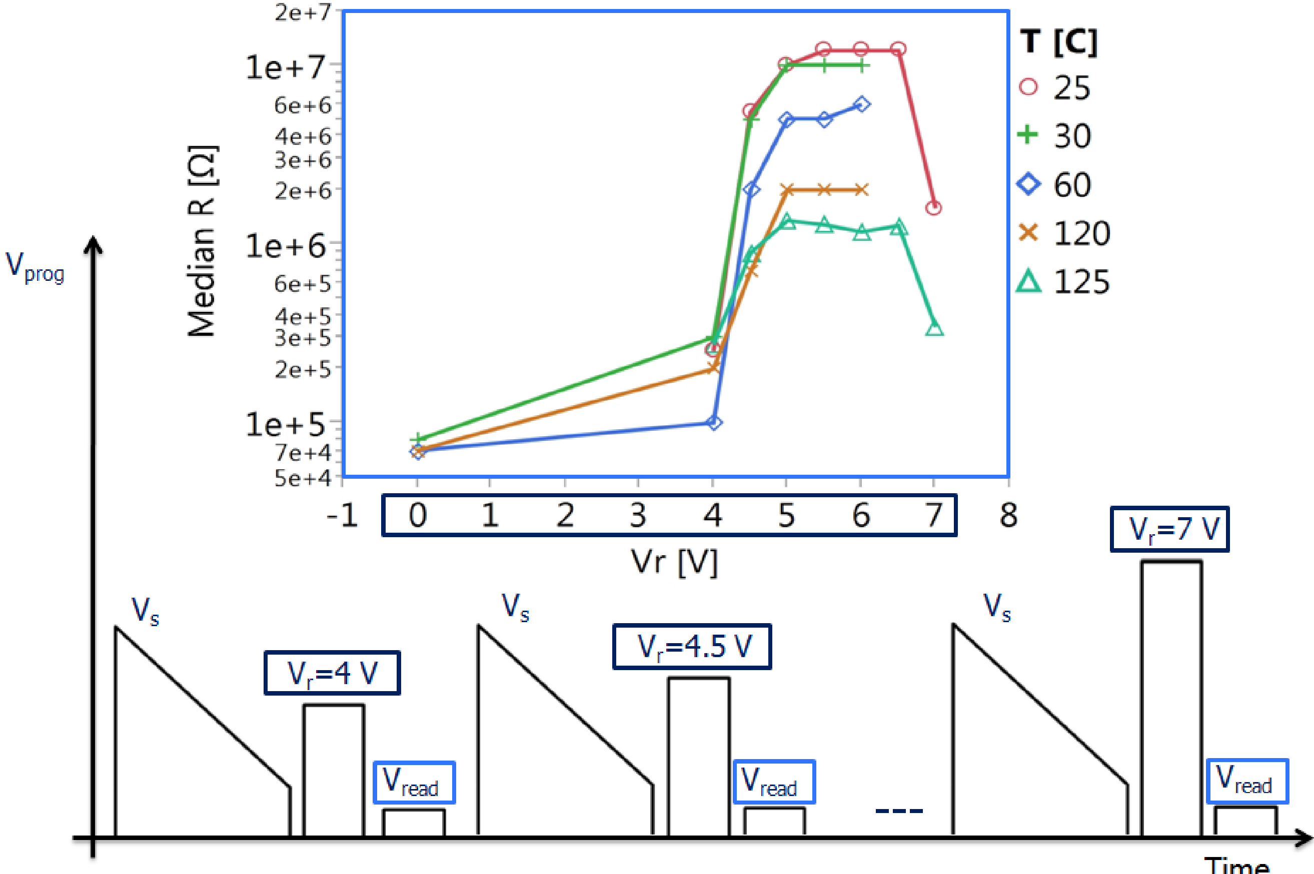

Figure 3.7 Sequence of programming and read pulses, showing the SET-to-RESET transition as a function of RESET pulse amplitude.

In this test, the RESET voltage (V_r) pulse amplitude is increased with increments of 0.50 V while holding the total RESET pulse time at 55 nsec for each RESET pulse applied. To initialize the sequence, a 5.50 V SET pulse is applied just prior to the RESET pulse. After the RESET pulse is applied, the READ current is sensed in *DMA* mode, and the cell resistance is calculated. The test was conducted at five different temperatures: 25 °C, 30 °C, 60 °C, 120 °C, and 125 °C. The READ points in Figure 3.7 are the median

resistance values taken or READ after the SET and RESET voltage pulses were applied at a given temperature. As mentioned above, the sampled median resistance was obtained from 440 bits in the 1-Gigabit array of *PCRAM* experimental cells.

As shown in Figure 3.7, the SET to RESET transition shows significant temperature dependence as the RESET voltage (V_r) transitions from 4 V to 5 V, which is the point at which the amorphous dome starts to form over the heater. At 4 V, the RESET pulse is marginal. For the 60 °C trace, little to no change in the median resistance is measured between the 0 V and the 4 V pulse. At ~4 V, the RESET pulse amplitude does not have sufficient cell current to generate the Joule heating necessary to heat the active area above the melting temperature (*Tm*) for the majority of the 440 bits sampled.

One more observation from Figure 3.7 is related to the cell resistance reaching an almost steady state for RESET voltages between 5 V and 6V but then decreasing on the 25 °C and 125 °C traces between 6.5 V and 7 V. Note: The 25 °C and 125 °C were the only two traces that had RESET voltages applied up to 7V, all other temperature traces were only applied up to 6V. With increased programming voltage (*Vr*), the thickness of the amorphous dome increases [71]. This drop in resistance with increasing programming current is referred to as the "Over RESET phenomena," which is defined as a decrease in the cell resistivity and activation energy even with the thickness of the amorphous cap increasing [71], as shown in Figure 3.8.

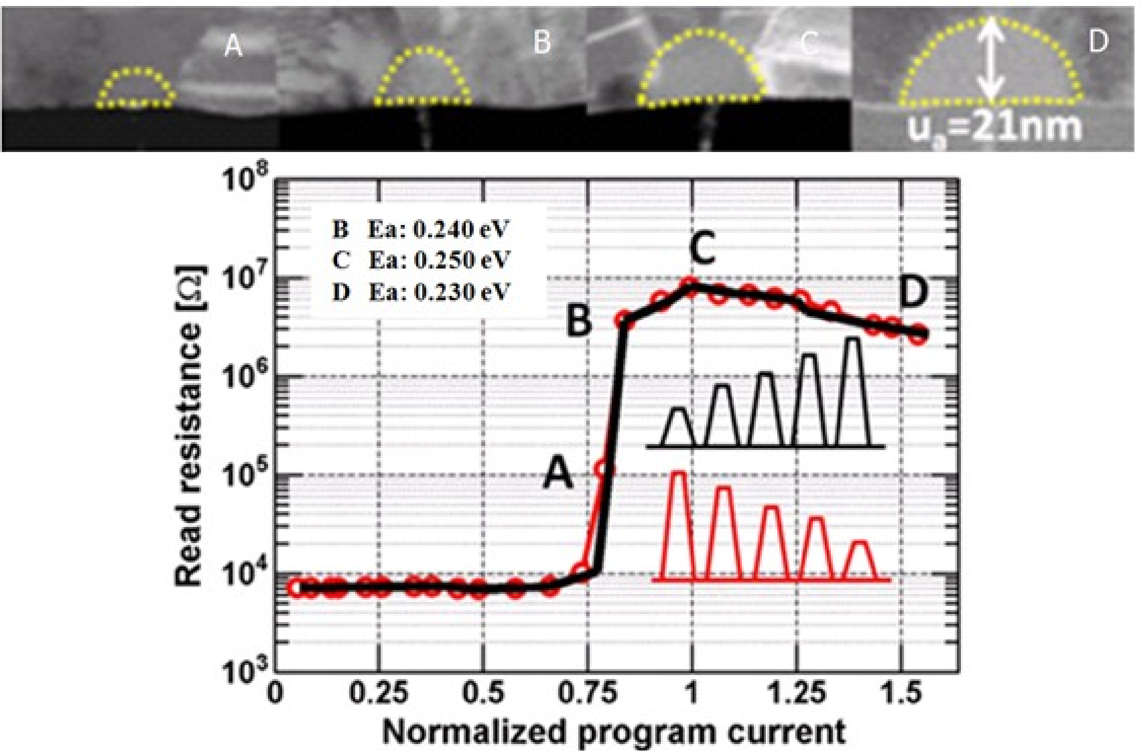

Figure 3.8 Over RESET phenomena: Top: TEM cross-sections of the active region of a *PCRAM* cell for programming currents A, B, C, and D; Bottom: READ resistance vs. programming current for sequences with increasing and decreasing programming current, showing decreasing activation energy for Over RESET bit D [71].

3.1.3 Distributions

3.1.3.1 Phase Distributions

To better understand the temperature dependence of the cell resistance in the RESET state, the natural log of the median cell conductance (of the data shown in Figure 3.7) is plotted as function of 1/T (Figure 3.9), where T is the temperature (in Kelvin). In Figure 3.9, the temperature dependence of the conductance in the amorphous phase (RESET state) of the *GST* film can better be seen based on the slope of the line for the various RESET pulse voltages over the temperature range. For RESET, pulse amplitudes between 3.9 V and 4.5 V bits are being partially RESET by the applied voltage pulse, meaning that both the 3.9 V and 4.5 V pulses show an intermediate behavior between

amorphous (RESET) and crystalline (SET) phases. The change in the slope of the 7 V trace should also be noted, which is related to the over programming phenomena shown in Figure 3.8, showing a similar change (or lowering of the conductance activation energy) as *Vr* is increased above 6 V.

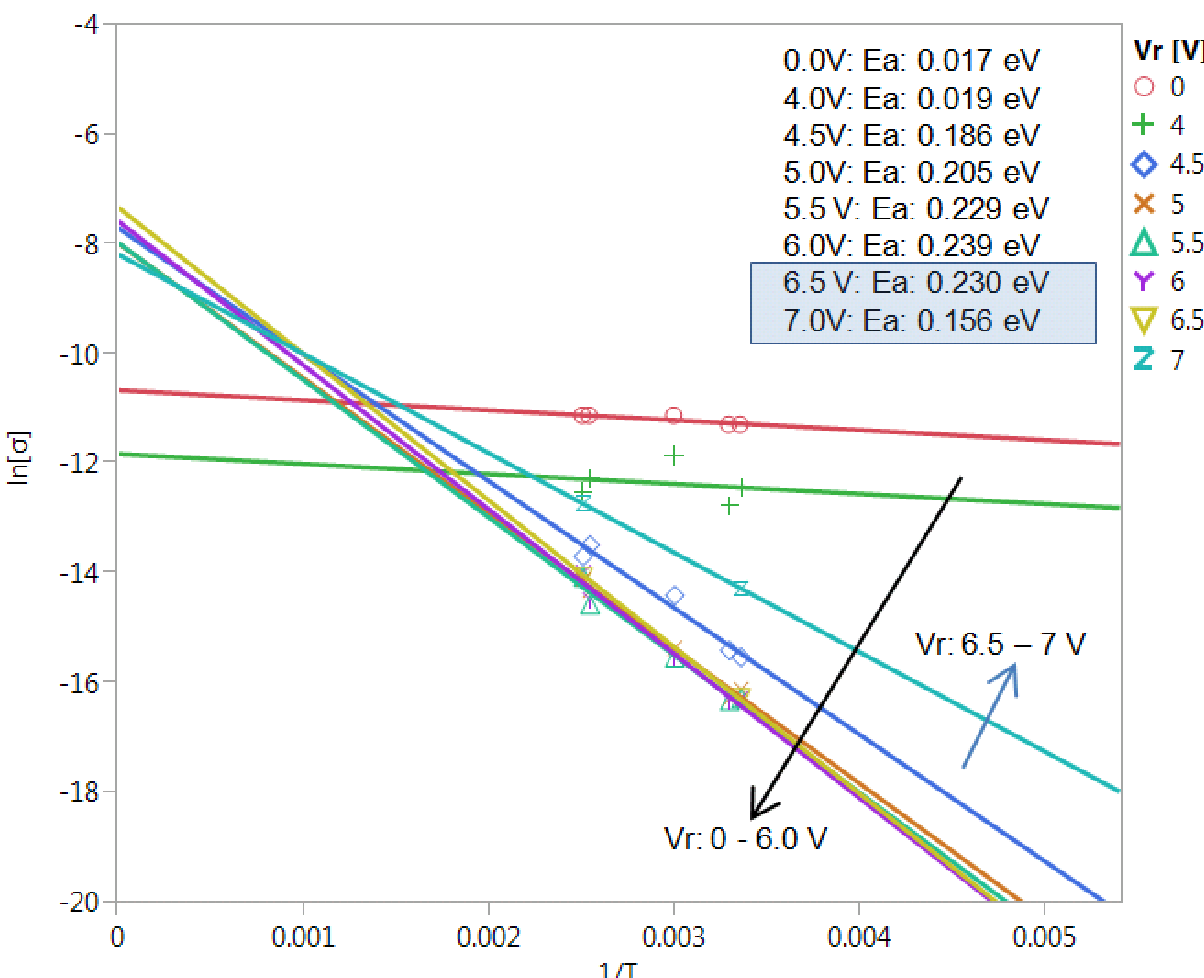

Figure 3.9 Temperature dependence of resistance for SET to RESET voltage pulse amplitude sequence.

The temperature dependence of the cell resistance in the RESET state is largely due to the amorphous phase of the *GST* material. For RESET, pulse voltages between 4.5-6 V, the slope and/or activation energies of the cells show a steady increase in the

conductance activation energy as *Vr* increases (as shown in Figure 3.9). Hence, the thickness of the amorphous dome is increasing as *Vr* increases and the energy barrier, which needs to be overcome for conduction in the chalcogenide glass to occur, is increasing. From the conduction activation energies calculated, the upper limit of the design space for *Vr* was set at 6 V, which shows the highest conduction activation energy prior to the over-reset transition.

3.1.3.2 Cumulative Distributions

To analyze the array performance to the SET and RESET programming pulses discussed in Sections 3.1.2 and 3.1.3, the cell percentages vs. resistance were reviewed to determine the spread of resistance values between the different cells inside the array, over the three different temperatures of 30 °C, 60 °C, and 120 °C.

Figure 3.10 shows a 440-bit distribution from a single-tile of SET and RESET cell resistances that were collected using the programming method discussed in Sections 3.1.2. Looking at the resistance distribution by cell percentage for the 440 bits of RESET *PCRAM* cells (shown in Figure 3.10 (middle)), it is apparent that the RESET voltage amplitude programming pulse used for the RESET operation is able to RESET the majority of the *PCRAM* cells, as the RESET voltage pulse amplitude reaches 5 V. The resistance tail discussed in Section 2.3 is present but not so apparent due to the small sample size (440 bits). The partial-RESET voltage pulse of 4.5 V has the most predominant RESET tail, which becomes less prevalent as the ambient temperature increases from 30 °C to 120 °C. It should also be noted that as the temperature increases each of the resistance distributions for a given RESET voltage pulse amplitude start to

spread apart. At 5.5 V, the pulse has slightly higher cell resistance values at lower cell percentages when compared to the 5.0 V and 6.0 V RESET voltage amplitude pulses.

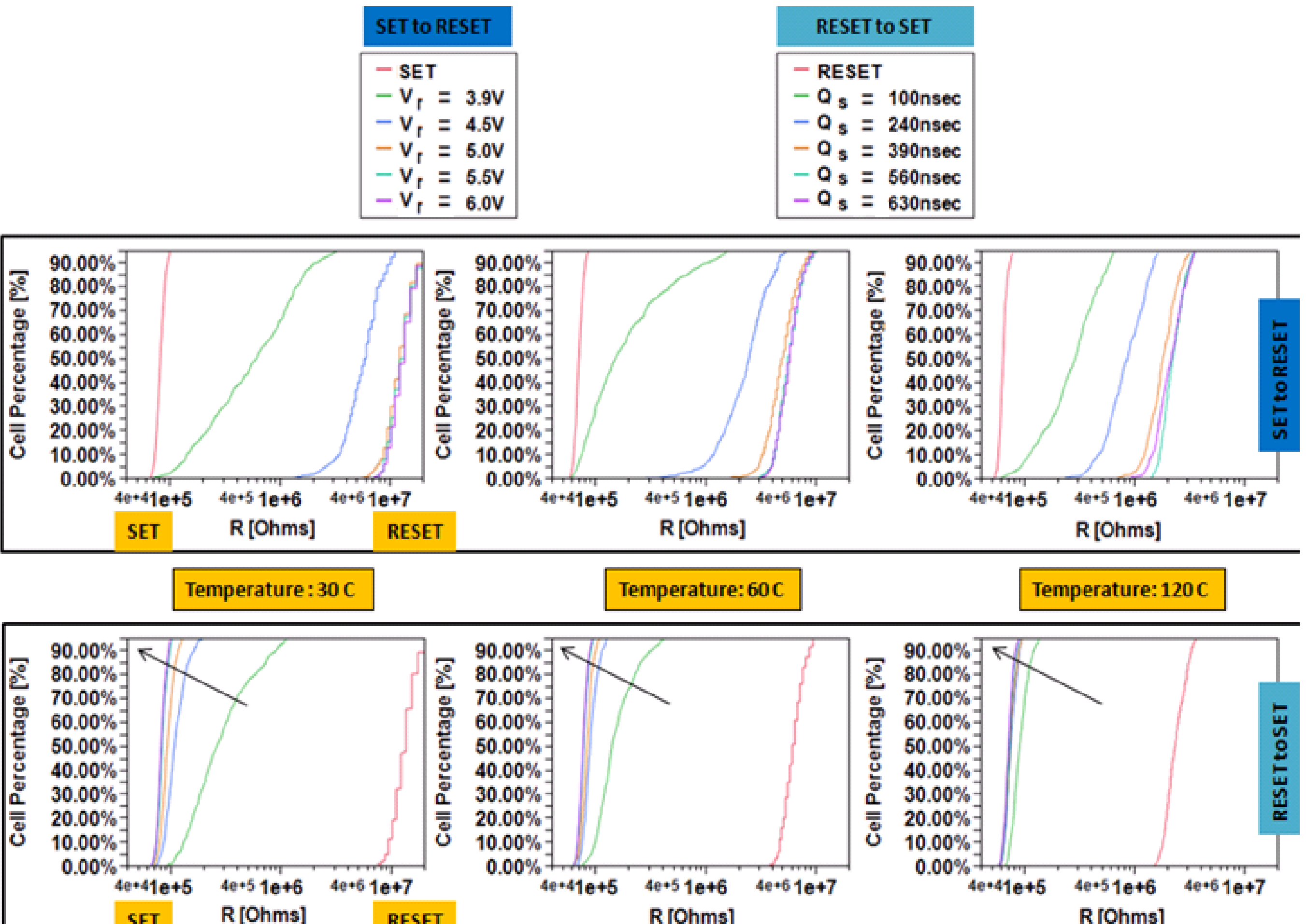

Figure 3.10 Cumulative distributions of the programmed resistance levels: Top: Legends for SET to RESET and RESET to SET pulse sequences; Middle: SET to RESET voltage pulse amplitude sequence; Bottom: RESET to SET voltage pulse quench time sequence.

For the SET voltage pulse quench time sequence, it was interesting to see that the top portion of the SET distribution converges with increased SET quench time (Q_s). However, as the temperature increased from 30°C to 120 °C, most of the bits in the 100 nsec quench time distribution start to match up with the distributions with longer quench times; this result demonstrates how at higher temperatures the partially-RESET bits (from

the lower SET quench time of 100 nsec) start to transition to the SET state, possibly due to nucleation or crystallization of the partially-RESET bits at higher ambient temperature.

3.1.4 Design of Experiments (DOEs) Setup

After completing the initial screening, the design space was determined to be: 1) Temperature (ranging from 25 to 125 °C), 2) RESET/SET voltage (ranging from 4V to 6V), and 3) Slope/Quench Time (ranging from 100 nsec to 1000 nsec) for the SET pulse. To keep the number of observations low and reduce the expense of the experiment, random sample wafers were gathered to avoid bias in the study, allowing a good sample and representation of the population of *PCRAM* engineering wafers. It should be noted that the die sampling within a wafer was selected from specific locations; however, the die selection was chosen at random. A representation of a lot, wafer, and die are shown in Figure 3.11.

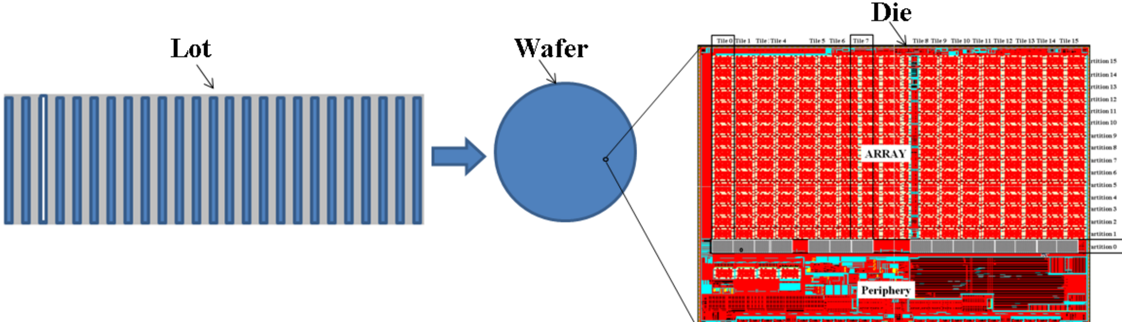

Figure 3.11 Representation of a *PCRAM* lot, wafer, and die.

Three separate engineering lots were sampled: B286889, B282212, and B286883. These lots were generated at different times within the production fabrication process. Moreover, multiple tool groups were used at different processing steps within the traveler flow. From these three lots, three wafers were randomly selected: A3, B20, and C1 respectively, as shown in Figure 3.12. Two of the wafers (A3 & B20) were used for the

measurements for the model creation, and the third wafer (C1) was used as the independent wafer to validate the optimal pulse condition model. DOEs were implemented using a selected window of pulse conditions and temperatures based on the initial screening. It should be noted that some of the conditions selected for the pulse voltages, SET quench times, and temperatures are outside of the normal operating conditions defined for the *PCRAM* product.

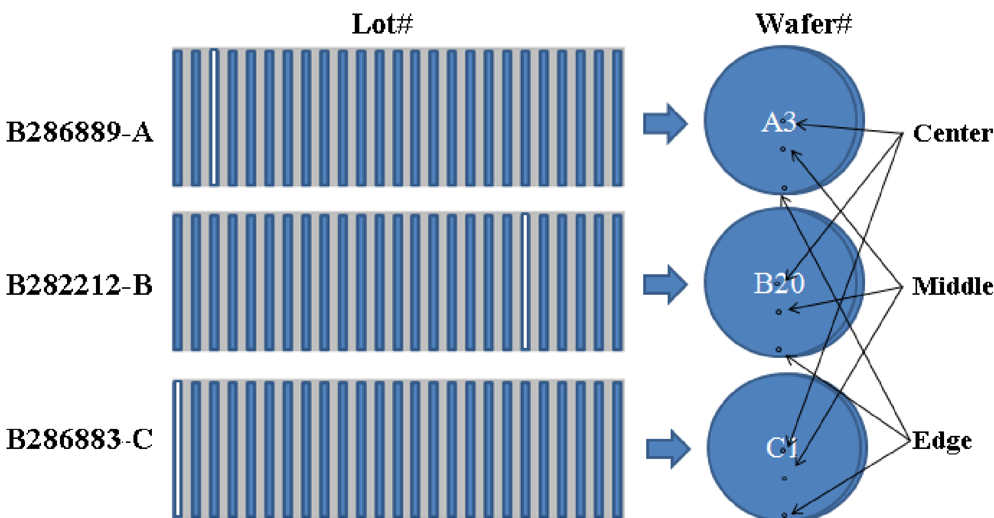

Figure 3.12 Representation of the engineering lot numbers and wafers selected. Die selection was taken at random from regions at the Center, Middle, and Edge of the wafers.

When setting up both the initial DOEs and subsequent DOEs, the use of statistical software (JMP) was needed to determine the best DOE model and to perform the statistical modeling needed to determine the main effects, interactions, and response of the *PCRAM* cell resistance. JMP (pronounced 'jump') is an interactive data visualization software and statistical analysis tool, allowing the user a wide range of statistical analyses and modeling tools [72]. JMP has been a part of Statistical Analysis System (SAS) since

1989, which is when the first version of the JMP software was launched [72]. JMP is used in applications such as DOEs, quality control, and scientific research [72].

The use of regression analysis in JMP became a very powerful tool in determining the optimal pulse conditions model and Bit Error Rate (*BER*) model equations, which will be discussed further, later in this section. From the three separate engineering lots, random die selection measurements were taken at locations in the center, middle, and edge of the wafer. For the comparison of the RESET and SET cell resistance, the bits were programmed with the standard Micron programming conditions for both the RESET and SET pulses. The variability plot of the cell resistances from the center (C), middle (M), and edge (E) of the wafers selected are shown in Figure 3.13 (RESET state) and Figure 3.14 (SET state), 441 bits were sampled from each die location.

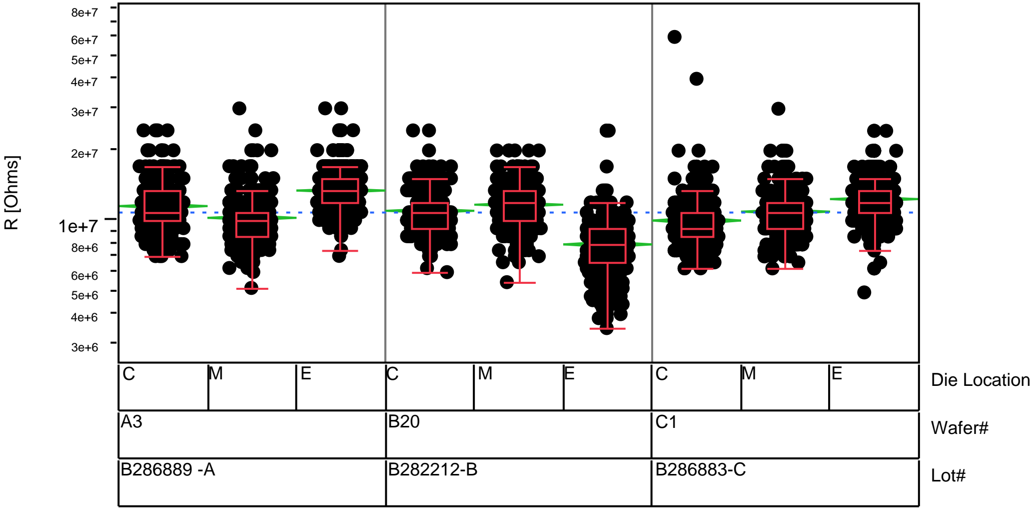

Figure 3.13 RESET state cell resistances of 441 *PCRAM* bits from the engineering wafers sampled at the center (C), middle (M), and edge (E) of each wafer after applying a 5.50 V RESET pulse.

The sample measurements taken show the variability present within-wafer and from lot-to-lot for the three separate engineering lots sampled. From the variability plots,

the engineering wafers were found to be comparable. Lot# B282212 (wafer# B20) did show overall lower edge (E) resistance when compared to the other two lots in the RESET state.

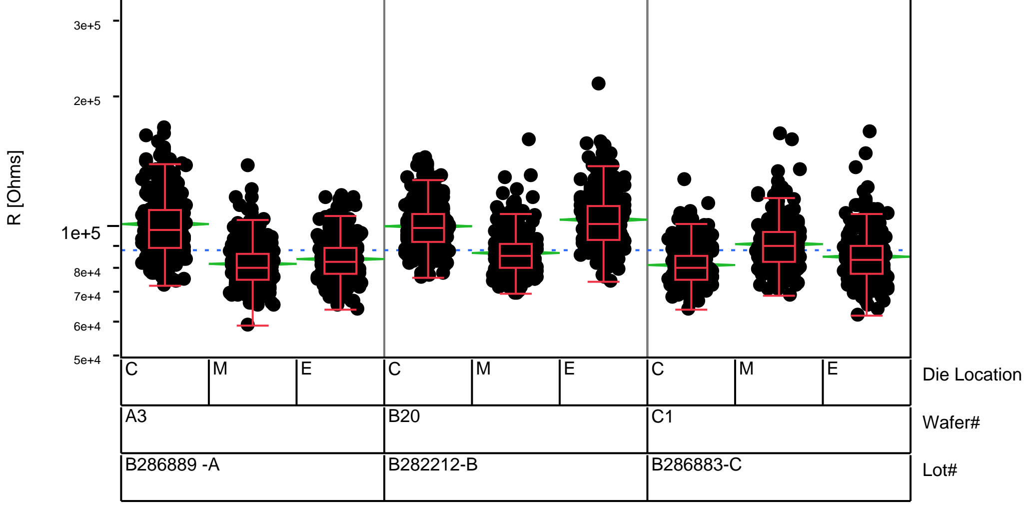

Figure 3.14 SET cell resistances of 441 *PCRAM* bits from the engineering wafers sampled at the center (C), middle (M), and edge (E) of each wafer, after wafers came from probe.

To help in eliminating some of the unknown responses from the screening tests, surface design models were used to determine the optimal pulse conditions by simultaneously studying multiple variables at one time to determine the main effects and interactions. From this data, tabulated results, box plots, profile results, and surface responses plots were used to graph the response of the resistance of the *PCRAM* cells to a given process variable change. This approach helped in unfolding the true response for each of the variables. From the response graphs, the direction of the response was then analyzed to determine the significance of the variable and eventually to find the optimal location for the pulse conditions by temperature.

When performing the response surface design, for the optimal pulse conditions, the pulse sequence for the response surface design DOEs were completed by performing what we will call "seasoning cycling." The seasoning cycling consisted of ten alternating SET and RESET checkerboard pattern (CKB) pulses across a single partition in the array (67 Mbits), with the given pulse conditions for the SET and RESET pulse. This was done to ensure that the cell resistance values for the SET/RESET states were representative of the given pulse conditions and temperature applied. Figure 3.15 shows an example of the voltage pulses for the RESET (V_r) and the SET (V_s) pulses.

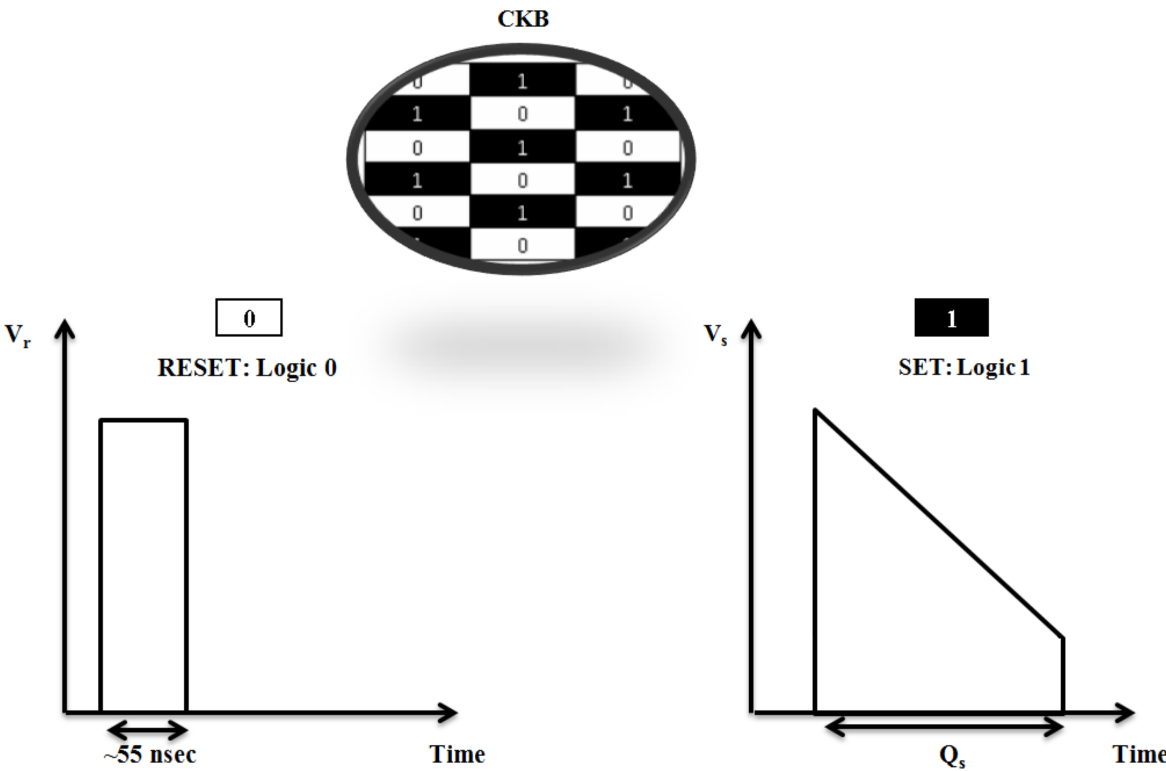

Figure 3.15 Top: Checkerboard programming pattern (CBK); Left: RESET programming pulse shape; SET programming pulse shape.

The programming of the single partition in the array is shown in Figure 3.16. After the single partition has finished the seasoning cycling in the checkerboard pattern,

the READ pulse is applied to a select number of rows and columns from a single 4 Mb tile to collect the sample for the analysis.

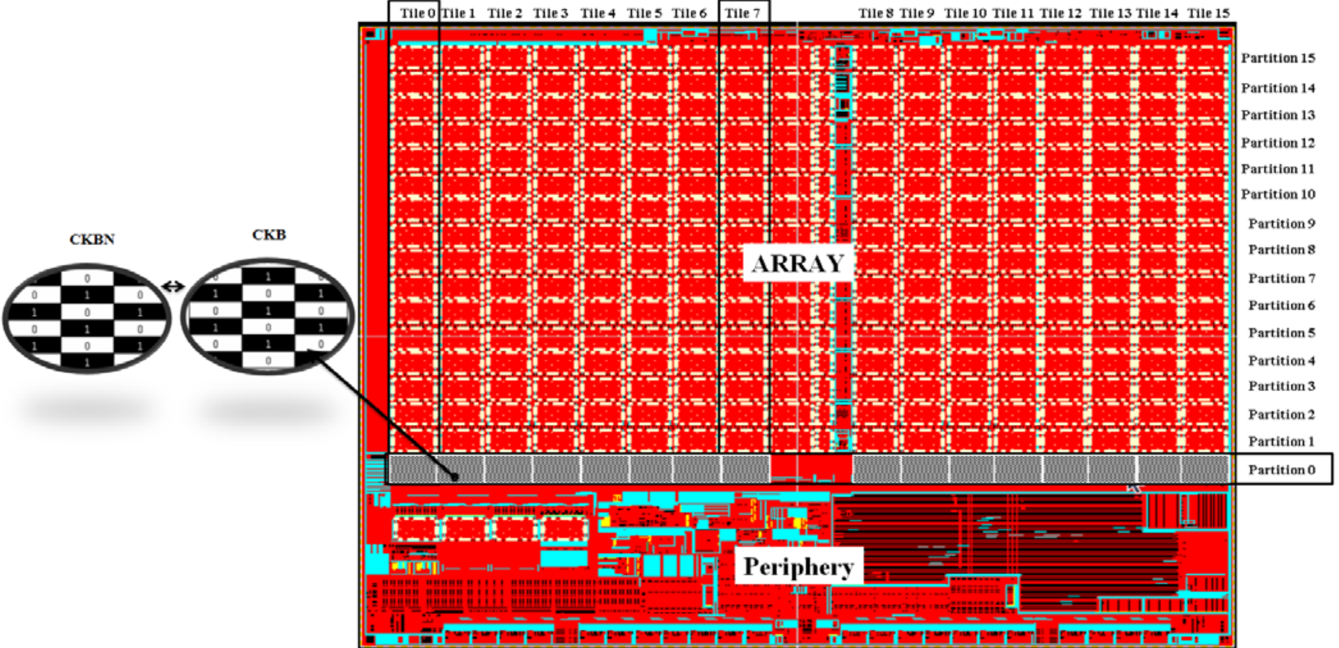

Figure 3.16 Representation of a single partition within a die being programmed with the checkerboard pattern.

The reason for the seasoning cycling and the checkerboard patterning with the given SET and RESET pulse conditions (prior to performing the READ pulse) was to ensure that the interaction between the SET and RESET pulse was taking effect and to check for possible thermal proximity disturb (discussed in Section 2.3). For example, when programming a single bit or an array of bits, the effect of both the SET and RESET pulses needs to be taken into consideration for a given pulse sequence. The reason for this is that the resistance of the intermediate resistance states depends on the distribution of the amorphous and crystalline phases inside the *GST* layer. In particular, the thickness of the amorphous cap obtained after the RESET programming pulse is applied is a key parameter that controls the resistance, and thus the intermediate states in the case of a

partial-RESET for a given bit. The amorphous cap thickness is also important when considering the partial-SET after a programming sequence since; in this case, it affects the minimum value of the cell resistance and, hence, the reading window as discussed in Chapter 2. Finally, the effect of thermal proximity disturb during programming can affect the neighboring bit if the programming temperature gets too hot, which can lead to loss of retention. For this reason, the seasoning cycling in a checkerboard pattern was used.

Considering that there was no cycling feature on the MicroMate (μM) or method of converting the SET pulse programming mode from current mode to voltage mode, software using Python needed to be created to do these tasks and to interface with the μM. The Python script was built to request input parameters such as the partition that would be programmed, number of cycles, and the file location of the modified trims file. Some of the more common script functions written and used in the cycling tests are provided in the appendix of this dissertation. The modified trims file contains a list of the standard trim values, which included the trim values used to change the SET pulse to voltage mode and trim values for changing the RESET pulse amplitude, SET pulse amplitude, and SET quench time. It should also be noted that all of the trims in this file could manually be changed if desired. After importing the modified trims file values into the EI manager of the μM, the script would then perform the seasoning cycling and the DMA READ on the given partition. The trim value changes that were made to go from current mode to voltage mode and to change the SET and RESET pulse conditions are listed in Table 3.1.

Table 3.1 Table of Trim Changes used for Voltage Mode RESET and SET pulse parameters.

Trim Changes	Address	Was (HEX value):	IS (HEX value):
RESET Pulse Amplitude	47C0	0x0007	0x0000 to 0x001F
SET Imola Voltage Mode	47C6	0x0000	0x0100
Bit Line Compensation	47DF	0x0110	0x0220
SET VHPRG	47C3	0x004B	0x001C
SET Pulse Amplitude	47C2	0x0048	0x0087 to 0x00CA
SET Quench Time	47C4	0x0006	0x0000 to 0x000C

CHAPTER 4: MODELING

4.1 Optimal Pulse Condition Modeling

The aim of this chapter is to present the model creation method used in determining the optimal pulse conditions for a given temperature. In the development of a prediction model for the optimal pulse conditions for the RESET and SET programming pulse (for a given temperature), the cell resistance was modeled as a function of temperature (*T),* RESET voltage (V_r), SET voltage (V_s), and SET quench time (Q_s). For the regression analysis, the least means squares method was used to generate the parameter estimates, model equations, surface plots, contour plots, and finally the profiling data used in determining the optimal pulse conditions.

4.1.1 Least Squares Regression

For all regression analysis performed in the Design of Experiments (DOEs), linear regression was used. The linear regression model describes the response to a set of independent variables, which in our case are T, V_r, V_s, Q_s, and *Cycling*. Standard least squares regression is used in this process. The technique fits a line that minimizes the sums of the squared distances from each individual point to the fitted-line and determines the line that fits best. For example, for a regression line where Resistance (R) is the dependent variable and Temperature (T) is the applied independent variable on a standard scatter Y by X plot, then the vertical deviation of the point (T_i, R_i) from the fit line $R = b_0 + b_1 T$ is

$$height\ of\ point - height\ of\ line\ = R_i - b_0 + b_1 T_i\ , \tag{4.1}$$

the sum of the squared vertical deviations from the points (T_i,R_i),..., (T_n,R_n) to the line is then

$$f(b_o, b_1) = \sum_{i=1}^{n} [R_i - b_0 + b_1 T_i]^2. \tag{4.2}$$

The point estimates of β_0 and β_1 are coefficients of $b_0, \ldots, b_k$ which minimize Equation 4.2. To determine the point estimates of β_0, β_1,..., β_k, the partial derivatives of $\frac{\partial f}{\partial b_0}, \frac{\partial f}{\partial b_1}, \ldots, \frac{\partial f}{\partial b_k}$ are taken and set equal to zero, resulting in a system of normal equations for the estimates. The errors in the fitted model, called "residuals," are the differences between the actual value of each observation and the value predicted by the fitted model. It is important to note that the residual data should have no systematic patterns, and the distribution of the residual data should be normal, otherwise a transformation of the cell resistance is needed to normalize the residuals and/or remove the patterns. Transforming the data entails creating another variable that is a function of the original response, such as the square root or log transformation. Transforming the data, prior to fitting the model may alter the variability patterns of the residuals and allow the model to be fit. If the model is found to fit after transforming the data, the results from the regression analysis of the transformed model need to then be back transformed for the point estimate values to be used in the model equation.

When a linear regression model is fit to the data, all eligible model parameters are estimated. One question that has to be answered before investigating assumptions and using the model for predictions is whether the regression relationship is significant. If it

is, then the assumptions can be tested and response predicted. This question can be stated in terms of the statistical hypothesis test shown in Equation 4.3:

$$H_o = \beta_1 = \beta_2 = \ldots.\beta_k = 0 \tag{4.3}$$

$$H_a\text{: at least one } \beta \text{ is not equal to } 0\ ,$$

where, H_o is the null hypothesis and H_a is the alternative hypothesis. The purpose of any statistical data analysis is to meet certain experimental objectives and to answer certain experimental questions. These experimental objectives and questions are stated in the form of hypothesis statements, which consist of both a null (H_o) and alternative hypothesis (H_a). Prior to any data being collected and analyzed, it is important to establish what it is that is being researched. The null hypothesis (H_o) is a statement about the value of one or more population parameters that is usually suspect. In other words, the null hypothesis usually contains the statement that reflects the process under normal conditions. These hypothesized values can be based on historical data, customer requirements, experience, or educated speculation. Most often statistical analyses are performed to disprove or invalidate the statement specified in the null hypothesis. The alternative hypothesis (H_a) is a statement about the value of one or more population parameters that is thought to be true. Usually, the statement in the alternative hypothesis reflects change or deviation from normal conditions.

In proving out the statistical hypothesis, test statistic (t-statistic) and p-values are often used. A test statistic is calculated using the sample data and is generally a transformation of the sample statistic by standardizing the difference between what is observed and what is hypothesized, given the amount of variation and the sample size. For each t-statistic, there is a p-value associated with it. The p-value is the likelihood or

probability of observing the observed value of the t-statistic or more extreme value given the scaled estimate is truly zero. The smaller the p-value the more likely the null hypothesis will be rejected. In other words, if the p-value is small (< 0.05) for a particular factor, then the conclusion is that the factor is statistically significant, or rather, there is a significant increase or decrease in the response as the factor is adjusted. If the p-value is large, then the factor could be removed from the model to help strengthen the other effects and to simplify the model.

There are four DOEs used in this research. For all DOEs, the null and alternative hypothesis is as shown in Equation 4.3. If any of the point estimate values yields a t-statistic (or t-ratio) greater than zero and have a p-value of less than 0.05, then the null hypothesis is rejected, and there is some significant response.

After determining the statistical hypothesis, for the model type, the response surface model design was then defined, which takes into account each of the relations as well as the squared terms for the model effects. The purpose of using a response surface model was to find the optimal values of the terms that produce the maximum or minimum expected response. This is accomplished by fitting a collection of terms in a quadratic model. For example, if there are two independent variables, Temperature (*T*) and Voltage (*V*), then:

Response Surface (*T*) fits: $\beta_0 + \beta_1 T + \beta_2 T^2$

Response Surface (*T,V*) fits: $\beta_0 + \beta_1 T + \beta_2 T^2 + \beta_3 V + \beta_4 V^2 + \beta_5 TV$

Once the regression analysis is completed, estimates of β_0 and β_1 are generated and sorted to screen the variables, which show the most significant effects. Sorting is based on the t-statistic (or t-ratio) and the p-value (or Prob >|t|).

4.1.2 DOE 1

4.1.2.1 DOE 1 RESET State Analysis

In determining the optimal pulse conditions for the RESET and SET pulse shape, a surface response Design of Experiment (DOE) was setup that takes into account low, medium, and high values for: 1) T, ranging from 25 to 125 °C, 2) V_r and V_s, ranging from 4 V to 6 V, and 3) Q_s, ranging from 100 nsec to 1000 nsec. The purpose of this design is to optimize RESET and SET pulse conditions by looking for the locations of maximum and minimum cell resistance for the RESET and SET states, respectively. When building a response surface design with multiple responses, often a factor setting that is optimal for one response may not be optimal for several responses. For this reason, it is best to determine a range for each response that is considered optimal and then simultaneously to analyze all the response surfaces to determine the optimal settings that are acceptable according to the ranges determined for each response. This method of simultaneously analyzing response surfaces is performed using the prediction profiler, which will be discussed later in this chapter.

The layout of this DOE was created using the DOE response surface design generator in JMP. The cube structure for this design is referred to as a “face center cube,” which is a form of a Central Composite Design (*CCD*), as shown in Figure 4.1.

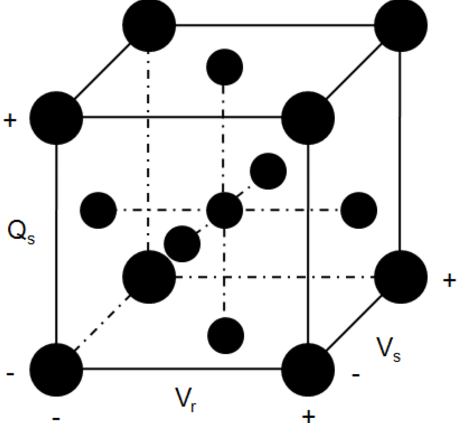

Figure 4.1 Centra Composite Design (CCD), Face Center Cube.

Using the face center cube design, the use of low, medium, and high values were implemented for *T*, V_r, V_s, and Q_s, to check for possible curvature in the response through the use of the medium values or "center points," as shown in Table 4.1.

Table 4.1 DOE 1 matrix of parameters.

T [°C]	V_r [V]	V_s [V]	Q_s[nsec]	TEST Sequence
25	4	4	1000	1
25	4	4	500	2
25	4	6	100	3
25	5	5	100	4
25	6	4	500	5
25	6	6	1000	6
25	6	5	1000	7
80	4	5	1000	8
80	5	5	500	9
80	5	6	500	10
80	6	5	100	11
125	4	4	100	12
125	5	4	100	13
125	6	4	1000	14
125	6	4	500	15
125	6	6	500	16
125	4	6	100	17
125	4	6	1000	18

After performing DOE 1, the individual resistance cell values collected from the designed experiment were grouped by T, V_r, V_s, and Q_s, as shown in the variability plot of Figure 4.2, which is showing only the RESET cell resistance values that were collected after the RESET programming pulse. From the variability plot, it is apparent that the variability in the RESET state resistance distribution for cells programmed with a RESET voltage (V_r) of 4 V is significantly larger than the other distributions that were programmed at higher V_r, at the same temperature.

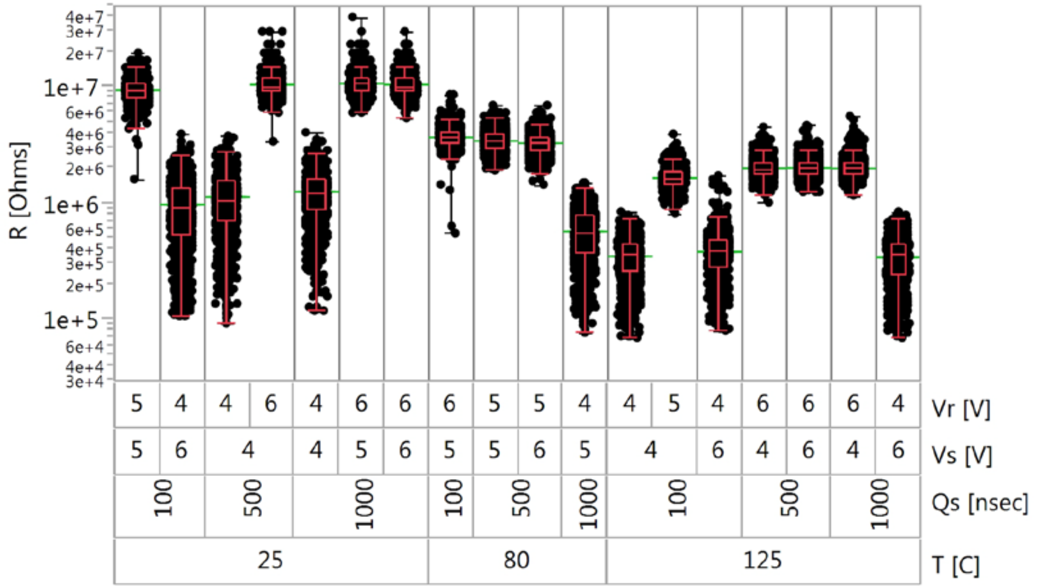

Figure 4.2 Variability plot of the RESET cell resistance bit values for DOE 1 going from SET to RESET state for the given pulse sequence and temperature.

It should also be noted that the overall distribution and median cell resistance of the test sequences programmed with $V_r = 4$ V show a statistically different RESET state than the other bits. This result shows that the majority of the bits, which were RESET at $V_r = 4$ V, are only partially RESET. This was expected based on the initial screening test performed in Section 3.1.3. The partial RESET of the bits is related to the limited volume of amorphous chalcogenide material (*GST*) above the heater element (or in the active

region). To fully RESET the bit, a larger volume of chalcogenide material needs to be melted through Joule heating prior to the quench into an amorphous state or RESET state for the device. In other words, the thickness of the amorphous cap obtained after the RESET programming controls the resistance and the intermediate states (in this case a partial-RESET) for the bits programmed at $V_r = 4$ V. To understand the cell resistance response and possible interactions that are occurring between the RESET and SET pulse parameters and Temperature, the least squares analysis was performed.

In order to perform the least squares analysis in JMP, the data table size had to be reduced due to data storage memory errors, when using JMP, from the large amount of array data collected. To reduce the file size, the median resistance for each DOE test sequence was calculated and only the median values were considered in the least squares analysis for DOEs 1 through 4. The median cell resistance values used for DOE 1 are shown in Figure 4.3. As briefly mentioned in Section 4.1.1, from the least means squares analysis, the parameter estimates (example shown in Figure 4.4) were generated. The model parameters from DOE 1-4 are sorted by the Prob>|t| tests with the most significant variables located at the top. It should be noted that the solid blue vertical lines on the parameter estimates graph show the Prob > |t| = 0.05 significance level for each of the variables for the RESET response in Figure 4.4.

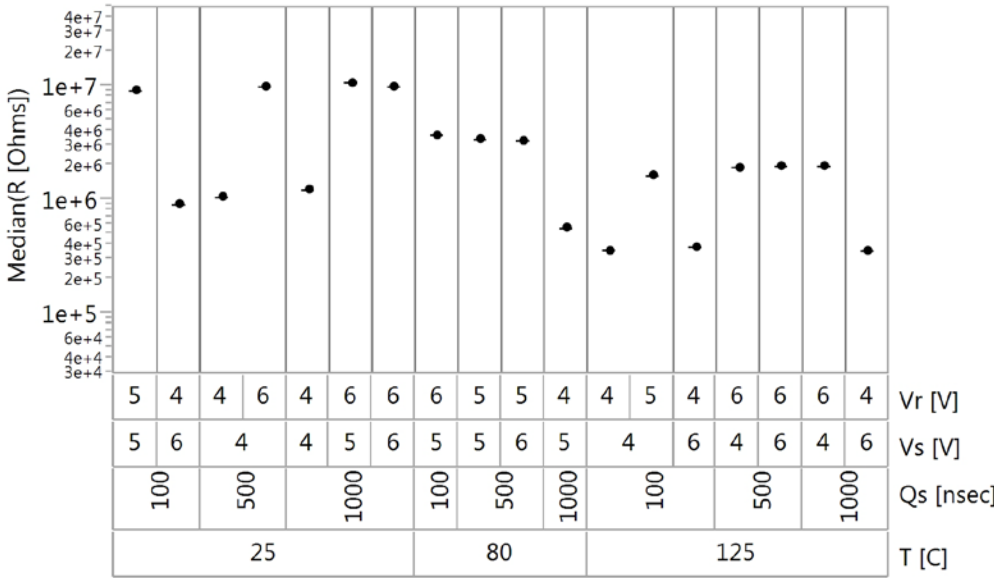

Figure 4.3 Variability plot of the median resistance values for the RESET state of DOE 1 used in the prediction profiler in JMP.

As shown in Figure 4.4, not all of the variables used in the RESET model for DOE 1 are significant. For the RESET state model, the SET voltage (V_s) and the SET quench time (Q_s) have Prob>|t| values greater than 0.05, meaning that they are not statistically significant in terms of the least means squares analysis response for the RESET state.

Term	Estimate	Std Error	t Ratio	Prob >|t|
Vr [V]	2.43E+06	1.66E+05	14.6	<.0001*
T [C]	-4.35E+04	3.64E+03	-12.1	<.0001*
(T [C]-76.1)*(Vr [V]-5.00)	-3.55E+04	3.70E+03	-9.61	<.0001*
(T [C]-76.1)*(T [C]-76.1)	8.63E+02	1.87E+02	4.62	0.0013*
(Vr [V]-5.00)*(Vr [V]-5.00)	-1.78E+06	3.95E+05	-4.51	0.0015*
(Vs [V]-4.94)*(Vs [V]-4.94)	-1.21E+06	4.31E+05	-2.82	0.0202*
Vs [V]	2.51E+05	1.91E+05	1.32	0.2204
Qs [nsec]	4.48E+02	4.25E+02	1.05	0.3203

Figure 4.4 Parameter estimates for the RESET state of DOE 1.

These parameters were purposely not excluded from the model, since the interaction of SET programming pulse parameters will be included into our model for

optimal pulse conditions. It should be noted that this report does not show the intercept (β_0); nevertheless, all other point estimates for the variables are shown. From the parameter estimates, the model equation for the RESET state of DOE 1 can be generated, as shown in Equation 4.4.

$$R_{RESET_DOE1} = -6.25 * 10^6 + 2.43 * 10^6 * (V_r) - 4.35 * 10^4 * (T) - 3.55 * 10^4 * \left((T - 76.1) * (V_r - 5.00)\right) + 863 * (T - 76.1)^2 - 1.78 * 10^6 * (V_r - 5.00)^2 - 1.21 * 10^6 * (V_s - 4.94)^2 + 2.51 * 10^5 * (V_s) + 448 * Q_s, \tag{4.4}$$

It should be noted that the significant figures for the parameter point estimates for DOEs 1 through 4 were set with three significant figures. This number was determined by the tool limitations (i.e., V_{read} : 1.20 +/- 0.01, 3-significant figures; I_{cell} = 0.08 to 19.99 +/- 0.02 μA, 4-significant figures), for the precision needed for the prediction expressions.

Using the RESET model Equation 4.4, a surface and contour plot of the two most significant variables (T and V_r) for DOE 1 are displayed in Figure 4.5, showing the RESET state cell resistance as a function of changing T and V_r.

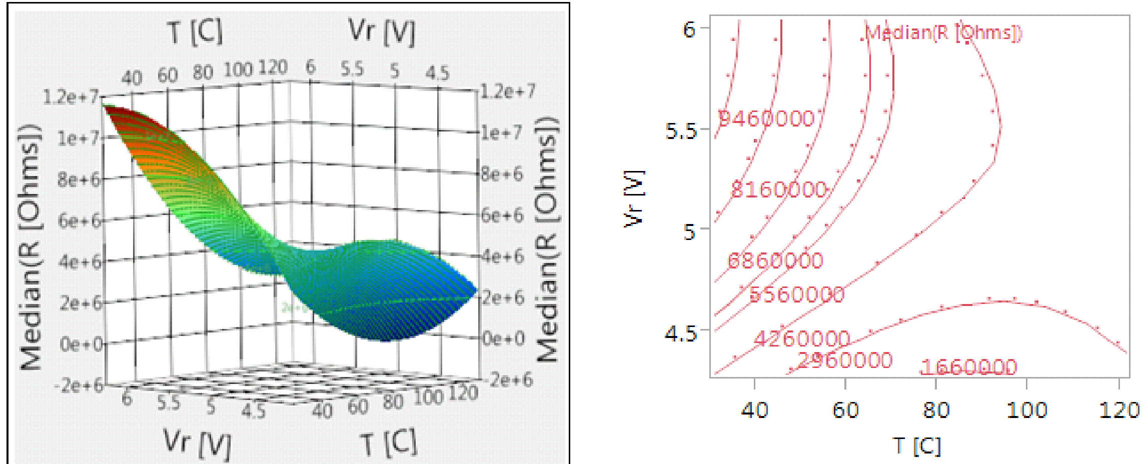

Figure 4.5 DOE 1: Left: Surface Plot of the RESET cell resistance; Right: Contour plot of the RESET cell resistance response of DOE 1.

From the surface plot and contour plots of the RESET cell resistance response, it is apparent that the direction of highest cell resistance is toward lower T and higher V_r. It should be noted that the dots next to the contour lines in the contour plot show the direction of higher cell resistance.

4.1.3.2 DOE 1 SET State Analysis

For the SET pulse conditions of DOE 1, when looking at the variability plot of the cell resistance distributions of the cells programmed with a SET Quench Time (Q_s) of 100 nsec (shown in Figure 4.6), it is apparent that the variability in the cell resistance distributions is much higher than the other test performed at the same temperature, showing how the SET pulse can lead to a partial-RESET operation over an array of cells if Q_s ~100 nsec.

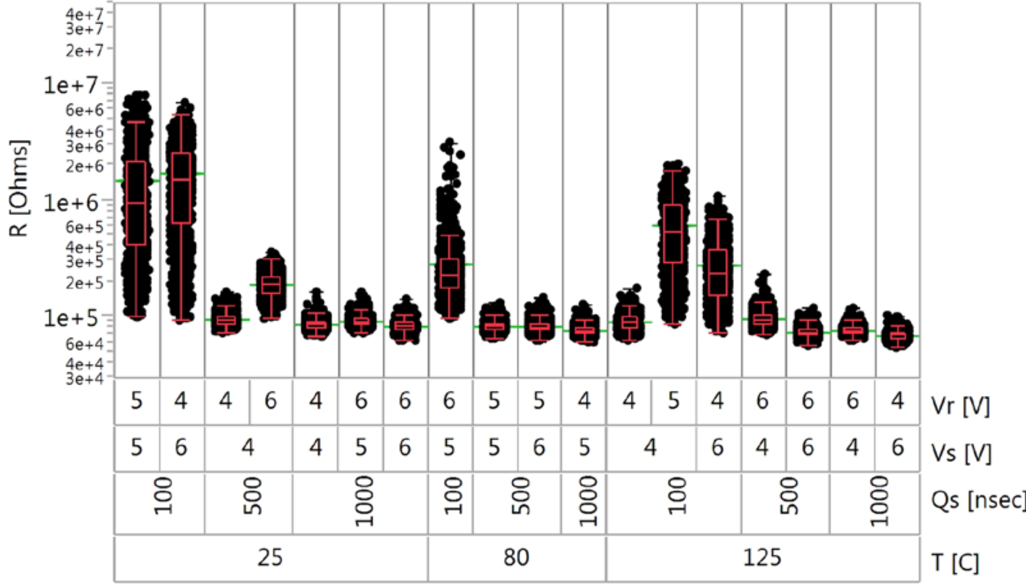

Figure 4.6 Variability plot of the SET state cell resistance for DOE 1 going from RESET to SET state for the given pulse sequence and temperatures.

Since the crystallization process must be active to reduce the amorphous volume size, the crystallization dynamics requires a longer programming duration [25]. It is clear that for optimal programming conditions for the SET state, quench times longer than 100 nsec are needed to fully crystallize the amorphous cap (created by the RESET pulse) and/or create a complete crystalline path between the top electrode and the heater element for the majority of the bits.

When performing the least means squares analysis for the SET state, the median resistance values for each of the test sequences from DOE 1 were calculated similar to the RESET state resistance values, which are shown in Figure 4.7.

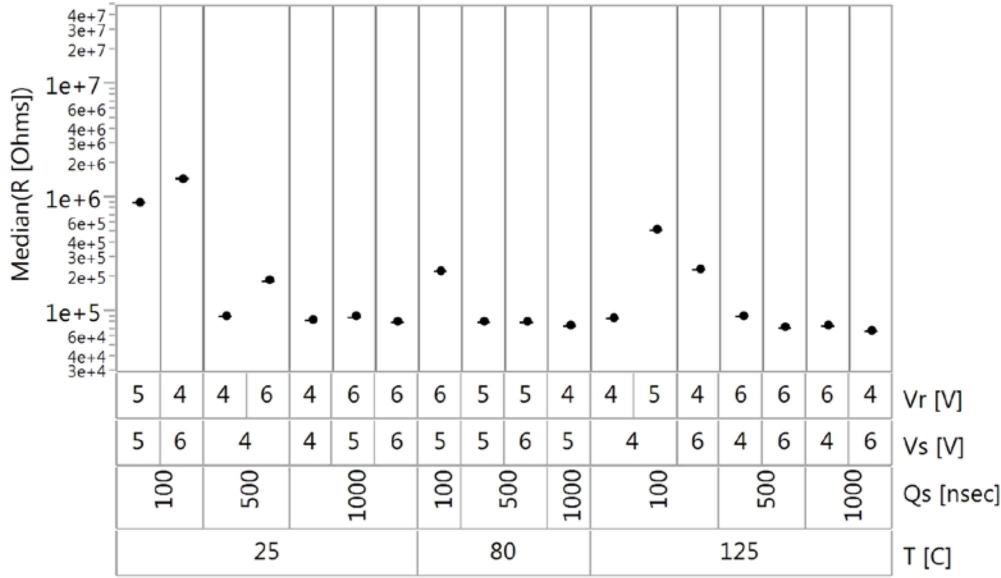

Figure 4.7 Variability plot of the median resistance values for the SET state of DOE 1 used for prediction profiler in JMP.

The significance of the SET quench time (Q_s) is also shown in the parameter estimates in Figure 4.8, where the three most significant parameters are Q_s, T, and the combination of Q_s.

Term	Estimate	Std Error	t Ratio	Prob >|t|
Qs [nsec]	1.08E-08	1.15E-09	9.39	<.0001*
T [C]	4.57E-08	9.48E-09	4.83	0.0005*
(Qs [nsec]-533)*(Qs [nsec]-533)	-1.59E-11	4.48E-12	-3.55	0.0045*
(Vr [V]-5.00)*(Vs [V]-4.94)	1.91E-06	5.38E-07	3.55	0.0046*
Vr [V]	-7.08E-07	4.81E-07	-1.47	0.1689
Vs [V]	3.49E-07	4.79E-07	0.73	0.4809

Figure 4.8 Parameter estimates for the SET state of DOE 1.

In should be noted that due to the residuals not being normally distributed when performing the linear regression analysis (without a transformation for SET resistance model), to obtain an accurate model for the SET state of DOE 1, a transformation of the SET state cell resistance values had to be performed prior to the regression analysis. The reciprocal transformation of the SET state cell resistance values was found to have the

best fit and a normal distribution for the residuals. From the parameter point estimates in Figure 4.8, the SET model equation was generated and is shown in Equation 4.5.

$$R_{SET_DOE1} = 1/(3.80 * 10^{-6} + 1.08 * 10^{-8} * (Q_s) + 4.57 * 10^{-8} * (T) - 1.59 * 10^{-11} * (Q_s - 533)^2 + 1.91 * 10^{-6} * \left((V_r - 5.00) * (V_s - 4.94)\right) - 7.08 * 10^{-7} * (V_r) + 3.49 * 10^{-7} * (V_s)), \quad (4.5)$$

Looking into the surface plot and contour plots of the SET state for Q_s vs. T (shown in Figure 4.9), one can see that the direction of minimal cell resistance is in the direction of longer Q_s times and higher T, with the largest drop in the cell resistance of the SET state taking place between 100-200 nsec for Q_s.

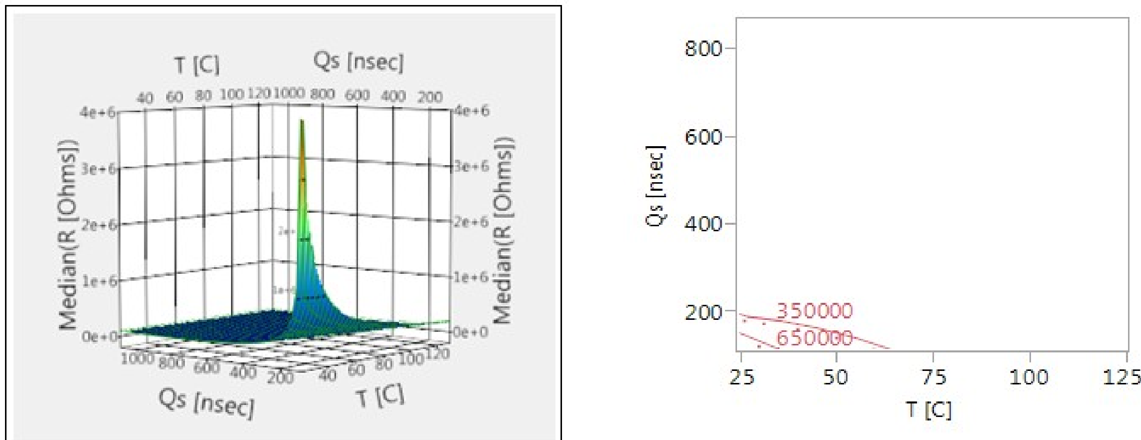

Figure 4.9 DOE 1: Left: Surface Plot of the SET state cell resistance response; Right: Contour plot of SET state cell resistance response.

This spike in the cell resistance at T =25 °C and Q_s =100 nsec is related to the SET pulse behaving like a RESET pulse, not allowing the chalcogenide material enough time to crystallize at lower ambient temperatures. This failure to crystallize is due to the speed of the quench, causing the majority of the bits to be placed in a partially RESET state, as discussed previously.

When looking at the programming window results from DOE 1 (shown in Table 4.2), the largest programming window exists at: $T = 25$ °C, $V_r = 6$ V, $V_s = 5$ V, and $Q_s =$ 1000 nsec, which aligns with the highest RESET resistance values. For both the RESET and SET median resistance, the resistance is reduced for higher temperatures. This is more apparent for the RESET state, because of the temperature dependence of the amorphous film as mentioned in Chapter 2 and Section 3.1.3.

Table 4.2 DOE 1: Resistance values for SET and RESET states by pulse conditions and Temperature.

T [°C]	*Vr* [V]	*Vs* [V]	*Qs* [nsec]	RESET: Median (R [Ohms])	SET: Median (R [Ohms])
25	4	4	1000	1.24E+06	8.65E+04
25	4	4	500	1.07E+06	9.41E+04
25	4	6	100	9.16E+05	1.52E+06
25	5	5	100	9.23E+06	9.38E+05
25	6	4	500	1.00E+07	1.91E+05
25	6	6	1000	1.00E+07	8.36E+04
25	6	5	1000	1.09E+07	9.17E+04
80	4	5	1000	5.69E+05	7.66E+04
80	5	5	500	3.43E+06	8.30E+04
80	5	6	500	3.33E+06	8.29E+04
80	6	5	100	3.75E+06	2.33E+05
125	4	4	100	3.64E+05	8.91E+04
125	5	4	100	1.64E+06	5.33E+05
125	6	4	1000	2.00E+06	7.68E+04
125	6	4	500	1.97E+06	9.41E+04
125	6	6	500	2.00E+06	7.39E+04
125	4	6	100	3.90E+05	2.41E+05
125	4	6	1000	3.60E+05	6.94E+04

4.1.3 DOE 2

4.1.3.1 DOE 2 RESET State Analysis

The results from DOE 1 led to the next designed experiment (DOE 2), described in Table 4.3. For DOE 2, the goal was to better understand the response of the RESET

voltage pulse amplitude (V_r) and the SET quench (Q_s) times pulse variables, which were found to be more significant to the overall cell resistance for the RESET and SET states, respectively. To understand these variables better, the window of values used for the design space of DOE 2 were adjusted, and the SET voltage (V_s) was held at 6 V. From DOE 1, it was apparent that $V_r = 4$ V is not sufficient to fully RESET the array of bits and that $Q_s = 100$ nsec for the SET pulse is not long enough to fully SET the array of bits. To account for this, the design space in DOE 2 was as follows: 1) *T,* ranged from 25 to 125 °C, 2) V_r, ranged from 5V to 6V, and 3) Q_s, ranged from 500 nsec to 1500 nsec.

Table 4.3 DOE 2 matrix of parameters.

T [°C]	*Vr* [V]	*Vs* [V]	*Qs* [nsec]	TEST_Sequence
25	5.5	6	1000	1
25	5.5	6	500	2
25	5.5	6	1500	3
25	5	6	1500	4
25	6	6	500	5
25	6	6	1000	6
25	6	6	1000	7
80	5.5	6	1000	8
80	5	6	500	9
80	5	6	500	10
80	6	6	1500	11
125	5.5	6	1500	12
125	5	6	1500	13
125	6	6	1000	14
125	6	6	500	15
125	6	6	500	16
125	5.5	6	1500	17
125	5.5	6	1000	18

In Figure 4.10, the cell resistances going from a SET to RESET state are shown in the variability plot, which is grouped by the pulse condition variables and temperature used in DOE 2. From Figure 4.10, it is apparent that the ambient temperature change

from 25 to 125 °C is causing a significant shift in the cell resistance; the overall cell resistance lowers as the ambient temperature increases. Moreover, it should be mentioned that due to the design window change of the RESET voltage pulse (V_r) amplitude increasing from 4 V to 5 V, the significance of the RESET voltage becomes less apparent. Hence, the ambient temperature plays a more significant role in the cell resistance for the RESET state of DOE 2, as was expected due to the sensitivity of the amorphous *GST* material to temperature.

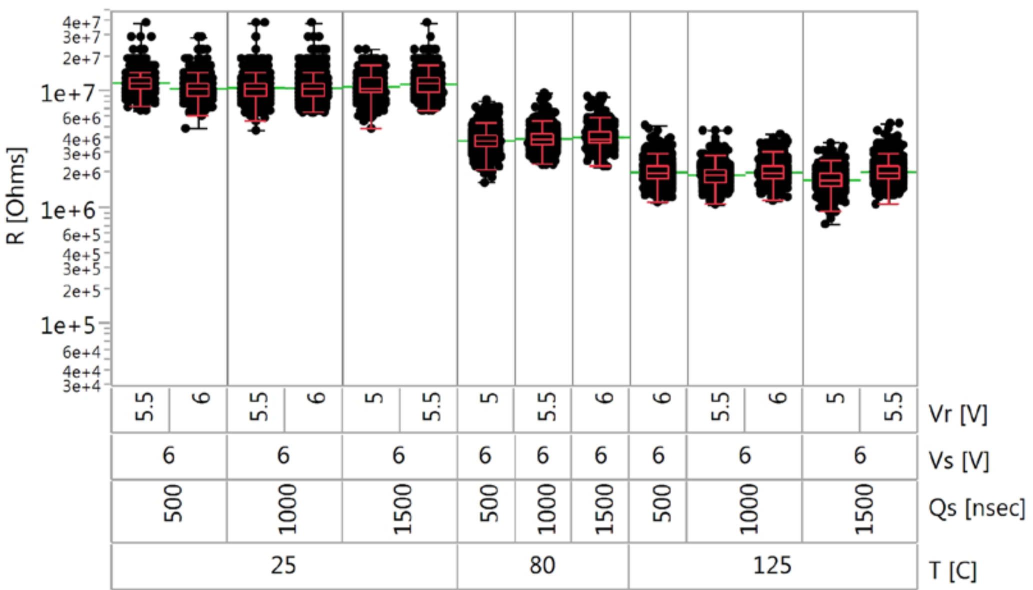

Figure 4.10 Variability plot of RESET state cell resistance for DOE 2 going from SET to RESET state for the given pulse sequence and temperature.

For DOE 2, the same method discussed for DOE 1 was used, in which the median cell resistance values were calculated prior to performing the least squares regression due to memory errors in JMP. In Figure 4.11, the cell resistance values for the RESET state of DOE 2 are shown in the variability graph. From the median resistance values collected in DOE 2, it can be seen that due to the change in the design space for V_r, V_s, and Q_s, the significant variable for the RESET state for DOE 2 is now the temperature (T), which is

showing an almost staircase-like drop in the RESET cell resistance as the ambient temperature increases.

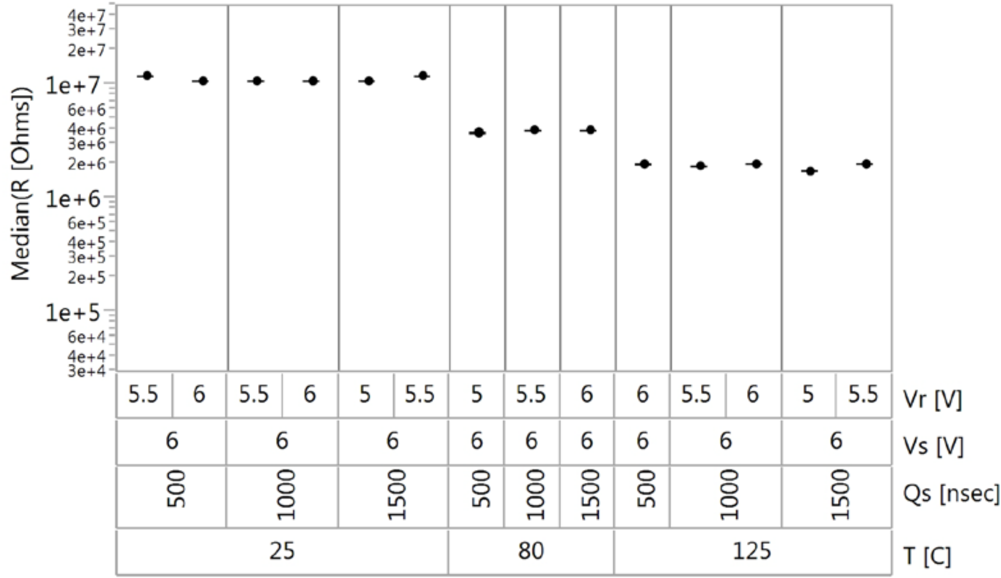

Figure 4.11 Variability plot of the median resistance values for the RESET state of DOE 2 used for prediction profiler in JMP.

The significance of the temperature can also be seen in the parameter estimates, which show *T*, and the combination of *T,* as the two most significant parameters for the RESET state (shown in Figure 4.12). However, it should also be noted that the combinations of V_r and *T* with V_r are the third and fourth most significant parameters, meaning that with the window of RESET voltages being tightened closer to the optimal pulse conditions, the interaction of V_r and *T* is now more significant than the single parameter of V_r.

Term	Estimate	Std Error	t Ratio	Prob >|t|
T [C]	-1.74E-02	1.38E-04	-126	<.0001*
(T [C]-76.1)*(T [C]-76.1)	2.92E-05	6.20E-06	4.71	0.0008*
(Vr [V]-5.58)*(Vr [V]-5.58)	-2.34E-01	5.25E-02	-4.46	0.0012*
(T [C]-76.1)*(Vr [V]-5.58)	1.23E-03	3.85E-04	3.21	0.0095*
(Qs [nsec]-1.00E+3)*(Qs [nsec]-1.00E+3)	1.29E-07	5.48E-08	2.36	0.0402*
Vr [V]	3.25E-02	1.78E-02	1.82	0.0986
Qs [nsec]	-1.74E-06	1.54E-05	-0.11	0.9124

Figure 4.12 Parameter estimates for the RESET state of DOE 2.

In order to get the point estimates shown in Figure 4.12, a transformation of the RESET cell resistance had to be performed. Due to the significant temperature dependence of the RESET state of DOE 2, a transformation was needed; the residuals without the transformation were not found to be normal, and for this reason a log transformation of the RESET state cell resistance was used and found to have the best fit with a normal distribution for the residuals. From the parameter point estimates in Figure 4.12, the RESET model equation was generated, which is shown in Equation 4.6.

$$R_{RESET_DOE2} = exp(16.4 - 1.74 * 10^{-2} * (T) + 2.92 * 10^{-5} * (T - 76.1)^2 - 2.34 * 10^{-1} * (V_r - 5.58)^2 + 1.23 * 10^{-3} * \left((T - 76.1) * (V_r - 5.58)\right) + 1.29 * 10^{-7} * (Q_s - 1.00 * 10^3)^2 + 3.25 * 10^{-2} * (V_r) - 1.74 * 10^{-6} * (Q_s)), \quad (4.6)$$

From Equation 4.6, the surface and contour plots of the RESET cell resistance vs. the two most significant single variables T and V_r is shown in Figure 4.13. In the surface plot, the direction of increased resistance again in the direction of lower T; however, this time the V_r is not playing much of a role in the effect of the RESET state cell resistance. This change is due to the values of V_r used in the design space window being between 5 and 6 V, showing the RESET cell resistance to be overall fairly aligned within this design space.

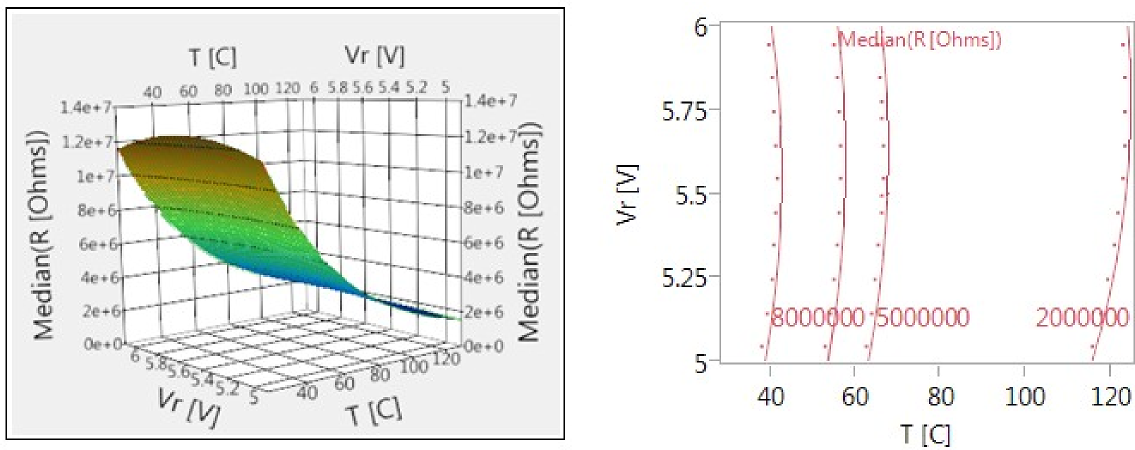

Figure 4.13 Surface Plot for the RESET state of DOE 2.

4.1.3.2 DOE 2 SET State Analysis

For the SET state cell resistance of DOE 2, shown in the variability plot of Figure 4.14, by changing the lower limit of the design space window for Q_s from 100 nsec to 500 nsec, the significance of Q_s on the SET state cell resistance is reduced. Moreover, from DOE 2 it is apparent that 500 nsec for the minimum value of Q_s appears to be sufficiently long enough to crystallize the active area or amorphous chalcogenide *GST* cap and/or create a complete crystalline path between the top electrode and the heater element. As a result, there was very little change seen in SET state cell resistance distributions between the different test sequences performed in DOE 2.

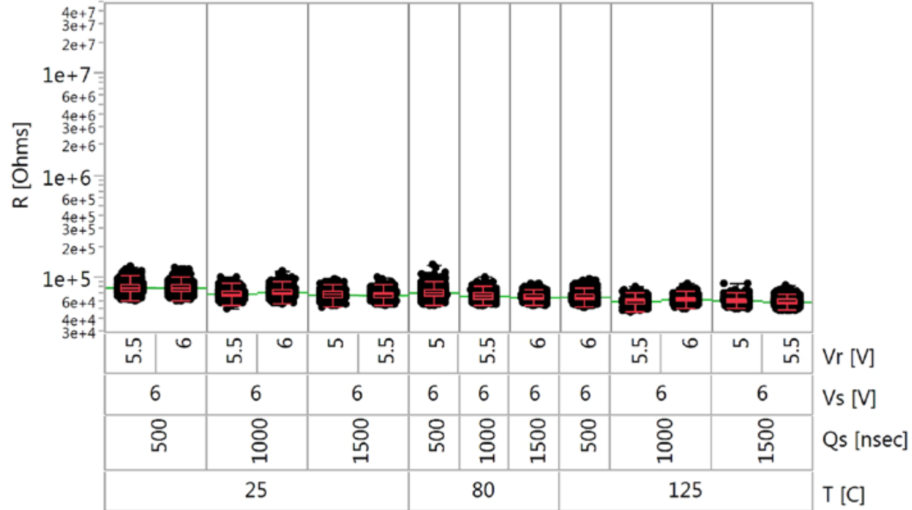

Figure 4.14 Variability plot of the SET state cell resistance for DOE 2, going from RESET to SET state for the given pulse sequence and temperatures.

For the SET state of DOE 2, the median cell resistances were again calculated prior to performing the regression analysis. The variability plot of the SET state cell resistances are shown in Figure 4.15.

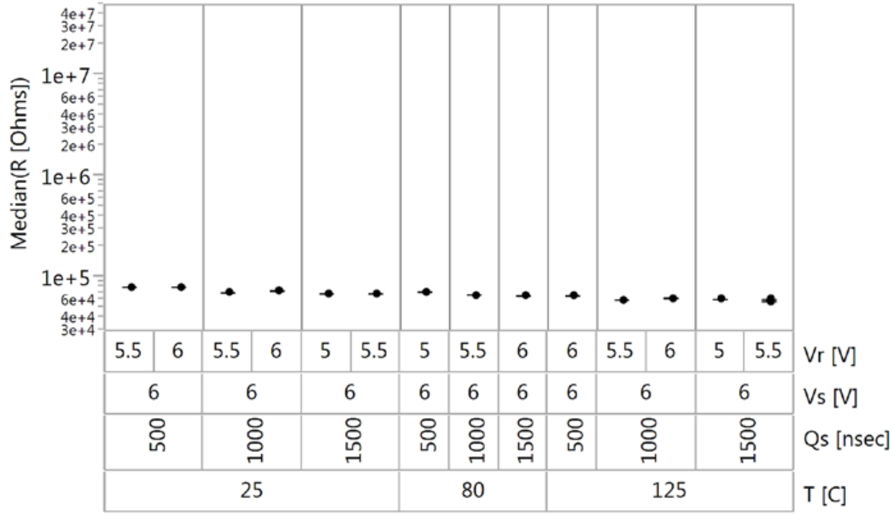

Figure 4.15 Variability plot of the median resistance values for the SET state of DOE2 used for prediction profiler in JMP.

After performing the least means squares analysis on the SET state for DOE 2, multiple parameter estimates were found to be statistically significant; T, Q_s, and the

combination of T and Q_s were the most significant parameters, as was found in DOE 1. The only notable change between DOE 1 and DOE 2 was the set of interaction terms, as shown in parameter estimate table in Figure 4.16.

Term	Estimate	Std Error	t Ratio	Prob >|t|
T [C]	-1.19E+02	5.73E+00	-20.8	<.0001*
Qs [nsec]	-7.88E+00	6.43E-01	-12.3	<.0001*
(T [C]-76.1)*(Qs [nsec]-1.00E+3)	6.27E-02	1.47E-02	4.25	0.0014*
(Qs [nsec]-1.00E+3)*(Qs [nsec]-1.00E+3)	7.26E-03	2.31E-03	3.14	0.0094*
(Vr [V]-5.58)*(Vr [V]-5.58)	5.02E+03	2.27E+03	2.21	0.0493*
Vr [V]	1.56E+03	7.41E+02	2.11	0.0587

Figure 4.16 Parameter estimates for the SET state of DOE 2.

From the point estimate values in Figure 4.16, the SET model equation was generated, as shown in Equation 4.7.

$$R_{SET_DOE2} = 7.52 * 10^4 - 119 * T - 7.88 * Q_s + 6.27 * 10^{-2} * \big((T - 76.1) * (Q_s - 1.00 * 10^3)\big) + 7.26 * 10^{-3} * (Q_s - 1.00 * 10^3)^2 + 5.02 * 10^3 * (V_r - 5.58)^2 + 1.56 * 10^3 * (V_r), \quad (4.7)$$

From Equation 4.7, the surface and contour plot of the SET cell resistance vs. the two most significant variables (T and Q_s) is shown in Figure 4.17. In the surface plot, very little information is gathered, due to the change in the design space window of Q_s from 100 -1000 nsec to 500 – 1500 nsec, which shows no sudden increase in cell resistance, as expected. Moreover, only a slight resistance and color change in the surface plot is detectable. From this slight color change in the surface model and contours of the cell resistance in the contour plot (show in Figure 4.17, right), one can see that the direction of minimum cell resistance for the SET state of DOE 2 is in the direction of higher T and longer Q_s as shown in DOE 1.

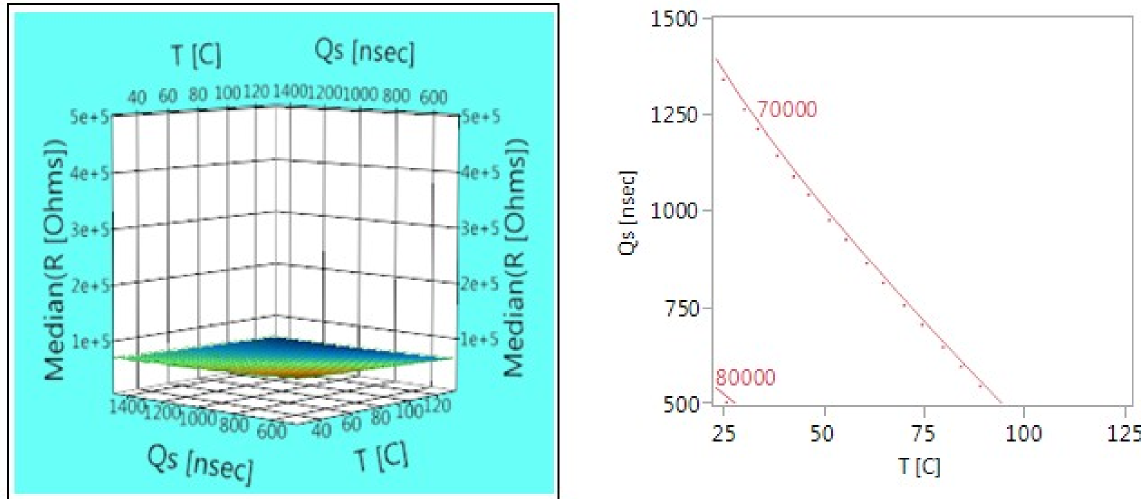

Figure 4.17 Surface Plot for the SET state of DOE 2.

The median cell resistance values from the different test sequences of DOE 2 are shown in Table 4.4. From the median cell values, the largest separation or reading window of median resistance values from DOE 2, exists at: T = 25 °C, V_r = 5.5 V, V_s = 6 V, and Q_s = 1500 nsec, which aligns with the highest RESET resistance values for DOE 2. Moreover, for both the RESET and SET median resistance, the resistance again is reduced for higher temperatures as was shown in DOE 1.

Table 4.4 DOE 2: Resistance values for SET and RESET states by pulse conditions and Temperature.

T [°C]	V_r [V]	V_s [V]	Q_s [nsec]	RESET: Median (R [Ohms])	SET: Median (R [Ohms])
25	5.5	6	1000	1.09E+07	7.16E+04
25	5.5	6	500	1.20E+07	8.11E+04
25	5.5	6	1500	1.20E+07	6.98E+04
25	5	6	1500	1.09E+07	6.98E+04
25	6	6	500	1.09E+07	8.16E+04
25	6	6	1000	1.09E+07	7.42E+04
25	6	6	1000	1.09E+07	7.45E+04
80	5.5	6	1000	4.00E+06	6.81E+04
80	5	6	500	3.75E+06	7.32E+04
80	5	6	500	3.87E+06	7.28E+04
80	6	6	1500	4.00E+06	6.67E+04

125	5.5	6	1500	2.03E+06	6.12E+04
125	5	6	1500	1.77E+06	6.16E+04
125	6	6	1000	2.03E+06	6.33E+04
125	6	6	500	2.00E+06	6.67E+04
125	6	6	500	2.03E+06	6.65E+04
125	5.5	6	1500	2.03E+06	5.85E+04
125	5.5	6	1000	1.94E+06	6.05E+04

4.1.4 DOE 3

4.1.4.1 DOE 3 RESET State Analysis

The results from DOE 1 and DOE 2 led to the next designed experiment DOE 3, shown in Table 4.5. The goal for DOE 3 was to reduce the design space window for T, which was found to be the dominant variable in DOE 2 for the RESET cell resistance response. Moreover, the SET voltage (V_s) pulse amplitude is adjusted once again to see if a larger response could be generated. DOE 3 takes into account low, medium, and high values for: 1) T, ranging from 50 to 90 °C, 2) V_r, ranging from 5 V to 6 V, 3) V_s, ranging from 4.5 V to 6 V, and 4) Slope/Quench Time ranging from 500 nsec to 1500 nsec for the SET pulse.

Table 4.5 DOE 3 matrix of parameters

T [°C]	V_r [V]	V_s [V]	Q_s [nsec]	TEST_Sequence
50	5.5	4.5	1000	1
50	5.5	4.5	500	2
50	5.5	6	1500	3
50	5	5.5	1500	4
50	6	4.5	500	5
50	6	6	1000	6
50	6	5.5	1000	7
70	5.5	5.5	1000	8
70	5	5.5	500	9
70	5	6	500	10
70	6	5.5	1500	11
90	5.5	4.5	1500	12
90	5	4.5	1500	13

90	6	4.5	1000	14
90	6	4.5	500	15
90	6	6	500	16
90	5.5	6	1500	17
90	5.5	6	1000	18

In Figure 4.18, the results from DOE 3 going from a SET to RESET state are shown in the variability plot, which is broken apart into the given test sequences from DOE 3. From Figure 4.18, it is apparent that the ambient temperature change between 50 and 70 °C shows a significant difference in the cell resistance; the overall cell resistance is lowered as the ambient temperature increases. It should also be noted that it appears that the probe pins during testing may have had marginal contact during test sequence #11 (T = 70 °C, V_r=6 V, V_s= 5.5 V, and Qs= 1500 nsec) due to the bi-modal distribution of bits shown with the RESET voltage at 6 V.

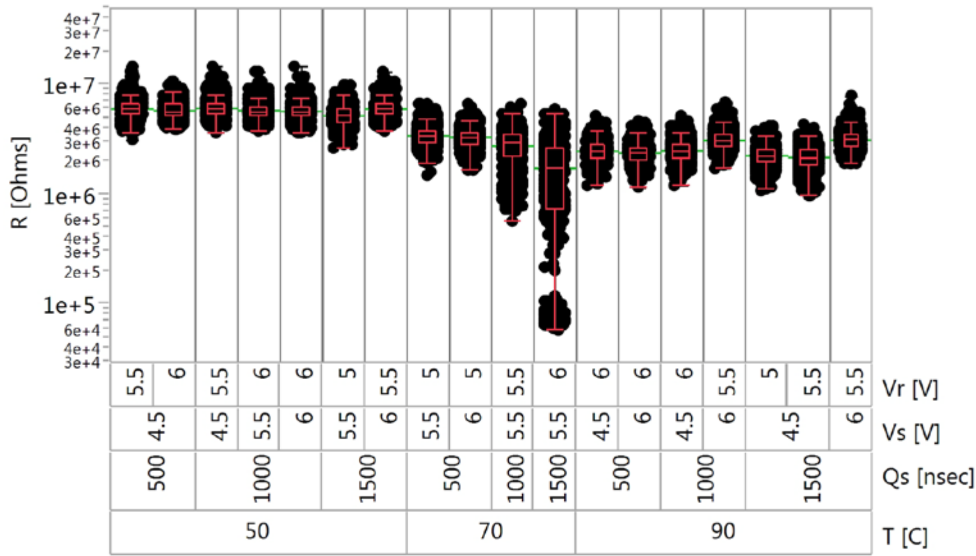

Figure 4.18 Variability plot of the RESET state cell resistance of DOE 3, going from SET to RESET state for the given pulse sequence and temperature.

The median resistance values were generated in the same method in DOE 3, as was done in the prior DOEs 1 and 2. The median cell resistance for the RESET state is shown in Figure 4.19.

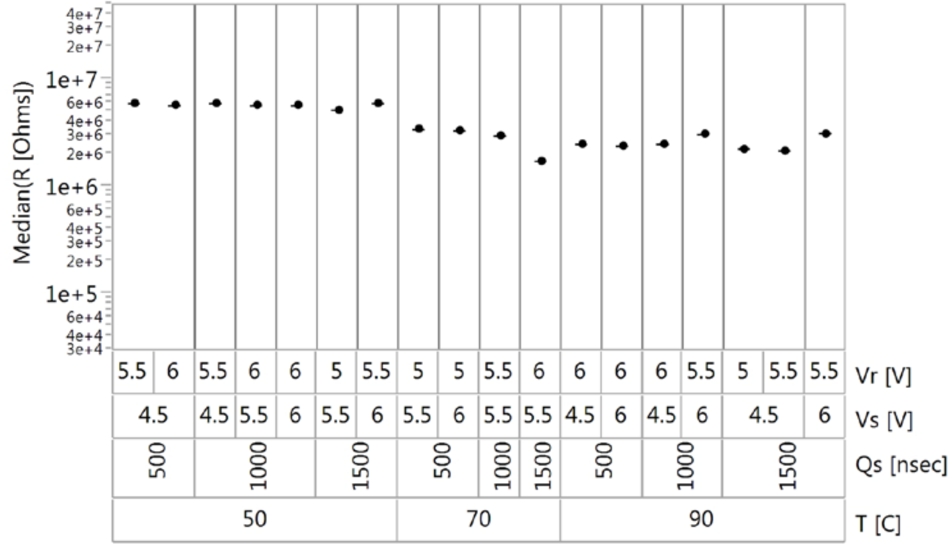

Figure 4.19 Variability plot of the median resistance values for the RESET state of DOE 3, which were used for prediction profiler in JMP.

With the reduced temperature, the staircase-like effect was not as apparent as it was in DOE2. However, the most significant variables for the RESET state of DOE 3 were still found to be *T*, combination of *T*, and Q_s as shown in Figure 4.20, which was somewhat unexpected since the SET quench time (Q_s) had not shown up as one of the top three significant variables for the RESET state in DOE 1 or 2. However, due to the lower median resistance from the bi-model distribution in test sequence #11, it appears that this lowering of the median resistance has caused increased significance of Q_s.

Term	Estimate	Std Error	t Ratio	Prob >|t|
T [C]	-7.79E+04	3.99E+03	-19.51	<.0001*
(T [C]-70.0)*(T [C]-70.0)	3.89E+03	4.81E+02	8.11	<.0001*
Qs [nsec]	-7.20E+02	1.86E+02	-3.86	0.0026*
Vr [V]	-7.10E+05	2.08E+05	-3.41	0.0058*
(Vr [V]-5.58)*(Vr [V]-5.58)	-1.69E+06	6.12E+05	-2.76	0.0185*
Vs [V]	2.32E+05	1.14E+05	2.03	0.0668

Figure 4.20 Parameter estimates for the RESET state of DOE 3.

From the point estimate values in Figure 4.20, the RESET model equation was generated and is shown in Equation 4.8.

$$R_{RESET_DOE3} = 1.18 * 10^{7} - 7.79 * 10^{4} * (T) + 3.89 * 10^{3} * (T - 70.0)^{2} - 720 * Q_{s} - 7.10 * 10^{5} * V_{r} - 1.69 * 10^{6} * (V_{r} - 5.58)^{2} + 2.32 * 10^{5} * (V_{s}), \quad (4.8)$$

Using the RESET model Equation 4.8, the surface and contour plots of the RESET cell resistance vs. *T* and V_r for DOE 3 is shown in Figure 4.21. In the surface plot, the RESET state cell resistance is increasing in the direction of lower *T*, with the maximum median cell resistance at ~5.5 V for V_r, similar to what was seen in DOE 2.

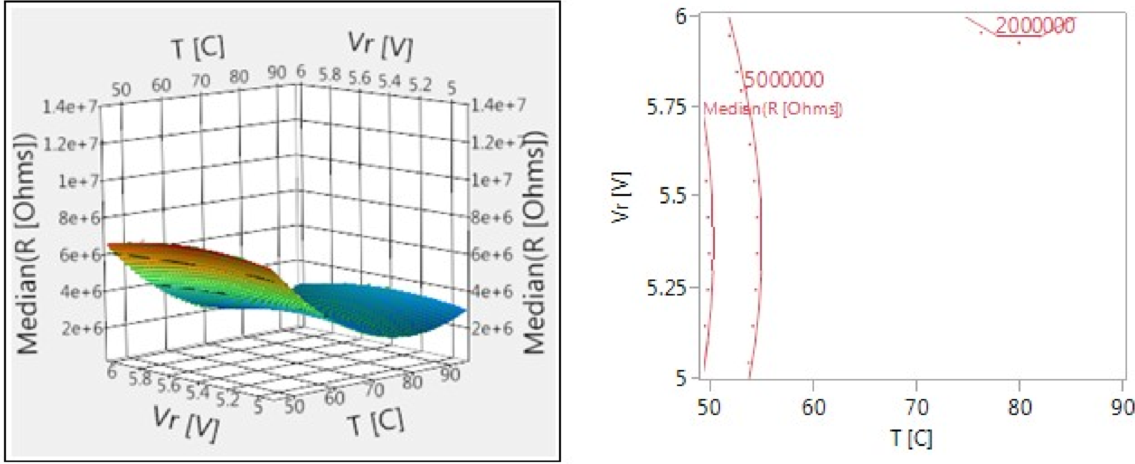

Figure 4.21 Surface Plot for the RESET state of DOE 3.

4.1.4.2 DOE 3 SET Regression Analysis

For the variability plot of the SET state cell resistance (shown in Figure 4.22), by adjusting the design space window of the ambient temperature from 25 to 125 °C to 50 to 90 °C, again no significant SET state cell resistance differences are seen.

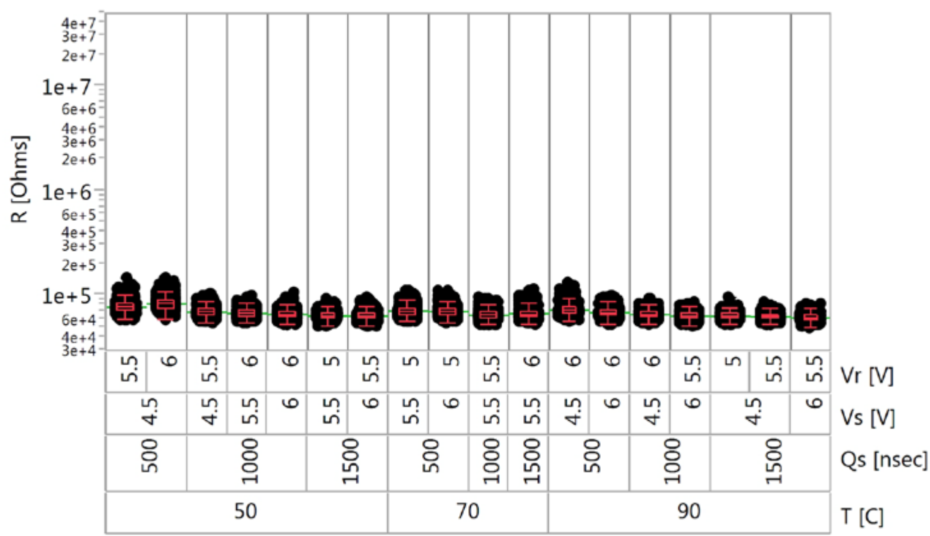

Figure 4.22 Variability plot of the SET state cell resistance of DOE 3, going from RESET to SET state for the given pulse sequence and temperatures.

For the SET state cell resistance, the variability graph of the median resistance values from DOE 3 are shown in Figure 4.23.

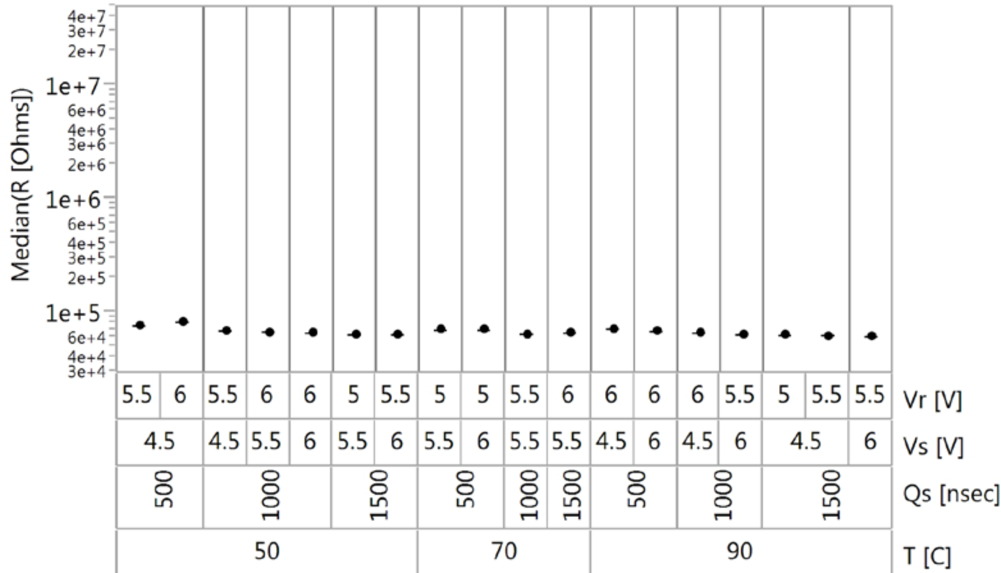

Figure 4.23 Variability plot of the median resistance values for the SET state of DOE 3, which were used for prediction profiler in JMP.

From the parameter estimates shown in Figure 4.24, the top three significant variables were found to be the SET quench time (Q_s), Temperature (T), and the combination of Q_s, in terms of the response of the cell resistance in the SET state among the variables.

Term	Estimate	Std Error	t Ratio	Prob >|t|
Qs [nsec]	-8.94E+00	8.91E-01	-10.1	<.0001*
T [C]	-1.19E+02	2.03E+01	-5.88	0.0001*
(Qs [nsec]-1.00E+3)*(Qs [nsec]-1.00E+3)	1.28E-02	3.19E-03	4.02	0.002*
Vs [V]	-2.04E+03	6.05E+02	-3.38	0.0062*
Vr [V]	2.76E+03	1.00E+03	2.75	0.019*
(T [C]-70.0)*(Qs [nsec]-1.00E+3)	1.39E-01	5.58E-02	2.48	0.0303*

Figure 4.24 Parameter estimates for the SET state of DOE 3.

Using the point estimate values shown in Figure 4.24, the creation of the SET model Equation 4.9 was generated.

$R_{SET_DOE3} = 7.88 * 10^4 - 8.94 * Q_s - 119 * T + 1.28 * 10^{-2} * (Q_s - 1.00 *$

$$10^3)^2 - 2.04 * 10^3 * (V_s) + 2.76 * 10^3 * (V_r) + 1.39 * 10^{-1} * ((T - 70.0) * (Q_s - 1.00 * 10^3)), \quad (4.9)$$

Using Equation 4.9, surface and contour plots of the SET state cell resistance vs. the two most significant variables (*T* and Q_s) for DOE 3 are shown in Figure 4.25. In the surface plot for the SET state cell resistance, similar to DOE 2, very little information is gained from the surface plot due to the tight resistance distribution between the different test sequences; the optimal SET pulse condition is in the direction of minimal cell resistance for the SET state, which is in the direction of higher *T* and higher Q_s as was seen for DOEs 1 and 2.

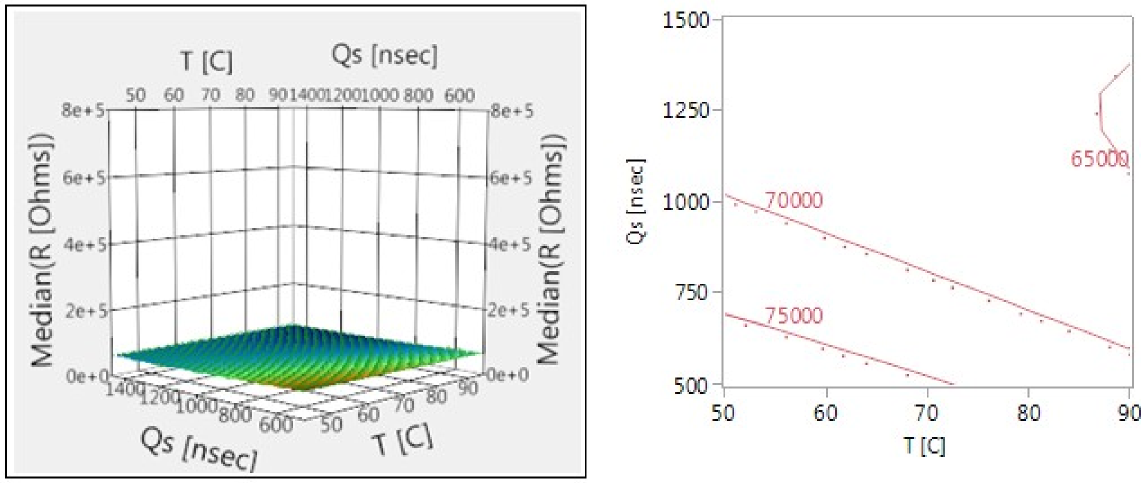

Figure 4.25 Surface Plot for the SET state of DOE 3.

The median resistance results from DOE3 are shown in Table 4.6. When looking at the programming window results from DOE 3, the largest programming window exists at: $T = 50$ °C, $V_r = 5.5$ V, $V_s = 6$ V, and $Q_s = 1500$ nsec, which again aligns with the highest RESET resistance values from DOE 3.

Table 4.6 DOE 3: Resistance values for SET and RESET states by pulse conditions and Temperature.

T [°C]	*Vr* [V]	*Vs* [V]	*Qs* [nsec]	RESET: Median (R [Ohms])	SET: Median (R [Ohms])
50	5.5	4.5	1000	6.00E+06	6.99E+04
50	5.5	4.5	500	6.00E+06	7.78E+04
50	5.5	6	1500	6.00E+06	6.42E+04
50	5	5.5	1500	5.22E+06	6.46E+04
50	6	4.5	500	5.71E+06	8.31E+04
50	6	6	1000	5.71E+06	6.67E+04
50	6	5.5	1000	5.71E+06	6.82E+04
70	5.5	5.5	1000	3.00E+06	6.54E+04
70	5	5.5	500	3.43E+06	7.10E+04
70	5	6	500	3.33E+06	7.08E+04
70	6	5.5	1500	1.74E+06	6.64E+04
90	5.5	4.5	1500	2.18E+06	6.34E+04
90	5	4.5	1500	2.26E+06	6.40E+04
90	6	4.5	1000	2.50E+06	6.66E+04
90	6	4.5	500	2.50E+06	7.27E+04
90	6	6	500	2.40E+06	6.88E+04
90	5.5	6	1500	3.16E+06	6.21E+04
90	5.5	6	1000	3.08E+06	6.45E+04

4.1.5 Optimal Pulse Conditions

Using results from DOEs 1, 2, and 3, the design space between each of the DOEs was changed slightly to see if the response within the overlapping areas of each design space showed similar response trends. The condensed minimum and maximum parameters used for T, V_r, V_s, and Q_s are shown in Table 4.7.

Table 4.7 DOE 1, 2, 3: Design Space Max and Min parameters values used for T, V_r, V_s, and Q_s.

T [°C] (Min/Max)	*Vr* [V] (Min/Max)	*Vs* [V] (Min/Max)	*Qs* [nsec] (Min/Max)	DOE
25/125	4/6	4/6	100/1000	1
25/125	5/6	6	500/1500	2
50/90	5/6	4.5/6	500/1500	3

To validate the optimal condition model from DOEs 1, 2, and 3, an independent wafer was measured at a T between 25 and 125 °C, with voltage values between 4 and 6 V for V_r and V_s, and Q_s from 100 to 1000 nsec. For the independent wafer measurements, a single checkerboard cycle instead of 10 seasoning cycles was used to see how DOEs 1, 2, and 3 performed with the independent wafer with a single programming pulse. After reviewing each of the RESET models from DOEs 1, 2, and 3, DOE 1 was found to have the best fit of the three models. As shown in Figure 4.26, the model was found to respond well to the data collected from the independent wafer, showing the largest variation at T = 125 °C, V_s = 5 V, V_r = 5 V, and Q_s = 550, which is a center point for the model.

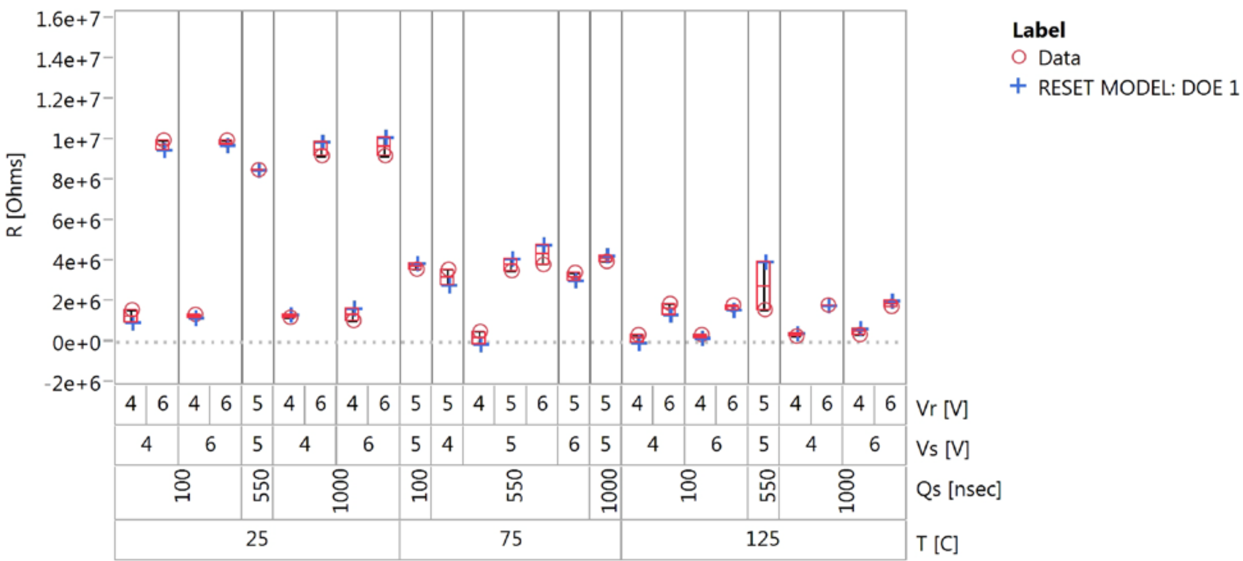

Figure 4.26 Variability plot of the RESET model vs. data collected from an independent wafer.

Similarly to the RESET model vs. independent wafer, the SET model from DOE 1 vs. independent wafer also responded very well to the data collected. The largest variation between the SET model and the independent wafer was seen at T = 25 °C, for Q_s = 100 nsec, and V_s of 4V, as shown in Figure 4.26.

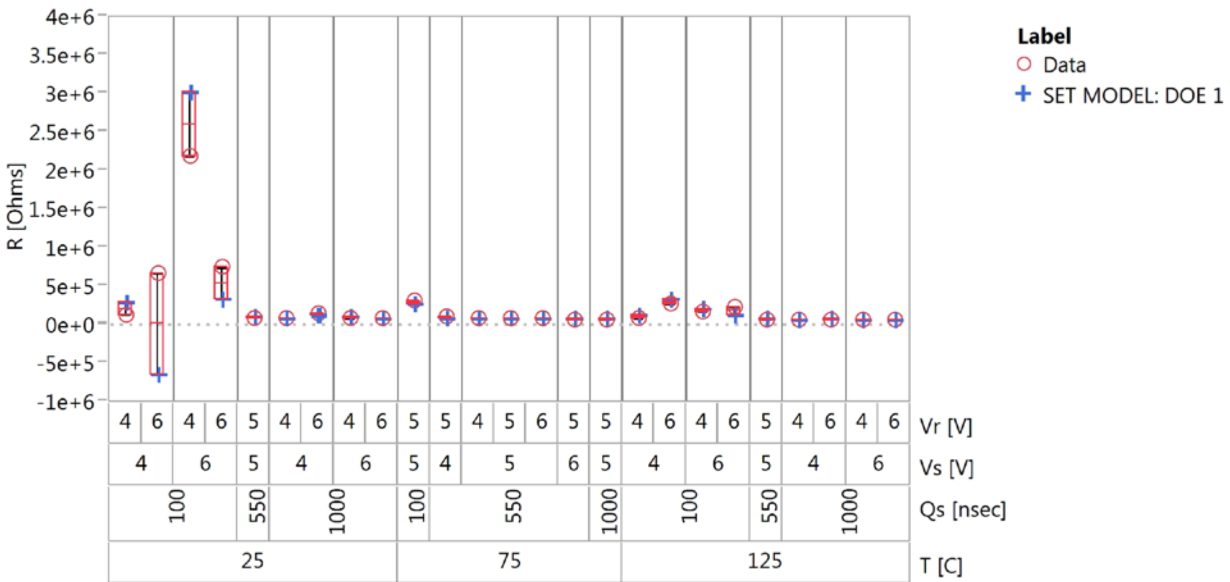

Figure 4.27 Variability plot of the SET model vs. data collected from an independent wafer.

From the results collected in DOEs 1, 2, and 3, only DOE 1 was examined when considering the optimal pulse conditions for the Micron/Numonyx *PCRAM* experimental wafers, considering that it is the only DOE that covers the design window of temperature and pulse conditions for the test. As shown in the variability plot in Figure 4.26, in the design space window for each of the DOEs, the predicted results align with the data collected on the independent wafer. However, for values outside the design window for DOEs 2 and 3, the prediction is no longer accurate. This can be seen best in the predictions of DOE 3 at T = 25 °C and 125 °C (which are outside of the design space window for the DOE). At these two temperatures, the model equation from DOE 3 is not able to accurately predict the response, and the values predicted are completely different than the actual response from the independent wafer. However, it should be noted that at T =50 °C, the prediction of DOE 3 is very close to the other predictions from DOEs 1 and 2, as shown in Figure 4.26.

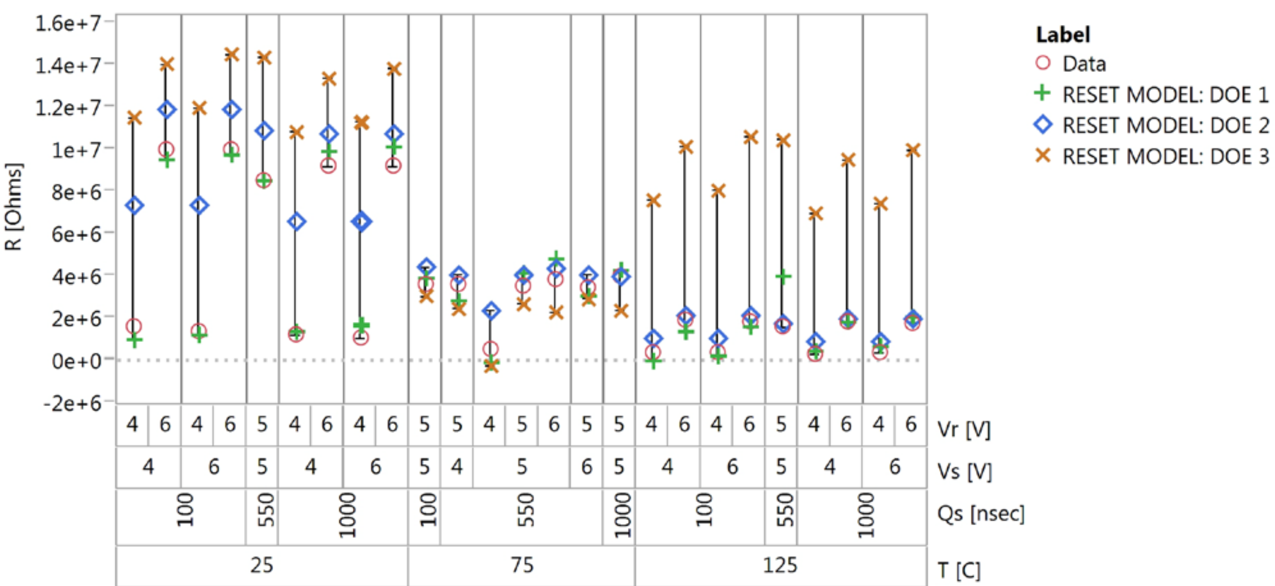

Figure 4.26 Variability plot of RESET models equations from DOEs 1, 2, and 3 vs. data collected from an independent wafer.

After concluding that DOE 1 was the best fit for the overall design space, the next step was to determine the optimal programming pulse for the both the RESET and SET states. In determining the optimal programming pulse conditions, a dynamic prediction profiler was used in JMP. Profiling is an approach to visualizing the regression response by seeing what would happen if you changed just one or two factors at a time. Essentially, a profile is a cross-section view of the least squares regression response of each of the variables used in the analysis. JMP's statistical software contains an interactive profiler, allowing dynamic profiling as the user drags the cursor along the response lines (shown in Figure 4.27). This dynamic profiling is very useful in determining the optimal conditions for a given temperature.

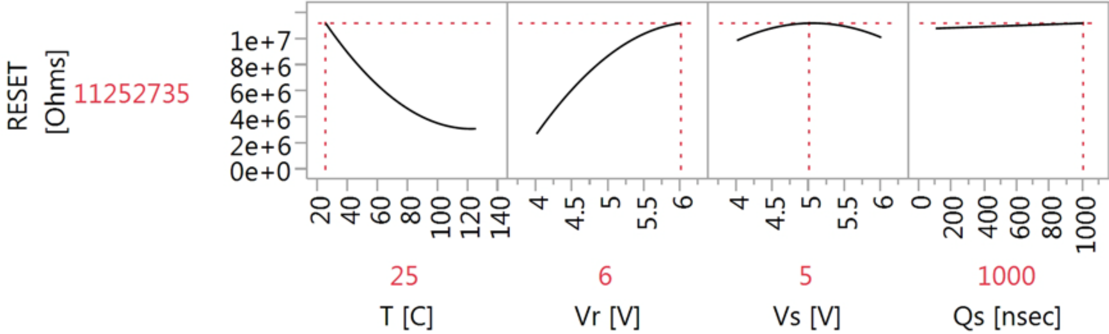

Figure 4.27 Prediction Profiler for the RESET state of DOE 1.

After adjusting the cursor to the maximum resistance for each of the variables, it is apparent that the profile response for T and V_r, for the RESET state shows a more significant effect on the cell resistance than V_S and Q_s, as expected from the earlier analysis. From the profiler response, it was found that the optimal pulse conditions for the RESET state of DOE 1 are at: $T = 25$ °C, $V_r = 6$ V, $V_s = 5$ V, and $Q_s = 1000$ nsec.

Moving to the prediction profiler view (or cross-section view) of the resistance for the RESET and SET model equations from DOE 1, one can see the interactions between the RESET and SET programming pulse operations across the temperature range of 25 °C to 125 °C. The combined RESET and SET (or stacked) prediction profiler view was created from Equations 4.4 and 4.5. From the prediction profiler, the optimal conditions (or the maximum RESET resistance and minimum SET resistance) from DOE 1, at an ambient temperature of 25 °C was found to be: $V_r = 6$ V, $V_s = 5$ V, and $Q_s = 1000$ nsec. These optimal conditions matched the RESET model, due to the large resistance response changes seen in the RESET resistance values when compared to the SET resistance values for the conditions used in DOE 1.

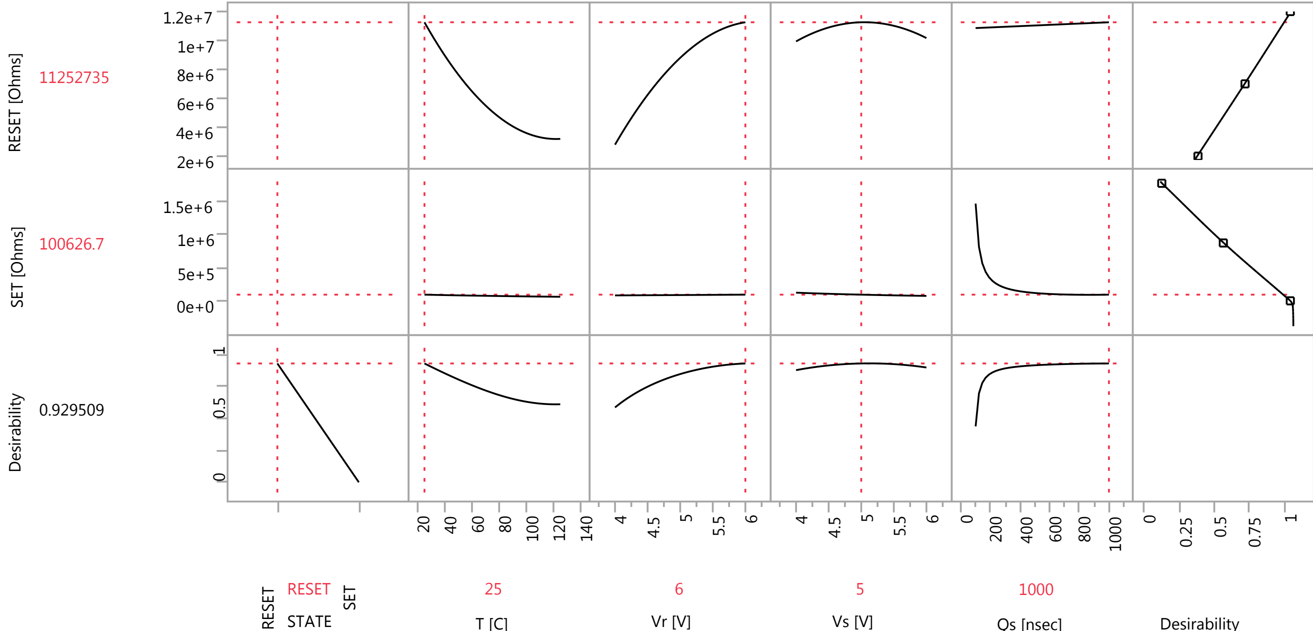

Figure 4.28 Prediction Profiler of the RESET and SET states of DOE 1.

For DOE 1, the prediction profiler values obtained in Figure 4.28 are considered the optimal pulse conditions for the given pulse conditions applied in the temperature range of 25 °C to 125 °C.

4.2 Conclusions

The method used for generating the RESET and SET models for the optimal pulse conditions were performed using least squares regression analysis. DOEs 1, 2, and 3 were analyzed separately, and model equations were generated for each; however, the optimal pulse conditions were only generated from DOE 1, because of the accuracy of the predicted response over the desired design window. To validate the model data of DOEs 1, 2, and 3, an independent experimental wafer was used. The final model for the RESET and SET optimal pulse conditions will be discussed in Chapter 5, and is used to generate the *BER* model.

CHAPTER 5: CYCYLING DOE 4 & RELIABILITY PREDICTION

5.1 DOE 4

From the data collected in DOEs 1, 2, and 3, the optimal pulse conditions were found without taking into consideration the effect of cycling. Hence, an additional DOE was setup to determine accuracy of prediction of the model equations after multiple programming cycles were performed on an array of *PCRAM* devices. This needed to be understood before performing the Bit Error Rate (*BER*) prediction analysis. From *PCRAM* reliability methods discussed in Chapter 2, it is apparent that cycling plays a role in the cell resistance response as the material is programmed from the SET to RESET state multiple times, and therefore needs to be considered when determining the optimal pulse conditions and when looking into the number of bit failures within the reading window for the Bit Error Rate (*BER*) model. For this reason, an additional cycling DOE (DOE 4) was created.

5.1.1 RESET Regression Analysis

The pulse conditions for DOE 4 matched the low, medium, and high values used in DOE 1 with the added variable of cycling. The cycling Design of Experiment (DOE 4) was setup (as shown in Table 5.1) to look into the main effects and interactions for the following factors: 1) T, ranging from 25 to 125 °C, 2) V_r and V_s, ranging from 4 V to 6 V, 3) Q_s, ranging from 100 nsec to 1000 nsec, and 4) *Cycling*, ranging from 1 to 1000 cycles.

In order to accurately capture all of the main effects, a full factorial response surface design was used. This response surface model needed 28 runs due to the added variable of cycling being implemented into DOE 4. The sample size used during the READ operation was 41 columns and 41 rows (1,681 bits) in DMA mode.

Table 5.1 DOE 4 matrix of parameters.

T [°C]	V_r [V]	V_s [V]	Q_s[nsec]	*Cycles*	TEST Sequence
25	4	4	100	1	1
25	4	4	1000	1000	2
25	4	6	100	1000	3
25	4	6	1000	1	4
25	5	5	550	100	5
25	6	4	100	1000	6
25	6	4	1000	1	7
25	6	6	100	1	8
25	6	6	1000	1000	9
75	4	5	550	100	10
75	5	4	550	100	11
75	5	5	100	100	12
75	5	5	550	1	13
75	5	5	550	100	14
75	5	5	550	100	15
75	5	5	550	1000	16
75	5	5	1000	100	17
75	5	6	550	100	18
75	6	5	550	100	19
125	4	4	100	1000	20
125	4	4	1000	1	21
125	4	6	100	1	22
125	4	6	1000	1000	23
125	5	5	550	100	24
125	6	4	100	1	25
125	6	4	1000	1000	26
125	6	6	100	1000	27
125	6	6	1000	1	28

In Figure 5.1, the variability plot of the RESET cell resistance values for the RESET state of the DOE 4 are shown. From the variability plot, it is apparent that a RESET voltage (V_r) of 4 V is not sufficient to RESET all the bits in the array (similar to DOE 1), showing more variability in the cell resistance and an overall lower cell resistance distribution across the bits sampled.

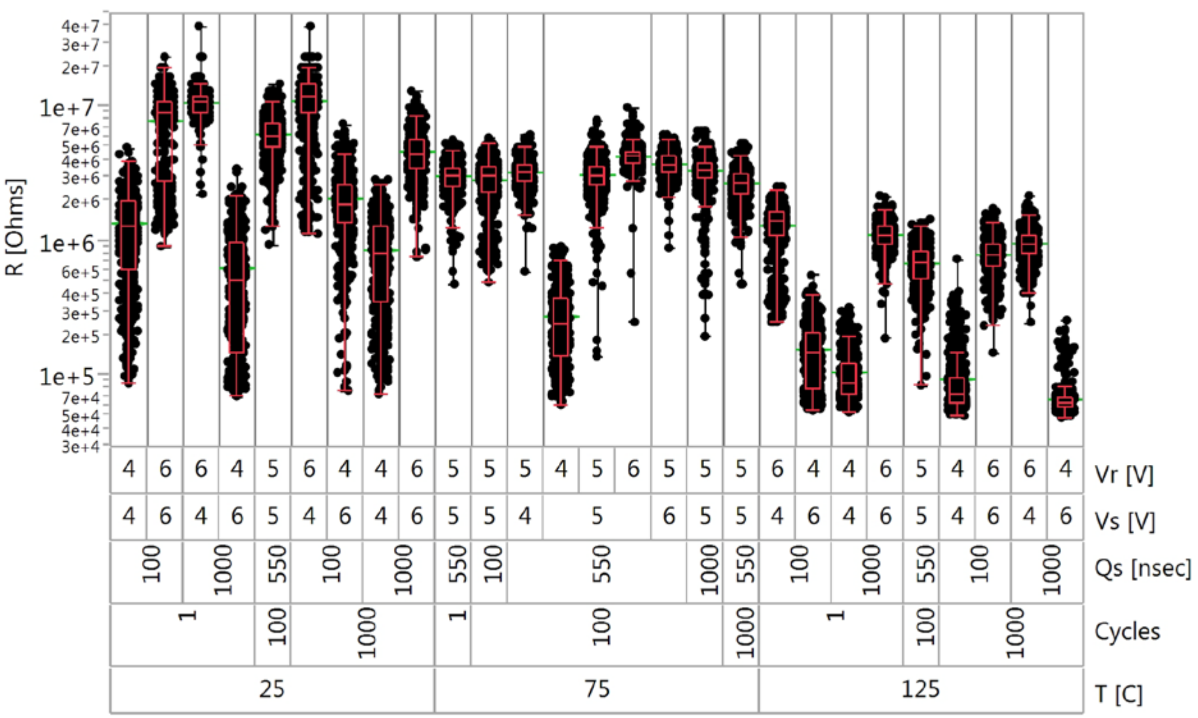

Figure 5.1 Variability plot of the RESET cell resistance bit values for the DOE 4, going from SET to RESET state for the given pulse sequence and temperature.

For the SET pulse conditions of the DOE 4, it is apparent that the SET Quench Time Q_s =100 nsec is insufficient in placing the majority of the bits in a SET state as mentioned previously in Chapter 4. This time is not long enough to allow crystallization of the amorphous dome over the top of the heater as shown in Figure 5.2.

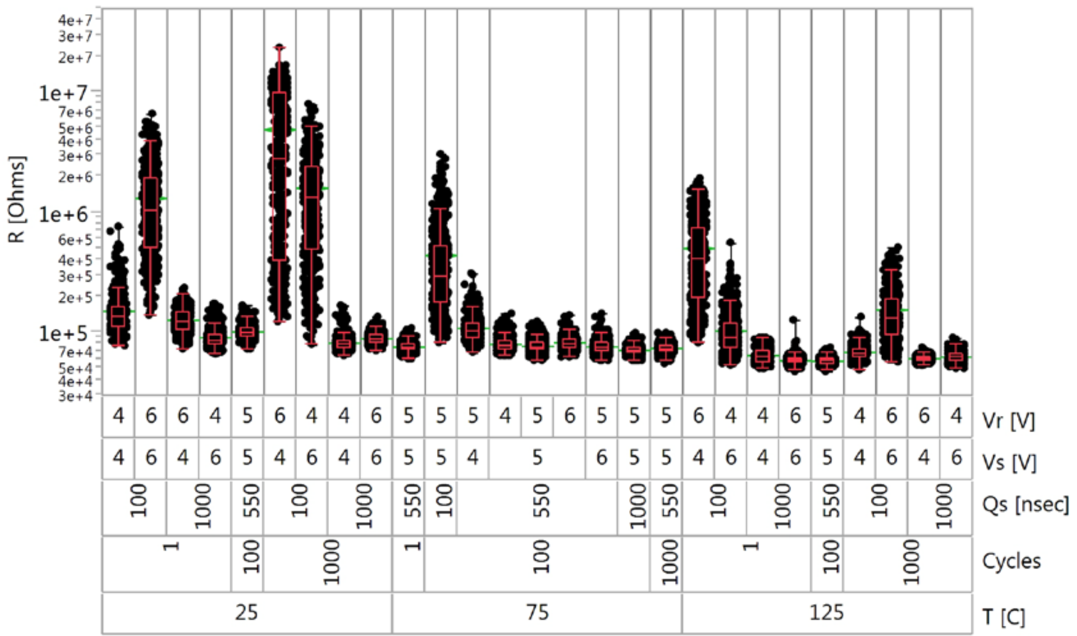

Figure 5.2 Variability plot of the SET state cell resistance for DOE 4, going from RESET to SET state for the given pulse sequence and temperatures.

After performing the READ operation on 41 columns and 41 rows (1,681 bits) and sensing the *DMA* current for the individual bits, a Fast-*DMA* (*FDMA*) READ was performed on a 4 Mbit tile, which outputs the number of cells at given cell current. However, the *FDMA* data is limited in that it does not provide the row and column information for the individual cell currents, only providing the number of cells at a given cell current.

The distribution of cell currents for each of the test sequences in DOE 4 was used to determine the number of failed bits within the programming window and was used to determine the pulse conditions that provide the lowest *BER* at the part-per-million (*PPM*) level.

For the optimal pulse condition modeling, the median resistance values from DOE 4 were calculated. These values are shown in the variability plot of Figure 5.3 and were used for the least squares regression analysis.

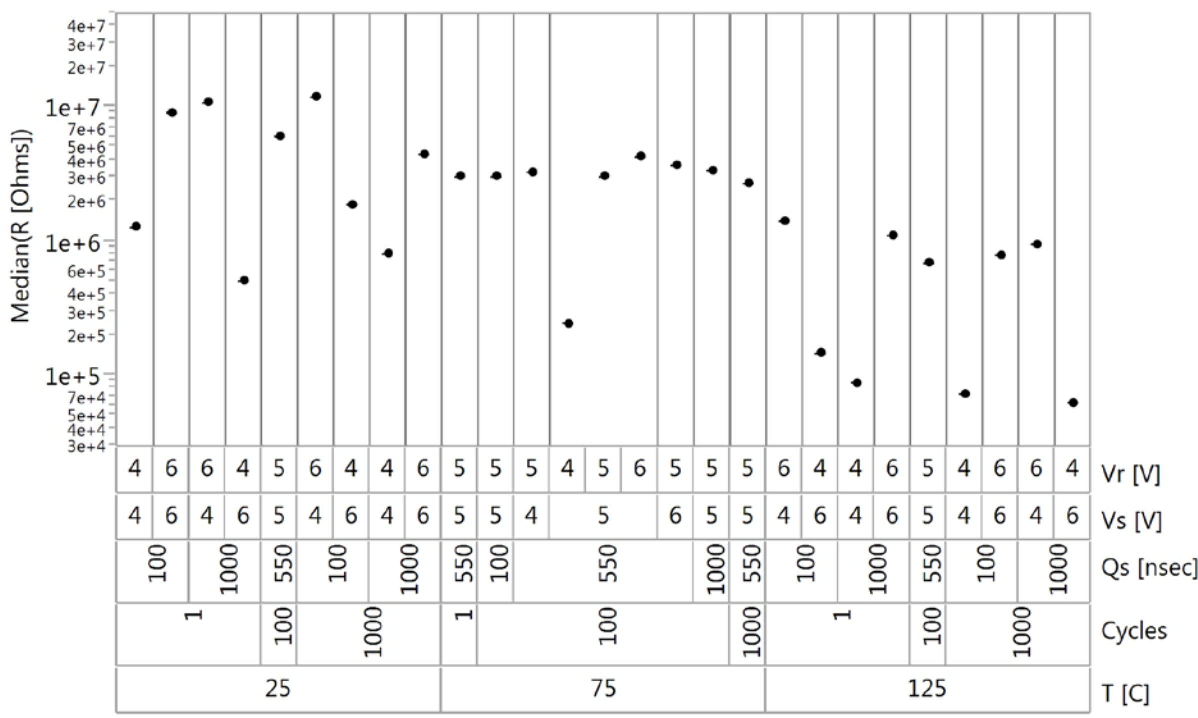

Figure 5.3 Variability plot of the median resistance values for the RESET state of the DOE 4, which were used for the optimal pulse condition model.

For the RESET state model of DOE 4, *T* was found to be the most significant variable in terms of the response of the RESET state median cell resistance, as shown in Figure 5.4. The temperature response is followed by V_r and by the combination of *T* and V_r in terms of significance of the cell resistance response. It should be noted that *Cycles* was not found to be significant in terms of the response of the median cell resistance for the RESET state model.

Term	Estimate	Std Error	t Ratio	Prob >|t|
T [C]	-4.66E+04	3.43E+03	-13.6	<.0001*
Vr [V]	2.23E+06	1.71E+05	13.1	<.0001*
(T [C]-75.0)*(Vr [V]-5.00)	-3.53E+04	3.64E+03	-9.69	<.0001*
(Vr [V]-5.00)*(Vs [V]-5.00)	-6.23E+05	1.82E+05	-3.43	0.0034*
(Qs [nsec]-550)*(Cycles-367)	-2.57E+00	7.82E-01	-3.28	0.0047*
(T [C]-75.0)*(Vs [V]-5.00)	1.05E+04	3.64E+03	2.89	0.0106*
Vs [V]	-4.92E+05	1.71E+05	-2.87	0.0112*
(T [C]-75.0)*(Qs [nsec]-550)	2.07E+01	8.08E+00	2.56	0.021*
Qs [nsec]	-7.00E+02	3.87E+02	-1.81	0.0897
Cycles	-4.68E+02	3.11E+02	-1.51	0.1527

Figure 5.4 Parameter estimates for the RESET state of DOE 4.

From the point estimate values in Figure 5.4, the RESET model equation for DOE 4 was generated, as shown in Equation 5.1.

$$R_{RESET_DOE_final} = -1.68 * 10^6 - 4.66 * 10^4 * (T) + 2.23 * 10^6 * (V_r) - 3.53 * 10^4 * \big((T - 75.0) * (V_r - 5.00)\big) - 6.23 * 10^5 * \big((V_r - 5.00) * (V_s - 5.00)\big) - 2.57 * \big((Q_s - 550) * (Cycles - 367)\big) + 1.05 * 10^4 * \big((T - 75.0) * (V_s - 5.00)\big) - 4.92 * 10^5 * (V_s) + 20.7 * \big((T - 75.0) * (Q_s - 550)\big) - 700 * Q_s - 468 * Cycles, \quad (5.1)$$

Using Equation 5.1, the prediction profiler was generated and used to determine the optimal pulse conditions for the RESET state of DOE 4. The optimal values were found to be: T = 25 °C, V_r = 6 V, V_s = 5 V, Q_s = 1000 nsec, $Cycles$ = 1 as shown in Figure 5.5. The prediction profiler T and V_r show the largest response for the RESET state similar to DOE 1. It should also be noted that V_s shows a higher RESET resistance at 4 V; however, as will be shown later in Figure 5.10, the SET resistance also increases at 4 V. For this reason, 5 V for V_s was considered optimal.

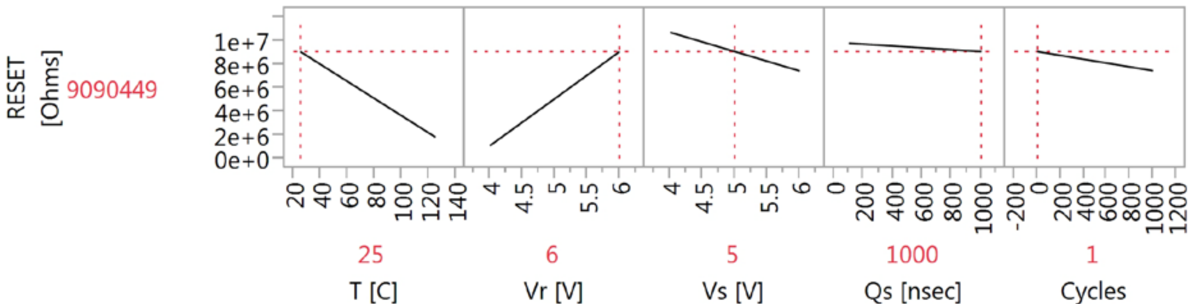

Figure 5.5 Prediction Profiler for the RESET state of the DOE 4.

From Equation 5.1, the surface and contour plot of the two most significant variables, T and V_r, for the RESET state of the DOE 4 are shown in Figure 5.6, which shows the surface profile and contour view of RESET state cell resistance. From the surface and contour plots, the direction of maximum resistance is found to be at higher V_r and lower T, similar to the results shown in DOE 1 , 2, and 3.

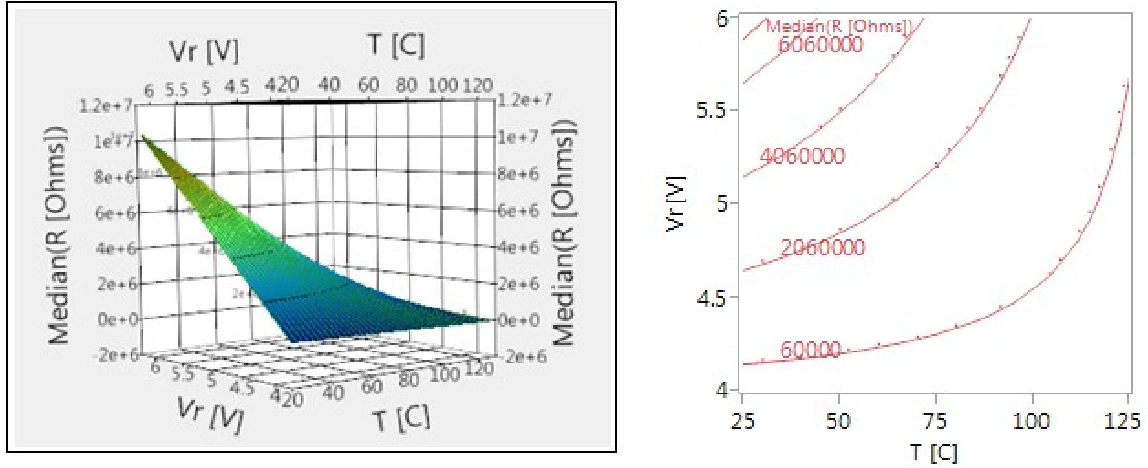

Figure 5.6 Surface and contour plot for the RESET state of the DOE 4.

Using RESET model Equation 5.1, surface models were also generated of the RESET state cell resistance for T vs. V_r, V_s, and Q_s, which are shown in Figure 5.7.

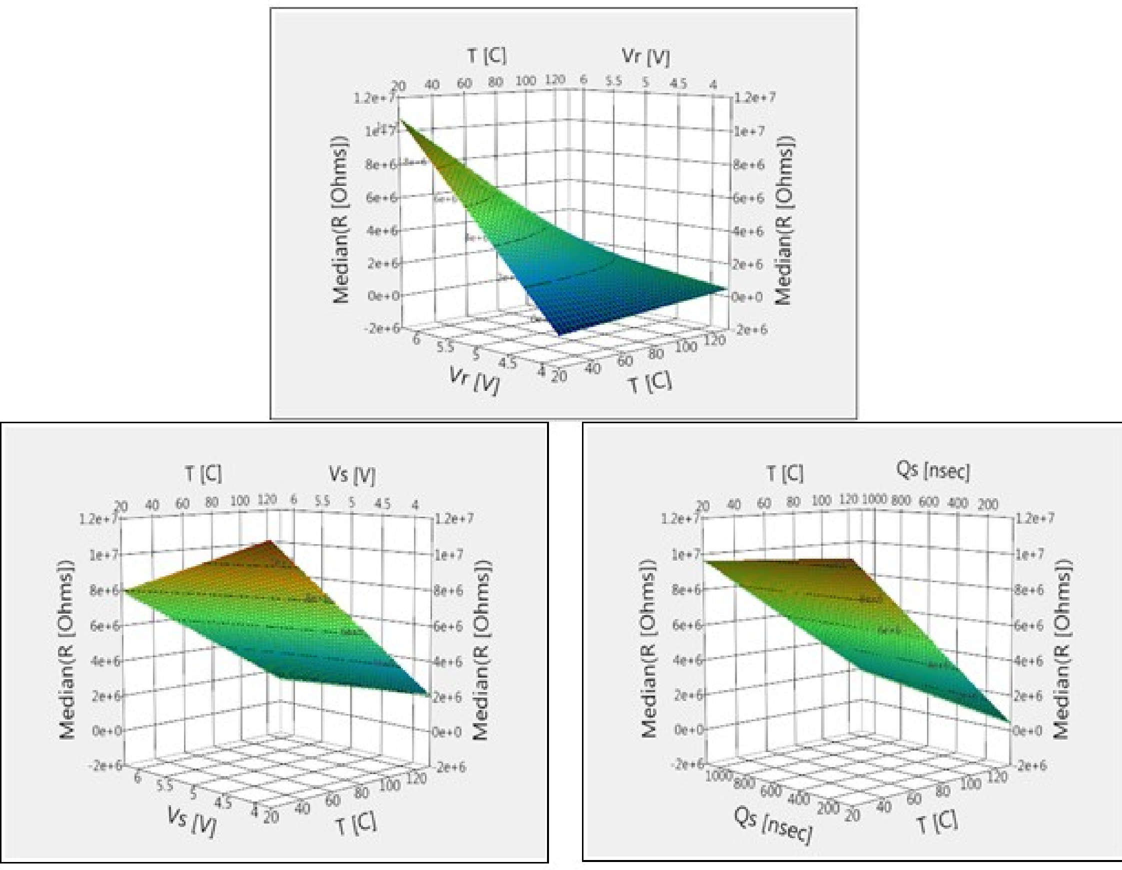

Figure 5.7 Surface Plot for the RESET state of the DOE 4. Top: Median cell Resistance (*R*) vs. Temperature (*T*) and RESET voltage (V_r); Bottom Left: Median cell Resistance (*R*) vs. Temperature (*T*) and SET voltage (V_s); Bottom Right: Median cell Resistance (*R*) vs. Temperature (*T*) and SET Quench Time (Q_s).

For the RESET state model, from the surface plots generated, it is apparent that lower ambient *T* is important to maintaining higher RESET state cell resistance. It should also be noted that between *T* of 25 °C and 85 °C, the largest drop in RESET cell resistance is seen, similar to DOE 1. This large drop in the RESET state cell resistance is largely a function of the temperature dependence of the dome of amorphous *GST* material directly over the heater as mentioned in Chapters 2 and 3.

5.1.2 SET Regression Analysis

For the optimal pulse condition modeling, the median resistance values from DOE 4 were calculated. These are shown in the variability plot of Figure 5.8, and were used for the least squares regression analysis.

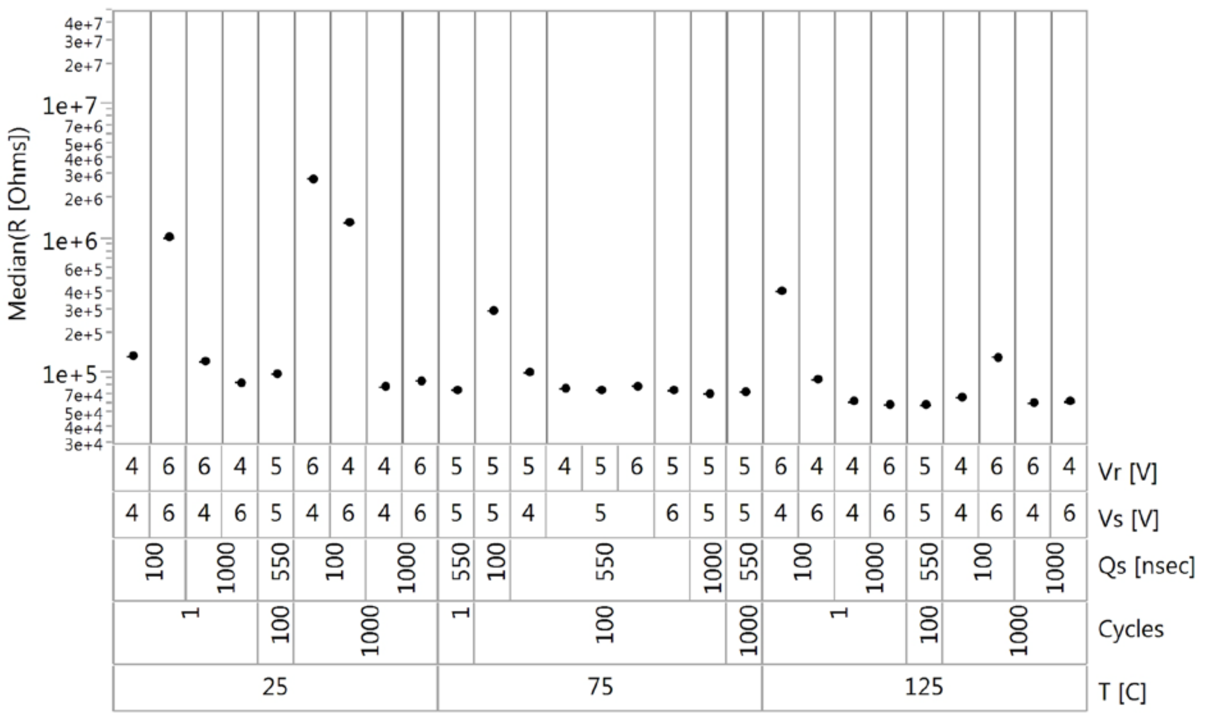

Figure 5.8 Variability plot of the median resistance values for the SET state of the DOE 4, which were used for prediction profiler in JMP.

For the SET state of the DOE 4, the top three parameter estimates of the RESET state median cell resistance were Q_s, the combination of T and Q_s, and T, as shown in Figure 5.9.

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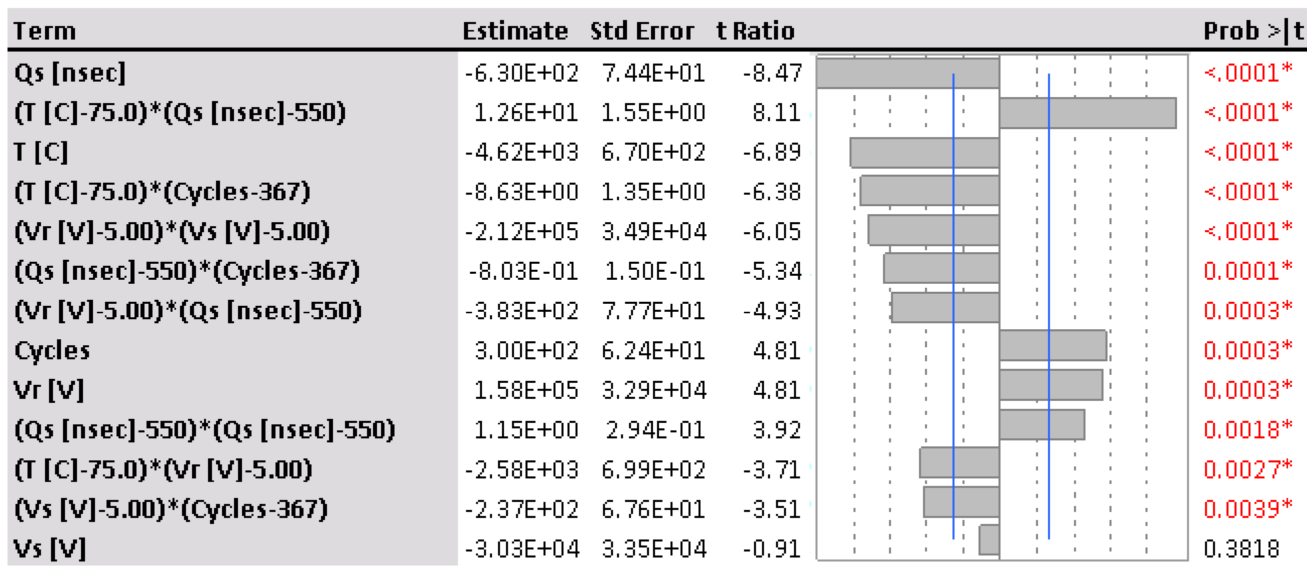

Term	Estimate	Std Error	t Ratio	Prob >|t|
Qs [nsec]	-6.30E+02	7.44E+01	-8.47	<.0001*
(T [C]-75.0)*(Qs [nsec]-550)	1.26E+01	1.55E+00	8.11	<.0001*
T [C]	-4.62E+03	6.70E+02	-6.89	<.0001*
(T [C]-75.0)*(Cycles-367)	-8.63E+00	1.35E+00	-6.38	<.0001*
(Vr [V]-5.00)*(Vs [V]-5.00)	-2.12E+05	3.49E+04	-6.05	<.0001*
(Qs [nsec]-550)*(Cycles-367)	-8.03E-01	1.50E-01	-5.34	0.0001*
(Vr [V]-5.00)*(Qs [nsec]-550)	-3.83E+02	7.77E+01	-4.93	0.0003*
Cycles	3.00E+02	6.24E+01	4.81	0.0003*
Vr [V]	1.58E+05	3.29E+04	4.81	0.0003*
(Qs [nsec]-550)*(Qs [nsec]-550)	1.15E+00	2.94E-01	3.92	0.0018*
(T [C]-75.0)*(Vr [V]-5.00)	-2.58E+03	6.99E+02	-3.71	0.0027*
(Vs [V]-5.00)*(Cycles-367)	-2.37E+02	6.76E+01	-3.51	0.0039*
Vs [V]	-3.03E+04	3.35E+04	-0.91	0.3818

Figure 5.9 Parameter estimates for the SET state of DOE.

From the point estimate values in Figure 5.9, the SET model equation was generated, which is shown in Equation 5.2.

$$R_{SET_DOE_final} = 7.84 * 10^4 - 630 * Q_s + 12.6 * \big((T - 75.0) * (Q_s - 550)\big) - 4.62 * 10^3 * (T) - 8.63 * \big((T - 75.0) * (Cycles - 367)\big) - 2.12 * 10^5 * \big((V_r - 5.00) * (V_s - 5.00)\big) - 8.03 * 10^1 * \big((Q_s - 550) * (Cycles - 367)\big) - 383 * \big((V_r - 5.00) * (Q_s - 550)\big) + 300 * Cycles + 1.58 * 10^5 * (V_r) + 1.15 * (Q_s - 550)^2 - 2.58 * 10^3 * \big((T - 75.0) * (V_r - 5.00)\big) - 237 * \big((V_s - 5.00) * (Cycles - 367)\big) - 3.03 * 10^4 * V_s, \tag{5.2}$$

In determining the optimal programming pulse conditions, the dynamic prediction profiler in JMP was used similar to DOE 1, which is shown in Figure 5.10.

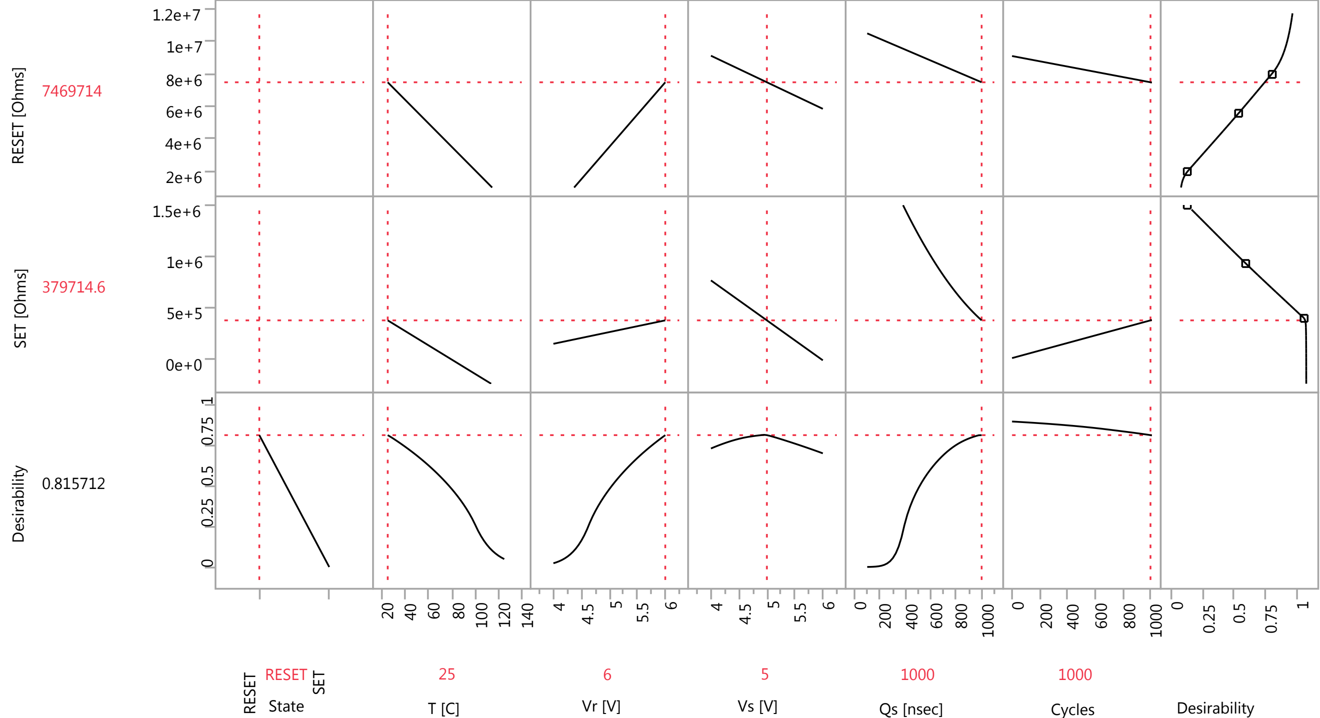

Figure 5.10 Prediction Profiler for the SET state of DOE.

In the prediction profiler view (or cross-section view) of the cell resistance for the RESET and SET model equations from DOE 4 (shown in Figure 5.10), one can see the interactions between the RESET and SET programming pulse operations across the temperature range of 25 °C to 125 °C with cycling. The combined RESET and SET (or stacked) prediction profiler view was created from Equations 5.1 and 5.2. From the prediction profiler, the optimal conditions (or the maximum RESET resistance and minimum SET resistance) from DOE 4, at an ambient temperature of 25 °C and at 1000 cycles, was found to be: V_r = 6 V, V_s = 5 V, and Q_s =1000 nsec. These results match the optimal conditions from the model generated in DOE 1.

From Equation 5.2, the surface and contour plots of the SET state cell resistance were generated for the two most significant variables (T and Q_s), which is shown in

Figure 5.11. The graphs show the direction of minimum cell resistance in the direction of higher T and Q_s, which matches what was seen in the prior DOEs.

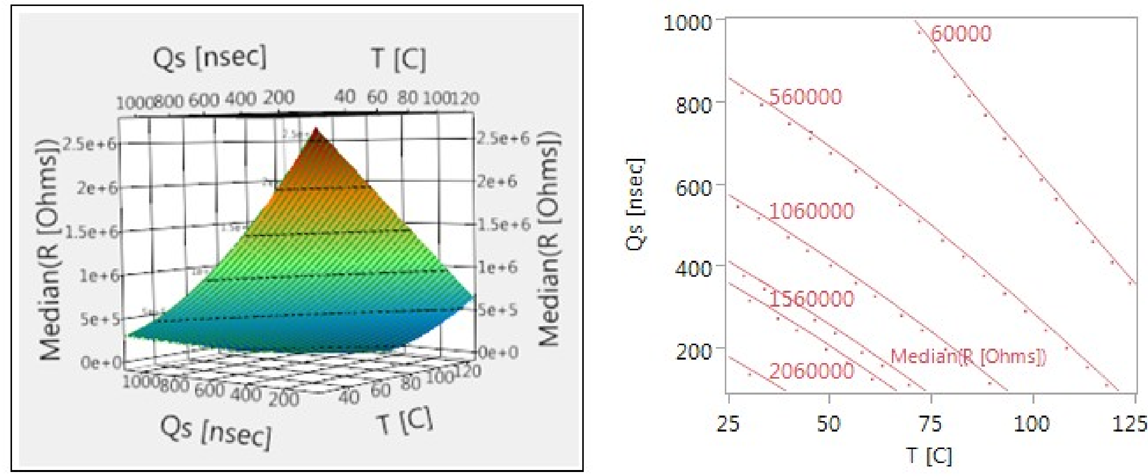

Figure 5.11 Surface and contour plots for the SET state of the DOE 4.

From the SET state model Equation 5.2, surface plots were generated for the SET state cell resistance for T vs. Q_s, V_r and V_s, as shown in Figure 5.12. From the surface plots of the SET model equation, it is apparent that higher values for Q_s, T, and V_s are important for maintaining minimum SET state cell resistance. It should also be noted that for the SET state, the largest change in the resistance response is seen with the change in Q_s between 100 nsec and 200 nsec, similar to DOE 1.

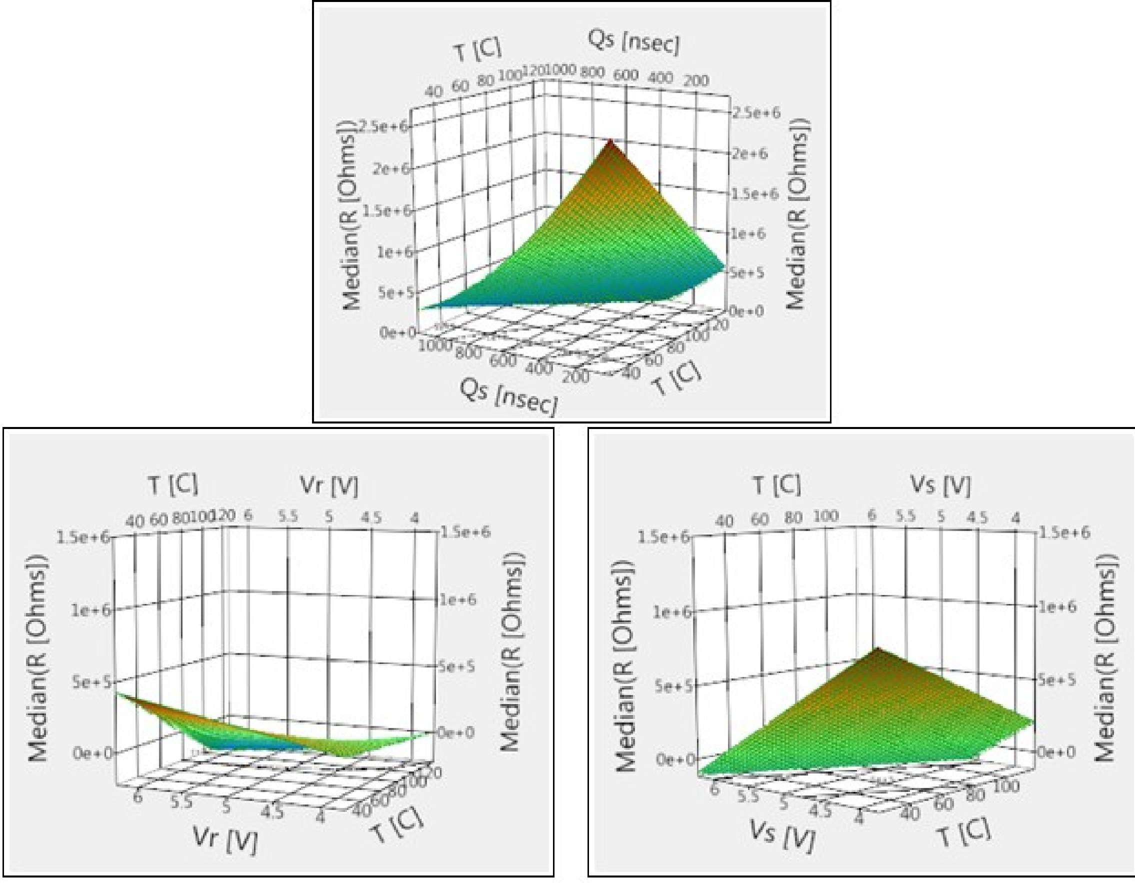

Figure 5.12 Surface Plot for the SET state of DOE 4. Top: Median cell Resistance (*R*) vs. Temperature (*T*) and SET Quench Time (Q_s); Bottom Left: Median cell Resistance (*R*) vs. Temperature (*T*) and RESET voltage (V_r); Bottom Right: Median cell Resistance (*R*) vs. Temperature (*T*) and SET Voltage (V_s).

5.2 Reliability Prediction Modeling

In this section, the model creation for reliability prediction using the *BER* from the optimal pulse conditions is discussed. The reliability model was generated from the *FDMA* data collected in DOE 4. In the development of a model capable of predicting the *BER* for a given pulse condition, fail criteria limits were based on the resistance of the cell for the SET and RESET states. The bit failure limits for the RESET and SET state were arbitrarily chosen, however, to ensure a reading window of at least one order of magnitude. The lower limit for the RESET state was placed at 1 MΩ, and the upper limit

for the SET cell resistance was placed at 0.1 MΩ; these limits were based on the collected resistance distributions. From the sum of the bits, which failed the criteria for the RESET and SET states, the *BER* was then calculated using Equation 5.3.

$$BER = \frac{\#\ Failed\ Bits}{Total\ Number\ of\ Bits\ sampled} \tag{5.3}$$

5.2.1 RESET Reliability Prediction Model

The sample size for each of the test sequences of DOE 4 was 2 Mbits. The percentage of failed bits for each of the test sequences or *BER* for DOE 4 is shown in Figure 5.13.

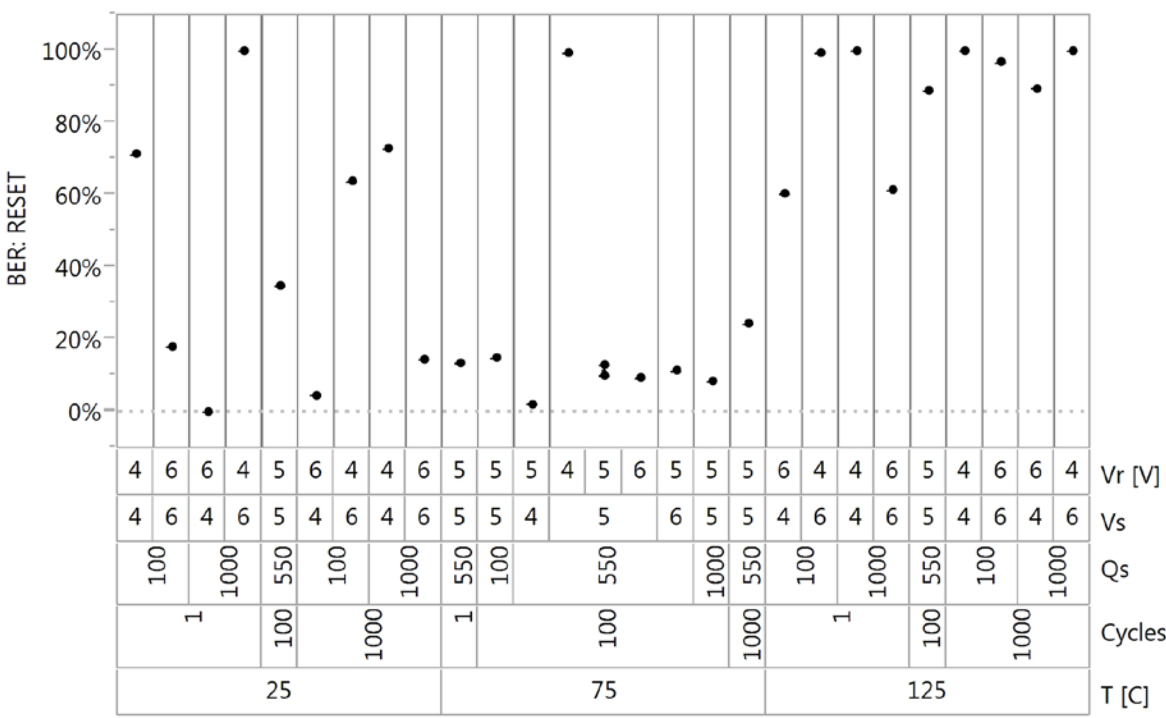

Figure 5.13 Variability plot of the *BER* going from the SET state to RESET state with the given pulse conditions.

For the regression analysis, the least means squares method was used to generate the prediction estimates, model equations, profiling data, and finally the surface model of

the reliability prediction model for the *BER*. From the least means squares analysis, the parameter estimates were generated and are shown in Figure 5.14. Similar to what was seen in DOEs 1 through 4, for the optimal pulse conditions regression analysis, the variables that were found have the most significant response in terms of the Bit Error Rate (*BER*) were found to be V_r, T, and the combination of T (third term in Figure 5.14).

Term	Estimate	Std Error	t Ratio	Prob > |t|
Vr [V]	-2.66E-01	2.73E-02	-9.75	<.0001*
T [C]	4.41E-03	5.46E-04	8.09	<.0001*
(T [C]-75.0)*(T [C]-75.0)	1.41E-04	2.72E-05	5.18	<.0001*
(Vr [V]-5.00)*(Vr [V]-5.00)	2.76E-01	6.79E-02	4.07	0.0009*
(T [C]-75.0)*(Vr [V]-5.00)	2.24E-03	5.68E-04	3.95	0.0011*
(Vr [V]-5.00)*(Cycles-357)	1.54E-04	5.49E-05	2.81	0.0127*
(Qs [nsec]-550)*(Qs [nsec]-550)	-7.42E-07	3.35E-07	-2.21	0.0417*
(T [C]-75.0)*(Cycles-357)	2.16E-06	1.10E-06	1.96	0.0672
Vs [V]	3.56E-02	2.68E-02	1.33	0.2022
Cycles	3.10E-05	5.13E-05	0.61	0.5535
Qs [nsec]	2.20E-05	5.95E-05	0.37	0.7163

Figure 5.14 Parameter estimates for RESET state *BER* of DOE 4.

From the parameter estimates shown in Figure 5.14, the *BER* model equation for the RESET state of DOE 4 was generated, as shown in Equation 5.4.

$$BER_{RESET_{DOE}} = 0.99 - 2.66 * 10^{-1} * (V_r) + 4.41 * 10^{-3} * (T) + 1.41 * 10^{-4} * \big((T - 75.0) * (T - 75.0)\big) + 2.76 * 10^{-1} * (V_r - 5.00)^2 + 2.24 * 10^{-3} * \big((T - 75.0) * (V_r - 5.00)\big) + 1.54 * 10^{-4} * \big((V_r - 5.00) * (Cycles - 357)\big) - 7.42 * 10^{-7} * (Q_s - 550)^2 + 2.16 * 10^{-6} * \big((T - 75.0) * (Cycles - 357)\big) + 3.56 * 10^{-2} * V_s + 3.01 * 10^{-5} * Cycles + 2.20 * 10^{-5} * (Q_s), \quad (5.4)$$

Using Equation 5.4, the prediction profiler was generated to show the cross-sectional view of the *BER* response for each variable. The prediction profiler response of the *BER* for the RESET state is shown in Figure 5.15. From the prediction profiler, the

parameters that were found to produce the minimum *BER* for the RESET state of DOE 4 were at: $T = 25$ °C to 85°C with the programming pulse values at $V_r = 6$ V, $V_s = 4$ V, Q_s =1000 nsec. Moreover, it should be noted that in the RESET state *BER* model, the optimal RESET voltage (V_r) pulse changes from 6 V to 5.5 V as the cycling increases from 1 to 1000 cycles. The prediction profile for the 1000 cycles is shown in Figure 5.15.

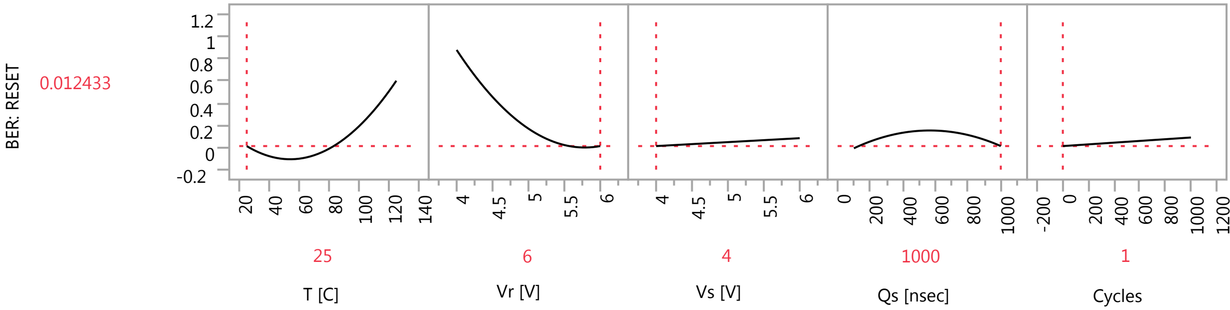

Figure 5.15 Prediction Profiler for the RESET state BER of the DOE 4.

Using the RESET model Equation 5.4, surface and contour plots were generated for the two most significant variables, T and V_r, of the *BER* response for the RESET state of DOE 4. The graphical representation of the RESET state *BER* response model is displayed in Figure 5.16, showing the direction of minimum *BER* to be for $T < 85$ °C and V_r between 5.4 and 6V.

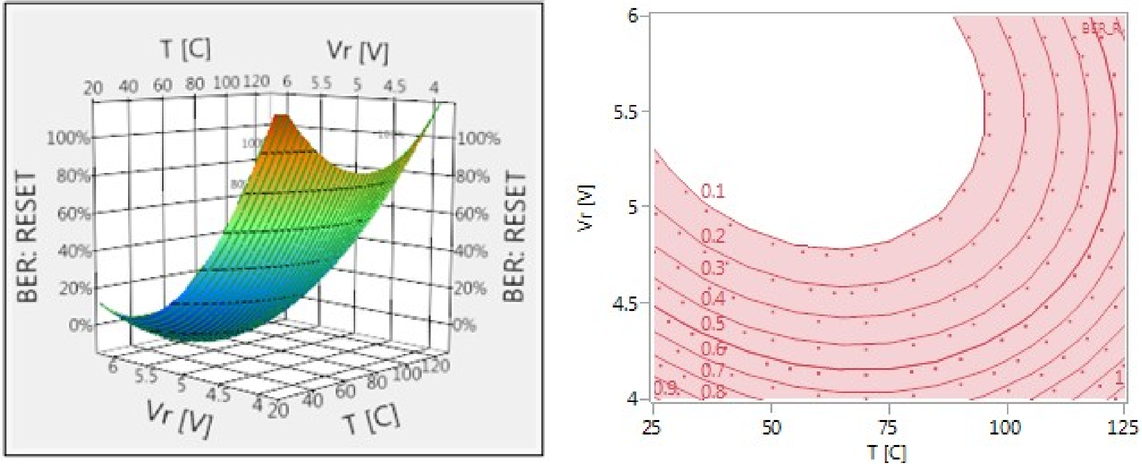

Figure 5.16 Surface and contour plot for the RESET state *BER* of the DOE 4.

Using the RESET model (Equation 5.4), surface models of the RESET state *BER* for *T* vs. V_r, V_s, and Q_s are shown in Figure 5.17. For the RESET state surface plots generated, it is apparent that maintaining T < 85°C and V_r between 5.4 and 6 V is important to keeping the minimum *BER* for the RESET state. It should also be noted that for *T* > 85°C, a significant increase in the *BER* is seen, showing the temperature sensitive nature of the amorphous *GST* material and loss of resolution of the state of the bit as *T* > 85°C. Moreover, at V_r < 5.4 V, a significant increase in the *BER* is also seen. This increase is due to lack of current for Joule heating, such that the *GST* material directly over the heater element is not being heated above the melting temperature of ~600 °C through Joule heating, and as a result the volume of the amorphous dome directly over the heater element is minimal, leading to higher bit sensing failures and/or *BER*.

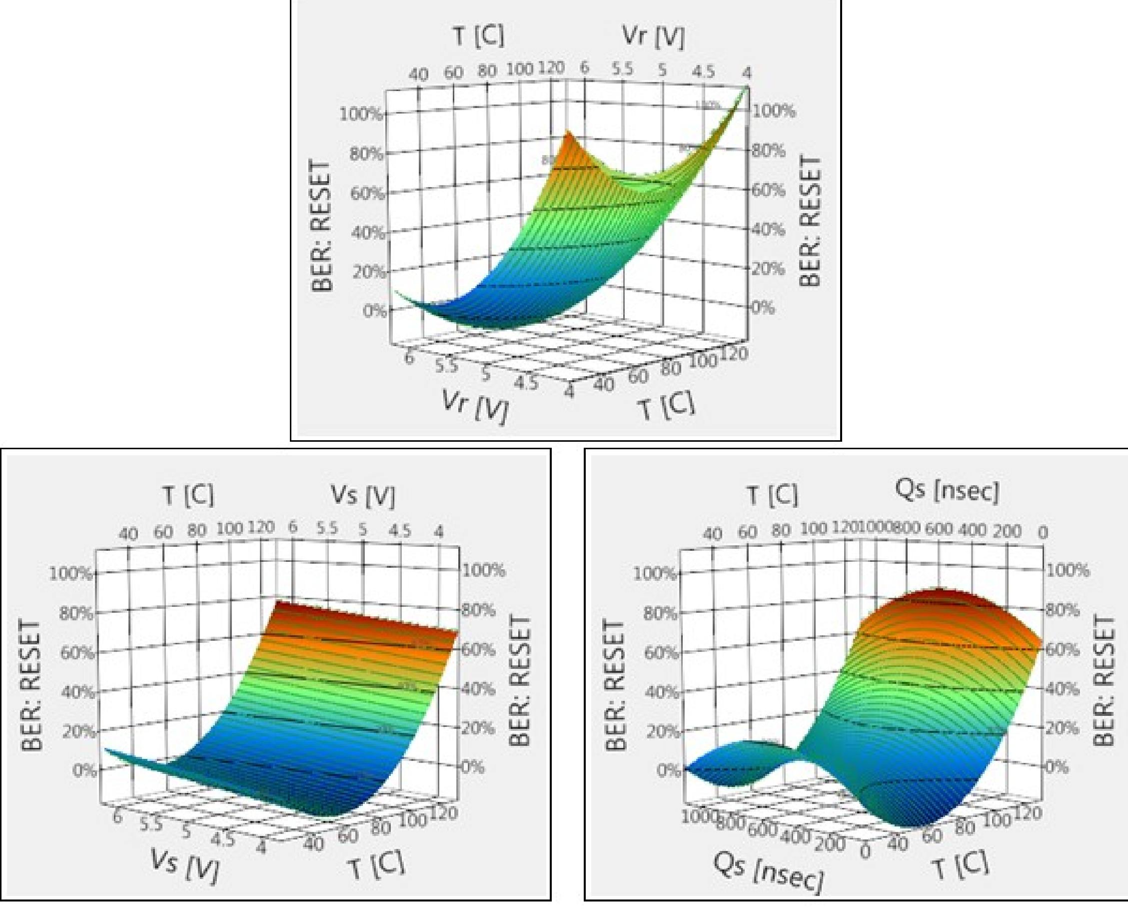

Figure 5.17 Surface Plot for the RESET state of the DOE 4. Top: BER vs. Temperature (*T*) and RESET voltage (V_r); Bottom Left: BER vs. aTemperature (*T*) and SET voltage (V_s); Bottom Right: BER vs. Temperature (*T*) and SET Quench Time (Q_s).

5.2.2 SET Reliability Prediction Model

For the SET state model, the *BER* for each of the test sequences from DOE 4 was calculated similarly to the RESET state *BER* values (using Equation 5.3) with the fail criteria set at 0.1 MΩ. The variability plot of the *BER* percentages for the SET state is shown in Figure 5.18.

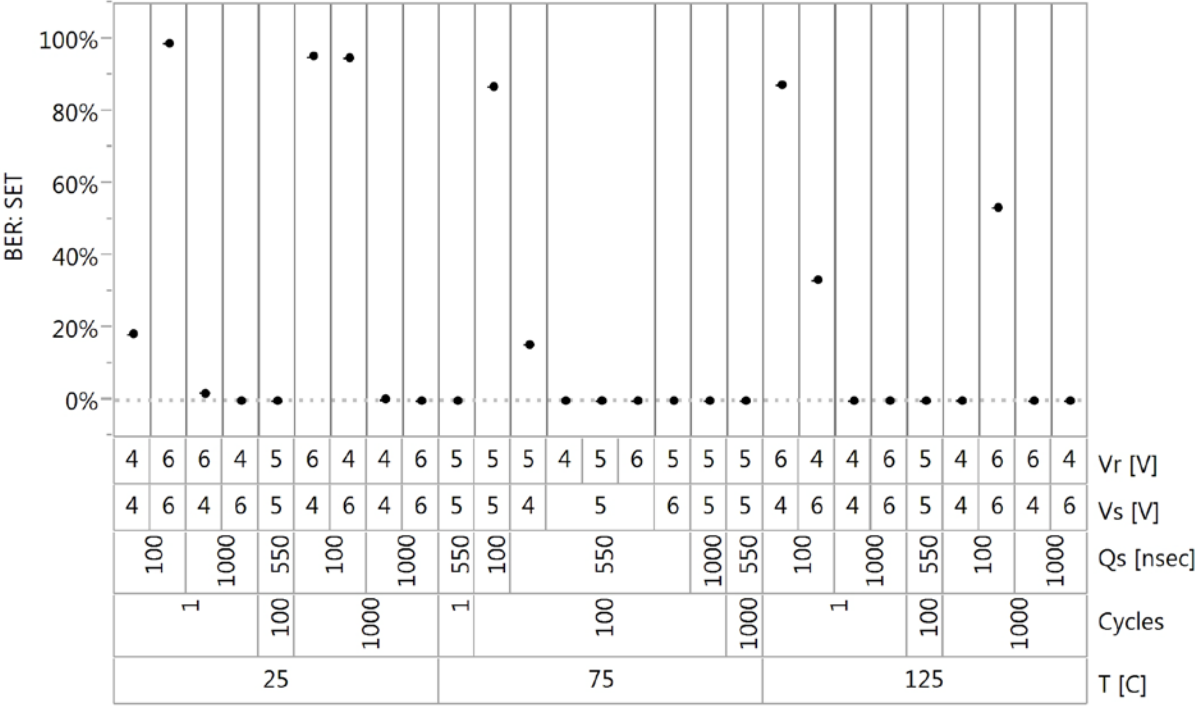

Figure 5.18 Variability plot for DOE 4 of the *BER*, going from the RESET state to SET state with the given pulse conditions.

As seen in the variability graph of the *BER* from the SET state cell resistance values, the SET quench time (Q_s) was found to have the most significant *BER* response in the SET state among all the variables, with Q_s between 100 nsec and 500 nsec showing the largest difference in the SET state *BER*. The significance of Q_s is also shown in the parameter estimates in Figure 5.19, where the three most significant parameters in terms of the SET state *BER* response were found to be Q_s, T, and the combination of V_s.

Term	Estimate	Std Error	t Ratio	Prob >|t|
Qs [nsec]	-1.08E-02	9.63E-04	-11.2	<.0001*
T [C]	-4.65E-02	8.67E-03	-5.36	<.0001*
(Vs [V]-5.00)*(Vs [V]-5.00)	3.33E+00	7.60E-01	4.38	0.0005*
(Vr [V]-5.00)*(Qs [nsec]-550)	-3.66E-03	1.02E-03	-3.59	0.0025*
(Vs [V]-5.00)*(Qs [nsec]-550)	-3.61E-03	1.02E-03	-3.53	0.0028*
(T [C]-75.00)*(Qs [nsec]-550)	-6.52E-05	2.04E-05	-3.19	0.0057*
(Vr [V]-5.00)*(Vs [V]-5.00)	-1.42E+00	4.60E-01	-3.09	0.0071*
Vs [V]	-1.34E+00	4.42E-01	-3.03	0.008*
(Vs [V]-5.00)*(Cycles-357)	2.57E-03	8.89E-04	2.89	0.0107*
Vr [V]	-5.14E-01	4.33E-01	-1.19	0.253
Cycles	-8.79E-04	8.20E-04	-1.07	0.2993

Figure 5.19 Parameter estimates for the SET state BER of the DOE 4.

From the point estimate values in Figure 5.19, the SET state model equation for the prediction response of the *BER* was generated, as shown in Equation 5.5.

$$BER_{SET_DOE} = exp(14.5 - 1.08 * 10^{-2} * (Q_s) - 4.65 * 10^{-2} * (T) + 3.33 * (V_s - 5.00)^2 - 3.66 * 10^{-3} * \big((V_r - 5.00) * (Q_s - 550)\big) - 3.61 * 10^{-3} * \big((V_s - 5.00) * (Q_s - 550)\big) - 6.52 * 10^{-5} * \big((T - 75.0) * (Q_s - 550)\big) - 1.42 * \big((V_r - 5.00) * (V_s - 5.00)\big) - 1.34 * V_s + 2.57 * 10^{-3} * \big((V_s - 5.00) * (Cycles - 357)\big) - 5.14 * 10^{-1} * (V_r) - 8.79 * 10^{-4} * Cycles), \tag{5.5}$$

From the SET model equation, surface and contour plots of the *BER* for the SET state of the two most significant variables Q_s and T were generated as shown in Figure 5.20. It can be seen that the direction of minimum *BER* is in the direction of higher Q_s and higher T.

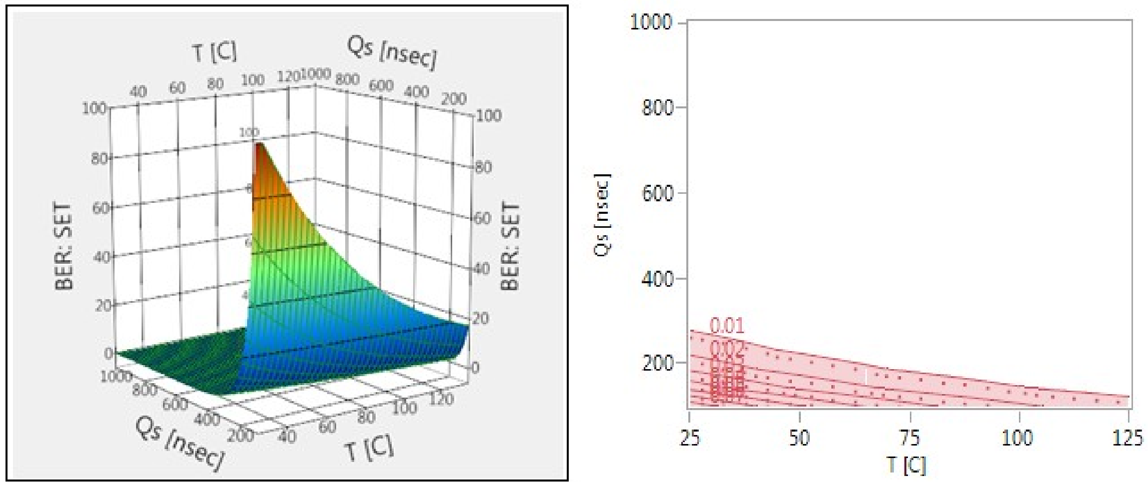

Figure 5.20 Surface and contour plot for the SET state BER of the DOE 4.

Using the model SET model equation 5.5, surface models of the SET state *BER* for Temperature (T) vs. RESET Voltage (V_r), SET Voltage (V_s), SET Quench Time (Q_s) were generated, as shown in Figure 5.21. For the SET state surface plots generated, it is apparent that higher Q_s is important for maintaining the minimum *BER* for the SET state. At a quench time of 100 nsec, one can see the significant increase in the *BER*, which is more apparent at lower ambient temperatures.

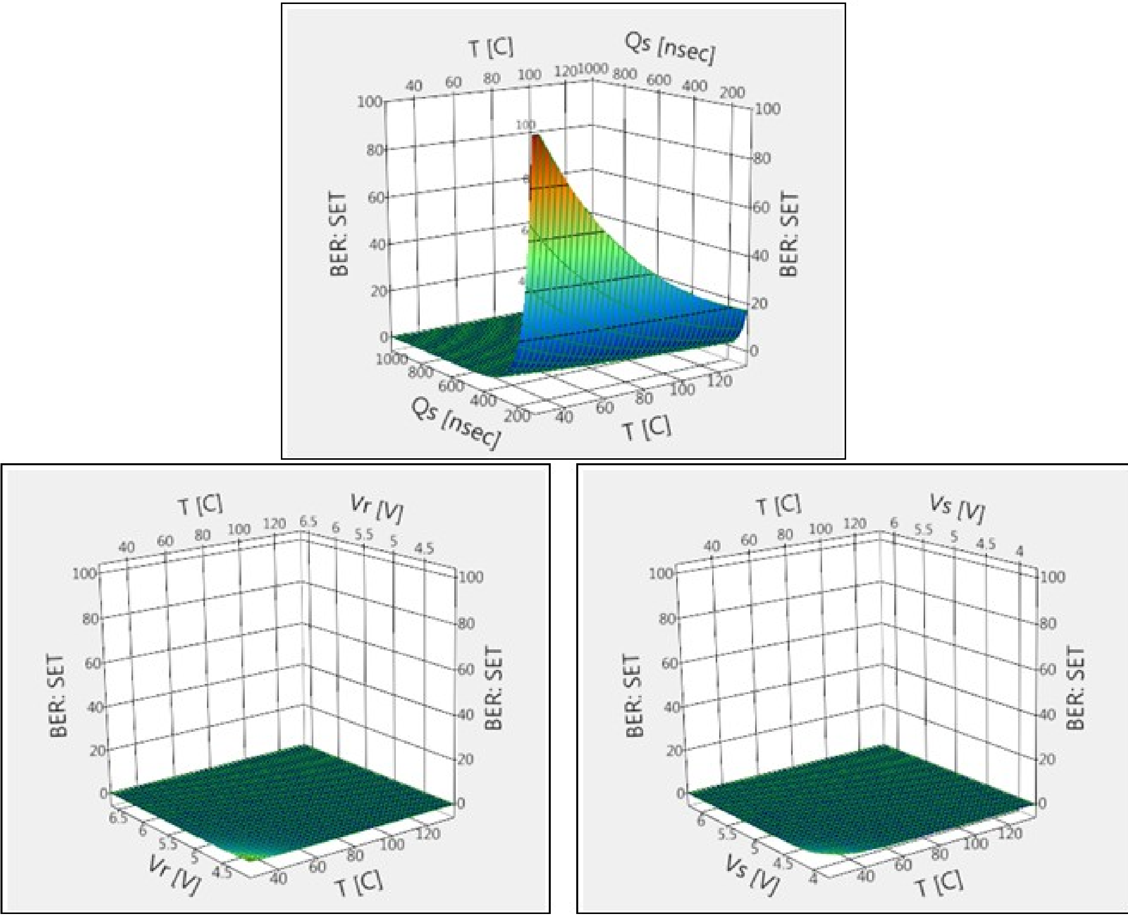

Figure 5.21 Surface Plot for the SET state of DOE 4. Top: BER vs. Temperature (*T*) and SET Quench Time (Q_s); Bottom Left: BER vs. Temperature (*T*) and RESET voltage (V_r); Bottom Right: BER vs. Temperature (*T*) and SET Voltage (V_s).

From the prediction profiler shown in Figure 5.22 of the *BER* for the SET state of DOE 4, the minimum *BER* at an ambient temperature of 25 °C was found to be at the conditions of: $V_r = 6$ V, $V_s = 5$ V, and $Q_s = 1000$ nsec for 1 cycle.

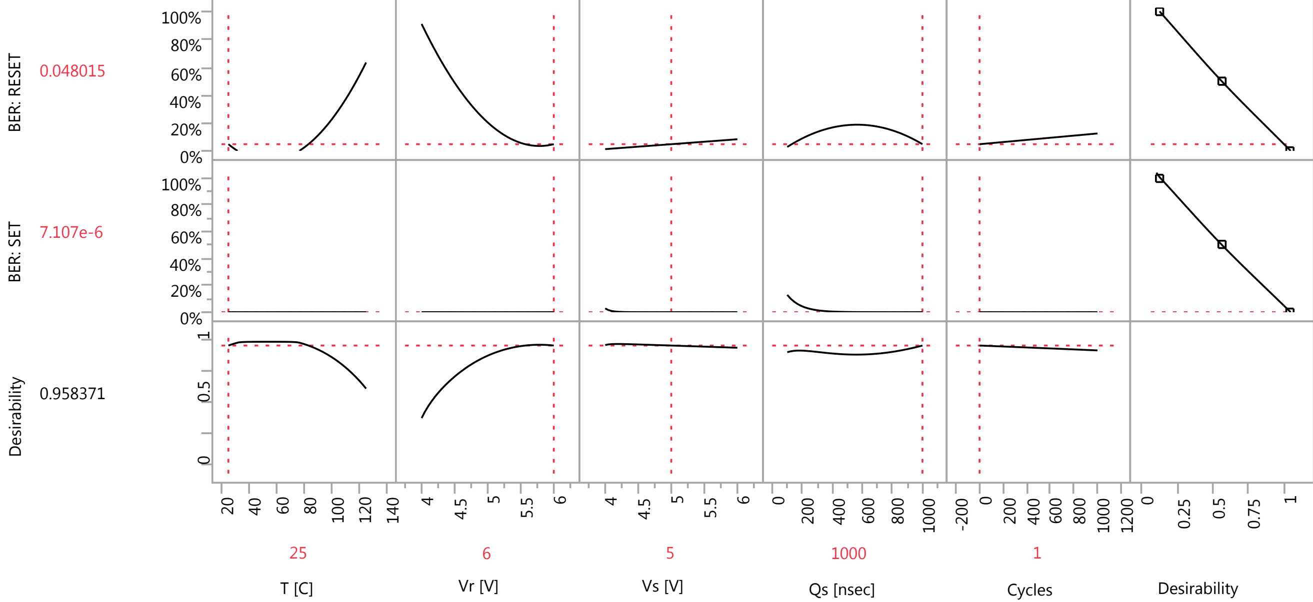

Figure 5.22 Prediction Profiler for the SET state BER of DOE 4.

5.3 Pattern Cycling Test

To validate the optimal pulse conditions and to look into possible thermal proximity disturb issues related to the programming and READ operation and/or other reliability issues when using the optimal pulse conditions, pattern cycling tests were performed. For the first patterning cycling test, multiple die were sampled across two different wafers, with the array only cycled once (1 cycle) prior to the pattern cycling. For the second test, a single die was sampled (to monitor the change in cell resistance for specific bits with cycling), with the array cycled 10 times (10 cycles) prior to the pattern cycling. The array pattern cycling test used a checkerboard pattern (shown in Figure 5.23); the White (W) and Black (B) cells were defined prior to starting the test. Once the cells were pre-defined, the following test sequence was performed: 1) white cells were programmed into a RESET state (and were not cycled again, but read two times between

each of the cycling tests), and 2) black cells were cycled at increments of 1, 10, 100, and 1000 cycles.

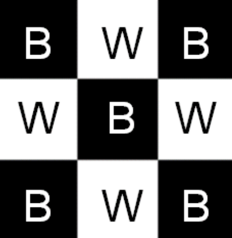

Figure 5.23 Checkerboard pattern for the pattern cycling tests "White" cells marked with "W" and Black cells marked with "B".

After each cycling increment was completed, both the White and Black cells were READ just after the final pattern cycle for the RESET state and the pattern cycle for the SET state. The results are shown in Figure 5.24.

From the results for the pattern cycling tests (shown in Figure 5.24), one can see the slight increase in cell resistance for the White cells (which were not cycled), between the pattern cycles from 1 to 1000 cycles. This increase was also seen for the Black cells but was not consistent between each of the cycling tests. The slight increase in resistance for the White cells is most likely a function of the resistance drift phenomena, related to the amorphous material as discussed in Chapter 2.

For the Black cells, as the cycling is increased above 100 cycles, a separation between the White and Black cells becomes more apparent; the median cell resistance for the Black cells starts to lower on some of the tests, which may be related to an increase in Sb % in the active area of the *GST* material as the bits are cycled [73], [74]. Examples of this phenomenon are shown in Figure 5.25.

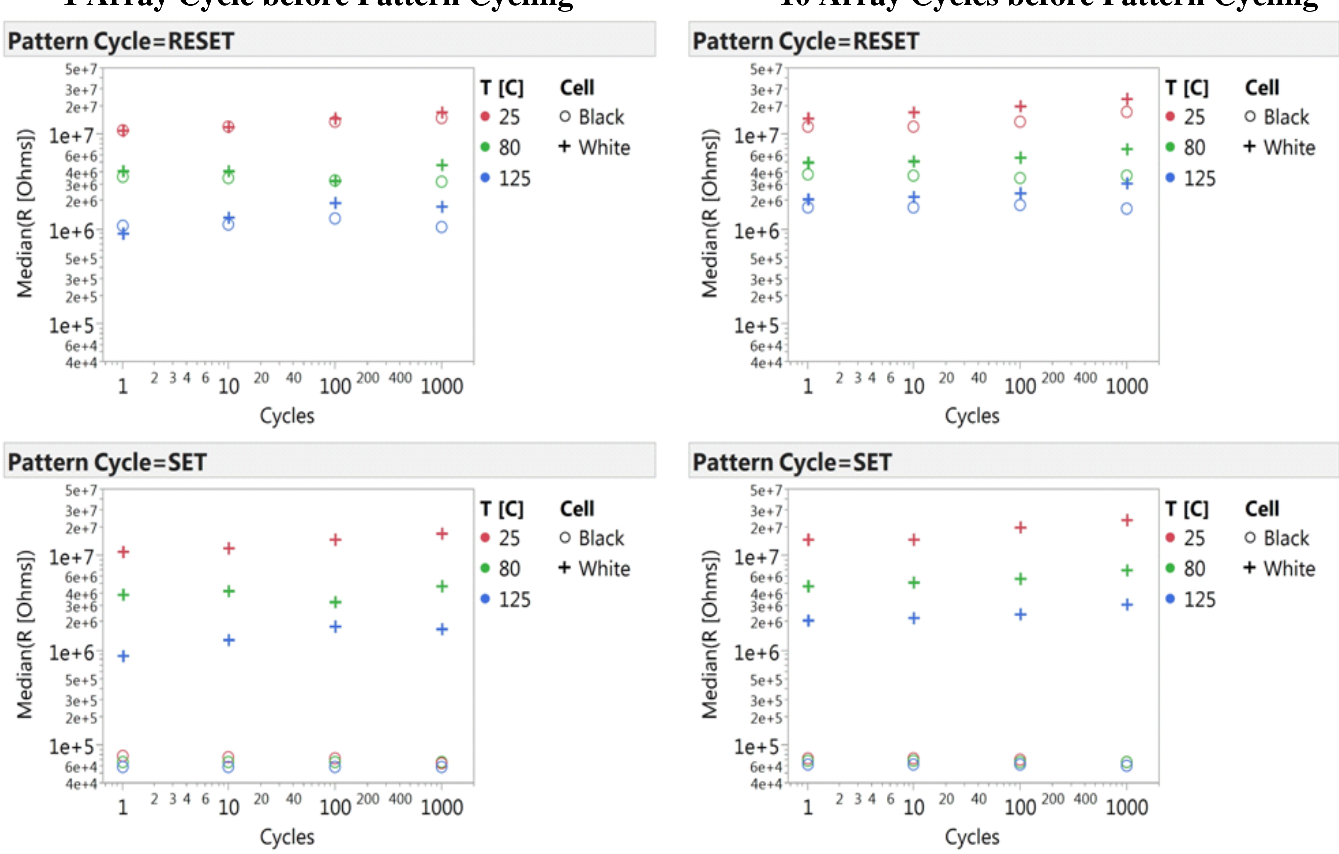

Figure 5.24 Median cell resistances (of Black and White cells) vs. programming cycle of the Black cells.

In this example, shown in Figure 5.25 (left), before cycling, the *GST* film does not show agglomeration of any of the atoms (Ge, Sb, Te); however, after cycling, the agglomeration of Sb atoms and a deficiency of Ge atoms is seen in the active region, just above the heater (or *BEC*) [73]. In Figure 5.25 (right), the cell resistance was monitored for different *GST* films and was found to decrease with increasing Sb% [74].

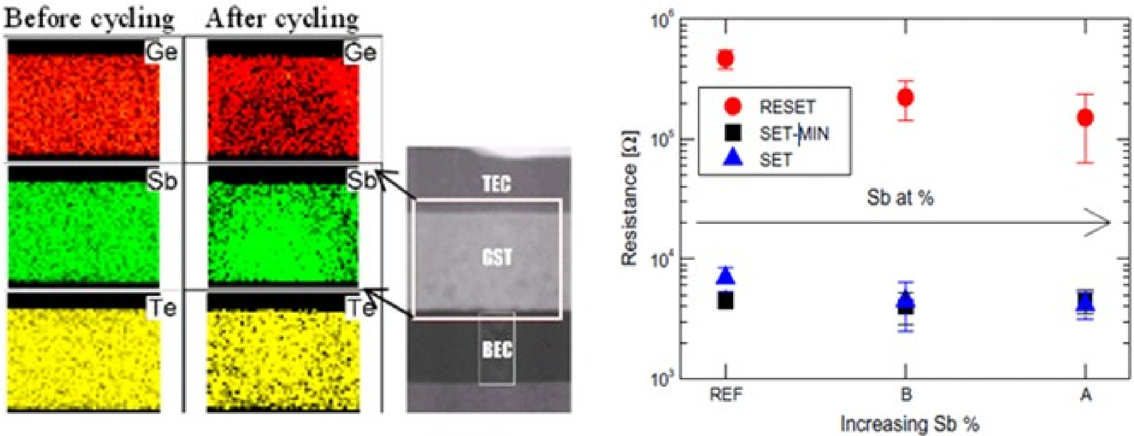

Figure 5.25 Left: Results of EDX elemental analysis showing an agglomeration of Sb atoms at the GST / Bottom Electrode Contact (BEC) interface after cycling [73]; Right: Cell resistance for the SET and RESET state with increasing Sb %, showing a decrease in cell resistance [74].

To look into the pattern cycling test further, the activation energies from the pattern cycling tests were calculated for each of the pattern cycles and then compared between the White vs. Black cells. As mentioned in Chapter 2, the activation energy can be calculated from the Arrhenius equation and/or the slope of the regression line of the ln[σ] vs. 1/*T* plot, where σ is the conduction and *T* is the temperature in Kelvin. The slope of the regression line is equal to - Ea / k, where Ea is the activation energy and k is Boltzmann's constant.

For the pattern cycling test with 1 cycle prior to pattern cycling, the activation energies of the White cells were found to change slightly (RESET: 0.188 eV vs. SET: 0.192 eV) when comparing the RESET and SET pattern cycle READ measurements (seen in Figure 5.26, top-left). However, for the pattern cycling test, which had 10 cycles prior to the pattern cycling, the activation energies were found to be aligned and were lower (RESET/SET: 0.162 eV) when comparing the RESET and SET pattern cycle READ measurements for the White cells, as seen in Figure 5.26, top-right.

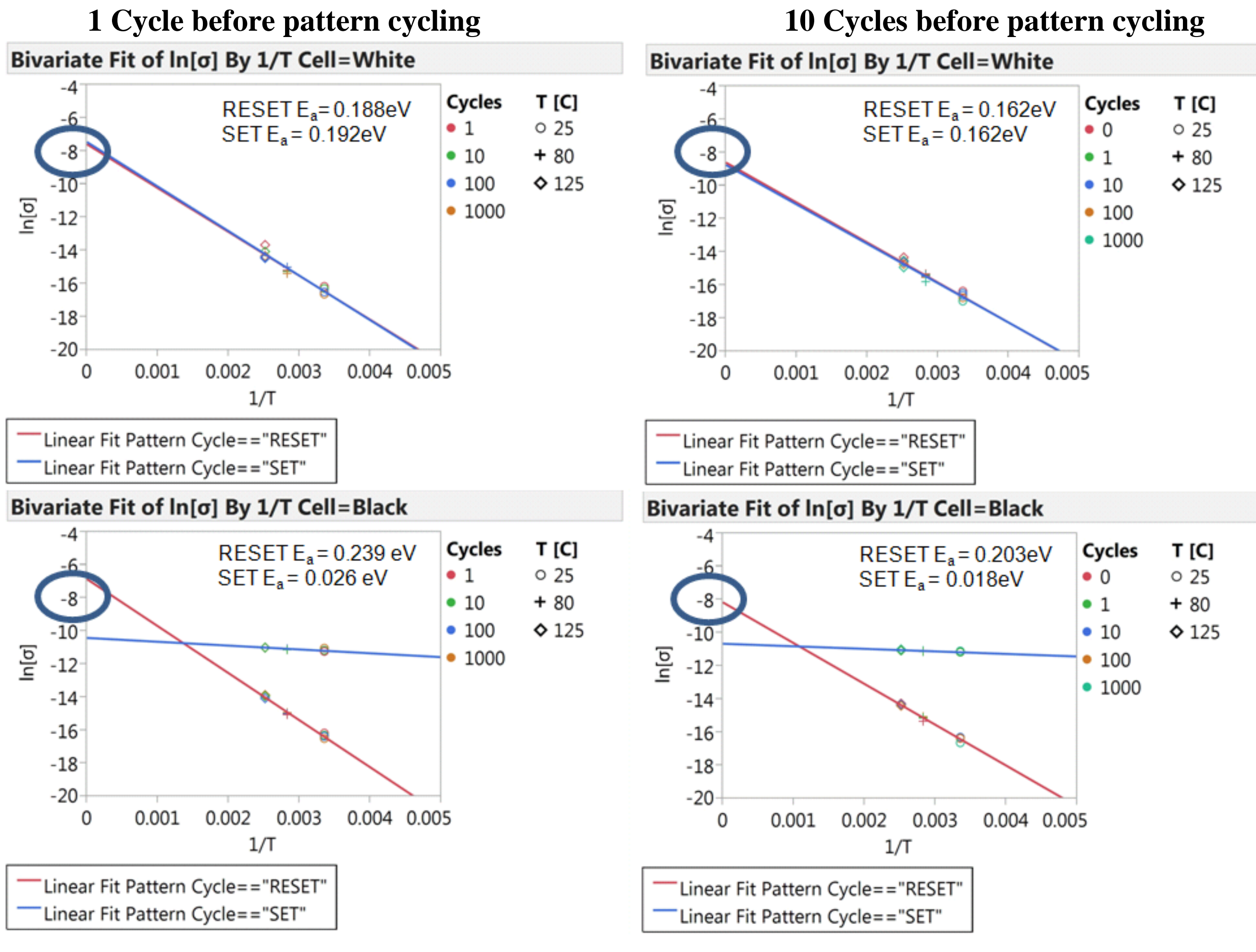

Figure 5.26 Natural log of the cell conductance vs. 1/Temperature plots, showing the temperature response and conduction activation energies for White (top) and Black (bottom) cells. Right (top/bottom): Pattern cycling test with 1-cycle performed prior to the pattern cycling. Left (top/bottom): Pattern cycling test with 10-cycles performed prior to the pattern cycling.

This lowering of the activation energy was also seen for the Black cells, when comparing the RESET and SET pattern cycle READ measurements (shown in Figure 5.26, bottom). In a recent paper reviewing the impact of Ge-Sb-Te concentration on the SET operation performance, it was found that with increasing Sb % the conduction activation energy is reduced as shown in Figure 5.27 [74].

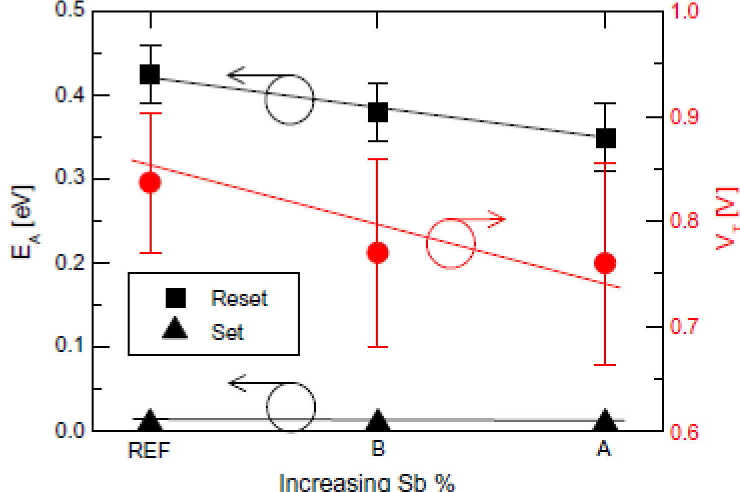

Figure 5.27 Conduction activation energy of RESET and SET states and threshold voltage trends as a function of increasing Sb concentration [74].

In determining the cycling effect, the activation energy was calculated for three different temperature ranges: 1) 25 °C to 80 °C, 2) 80 °C to 125 °C, and 3) 25 °C to 125 °C. A plot of the conduction activation energy vs. pattern cycles was generated as shown in Figure 5.28.

For the 1-cycle prior to patterning test, it was found that the activation energies were not aligned until the Black cells had been cycled up to 100 cycles (shown in boxed region of Figure 5.28, top-left). However, when looking at the 10 cycle test, the Black cells were aligned very early, and the activation energies were to found to also match for the White cells (shown in Figure 5.28, top-right). It should also be noted that from 100 to 1000 cycles a slight increase in the activation energy can be seen in the Black cells for both the 1 Cycle and 10 Cycle tests (shown in Figure 5.28, bottom-left/right), which conflicts with the Sb % data, since the activation energy should be going down with increased cycling, unless the agglomeration of Sb changes with the number of cycles.

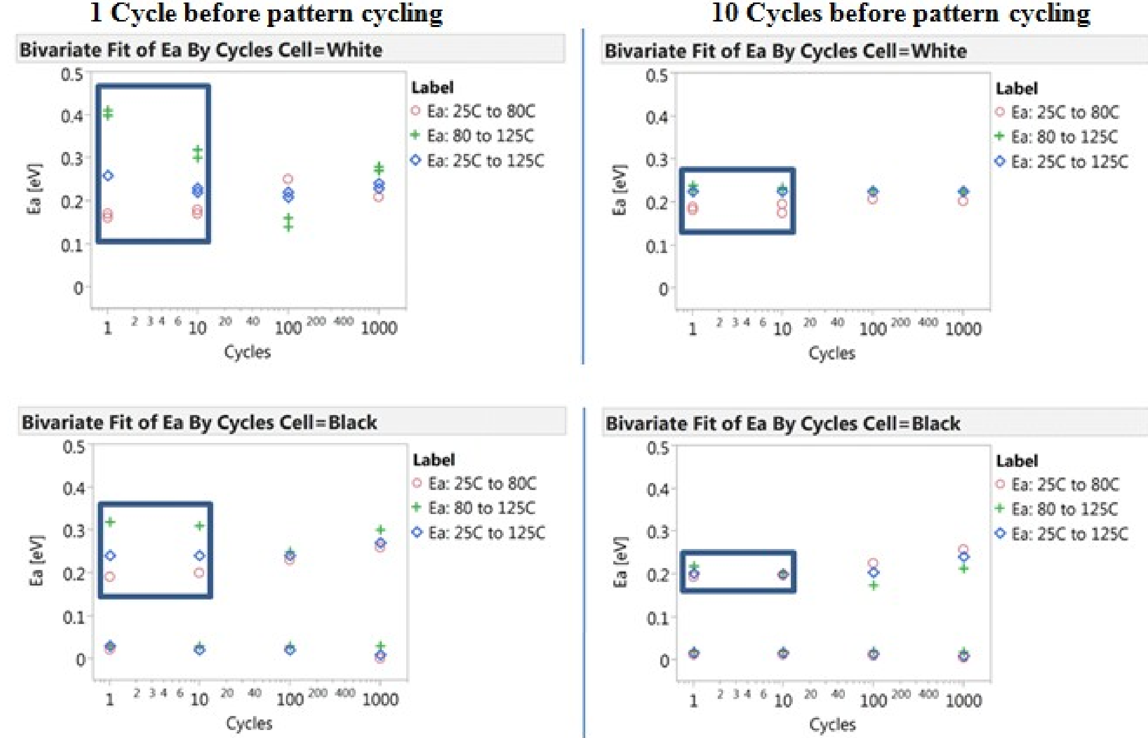

Figure 5.28 Conduction activation energy vs. Cycling. Left (top/bottom): Pattern cycling test data for 1-cycle test prior to pattern cycling; Right (top/bottom): Pattern cycling test data for 10-cycle test prior to pattern cycling.

For the contour map of the cell resistance vs. bit location (column vs. row) in the array, after performing the pattern cycling test, high resistance islands were found to be forming as increased cycling was performed in the RESET state. The high resistance islands more commonly grow around some of the Black cells, which were found to have high resistance after a single cycle. With increased cycling the high resistance islands begin to spread to neighboring White cells, and eventually at 1000 cycles the Black and White cells show similar high resistance values in the RESET state, which is shown in Figure 5.29.

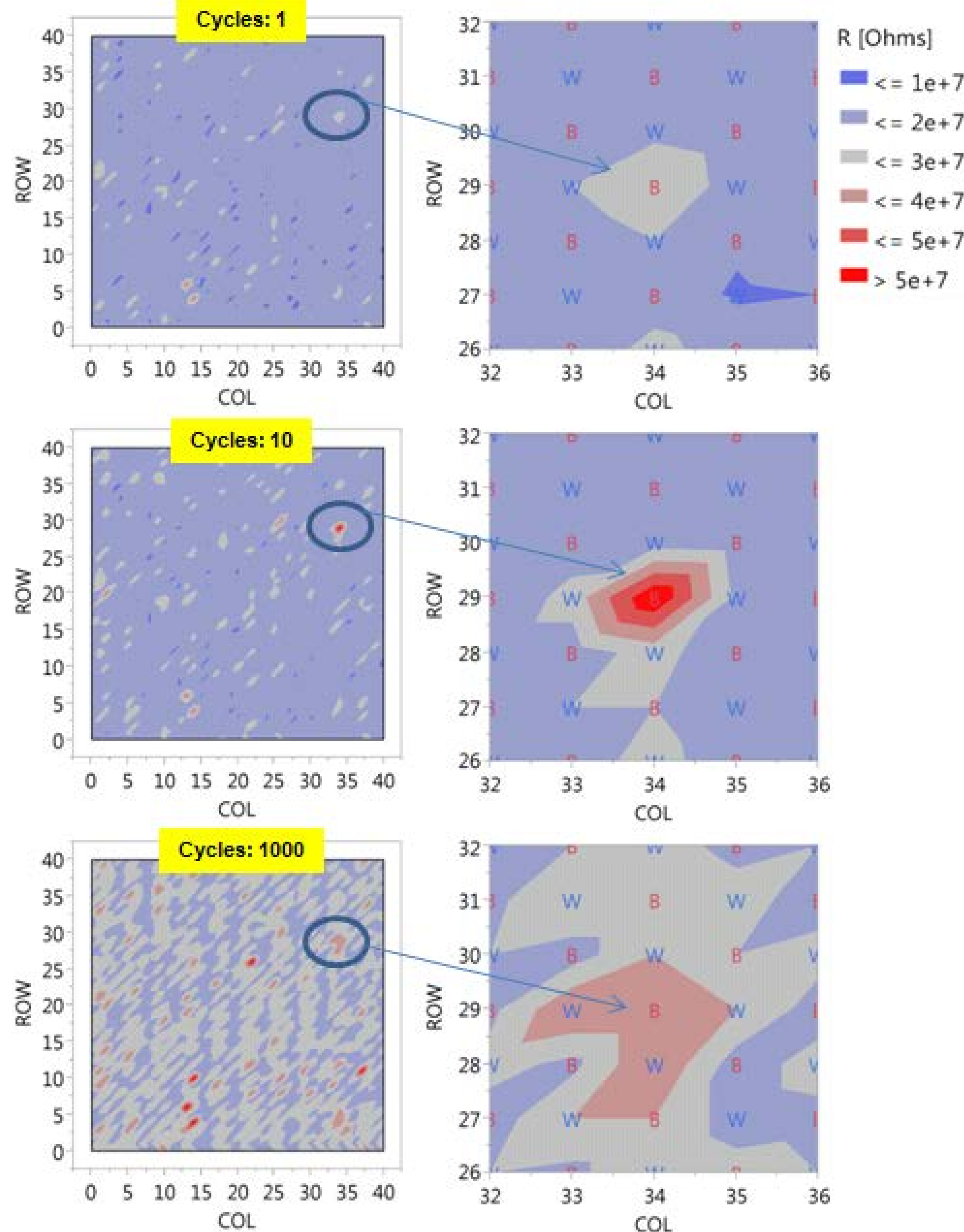

Figure 5.29 Contour map of the cell resistance vs. bit location (column and row) for a single tile, with pattern cycling performed, showing the resistance change after 1, 100, and 1000 cycles in the RESET state.

To explore the cause of the high resistance islands, which were found to grow in the RESET state, the pattern cycling test was performed again; this time the tests were performed on a 200 mm production wafer, which had been through Wafer Level Reliability (*WLR*) testing at Micron. As mentioned, the initial thought was that the high

resistance islands could be the result of the resistant drift phenomena and not related to thermal proximity disturb between the bits. To determine if this was the case, the third pattern cycling test was performed by: 1) cycling the array 10 times in the "Black" and "White" checkerboard pattern prior to performing the pattern cycling, 2) for the pattern cycling a "no operation" time delay was put into the script instead of an actual cycling pulse for the Black cells to imitate the time delay between 1, 10, 100, and 1000 cycles (and monitor the resistance drift with time), and 3) the READ pulse was performed after the same time delay at 1, 10, 100, and 1000 cycles at T = 25 °C. The results are shown in Figure 5.30.

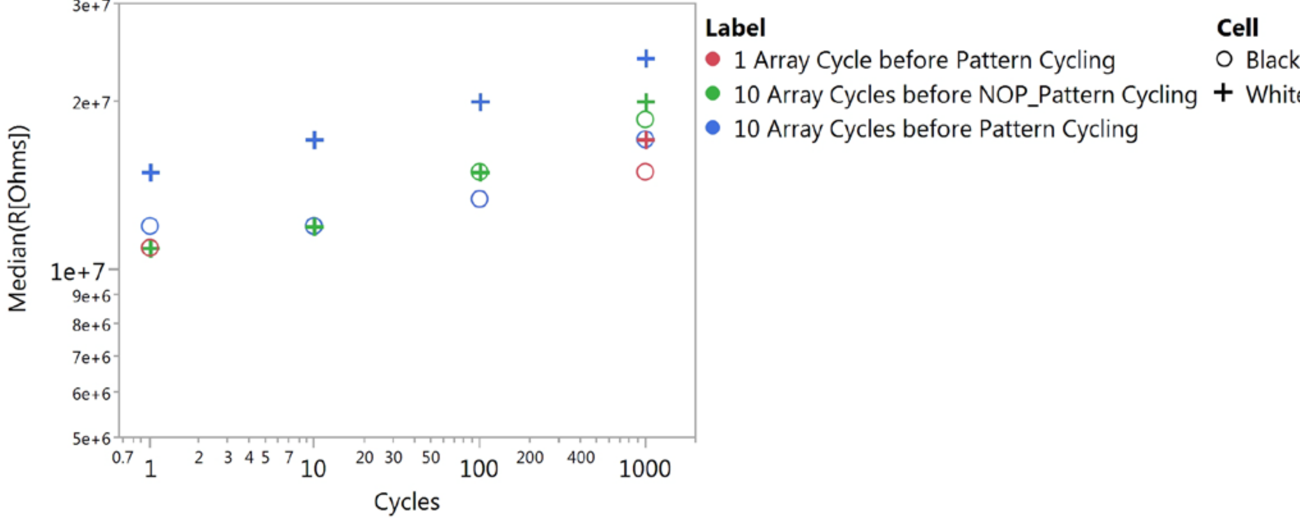

Figure 5.30 Pattern Cycling vs. No Operation Pattern Cycling after 1, 100, and 1000 cycles.

From the results shown in Figure 5.30, the cell resistance of the no operation pattern cycling test was found to more closely match the 1 array cycle pattern cycling than the 10 array cycles prior to pattern cycling test.

Due to no operation being performed on the Black cells in the third pattern cycling, it is apparent that the increase in resistance shown in Figure 5.30, with increased

cycles (or in this case time) is related to the resistance drift phenomena and not thermal proximity disturb. However, the reason for the cell resistance difference between the Black cells being slightly lower than the White is not well understood, and may be influenced by the Black cells having been cycled 10 times at the start of the test. Looking into the contour plots of the cell resistance, the high resistance islands were again found, and the island growth was still present. However, it should be noted that the islands are not as easy to see until the no operation pattern cycling test reached the same time delay of 1000 cycles.

Since the no operation pattern cycling test does not perform any program cycling on the Black bits, other than the initial 10 cycles, it was concluded that the high resistance island growth shown in Figure 5.31 is not a function of cycling Black bits or related to thermal proximity disturb, but is more a function of the resistance drift phenomena.

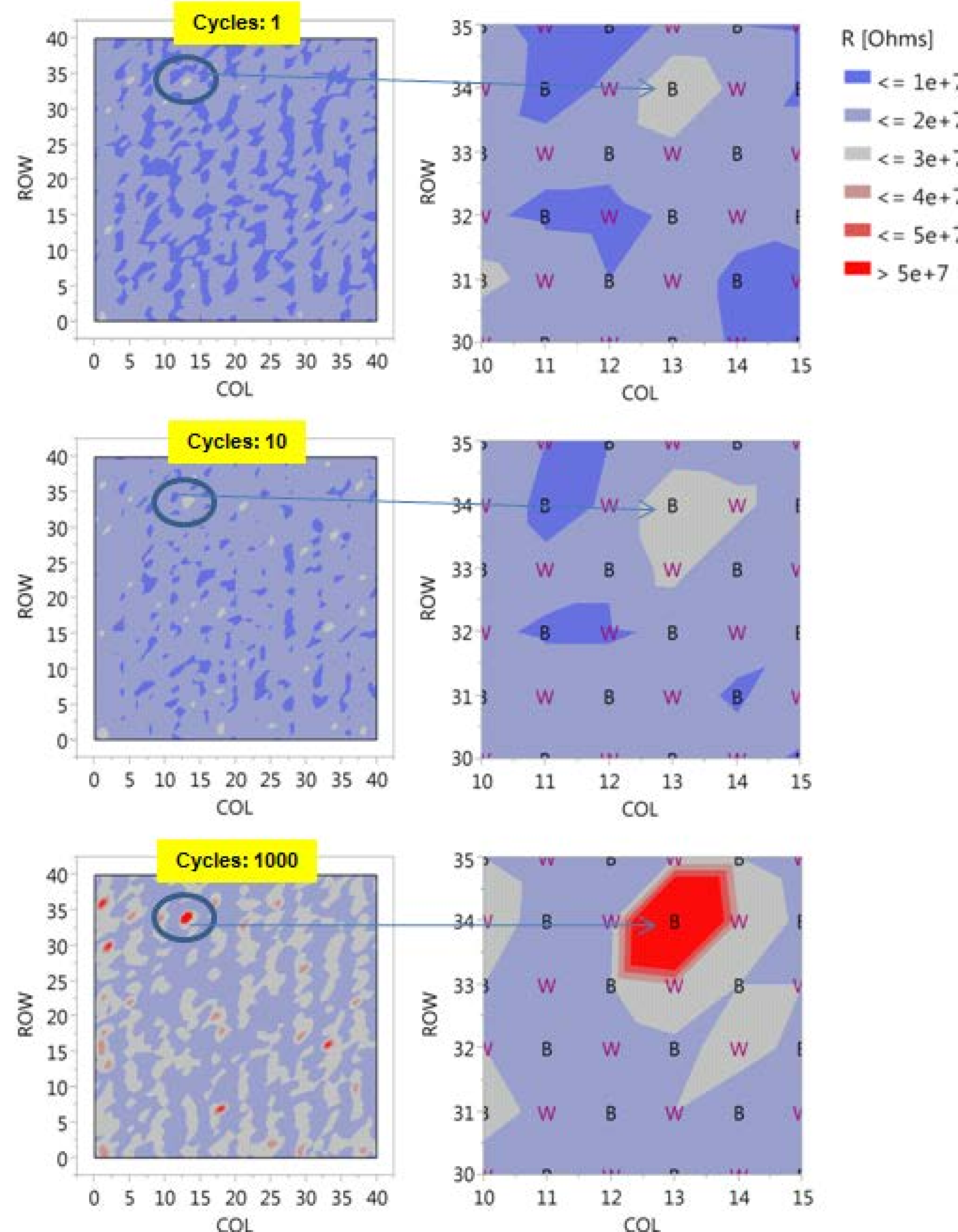

Figure 5.31 Contour map of the cell resistance vs. bit location (column and row) for a single tile No Operation Pattern Cycling test showing the cell resistance after 1, 100, and 1000 cycles.

5.4 Application

The novelty of this reliability method and the associated prediction models is twofold: 1) the reliability prediction model predicts a single combination of temperature

and pulse conditions giving the lowest *BER* for temperatures between 25 to125 °C, and 2) the ability to design a circuit that can self-adjust the pulse conditions according to the temperature of the memory, in order to provide the lowest *BER*. Once the model equations are created for a given *PCRAM* part, they can be used as a representation of the population sampled. However, if the product changes, the reliability prediction method will need to be performed again to update the pulse condition and *BER* models.

In performing the new reliability prediction method, the following steps are needed:

1) Collect several wafers at random to represent the population being sampled;
2) Perform the initial screening of the pulse conditions for temperatures between 25 °C and 125 °C;
3) Determine the design space for the Design Of Experiment (DOE);
4) Create a response surface DOE;
5) Perform the DOE and gather distribution data on at minimum 1 Mbits for the *BER* modeling;
6) Use regression analysis to develop the model equations from the cell resistance response for the pulse conditions and the *BER*; and
7) Use the prediction profiler in JMP to determine the optimal pulse conditions and the location of lowest *BER* to determine the single combination of temperature and pulse conditions giving the lowest *BER* for temperatures between 25 °C and 125 °C.

5.5 Conclusions

This dissertation was devoted to finding the optimal pulse conditions on experimental wafers from the Micron/Numonyx 45 nm technology *PCRAM* devices and to developing a reliability prediction method to model and predict a single combination of temperature and pulse conditions to give the lowest Bit Error Rate (BER).

Chapter 1 described the motivation for looking at *PCRAM* as a promising emerging memory with respect to other innovative non-volatile memory technologies. Moreover, the properties as well as the working principles of a *PCRAM* cell were covered. In Chapter 2, reliability methods used for semiconductors and *PCRAM*, including some of the limitations, were reviewed and the proposal for the new reliability method was presented. Chapter 3 described the experimental setup for DOEs 1, 2, 3, along with the initial screening for the design space. In Chapter 4, modeling of DOEs 1, 2, and 3 was performed using the least squares method and used to find the optimal pulse conditions, which were determined to be T = 25 °C, V_r = 6 V, V_s = 5 V, Q_s =1000 nsec from DOE 1.

Finally, in Chapter 5, DOE 4, which incorporated device cycling into the optimal pulse condition model, was performed, and the reliability prediction model of the *PCRAM* devices was generated. This model predicts a single combination of temperature and pulse conditions, which give the lowest Bit Error Rate on the Micron/Numonyx 45 nm technology.

The *BER* model was generated from distribution data from a 4 Mbit tile, predicting a single combination of temperature and pulse conditions giving the lowest *BER*, which are : Vr = 6 V, Vs = 5 V, and Qs =1000 nsec for lower cycles and Vr = 5.5

V, Vs = 5 V, and Qs =1000 nsec for 1000 cycles. Pattern cycling tests were performed to determine possible reliability and/or disturb issues using the optimal pulse conditions found. The test results show resistance drift for the White cells and possible Sb% change for the Black cells with cycling. When looking at the contour maps of the cell resistance across the array, islands of high resistance were found, which spread to neighboring White cells. Looking into the high resistance islands on the no operation cycling pattern test, a similar pattern as was seen in the pattern cycling test. Since the no operation pattern cycling test does not perform any program cycling to the Black bits, we can safely conclude that the high resistance island growth is not a function of the cycling of the phase change material and/or thermal proximity disturb with the optimal pulse conditions but is more a function of the resistance drift phenomena.

From this research, the future work includes: 1) Investigate the cell resistance difference between the White and Black cells in the RESET state, 2) explore how the optimized pulse conditions perform with increased cycling, and 3) Correlating the optimal pulse conditions to data retention lifetime prediction.

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APPENDIX

Python Script for Cycling

```
#JaredBarclay
# Input Variable list: Loop count, Partition

import sys
import Microsoft
sys.path.append("G:\RD\FAB\CMP\JBARCLAY2\scripts")
import um2_cli;
import re;
import fileinput
import os
import getopt
from um2_cli import *
from System.Collections.Generic import *

#Global Variables
Gl_Loop = int(sys.argv[1])
Gl_Partition = int(sys.argv[2])
#End Global Variables

# Overwrite Begin
def
cell_overwrite(partition_start=0,partition_end=0,row_start=0,row_end=2047,col_start=0,
col_end=2047,polar="True",pat="Ones"):
    "This does a cell overwrite of the whole partition against some pattern"
    u.Cli('um-set-polarity %s' %(polar)) #True, Complement, Alternating
    u.Cli('um-set-background %s' %(pat)) #Ones, Logical Checkboard
    u.RunCommandGetResults('Overwrite ApplyShadow=1 Display_SR_Time=0
OverWriteMode=1 part_s=%i part_e=%i row_s=%i row_e=%i col_s=%i col_e=%i'
    %(partition_start,partition_end,row_start,row_end,col_start,col_end))
# Overwrite End

# Write Pattern Begin
def
Write_Pattern(partition_start=0,partition_end=0,row_start=0,row_end=2047,polar="True
",pat="Ones"):
    "This does a cell overwrite of the whole partition in ones pattern"
    u.Cli('um-set-polarity %s' %(polar)) #True, Complement, Alternating
```

```
    u.Cli('um-set-background %s' %(pat)) #Ones, Logical Checkboard
    u.RunCommandGetResults('Write_Pattern ApplyShadow=1 Display_SR_Time=0
Write_CK=0 Write_CKbar=1 part_s=%i part_e=%i row_s=%i row_e=%i'
    %(partition_start,partition_end,row_start,row_end))
# Write Pattern End

# Dma Begin
def
Dma(partition_start=0,partition_end=0,row_start=0,row_end=2047,col_start=0,col_end=
2047,polar="True",pat="Ones"):
    "This takes the DMA on some in a partition on all row+columsn by default against
some pattern"

    u.Cli('um-set-polarity %s' %(polar)) #True, Complement, Alternating
    u.Cli('um-set-background %s' %(pat)) #Ones, Logical Checkboard
    #Delete the UM2 data file before running so data is clean
    #u.ClearOutputPane('Data')
    mte.Globals.VariableValue["TestComplete"] = 0 #clears the flag that indicates when
the test is done
    isComplete = mte.Globals.VariableValue["TestComplete"]  # at the end of the test, the
VBA macro will set this variable to a 1.
    isStopped = mte.Tester.IsActiveBinTestStopped   #set to true if you stop the test by
hitting the stop button.
    u.RunCommandGetResults('Dma ApplyShadow=1 tile_s=7 tile_e=7 dq_s=7 dq_e=7
part_s=%i part_e=%i row_s=%i row_e=%i col_s=%i col_e=%i'
    %(partition_start,partition_end,row_start,row_end,col_start,col_end))
     isComplete = mte.Globals.VariableValue["TestComplete"]  # at the end of the test, the
VBA macro will set this variable to a 1.
# Dma End

# Distribution Begin
#modified on - changed while loop to include isStopped condition
def
Distribution_Pattern(Read_CK=1,Read_CKN=0,current_start=0,current_end=15,current
_step=0.5,partition_start=0,partition_end=0,polar="True",pat="Ones"):
    "This takes the Distribution on some section in a partition on all row+colums by
default against some pattern"
    u.Cli('um-set-polarity %s' %(polar)) #True, Complement, Alternating
    u.Cli('um-set-background %s' %(pat)) #Ones, Logical Checkboard
    mte.Globals.VariableValue["TestComplete"] = 0 #clears the flag that indicates when
the test is done
    isComplete = mte.Globals.VariableValue["TestComplete"]  # at the end of the test, the
VBA macro will set this variable to a 1.
    isStopped = mte.Tester.IsActiveBinTestStopped   #set to true if you stop the test by
hitting the stop button.
```

```
   u.RunCommandGetResults('Distribution_Pattern ApplyShadow=1 SingleTile=1 tile=9
row_s=0 row_e=2047 Read_CK=%i Read_CKN=%i current_s=%i current_e=%i
CurrentStep=%f part_s=%i part_e=%i'

%(Read_CK,Read_CKN,current_start,current_end,current_step,partition_start,partition_e
nd))
# Distribution End


#Cycling Begin
cell_overwrite(Gl_Partition,Gl_Partition,0,2047,0,2047,"Complement","Ones")  #RESET
Array
Dma(Gl_Partition,Gl_Partition,0,2,0,2,"True","Ones")  #READ Array

j = 1
while j < Gl_Loop:

   Write_Pattern(Gl_Partition,Gl_Partition,0,2047,"True","Ones") # writes CKB ones
pattern

   #Dma(Gl_Partition,Gl_Partition,0,1,0,1,"True","Ones") # performs Dma Read.

   Write_Pattern(Gl_Partition,Gl_Partition,0,2047,"Complement","Ones") # writes CKB
ones complement pattern.

   #Dma(Gl_Partition,Gl_Partition,0,1,0,1,"Complement","Ones") # performs Dma Read.

   j = j + 1

print('1000 CKB cycles') # prints out cycle count once loop is completed
# Cycling End
```