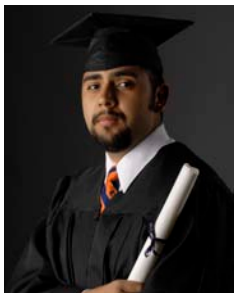
Investigation of Single pMOSFET Gate Oxide Degradation on NOR Logic Circuit Operability



David Estrada[1]: McNair Scholar
W.B. Knowlton[1, 2]: Faculty Mentor
M. L. Ogas[1], R.G. Southwick III[1], J. Kiepert[1],
T. Gorseth[1], R. J. Baker[1]: Contributing Authors

[1]Department of Electrical and Computer Engineering, Boise State University 1910 University Dr., Boise, ID 83725 USA
[2]Department of Materials Science and Engineering, Boise State University 1910 University Dr., Boise, ID 83725 USA

The impact of gate oxide degradation of a single pMOSFET on the performance of the CMOS NOR logic circuit has been examined using a switch matrix technique. A constant voltage stress of -4.0V was used to induce a low level of degradation to the 2.0nm gate oxide of the pMOSFET. Characteristics of the CMOS NOR logic circuit following gate oxide degradation are analyzed in both the DC and V-t domains. The NOR gate rise time increases by approximately 30%, which may lead to timing or logic errors in high frequency digital circuits. Additionally, the voltage switching point of the NOR logic circuit shifts by 9% which could affect operation of analog or mixed signal designs. This shift in NOR logic circuit performance is correlated to an increased channel resistance of the stressed pMOSFET.

Introduction

As gate oxide thicknesses (t_{ox}) are scaled below 2.0nm, the effects of gate oxide (*GOX*) degradation become progressively more important, due in large part to an increased gate leakage current. Recent studies have focused on the effects of *GOX* degradation on CMOS inverter performance [1-8], yet reports on physical *GOX* degradation effects on other CMOS logic circuits, such as the NOR logic circuit, cannot be found. Additionally, much of the focus of studies on inverter performance has been on the voltage transfer characteristics (DC measurement) exclusive of time-domain circuit response [1, 2, 7, 8]. In these studies, a circuit level stress is applied to a monolithic structure thereby limiting the amount and the type of degradation induced to one or both of the MOSFETs. Because access to the individual MOSFETs is not possible in a monolithic structure, direct characterization of the individual MOSFETs is also not possible.

Only a few studies of simple integrated circuit building blocks (SICBBs), such as the inverter and NAND logic circuits, have used a technique in which direct characterization of individual MOSFETs before and after stress is possible [3, 6, 9]. A switch matrix technique is employed in these studies to correlate degraded MOSFET parameters such as drive current (I_D) and threshold voltage (V_{TH}) to circuit performance in the DC and voltage-time domain (V-t). Additionally, only a preliminary study has been performed on the NOR logic circuit in which the capacitive loading related to this technique has not been fully investigated [10].

This study investigates the NOR logic circuit performance in the DC and V-t domains following degradation of a single pMOSFET with t_{OX} of 2.0 nm using the switch matrix technique. Specifically, the reliability assessment of low-level *GOX* degradation (e.g., negative bias temperature instability [11-13], stress induced leakage current [14], progressive breakdown [15, 16], etc.), termed wearout in this paper, is investigated to help assess the impact of pMOSFET wearout on NOR logic circuit operability. The capacitive loading associated with the switch matrix technique is also investigated.

Theory of Proposed Characterization Technique

When dealing with small scale devices, the size of the capacitive load placed on the device is of great concern as the ability of the device to drive the load comes into question. Furthermore, the speed of small scale devices can easily be inhibited by the capacitive load due to charging effects. This could affect the ability to achieve high speed digital circuits using small scale devices. In a typical IC, several circuits (e.g. output buffers, charge pumps, and loop filters) can heavily load the output of a NOR logic circuit in both digital and mixed signal applications. The capacitive load (C_L) for these circuits can be 1 pF or larger. Therefore, it is a definite concern that the large C_L associated with the switch matrix technique could affect trends in fractional percent change (*%*Δ) of V-t data, e.g. *%*Δ *rise time (*t_r*)*, when assessing the reliability of a SCIBB configured using this technique. Hence, simulations were performed using a 50 nm CMOS SPICE model on a NAND logic circuit, which demonstrates for changes in C_L ranging from 10 fF up to 1 nF (but holding C_L constant during each simulation), $\%\Delta t_r$ remains the same (Figure 1). Wearout in the single pMOSFET was simulated by shifting the V_{TH} SPICE model parameter to match empirical data obtained by Ogas *et al.* [9].

Furthermore, using transition times associated with the digital model of a MOSFET as described

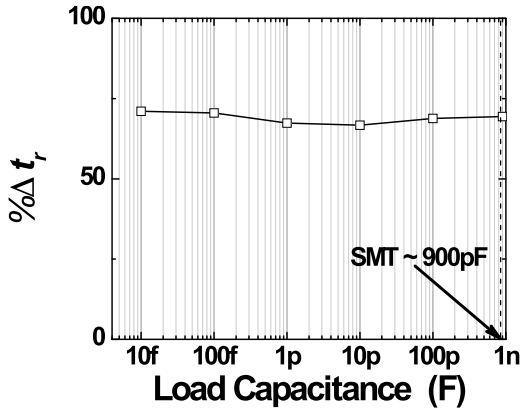


Figure 1. %Δt_r simulated as a function of C_L

by Baker [17], it is shown mathematically that $\%\Delta t_r$ is independent of C_L. The digital model output t_r of a MOSFET can be expressed as (1):

$$t_r \propto R_{CH} C_L \tag{1}.$$

A change in R_{CH} can be directly related to a change in t_r if a capacitive load on a NOR logic gate remains constant. Hence, equation 1 can then be written in terms of a change in R_{CH} (ΔR_{CH}) given by:

$$\Delta t_r \propto \left(R_{CH,Fresh} - R_{CH,wearout}\right) C_L \tag{2}$$

or,

$$\Delta t_r \propto \left(\Delta R_{CH}\right) C_L \tag{3}$$

To obtain a fractional percentage, equation (2) is expanded and divided by the fresh value or t_r (where fresh is defined as prior to wearout) resulting in:

$$\%\Delta t_r \propto \frac{R_{CH,Fresh} C_L - R_{CH,wearout} C_L}{R_{CH,Fresh} C_L} \propto \frac{R_{CH,Fresh} - R_{CH,wearout}}{R_{CH,Fresh}} \propto \%\Delta R_{CH} \tag{4}$$

Therefore, simulations and mathematical derivations indicate the switch matrix technique is well suited to examine the reliability of SICBBs in the V-t domain since C_L for this technique is about 900 pF and remains constant throughout testing.

Experimental

The metal oxide semiconductor (MOS) devices used in this study were fabricated by SEMATECH using 0.1 µm CMOS technology and have a t_{OX} of 2.0 nm. The MOSFETs configured in the NOR logic circuit have a width and length of 10 µm and 0.1 µm, respectively and an oxide area (A_{OX}) of $1x10^{-8}$ cm^2. The Agilent semiconductor characterization system used to make measurements is described in previous studies [6]. By applying a constant voltage stress (CVS) of -4 V to the gate of the device, *GOX* degradation is induced in a single pMOSFET. CVS is applied in cycles of 600 seconds for five consecutive cycles, with interruptions for device and circuit characterization at room temperature, approximately 298 K. The remaining MOSFETs of the NOR logic circuit are not stressed.

Six NOR logic circuits, with a single degraded pMOSFET configured in 1 of 2 positions (Figure 2), were analyzed prior to and after *GOX* degradation is induced in the pMOSFET. The four input/output (I/O) NOR logic circuit states investigated are summarized in Table 1. States are labeled with the pMOSFET position followed by the I/O state. The configurations shaded in Table I correspond to transitions in the NOR logic with the degraded pMOSFET in either the upper or lower position. The results are presented for these two configurations in which pMOSFET wearout affects the circuit performance in the voltage-time domain (V-t). Data collected and analyzed for the NOR logic circuit includes Vt data and voltage transfer characteristics (VTCs). V-t results allow for the evaluation of t_r by measuring the time required for the output voltage to transition from 10 % to 90% of the final output value [17].

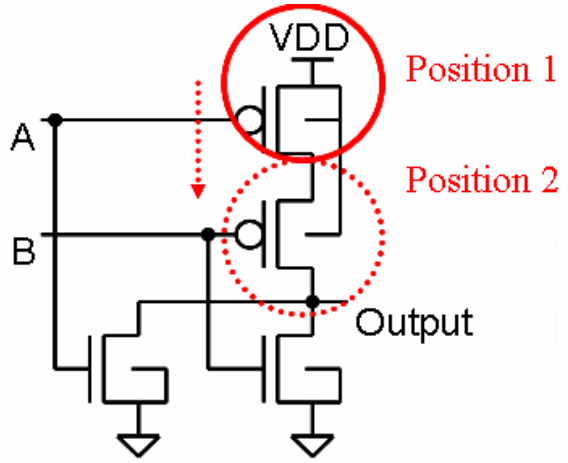


Figure 2. NOR logic circuit with stressed pMOSFET positions circled

TABLE I
NOR GATE INPUT CONFIGURATIONS INDICATING I/O STATE

Position	Configuration	Input/Output			
		1	2	3	4
1,2	Input A	VDD	**GND**	Pulse	**Pulse**
	Input B	Pulse	**Pulse**	VDD	**GND**
	Output	0	**0,1**	0	**0,1**

Grey = positions affected by degradation. 0,1 = output transition

Data collected for the degraded pMOSFET includes maximum drain current ($I_{D,MAX}$), threshold voltage (V_{TH}), and small-signal source-to-drain conductance (g_{sdm}). The linear extrapolation technique is used to determine the pMOSFET V_{TH} [17]. Additionally, gate leakage current (I_G-V_G) is measured following each stress cycle to verify operation in the wearout regime. Previous studies on inverter circuits comprised

of MOSFET devices with a t_{OX} of 2.0 nm and an A_{OX} of 1x10^{6} cm^2 provide a reference for expected wearout and breakdown regimes [4]. Ogas *et al.* provide further description of the measurement and choice of applied voltages in previous work [4]. The g_{sdm} is measured using a small-signal conductance measurement similar to that described by Kong *et al.* [18]. The small-signal conductance measurement used in this study differs from Kong *et al.*'s method in that a 14mV RMS test signal at 1MHz is applied to the drain of the device under test, while the voltage sources of the Agilent 4156C parameter analyzer provide the gate and substrate biases through connections configured using the Agilent E5250A switch matrix.

Results

The NOR logic circuit and pMOSFET results reported include the %Δ from fresh to wearout in terms of mean and standard deviation (i.e. associated error), as presented in Table 2. Sources of error associated with the NOR V-t measurements include differences in MOSFET characteristics between the devices used to configure the NOR logic circuit. Sources of error associated with the devices are due to the statistical nature of degradation in the channel.

TABLE 2. NOR Logic Circuit and Device Statistics

I-V Parameter	Mean	Standard Deviation
NOR V-t (1-2)	23.8%	5.73%
NOR V-t (1-4)	27.2%	7.25%
NOR V-t (2-2)	30.5%	6.24%
NOR V-t (2-4)	27.1%	6.20%
NOR VTC (1-4)	9.28%	1.56%
NOR VTC (2-2)	8.49%	1.28%
$I_{D,MAX}$	43.4%	7.57%
V_{TH}	23.0%	4.52%
g_{sdm}	29.5%	8.07%
R_{CH}	43.6%	18.2%

A. NOR Circuit

V-t characteristics are examined for configurations 1-2, 1-4, 22, and 2-4 (Table-1) following each pMOSFET stress cycle. As expected, these V-t configurations are the only configurations affected by pMOSFET wearout. Figure 3 shows the typical NOR V-t response for these configurations. The NOR V-t response for configuration 1-2 (Figure 3), shows an increase in %Δt_r of approximately 24 %, relative to the Fresh response. The results for the remaining configurations are presented in Table-2.

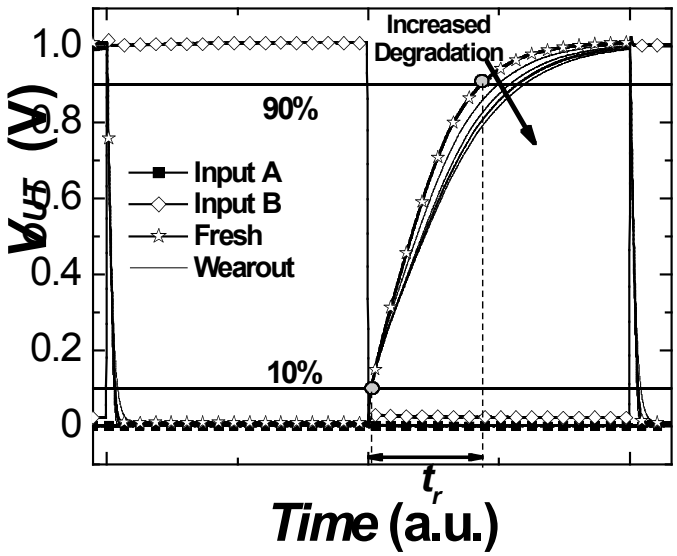


Figure 3. Voltage-time domain (V-t) results for the NOR logic circuit following wearout in a single pMOSFET. Significant changes in rise time (t_r) from fresh to wearout are apparent as shown for configuration 1-2. Similar results were observed for configurations 1-4, 2-2, and 2-4. The time axis is displayed in arbitrary units (a.u.).

Figure 4 shows the typical NOR VTC response for configuration 22. A shift to the left in the VSP is observed which is indicative of pMOSFET wearout. Configuration 1-4 results in a shift of the VSP to the left by 9.28% while configuration 2-2 (Fig.4) exhibits a shift of about 8.49% relative to the fresh condition. As expected, configurations 1-2 and 2-4 are not affected by pMOSFET wearout as the degraded device is held at ground effectively preventing the degraded pMOSFET from significantly affecting the VTC in the DC domain.

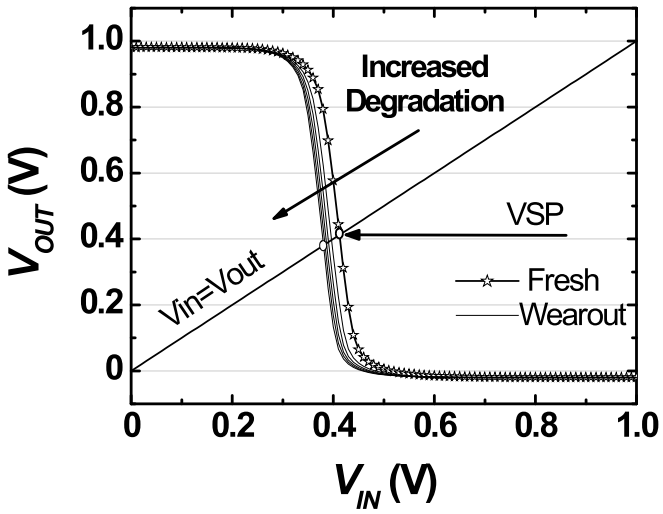


Figure 4. Voltage transfer characteristics (VTC) results for the NOR circuit in configuration 2-2. A shift to the left in the voltage switching point (*VSP*) is observed from fresh to wearout. Similar results are observed for configuration 1-4.

B. pMOSFET

Following induced wearout, the pMOSFET DC characteristics exhibit an increase in V_{TH} by 23.0% (Fig. 5), a decrease in $I_{D,MAX}$ (Fig. 5 inset) by 43.4 %, and a decrease in g_{sdm} (Fig. 6) by 29.5 % relative to the fresh condition.

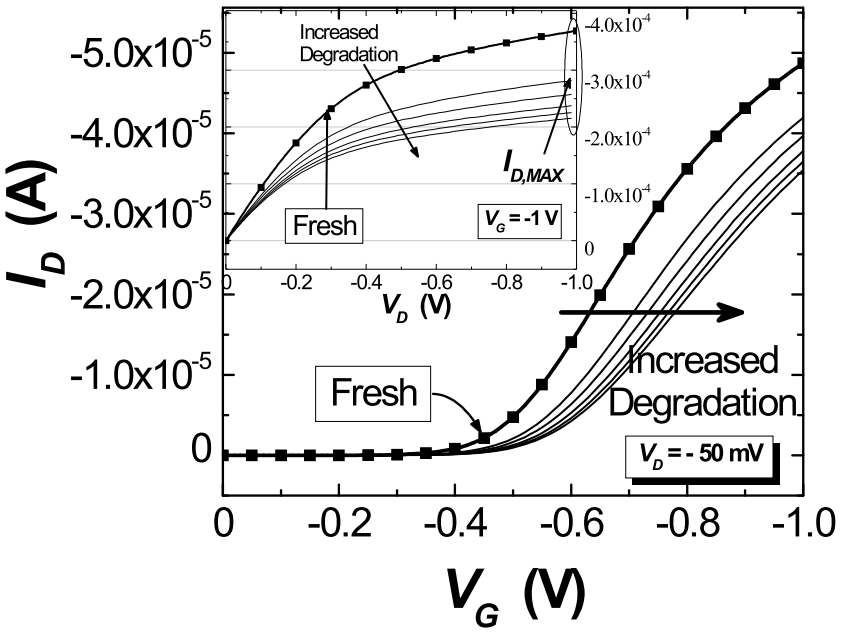


Figure 5. Typical pMOSFET linear drain current versus gate voltage (linear I_D-V_G) results for fresh through wearout. A shift to the right from fresh to wearout is indicative of increased V_{TH}. (The inset illustrates that typical pMOSFET drain current versus drain voltage (I_D-V_D) results for fresh through wearout showing a decrease in $I_{D,MAX}$ with increasing wearout, in which $I_{D,MAX}$ data is measured at V_D=V_G=VDD. The gate voltage is held constant at -1 V throughout the test.)

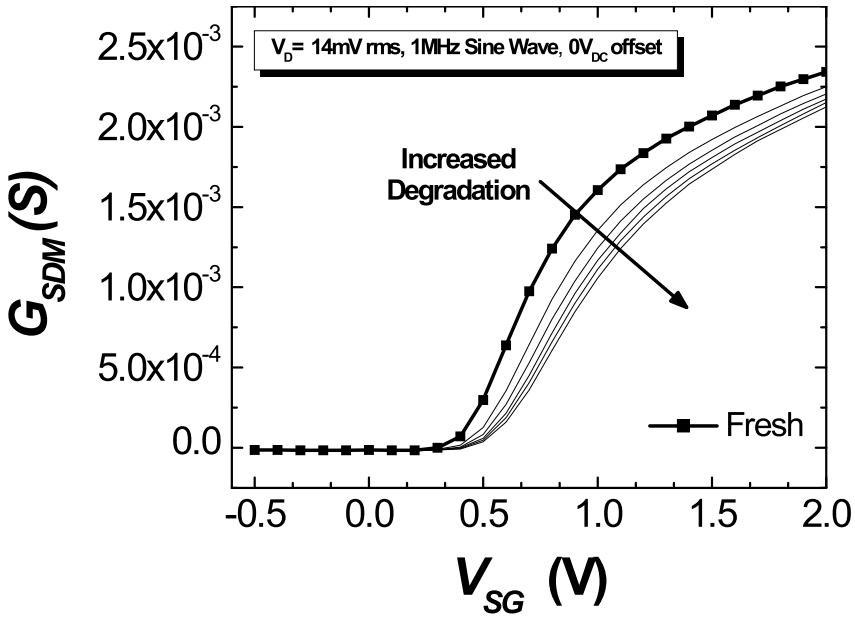


Figure 6. Results of small-signal conductance measurement showing a decrease in source-drain conductance as a function of V_{SG} from fresh to wearout. Results are measured at V_G=VDD=-1V.

Discussion

A.NOR Logic Circuit

The degree of degradation observed in the time domain by the NOR logic circuit appears to be more significant than the degradation exhibited in the VTCs under equivalent test conditions (Figs. 3 and 4) as the VTCs display a full logic transition with a smaller shift in circuit performance relative to the fresh condition. Cheek *et al*. reported similar results following inverter circuit analysis [6]. Taur and Ning describe the pMOSFET as the "pull-up" device and the nMOSFET as the "pull-down" device[18]. Therefore, a degraded pMOSFET is expected to affect only the t_r [3] and a degraded nMOSFET affects the fall time (t_f). Hence, a change in t_f is not expected nor is it observed. A similar correlation can be made for the NOR VTCs from Fig. 4, in which the leftward shift of the VSP is directly related to a decrease in pMOSFET performance. This can be explained intuitively by comparing the strength of the pMOSFETs to the nMOSFETs. As the pMOSFET is degraded it becomes weaker and the nMOSFETs of the circuit begin to dominate the VTC allowing for an earlier "pull down" effect or an earlier VSP. Similar results were observed for inverters in which a degraded pMOSFET and a fresh nMOSFET shifted the VSP to the left [4, 6].

B. pMOSFET

By using the switch matrix technique, it is seen that the NOR logic circuit response is significantly impacted by single pMOSFET wearout. The degraded pMOSFET characteristics suggest degradation in the channel as the cause for the large change in t_r as both V_{TH} and $I_{D,MAX}$ are related to channel resistance. To ensure traditional breakdown events have not occurred and influenced results, the I_G-V_G data of the degraded pMOSFET is compared to that of a device progressively degraded to a traditional breakdown event (Fig. 7). The wearout region investigated (Fig. 7) corresponds to the region of operation for the stressed pMOSFETs used in this study. It should be noted that a progressive increase in current is observed in the CVS test which may be an indication of progressive breakdown [12, 20].

C. Channel Resistance

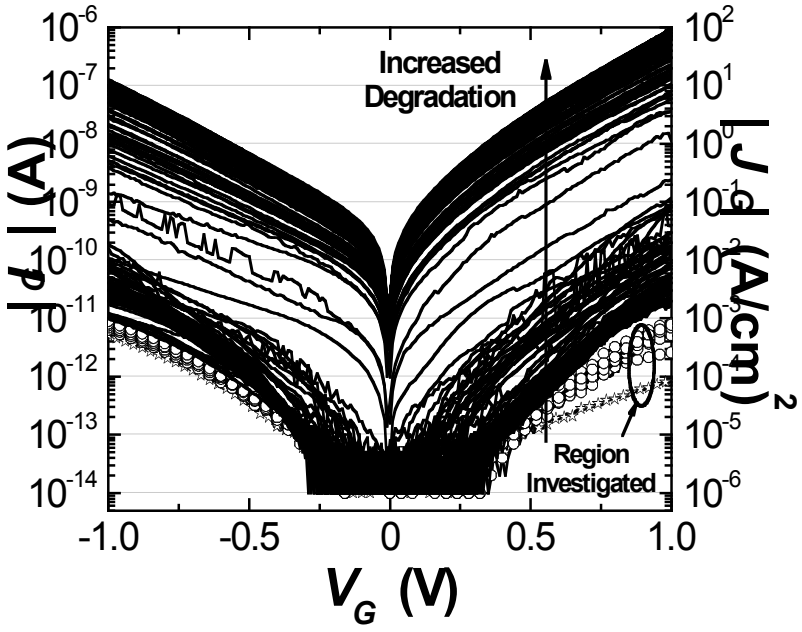


Figure 7. Log plot of the gate current versus gate voltage response a degraded pMOSFET progressively stressed to hard breakdown. The encircled wearout region illustrates the Fresh to wearout I_G-V_G response for the degraded pMOSFETs used in this study. The full range of oxide degradation is shown to highlight the low-leakage regime which suggests that a traditional oxide breakdown is not being induced in the pMOSFETs [24]. The arrow indicates the progression of increased degradation.

R_{CH} was investigated experimentally to confirm the direct relation between $\%\Delta t_r$ and $\%\Delta R_{CH}$. $\%\Delta R_{CH}$ values were obtained by measuring g_{sdm} using a small-signal conductance measurement as described by Kong *et al.* [18]. To verify this technique is applicable to the pMOSFET, a similar derivation for g_{sdm} is calculated from the DC drain current equation of an pMOSFET based upon the gradual channel approximation [21]. These calculations result in:

$$g_{sdm} = \frac{1}{R_{SD} + \frac{1}{\beta (V_{SG} + V_{TH})}} \tag{4}$$

where ,

$$R_{CH} = \frac{1}{\beta (V_{SG} + V_{TH})} \tag{5}$$

and,

$$\beta = \frac{\mu_{eff} C_{OX} W_{eff}}{L_{eff}} . \tag{6}$$

R_{SD} is the total parasitic source and drain resistance measured in series with R_{CH}. R_{SD} can be assumed to be small compared to R_{CH} [21, 22] and to remain fairly constant after CVS, as the majority of the pMOSFET degradation occurs in the channel [23]. Therefore, equation 4 can be approximated by:

$$g_{sdm} \approx \frac{1}{R_{CH}} . \tag{7}$$

or equivalently,

$$R_{CH} \approx \frac{1}{g_{sdm}} \quad (8).$$

A correlation between $\%\Delta R_{CH}$ and g_{sdm} can be derived using equation 8. ΔR_{CH} can be written as:

$$\Delta R_{CH} \approx \frac{1}{g_{sdm,Fresh}} - \frac{1}{g_{sdm,Wearout}} \quad (9).$$

Using a common dominator (9) can be written as:

$$\Delta R_{CH} \approx \frac{-\Delta g_{sdm}}{g_{sdm,Wearout}\, g_{sdm,Fresh}} \quad (10).$$

Dividing by $R_{CH,Fresh}$ to convert (10) to percent change results in:

$$\%\Delta R_{CH} = \frac{\Delta R_{CH}}{R_{CH,Fresh}} = \frac{-\Delta g_{sdm}}{g_{sdm,Wearout}}, \quad (11)$$

which was shown to be proportional to $\%\Delta t_r$ in both equation (3) and experimentally in Fig. 8.

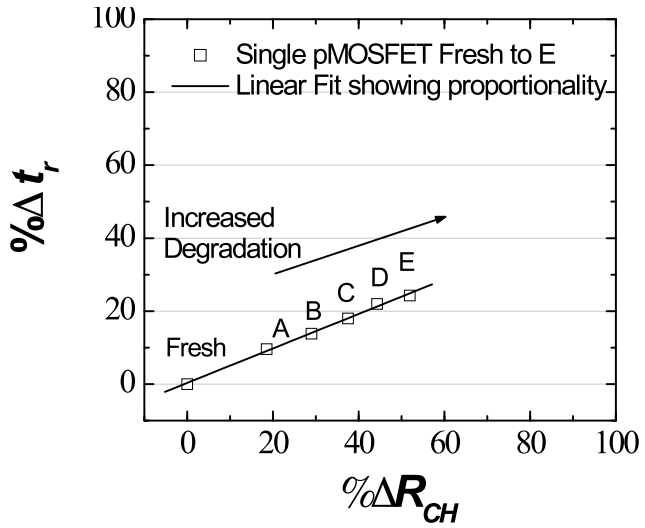


Figure 8. $\%\Delta R_{CH}$ of a single degraded pMOSFET and corresponding $\%\Delta t_r$ of the associated NOR logic circuit. Linear fit shows the direct proportionality between $\%\Delta R_{CH}$ and $\%\Delta t_r$.

Conclusions

The results reported show that wearout in one pMOSFET of a NOR logic circuit leads to a significant increase in t_r attributed to a decrease in g_{sdm} or equivalently, an increase in R_{CH}. The changes in NOR logic circuit performance in the V-t domain may affect the ability of the circuit to operate properly, particularly in applications requiring high speed switching. Furthermore, this study suggests that the NOR circuit configuration is less sensitive to single pMOSFET wearout than the NAND circuit. This study further validates the use of the switch matrix technique for circuit reliability analysis in the Voltage-time domain. It has also been proposed and shown that the small-signal conductance measurement can be employed using a switch matrix technique to characterize the reliability of SICBBs and MOSFETs. Additionally, it is shown that the relatively heavy capacitive load associated with the switch matrix technique does not affect the viability of the technique when characterizing devices and SICBBs.

Acknowledgments

The authors would like to thank Gennadi Bersuker and Rino Choi of SEMATECH Inc. in Austin, Texas for their technical guidance and contributions related to this project. Funding for the project was supported in part by the DoD Multidisciplinary University Research Initiative (MURI) program #F49200110374, NASA Idaho Space Grant, NASA Idaho EPSCoR, Idaho NSF EPSCoR Award #EPS-0132626, NSF MRI Award #0216312, DARPA Contract #N66001-01-C-80345, and NIH INBRE #P20RR16454.

References

[1] R. Rodriguez, J. H. Stathis, and B. P. Linder, "A model for gate-oxide breakdown in CMOS inverters," *IEEE Electron Device Letters*, vol. 24, pp. 114-116, 2003.

[2] R. Rodriguez, J. H. Stathis, and B. P. Linder, "Modeling and experimental verification of the effect of gate oxide breakdown on CMOS inverters," presented at IEEE International Reliability Physics Symposium, 2003.

[3] N. Stutzke, B. J. Cheek, S. Kumar, R. J. Baker, A. J. Moll, and W. B. Knowlton, "Effects of circuit-level stress on inverter performance and MOSFET characteristics," presented at IEEE International Integrated Reliability Workshop, 2003.

[4] M. L. Ogas, R. G. Southwick, B. J. Cheek, R. J. Baker, B. Gennadi, and W. B. Knowlton, "Survey of oxide degradation in inverter circuits using 2.0 nm MOS devices," presented at IEEE International Integrated Reliability Workshop, 2004.

[5] H. M. Huang, C. Y. Ko, M. L. Yang, P. J. Liao, J. J. Wang, A. Oates, and K. Wu, "Gate oxide multiple soft breakdown (multi-SBD) impact on cmos inverter," presented at IEEE International Reliability Physics Symposium, 2004.

[6] B. Cheek, N. Stutzke, S. Kumar, R. J. Baker, A. J. Moll, and W. B. Knowlton, "Investigation of circuit-level oxide degradation and its effect on CMOS inverter operation and MOSFET characteristics," presented at IEEE International Reliability Physics Symposium, 2004.

[7] R. Rodriguez, J. H. Stathis, B. P. Linder, R. V. Joshi, and C. T. Chuang, "Influence and model of gate oxide breakdown on CMOS inverters," *Microelectronic Engineering*, vol. 43, pp. 1439-1444, 2003.

[8] R. Rodriguez, J. H. Stathis, and B. P. Linder, "Effect and model of gate oxide breakdown on CMOS inverters," *Microelectronic Engineering*, vol. 72, pp. 34-38, 2004.

[9] M. L. Ogas, P.M. Price, J. Kiepert, R. J. Baker, G. Bersuker, and W. B. Knowlton, "Degradation of rise time in NAND gates using 2.0 nm gate dielectrics," presented at IEEE International Integrated Reliability Workshop, 2005.

[10] T. L. Gorseth *et al.* "Preliminary Study of NOR Digital Response to Single pMOSFET Dielectric Degradation", presented at the Workshop on Microelectronic Devices, 2006.

[11] M. Denais, V. Huard, C. Parthasarathy, G. Ribes, F. Perrier, N. Revil, and A. Bravaix, "Interface trap generation and hole trapping under NBTI and PBTI in advanced CMOS technology with a 2-nm gate oxide," *IEEE Transactions on Device and Materials Reliability*, vol. 4, pp. 715-722, 2004.

[12] A. Haggag, N. Liu, D. Menke, and M. Moosa, "Physical model for the power-law voltage and current acceleration of TDDB," *Microelectronics Reliability*, vol. 45, pp. 1855-1860, 2005.

[13] J. H. Stathis and S. Zafar, "The negative bias temperature instability in MOS devices: A review," *Microelectronics Reliability*, vol. 46, pp. 270-286, 2006.

[14] B. E. Weir, P. J. Silverman, D. Monroe, M. A. Krisch, M. A. Alam, G. B. ALers, T. W. Sorsch, G. L. Timp, F. Baumann, C. T. Liu, Y. Ma, and D. Hwang, "Ultra-thin gate dielectrics: They break down, but do they fail?," presented at IEEE International Electron Devices Meeting, 1997.

[15] H. C. Lin, D. Y. Lee, and T. Y. Huang, "Breakdown modes and their evolution in ultrathin gate oxides," *Japanese Journal of Applied Physics*, vol. 41, pp. 5957-5963, 2002.

[16] A. Cester, A. Paccagnella, G. Ghidini, S. Deleonibus, and G. Guegan, "Collapse of MOSFET drain current after soft breakdown," *IEEE Transactions on Device and Materials Reliability*, vol. 4, pp. 63-72, 2003.

[17] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, vol. 2: IEEE Press: Wiley-Interscience, 2005, pp. 278, 317-318.

[18] F. C. J. Kong, Y. T. Yeow, and Z. Q. Yao, "Extraction of MOSFET threshold voltage, series resistance, effective channel length, and inversion layer mobility from small-signal channel

conductance measurement," *IEEE Transactions on Electron Devices*, vol. 48, pp. 2870-2874, 2001.
[19] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Boston: Cambridge University Press, 1998, pp. 224-279.
[20] F. Monsieur, E. Vincent, D. Roy, S. Bruyere, J. C. V. il, G. Pananakakis, and G. Ghibaudo, "A thorough investigation of progressive breakdown in ultra-thin oxides. Physical understanding and application for industrial reliability assessment," presented at IEEE International Reliability Physics Symposium, 2002.
[21] Y. Taur, "MOSFET channel length: extraction and interpretation," *IEEE Transactions on Electron Devices*, vol. 47, 2000.
[22] M. C. Ozturk, "Source/drain junctions and contacts for 45nm CMOS and Beyond," presented at International Conference on Characterization and Metrology for ULSI Technology, 2005.
[23] F. Crupi, B. Kaczer, R. Degraeve, A. D. Keergieter, and G. Groeseneken, "A comparative study of the oxide breakdown in short-channel nMOSFETs and pMOSFETs stressed in inversion and in accumulation regimes," *IEEE Transactions on Device and Materials Reliability*, vol. 3, 2003.
[24] D. J. Dumin, "Oxide wearout, breakdown, and reliability," *International Journal of High Speed Electronics and Systems*, vol. 11, pp. 617-718, 2001.