K-DELTA-1-SIGMA MODULATORS FOR WIDEBAND ANALOG-TO-DIGITAL CONVERSION

by

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ABSTRACT

As CMOS technology scales, the transistor speed increases enabling higher speed communications and more complex systems. These benefits come at the cost of decreasing inherent device gain, increased transistor leakage currents, and additional mismatches due to process variations. All of these drawbacks affect the design of high-resolution analog-to-digital converters (ADCs) in nano-CMOS processes. To move towards an ADC topology useful in these small processes a first-order K-Delta-1-Sigma (KD1S) modulator-based ADC was proposed. The KD1S topology employs inherent time-interleaving with a shared integrator and K-quantizing feedback paths and can potentially achieve significantly higher conversion bandwidths when compared to the traditional switched-capacitor delta-sigma ADCs. The shared integrator in the KD1S modulator settles over a half the clock period and the op-amp is designed to operate at the base clock frequency.

In this dissertation, the first-order KD1S modulator topology is analyzed for the effects of the non-idealities introduced by the K-path operation of the switched-capacitor integrator. Then, the concept of KD1S modulator is extended to higher-order modulators in order to achieve superior noise-shaping performance. A systematic synthesis method has been developed to design and simulate higher-order KD1S modulators at the system level. In order to demonstrate the developed theory, a prototype second-order KD1S modulator has been designed and fabricated in a 500-nm CMOS technology.

The second-order KD1S modulator exhibits wideband noise-shaping with an SNDR of 42.7 dB or 6.81 bits in resolution for $K_{path} = 8$ paths, an effective sampling rate of $f_{s,new} = 800$ MHz, effective oversampling ratio $K_{path} \cdot OSR = 64$ and a signal bandwidth of 6.25 MHz. The second-order KD1S modulator consumes an average current of 3.0 mA from the 5 V supply and occupies an area of 0.55 mm^2.

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CHAPTER 1 INTRODUCTION

Continued CMOS scaling has enabled ever increasing device speeds leading to numerous applications in wireless, wireline and optical communication. The integrated circuit technologies used to manufacture analog-to-digital converters (ADCs) are shrinking to enable more system functionality in a smaller chip area. This reduction in size comes at the cost of greater manufacturing variances, including transistor characteristics, which limit the availability of precise components often required in an ADC. Further, the large increase in the number of wireless communication standards call for processing of the electromagnetic spectrum from 900 MHz to the GHz's range [2]. The applications include cellular telephony (GSM, EDGE, WCDMA, etc.), ultra-wide band communication (UWB), personal area networks (Bluetooth, ZigBee, etc.), Wireless LAN, WiMAX and Cognitive Radio [3]. Another application of interest is the development of a low-power single-chip software defined radio (SDR) which requires GHz rate data conversion. Figure 1.1 shows the classification of ADCs based upon their bit resolution and conversion bandwidth specifications compiled from [4]. As illustrated in this figure, the fundamental limitation on the achievable ADC resolution is set by the clock jitter and thermal noise.

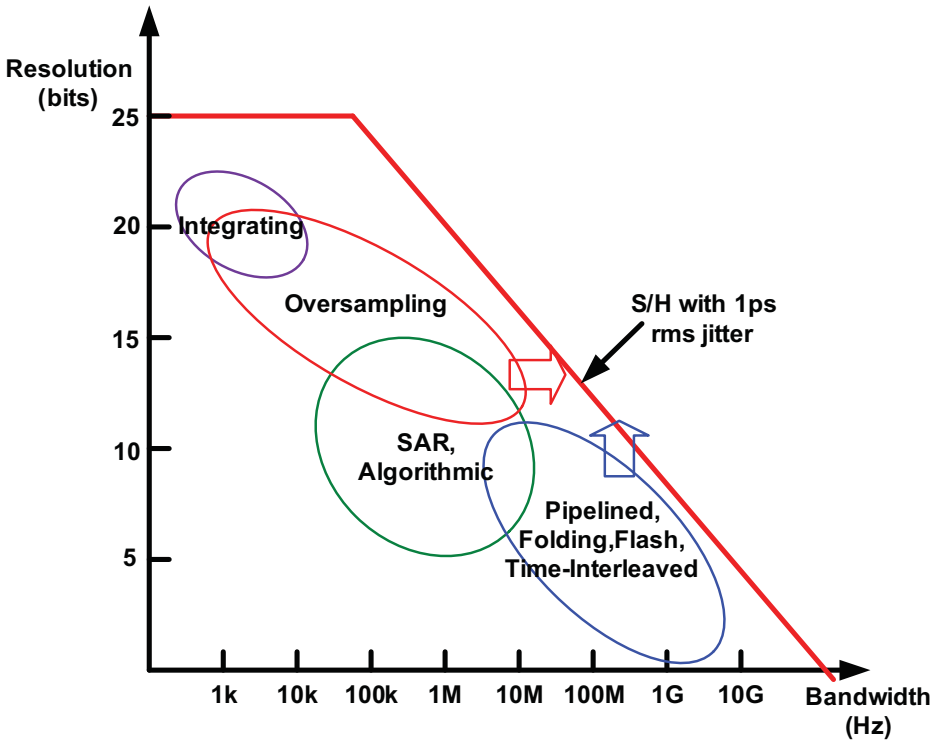

Figure 1.1: Classification of Analog-to-Digital Converters based upon their resolution and conversion bandwidth.

Typically in CMOS technology, Flash ADCs have been used for higher-speed data conversion from 100's of MHz to several GHz's at lower resolution (5-6 bits), pipelined ADCs for moderate resolution (10-12 bits) for 100-250 MHz range and oversampling (Delta-Sigma) ADCs for lower bandwidths (kHz's to MHz's) and high-resolution (12- up to 24 bits).

CMOS scaling benefits the Flash ADCs and the oversampling ADCs by realizing increasing higher sampling rates. However, the resulting high-speed of scaled CMOS transistors is concomitant with the degrading intrinsic transistor gain ($g_m \cdot r_o$), pronounced process variations and poor component matching [5]. In order to design

high-resolution pipelined ADCs in nano-CMOS with significant device offsets, complicated digital-calibration schemes are employed at the cost of increased area, latency and power consumption [1, 6, 7]. Thus, it is imperative to further explore ADC topologies which are inherently tolerant to device-mismatches, lower amplifier gain and other circuit-imperfections in nano-CMOS.

1.1 Motivation

Delta-sigma modulation based ADCs which employ oversampling and a feedback architecture offer possibilities of attaining higher dynamic range as we scale further into the nano-CMOS regime. However due to oversampling, their conversion rates are significantly lower than their Nyquist-rate counterparts. Numerous attempts have been made to employ multiple delta-sigma modulators in parallel (or by using time-interleaving) to achieve Nyquist-rate data conversion. These architectures have their own deficiencies resulting from the path mismatches and a linear increase in power consumption with the number of parallel channels [8].

Recently there has been activity in employing delta-sigma ADCs for next-generation wireless applications which require over 60 dB of dynamic range and greater than 25 MHz conversion bandwidth. Several continuous-time delta-sigma architectures have been proposed for lower power (less than 20 mW) for such wireless applications [9, 10]. Also, there have been efforts in designing reconfigurable delta-sigma ADCs for multi-standard operation [11].

This dissertation analyzes a new noise-shaping topology, called the *K*-Delta-1-Sigma (KD1S) modulator, for wideband conversion which was disclosed in [12]. The KD1S topology employs time-interleaved sampling with a shared integrator. The interleaved single-bit quantizers (which is simply an array of comparators) employed in the KD1S modulator allow very high-speed sampling with lower implementation complexity. Due to single-bit quantization, the feedback digital-to-analog converters (DACs) in the modulator are inherently linear and thus the complexity of element mismatch shaping is avoided. Therefore, the KD1S modulator architecture offers several advantages over a multi-bit modulator employing the same number of comparators. However, the quantizer in the KD1S modulator requires the comparator to operate at a higher speed, set by the effective sampling rate of the modulator, which is favorable in the nano-CMOS technologies. In summary, the KD1S architecture trades off high comparator speed with lower implementation complexity of the quantizer and with the lower peformance requirements of the op-amps.

In the traditional time-interleaving ADC architectures, the phase skew, path-offset and gain-mismatch result in severe degradation in the achievable dynamic range and the signal-to-noise ratio (SNR). However in the KD1S modulator, the distortion due to the mismatch and phase skew in the time-interleaved sampling paths is averaged by the number of paths and by the oversampling ratio (OSR) for each path. The noise introduced into the signal band due to clock jitter is also averaged by the number of paths and the OSR which results in a higher SNR in the KD1S modulator. The KD1S

architecture for high-speed data conversion offers other advantages which are analyzed in detail in the subsequent chapters.

The first-order KD1S modulator architecture, presented in [13] and [14], has been extended to a generalized higher-order modulator. A systematic synthesis method for higher-order KD1S modulator has been presented. First- and second-order KD1S designed using this procedure has been fabricated in a 500-nm CMOS technology. The aim of this research is to determine the limitations of the KD1S topology.

1.2 Dissertation Organization

This dissertation covers a detailed theoretical analysis of the *K*-Delta-1-Sigma modulators along with a synthesis method for higher-order KD1S topologies. The effects of various circuit non-idealities and their influence on the KD1S performance have been detailed. The design and testing procedure for the prototype chips has been presented. The remaining dissertation has been organized as follows :

Chapter 2 provides a brief background on design issues involved in the time-interleaved analog-to-digital converters (TI-ADCs). The analytical results presented in this chapter are used in subsequent chapters to analyze the time-interleaved sampling structure inherent in the KD1S modulator.

Chapter 3 provides an introduction to delta-sigma modulators and describes the approaches to design wideband ADCs without employing complicated calibration in nano-CMOS processes.

Chapter 4 describes the KD1S modulator and details the effects of circuit non-idealities on the modulator performance. The KD1S modulator performance has been analyzed and simulated for circuit limitations like finite op-amp gain and unity-gain

frequency, slewing in op-amps and finite comparator delay. The effect of quantization noise folding due to path mismatch and clock phase skew is also analyzed.

Chapter 5 discusses the design of the second-order KD1S modulator, presents behavioral simulation results and details the effects of circuit non-idealities.

Chapter 6 presents a synthesis and simulation method for generalized higher-order KD1S modulators. A novel state-space embedding method for KD1S modulators has been developed for their rapid simulation and performance estimation.

Chapter 7 details the transistor level design of first- and second-order KD1S modulators, chip design and simulation, test board design and measurement results from the prototype chip.

Chapter 8 concludes the dissertation and discusses future directions for this research.

Appendix A provides the listing of the MATLAB codes used for signal processing throughout the dissertation.

CHAPTER 2 TIME-INTERLEAVED ANALOG-TO-DIGITAL CONVERTERS

The effective sampling-rate of analog-to-digital converters (ADCs) can be increased by operating multiple slower ADCs in parallel which results in a faster time-interleaved ADC (TI-ADC). This chapter presents detailed analysis for the TI-ADCs and the resulting non-idealities. The analytical results presented in this chapter will be applied to the analysis of KD1S modulators which employ time-interleaved sampling along with a shared loop-filter.

2.1 Time-Interleaved Analog-to-Digital Converters

Time-interleaving of slower ADCs in parallel is an attractive way to achieve an increase in the conversion rate [15]. Figure 2.1 illustrates the concept of time-interleaving ADCs. Here, M- ADCs operating at a frequency of f_s/M, called the *slices*, are clocked on the M-phases of a clock. The outputs of the slices are multiplexed to obtain output digital codes operating at an equivalent clock frequency of f_s. Thus, the speed requirements on the individual ADC slices are relaxed by a factor of M. The resulting increase in power and area of the time-interleaved ADC (TI-ADC) does not necessarily increase linearly with M when compared to the an equivalent single-path faster ADC. This is due to the fact that the op-amps in each of the slices require smaller bias currents, and also the op-amps can be shared across paths to reduce power consumption and area [5]. Thus, time-interleaving enables much higher speed than allowed by the CMOS

technology used for implementation of a single channel ADC. However, the mismatch between the parallel paths introduces distortion and lowers the resulting signal to noise and distortion ratio (SNDR). The dominant sources of error in TI-ADCs are the clock phase-skew, offset errors, gain and bandwidth mismatch across the paths [5, 15].

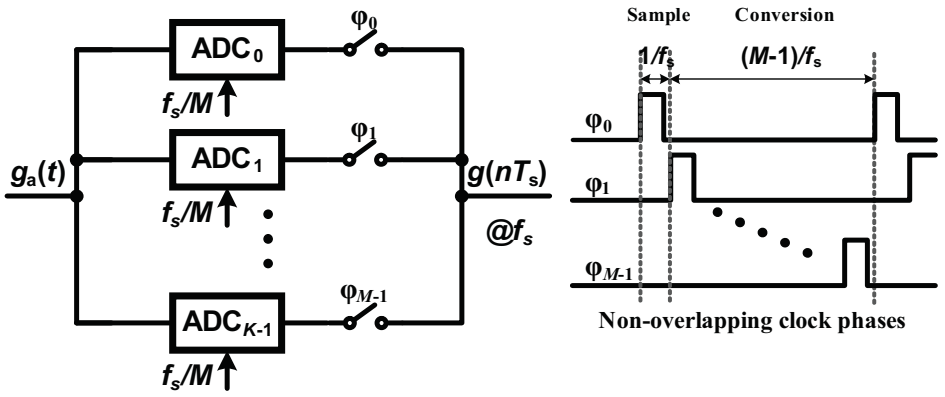

Figure 2.1: Time-interleaved ADCs and the corresponding clock phases.

Figure 2.2 depicts the sampling of an input sinewave by a time-interleaved ADC. Here, the samples in the channels $m = 0, ..., M-1$ are ideally sampled at the time instants $t_m, t_{m+M}, t_{m+2M}, \ldots$ where $t_m = mT$, and T is the equivalent sampling period of the TI-ADC. Because of the imperfections in the clock phases from skew and jitter, the sampling instants will vary from channel-to-channel. Assuming that the jitter noise for each of the clock phases is uncorrelated from each other and has a flat spectrum (white noise characteristics), the effect of aperture error due to jitter can be treated like the jitter noise for the overall TI-ADC. However, due to clock skew, the sampling instances will vary for each of the channel and is represented as [5, 16]

$$t_m = mT - r_m T \tag{2.1}$$

where r_m is the relative error in the sampling instant with respect to the overall sampling period ($T = \frac{1}{f_s}$), i.e. $r_m = \frac{T_{skew}}{T}$. A detailed mismatch analysis using non-linear sampling theory for TI-ADCs is provided in [5, 16], and is briefly derived and re-interpreted in this section for the benefit of the reader.

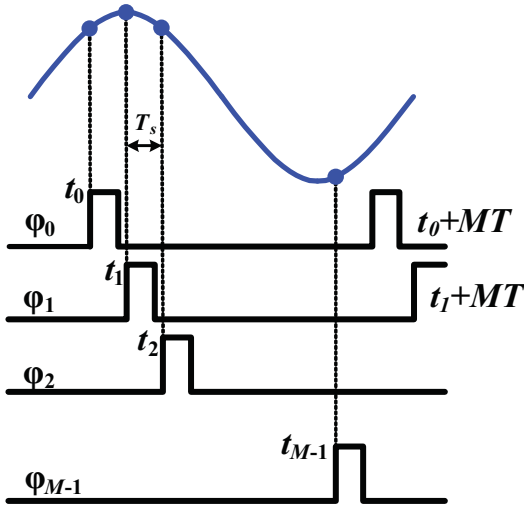

Figure 2.2: Sampling of an input sine wave by a time-interleaved ADC.

Let the analog input signal to the TI-ADC, $g_a(t)$ have its Fourier spectrum given by $G_a(f)$. Then the resulting Fourier transform of the output of the time-interleaved sampling system is given by the following double-summation [16]

$$G(f) = \frac{1}{MT}\sum_{m=0}^{M-1}\left[\sum_{k=-\infty}^{\infty} G_a\left(f-\frac{k}{MT}\right)e^{-j2\pi\left[f-\frac{k}{MT}\right]t_m}\right]e^{-j2\pi mfT} \tag{2.2}$$

which is rewritten in terms of r_m to give

$$G(f) = \frac{1}{T}\sum_{k=-\infty}^{\infty}\left[\frac{1}{M}\sum_{m=0}^{M-1} e^{-j2\pi\left[f-\frac{k}{MT}\right]r_m T}e^{-j2\pi\frac{km}{M}}\right]G_a\left(f-\frac{k}{MT}\right) \tag{2.3}$$

Equations 2.2 and 2.3 are two generalized representations of the spectra for a non-uniformly sampled signal [16]. If there are no channel-mismatches and timing errors

in the TI-ADC, then we can simplify Equation 2.3 with $r_m = 0$, and using the result $\sum e^{-j2\pi\frac{km}{M}} = M$ for $k = 0, M, 2M, \ldots$, results in the spectrum

$$G(f) = \frac{1}{T}\sum_{k=-\infty}^{\infty} G_a\left(f - \frac{k}{T}\right) \tag{2.4}$$

which is same as the spectrum for a uniformly sampled signal with a time-period T.

2.2 Non-uniformly Sampled Sinusoidal

Sinusoidal signals are generally used as test input signals for ADCs and are used to characterize the resulting distortion and inter-mixing in the system. Thus, it's convenient to derive the spectrum of a non-uniformly sampled sinusoidal signal for use in deriving the characteristics of a TI-ADC. For a complex sinusoidal $e^{j2\pi f_0 t}$, with a frequency f_0, the spectrum is given as

$$G_a(f) = \delta(f - f_0) \tag{2.5}$$

Substituting Equation 2.5 in Equation 2.3, we get the resulting discrete-time spectrum [16]

$$G(f) = \frac{1}{MT}\sum_{m=0}^{M-1}\left[\sum_{k=-\infty}^{\infty}\delta\left(f - f_0 - \frac{k}{MT}\right)e^{-jr_m 2\pi\frac{f_0}{f_s}}e^{-j2\pi\frac{km}{M}}\right] \tag{2.6}$$

Now, let's define an amplitude sequence $A(k)$, $k = 0, 1, ..., M$, such that [16]

$$A(k) = \sum_{m=0}^{M-1}\left(\frac{1}{M}e^{-jr_m 2\pi\frac{f_0}{f_s}}\right)e^{-j2\pi\frac{km}{M}} \tag{2.7}$$

then we can rewrite Equation 2.6 as [16]

$$G(f) = \frac{1}{T}\sum_{k=-\infty}^{\infty} A(k)\delta\left(f - f_0 - \frac{k}{MT}\right) \tag{2.8}$$

Equations 2.6 and 2.8 comprise the spectral representation of the non-uniformly sampled complex sinusoidal signal [16]. This resulting discrete-time sinusoidal representation has the following properties [16]:

1. From Equation 2.7, it can be observed that $A(k)$ is periodic with an index k and a period of M. Thus, the spectrum $G(f)$ given by Equation 2.8 is periodic with a period $1/T = f_s$.

2. A single period of the spectrum (from $f = 0$ to $1/T$) is comprised of M spectral tones, separated by a frequency difference of f_s/M. The main sampled signal is located at f_0 with a magnitude $|A(0)|$, while the m^{th} tone is located at $f_0 + \frac{m}{M} f_s$ with a magnitude given by $|A(m)|$. The TI-ADC sampled spectrum is illustrated in Figure 2.3.

3. Note that the discrete sequence $A(k)$ is the discrete-time Fourier transform (DFT) of the sequence $a(m) = \frac{1}{M} e^{-jr_m 2\pi \frac{f_0}{f_s}}$, $m = 0, 1, ..., M-1$. Then, by using the Parseval's theorem [17] we have

$$\sum_{k=0}^{M-1} |A(k)|^2 = \sum_{m=0}^{M-1} |a(m)|^2 = 1 \tag{2.9}$$

   The sequence $a(m)$ represent the relative complex ratio of the mismatch tones in the TI-ADC, located at frequencies $f_0 + \frac{m}{M} f_s$. Also we know that for a DFT, $A(M-k) = A(k)$ due to the circular symmetry property [17].

4. Equation 2.9 leads to the simple calculation of the SNDR for non-uniform sampling, given as

$$SNDR_{ns} = 10\log_{10}\left(\frac{|A(0)|^2}{1-|A(0)|^2}\right) dB \tag{2.10}$$

Based on the equations derived in the last section, we can now derive the effects of various mismatch errors in TI-ADCs.

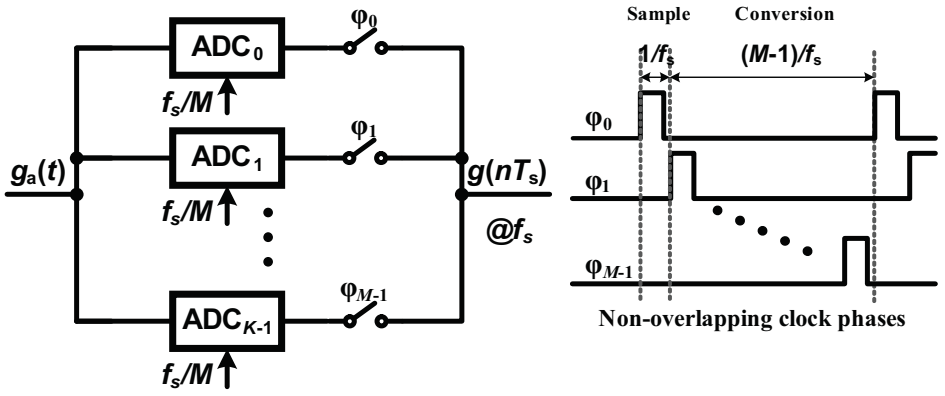

Figure 2.3: Spectrum of a non-uniformly sampled complex sinusoid.

From Equation 2.8, we can write the non-uniformly sampled spectrum for a real input signal $a_0 \cdot sin(2\pi f_{in}t)$ as

$$G(f) = \frac{a_0}{2jT}\sum_{k=-\infty}^{\infty}\left[A(k)\delta\left(f+f_{in}-\frac{k}{MT}\right) - A^*(M-k)\delta\left(f-f_{in}-\frac{k}{MT}\right)\right] \tag{2.11}$$

which implies that the spectrum of the input signal repeats at frequencies $f_{in}+\frac{k}{M}f_s$, $k = 0,...,M-1$ with a multiplier given by $|A(k)| = |A^*(M-k)|$, where the index $k = 1,...,M-1$ corresponds to the location of the distortion tones.

2.2.1 Path Offset Errors

Assuming that there is no phase skew ($r_m = 0$) or gain mismatch in the TI-ADC channels but that there exist fixed offsets in the channels. A distortion term due to the channel offsets in the TI-ADCs results as [5]

$$A(k) = \sum_{m=0}^{M-1} \left(\frac{1}{M} o_m \right) e^{-j2\pi \frac{km}{M}} \tag{2.12}$$

where o_m is the offset for path $m \in \{0, 1, ...M-1\}$. Here $o_m \sim N(0, \sigma_o)$ are identical and independently distributed random (i.i.d.) variables with Gaussian distribution and with zero mean. Thus, the distortion due to channel offsets is not signal dependent and appears at frequencies mf_s/M. From Parseval's relation we have the distortion power given by

$$P_d = E\left[\sum_{k=0}^{M-1} |A(k)|^2 \right] = E\left[\sum_{k=0}^{M-1} o_m^2 \right] = \sigma_o^2 \tag{2.13}$$

where $E()$ is the expectation function and σ_o^2 is the variance of the channel offsets. From this, we can estimate the offset-limited SNDR for the TI-ADC as

$$SNDR_o < 10 \cdot log\left(\frac{P_s}{P_d} \right) = 20 \cdot log\left(\frac{A_0}{\sigma_o \sqrt{2}} \right) \tag{2.14}$$

which implies that a large variance in channel offsets linearly degrades the resulting SNDR (in dB).

2.2.2 Gain Mismatch Errors

Assuming that there is only gain mismatch error in the channels of the TI-ADC and that the phase skew and the offsets are absent, we can write the distortion term resulting

from gain mismatch in TI-ADCs as [5]

$$A(k) = \sum_{m=0}^{M-1} \left(\frac{1}{M} a_m \right) e^{-j2\pi \frac{km}{M}} \tag{2.15}$$

where $a_m \sim N(a, \sigma_a)$ are i.i.d. random variables representing the gain of each channel. By definition, the channel gains are assumed to be normally distributed with mean a and variance σ_a. From Equation 2.11 we can observe that the distortion tones are located at the frequencies $f_{in} + k\frac{f_s}{M}$ and $f_s - (f_{in} + k\frac{f_s}{M})$, $k = 1, ..., M-1$. Thus, all the distortion tones are folded back into the Nyquist baseband from 0 to $f_s/2$. The signal amplitude is given by $A(0)$ while $A(m)$, $m = 1, .., M-1$ represent the amplitude of the distortion tones [5].

Now, we estimate the expected value of the total power of signal and distortion tones given as

$$\begin{aligned} P_{tot} &= \frac{1}{2} E\left[\sum_{k=0}^{M-1} |A(k)|^2 \right] = E\left[\frac{1}{2M} \sum_{m=0}^{M-1} |a(m)|^2 \right] \\ &= \frac{1}{2M} \sum_{m=0}^{M-1} E\left[a^2(m) \right] = \frac{E\left[a_0^2 \right]}{2} = \frac{\sigma_a^2 + a^2}{2} \end{aligned} \tag{2.16}$$

Similarly, the signal power is estimated as [5]

$$\begin{aligned} P_s &= \frac{E\left[A(0) \cdot A^*(0) \right]}{2} = \frac{1}{2M^2} \sum_{m=0}^{M-1} \sum_{n=0}^{M-1} E\left[a_m \cdot a_n \right] \\ &= \frac{1}{2M} E\left[a_m^2 \right] + \frac{1}{2M^2} \left(M^2 - M \right) \left(E\left[a_m \right] \right)^2 \\ &= \frac{1}{2M} \left(\sigma_a^2 + a^2 \right) + \frac{1}{2M^2} M \left(M - 1 \right) a^2 = \frac{1}{2M} \left(\sigma_a^2 + M \cdot a^2 \right) \end{aligned} \tag{2.17}$$

Since the distortion power P_d is equal to $P_{tot} - P_s$, we can estimate the SNDR as [5]

$$\begin{aligned} SNDR &= 10 \cdot log\left(\frac{P_s}{P_{tot}-P_s}\right) = 10 \cdot log\left(\frac{\frac{1}{2M}\left(\sigma_a^2 + M \cdot a^2\right)}{\frac{\sigma_a^2+a^2}{2} - \frac{1}{2M}\left(\sigma_a^2 + M \cdot a^2\right)}\right) \\ &= 10 \cdot log\left(\frac{\frac{1}{M}\left(\sigma_a^2 + M \cdot a^2\right)}{\left(1-\frac{1}{M}\right)\sigma_a^2}\right) \end{aligned} \tag{2.18}$$

Assuming that $\sigma_a \ll a$, we can approximate Equation 2.18 as [5]

$$SNDR \approx 20 \cdot log\left(\frac{a}{\sigma_a}\right) - 10 \cdot log\left(1 - \frac{1}{M}\right) \tag{2.19}$$

The second term in Equation 2.19 changes by a maximum of 3 dB (or 0.5 bit) as M ranges from 2 to ∞. Figure 2.4 plots the effective number of bits (ENOB) resulting from the time-interleaved sampling as a function of the gain mismatch error (σ_a), for time-interleaved sampling with $M = 2$, 4 and 8 channels and with the mean channel gain $a = 1$.

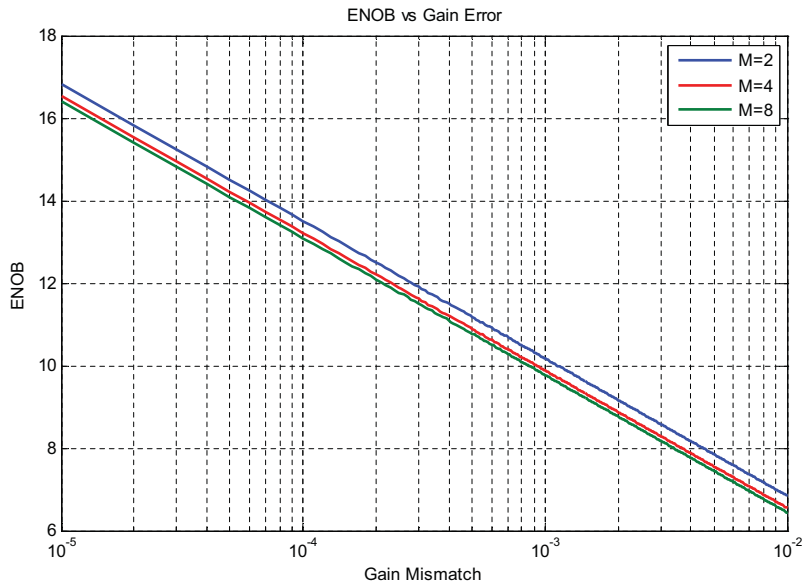

Figure 2.4: ENOB as a function of the standard deviation of the gain mismatch with M ADCs in parallel.

Here, we can observe that with a channel gain mismatch of 0.1%, which is the nominal capacitance ratio mismatch in a CMOS process, the TI-ADC is limited to 10 bits in resolution [5].

2.2.3 Phase Skew Errors

Now if we assume that only clock phase skew is present across the TI-ADC channel and the offset and gain errors are absent, we have the distortion term given by

$$A(k) = \sum_{m=0}^{M-1} \left(\frac{1}{M} e^{-j2\pi f_{in} r_m T} \right) e^{-j2\pi \frac{km}{M}} \tag{2.20}$$

Again, the distortion tones appear at the frequencies $f_{in} + k\frac{f_s}{M}$ and $f_s - (f_{in} + k\frac{f_s}{M})$, $k = 1, ..., M-1$, and fold back into the Nyquist baseband. Thus, the spectra of the noise introduced due to the phase skew is discrete as opposed to the continuous (white or with skirts) spectrum of the noise introduced due to the clock jitter. If the phase skew errors are assumed to be Gaussian i.i.d. random variables with zero mean and a variance σ^2_{skew}, the SNDR can be derived similarly to the gain mismatch analysis. Let's define the i.i.d. random variables $\alpha_m = r_m f_{in}/f_s$, $m = 0, 1, ..., M-1$ with a PDF (probability density function), $p(\alpha)$ and its characteristic function given by [16]

$$P(\omega) = E\left(e^{j\omega\alpha}\right) \tag{2.21}$$

Then, the signal power P_s is estimated as [16]

$$\begin{aligned} P_s &= E\left[A(0)\cdot A^*(0)\right] = \frac{1}{M^2}\sum_{m=0}^{M-1}\sum_{n=0}^{M-1} E\left[e^{-j2\pi(\alpha_m-\alpha_n)}\right] \\ &= \frac{1}{M}+\left(1-\frac{1}{M}\right)\left(|P(2\pi)|\right)^2 \\ &= |P(2\pi)|^2+\frac{1}{M}\left(1-|P(2\pi)|^2\right) \end{aligned} \tag{2.22}$$

and thus the SNDR is estimated is [16]

$$\begin{aligned} SNDR_{skew} &= 10\cdot log\left(\frac{E\left[A(0)\cdot A^*(0)\right]}{1-E\left[A(0)\cdot A^*(0)\right]}\right) \\ &= 10\cdot log\left(\frac{1+(M-1)\left|P(2\pi)\right|^2}{(M-1)\left(1-|P(2\pi)|^2\right)}\right) \end{aligned} \tag{2.23}$$

For a Gaussian distribution $\alpha_m \sim N(0,\sigma)$, substituting the $|P(2\pi)|$ by $e^{2^{\pi^2\sigma^2}}$ and then taking Taylor's series expansion of the log term around $\sigma = 0$ and retaining only the first term, we get the approximated SNDR as [16]

$$SNDR_{skew} = 20\cdot log\left(\frac{1}{2\pi\sigma}\right) - 10\cdot log\left(1-\frac{1}{M}\right) \tag{2.24}$$

Now we substitute $\sigma = f_{in}\sigma_{skew}$, to obtain the final SNDR relation

$$SNDR = 20\cdot log\left(\frac{1}{2\pi f_{in}\sigma_{skew}}\right) - 10\cdot log\left(1-\frac{1}{M}\right) \tag{2.25}$$

From Equation 2.25 we can see that the SNR drops 20 dB per decade with change in either the signal frequency f_{in} or the phase-skew standard deviation σ_{skew}. Thus the degradation in the SNDR is 0.5 bit for the complete range of M, while its greater than 3.3 bits per decade increase in f_{in} or σ_{skew}. Figure 2.5 plots the effective number of bits (ENOB) resulting from the time-interleaved sampling as a function of the phase skew

(σ_{skew}), for input signal frequencies of 10 MHz, 100 MHz and 1 GHz. Here, for each of the plots the equivalent clock rate (f_s) of the TI-ADC is such that the Nyquist sampling criterion is satisfied, i.e. $f_s > 2f_{in}$, while each of the 8 channels operate at a clock rate of $f_s/8$. Assuming a nominal phase skew of 10 ps, we can not expect more than 10 bits of resolution with $f_{in} = 10$ MHz and a resolution of 7 bits at $f_{in} = 100$ MHz. Thus phase skew severely limits the effective resolution of a Nyquist-rate TI-ADC.

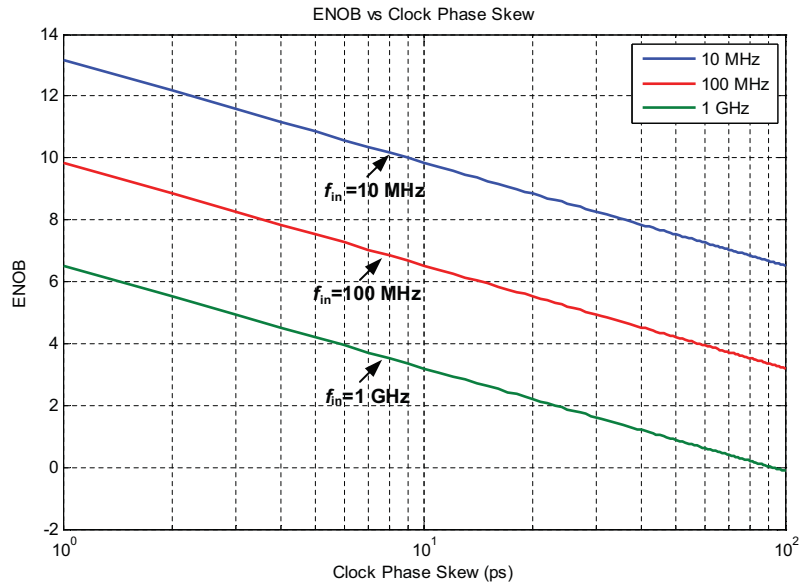

Figure 2.5: ENOB vs clock phase skew for an eight-channel time-interleaved ADC. Here, $f_s > 2f_{in}$, and the ENOB is independent of the sampling frequency.

2.2.4 Errors Due to Bandwidth Mismatch

A commonly ignored but rather important source of error in time-interleaved systems results due to mismatch in the bandwidth of the channels [18]. A typical example of a situation with bandwidth mismatch is of the time-interleaved track-and-hold (T/H) circuits. Each track-and-hold has a first-order response set by the switch on-resistance

(R_{sw}) and the hold capacitance (C_H). The $R_{sw}C_H$ time-constant sets the frequency response of the T/H and any mismatch in the $R_{sw}C_H$ product will cause bandwidth mismatch across the channels. The bandwidth mismatch causes AC gain and phase mismatch in the sampled signal in each of the channels. The phase mismatch introduced due to the bandwidth mismatch is a non-linear function of the input frequency. The reader is referred to [18] for analytical expressions derived for the SNDR due to the bandwidth mismatch in time-interleaved systems.

2.3 Oversampling in Time-Interleaved ADCs

Note that the distortion tones due to the path-mismatches in a TI-ADC appear at $f_{in} + k\frac{f_s}{M}$ and $f_s - (f_{in} + k\frac{f_s}{M})$, $k = 1, ..., M-1$, i.e. at a separation of f_s/M from the input frequency. Now if we have the situation where $f_{in} \leq \frac{f_s}{2M}$ implying an oversampling by M, we can avoid the appearance of these distortion tones in the signal band. However, in that case we lose the advantage of M-fold increase in conversion bandwidth obtained by employing time-interleaving although there is an increase in resolution by $0.5 \cdot \log_2(M)$ bits due to reduction in the quantization noise after filtering. Also, the oversampling ratio (OSR) can not be less than the number of paths M for a distortion free baseband i.e. $OSR \geq M$. The distortion tones can be filtered out by digital filters resulting in an $\frac{1}{2}log_2(OSR)$ bit increase in resolution. We will revisit the effects of channel mismatch errors in a time-interleaved delta-sigma ADC in Chapter 3, where the quantization noise folds back into the baseband due to the channel mismatch errors and thus degrading the SNDR [5].

2.4 Randomization and Calibration

The effects of channel mismatches can be reduced by employing randomization across the M parallel paths. By randomly selecting the channel to convert a given sample, the correlation between the input signal and the channel mismatch is reduced and the energy of the distortion tones is spread across the frequency band from 0 to f_s, and thus raising the noise floor [19]. A background calibration scheme can also be employed to improve the performance of time-interleaved Nyquist rate ADCs by mitigating offset and gain errors [20, 21]. However the distortion induced by phase skew is difficult to reduce by calibration as the calibration algorithms can not be run in background and require a rather complicated implementation [5].

2.5 Conclusion

In this chapter, the offset, gain-mismatch, phase-skew and bandwidth mismatch errors resulting from the time-interleaving of ADCs were discussed and their analytical results were presented. Amongst the errors introduced due to time-interleaving, the distortion due to clock phase-skew is the most detrimental to the resulting SNDR and can not be easily mitigated by calibration.

CHAPTER 3 WIDEBAND ANALOG-TO-DIGITAL CONVERTERS

This chapter discusses the issues involved with high-resolution and wideband data conversion using Nyquist rate ADCs in nano-CMOS technologies. Delta-sigma modulation based ADC architectures are gaining prominence due to their lower requirement on op-amp gain and component matching requirements although their conversion bandwidth is limited as they employ oversampling. A brief exposition on delta-sigma modulators is provided and later modulation based parallel delta-sigma modulators are discussed which can potentially lead to Nyquist-rate data conversion.

3.1 Digital Calibration of ADCs

For conversion speeds of up to 100 - 200 MHz with resolution greater than 10 bits, the pipelined ADC has been the preferred architecture for wideband wireless, instrumentation and data acquisition applications. In the nano-CMOS processes, the performance of the pipelined ADC is constrained by the capacitor mismatch, finite op-amp gain and op-amp nonlinearity. This results from the fact that it is becoming challenging to design op-amps exhibiting high gain and wide swing in nano-CMOS. The capacitor mismatch and finite op-amp gain in the pipelined stages (called a multiplying digital-to-analog converter or simply MDAC) introduce a residue gain error while the op-amp non-linearity results in a non-linear component in the input/output characteristic of the MDAC stage. Recently there has been an emphasis on employing digital calibration to

correct the gain errors and nonlinearity in the pipelined ADC stages. Here, we briefly discuss a representative calibration scheme presented in [1].

The example MDAC is shown in Figure 3.1 and its input/output relation is derived in [1] and is given by

$$\begin{aligned} V_{in} &= \frac{1}{2}(1+\varepsilon)V_{out} + f^{-1}(V_{out}) + \frac{1}{2}(1-\varepsilon)D_{out}V_{REF} \\ &= \frac{1}{2}(1+\varepsilon)V_{out} + \left(1+\frac{C_p}{2C}\right)f^{-1}(V_{out}) + \frac{1}{2}(1-\varepsilon)D_{out}V_{REF} \end{aligned} \tag{3.1}$$

where ε is the mismatch in the capacitor ratio, $f(\cdot)$ represents the input/output characteristic of the op-amp in closed loop, V_{in} is the MDAC input voltage, D_{out} is the digital output of the sub-DAC, V_{out} is the residue of the stage, and V_{REF} is the reference used for comparison. Here, $C_1 = C(1+\varepsilon)$, $C_2 = C(1+\varepsilon)$ and C_p is the effect of the input capacitance of the op-amp. Using this model, the approximate input of the MDAC can be estimated by the third order polynomial given by [1]

$$V_{in,appx} = \alpha_1 V_{out} + \alpha_3 V_{out}^3 + \frac{1}{2}(1-\varepsilon)D_{out}V_{REF} \tag{3.2}$$

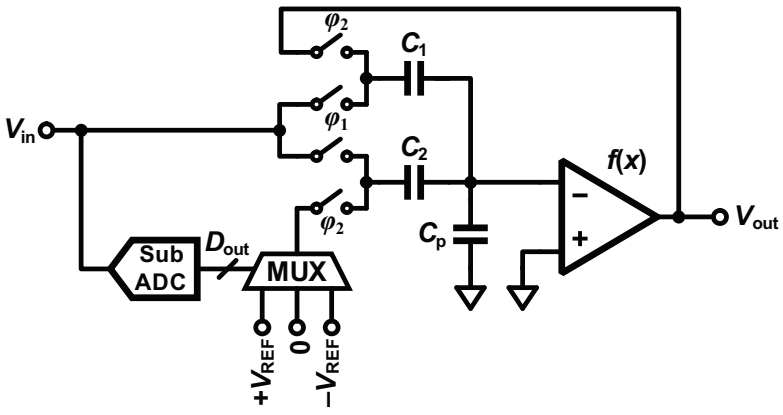

Figure 3.1: A 1.5-bit pipelined stage (MDAC) [1].

The digital calibration scheme employed in this 14-stage pipelined ADC is shown in Figure 3.2. The coefficients w_j's account for the capacitance mismatch for each of the MDAC stages. The digital calibration estimates the values for α_1, α_3, and w_j for each of the MDAC stages using a least mean square (LMS) adaptive algorithm. The calibration algorithm recursively starts by calibrating the last (and the least critical) stage. The calibrated stages together form an ideal back-end ADC and are used for calibrating the next stage in the sequence. The adaptive function $(\alpha_1 D_{BK} + \alpha_3 D_{BK}^3)$ estimates the approximate input voltage $V_{in,appx}$ for each of the stages and undoes the nonlinearity $g(x)$ introduced by the stage. For the LMS algorithm, a predefined digital training input set called D_{cal} is employed. A reference DAC is used for generating the analog input v_{in} from D_{cal} vectors. The sum of all the adaptive function outputs and the weighted MDAC outputs is called D_{tot}. The difference $D_{cal} - D_{tot}$ acts as the error term for the LMS engine, and its mean squared value is minimized for the pipelined ADC in a recursive manner. For further details on the calibration algorithm the reader is referred to [6]. Other recent examples of digital calibration of pipelined ADCs are available in [7, 22].

It is evident from the example of a pipelined ADC calibration scheme that the complexity of the system is increased by the need to accurately calibrate each of the MDAC stages. In order to realize such calibration schemes, precise back-end ADC and DACs are required for the digital correction of individual pipelined stages. It can be seen in this example that any error in the back-end ADC stages will cascade across the calibration of the subsequent stages. Thus, the convergence and resulting accuracy of such

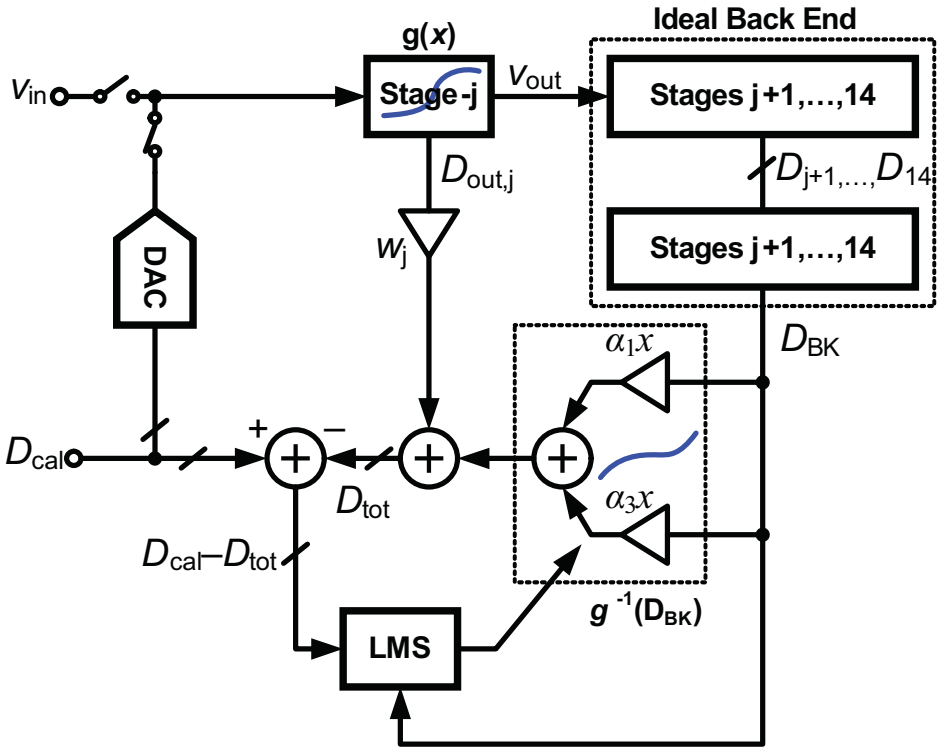

Figure 3.2: Diagram showing the concept of digital calibration of a pipelined ADC in [1].

schemes is an important concern. Furthermore, besides developing proven digital calibration schemes for pipelined ADCs with good convergence, it is imperative to explore wideband ADC architectures which are inherently tolerant to device mismatches and lower op-amp gain with the continued scaling of CMOS technology.

3.2 Delta-Sigma Modulation

Oversampling or delta-sigma ADCs trade sampling frequency with the signal bandwidth to achieve much higher signal-to-noise ratio (SNR) [13, 23]. Figure 3.3 illustrates the motivation behind the delta-sigma modulation (DSM). Here, a low-resolution ADC and DAC (1-bit quantizer in this case) are employed in a feedback loop along with a

loop-filter, $H(z)$. The modulator employs oversampling, i.e. the sampling frequency is a generally a large multiple of the input signal bandwidth, defined as the oversampling ratio (OSR).

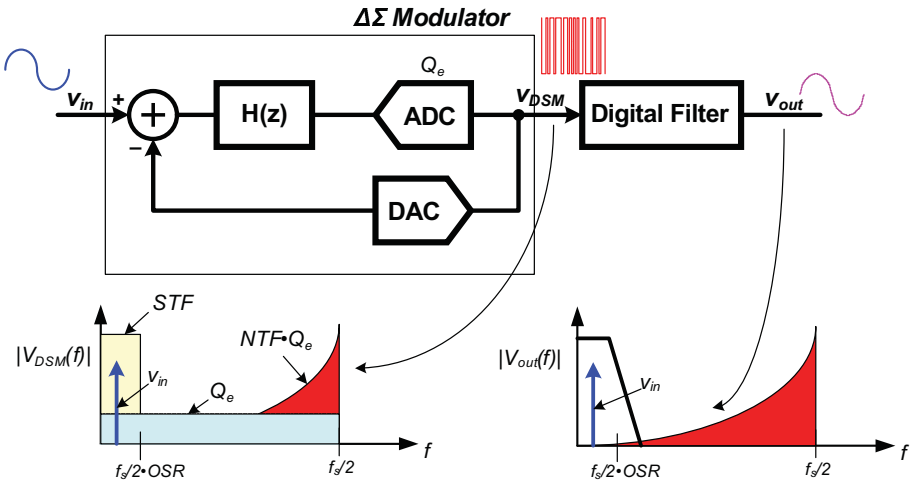

Figure 3.3: Block diagram of an ADC employing Delta Sigma Modulation.

The DSM loop shapes the quantization noise, $Q_e(z)$, and moves it to a higher frequency away from the baseband signal bandwidth. The noise-shaping occurs due to the differentiation of the quantization noise in the feedback loop, which in the frequency domain leads to high-pass filtering. The noise-shaping results in lower quantization noise in the signal bandwidth and the modulated noise can be filtered out digitally leading to a much higher signal to quantization noise ratio (SQNR). Thus, much of the analog signal processing is transferred to the digital domain. This is favorable in nano-CMOS as with scaling the digital circuitry is cheap, consumes lower power and is generally automatically synthesized [13]. Next, the first- and second-order switched-capacitor delta-sigma modulators are briefly discussed to provide a background for the first- and second-order KD1S modulators.

3.2.1 First-order Delta-Sigma Modulator

Figure 3.4 shows the block diagram of a discrete-time first-order delta-sigma modulator (DSM). The DSM consists of a difference (Delta) block, a delaying discrete time integrator (Sigma) and a quantizer modeled by the linear additive quantization noise term $Q_e(z)$.

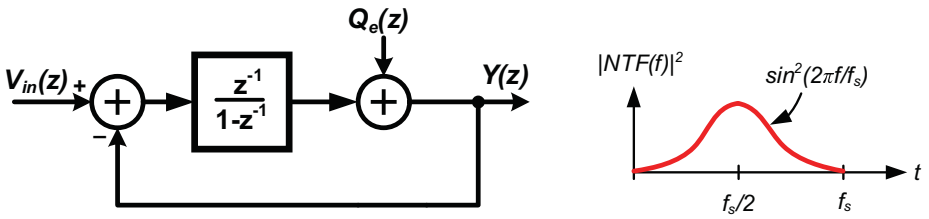

Figure 3.4: Block diagram and noise transfer function of a first-order delta-sigma modulator.

Figure 3.5 shows the switched-capacitor implementation of a first-order DSM. The integrator is implemented using an op-amp and the single-bit quantizer is implemented with a clocked comparator. The integrator and the comparator are clocked on the opposite phases ϕ_1 and ϕ_2 respectively and each of them settle within $T_s/2\,(=1/2f_s)$ time interval, where f_s is the sampling clock rate. In this DSM (see Figure 3.5), the output of the integrator is picked up by the comparator at phase ϕ_1 and quantized in half clock cycle. This quantized digital output is subtracted from the input signal (sampled-and-held at phase ϕ_1) and passed onto the integrating op-amp. The integrator integrates this feedback error $(v_{in}[n]-y_0[n])$ during phase ϕ_2, and the output of the integrator is updated before the next clock phase ϕ_1 and this noise-shaping cycle repeats itself.

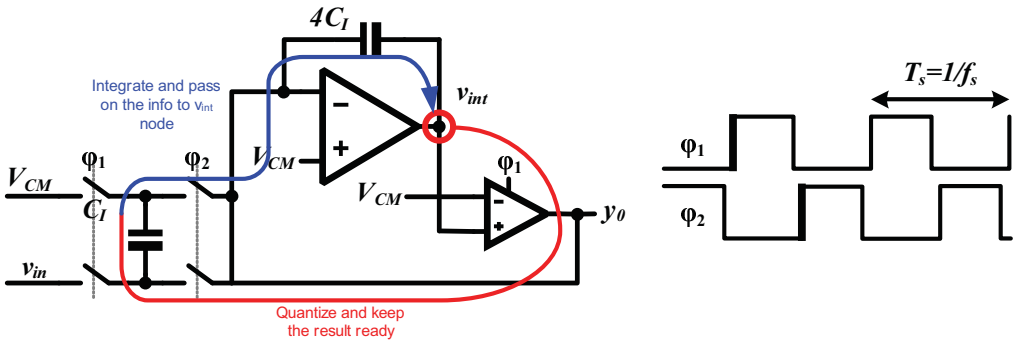

Figure 3.5: A first-order discrete-time delta-sigma modulator.

The relation between the input and output of the first-order DSM is given as

$$Y(z) = z^{-1}V_{in}(z) + (1 - z^{-1})Q_e(z) \tag{3.3}$$

The signal transfer function ($STF(z)$) is equal to z^{-1}, which is just a unit delay. The noise transfer function ($NTF(z)$) is equal to $(1 - z^{-1})$ which implies first-order differentiation of the quantization noise. The NTF can be expressed in frequency domain as

$$NTF(f) = 2 \cdot sin\left(\frac{\pi f}{f_s}\right) \tag{3.4}$$

Thus, effectively the quantization noise is differentiated and pushed out of the input signal band. After digital filtering using an ideal lowpass filter, the resulting SNR can be specified as a function of the oversampling ratio by the expression [13]

$$SNR = 6.02N + 1.76 - 5.17 + 30 \cdot log_{10}(OSR) \tag{3.5}$$

This increase in SNR leads to the effective bit resolution given by

$$N_{eff} = N - 0.566 + 1.5 \cdot log_2(OSR) \tag{3.6}$$

where N is the resolution of the quantizer. This can be interpreted as an increase in 1.5 bits per doubling in *OSR*. For example, by employing a single bit quantizer and an *OSR* of 64, 10-bits of resolution can be obtained with a first-order DSM.

The delta-sigma feedback loops are insensitive to device mismatch and nonlinearity in the forward path due to the high loop gain at the lower frequencies. The op-amp DC gain can be as low as the modest value of *OSR* and its unity gain frequency (f_{un}) can be comparable to the sampling frequency (i.e. $3f_s$ for 99.9% settling). This leads to high *SNR* at very high sampling frequencies and in presence of large device mismatches. Here, the feedback DAC realized by the single-bit quantizer output is inherently linear.

3.2.2 Second-Order Delta-Sigma Modulator

The noise-shaping concept of the first-order DSM can be extended to higher-orders by incorporating higher-order loop filters. Figure 3.6 shows the block diagram of a discrete-time second-order DSM. The relation between the input and output of the second-order DSM is given by

$$Y(z) = z^{-2}V_{in}(z) + (1-z^{-1})^2 Q_e(z) \tag{3.7}$$

Here, the STF is equal to z^{-2} and the NTF is equal to $(1–z^{-1})^2$ which implies double differentiation of the quantization noise. After the digital filtering using an ideal low-pass filter, the resulting *SNR* is given as the function of the oversampling ratio by the expression [13]

$$SNR \approx 6.02N + 1.75 - 12.9 + 50 \cdot log_{10}(OSR) \tag{3.8}$$

This increase in SNR leads to the effective bit resolution given by

$$N_{eff} = N - 1.85 + 2.5 \cdot log_2(OSR) \tag{3.9}$$

Therefore, the second-order noise-shaping results in an increase in 2.5 bits per doubling in OSR. Moreover, by employing a single bit quantizer and an *OSR* of 64, 16 bits resolution can be obtained with a second-order DSM.

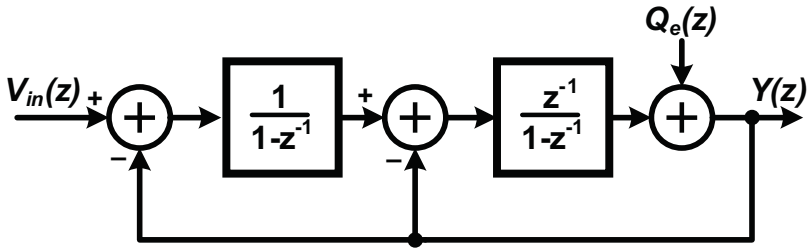

Figure 3.6: A discrete-time second-order DSM.

A switched-capacitor implementation of second-order DSM is shown in Figure 3.7. Here, the two integrators settle in opposite clock phases.

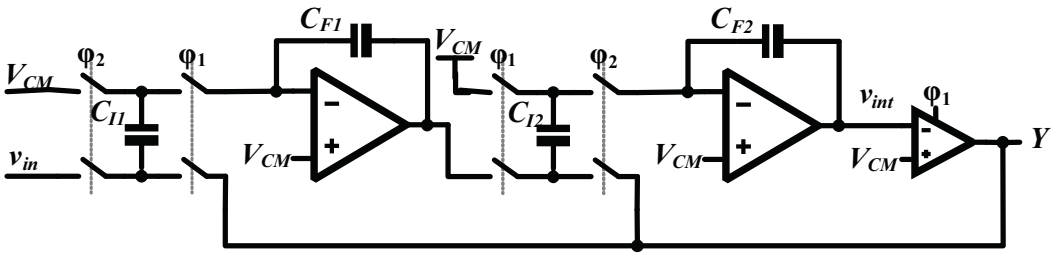

Figure 3.7: A switched-capacitor implementation of the second-order DSM.

Figure 3.8 compares the NTF of the first and second-order DSMs on a log-log plot. The second-order NTF has a slope of +40 dB/dec as compared to 20 dB/dec for the first-order DSM. As a consequence, the modulation noise is reduced in the signal band leading to higher SNR after digital filtering. The second-order noise-shaping concept

can be extended to even higher-orders ($M > 2$). An M^{th}-order noise-shaping loop results in an increase in a bit resolution of $(M + 0.5)$ per doubling in OSR. Even though higher-order noise-shaping is preferred for higher bit resolution, the stability of the modulator becomes conditional with higher out-of-band (OBG) gain in the NTF. An empirical rule of thumb called the Lee's rule [24] suggests an upper bound of 1.5 on OBG for stable higher-order DSMs [23].

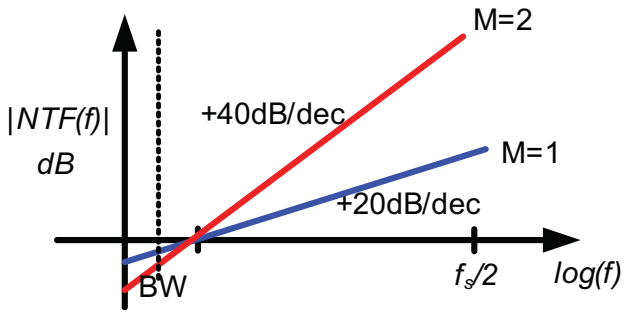

Figure 3.8: Comparison of the NTFs of first and second-order DSMs.

Recently there has been a spate of reporting of delta-sigma ADCs, both discrete-time and continuous-time, with increasing signal bandwidth and resolution. Continuous-time DSMs with low oversampling ratios (OSR) have been preferred for wideband data conversion (e.g. 20 MHz bandwidth at 420 MHz sampling rate) due to lower bandwidth requirements on the op-amps and inherent anti-aliasing [11]. Thus use of delta-sigma modulation (DSM) is favorable for data-conversion as the feedback desensitizes the

device mismatch in nano-CMOS processes. Also, with DSM, the complexity is transferred from the analog domain to the digital, which is favorable in nano-CMOS processes [13, 23, 25]. However, due to oversampling the delta-sigma ADCs are narrowband and the signal bandwidth is limited to

$$BW \leq \frac{f_s}{2 \cdot OSR} \tag{3.10}$$

It is obvious that the conventional delta-sigma ADCs can not achieve Nyquist-rate sampling as desired for wideband digitization. The following section considers this problem and proposes new wideband DSM architectures.

3.3 Prior and Current Art in Wideband Delta-Sigma Modulators

Several approaches have been proposed in the literature to increase the conversion bandwidth of the delta-sigma ADCs. The dominant wideband topologies are discussed in this section along with their limitations.

3.3.1 Double-Sampling DSM

Double-sampling is a straightforward technique to double the effective sampling rate of the delta-sigma modulator without increasing the clock frequency [26, 27, 28, 29, 30]. In the conventional switched-capacitor delta-sigma modulators seen in Figures 3.5 and 3.7, the input is sampled during the phase ϕ_1 and then the comparator quantizes the integrator's output (quantization phase) while during the phase ϕ_2 integration is carried out (integrating phase). Thus the integrator operates only during half the clock period

($T_s/2$ duration) and is idle during the other half. Double-sampling is employed to double the effective clock-rate of the modulator by making the integrator operate during both the clock phases. As shown in Figure 3.9, the input is sampled at both the clock phases, and the feedback signal is transferred to the integrator on the rising as well as the falling edge of the clock.

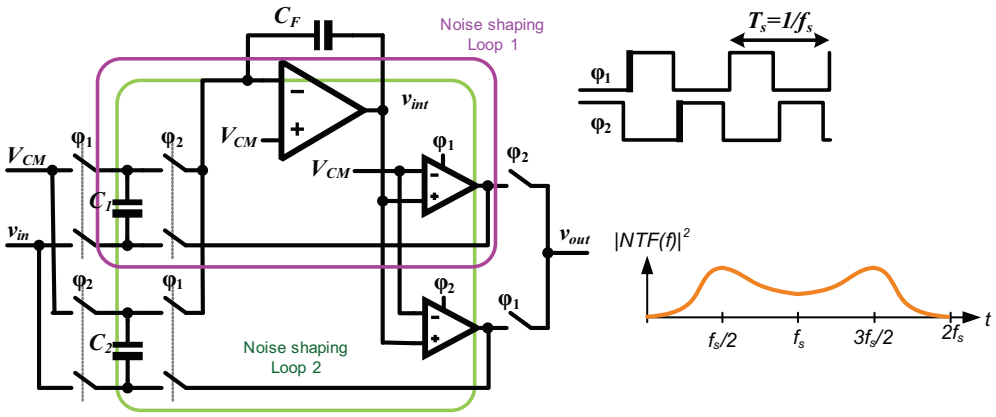

Figure 3.9: A first-order delta-sigma modulator employing double-sampling.

Two comparators are employed on both the clock phases resulting in an effective clock-rate of $2f_s$. However, since the signal for each of the paths is fed back after a loop-delay equal to T_s, double-sampling leads to two bulges centered at $f_s/2$ and $3f_s/2$ in the NTF response with a dip at $f_s/2$. The resulting spectrum for a double-sampling first-order DSM, simulated in Spectre is shown in Figure 3.10. Here, the modulator is clocked with a clock frequency of $f_s = 100$ MHz, a comparator delay T_c equal to $5\,ns$, the op-amp's unity-gain frequency, $f_{un} = 3 \cdot f_s = 300\,MHz$ and an oversampling ratio of $OSR = 16$. Note that in this case the comparator in the first path is clocked with the phase ϕ_1, allowing the integrator half-clock period ($T_s/2$) to settle. Since the loop delay for each path is equal to T_s, the peak in the NTF occurs at a multiple of $\frac{1}{2T_s} = \frac{f_s}{2}$,

as observed in the Figure 3.10.The resulting *SNDR* is equal to 33 dB or 5.20 bits in resolution.

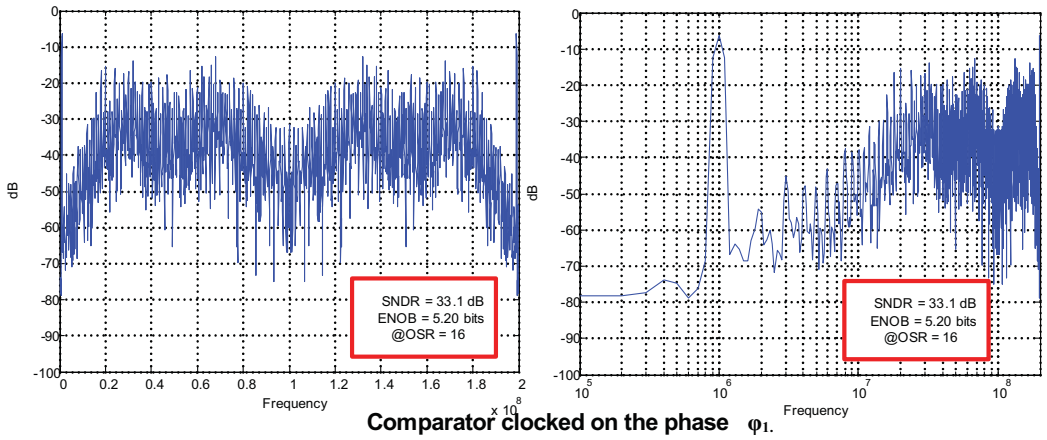

Figure 3.10: Spectrum (linear and log frequency) for a double-sampling first-order DSM with $f_s = 100$ MHz, $T_c = 5$ ns, op-amp $f_{un} = 3f_s = 300$ MHz,$OSR = 16$, and $BW = 6.25$ MHz.

Noise Folding in Double-Sampling DSM

A disadvantage of double-sampling is that it is sensitive to mismatch between the two signal paths, which causes quantization noise to fold from the frequencies close to the Nyquist frequency into the signal band and thus increases the noise floor. This increases the in-band noise (IBN) which in turn limits the achievable SNDR from the modulator [26].

A path mismatch arises from the fact that the two input sampling capacitors, C_1 and C_2 in Figure 3.9 are not perfectly matched when these capacitors are fabricated on a chip. Typically in a modern CMOS process, the standard deviation of the capacitor mismatch (σ_{cm}) ranges from 0.1% to 0.3% [31]. Then the path mismatch induced due

to the variation in the capacitors is given by [26]

$$\delta = \frac{C_1 - C_2}{C_1 + C_2} \tag{3.11}$$

Because of this path mismatch, the input to the sampling integrator in the modulator undergoes amplitude modulation (AM) with a frequency of $f_s/2$. Furthermore, due to the amplitude modulation, the shaped quantization noise at the frequency $f_s/2$ is frequency translated to the baseband, and this effect is called the *noise folding*. The analysis of noise folding is presented as follows. Consider the equivalent block diagram for a double-sampling modulator's front-end as shown in Figure 3.11 [26].

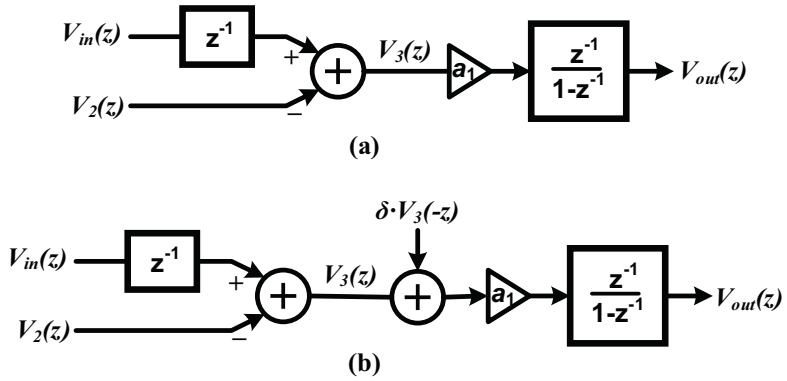

Figure 3.11: Signal flow diagram for a double-sampled DSM. (a) case without the path mismatch, and (b) with the folded noise due to the path mismatch.

Now, let's define the average value of the sampling capacitors as $C_0 = (C_1 + C_2)/2$. The mismatch ratio is given by the Equation 3.11. Then the output of the discrete-time delaying integrator is given by the relation [26]

$$v_{out}[n] = v_{out}[n-1] + \frac{C_0}{C_F}\left(1 + (-1)^n \delta\right)\left(v_{in}[n-1] - v_2[n]\right) \tag{3.12}$$

where the $(-1)^n$ term appears from the fact that the input sampling capacitors ($C_0(1+\delta)$ and $C_0(1-\delta)$) are used on the alternating clock phases. Here, $v_2[n]$ is the signal fed back to the modulator and subtracted from the input. Equation 3.12 can be re-written as [26]

$$v_{out}[n] = v_{out}[n-1] + \frac{C_0}{C_F}\left(v_{in}[n-1] - v_2[n] + v_{eq}[n]\right) \tag{3.13}$$

where the equivalent noise (v_{eq}) added due to the amplitude modulation is given by

$$v_{eq}[n] = (-1)^n \delta \cdot (v_{in}[n-1] - v_2[n]) = (-1)^n \delta \cdot v_3[n] \tag{3.14}$$

Here, $v_3[n] = v_{in}[n-1] - v_2[n]$ is the equivalent signal at the input of the integrator as seen in Figure 3.11). Taking the $z-$transform of $v_3[n]$, we get

$$V_3(z) = z^{-1}V_1(z) - V_2(z) \tag{3.15}$$

The signal $V_3(z) \approx z^{-1}NTF(z)Q_e(z)$ contains the shaped quantization noise fed back to the input of the modulator. Now, realizing the fact that the amplitude modulation of v_3 by $(-1)^n$ in Equation 3.14 is equivalent to modulation by the signal

$$(-1)^n = cos(n\pi) = cos(2\pi f/f_s)|_{f=f_s/2} \tag{3.16}$$

which translates the noise peak at the frequency $f_s/2$ to the baseband leading to the modulation noise folding. Now observing the relation [26]

$$V_{eq}(z) = \delta \sum_{n=0}^{\infty}(-1)^n z^{-n} v_3[n] = \delta \sum_{n=0}^{\infty}(-z)^{-n} v_3[n] = \delta \cdot V_3(-z) \tag{3.17}$$

the AM by $f_s/2$ is equivalent to a $z-$domain substitution $z \rightarrow z^{-1}$. Thus in Figure 3.11 (b), the folded noise $\delta \cdot V_3(-z)$ has been shown to be added at the input of the integrator.

This raises the in-band noise floor by an amount depending upon the capacitor mismatch coefficient δ and limits the effective resolution (ENOB) achievable by the modulator. The equation governing the noise-shaping behavior of the DSM with noise folding is now given as [26]

$$\begin{aligned} Y(z) &= STF(z)V_{in}(z) + NTF(z)Q_e(z) + STF(z)V_{eq}(z) \\ &\approx STF(z)V_{in}(z) + NTF(z)Q_e(z) + \delta \cdot z^{-1}NTF(-z)Q_e(-z) \end{aligned} \tag{3.18}$$

Figure 3.12 illustrates the noise-folding effect in a double-sampling modulator. Due to the significant reduction in SNDR as a result of quantization noise folding into the baseband, the simple double-sampling structure seen in Figure 3.9 is avoided [32]. The effects of noise folding are mitigated by employing bilinear integrator topologies with fully-floating capacitors and fully-differential operation as discussed in [26, 29, 30].

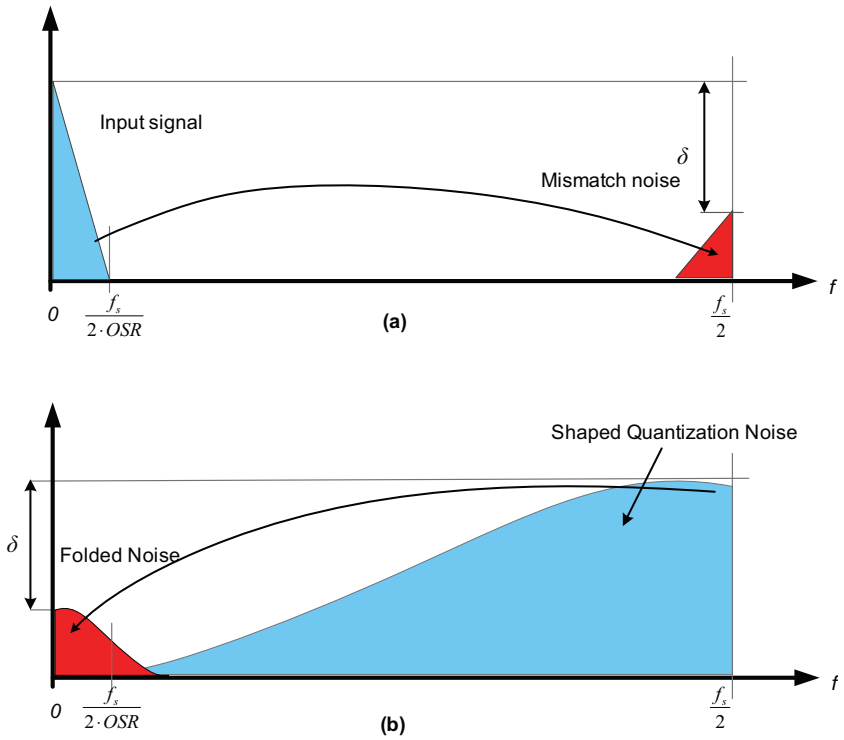

Figure 3.12: Noise folding effect due to the path-gain mismatch in a double-sampling DSM. (a) Gain mismatch effect on the input path, (b) Gain mismatch effect on the feedback path where the quantization noise is folded back into the signal band.

3.3.2 Time-Interleaving of Delta-Sigma Modulators

The time-interleaving concept used for the Nyquist-rate ADCs can be extended to the delta-sigma modulators as shown in Figure 3.13. A straightforward time-interleaving of the delta-sigma modulators only achieves a 0.5 bit of gain in resolution (3 dB *SNR*) per doubling in the number of paths. Also, interleaving of K_{path} delta-sigma modulator does not produce true-noise-shaping in frequency where the quantization noise is moved all the way up to the frequency $K_{path}f_s/2$. Instead we observe noise-shaped ripples in the

noise transfer function (NTF) of such a modulator with peaks at odd multiples of $f_s/2$ (see Figure 3.14) [13].

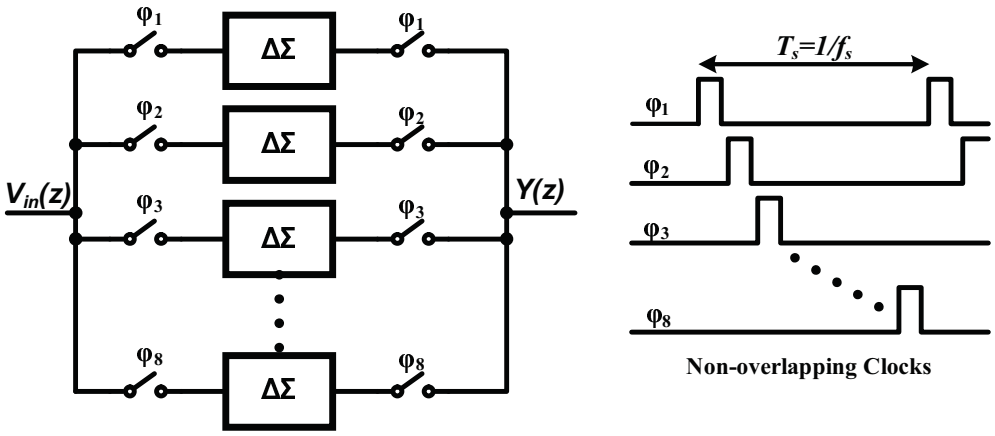

Figure 3.13: A time-interleaved delta-sigma modulator array.

The ripples in the time-interleaved DSM arise due to the fact that the feedback signal in the delta-sigma loop arrives back to the input only after a delay of $T_s(=1/f_s)$. For a parallel DSM, the K-paths are mutually exclusive and typically require K_{path} different set of integrators and comparators which results in much higher power consumption and layout area. Also, the time-interleaved DSM is plagued by the channel mismatch and phase skew errors discussed earlier in Chapter 2.

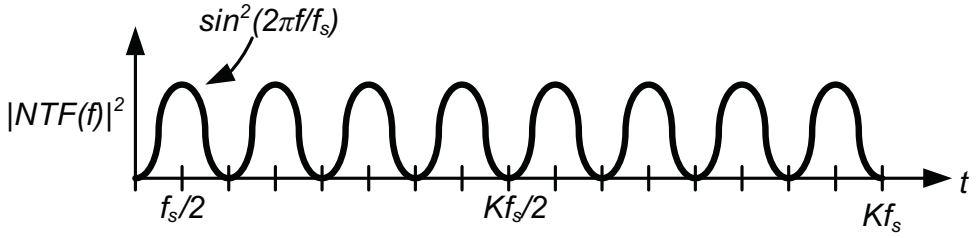

Figure 3.14: Noise-shaping for a K-path interleaved delta-sigma modulator.

In order to achieve true noise-shaping with interleaving of delta-sigma modulators, the loop delay of the modulator must be equal to T_s/K_{path}. Thus the delta-sigma modulators do not time-interleave like their Nyquist rate counterparts.

3.3.3 Parallel Delta-Sigma Modulators

In the last section we observed that the most simplistic time-interleaving of multiple delta-sigma modulators results in only 0.5 bit increase in resolution when the same bandwidth is considered as the single DSM. An alternative architecture called modulation based parallel architecture which can achieve Nyquist-rate conversion [8, 33, 34, 35]. The block diagram of the modulation-based parallel DSM is shown in Figure 3.15.

In this architecture, M- DSMs are connected in parallel and the input is modulated by the vector sequence $\mathbf{u}[n] = \mathbf{u}_{r,\langle n \rangle_M}$ and is applied to the modulator array. The modulated signals are then filtered by the digital filter with an impulse response given by $h[n]$ and the filter outputs are demodulated by the sequence $\mathbf{u}^*[n] = \mathbf{u}^*{}_{\langle n \rangle_M}$. Here, r denotes the row in the modulator array and $\langle n \rangle_M$ denotes the sequence in time generated by the modulo operation with a base M. The terms in the sequence $\mathbf{u}[n] = \mathbf{u}_{r,<n>_M}$ are the elements of a unitary matrix $U \in \mathbb{C}^{\mathbb{M}\times\mathbb{M}}$ (i.e. $U^*U = UU^* = I_M$) . The summation of the individual filter outputs forms the output $y[n]$ of the overall parallel DSM [8].

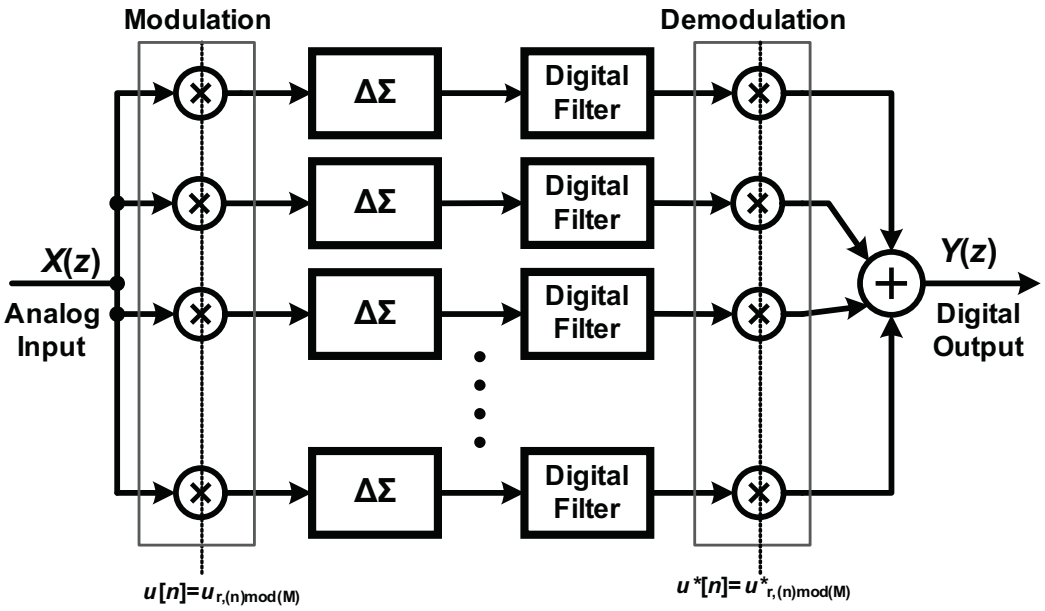

Figure 3.15: A generalized block diagram of the parallel delta-sigma ADC employing modulation.

Let the digital filter with impulse response $h[n]$ be a real FIR (finite impulse response) filter of length $(2L+1)$ and have a delay d. Then, the output of the ADC is given by [8, 34]

$$\begin{aligned} y[n] &= \sum_{r=0}^{M-1} \sum_{k=-L}^{L} h[k] \cdot x[n-k] \mathbf{u}_{r,\langle n-k \rangle_M} \cdot \mathbf{u}^*{}_{\langle n+d-k \rangle_M, r} \\ &= \sum_{k=-L}^{L} h[k] \cdot x[n-k] \cdot \sum_{r=0}^{M-1} \mathbf{u}_{r,\langle n-k \rangle_M} \cdot \mathbf{u}^*{}_{\langle n+d-k \rangle_M, r} \end{aligned} \tag{3.19}$$

Since the sequence $u_{i,j}$ are the elements of a unitary matrix, the summation $\sum_{r=0}^{M-1} \mathbf{u}_{r,\langle n-k \rangle_M} \cdot \mathbf{u}^*{}_{\langle n+d-k \rangle_M, r} = C_M(k)$ is a comb sequence. This results in the output of the ADC being given by

$$y[n] = \sum_{k=-L}^{L} h[k] \cdot x[n-k] \cdot C_M(k) \tag{3.20}$$

Now, for the parallel ADC to be Nyquist-rate ADC, we should be able to segregate the individual channel outputs without any interference between the M channels in the parallel ADC. This leads to the restriction on the digital filter that $h[n] = 1$ for $n = 0$ and that $h[n] = 0$ for $\langle n \rangle_M = 0$. Three parallel ADC architectures are available in literature based on three type of unitary matrices: the identity matrix, the DFT matrix and the Hadamard matrix. Here, we describe the Hadamard modulation based parallel ADC. The Hadamard matrix $H_M \in \mathbb{R}^{\mathbb{M}\times\mathbb{M}}$ is generated by using the recursion

$$H_{n+1} = \frac{1}{\sqrt{2}} \begin{bmatrix} H_n & H_n \\ H_n & -H_n \end{bmatrix} \tag{3.21}$$

where the seed 2×2 Hadamard matrix is defined as

$$H_2 = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \tag{3.22}$$

The advantage of using Hadamard matrix for modulation is that its coefficients are made up of $+1$ and -1, which can easily be implemented in switched-capacitors by selectively passing or switching the fully-differential signals based upon the modulation sequence. From the filter description, the resulting quantization noise power is estimated as [8, 34]

$$\begin{aligned} e_Q^2 &= \left(\frac{1}{M} \sum_{i=0}^{M-1} \sum_{j=0}^{M-1} \left| u_{i,j} \right|^2 \right) \frac{\Delta^2}{12} \frac{1}{2\pi} \int_{-\pi}^{\pi} \left| NTF(e^{j\omega}) H(e^{j\omega}) \right| d\omega \qquad (3.23) \\ &\simeq \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)} \frac{1}{M^{2L}} \end{aligned}$$

which implies that for every doubling in the number of channels (M) the ADC resolution increases by L bits, where L is the order of the modulator. The limitations of the modulation based parallel delta-sigma ADC include :

1. Large area and power requirements as M identical slower delta-sigma modulators are employed.

2. The requirements on the digital filters $h[n]$ are stringent, resulting in a large layout area and significant power consumption.

3. Gain and phase mismatch across the parallel channels introduces errors causing a reduction in the SNDR. Randomization and digital calibration is generally employed to reduce the distortion.

A parallel ADC architecture based upon the concept of filter banks, called frequency band decomposition (FBD) ADC, is shown in Figure 3.16 [8]. Here, each of the parallel channels converts a different band of frequency and thus covering the whole Nyquist spectrum. The signal path in each of the parallel channels is comprised of a band-pass delta-sigma modulator (low-pass modulator for the first channel and a high-pass modulator for the last channel) followed by a corresponding digital filter that filters out the shaped noise around the signal band of interest.

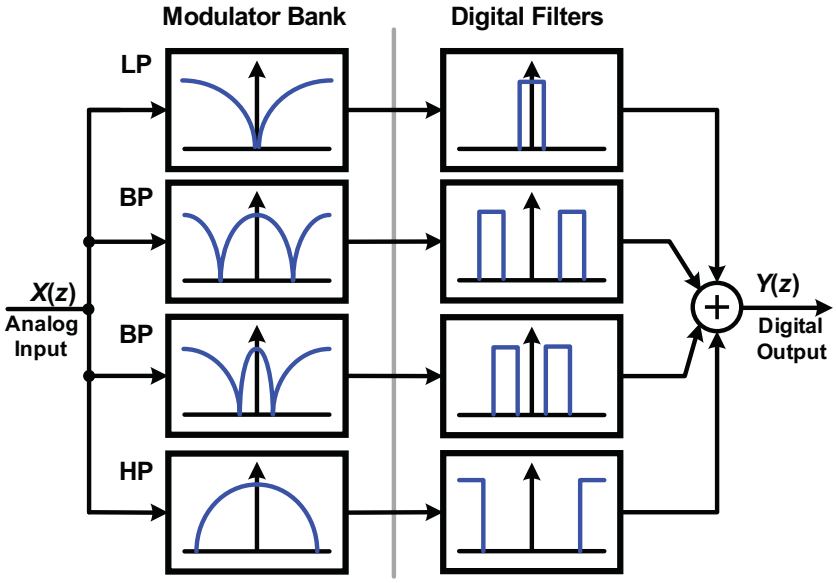

Figure 3.16: Block diagram of a four-channel parallel delta-sigma modulator employing frequency band decomposition.

For a FBD parallel ADC with M channels employing L^{th} order modulators resulting quantization noise power is given by

$$e_Q^2 \approx \frac{\Delta^2}{12}\frac{\pi^L}{(L+1)(M-1)}\frac{1}{2^{L+1}} \tag{3.24}$$

which implies that for every doubling in the number of channels (M) there is an increase of L bits in resolution. The FBD ADCs are relatively insensitive to channel mismatch. However, it is challenging to design the FBD ADC as each of the channel employs a completely different modulator and digital filter.

A few other parallel delta-sigma modulators employing polyphase filter decomposition were presented in [36, 37]. Again, these topologies suffer from the drawbacks of M-fold increase in layout area and power consumption. Also implementation of such

polyphase decomposition topologies beyond four channels becomes very complicated and cumbersome.

3.3.4 Wideband Continuous-Time Delta-Sigma Modulators

Continuous-time delta-sigma modulators (CT-DSMs) with low oversampling ratios (OSR) have recently become popular for implementing wideband, high-resolution, ADCs for wireless communications [9, 38, 39, 40]. In a CT-DSM, the loop filter is implemented using continuous-time circuitry (see Figure 3.17), which results in significantly lower power consumption when compared to its switched-capacitor counterpart. Moreover, since the sampling takes place at the quantizer instead of sampling at the front as in the case of the discrete-time DSM, the loop filter also doubles as an anti-aliasing filter (AAF). This inherent anti-aliasing feature is favorable in wireless applications where the integration of an additional AAF is avoided and the noise figure requirements in the RF signal chain are relaxed [41].

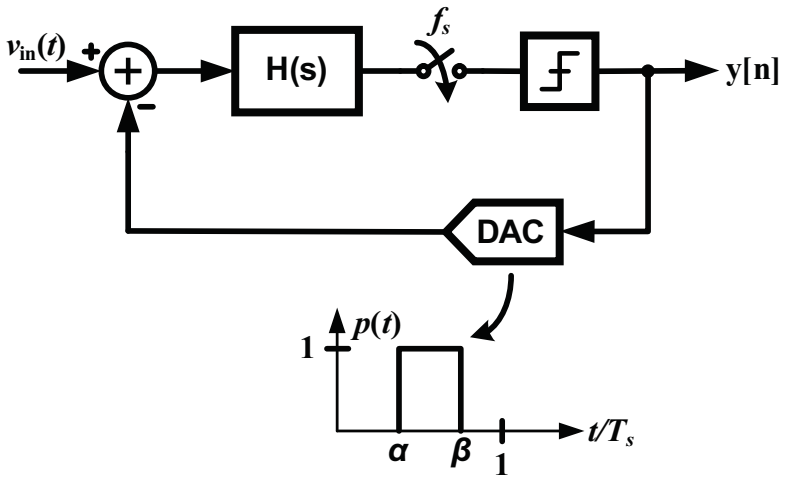

Figure 3.17: Block diagram of a continuous-time delta-sigma modulator. Here the feedback DAC pulse shape is shown as a generic rectangular pulse with excess loop delay (α), encountered in practical CT-DSM designs..

A recent example of a wideband CT-DSM architecture can be found in [9, 10] and illustrated in Figure 3.18. In this architecture, a single-loop modulator with fifth-order was chosen for aggressive noise-shaping with careful consideration for stability. A multi-bit quantizer with 11 levels was employed to optimize the out-of-band gain (OBG) of the NTF with respect to the power consumption and SQNR. A feed-forward type architecture was employed as the output swing of the feed-forward loop-filter is much smaller than the in the distributed feed-back architecture. This reduces the power consumption and enhanced the gain (and thus linearity) in the critical first stage integrator in the loop-filter. The disadvantage of the feed-forward type topology are that it requires a fast multi-input adder just before the quantizer which increases the forward path delay and consumes additional power. Another disadvantage of the feed-forward architecture is that it usually leads to an out-of-band peaking in the STF, which allows

blockers and reduces the dynamic range of the modulator in the wireless applications [10] .

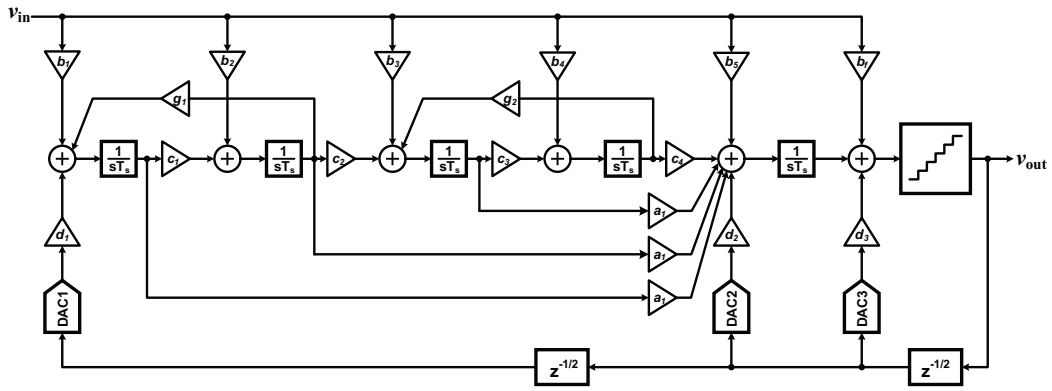

Figure 3.18: The architecture of a wideband continuous-time delta-sigma modulator for wideband data conversion.

A major consideration in the CT-DSM is the loop stability in the presence of excess loop delay due to the bandwidth limitations of the CT loop-filter. In [10], it was observed that the loop-stability is more sensitive to the first several samples of the loop's impulse response than the later ones. From this it can be concluded that the equivalent bandwidth of the low-order loops in the modulator, which contribute to the first few samples, is more critical than that of the higher-order loops. Thus an additional feedback DAC (i.e. DAC2) is employed to force the last integrator to form a first-order loop and alleviate the gain and bandwidth requirement on the first *critical* integrator. The feedback DAC, DAC3, is used for excess delay compensation by having a direct path from the quantizer output to the loop-filter's output. A multi-bit quantizer with NRZ pulse shaping is usually employed to minimize the jitter sensitivity of the modulator [42]. Also, the extra feed-in branches from the input eliminate the out-of-band STF peaking.

The DSM in [10] has reported a measured SNDR of 56 dB (or 9 bits in resolution) for 20 MHz conversion band with an OSR of 8. The power consumption of this modulator is 18 mW which results in a figure-of-merit (FoM) of 0.87 pJ/conversion [10] . Thus a careful and calibrated optimization on the various modulator parameters is employed to obtain wideband data conversion with low power consumption using continuous-time circuitry. Low OSR cascades (MASH) of CT-DSM are also being considered in the literature for achieving aggressive noise-shaping with lower order loops to alleviate the loop stability concerns [41, 43, 44]. Wideband low-power CT-DSM design and their computer-aided design (CAD) and simulation are promising topics for research.

3.4 Conclusion

Pipelined ADCs have traditionally been used for achieving a moderate resolution of 10-12 bits with up to 100-200 MHz conversion bandwidth. With continued scaling, the design of pipelined ADCs has become challenging due to the lower op-amp gain and nonlinearity. Digital calibration algorithms are being employed to mitigate the mismatch and non-linearity in the pipelined ADCs and thus leading to complicated system implementations. Delta-sigma modulation-based ADCs are the favorable architecture for data conversion in nano-CMOS but are limited to lower conversion bandwidths due to oversampling. Double-sampling is employed in discrete-time DSMs to double the effective sampling rate. However, the problem of noise folding in the double-sampling modulators must be mitigated by careful circuit design. Simple time-interleaving of DSMs does not lead to a useful increase in conversion bandwidth as the loop-delay is

not improved with interleaving. Modulation based parallel DSMs have been proposed for achieving Nyquist-rate data conversion, but such architectures suffer from channel mismatch errors and entail large power consumption due to component multiplication. On the other hand, continuous-time DSMs have made significant progress in achieving low-power wideband data conversion but are still short of the conversion bandwidths obtained by the pipelined ADCs.

CHAPTER 4 THE *K*-DELTA-1-SIGMA MODULATOR

A new topology called *K*-Delta-1-Sigma (KD1S) was disclosed in [12] to achieve wide-band noise-shaping using time-interleaved sampling and a shared integrator. This chapter investigates the performance of the first-order KD1S modulator and analyzes the effects of component idealities in a practical design. The analytical results developed in this chapter will be applied to the higher-order KD1S modulators developed in subsequent chapters.

4.1 Switched-Capacitor Integrator (SCI) Dynamics

In order to understand *K*-path switched-capacitor dynamics, it is instructive to revisit the transient dynamics of a conventional single-path switched-capacitor integrator. Figure 4.1 shows the schematic of a switched-capacitor integrator (SCI) along with the waveforms illustrating the circuit's transient dynamics.

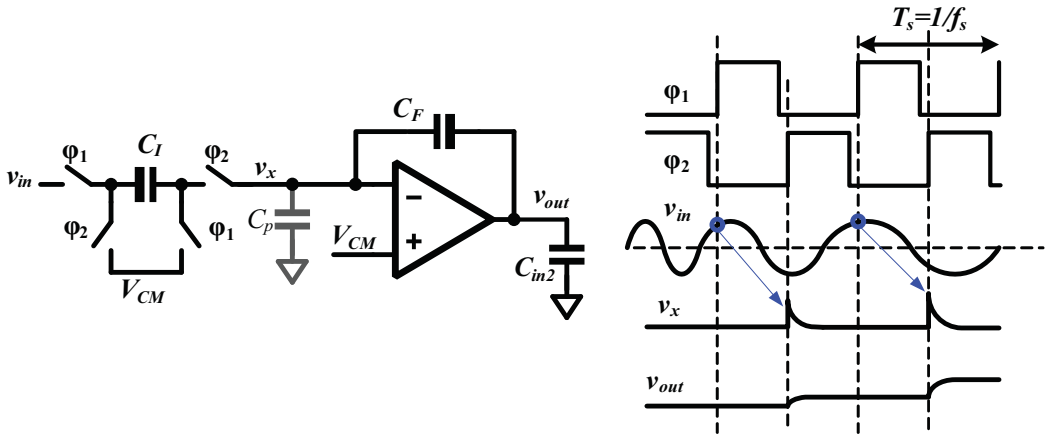

Figure 4.1: A switched-capacitor integrator and the waveforms showing its transient dynamics.

The speed and settling characteristics of the SCI are governed by the op-amp used in the integrator. Assuming a single-stage op-amp, the unity-gain frequency of the op-amp is given as [5]

$$f_{un} = \frac{g_m}{2\pi C_L} \tag{4.1}$$

where g_m is the transconductance of the input diff-pair of the op-amp and C_L is the total load capacitance loading the op-amp. For, a two-stage op-amp the load capacitance should be replaced by the compensation capacitance C_C [5] in Equation 4.1. The load capacitance for the op-amp in the SCI is given by

$$C_L = C_{in2} + \frac{(C_I + C_p)\,C_F}{C_I + C_F + C_p} \tag{4.2}$$

where C_{in2} is the input capacitance of the stage following the SCI and C_p is the net parasitic capacitance at the input of the op-amp in the SCI. The 3-dB frequency of the

SCI is estimated as

$$f_{3dB} = \beta f_{un} \tag{4.3}$$

where the feedback factor β is given by

$$\beta = \frac{C_F}{C_I + C_F + C_p} \tag{4.4}$$

Thus the 3-dB bandwidth of the SCI can be expressed as [5]

$$f_{3dB} = \frac{1}{2\pi} \frac{g_m}{C_{in2} + \frac{(C_I + C_p)C_F}{C_I + C_F + C_p}} \frac{C_F}{C_I + C_F + C_p} \tag{4.5}$$

Since the settling time of the SCI depends upon how fast the op-amp current charges the load capacitances, the time constant (τ) for the first-order settling of the integrator (assuming that there is no slewing) is given as

$$\tau = \frac{1}{2\pi\beta f_{un}} \tag{4.6}$$

The input v_{in} is sampled on to the capacitor C_I during the sampling phase (ϕ_1 is high). During the integration-phase (ϕ_2 is high), a fraction of the sampled input $v_{in}[(n-\frac{1}{2})T_s]$ is transferred to the node v_x due to charge-sharing. Next, the op-amp acts to settle the node v_x back to V_{CM} by transferring charge to the integrating capacitor C_F. During the transient settling, a displacement current flows in the capacitors which is given by

$$i_d(t) = (C_I + C_p) \frac{d(-v_x(t))}{dt} = C_F \frac{d(v_x(t) - \triangle v_{out}(t))}{dt} \tag{4.7}$$

Also we have, $v_x[nT_s] = v_{in}[(n-\frac{1}{2})T_s] = V_0$ (say), which is sampled on the input capacitor (C_I) during the clock phase ϕ_1, and transferred to node v_x on the rising edge of phase ϕ_2. This charge transfer leads to a sudden jump (or fall) in the node v_x by the amount V_0,

which gradually decays with the time-constant τ. During this time, when the spike on v_x decays, the charge is transferred to the output with the same time-constant and eventually the output of the integrator moves by the amount $\triangle v_{out} = \frac{C_I}{C_F} V_0$. These transient voltages, for $nT_s < t < (n+\frac{1}{2})T_s$, are given by

$$\begin{aligned} \triangle v_{out}(t) &= \frac{C_I}{C_F} V_0 \left(1 - e^{-\frac{t}{\tau}}\right) \\ v_x(t) &= V_0 e^{-\frac{t}{\tau}} \end{aligned} \tag{4.8}$$

If the clock rate is f_s then at the end of the half clock phase, the values of v_{out} and v_x are given as

$$\begin{aligned} \triangle v_{out}[(n+1/2)T_s] &= \frac{C_I}{C_F} V_0 \left(1 - e^{-\frac{T_s}{2\tau}}\right) = G_I V_0 (1 - \alpha_0) \\ v_x[(n+1/2)T_s] &= V_0 e^{-\frac{T_s}{2\tau}} = V_0 \alpha_0 \end{aligned} \tag{4.9}$$

where the settling factor α_0 is given as

$$\alpha_0 = e^{-2\pi\beta f_{un} T_s/2} = e^{-\pi\beta f_{un}/f_s} \tag{4.10}$$

and the integrator gain is defined as $G_I = C_I/C_F$.

We can observe that for the op-amp unity-gain frequenct $f_{un} = \infty$ and the DC gain $A_{OL} = \infty$, we have $\alpha_0 = 0$, which implies that the integrator settles instantaneously and 100% of the input charge is transferred to the output. As f_{un} becomes comparable to f_s, the amount of settling decreases. For $\beta = 0.5$ and 90% transient settling

$$f_{un} = -\frac{ln(\alpha_0)}{\pi\beta} f_s = 1.5 f_s \tag{4.11}$$

Similarly for 99% settling we require $f_{un} = 3f_s$. In general, for N-bits resolution, the bandwidth requirement for the sampling integrator is given by [23]

$$\frac{f_{3dB}}{f_s} = \frac{\beta f_{un}}{f_s} > \frac{(N+1)\,ln2}{\pi} \tag{4.12}$$

Thus for an SCI all we need to remember is that after the end of transient settling, v_x becomes $\alpha_0 v_{in}[nT_s]$ and v_{out} changes by $(1-\alpha_0)\,G_I v_{in}[nT_s]$. Also, we have the relation

$$\triangle v_{out} = \frac{(1-\alpha_0)}{\alpha_0} G_I v_x \tag{4.13}$$

4.2 The *K*-Path Switched-Capacitor Integrator (*K*-SCI)

In a discrete time realization of a delta-sigma modulator, using switched-capacitors, the maximum attainable oversampling clock rate is limited by the op-amp settling requirements. The op-amp settling error increases exponentially with a decrease in f_{un}/f_s ratio. The K-path switched-capacitor integrator increases the sampling rate of the conventional SC Integrator by K_{path} times, without any increase in op-amp settling requirements. The proposed integrator employs K-parallel switched-capacitors operating on the phases of a non-overlapping clock shown in Figure 4.2.

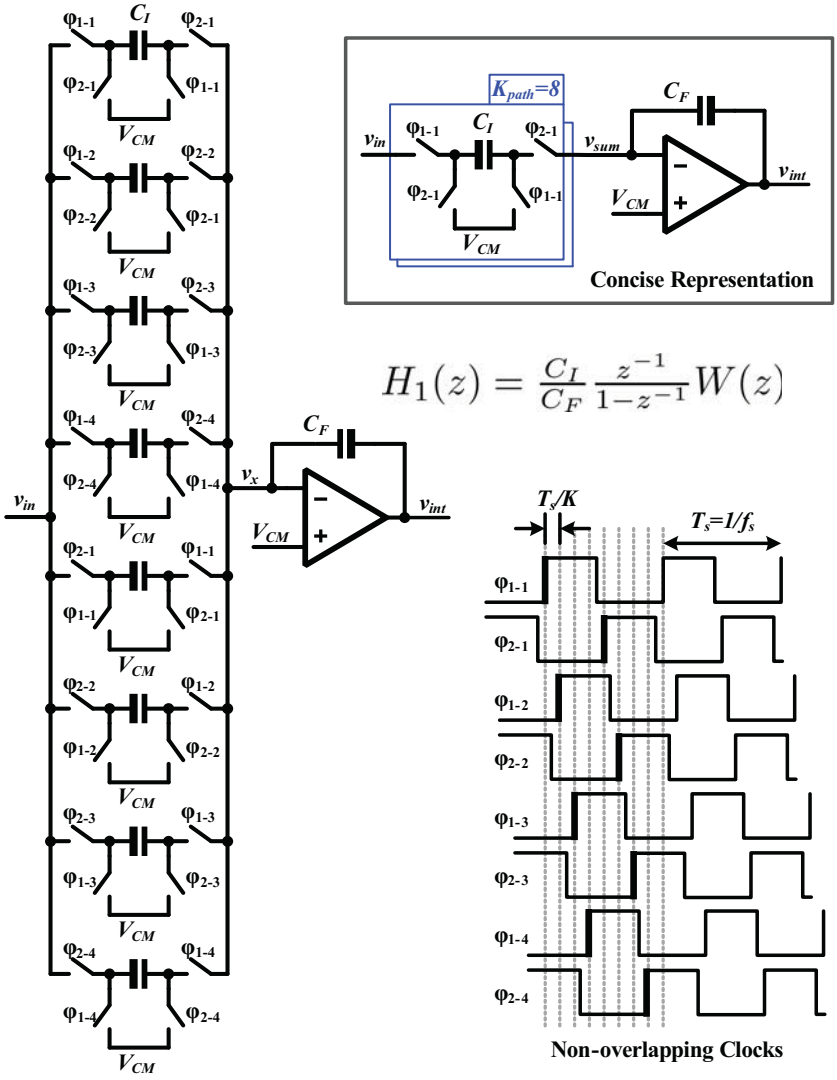

Figure 4.2: A K-path switched-capacitor integrator with a shared op-amp with the associated time-interleaved clocking scheme. A concise graphical representation for the K-SCI is shown in the inset.

In this integrator, for each of the switched-capacitor sections, the sampling and the integrating phases last for a time interval equal to $T_s/2$, i.e. half the clock period. Here, the unity-gain frequency, f_{un}, of the op-amp can be as low as $3f_s = \frac{3}{8}f_{s,new}$ for 90% settling for each path.

The discrete-time dynamics of the SC K-path integrator can be understood as follows. The input signal for a path is sampled on the falling edges of the 8-phase clock (say ϕ_{1-1} for the first path). This is followed by the rising edge of the phase ϕ_{2-1}, when the capacitor (C_I) with the charge proportional to the sampled input is connected to the integrator. Note that, at a particular instance four (i.e. $K_{path}/2$) sampling capacitors are connected to the integrator through the switches. Now, if the time interval between the rising edges of the 8-phase clock is much larger than the switched-capacitor charging time, charge sharing will occur amongst the four capacitors connected to the integrator's input node (v_x). After charge sharing, the integrator's output will change corresponding to the *initial-push* delivered by the partial settling of the integrator. The charge spreading effects are illustrated in Figure 4.3. In this discussion, it has been assumed that there is no slewing in the integrator and the settling is linear. Also, the DC gain of the op-amp is assumed to be large enough to avoid settling error.

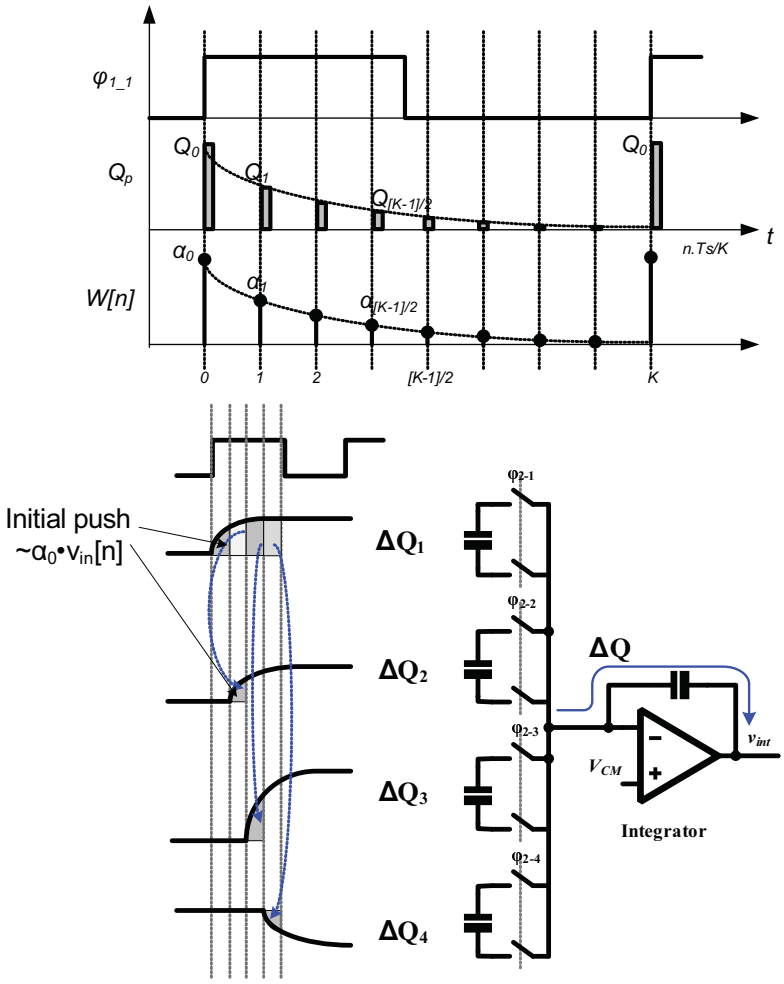

Figure 4.3: Illustration of charge-spreading and the equivalent filtering action in a K-path SCI.

The idea here is to emulate the operation of an ideal integrator without utilizing a faster op-amp for the high-speed integrator. Let the shared input node, v_x, of the integrator has a voltage equal to v_0 at time $t = 0$–. At this instance, input voltage $v_{in}[0]$ is sampled on the input capacitor (C_I) in the first path with the falling edge of phase ϕ_{1-1}. Then, at $t = 0+$, when ϕ_{1-1} goes high, charge sharing occurs amongst the capacitors of the paths enumerated 0, 5, 6 and 7. The resulting voltage on node v_x just

after charge sharing is given as

$$v_x(t=0) = \frac{3}{4}v_0 + \frac{1}{4}v_{in}[0] \tag{4.14}$$

Now this voltage spike on the node v_x will decay over the *time-slice* $T_{s,new}(=T_s/K)$ and will be reduced to $\alpha_0 v_x[0]$ (see Equation. 4.13). The coefficient α_0 represents the initial 'push' rendered by the partial settling of the integrator. Thus after one time-slice, we have

$$v_x(t=T_s/K) = \frac{3}{4}\alpha_0 v_0 + \frac{1}{4}\alpha_0 v_{in}[0] \tag{4.15}$$

Let the initial condition $v_0 = 0$. Then, after dropping the term T_s/K and using only the discrete-time indices, we get

$$v_x[0] = v_x[T_s/K] = \frac{1}{4}\alpha_0 v_{in}[0] \tag{4.16}$$

Similarly, we can write the progression

$$\begin{aligned}
v_x[1] &= \frac{1}{4}\alpha_0 v_{in}[1] + \frac{3}{4^2}\alpha_0^2 v_{in}[0] \\
v_x[2] &= \frac{1}{4}\alpha_0 v_{in}[2] + \frac{3}{4^2}\alpha_0^2 v_{in}[1] + \frac{3^2}{4^3}\alpha_0^3 v_{in}[0] \\
\cdots &\quad \cdots \quad \cdots \\
v_x[n] &= \frac{1}{4}\alpha_0 v_{in}[n] + \frac{3}{4^2}\alpha_0^2 v_{in}[n-1] + \frac{3^2}{4^3}\alpha_0^3 v_{in}[n-2] + \cdots + \infty
\end{aligned} \tag{4.17}$$

Thus, we have

$$v_x[n] = \frac{\alpha_0}{4}\sum_{i=0}^{\infty}\left(\frac{3}{4}\alpha_0\right)^i v_{in}[n-i] \tag{4.18}$$

or

$$V_x(z) = \frac{\alpha_0}{4} \frac{1}{\left(1 - \frac{3}{4}\alpha_0 z^{-1}\right)} V_{in}(z) \tag{4.19}$$

In general for K-paths we have

$$V_x(z) = \frac{\alpha_0}{K_{path}/2} \frac{1}{\left(1 - \frac{(K_{path}/2)-1}{(K_{path}/2)}\alpha_0 z^{-1}\right)} V_{in}(z) \tag{4.20}$$

Now, there will be a transfer of charge from the $K_{path}/2$ capacitors attached to the node v_x to the integrating capacitor. Using Equation. 4.13 this will lead to the change in the output given by

$$\begin{aligned} \triangle V_{out}(z) &= \frac{(1-\alpha_0)}{\alpha_0} \frac{\left(K_{path}/2\right) C_I}{C_F} \frac{\alpha_0}{K_{path}/2} \frac{1}{\left(1 - \frac{(K_{path}/2)-1}{(K_{path}/2)}\alpha_0 z^{-1}\right)} V_{in}(z) \\ &= \frac{C_I}{C_F} \frac{(1-\alpha_0)}{\left(1 - \frac{(K_{path}/2)-1}{(K_{path}/2)}\alpha_0 z^{-1}\right)} V_{in}(z) \end{aligned} \tag{4.21}$$

Thus, the equivalent transfer function for the K-path integrator is given as

$$H_1(z) = \frac{C_I}{C_F} \frac{z^{-1}}{1 - z^{-1}} \frac{1 - \alpha_0}{1 - \gamma_0 z^{-1}} \tag{4.22}$$

where the op-amp settling factor $\alpha_0 = e^{-\pi\beta \frac{f_{un}}{K_{path} f_s}}$ and the additional pole location is given as $\gamma_0 = \left(\frac{K_{path}/2-1}{K_{path}/2}\right)\alpha_0$. This is equivalent to an ideal discrete-time integrator response being convolved with a charge-spreading filter given by the transfer function

$$W(z) = \frac{1 - \alpha_0}{1 - \gamma_0 z^{-1}} \tag{4.23}$$

The K-path integrator acts like an integrating lowpass filter and is subsequently used in K-path noise-shaping DSMs. We can observe that as the number of paths increases,

the DC gain of the charge-spreading filter $W(z)$ becomes

$$W(f=0) \approx W(z=1) = \lim_{K_{path}\to\infty} \frac{(1-\alpha_0)}{\left(1-\frac{(K_{path}/2)-1}{(K_{path}/2)}\alpha_0\right)} = \frac{(1-\alpha_0)}{(1-\alpha_0)} = 1 \qquad (4.24)$$

which implies that almost all of the input charge sampled on each of the input capacitors is eventually transferred to the integrator output, even for low values of the settling factor α_0. This is the principle reason behind using the K-path approach rather than employing a single-path DSM at Kf_s clock frequency with partial settling of $(1-\alpha_0)$. Figure 4.4 shows the magnitude response of the K-SCI ($H_1(z)$) for $K_{path} = 8$, β = 0.5 and $f_{un} = 1.5f_s$. Also, the magnitude responses of the charge-spreading filter, $W(z)$, and the ideal integrator $H(z)$ are plotted. Here, we can observe that the K-SCI's magnitude response closely follows the ideal SCI's response at low frequencies with a loss of only 1.5 dB.

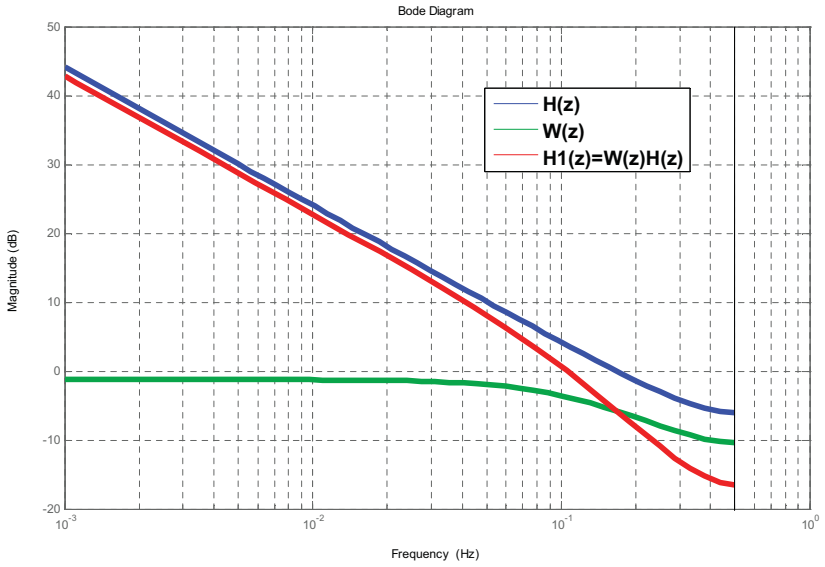

Figure 4.4: A plot showing the K-path integrator magnitude response for $f_{un} = 1.5 f_s$. Here, $H(z)$ is the near-ideal integrator response, $W(z)$ is the response of the charge spreading filter and $H_1(z) = W(z)H(z)$ is the response of the K-path integrator.

Thus, the K-path SCI implements a faster integrator with near ideal performance with much lower op-amp gain-bandwidth requirements. The transient operation of the K-path SCI is illustrated in the simulation results shown in Figure 4.5.

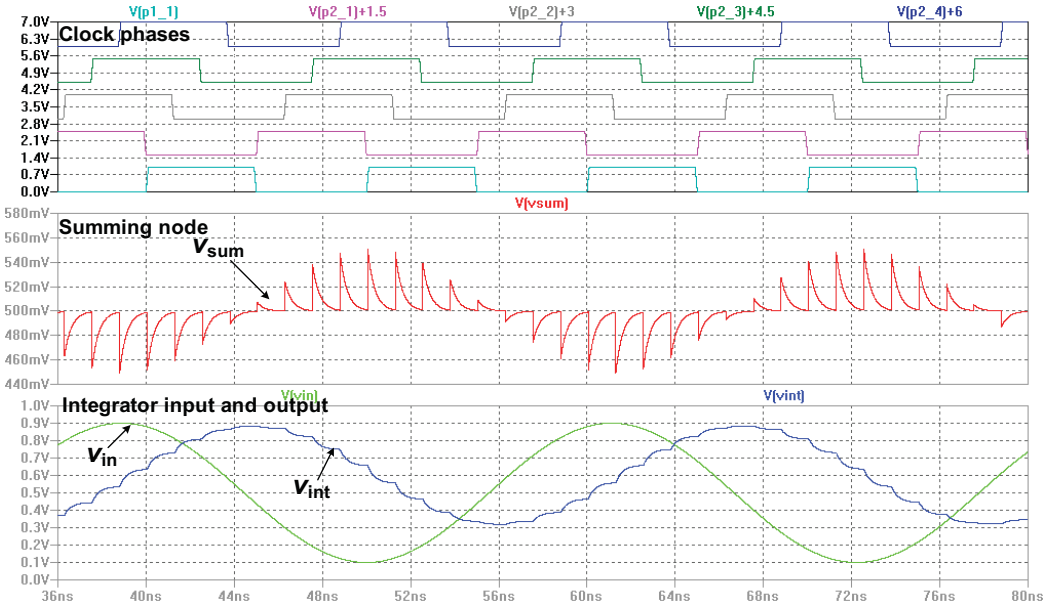

Figure 4.5: Transient simulation of a K-path integrator showing the integrator input and output, the op-amp summing node and the clock phases.

4.2.1 Path Mismatch in the K-path SC Integrator

The mismatch in the input sampling capacitors (the K-Deltas) will contribute to distortion errors due to path gain mismatches. The skew in the K-phases of the clock will also lead to reduction in SNDR as described in Section 2.1. Since the op-amp is shared across the paths, it doesn't contribute to any path mismatch. As illustrated in Figure 4.3, during any clock phase, $\frac{K_{path}}{2}$ sampling capacitors ($C_I's$) are connected together to transfer the charge collectively. Thus, the mismatch error of each of the sampling capacitors is averaged by $\frac{K_{path}}{2}$, and thus the equivalent capacitor mismatch in a K-SCI is estimated as

$$\sigma_{cmK} = \frac{\sigma_{cm}}{\sqrt{K_{path}/2}} \tag{4.25}$$

However, if oversampling greater than K_{path} is employed, the distortion tones located at the multiple of $1/f_s$ can be avoided.

4.3 The First-Order K-Delta-1-Sigma Modulator

The K-Delta-1-Sigma (KD1S) was disclosed in [12] to achieve wideband noise-shaping using a time-interleaved switched-capacitor implementation. The KD1S, shown in Fig. 4.6, employs K time-interleaved sampling paths (K-Deltas) with a shared integrator (1-Sigma) [14]. Here, the KD1S modulator is clocked by $K-$ phases of a clock with rate equal to f_s. The effective sampling rate of the modulator is set by the spacing between the edges of the clock phases and is given as [13]

$$f_{s,new} = K_{path} \cdot f_s \tag{4.26}$$

These K- non-overlapping clock-phases can be generated by using a ring-oscillator or a Delay Locked Loop (DLL). If the phases are tapped from a ring oscillator, designed using inverters with 10 ps delay, an effective sampling frequency ($f_{s,new}$) of 100 GHz can be achieved [13]. However, the maximum achievable effective sampling rate is determined by the loop-delay in the KD1S modulator. Also, summing of the K-path outputs, $y_k[n]$, $k = 0, 1, .., (K–1)$, using a fast adder leads to a path-filter response of $(1–z^{–K})/(1–z^{–1})$, which acts as a simple decimation filter. As shown in Figure 4.6, the input sampling phase for a path lasts for T_s/K_{path} time-slice while the integrating phase has duration equal to $T_s/2$. As we can observe the integrator is connected to $K_{path}/2$

distinct paths at any given time, and thus spreading the sampled input signal across $K_{path}/2$ paths.

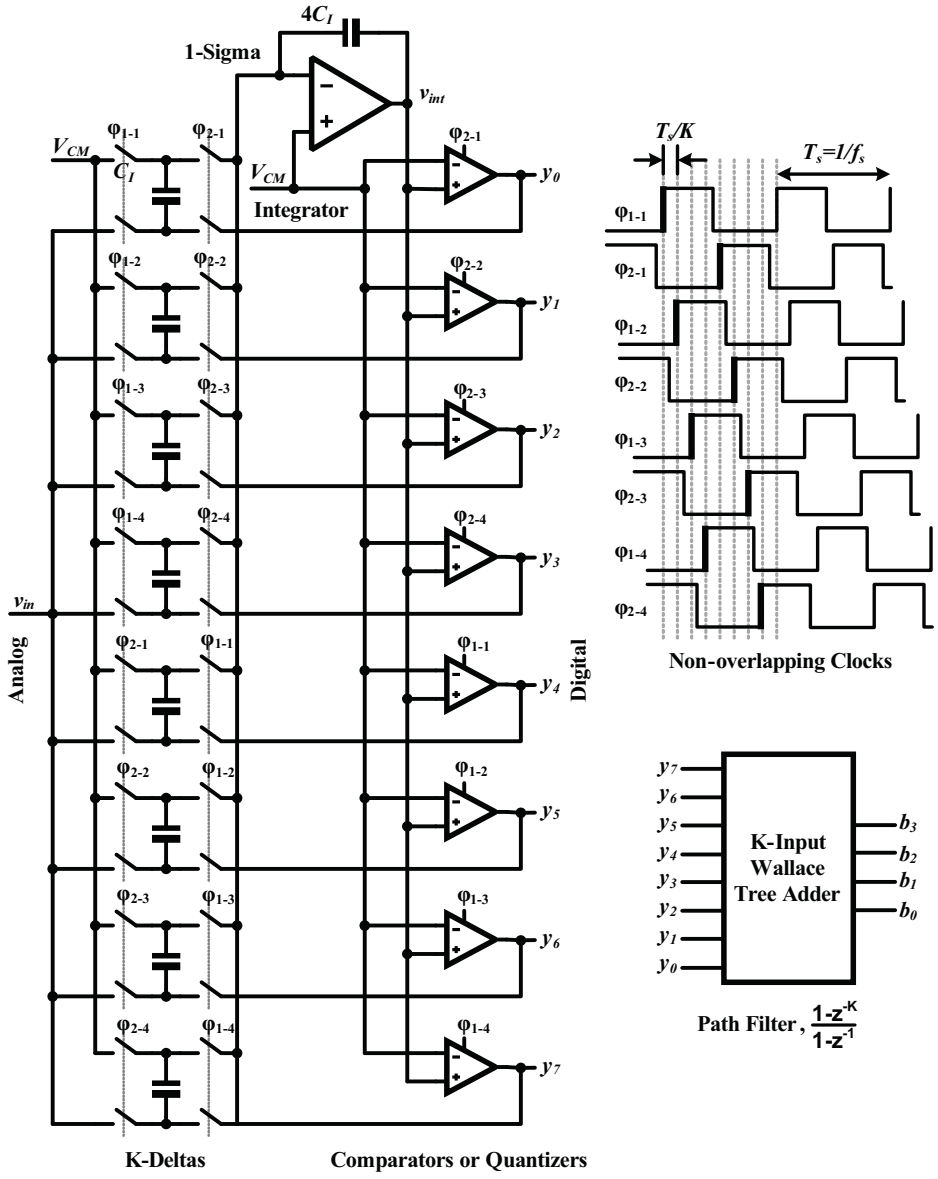

Figure 4.6: The *K*-Delta-1-Sigma modulator topology.

Since a single op-amp is shared across all the K- paths, the forward path mismatches due to the op-amp offset and gain-mismatch are obviated. However, we still need to consider the effects of the capacitor mismatch across the K-deltas discussed in Section 4.4. The offsets of each of the comparators are desensitized by the large loop-gain. We can observe that the shared integrator in the KD1S, acts like the K-path switched-capacitor integrator discussed earlier in Section 4.2. The K-path integrator can be designed with an op-amp with a unity-gain frequency (f_{un}) equal to a small multiple of f_s, the clock rate. This eliminates the need for a high-speed op-amp for ultra high-speed (GHz range) oversampling.

In order to achieve true first-order noise-shaping, the comparator in each path must fully respond to the partial settling of the integrator within $T_s/(2K_{path})$ time interval. In other words, the quantization noise in the modulator is differentiated in every T_s/K_{path} *time-slice*. The noise-transfer spectrum for the ideal KD1S modulator is shown in Fig. 4.7 and compared with the noise-shaping of a parallel DSM. Here, the quantization noise is pushed out to frequencies as high as $K_{path} \cdot f_s/2$ and thus achieving noise-shaping similar to a first-order delta-sigma modulator operating with a $K_{path} \cdot f_s$ effective clock rate. The noise transfer function for the ideal KD1S is

$$NTF(f) = 2sin\left(\frac{2\pi f}{K_{path} f_s}\right) \tag{4.27}$$

and the effective number of bits is given as

$$N_{eff} = N - 0.566 + 1.5 \cdot log_2(K_{path} \cdot OSR) \tag{4.28}$$

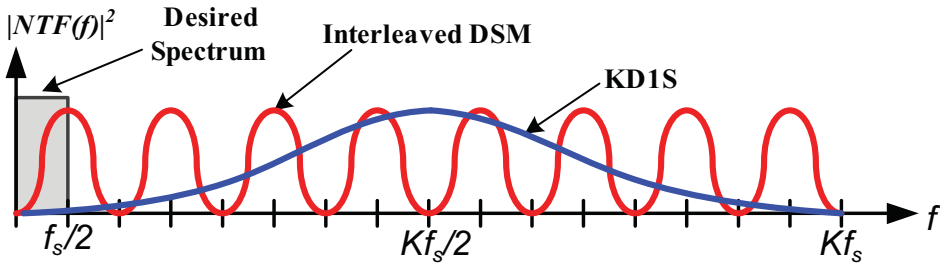

Figure 4.7: True wideband noise-shaping using a *K*-Delta-1-Sigma Modulator.

The the KD1S topology seen in Fig. 4.6 achieves a 1.5 bit gain in resolution per doubling in the number of paths. In other words, doubling of the number of paths has the same effect as doubling the *OSR*. Note that the order of the state-space of the KD1S loop-filter is equal to unity, as it employs a single *K*-path integrator to implement its state-space. Hence, despite employing time-interleaved sampling, the KD1S modulator is not analogous to time-interleaved (or parallel) delta-sigma modulators where the effective order of the system is equal to the number of paths. Due to this distinction the KD1S topology, employing a single op-amp, can't be used for polyphase implementation of complex transfer functions as in [45]. The advantage of the KD1S modulator lies in the fact that it enables very high sampling rate using switched-capacitors with loop-delay only limited by the comparator delay and thus alleviating the stringent bandwidth requirements on the op-amp employed in the switched-capacitor integrator.

4.3.1 Ideal Simulation Results

The simulation result for an example KD1S modulator with ideal components is illustrated in Figure 4.8. Here, $K_{path} = 8$ paths, each path clocked with a clock frequency

(f_s) of 100 MHz. The effective sampling rate, $f_{s,new}$, is equal to 800 MHz. The measured (using Matlab) signal to noise ratio (SNR) for a signal bandwidth of 6.25 MHz (i.e. $K_{path} \cdot OSR = 8 \times 8 = 64$) is equal to 58 dB or 9.43 bits in resolution. This establishes the true first-order noise-shaping in a KD1S modulator.

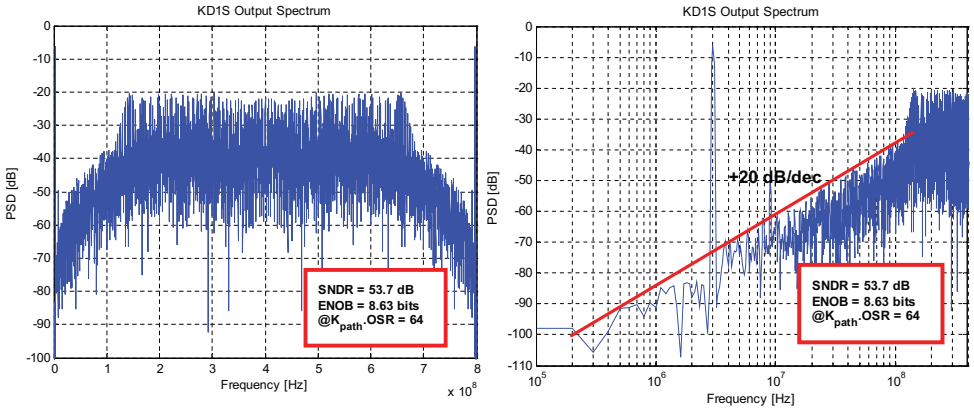

Figure 4.8: Simulation results (PSD of the output with linear and log frequency axes) for a KD1S modulator with ideal components. Here, $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz, $OSR = 8$, and $BW = 6.25$ MHz.

4.3.2 Noise Flow in the KD1S Modulator

Figure 4.9 illustrates the design intuition behind the first-order noise-shaping in a KD1S. During phase ϕ_{2-1}, the first comparator quantizes the integrator output (v_{int}) and passes the output y_1 back to the first delta block within a time interval less than $T_s/(2K_{path})$.

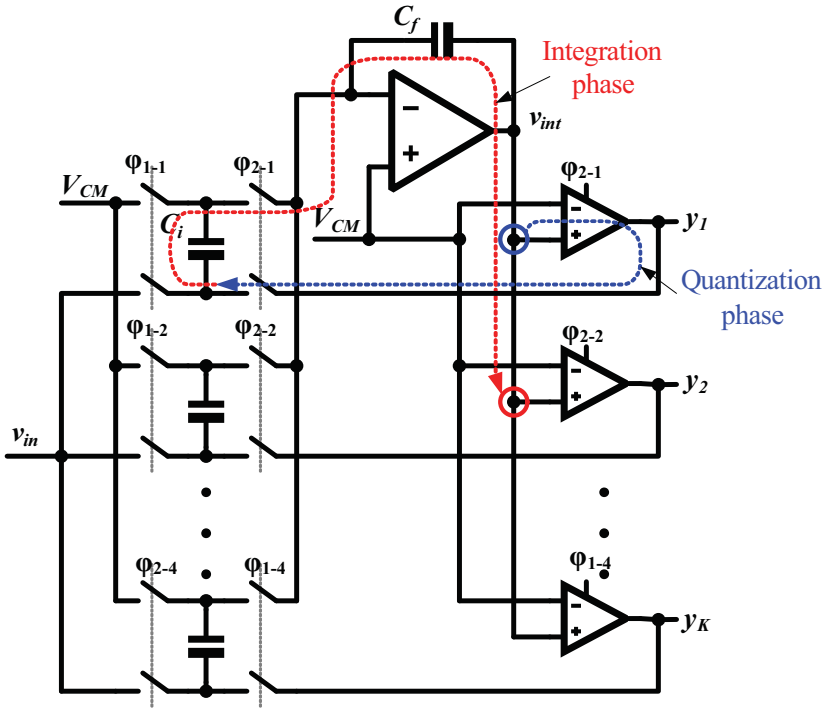

Figure 4.9: Illustration of the noise-shaping flow in a KD1S modulator.

When the ϕ_{2-1} switches close, the error signal ($v_{in}[n]$–$y_1[n]$) is fed back to the integrator. Now the integrator makes an initial push during the next $T_s/2K_{path}$ time-interval and updates the integrator output v_{int}. This new v_{int} value is now quantized (at phase ϕ_{2-2}) by the second comparator in the following time-slice and the error ($v_{in}[n+1]$–$y_2[n+1]$) is fed back to the integrator. This cycle repeats itself for all the paths with an unbroken noise-shaping sequence. Also note that for each of the paths, noise differentiation is performed and cycled back to the node v_{int} with a time-slice of T_s/K_{path}. Simulations show that if this noise-shaping sequence is broken, the SNR of the KD1S modulator drops. Thus for optimum performance, the comparators must be clocked on an earlier clock-phase such that the node v_{int} has the latest information. For

example, if the comparator delay (T_c) follows the condition,

$$T_s/2K_{path} < T_c \leq T_s K \tag{4.29}$$

then the first comparator should be clocked on the phase ϕ_{1-4} instead of ϕ_{2-1}, so that v_{int} gets the latest information fed back to it through the integrator.

4.4 Effects of Circuit Nonidealities in KD1S

The KD1S modulator, seen in Figure 4.6 was simulated using an ideal op-amp and comparators and thus it achieved true wideband noise-shaping. However, a practical modulator is implemented using op-amps having finite gain and unity-gain frequency and with comparators exhibiting a finite delay. The effects of the component non-idealities on the generalized KD1S modulator performance are detailed in this section. The following discussion also pertains to higher-order KD1S modulators which are presented in subsequent chapters.

4.4.1 Finite Op-amp Unity-Gain Frequency (f_{un})

Since a practical low-power KD1S modulator is realized using the K-path switched-capacitor integrator with a finite unity-gain frequency (f_{un}), an extra pole is introduced into the loop filter response as described in Section 4.2. The charge spreading filter, $W(z)$, appears in the signal and noise transfer functions of the modulator which are now

given by

$$\begin{aligned} NTF(z) &= \frac{1}{(1+H(z)W(z))} \\ STF(z) &= \frac{H(z)W(z)}{(1+H(z)W(z))} \end{aligned} \tag{4.30}$$

where $W(z)$ is given by Equation 4.23 as $W(z) = \frac{1-\alpha_0}{1-\gamma_0 z^{-1}}$ where $\alpha_0 = e^{-\pi\beta\frac{f_{un}}{Kf_s}}$ and the additional pole location is given as $\gamma_0 = \left(\frac{K_{path}/2-1}{K_{path}/2}\right)\alpha_0$. Recalling that the factor α_0 results for the partial settling of the op-amp in a single time-slice $\left(\frac{T_s}{K_{path}}\right)$ and leads to the parasitic pole at $z = \gamma_0$ in the integrator's frequency response. The additional factor of $\left(\frac{K_{path}/2-1}{K_{path}/2}\right)$ results from the loss of charge in the shared $\frac{K_{path}}{2}$ capacitors when a capacitor leaves the charge-sharing assembly and a fresh capacitor joins it with new information to charge share with the remaining $\left(\frac{K_{path}}{2}-1\right)$ capacitors. The resulting noise transfer function for the single-bit first-order KD1S modulator (assuming a quantizer gain of 1) is given by

$$NTF(z) = \frac{\left(1-z^{-1}\right)\left(1-\gamma_0 z^{-1}\right)}{1-(\alpha_0+\gamma_0)z^{-1}+\gamma_0 z^{-2}} \tag{4.31}$$

The parasitic pole $z = \gamma_0$ of the K-SCI response leads to an NTF zero at $z = \gamma_0$. The STF is given as

$$STF(z) = \frac{(1-\alpha_0)z^{-1}}{1-(\alpha_0+\gamma_0)z^{-1}+\gamma_0 z^{-2}} \tag{4.32}$$

The effect of the finite unity-gain frequency f_{un} of the op-amp and hence charge spreading response, $W(z)$, is shown in Figure 4.10. An interesting effect on the noise-shaping is observed in the simulations due to the presence of the parasitic NTF zero at $z = \gamma_0$. The extra NTF zero leads to a second-order noise-shaping near the DC and hence

slightly increases the resulting SNDR. From the simulation of the KD1S modulator with $f_{s,new} = K_{path} \cdot f_s = 8 \cdot 100 = 800$ MHz and $OSR = 8$, an op-amp unity-gain frequency equal to $f_s = \frac{3}{8} f_{s,new} = 300$ MHz leads to an optimal SNDR equal to 56.7 dB or 9.13 bits in resolution. All the Matlab simulated spectrum plots presented in this dissertation are generated by extending the Delta-Sigma Toolbox [25] explained later in Chapter 6. In these plots as in Figure 4.10, the zig-zagged blue lines represent the spectrum of the time-domain simulation of the DSM, while the solid red line denotes the NTF's magnitude response. Note that, in these simulated plots, the comparator delay has been kept ideal i.e. equal to zero.

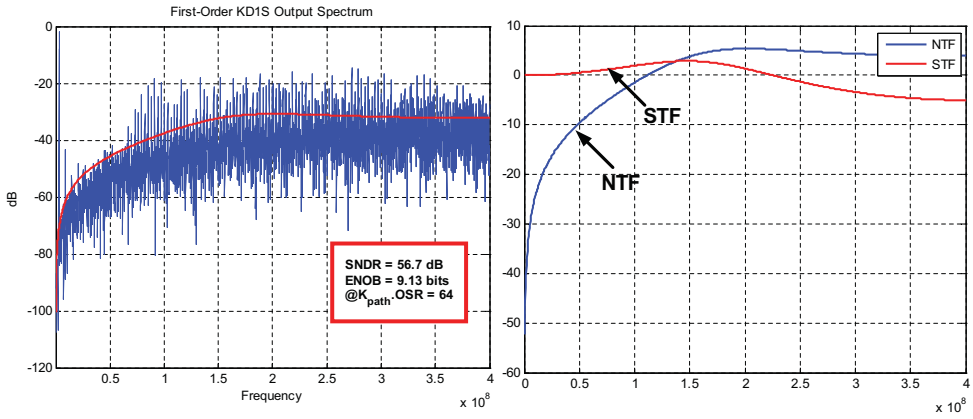

Figure 4.10: KD1S noise-shaping with an op-amp with finite unity gain frequency ($f_{un} = \frac{3}{8} f_{s,new} = 300 MHz$). The second plot shows the NTF and STF for the modulator. Here, $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz, $OSR = 8$, and $BW = 6.25$ MHz.

Simulations demonstrate a loss of 1-bit in resolution for the worst case of $f_{un} = f_s = \frac{f_{s,new}}{K_{path}}$ (i.e. the op-amp unity gain frequency is equal to the base clock frequency). Despite this reduction in SNR, the first-order KD1S bit resolution is still quite significant. Thus an optimal value of op-amp f_{un} must be chosen for a given resolution and

power consumption. Note that even though the requirements on the op-amp's f_{un} are relaxed by K_{path}-times, due to the large fan-out of the sampling and feedback capacitance this does not translate into a K_{path}-fold power reduction in the op-amp. The effective load on the op-amp in a KD1S topology is $C_L = \frac{K_{path}}{2}C_{out} + C_F||\frac{K_{path}}{2}C_I$, where C_{out} is the load on op-amp's output for a single path. Assuming a single pole op-amp (i.e. $f_{un} = g_m/C_L$), the relative benefit in op-amp's power consumption, η, when using a KD1S modulator over an equivalent single-path delta-sigma modulator is estimated by taking the ratio of the required transconductances ($g'_m s$)

$$\eta = \frac{g_{m,DS}}{g_{m,KD1S}} = \frac{3K_{path}f_s(C_{out} + C_F||C_I)}{3f_s(\frac{K_{path}}{2}C_{out} + C_F||\frac{K_{path}}{2}C_I)} = \frac{K_{path}\,(C_{out} + C_F||C_I)}{\frac{K_{path}}{2}C_{out} + C_F||\frac{K_{path}}{2}C_I} \tag{4.33}$$

For K_{path}= 8 and for typical values for the capacitors being given by $C_I = 100\,fF$, $C_F = 500\,fF$ and $C_{out} = 100\,fF$, we get $\eta = 2.35$. Thus, we get an op-amp power advantage of roughly 2.4 times over the corresponding single-path, discrete-time delta-sigma operating at $K_{path}f_s$ clock rate. In this calculation, the parastitic loading on the op-amp was ignored but it will be higher as the number of paths increase. Thus, we can observe that with an increase in the number of paths, the larger capacitance fan-out on the op-amp increases the power consumption of the modulator.

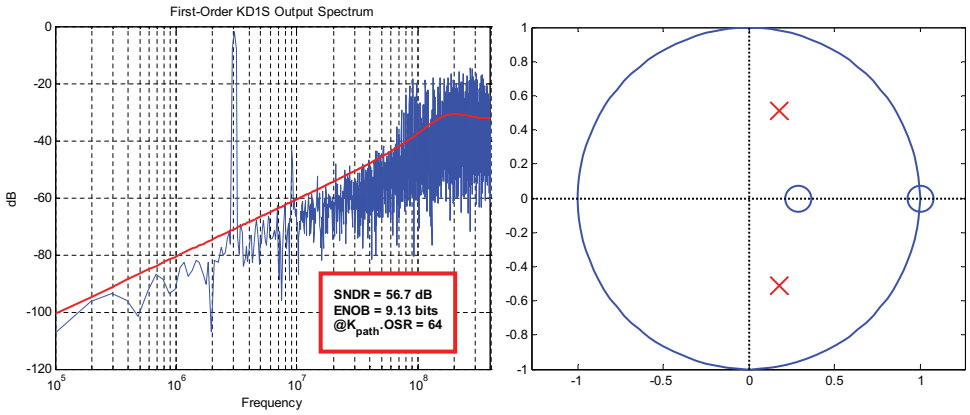

Figure 4.11: Simulated PSD of the output and the NTF pole-zero plot for the first-order KD1S modulator with $f_{s,new} = 800$ MHz, $f_{un} = \frac{3}{8} f_{s,new} = 300$ MHz, $K_{path} = 8$,$OSR = 8$, and $BW = 6.25$ MHz.

4.4.2 Finite Op-amp Gain

If the DC gain A_{OL} of the op-amp is finite, then the output of the K-path integrator is given as

$$H_1(z) = \frac{C_I}{C_F} \frac{pz^{-1}}{1 - pz^{-1}} W(z) \tag{4.34}$$

where the location of the pole, p, is given by [23]

$$p = \frac{1}{1 + \frac{C_I}{C_F} \cdot \frac{1}{A_{OL}}} \approx 1 - \frac{C_I}{C_F} \cdot \frac{1}{A_{OL}} \tag{4.35}$$

The resulting pole location p is slightly less than 1. The gain of the integrator is not infinite as for the ideal case and thus the integrator is lossy or *leaky*. The noise transfer function of the KD1S modulator is now given as

$$NTF(z) = \frac{1 - pz^{-1}}{1 - \left(1 - \frac{C_I}{C_F} W(z)\right) pz^{-1}} \tag{4.36}$$

In the above equation, we can observe that the NTF's zero has shifted from its ideal location at $z = 1$ to $z = p$ inside the unit circle. This leads to the *filling-in* of the notch in the signal band of interest, i.e. $f \in \left[0, \frac{f_{s,new}}{2K_{path}OSR}\right]$, with quantization noise. This is due to the fact that at low frequencies $|NTF(f)|^2 \approx A_{OL}^{-2} + (2\pi f)^2$ across the signal band, as opposed to the case when $A_{OL} = \infty$ [23]. Now for this additional noise to be lower than 0.2 dB, the design criterion for the first-order KD1S,

$$A_{OL} > K_{path} \cdot OSR \tag{4.37}$$

must be satisfied . Thus for a KD1S design with $OSR = K_{path} = 8$, we require an op-amp gain of at least 40 dB. The gain-error due to the finite op-amp gain is

$$\varepsilon_{gain} = \frac{C_I}{C_F} \cdot \frac{1}{A_{OL}} \tag{4.38}$$

Figure 4.12 illustrates the effect of the finite gain of the op-amp employed in the KD1S modulator with $f_{un} = \frac{3}{8} f_{s,new}$= 300 MHz. Here, the SNDR drops by 5.6 dB ($\sim$0.93 bit) as A_{OL} drops from 50 dB to 25 dB. The gain-error term changes the effective gain of the integrator but doesn't affect the SNR of the modulator. Also, a large op-amp gain reduces the dead-band around $v_{in} = 0$, given by $1/2A_{OL}$ [23].

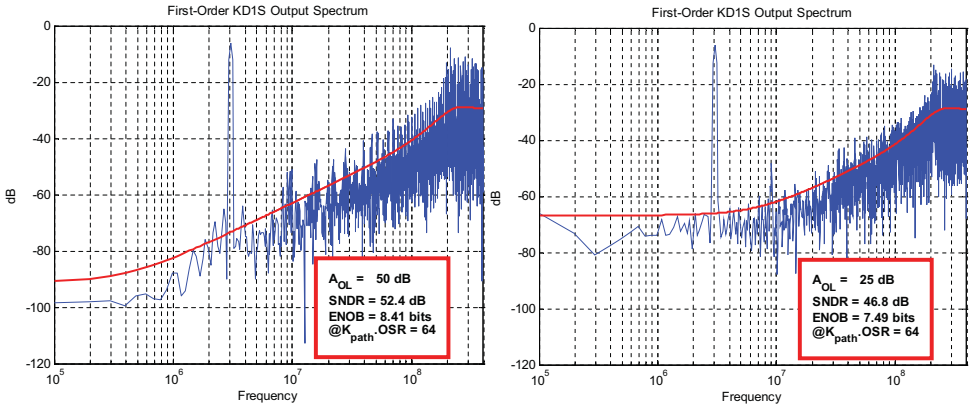

Figure 4.12: Simulated NTFs for the first-order KD1S modulator with the op-amp open-loop gain (A_{OL}) of 50 dB and 25 dB. Again here, $f_{s,new} = 800$ MHz, $f_{un} = \frac{3}{8} f_{s,new} = 300$ MHz, $K_{path} = 8$, $OSR = 8$, and $BW = 6.25$ MHz.

4.4.3 Slewing in the Op-amp

The analysis in Section 4.4.1 assumed that the op-amp follows true first-order settling and doesn't have any slew rate limitations. However, a real op-amp does exhibit a finite slew rate which limits the maximum rate at which the op-amp's output can change [46]. A pertinent model for the settling characteristics of a single-path switched-capacitor integrator is given by [47]

$$v_{out}((n+1)T_s) = v_{out}(nT_s) + g\left(a_1 \cdot v_{in}(nT_s) - a_2 \cdot y(nT_s)\right) \tag{4.39}$$

where $a_1$and a_2 are the gains for the input signal $v_{in}(nT_s)$ and the modulator feedback DAC output $y(nT_s)$ respectively. The function $g(x)$ describes the non-linear settling of the op-amp due to finite unity-gain frequency and slew-rate limitation. The effective

gain due to a slew-rate limited single-pole settling is given as [47]

$$g(x) = \begin{cases} x\left(1 - e^{-t_s/\tau}\right), & |x| \leq \tau \cdot SR \\ x - sgn(x) \cdot \tau \cdot SR \cdot e^{\left(\frac{|x|}{\tau \cdot SR} - \frac{t_s}{\tau} - 1\right)}, & \tau \cdot SR \leq |x| \leq (\tau + t_s) SR \\ sgn(x) \cdot SR \cdot t_s, & |x| > (\tau + t_s) SR \end{cases} \tag{4.40}$$

where $\tau = \frac{1}{2\pi\beta f_{un}}$ is the time-constant for the single-pole op-amp, SR is the maximum slew-rate of the op-amp and $t_s = \frac{T_s}{2}$ is the available settling time for the integrator. The slew-rate for the single-pole op-amp is given by

$$SR = \frac{I_{SS}}{C_L} \tag{4.41}$$

Here, I_{SS} is the net bias current in the input diff-amp and C_L is the total load on the op-amp (see Equation 4.2). Figure 4.13 plots $g(x)$ vs x for a range of values of the product $\tau \cdot SR = \frac{SR}{2\pi\beta f_{un}}$, which represents the ratio of the slew-rate and the bandwidth of the op-amp. The settling time allowed for the integrator is $t_s = T_s/2$. Here the unity-gain frequency of the op-amp is chosen as $f_{un} = 3f_s$ and $f_{un} = f_s$ for the two plots. We can observe here that for $\tau \cdot SR \geq 1$, the settling is linear and the gain error is roughly 0.01% for $f_{un} = 3f_s$ and 20% for $f_{un} = f_s$. As the slew-rate of the op-amp decreases ($\tau \cdot SR < 1$), the settling is non-linear and is limited by the maximum slew-rate. This introduces input dependent distortion into the modulator's output and leads to a decrease in SNDR.

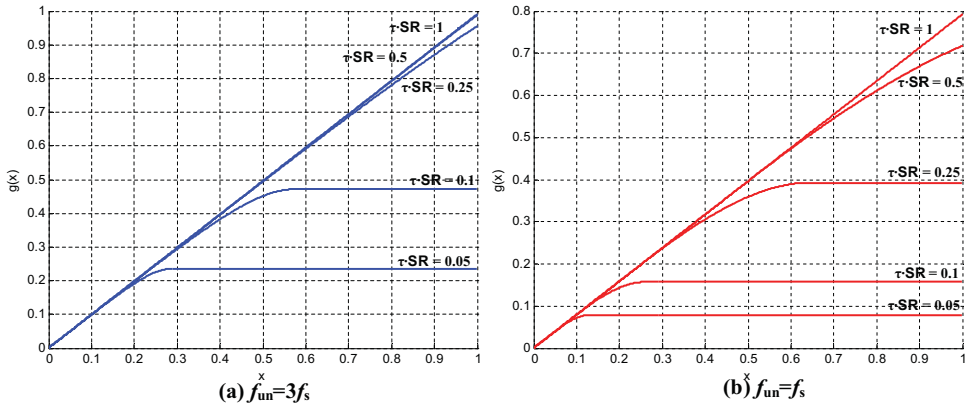

Figure 4.13: The behavioral model for the integrator settling with slew-rate limitations. The gain function g(x) is plotted for increasing values of $\tau \cdot SR$ and $t_s = T_s/2$.

The non-linear behavioral model seen in Equation 4.40 can be used for time-domain modulator simulation using either Matlab or Simulink. From the behavioral simulations performed in [47] the SNDR contours for slew-rate as a function of the op-amp bandwidth are plotted in Figure 4.14. The simulation results exhibited two distinct regions where high SNDR (100 dB for a third-order modulator) is obtained without requiring a high slew-rate. The first region, called the *slow regime*, corresponds to linear settling with no slew-rate limitations. In the slow regime, the number of settling time-constants ($n_\tau = t_s/\tau$) can be as low as 3 or 4, but the normalized slew rate ($SR_N = \frac{SR \cdot t_s}{a_{f1} \triangle_1}$) must be greater than n_τ. In this expression, $a_{f1} \cdot \triangle_1$ is the equivalent gain for the quantizer feedback to the first integrator of the modulator. This implies that if in a design n_τ increases due to a fast process corner while SR_N remains unchanged, the modulator deviates from the linear settling regime and the SNDR performance is degraded [47].

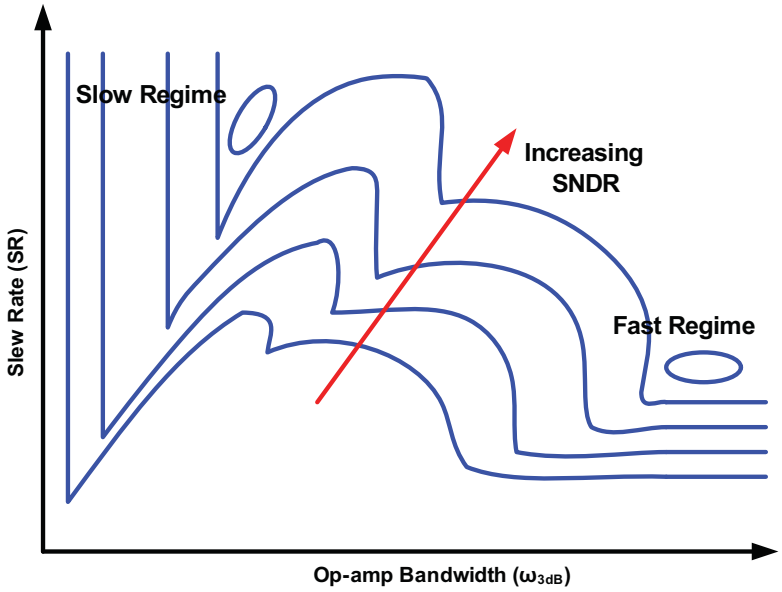

Figure 4.14: Slew-rate vs bandwidth contours for the switched-capacitor integrator.

In the *fast regime*, the integrator is strongly slew-rate limited but the integrator settling is fast enough to mitigate the effects of non-linear settling. This occurs for the case when $n_\tau > 12$. In this region, the normalized slew-rate (SR_N) only needs to be greater than 2 as opposed to a value of 3 or 4 in the case of the slow regime. Also if due to the fast process corner n_τ increases, the modulator's performance is enhanced. Depending upon the resolution of the modulator, the op-amp for the first integrator is carefully designed for accuracy by considering the intuition developed from this behavioral model.

In order to gain intuition for the slew-rate limitations of the KD1S modulator, we observe the time-domain settling of the K-path integrator. From Figure 4.3, we saw that the integrator is fired regularly every T_s/K_{path} time-slice and has partial exponential settling of $(1-\alpha_0)$ where $\alpha_0 = e^{-\pi\beta f_{un}/f_s}$ (i.e. 31% settling for $\frac{3}{8}f_{s,new}$) . The idea is that the charge for each path can take up to $K_{path}/2$ time-slices (i.e. $T_s/2$ total duration)

to be transferred to the integrating capacitor and thus reducing the limitation on the op-amp's unity-gain frequency requirements. Now, if we wish to operate the modulator in the slow regime with $f_{un} = \frac{3}{8} f_{s,new}$, we need to ensure that there is no slew-rate limitation on the op-amp for $t_s = \frac{T_s}{K_{path}}$. This implies that we need to satisfy the condition $SR > 1/\tau$ for complete linear settling of the op-amp. This leads to a lower bound on the slew-rate given by $SR > 1.34\,V/ns$ for a KD1S modulator with $f_s = 100\,MHz$, $K_{path} = 8$, and $f_{un} = 300\,MHz$. Operation of the KD1S modulator in the fast regime with $n_\tau > 12$ will lead to very high power consumption in the op-amp, and is thus avoided.

4.4.4 Real Quantizer Effects

So far in the simulations of the KD1S modulator, we have assumed an ideal quantizer (the comparator for a single-bit design) delay equal to zero, but in a real modulator the comparators will have a finite delay. In a KD1S modulator, the comparators are implemented using regenerative latches. This section discusses the impact of the real quantizer characteristics on the KD1S modulator performance.

The behavior of the quantizers operating at high-speed (GHz) sampling rates in a continuous-time delta-sigma modulator has been characterized in detail in [48]. Figure 4.15 illustrates the characteristics of a practical quantizer (or a comparator for single-bit quantization). Here, the input v_x is applied to the quantizer with a slope v_{sl} and the comparator is simulated for a complete set of (v_x, v_{sl}). The resulting time-delay normalized to the clock-period ($\rho_d = \frac{T_d}{T_s}$) is plotted on the y-axis. In an ideal quantizer

ρ_d is always zero irrespective of how small v_x is. However a real quantizer will exhibit the following three dominant non-idealities [48]:

Excess Delay

As seen in Figure 4.15 (b), the excess delay will correspond to a vertical shift. This is the minimum delay that will be offered by the quantizer, which must be accounted for in the modulator design.

Hysteresis

Hysteresis (see Figure 4.15 (c)) causes a horizontal shift in the x-axis proportional to the amount of hysteresis. In higher-order modulators, a large amount of hysteresis causes the histogram distribution of the integrator outputs to widen and cause harmonic distortion due to saturation. This is due to the fact that as long as the quantizer output level stays the same, the integrators in the loop-filter will continue to integrate in the same direction and thus causing larger signal swings. Thus the amount of hysteresis must be bounded to a smaller value in the range of 0.2 V [48].

Metastability

Figure 4.15 (d) depicts the effects of comparator metastability. Due to metastability, the sharp corner in the ideal quantizer becomes rounded. The area under the curve signifies the severity of metastability in the quantizer. From this curve, the comparator delay varies with the input value $v_x$and the slope v_{sl} of the input signal. The metastability of

the comparator results from its inability to resolve small inputs and reach the full logic level in the limited amount of settling time. The metastability of a comparator is related to its resolution and its small-signal gain. The probability of error due to metastability is given by the relation

$$P_e \approx 2^N \cdot \frac{1}{A_c} \cdot e^{-\frac{t_0}{\tau_c}} = 2^N \cdot \frac{1}{A_c} \cdot e^{-\pi \frac{BW}{f_s}} \tag{4.42}$$

where N is the quantizer resolution, A_c its small-signal gain, $\tau_c = \frac{g_m}{C_{load}}$ the settling constant for the regenerative latch and BW is the -3 dB bandwidth of the latch type comparator [5]. The comparator metastability severely degrades the performance of a modulator at high sampling speeds by whitening the shaped in-band quantization noise. Also there is an excess delay in the quantizer due to the dependence of the comparator delay on the input signal magnitude [49].

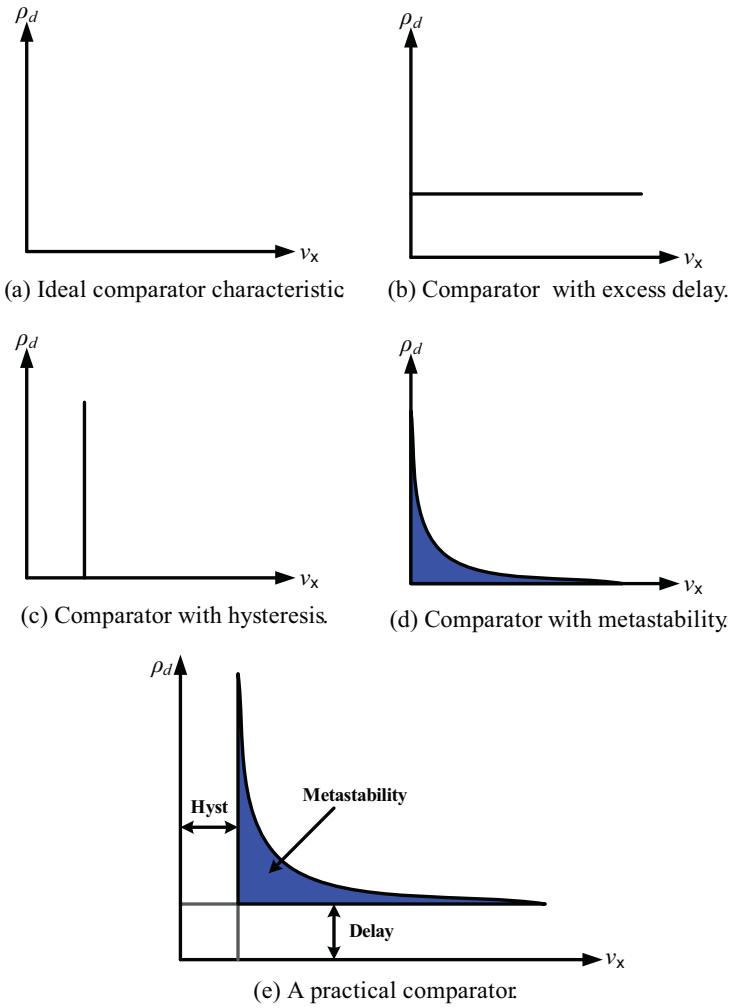

Figure 4.15: Illustration of the delay, hysteresis and metastability in a real comparator or quantizer.

A practical comparator (quantizer) exhibits all three non-idealities simultaneously. The impact of these non-idealities is now considered with respect to the KD1S modulator(s). The input referred offset and noise of the comparator is desensitized by the high integrator gain and large amount of hysteresis can be tolerated by the single-bit first-order KD1S modulator. Typically in a CMOS process, the cross coupled latch regeneration time (τ_{reg}) is inversely related to the f_T of the transistors and is in the GHz

range in the nano-CMOS processes. The comparator delay, T_c, is equal to the regeneration time (τ_{reg}) and the delay in the output buffer. Thus the KD1S modulator can be designed to operate at the rates governed only by the comparator settling. Since the integrator settling and comparator's delay can take independent time-slices of $\frac{T_s}{K_{path}}$ duration (i.e. z^{-1}delay each) to make a correct decision, as in the double-sampling case, the maximum achievable effective sampling rate ($f_{s,new}$) of KD1S modulator can be estimated as

$$f_{s,new} = \frac{T_s}{K_{path}} \leq \frac{1}{T_c} \tag{4.43}$$

We can still achieve noise-shaping when the path settling time is larger than T_s/K_{path} at the cost of larger in-band noise (IBN) and reduction in SNR. Figure 4.16 demonstrates the effect of comparator delay on the resulting KD1S SNR.

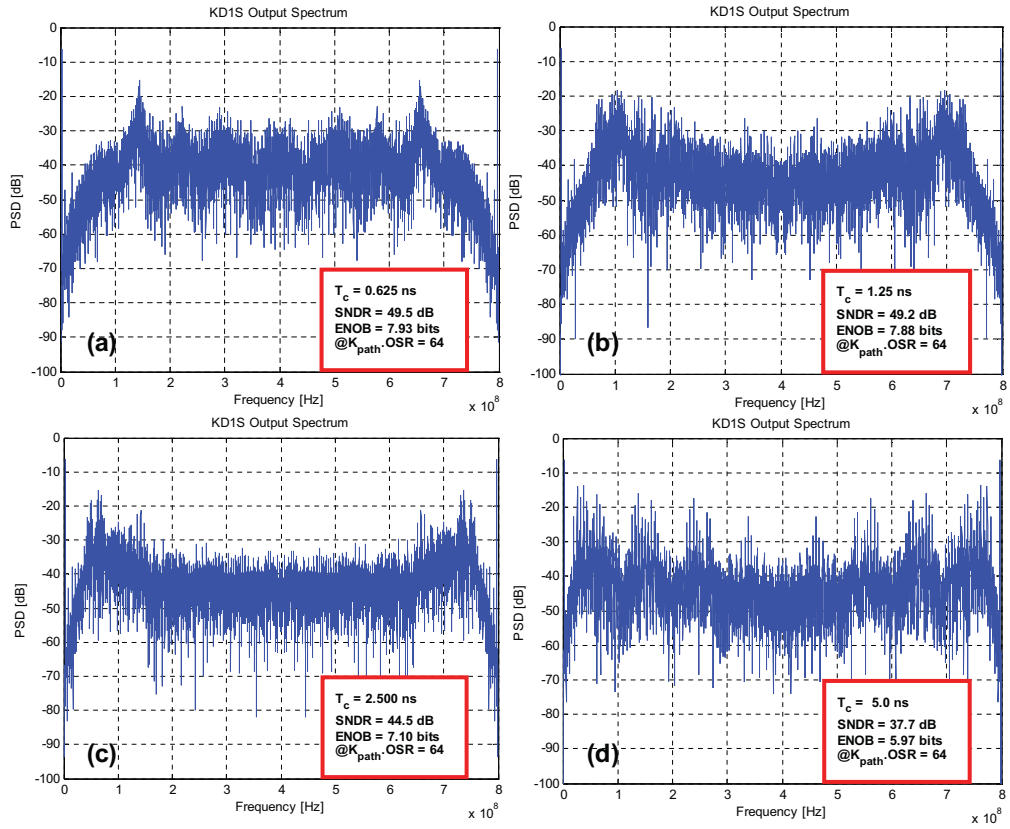

Figure 4.16: Effects of comparator delay on the SNR of a first-order KD1S modulator simulated in Spectre with $f_s = 100$ MHz, $f_{un} = 300$ MHz, $K_{path} = 8$, $OSR = 8$, and $BW = 6.25$ MHz. The KD1S modulators were simulated with a respective clocking scheme to minimize the loop-delay. (a) $T_c = 625$ ps, (b) $T_c = 1.25$ ns, (c) $T_c = 2.5$ ns, and (d) $T_c = 5.0$ ns.

Here, the SNR and the bit resolution degrade from 8-bits to 6-bits as we increase the comparator delay from $T_s/2K_{path}$ to $T_s/2$. From these results, the optimum operating delay of the comparator is at most T_s/K_{path}. Note that for each of these simulation with varying comparator delay, the clock phase for the comparators was adjusted such that the loop-delay is minimized. For this delay the NTF response shows a dip at the frequency $K_{path}f_s/2$. The two peaks in the NTF for this case can be explained by the Circular Clock Phase Diagrams (CCPD) devised by the author, as seen in Figure 4.17.

For the CCPD for $T_c < T_s/2K_{path}$, the integrator output (v_{int}) is picked up at the phase ϕ_{2-1}, quantized (Q-phase) and then partially integrated (I-phase) and returned to v_{int} within a single time-slice (T_s/K_{path}) just in time for the phase ϕ_{2-2}. This leads to a single noise-shaping loop and hence true noise-shaping with a single sine crest. On the other hand for the case when $T_c = T_s/K_{path}$, the value of v_{int} is picked up at the phase ϕ_{2-1}, quantized (Q-phase) and then partially integrated (I-phase) and returned to v_{int} only after two time-slices (i.e. $\frac{2T_s}{K_{path}}$ delay) just before the phase ϕ_{2-3}, and thus skipping over the clock phase ϕ_{2-2}. This leads to two noise-shaping loops being formed operating on alternate clock phases, leading an NTF response similar to the double sampling case. Also for the second case, the first comparator was clocked on the phase ϕ_{1-4} in order to maintain an unbroken noise-shaping sequence (optimal clocking). Therefore, the comparator delay and clocking are an important concern in the K-path modulator design.

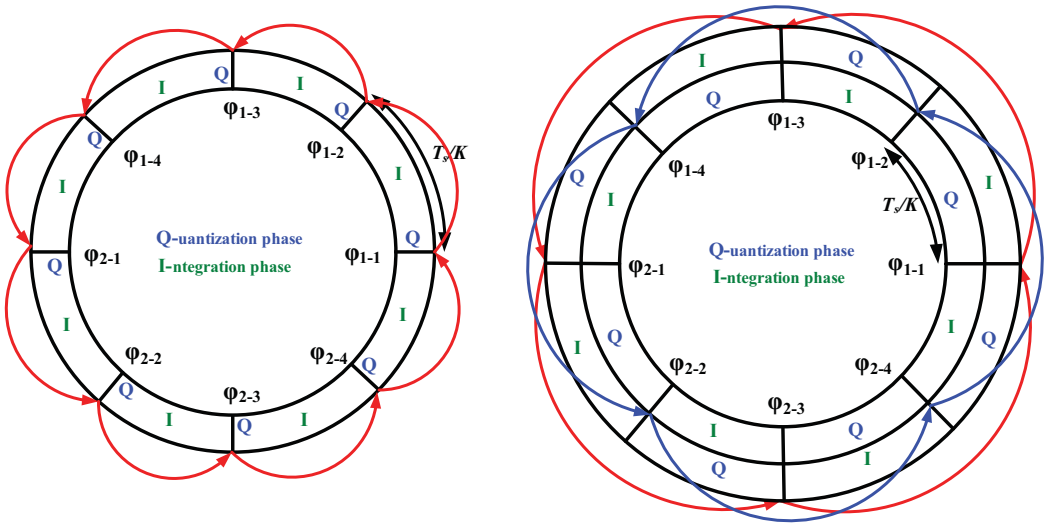

Figure 4.17: Circular clock phase diagram for KD1S modulator for two distinct comparator delays.

In order to accommodate the finite delay of the comparator, the NTF is now described as

$$NTF(z) = \frac{z^{-d}}{\left(1 + z^{-d}H(z)W(z)\right)} = \frac{\left(1 - z^{-1}\right)\left(1 - \gamma_0 z^{-1}\right)}{1 - (\gamma_0 + 1)z^{-1} + \gamma_0 z^{-2} + (1 - \alpha_0)z^{-(d+1)}} \quad (4.44)$$

where d is the delay of the comparator normalized to the time-slice T_s/K_{path}. For $T_s = T_s/K_{path}$, we have $d = 1$. Thus the comparator delay affects the location of the poles of the loop-filter and affects the stability of the modulator. The modulator with finite comparator delay of T_s/K_{path} (i.e. z^{-1}) is simulated in Matlab as shown in Figure 4.18. The resulting resolution is 7.98 bits which is in close agreement with the Spectre simulated result seen in Figure 4.16. Note that the poles in the NTF have moved out towards the unit circle when compared to the plot in Figure 4.11, which is the result of additional loop-delay due to the comparator.

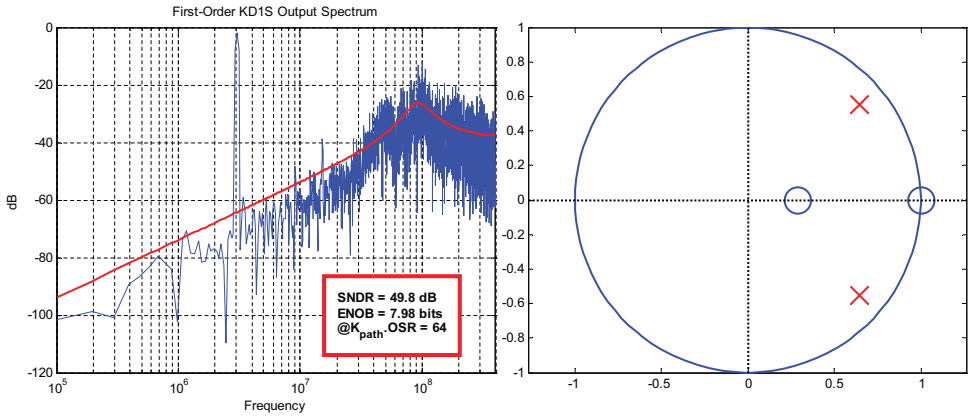

Figure 4.18: Matlab simulated PSD of the output and the NTF pole-zero plot for the first-order KD1S modulator with $f_{s,new} = 800$ MHz, $f_{un} = 300$ MHz, $K_{path} = 8$, $OSR = 8$, $BW = 6.25$**,** and the comparator delay $T_c = T_s/K_{path} = 1.25$ ns.

Effects of Signal Dependent Delay

As seen earlier the delay of a real comparator depends upon the input signal magnitude. For very small inputs, the comparator may take much longer than the expected comparator delay. This will be a frequent case in a delta-sigma modulator, where the quantizer input can get very close to its reference for comparison (i.e. V_{CM}). This effect is more pronounced at GHz speeds where the gain of the regenerative latch is low and the small input metastability is dominant [48]. In a single-path DSM, the comparator is allowed only $T_s/2$ to settle and then the latch is reset. If the comparator doesn't settle completely in that interval, then its a metastability error. But due to the structure of the KD1S topology where the comparator's output is connected to the input sampling capacitor for a duration of $T_s/2$, the comparator's output can continue to settle way over the T_s/K_{path} time-slice. Thus, in the presence of input dependent delay the transfer

function of the comparator can be modeled as

$$A_c e^{-s(T_d+\Delta t(n))} \tag{4.45}$$

where A_c is the variable gain of the comparator, T_d is the nominal comparator delay, and $\Delta t\,(n)$ is the variable delay due to the small input metastability. The probability distribution function (PDF) of $\Delta t\,(n)$ appears close to be exponential as seen in the curve in Figure 4.15 (e). The variable delay causes a modulation of the loop-delay in the modulator and contributes to the ripples in the NTF response. These ripples in the NTF increase the in-band noise and reduce the SNDR. This effect is more pronounced at GHz sampling frequencies where the variance of $\Delta t\,(n)$ is large. The effect of the variable delay of the comparator on the KD1S modulator performance must be carefully simulated for a given transistor-level implementation of the modulator. Verilog-A behavioral system modeling is quite useful for rapid simulation and characterization of non-ideal effects of comparators in a delta-sigma modulator [50].

4.4.5 Capacitor Mismatch, Phase Skew and Noise Folding

As seen for a double-sampling delta-sigma modulator in Section 3.3.1, the mismatch in the sampling capacitors leads to folding of shaped quantization noise from $f_s/2$ to the signal band. As we can observe in Figure 4.6, there are K_{path} distinct capacitors through which the shaped quantization noise is fed back to the modulator. A mismatch across these capacitors (i.e. the K-Deltas) will also lead to folding of shaped quantization noise into the signal band of interest as shown in Figure 4.19.

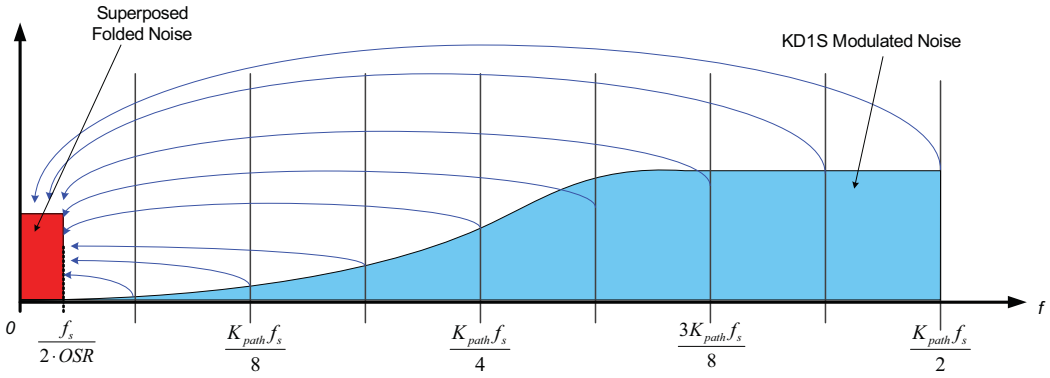

Figure 4.19: Noise-folding effects in a KD1S modulator due to path gain mismatches. The shaped quantization noise from the frequencies $kf_s,\ k = 1,..K_{path}$ gets folded into the signal band.

The derivation of noise-folding due to K-delta mismatches follows from the analysis of channel mismatch errors detailed in Section 2.1. In the KD1S modulator seen in Figure 4.6, the signal fed back to the input K-deltas is defined as

$$V_3(z) = z^{-\frac{K_{path}}{2}} V_{in}(z) - Y(z) \tag{4.46}$$

which implies that the difference of the input $v_{in}[n]$, delayed by $\frac{K_{path}}{2}$ samples delay, and the output $y_i[n]$, $i = (n)\,mod\,\left(K_{path}\right)$ is fed to the K-path integrator as $v_3[n]$. The delay of $\frac{K_{path}}{2}$ samples in the input is due to the fact that the input is sampled $T_s/2$ time earlier (on phase ϕ_{1-1} for path 0) than when it's transferred to the integrator on the phase ϕ_{2-1} for the corresponding path 0. Let $V_3(f)$ be the Fourier transform of the signal $v_3[n]$. From the Equation 2.2, we obtain the relation for the equivalent feedback quantization noise, $V_{fb}(f)$, resulting due to path mismatches being given by

$$V_{fb}(f) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} \left[\sum_{m=0}^{K_{path}-1} e^{-j2\pi\left(f-\frac{k}{T_s}\right)\frac{rmT_s}{K_{path}}} e^{-j2\pi\frac{km}{K_{path}}} \right] V_3\left(f - \frac{k}{T_s}\right) \tag{4.47}$$

Note that the notation has changed from Section 2.1 to accommodate the KD1S topology convention by substituting $M = K_{path}$, $T = \frac{T_s}{K_{path}} = T_{s,new}$ in Equation 4.47. Equation 4.47 can be re-written as

$$V_{fb}(f) = \frac{1}{T_{s,new}} \sum_{k=-\infty}^{\infty} A(k) V_3 \left(f - \frac{k}{T_s} \right) \tag{4.48}$$

where the distortion terms are given by

$$A(k) = \frac{1}{K_{path}} \sum_{m=0}^{K_{path}-1} \left(a_m e^{-j2\pi\rho(f)} \right) e^{-j2\pi \frac{km}{K_{path}}} \tag{4.49}$$

Here, the exponent $\rho(f) = \frac{r_m f}{f_{s,new}}$, denotes the error contribution due to the phase-skew ($r_m = T_{skew} \cdot f_{s,new}$) for a signal tone at frequency f. From Equation 4.48 we can observe that the feedback signal, $V_3(f)$ is frequency translated from a frequency $\frac{k}{T_s}$, $k = 1, .., \left(K_{path} - 1\right)$ to the baseband with a multiplier given by $A(k)$.

Now, we try to obtain a representation of the folded noise in the z-domain. Since it's analytically unwieldy to handle continuous dependence of phase-error skew on continuous frequency, we will limit our attention to the signal frequencies which directly get amplitude modulated into the baseband (they are, $f_m = m \cdot f_s$, $m = 1, 2, ..., \left(K_{path} - 1\right)$). Also, an additional path-gain term $a_m = \frac{C_{I,m}}{C_0}$ has been included in Equation 4.49 to model the gain error due to capacitor mismatches, as in Section 2.2.2. Here, C_0 is the mean capacitance of the K-deltas sampling capacitors $C_{I,m}$ and $C_{I,m} = C_0(1 + \delta_m)$,

where δ_m is the equivalent capacitance mismatch for the m^{th} path. We now have

$$\begin{aligned} A(k) &\approx \frac{1}{K_{path}} \sum_{m=0}^{K_{path}-1} \frac{C_{I,m}}{C_0} e^{-j2\pi\rho(mf_s)} e^{-j2\pi\frac{m\cdot k}{K_{path}}} \\ &= \frac{1}{K_{path}} \sum_{m=0}^{K_{path}-1} \frac{C_{I,m}}{C_0} e^{-j2\pi\rho(mf_s)} \left(e^{-j\frac{2\pi m}{K_{path}}}\right)^k \\ &= \frac{1}{K_{path}} \sum_{m=0}^{K_{path}-1} b_m \left(e^{-j\frac{2\pi m}{K_{path}}}\right)^k \end{aligned} \tag{4.50}$$

where $b_m = \frac{C_{I,m}}{C_0} e^{-j2\pi\rho(mf_s)}$, $m = 1,2,...,(K_{path}-1)$ is the equivalent gain for m^{th} path due to capacitor mismatch and phase-skew combined together. Note that, $A(k)$ are the K_{path}-point DFT on the equivalent path gains b_m. Realizing that $V_3(f - \frac{k}{T_s})$ is equivalent to $V_3(ze^{j\frac{2\pi k}{K_{path}}})$ in z-domain, we can re-write Equation 4.48 as

$$\begin{aligned} V_{fb}(z) &= \sum_{k=0}^{K_{path}-1} A(k) V_3(ze^{j\frac{2\pi k}{K_{path}}}) \\ &= V_3(z) + \sum_{k=1}^{K_{path}-1} A(k) V_3(ze^{j\frac{2\pi k}{K_{path}}}) \end{aligned} \tag{4.51}$$

Thus the quantization noise folded back to the baseband is estimated as

$$\begin{aligned} V_{eq}(z) &= V_{fb}(z) - V_3(z) \\ &= A(1)V_3\left(e^{j\frac{2\pi}{K_{path}}}z\right) + A(2)V_3\left(e^{j\frac{4\pi}{K_{path}}}z\right) + \cdots \\ \cdots &+ A\left(K_{path}-1\right)V_3\left(e^{j\frac{2\pi(K_{path}-1)}{K_{path}}}z\right) \end{aligned} \tag{4.52}$$

and the KD1S modulator's output is given by

$$\begin{aligned} Y(z) &\approx STF(z)V_{in}(z) + NTF(z)Q_e(z) + \cdots \\ &+ \sum_{k=1}^{K_{path}-1} A(k)\cdot z^{-1} STF(z)\cdot NTF(e^{j\frac{2\pi k}{K_{path}}}z)\cdot Q_e(e^{j\frac{2\pi k}{K_{path}}}z) \end{aligned} \tag{4.53}$$

Thus, we obtain superposed folding of shaped quantization noise from frequencies $mf_s = \frac{m}{K_{path}} f_{s,new}$ (i.e. $z = e^{-j\frac{2\pi m}{K_{path}}}$) to the baseband (i.e. $f = 0$ or $z = 1$). Also, we can use the transformation $z \rightarrow e^{j\frac{2\pi m}{K_{path}}} z$ on $V_3(z)$ and then scale it by $A(k)$ (i.e. the K_{path}-point DFT of δ_m) to obtain the noise component folding from the frequency kf_s. Since it is untenable to derive a closed form expression for the resulting SNDR with noise-folding given by Equation 4.53, however this equation is useful in Matlab simulations to estimate the noise-floor level and the resulting SNDR and resolution obtained. Note that, due to charge-sharing between $K_{path}/2$ input capacitors, the variance of the capacitor mismatch term δ_m is given by $\frac{\sigma_{cm}}{\sqrt{K_{path}/2}}$. Figure 4.20 illustrates the multiple noise-folding in a KD1S modulator due to gain mismatch and phase-skew. The thickness of the lines showing the coupling in the figure signify the relative amount of noise coupled into the signal-band. Here, the maximum noise contribution in the signal-band is from the modulation noise peak at $K_{path} f_s/2$ and the multiplier is given by $A\left(\frac{K_{path}}{2}\right) = A_4$. Also, we have the noise-folding co-efficients given by $A(K_{path} - k) = A^*(k)$.

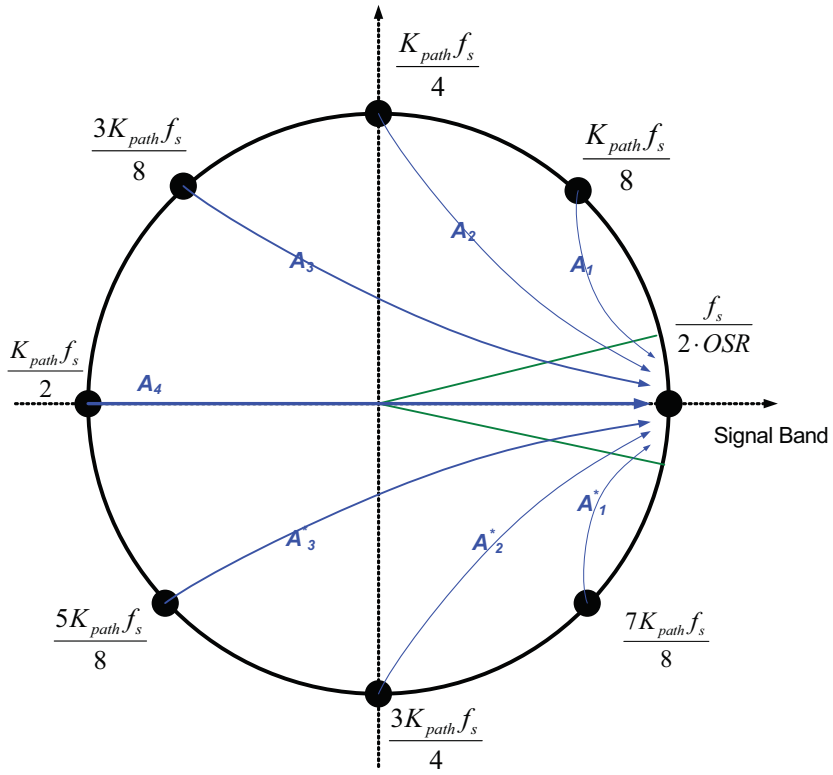

Figure 4.20: Graphical illustration of noise folding, in a KD1S modulator with path mismatches, on a z-plane. Here $K_{path} = 8$.

Also, it can be observed that oversampling or sharing the integrator across the K-paths doesn't attenuate the folded-back noise. The raised noise-floor due to the folded noise ultimately limits the resolution attainable by a KD1S topology in presence of capacitance mismatches and phase-skew errors. Thus, special care must be taken to minimize phase-skew in clock routing and clock-phase generation circuit.

4.4.6 Clock Jitter

The error introduced due to the clock jitter in the switched-capacitor configuration has two components:

1. The Input Sampling Jitter

Assuming that the clock jitter is white noise, i.e. the jitter noise is spread uniformly from 0 to $f_{s,new}/2$. The effect of the clock-skew, which will cause the mean of the individual clock jitter to be non-zero, has already been considered. Thus we can safely assume that the clock jitter in each of the clock phases is a zero mean Gaussian random variable in time. Also, it is assumed that the jitter-noise of all the K-clock phases are uncorrelated with each other. The white jitter noise is filtered by the decimation filter and its variance is reduced by the effective oversampling ratio i.e. $K_{path} \cdot OSR$. The SNR limitation on the K-path sampling due to clock jitter is given by

$$SNR_{jn} = 20 \cdot log\left(\frac{K_{path} \cdot OSR}{2\pi f_{in}\sigma_{jt}}\right) \tag{4.54}$$

where σ_{jt} is the standard deviation of the clock jitter noise. Figure 4.21 illustrates the increase in the effective number of bits (ENOB) with the increasing effective oversampling ratio ($K_{path} \cdot OSR$) for an rms jitter of $\sigma_{jt} = 1\,ps$. As the input frequency increases, the ENOB is decreased due to increased aperture error due to jitter. But when oversampling is employed the out-of-band jitter noise is filtered out and hence the effective resolution increases.

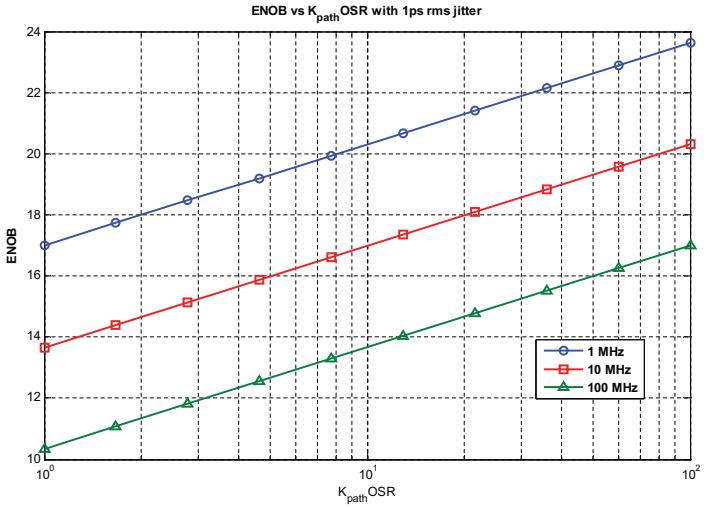

Figure 4.21: ENOB vs the effective oversampling ratio for a K-path sampling scheme with 1 ps rms clock jitter. The plots are for input frequencies (f_{in}) of 1 MHz, 10 MHz and 100 MHz. The effective sampling frequency for each of the plots is $f_{s,new} = 2K_{path} \cdot OSR \cdot f_{in}$.

However, if the clock jitter has $1/f$ characteristic, the jitter-noise will have a spectrum that appear as "skirts" on the spectral line of the fundamental and the distortion tones due to the clock jitter. In this case, oversampling will not effectively attenuate the colored jitter noise spectrum. Thus the spectral purity of the clock-phase source is an important consideration especially when the clock phases are generated using a VCO (voltage controlled oscillator) [51].

2. The reconstruction of the output-signal

In the switched-capacitor KD1S implementation, the charging/discharging time of the switched-capacitor is very small due to complete settling of the switched-capacitor DAC. Due to the exponential settling, the amount of feedback charge Δq_d lost due to the timing error is relatively small. It is assumed that the settling time-constant of

the DAC, $R_{DAC}C_{DAC}$, is much smaller than T_s/K_{path} . Thus the in-band noise (IBN) noise added due to the DAC pulse modulation due to clock jitter is negligible. Here, the KD1S modulator score over the CT-DSM, where the DAC pulse shape modulation is detrimental to the modulator performance. We can conclude that the jitter noise in the KD1S modulator is independent of the topology or the order of the modulator [51].

4.5 Noise Effects in a KD1S Modulator

A detailed treatment of thermal noise analysis for discrete-time delta-sigma modulators has been provided in [23, 52]. In this section we list important results from [52] and apply them to the noise analysis of the KD1S modulator.

The power spectral densities (PSD) of the thermal noise voltage and current for a resistor are given by

$$\begin{aligned} S_v(f) &= 4kTR\,(V^2/Hz) \\ S_i(f) &= \frac{4kT}{R}\,(A^2/Hz) \end{aligned} \tag{4.55}$$

where $k = 1.38 \times 10^{-23} J/K$ is the Boltzmann's constant, T is the absolute temperature of the resistor in Kelvin, and R is the resistor's value. The thermal noise voltage is white and thus its PSD $S_v(f)$ has a flat spectrum up to terahertz of frequencies. Thus the root-mean-square (rms) of the thermal noise voltage (v_n) delivered by a resistor over a bandwidth Δf is given by [46]

$$v_n = \sqrt{4kTR\Delta f}\,(V) \tag{4.56}$$

A transistor (MOSFET) operating as a switch (in triode) has its thermal noise power spectral density (PSD) given by [52]

$$S_{vt} = 4kTR_{on}\ (V^2/Hz) \tag{4.57}$$

where R_{on} is the on-resistance of the transistor. For a transistor biased in saturation, the noise-current PSD is given by [52]

$$S_{it}(f) = 4kT\alpha g_m = \frac{8}{3}kTg_m\ (A^2/Hz) \tag{4.58}$$

Here, g_m is the transconductance of the transistor and α is a factor for the MOSFETs and is roughly equal to $2/3$. The Flicker noise or the $1/f$ noise which arises due to the random motion, in the channel along the silicon and the oxide interface, by jumping across the trap states. The PSD of the flicker noise is given by [46]

$$S_{vf}(f) = \frac{K_{1/f}}{WLf}\ (V^2/Hz) \tag{4.59}$$

where W and L are the width and length of the transistor, $K_{1/f}$ is a constant depending upon the CMOS process. The flicker noise has a low-pass frequency characteristics and thus concentrating the noise power at low frequencies or narrow bandwidths. The flicker noise can be usually reduced by employing larger devices and by using PMOS transistors for amplification instead of NMOS . However, as we approach smaller nano-CMOS process the distinction between the flicker noise of PMOS and NMOS is dominishing [23, 53].

Sampled Thermal Noise

When a thermal noise voltage v_n with a PSD $S_v(f)$ is passed through a first-order filter, with a response given by

$$H(s) = \frac{G_0}{1+s\tau} \tag{4.60}$$

the resulting noise voltage has a mean-squared value given as [52]

$$\overline{v_{no}^2} = \frac{G_0^2 S_v}{4\tau} \tag{4.61}$$

Here, G_0 is the equivalent DC gain of the filtering stage and $\tau = 1/(2\pi f_{3dB})$ is its the time constant. Now the thermal noise voltage v_n is passed through the low-pass filter $H(s)$ and its output is sampled on a capacitor C with a sampling frequency f_s resulting in a noise voltage v_{nos}. Due to sampling, the PSD of the noise processed by $H(s)$ is folded back into the baseband due to aliasing and due to this repeated folding the PSD of v_{nos} is nearly white. Since the mean-squared (MS) value of the sampled noise $v_{nos}(t)$ is essentially same as the and is expressed as that of $v_n(t)$, the PSD of the sampled noise is expressed as [52]

$$S_{nos}(f) = \frac{\overline{v_{no}^2}}{f_s/2} = \frac{G_0^2 S_v}{2\tau f_s} \tag{4.62}$$

Thus, the PSD of the sampled noise is raised, due to folding, by a factor of $\frac{1}{2\tau f_s}$, which is larger than $(N+1)\ln 2$ for N-bit resolution. This value is 8.8 dB for $N = 10$ bits resolution. Using the result seen in Equation 4.62, the MS value of the thermal noise sampled by a sample-and-hold stage, implemented with a first-order op-amp with total

load C_0 and feedback gain β, is given by [23, 52]

$$\overline{v_{out}^2} = \frac{4kT}{3C_0} \tag{4.63}$$

K-path SC Integrator Noise Analysis

In a K-path switched-capacitor integrator, thermal noise is introduced due to the finite resistance of the switches and from the op-amp. Figure 4.22 shows the equivalent schematics for analyzing the effects of thermal noise in a K-SCI. Here, the input $v_{in} = 0$ is assumed to simplify the analysis. For the first path, during the phase ϕ_{1-1}, The thermal noise due to the conductive switches S_1 and S_3 is sampled onto the associated sampling capacitor C_I. In the Figure 4.22(a), the conducting switches S_1 and S_3 have been replaced by their equivalent noise sources $v_{n1}$and v_{n3} and their on resistances R_{on1} and R_{on3} respectively. In Figure 4.22(b), the noise sources have been replaced by a single equivalent noise source v_n (as v_{n1} and v_{n3} are uncorrelated noise sources) and the resistances have been combined into $2R_{on}$ equivalent resistance. The PSD of the noise voltage source v_n is given by $4kT(2R_{on}) = 8kTR_{on}$. Thus, the PSD of the noise voltage across the capacitor C_I is given by

$$S_{C_I}(f) = \frac{8kTR_{on}}{1 + (2\pi f\tau_0)^2} \tag{4.64}$$

where $\tau_0 = 2R_{on}C_I$ is the time-constant associated during the sampling phase. The MS value of the total thermal noise sampled on C_I during the sampling phase is calculated

as

$$\overline{v_{C_I,1}^2} = \int_0^\infty S_{C_I}(f)df = \int_0^\infty \frac{8kTR_{on}df}{1+(2\pi f\tau_0)^2} = \frac{kT}{C_I} \tag{4.65}$$

and this is independent of R_{on}. This is the classical result of the kT/C noise when the white thermal noise due to a resistance is band-limited by a capacitor [46]. This kT/C_I MS noise is held in each of the C_I's after their individual sampling phases are completed.

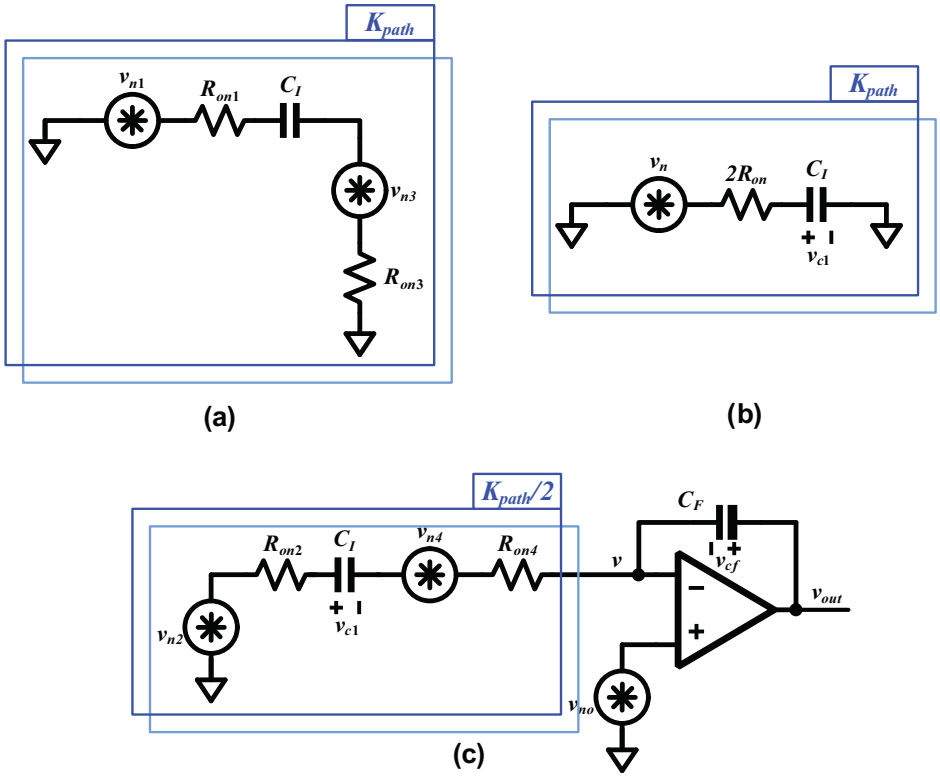

Figure 4.22: Noise analysis for the K-path integrator: **(a)** Equivalent noise during the sampling phase for each of the capacitors. **(b)** Equivalent noise schematic for (a). **(c)** Equivalent noise schematic during the integration phase.

During the integration phase (i.e. phase ϕ_{2-1} for the first path, ϕ_{2-2} for the second path and so on), $K_{path}/2$ sampling capacitors are connected to the integrator and contribute to the thermal noise sampled on each of the C_I's during this phase. During this phase, the switches S_2 and S_4 are closed and the switches S_1 and S_3 are open. The sum of the sampled thermal noise on each of the C_I's and the noise contribution from the op-amp is eventually transferred to the integration capacitor C_F. The resulting noise circuit is seen in Figure 4.22(c). In this case, besides the noise from switch resistances R_{on2} and R_{on4}, the op-amp also contributes its input referred thermal noise (v_{no}). As seen in the Section 4.2, the dynamics of the K-SCI during the integration phase are complicated due to the partial settling for each path in the first time-slice of T_s/K_{path} and the spread-out of the settling across the $T_s/2$ time interval (e.g. when ϕ_{2-1} is high for the first path). In order to simplify the analysis of noise during the integration phase, initially a single pole model for the op-amp is assumed as shown in Figure 4.23. It is further assumed that the loop-gain of this op-amp is large i.e. $\beta g_{m1} R_L \gg 1$ and the output load resistance $R_L \to \infty$. Here, the feedback factor $\beta = \frac{C_F}{(K_{path}/2)C_I + C_F}$. Later, we will introduce the effects of the frequency response of the K-path integrator in our noise analysis.

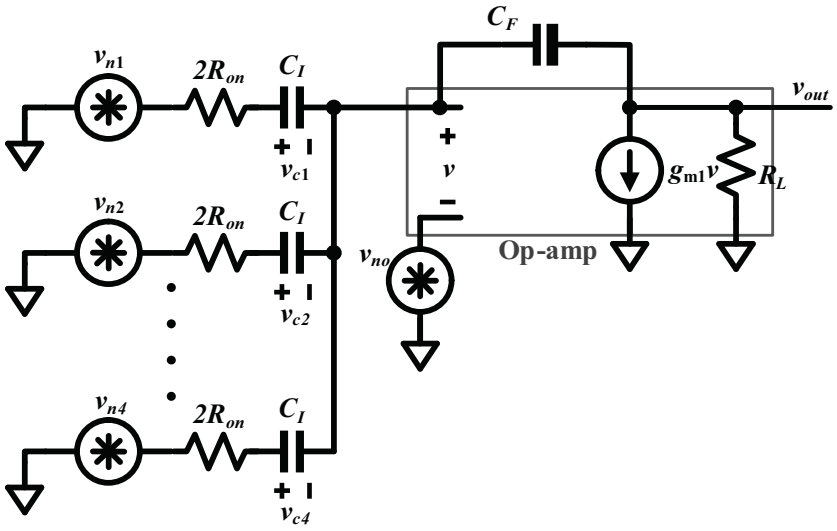

Figure 4.23: Equivalent noise schematic during the integration phase with a single-stage op-amp, during the integration phase ϕ_{2-1}.

Applying nodal analysis on Figure 4.23 in the Laplace domain, we get the noise voltage across C_I in each of the paths as

$$V_{C_I}(s) = \frac{\left(\frac{1}{K_{path}/2}\sum_{k=1}^{K_{path}/2} V_{nk}(s)\right) - V_{no}(s)}{(1+s\tau_1)} \tag{4.66}$$

where

$$\tau_1 = \left(2R_{on} + \frac{K_{path}}{2g_m}\right) C_I \tag{4.67}$$

is the time-constant associated with the integration phase, $\mathscr{L}(v_{nk}(t)) = V_{nk}(s)$ are the individual equivalent noise sources of each of the paths connected to the op-amp in Figure 4.23 . It can be observed that the thermal noise voltages for each of the uncorrelated sources are averaged across the $K_{path}/2$ paths and are sampled onto each of the capacitors C_I. The MS of the noise voltage (or the noise power) across C_I due to the switches

is estimated as

$$\begin{aligned}\overline{v_{c_I,sw}^2} &= \frac{S_n(0)}{4\tau_1} = \frac{\frac{8kTR_{on}}{K_{path}/2}}{4\left(2R_{on}+\left(K_{path}/2g_m\right)\right)C_I} \\ &= \frac{kT}{C_I}\cdot\left(\frac{1}{K_{path}/2}\right)\cdot\frac{1}{1+1/x}\end{aligned} \tag{4.68}$$

Here a paramater $x = \frac{2R_{on}g_{m1}}{K_{path}/2} = \frac{4g_{m1}R_{on}}{K_{path}}$ has been employed. Note that the thermal noise for each of the paths have been averaged with a resulting MS value of

$$var\left(\frac{1}{K_{path}/2}\sum_{k=1}^{K_{path}/2} v_{nk}\right) = \frac{8kTR_{on}}{K_{path}/2} \tag{4.69}$$

The contribution from the op-amp's thermal noise to the noise power in C_I is given by [52]

$$\begin{aligned}\overline{v_{c_I,op}^2} &= \frac{S_{no}}{4\tau_1} = \frac{(16/3)\,kT/g_{m1}}{4\left(2R_{on}+\left(K_{path}/2g_m\right)\right)C_I} \\ &= \left(\frac{4}{3}\right)\cdot\frac{kT}{C_I}\cdot\frac{1}{1+x}\end{aligned} \tag{4.70}$$

Now, at the end of the integration phase, the total noise voltage stored on a single C_I is given by the $v_{c_I,sw} + v_{c_I,op} - v_{c_{I,1}}$. As these three noise terms $v_{c_{I,1}}$, $v_{c_I,sw}$ and $v_{c_I,op}$ and are uncorrelated, the total thermal noise power is given as

$$\begin{aligned}\overline{v_{c_I}^2} &= \frac{kT}{C_I}\cdot\left(\frac{1}{K_{path}/2}\right)+\frac{kT}{C_I}\cdot\left(\frac{1}{K_{path}/2}\right)\cdot\frac{1}{1+1/x}+\left(\frac{4}{3}\right)\cdot\frac{kT}{C_I}\cdot\frac{1}{1+x} \\ &= \frac{kT}{\left(K_{path}/2\right)C_I}\left(1+\frac{x}{1+x}+\frac{K_{path}}{2}\cdot\frac{4/3}{1+x}\right) \\ &= \frac{kT}{\left(K_{path}/2\right)C_I}\left(\frac{2x+\frac{2K_{path}+1}{3}}{1+x}\right) = \frac{2kT}{\left(K_{path}/2\right)C_I}\left(1+\frac{\frac{K_{path}-3/2}{3}}{1+x}\right)\end{aligned} \tag{4.71}$$

Note that the first term in the Equation 4.71 divided by $\frac{K_{path}}{2}$ due to the averaging of these noise voltage sources across the $\frac{K_{path}}{2}$ paths connected to the op-amp. Thus

in a K-path integrator the thermal noise of the capacitors is averaged and is equivalent to the noise contribution by an equivalent capacitance of $\frac{K_{path}}{2}C_I$. From Equation 4.71 the ratio of the noise contribution, during the integration phase, from the switch to that of the op-amp is $\frac{3x}{2K_{path}}$. Thus for $x \gg 1$ (or $g_{m1} \gg \frac{1}{R_{on}}$), the noise due to the switches dominates and for the case $x \ll 1$ (i.e. $g_{m1} \ll \frac{1}{R_{on}}$), the op-amp noise dominates. For $x \gg 1$, the total noise is minimized and is simply equal to $\frac{2kT}{(K_{path}/2)C_I}$. However, this condition entails a large current in the op-amp stage and thus large power consumption [52].

An optimal solution for the thermal noise is when the g_{m1} is constrained minimized for a given size of capacitance C_I and the settling time τ_1. From the Equations 4.67 and 4.71, we get the optimal value for g_{m1} given by

$$g_{m1} = \frac{kT}{\tau_1 \overline{v_{c_I}^2}} \left(\frac{\frac{2K_{path}+1}{3} + 2x}{1+x} \right) \tag{4.72}$$

Now, during the integration phase, $\frac{K_{path}}{2}$ capacitors (C_I's) are connected to the virtual ground of the op-amp, and is in series with the integration capacitor C_F. Then C_F acquires the same noise charge as the $\frac{K_{path}}{2} \times C_I$ capacitors (q_{c_I}) and the MS noise on C_F is increased by

$$\overline{(\Delta v_{c_F})^2} = \frac{q_{c_I}}{C_F^2} = \frac{kT\left(K_{path}/2\right)C_I}{C_F^2} \left(\frac{\frac{2K_{path}+1}{3} + 2x}{1+x} \right) \tag{4.73}$$

on every time-slice of T_s/K_{path}. Thus we can conclude that in a K-path integrator, the KT/C noise is governed by the capacitance $\frac{K_{path}}{2} \cdot C_I$ and thus allowing lower values of C_I to be used for a given thermal noise budget. Thus for $K_{path} = 8$, the rms noise

$C_I = 100\,fF$ is equal to the noise contributed by a $400\,fF$ sampling capacitor in a single-path DSM.

The output referred noise PSD for the K-SCI is given by [52]

$$S_{vo} = S_{vin} \cdot |H_1|^2 + S_{vout} \tag{4.74}$$

In the Equation 4.74, the power of the input referred source $v_{n,in}$ is given by Equation 4.71 and the power of the output noise source $v_{n,out}$ is given by the equation 4.63. Here, the PSDs are estimated as $S_{vin} = \frac{\overline{v_{n,in}^2}}{f_{s,new}/2}$ and $S_{vout} = \frac{\overline{v_{n,out}^2}}{f_{s,new}/2}$. The transfer function of the K-path integrator can be modeled as

$$H_1(z) = \frac{G_I z^{-1}}{1 + \mu\,(1+G_I) - (1+\mu)z^{-1}} \cdot \frac{1-\alpha_0}{1-\gamma_0 z^{-1}} \tag{4.75}$$

where $G_I = C_I/C_F$ is the equivalent K-SCI gain factor, μ=$\frac{1}{A_{OL}}$, and α_0 and γ_0 are as defined in Section 4.2. The output referred noise power is calculated by numerically integrating the output PSD S_{vo} in the signal band of interest, i.e. for $f \in [0, f_B]$, $f_B = \frac{f_{s,new}}{K_{path} \cdot OSR}$ [52].

KD1S Modulator Noise Analysis

Figure 4.24 shows an equivalent model of a KD1S modulator with the noise sources. Here, $H_1(z)$ represents the K-path integrator, and v_{in1} and v_{no1} are the input and output noises associated with the K-SCI. Generally in a DSM design, 75% of the noise power is allocated for the thermal noise and the quantizer resolution is chosen such that quantization noise is a small constituent of the total noise power . For example, 5% budget for the quantization noise out of the total noise is a good design number [52, 23]. For the

first-order KD1S topology, the dominant noise source is the K-SCI. The input referred noise of the quantizers is accommodated in the quantization noise budget itself.

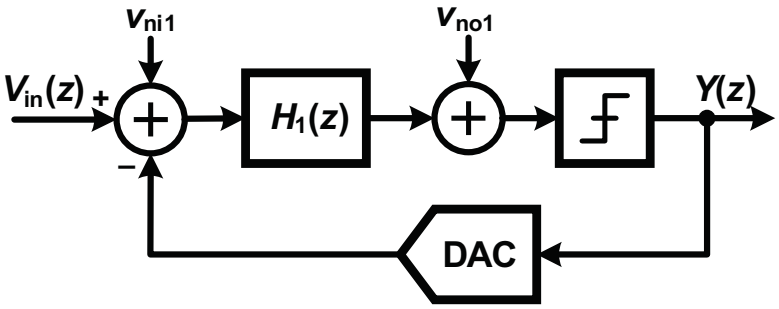

Figure 4.24: Noise sources in a first-order KD1S modulator.

Since, the signal transfer function (STF) for the modulator is roughly equal to unity in the signal-band, the output thermal noise of the first-order KD1S modulator is estimated by integrating S_{vo} in the Equation 4.74 over the signal band from $f = 0$ to f_B. For higher-order KD1S topologies, the thermal noise analysis is same as detailed in [52] with the integrator noise terms substituted by the results obtained in this section.

Capacitor Sizing

We can use the result from Equation 4.71 to do a quick estimate for the size of the input sampling capacitor required in a KD1S modulator. Assuming that the noise contribution from the op-amp is negligible, then we have the input referred thermal noise of the KD1S modulator given by

$$v_n^2 = \frac{2kT}{\left(K_{path}/2\right) C_I} \tag{4.76}$$

Since, this noise is spread over the spectrum from $f = 0$ to $f_s/2$, the noise power in the signal band is

$$v_{n1}^2 = \frac{v_n^2}{OSR} \tag{4.77}$$

Also, we have the requirement for a given SNR that

$$v_{n1}^2 < 10^{\left(-\frac{SNR}{10}\right)} \cdot A^2 \tag{4.78}$$

where $A \leq V_{DD}/2$ is the maximum amplitude of a sinusoidal signal and V_{DD} is the supply voltage. Thus if the thermal noise is dominated by the first integrator in a KD1S modulator, the input sampling capacitor C_I is limited by

$$C_I > \frac{2kT}{\left(\frac{K_{path}}{2}\right) \cdot OSR \cdot v_n^2} = \frac{4kT}{10^{\left(-\frac{SNR}{10}\right)} \cdot A^2 \cdot OSR \cdot K_{path}} \tag{4.79}$$

and the maximum SNR for a given value of C_I is

$$SNR < 10 \cdot \log_{10}\left(\frac{A^2 \cdot K_{path} \cdot OSR}{4kT/C_I}\right) \tag{4.80}$$

From the above equation, with a input sampling capacitances of $C_I = 100\,fF$ and $V_{DD} = 5\,V$ we can achieve an SNR of 67 dB or 10.8 bits in resolution. Thus, the thermal noise requirements in a first-order KD1S modulator are set by the equivalent capacitance $\frac{K_{path}}{2}C_I$ and a lower value for $C_I = 100\,fF$ can be used to achieve a moderate SNR.

4.6 Conclusion

The first-order KD1S modulator disclosed in [12] has been analyzed by incorporating all possible circuit level impairments. Step-by-step simulation results are presented by

gradually introducing the effects of op-amp gain, unity-gain frequency and slew-rate limitations and the effects finite comparator delay. The effects of quantization noise folding due to capacitance mismatch and clock phase skew in the *K*- sampling paths are analyzed. Finally, a detailed noise analysis of the KD1S modulator was presented along with the trade-offs involved in the sampling capacitor sizing.

CHAPTER 5 A SECOND-ORDER KD1S MODULATOR TOPOLOGY

In the last chapter, a first-order KD1S modulator topology was described and the effects of the circuit non-idealities were discussed. In this chapter, a second-order noise shaping KD1S topology is introduced. The circuit non-idealities for the second-order KD1S follow the discussions presented for the first-order modulator. However, specific discussion on the non-idealities which are pertinent to the second-order topology are provided.

5.1 A Second-Order KD1S Modulator

The first-order KD1S modulator, discussed in Chapter 4, had the advantages of simple design, unconditional stability, and robustness. However, the performance of a first-order modulator is limited by lower resolution for a given oversampling ratio (OSR) and the presence of idle tones [23]. As explained in Section 3.2.2, a second-order noise-shaping topology randomizes the idle tones and spreads their energy over the spectrum. Also due to the second-order noise shaping the in-band quantization noise (IBN) is further reduced and the noise-transfer function (NTF) has ideally a 40 dB/decade slope. The theory developed for the first-order KD1S modulator has been extended to realize a second-order K-path delta-sigma modulator. Figure 5.1 presents a discrete-time second-order KD1S modulator topology. The K-phase clocking and the output summing is the

same as seen in Figure 4.6. Figure 5.2 depicts a concise representation for the second-order KD1S modulator shown in Figure 5.1.

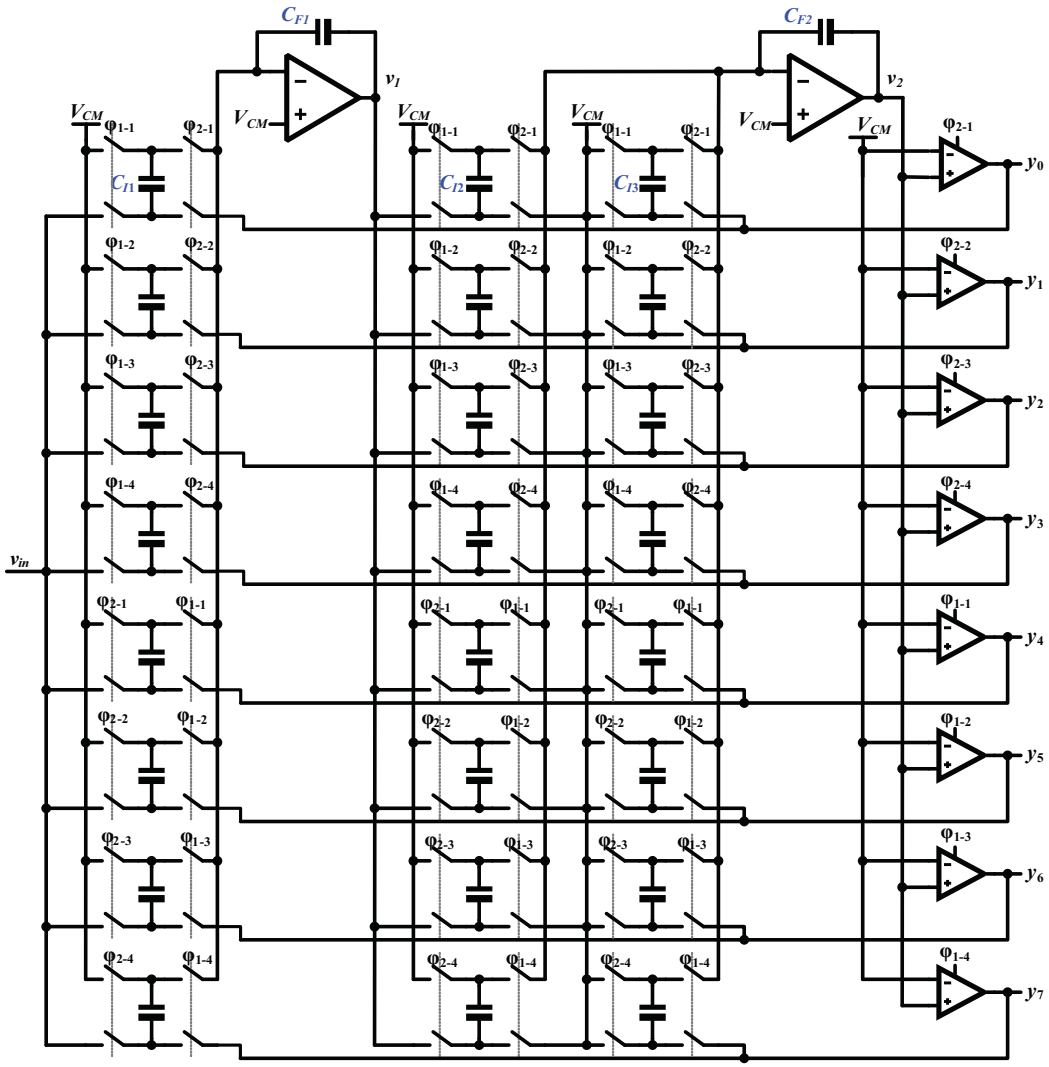

Figure 5.1: A second-order noise-shaping KD1S modulator topology with a singly-ended switched-capacitor implementation.

In Figure 5.1, the first path the first integrator is clocked on the phase ϕ_{2-1} and it partially settles for T_s/K_{path} (or z^{-1} delay) duration. The partially settled output is available by the time the clock phase ϕ_{2-2} goes high. Note that when the phase ϕ_{2-1}

goes high, the voltage at node v_1 (i.e. the output of the first integrator) contains integrated information which was sampled earlier at phase ϕ_{1-4} and is now delayed by z^{-1}. This clocking scheme is not same as the second-order, single-path delta-sigma modulator seen in Figure 3.7 where each of the op-amps fully settled in $T_s/2$ period and thus the first integrator had a non-delaying response. On the other hand in a KD1S modulator, the first integrator continues to settle after the T_s/K_{path} (or z^{-1} delay for partial settling) interval to the $T_s/2$ (or $z^{-K_{path}/2}$ delay) period. Here, the second integrator and the comparator in the first path are clocked on the phase ϕ_{2-1}. In this case, the comparator immediately picks the information presented at the node v_2 (i.e. the output of the second integrator) and starts regenerating upon the initial signal. In the meanwhile the integrator starts to partially settle and updates the information on the node v_2 after a z^{-1} delay. Thus, the comparator always acts upon the information which the second integrator started processing z^{-1} delay earlier. Thus, we can conclude that both the integrators in the topology have a minimum delay of T_s/K_{path}, or z^{-1} with respect to a clock rate of $f_{s,new}$, for the partial settling of each path. This also follows from the Section 4.2 where it was shown that the transfer function of a K-path switched-capacitor integrator is given by $H_1(z) = \frac{C_I}{C_F}\frac{z^{-1}}{1-z^{-1}}W(z)$, which always incurs a delay of z^{-1}. Thus, the second-order delta-sigma topology seen in the Figure 3.6, can not be directly used in a second-order KD1S modulator.

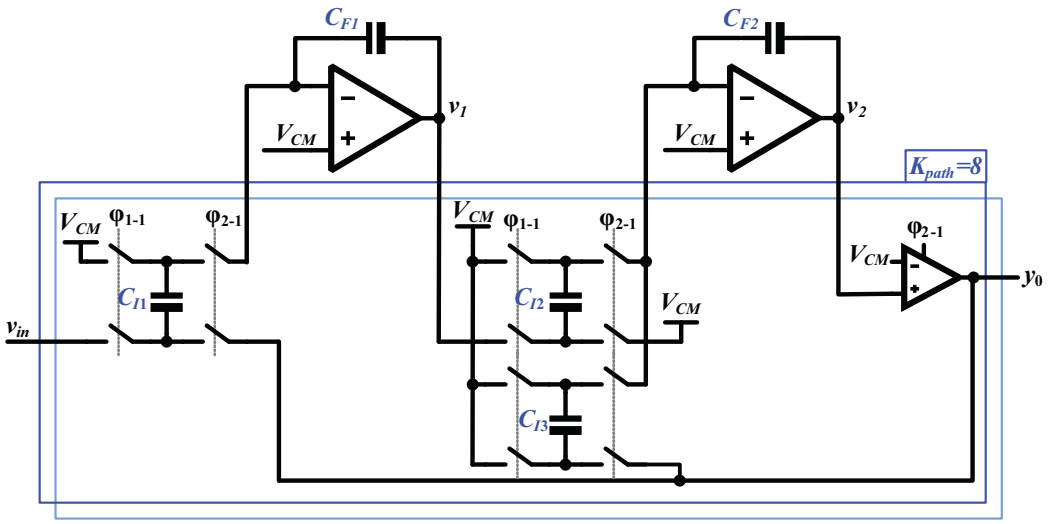

Figure 5.2: A concise schematic representation for the second-order KD1S modulator seen in Figure 5.1.

Due to the two delaying K-path integrators involved, the second-order CIFB (Cascade of Integrators with distributed Feedback) topology is required for realizing the KD1S modulator with second-order noise-shaping [23]. This is illustrated in the block diagram for the second-order KD1S modulator shown in Figure 5.3, where the two K-path integrators are employed each with a partial settling delay of z^{-1}. Also, the block diagram incorporates the charge spreading filters $W_1(z)$ and $W_2(z)$ for both the integrators. Assuming that the integrators in the modulator were ideal and that $W_{1,2}(z) = 1$, then for this topology the noise-transfer function (NTF) is given by [23]

$$NTF(z) = \frac{(1-z^{-1})^2}{D(z)} \tag{5.1}$$

where

$$D(z) = (1-z)^2 + a_2 b_1 z^{-1}(1-z^{-1}) + a_1 a_2 z^{-2} \tag{5.2}$$

For example, in order to realize $NTF(z) = (1 - z^{-1})^2$ and $STF(z) = z^{-2}$, we need to simultaneously satisfy the criterion $a_1 a_2 = 1$ and $a_2 b_1 = 2$. If we select $a_1 = a_2 = 1$, then we require $b_1 = 2$. This can be intuitively understood from the observation that, since the first integrator has introduce an extra delay of z^{-1}, we need to provide larger amount of feedback to the input of the second integrator to compensate for the extra delay across the first integrator. Here, the effective gain of the quantizer is assumed to be unity, but the real quantizer gain should be accommodated later in the modulator transfer functions for precise modeling.

In a practical design, the values of a_1, a_2 and b_1 are range scaled to limit the integrator output swing to the linear region of operation. In the switched-capacitor implementation seen in Figure 5.1, $a_1 = \frac{C_{I1}}{C_{F1}}$ and $a_2 = \frac{C_{I2}}{C_{F2}}$ are the effective gains of the two integrators. The feedback gain to the input of the first integrator is equal to unity. The feedback gain to the input of the second integrator (b_1) is realized by using an additional capacitor C_{I3} such that $b_1 = \frac{C_{I3}}{C_{F2}} \cdot \frac{1}{a_2} = \frac{C_{I3}}{C_{I2}}$. Thus, the capacitor ratio $\frac{C_{I3}}{C_{I2}}$ sets the feedback gain to the input of the second integrator.

The clocking for second-order KD1S, as seen in the Figure 5.1, is critical and follows from the design intuition developed for KD1S noise-shaping flows. The resulting bit-resolution for an ideal second-order KD1S modulator is roughly given by

$$N_{eff} \approx N - 1.85 + 2.5 \cdot log_2(K_{path} \cdot OSR) \tag{5.3}$$

which implies an increase in 2.5 bits per doubling in the number of paths (K_{path}).

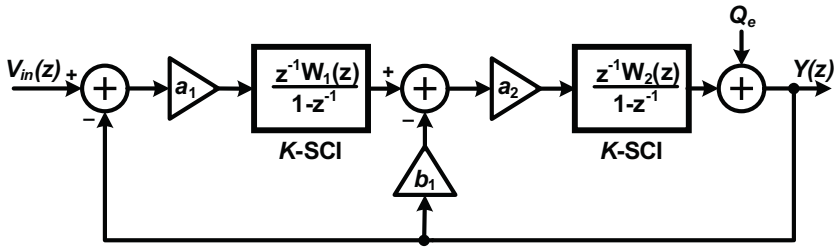

Figure 5.3: Block Diagram for the second-order KD1S modulator seen in Figure 5.1.

5.1.1 Integrator Saturation and Dynamic Range Scaling

After selection of the second-order KD1S topology we need to ensure that the integrator states (v_1 and v_2 in Figure 5.1) are always bounded. This ensures that the loop-filter operates in the linear region so that the op-amps do not saturate and the quantizer is not overloaded. Typically the linear range for the op-amps is within 50%-60% of the full supply range around the common-mode voltage (V_{CM}). If the modulator's loop filter is designed such that the integrator states have an excursion beyond the linear range of the op-amp or even beyond the supply rails, the transistors in the op-amp start trioding and the op-amp's gain drops. This leads to non-linear effects in the modulator which leads to distortion and even instability [23].

Also, if the modulator input is large enough so that the internal states (i.e. the integrator outputs) increase monotonically without being bounded, the loop will become unstable. This also sets a limit on the maximum input amplitude which can be accommodated by the second-order modulator and is called the *maximum stable amplitude* (MSA). The MSA is less than the full scale range of the feedback DAC at in the front, and it decreases as the order of the modulator is increased. Recalling that the input to

the quantizer is given by [23]

$$V_Q(z) = STF(z)V_{in}(z) + (NTF(z) - 1)\,E_Q(z) \tag{5.4}$$

we observe that the input to the quantizer is the sum of the input amplified by the STF and the filtered quantization noise. Now, when the quantizer input $v_Q[n]$ reaches the edge of the no-overload range of the quantizer, the additional filtered noise can overload the quantizer. This overload will in turn increase the quantization noise $e[n]$ which will in turn push the quantizer into the same direction and thus compounding the quantizer overload. This leads to a positive feedback on the amplitude of $v_Q[n]$ and eventually saturates the active blocks in the modulator. Also during the duration of quantizer overload, the noise shaping doesn't occur as desired, leading to filling up the notch in the NTF in the signal band resulting in a degradation of SNDR. If the modulator doesn't recover from the overload situation, an external reset is required to re-start the modulator [23].

The internal states of the loop-filter are restricted to the linear range by employing algorithmic *dynamic range scaling* available in the Delta-Sigma Toolbox in Matlab [25] and further explained in the Section 6.4.4. In the KD1S designs presented in this chapter, the integrator states are limited to 60% of the supply voltage around the common-mode, i.e., in the voltage range $[V_{CM} - 0.3V_{DD}, V_{CM} + 0.3V_{DD}]$.

5.1.2 Ideal Simulation Results

The second-order KD1S topology seen in the Figures 5.1 and 5.2 was synthesized and then dynamic range scaled using the Delta-Sigma Toolbox [25]. This resulted in the filter coefficients values in Figure 5.3 given by $a_1 = 0.167$, $a_2 = 0.1$, and $b_1 = 0.6$. In this design, the input sampling capacitors in the integrators have been chosen to be $C_{I1} = C_{I2} = 100\,fF$. From Section 4.5, the resulting kT/C noise limits the SNR to 10.8 bits in the 500-nm CMOS process with $V_{DD} = 5\,V$. These **a** and **b** coefficient values, when mapped to the topology in Figure 5.2, result in the capacitor values of $C_{F1} = 600\,fF$, $C_{F2} = 1\,pF$ and $C_{I3} = 60\,fF$. Here, $K_{path} = 8$ paths, each with a clock frequency (f_s) of 100 MHz are employed. The effective sampling rate $f_{s,new}$ is equal to 800 MHz. Ideal op-amps, with no bandwidth limitations and a DC gain of 60 dB, were initially used for the simulations. Also, the comparator (or 1-bit quantizer) was assumed to be ideal with a zero delay.

The behavioral Spectre simulation results for the second-order KD1S topology are shown in Figure 5.4. A sinusoidal input of amplitude of 400 mV and 3 MHz frequency was used in the simulation. The integrator states are confined to the range $[0.3\,V, 0.9\,V]$ by design (here $V_{DD} = 1.2$ V and $V_{CM} = 0.6$ V) . The simulated SQNR (Signal-to-Quantization Noise Ratio) for a signal bandwidth of 6.25 MHz (i.e. $K_{path} \cdot OSR = 64$) is equal to 71.8 dB or 11.63 bits in resolution. Also the spurious tones are reduced, when compared to the first-order KD1S, leading to higher dynamic range (DR). The simulated spurious free dynamic range (SFDR) in the signal band is 60 dB.

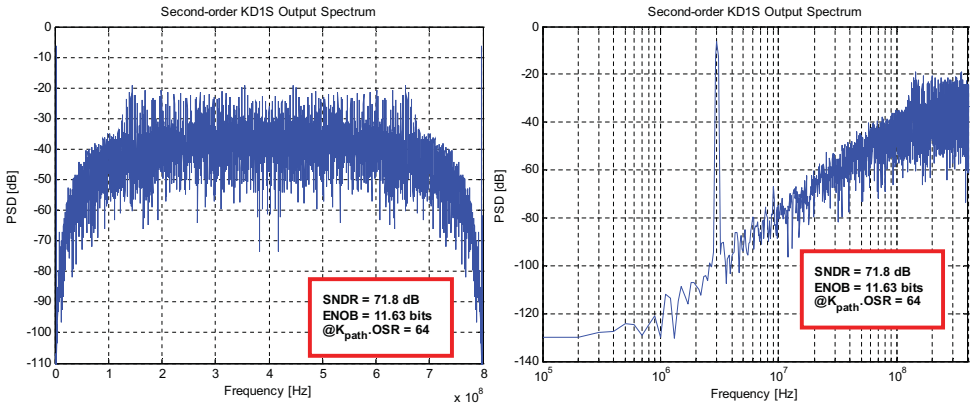

Figure 5.4: Spectre behavioral simulation result for the second-order KD1S modulator with ideal components. Here, $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz, $OSR = 8$, and $BW = 6.25$ MHz. The quantizer and op-amps are ideal.

Figure 5.5 plots the histograms of the integrator states in the above designed second-order KD1S modulator. We can observe that outputs of both the integrators are bounded well within the desired $[0.3V, 0.9V]$ range.

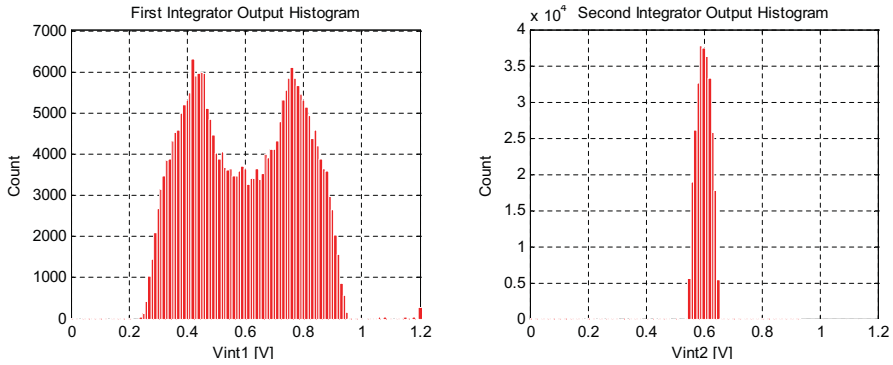

Figure 5.5: Histogram of the integrator states for the second-order KD1S modulator for the response seen in Figure 5.4.

5.2 Effects of the circuit non-idealities

The effects of the circuit non-idealities for the second-order KD1S modulator largely follow the same criterion as described in Section 4.4. Here, we present the analytical and simulation results which are specific to the second-order KD1S topology.

5.2.1 Finite Op-amp Unity-Gain Frequency (f_{un})

Since we employ K-path integrators in the second-order KD1S modulator which have a finite unity-gain frequency (f_{un}). This results in two additional poles in the loop filter response of the modulator. The charge spreading filters, $W_{1,2}(z)$, appear in the signal and noise transfer functions of the modulator which are now given by

$$\begin{aligned} NTF(z) &= \frac{1}{1+k_q b_1 a_2 H(z) W_2(z) + k_q a_1 a_2 H^2(z) W_1(z) W_2(z)} \\ STF(z) &= \frac{k_1 a_1 a_2 H^2(z) W_1(z) W_2(z)}{1+k_q b_1 a_2 H(z) W_2(z) + k_q a_1 a_2 H^2(z) W_1(z) W_2(z)} \end{aligned} \tag{5.5}$$

where $W_{1,2}(z)$ are given by Equation 4.23 as $W_{1,2}(z) = \frac{1-\alpha_0}{1-\gamma_0 z^{-1}}$ where $\alpha_0 = e^{-\pi\beta\frac{f_{un}}{Kf_s}}$ and $\gamma_0 = \left(\frac{K_{path}/2-1}{K_{path}/2}\right)\alpha_0$ for each of the op-amps. Also here, $H(z) = \frac{z^{-1}}{1-z^{-1}}$ is the transfer function for an ideal delaying integrator and k_q is the gain of the quantizer. The NTF and STF for the second-order modulator are illustrated in Figure 5.6. Here, the STF exhibits a low-pass response and is relatively flat in the signal band (0.04 dB droop at 6.25 MHz). The NTF exhibits slight peaking due to the extraneous poles.

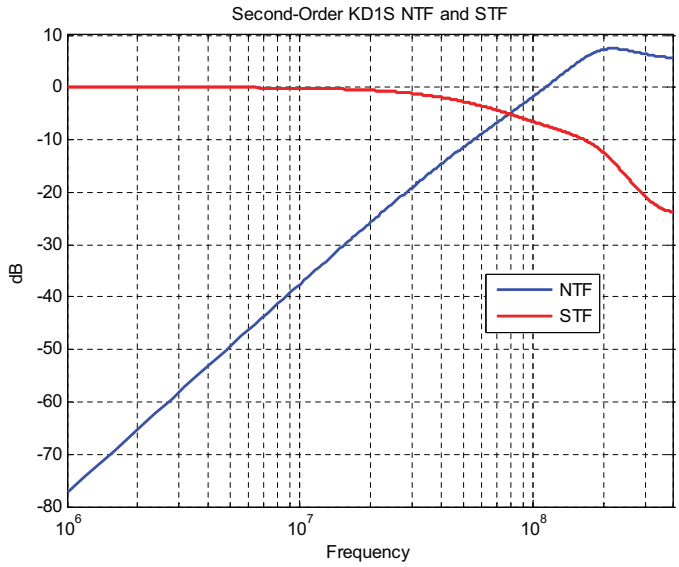

Figure 5.6: NTF and STF for the second-order KD1S modulator with $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz, $f_{un} = \frac{3}{8} f_{s,new} = 300$ MHz, $OSR = 8$, and $T_c = 0$.

The ideal second-order KD1S modulator topology discussed in Section 5.1.2 is now simulated with op-amps having finite unity-gain bandwidth (f_{un}) with other circuit parameters remaining the same. A behavioral model of the op-amp is employed with unity-gain frequency equal to $f_s = \frac{3}{8} f_{s,new} = 300$ MHz and with a DC gain (A_{OL}) equal to 60 dB. Slew rate limitations of the op-amp have not been included in the behavioral model. Again, the comparator is assumed to be ideal with a zero delay. The effects of a practical quantizer modeling is presented later in this chapter. The Spectre simulation results for the second-order KD1S topology are shown in Figure 5.7. Here, due to the presence of extra poles the NTF response is slightly sharper than the +40 dB/dec slope seen in Figure 5.4. The simulated SQNR for a signal bandwidth of 6.25 MHz (i.e. $K_{path} \cdot OSR = 64$) is equal to 71.7 dB or 11.62 bits in resolution, which is almost the

same as the performance seen for the ideal modulator response in Figure 5.4. Figure 5.8 plots the histograms of the integrator states and confirms that the outputs of the both the integrators are still bounded within 60% of the supply range.

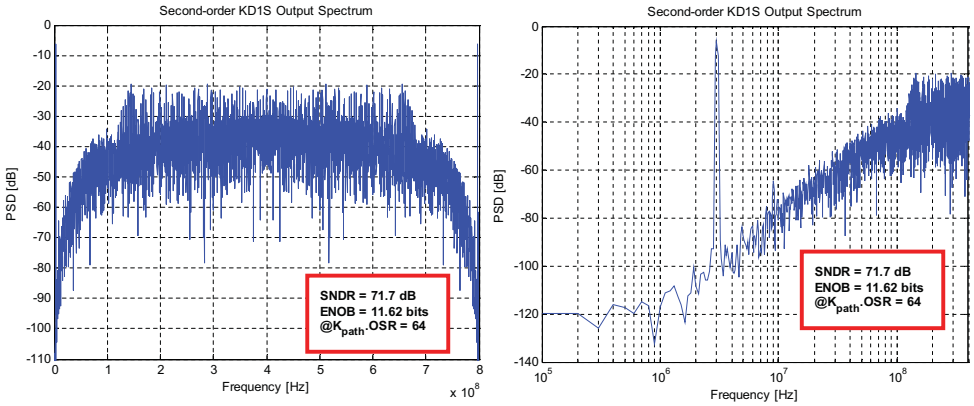

Figure 5.7: Spectre behavioral simulation result for the second-order KD1S modulator with ideal components. Here, $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz, $OSR = 8$, and $BW = 6.25$ MHz. The quantizer is ideal and has zero delay (i.e. $T_c = 0$).

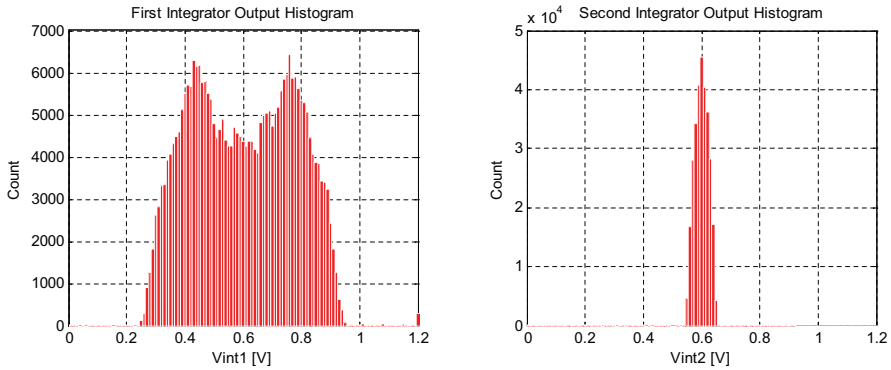

Figure 5.8: Histogram of the integrator states for the second-order KD1S modulator for the response seen in Figure 5.7.

The second-order KD1S modulator with the block diagram seen in Figure 5.3 was also simulated in Matlab using the delta-sigma toolbox by incorporating the model for

the K-path integrator (refer to Section 6.4.3 for details on modeling). The design parameters are the same as used in the above design. The resulting SNDR of 69 dB (11.14 bits in resolution) is in close agreement with the results obtained by the Spectre simulations see in Figure 5.7. Also we can observe the additional two NTF poles due to the charge spreading effects in the K-path integrators modeled by $W(z)$. The maximum stable amplitude from simulations is found to be ($u_{max} = 0.967$) and the effective quantizer gain is $k_q = 2.8$. We will further use this Matlab model to study the stability of the KD1S modulator with circuit non-idealities.

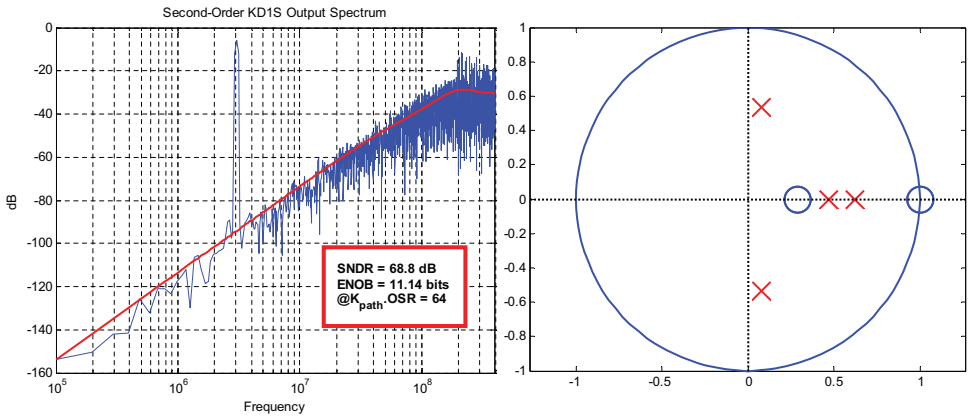

Figure 5.9: Matlab simulated PSD of the output and the NTF pole-zero plot for the second-order KD1S modulator with $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz, $f_{un} = \frac{3}{8} f_{s,new} = 300$ MHz, $OSR = 8$, $BW = 6.25$ MHz, andT_c =0.

Clearly for a single-bit quantizer, the quantizer gain k_q depends upon the input signal to the quantizer and leads to non-linear effects and movement of poles in the modulator response. The effective quantizer gain is obtained through simulations by using the relation $\hat{k_q} = \frac{E[|y|]}{E[y^2]}$. This estimated quantizer gain value is substituted in the NTF and STF expressions. We can observe that the denominator of the NTF and STF in Equation

5.5 is a fourth order polynomial and thus has four poles (see Figure 5.10). The locations of the two extraneous poles, introduced due to the $W_{1,2}(z)$, depend upon the unity-gain frequencies (f_{un}) of the two op-amps employed in the loop filter. As illustrated in Figure 5.10, the poles move inwards (away from the unit circle) and improve the modulator stability as the f_{un} is raised from $3f_s$ to $5f_s$. This introduces a trade-off between the power consumption in the op-amps and the modulator stability. This becomes more critical when we consider the finite delay of the quantizer in our simulation model.

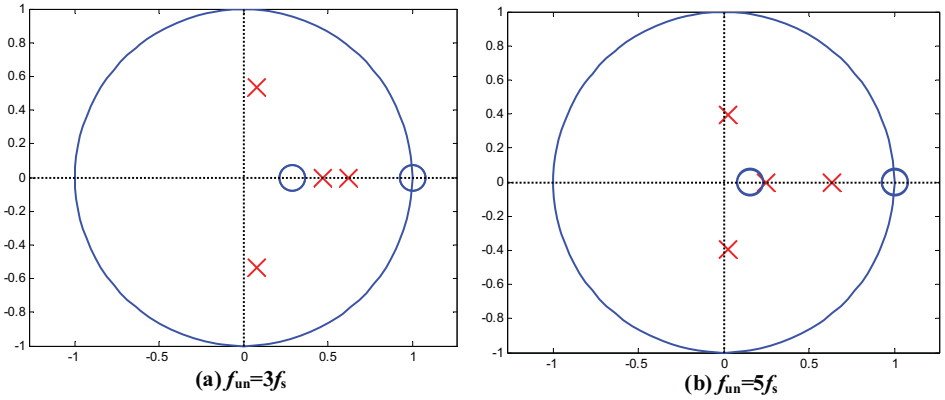

Figure 5.10: Effect of the op-amp f_{un} on the pole location of the NTF and STF for a second-order KD1S modulator.

5.2.2 Finite Op-amp Gain

The effects of the finite open-loop gain of the op-amps (A_{OL}) for a first-order KD1S were covered in Section 4.4.2. The design criterion for the op-amp gain remains the same as $A_{OL} > K_{path} \cdot OSR$ for second-order KD1S modulator. This is illustrated in Figure 5.11 where finite gain of the op-amp employed in the KD1S modulator with $f_{un} = \frac{3}{8} \cdot f_{s,new}$= 300 MHz and $K_{path} \cdot OSR = 64$. Here, the SNDR drops from 68 dB

to 65.8 dB as the A_{OL} is reduced from 50 dB to 25 dB. Also by increasing the op-amp gain beyond $A_{OL} > 20 \cdot log_{10}\left(K_{path} \cdot OSR\right) \approx 40$ dB, the enhancement in the SNDR is less than 0.5 dB. Furthermore, the dead-band behavior in the second-order modulator is severely reduced as the equivalent open-loop gain of the loop-filter is now proportional to A_{OL}^2 [23].

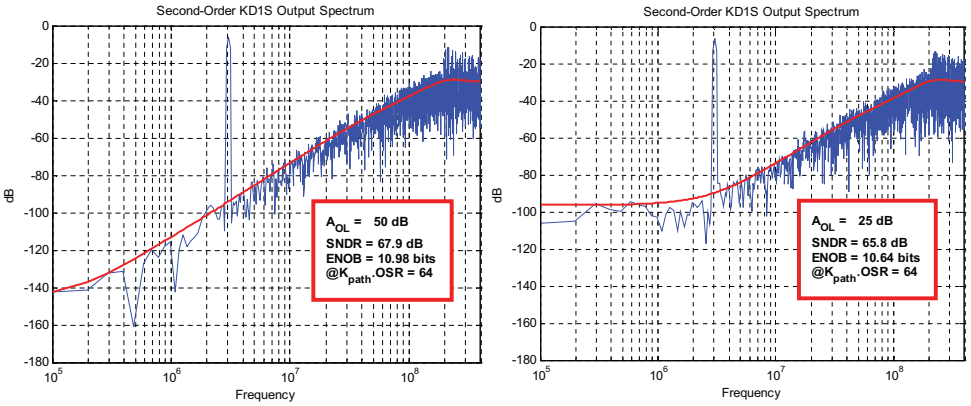

Figure 5.11: Simulated NTFs for the second-order KD1S modulator with the op-amp open-loop gains (A_{OL}) of 50 dB and 25 dB.

The accuracy requirements for the input integrator are high as any error introduced at the input will limit the resulting modulator SNDR. Thus, the op-amp in the first integrator must be carefully designed to avoid slewing as seen in Section 4.4.3.

5.2.3 Real Quantizer Effects

The non-idealities involved in a practical quantizer were discussed in Section 4.4.4. The finite delay, required by the comparator to make a decision on its input, sets the maximum sampling rate achievable by a KD1S modulator. This comparator delay is variable and depends upon the input signal amplitude due to the limited gain of the regenerative

latch. In the simulation results shown in Figure 5.4, the comparator delay was assumed to be equal to zero (i.e. $T_c = 0$) and 72 dB SNDR was obtained. Also the comparator in the first path (see Figure 5.2) was clocked on the phase ϕ_{2-1}. This allowed the state of the second integrator (v_2) to be quantized and fed-back to the integrators' input, through the switched-capacitors, almost instantaneously. Then the loop-delay across each of the integrators was equal to $\frac{T_s}{K_{path}}$ (or z^{-1}). The feedback loop delay of $\frac{T_s}{K_{path}}$ leads to *true noise-shaping* with a single peak at $K_{path}f_s/2$. Next we consider a practical case where the comparator delay is $T_c = \frac{T_s}{2K_{path}}$ and the first comparator is clocked on the phase ϕ_{2-1}. Now the quantized feedback is returned to the integrator within the current time-slice but with a $\frac{T_s}{2K_{path}}$ delay. Figure 5.12 shows the simulated response of the second-order KD1S modulator with $T_c = T_s/2K_{path}$ with other specifications being the same as Figure 5.4. Here, the comparator delay has been modeled using Verilog-A with a variable delay parameter. The resulting SNDR is 62.6 dB which is roughly 9 dB less than the ideal simulation seen in Figure 5.4. This results in a 1.5 bits loss in resolution.

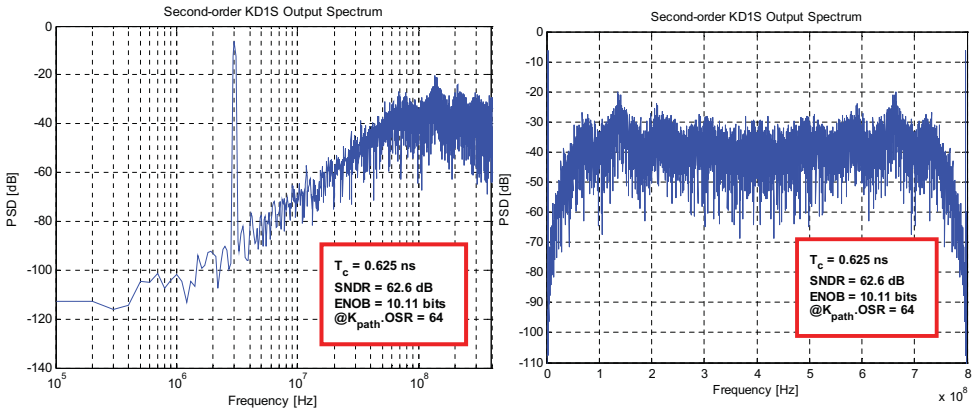

Figure 5.12: Spectre simulated PSD (log and linear frequency scales) of the second-order KD1S modulator with comparator delay $T_c = 625$ ps and the first comparator is clocked on ϕ_{2-1}. Here, $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz, $f_{un} = \frac{3}{8} f_{s,new} = 300$ MHz, $OSR = 8$, and $BW = 6.25$ MHz.

The reduction in SNDR with a $\frac{T_s}{2K_{path}}$ comparator delay is due to the fact that the integrators in the modulator now receive the quantized feedback later and in the mean-time the integrator's output continue to move in the same direction as defined by the last output held in the comparator. Thus the current information fed to the integrators have an information content from the past cycle with a T_s delay. Also the integrator is not having the full $\frac{T_s}{K_{path}}$ time-slice to make the initial push by the α_0 partial settling factor. These undesirable effects upset the ideal noise-shaping and causes ripples in the NTF response and raise the noise floor in the signal band as seen in Figure 5.12. Note that these ripples in the NTF response have peaks at odd multiples of $f_s/2$ which points to a loop delay of T_s for some of the information being fed back to the integrators. Moreover, since the integrators do not receive the instantaneous quantized feedback, the integrators states continue to move beyond the desired range. We can observe in Figure 5.13 that the histograms of the integrators states (their output nodes) have a wider spread

than seen in Figure 5.5. Thus in order to keep the integrator states bounded within the 60% V_{DD} range, we need to use more aggressive dynamic range scaling in the original design.

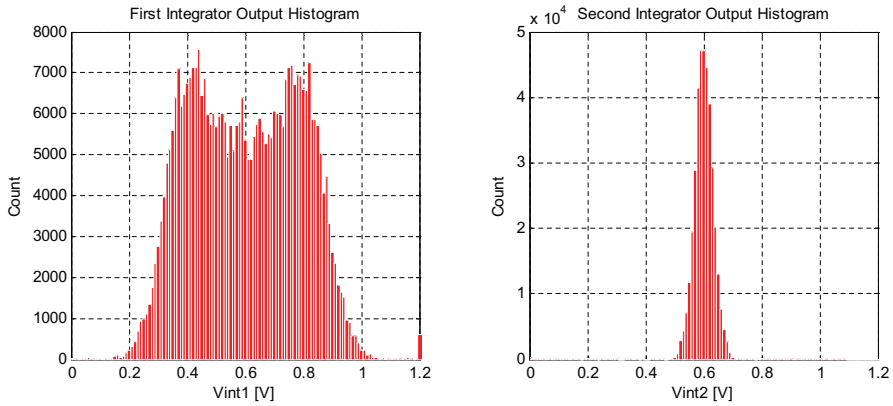

Figure 5.13: Histogram of the integrator states for the second-order KD1S modulator for the response seen in Figure 5.12.

Next, the comparator delay is increased to a full time-slice (i.e. $T_c = \frac{T_s}{K_{path}}$) while the first comparator is still clocked with phase ϕ_{2-1}. The resulting spectrum is shown in Figure 5.14 and the histogram of the integrator states is shown in Figure 5.15. Here, we see that ripples in the NTF response at the odd multiples of $f_s/2$ get more pronounced and the SNDR drops further to 40.8 dB (i.e. 6.5 bits resolution). This is a case where the noise-shaping flow has been broken and the integrators mostly get information being fed-back with a delay of T_s and not the latest quantized feedback.

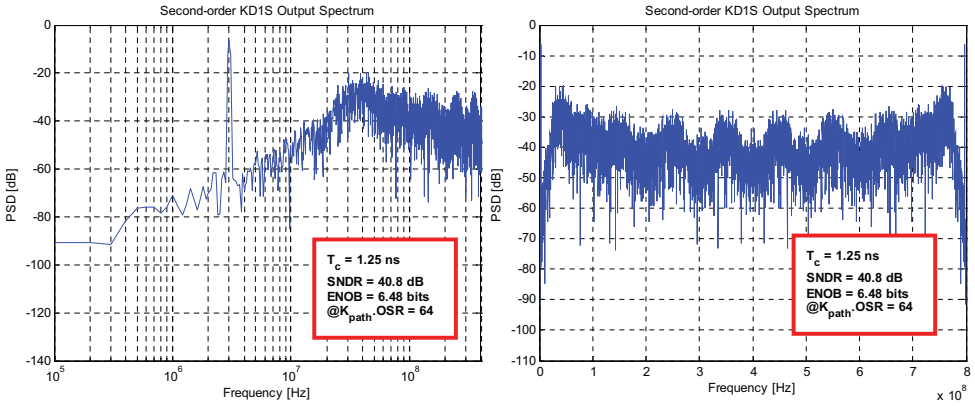

Figure 5.14: Spectre simulated PSD (log and linear frequency scales) of the second-order KD1S modulator with comparator delay $T_c = 1.25$ns and the first comparator is clocked on ϕ_{2-1}. Here, $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz,$f_{un} = \frac{3}{8} f_{s,new} = 300$ MHz, $OSR = 8$, and $BW = 6.25$ MHz.

Figure 5.15: Histogram of the integrator states for the second-order KD1S modulator for the response seen in Figure 5.14.

Also this extra delay causes the integrators states to be spread over supply voltage causing saturation in the first integrator. This problem can be mitigated by changing the clocking sequence of the comparators in such a way that the input to the integrators contains the latest quantized feedback. This was shown for the first-order KD1S modulator in Section 4.4.4. The modified comparator clocking is as shown in Figure 5.16

where the comparator in the first path is fired on the phase ϕ_{1-4} instead of ϕ_{2-1}. The second comparator is fired on the phase ϕ_{2-1}, the third on ϕ_{2-2}, and so on.

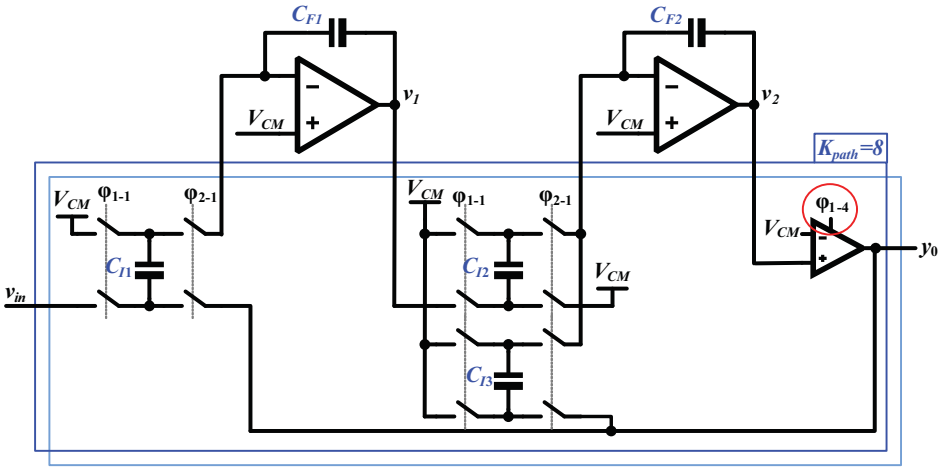

Figure 5.16: The second-order KD1S modulator with modified clock scheme to accommodate the $T_c = T_s/K_{path}$ (or z^{-1}) delay in the comparator.

The resulting NTF response is shown in Figure 5.17 and the histograms for the integrators states are shown in Figure 5.18. Here we see that the ripples in the NTF response have disappeared, but the now the response shows two distinct lobes. These lobes resemble the response of a double-sampling delta-sigma modulator. Also the lobes are tilted towards the baseband due to the charge spreading response ($W(z)$) of the K-path integrator. Here, the simulated SNDR is 52.4 dB and the resolution is 8.4 bits.

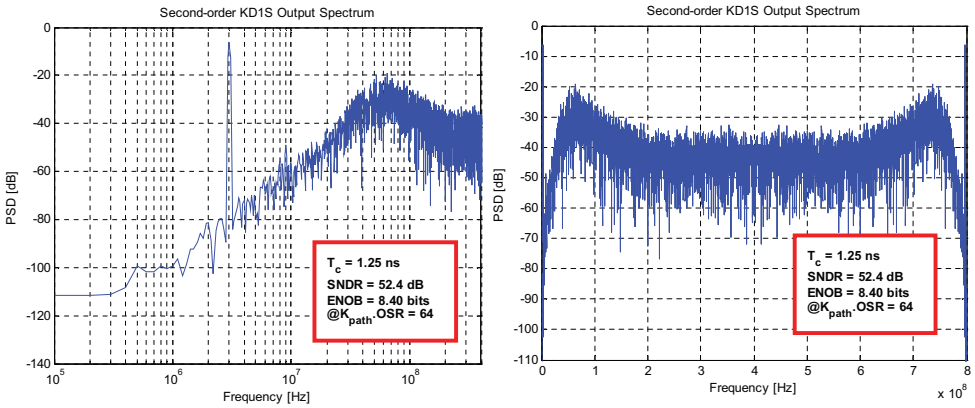

Figure 5.17: Spectre simulated PSD (log and linear frequency scales) of the second-order KD1S modulator with comparator delay $T_c = 1.25$ ns and the first comparator is clocked on ϕ_{1-4}. Here, $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz,$f_{un} = \frac{3}{8} f_{s,new} = 300$ MHz, $OSR = 8$, and $BW = 6.25$ MHz.

The integrator states are bounded within the supply rails. However the output of the first integrator has excursions beyond 60% of V_{DD} due to excess delay in the comparator.

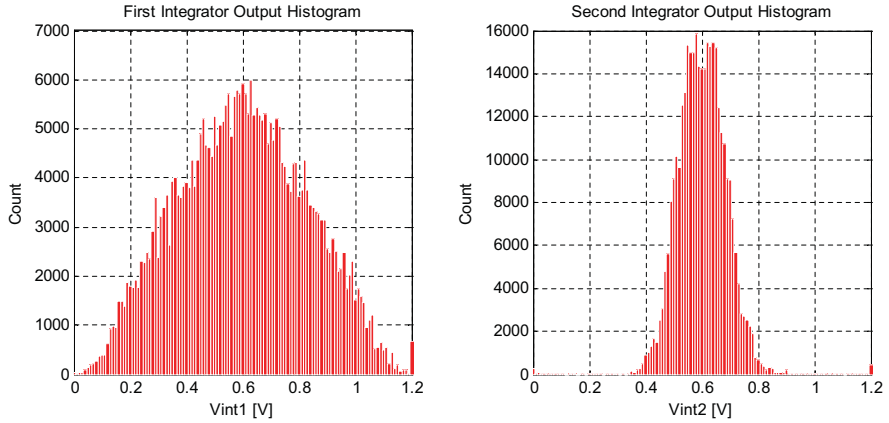

Figure 5.18: Histogram of the integrator states for the second-order KD1S modulator for the response seen in Figure 5.17.

This case, with a comparator delay of $T_c = \frac{T_s}{K_{path}}$ (or z^{-1}), has been modeled in Matlab and the resulting spectrum and pole-zero plot are shown in Figure 5.19. Note that the SNDR is close to the results obtained from Spectre simulation in the Figure

5.17. We can observe in the pole-zero plot that the poles are getting closer to the unit circle and thus reducing the stability margin of the modulator.

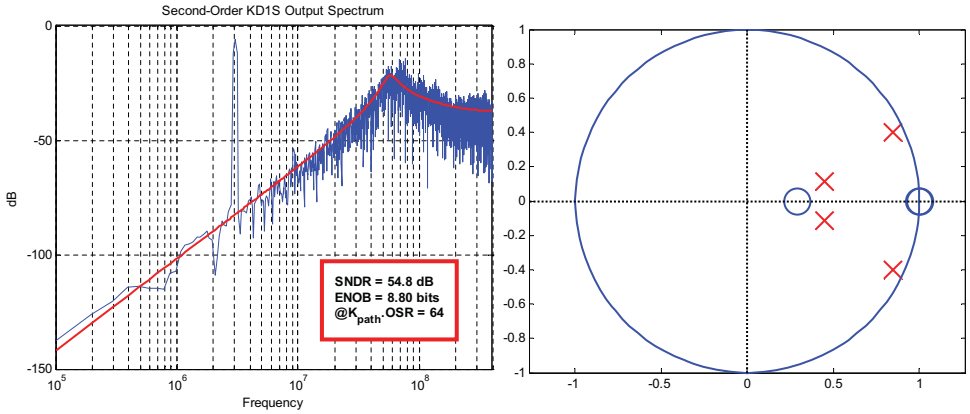

Figure 5.19: Matlab simulated PSD of the output and the NTF pole-zero plot for the second-order KD1S modulator with $f_{s,new} = 800$ MHz, $f_{un} = \frac{3}{8} f_{s,new}$, $K_{path} = 8$, $OSR = 8$, and T_c =1.25 ns (or z^{-1}).

The Spectre simulated results for the second-order KD1S modulator are depicted in Figure 5.20. Here we can see that the resolution drops rather linearly with an increase in the comparator delay. The ideal resolution of 11.14 bits for the conversion bandwidth of $BW = 6.25 MHz$ at $K_{path} \cdot OSR = 64$ is not possible to achieve with practical circuitry. However, we can achieve resolutions of 10.11 bits and 8.4 bits with comparator delays of 625 ps and 1.25 ns respectively.

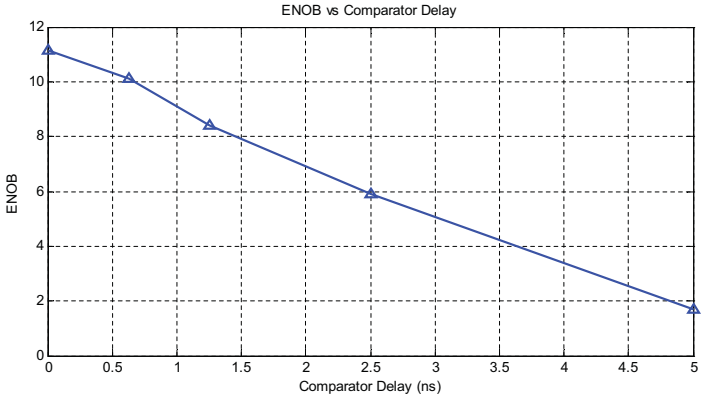

Figure 5.20: Effective resolution (ENOB) vs the Comparator delay for the second-order KD1S modulator measured with sinusoidal inputs. Here, the effective clock frequency is $f_{s,new} = 800$ MHz and $BW = 6.25$ MHz.

Thus we can conclude that the best SNDR performance from a second-order KD1S is achieved when the effective clock rate is given by

$$f_{s,new} = \frac{T_s}{2K_{path}} \leq \frac{1}{2T_c} \tag{5.6}$$

5.2.4 Capacitor Mismatch and Clock Skew

In Section 4.4.5, the noise folding due to the capacitor mismatches and clock-phase skew in the K-path integrator were analyzed. As seen in Figure 4.19 and from Equation 4.53, these mismatches cause the shaped quantization to fold back into the signal band from frequencies at multiples of f_s. In the second-order topology, the folding will also occur at the input of the second integrator in the loop. This will result in additional

noise appearing in the signal band and is described for the second-order modulator by

$$\begin{aligned} Y(z) &\approx STF(z)V_{in}(z) + NTF(z)Q_e(z) + \cdots \\ &\quad + \sum_{k=1}^{K_{path}-1} A_1(k)\cdot z^{-1} STF(z)\cdot NTF(e^{j\frac{2\pi k}{K_{path}}}z)\cdot Q_e(e^{j\frac{2\pi k}{K_{path}}}z) \\ &\quad + \sum_{k=1}^{K_{path}-1} A_2(k)\cdot z^{-1} STF_2(z)\cdot NTF(e^{j\frac{2\pi k}{K_{path}}}z)\cdot Q_e(e^{j\frac{2\pi k}{K_{path}}}z) \end{aligned} \tag{5.7}$$

where $A_{1,2}(k)$ are the distortion terms due to capacitor mismatch and clock-phase skew in the the first and second K-path integrators, and STF_2 is the signal transfer function from the input of the second integrator to its output. Figure 5.21 shows simulated comparison between the KD1S modulator performance with Gaussian distributed phase skew with 50 ps standard deviation (and with zero mean) and without phase skew. The simulated response shows that the noise floor in the signal band increases due to the noise folding effects causing a drop in SNDR by 6.5 dB or 1.08 bits in resolution. Thus, the inherent anomalies due to the time-interleaved structure of the modulator pose a stringent limit on the achievable modulator SNDR performance.

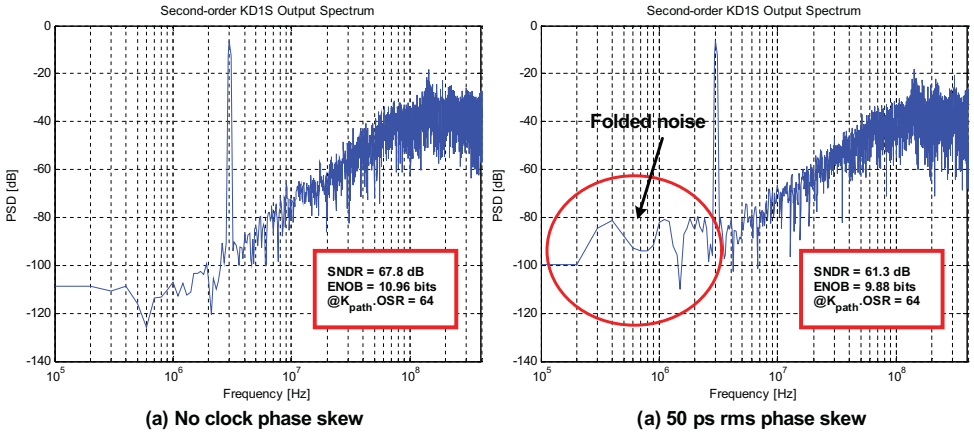

Figure 5.21: Spectre simulation showing the noise-folding due to clock-phase skew in the second-order KD1S modulator. (a) Spectrum with no phase skew, (b) spectrum with Gaussian distributed phase skew with 50 ps standard deviation. Here, $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz,$f_{un} = \frac{3}{8} f_{s,new} = 300$ MHz, $OSR = 8$, and $BW = 6.25$ MHz.

5.2.5 Clock Jitter

The discussion on the effects of clock jitter in the first-order KD1S modulator (see Section 4.4.6) also pertain to the second-order topology.

5.3 Conclusion

A second-order KD1S modulator design has been presented and analyzed and simulated for op-amp and comparator non-idealities. In order to achieve a stable second-order modulator, a CIFB topology with an extra feed-back branch to the second integrator is employed. The response of the K-path integrator was analytically modeled and dynamic range scaling was employed to ensure that the integrator outputs remain in the linear region.

CHAPTER 6 SYNTHESIS OF HIGHER-ORDER KD1S MODULATORS

In this chapter, higher-order delta-sigma modulation is briefly explained along with the generic modulator topologies pertaining to KD1S modulators. A short tutorial on the internal working of the delta-sigma toolbox [25] is provided. A state-space based embedding method is introduced which allows systematic synthesis and simulation of higher-order KD1S modulators.

6.1 Higher-order Delta-Sigma Modulators

Delta-sigma modulators with an order greater than two lead to more aggressive noise shaping and thus better performance. However, these benefits arrive at the cost of more circuitry and reduced input signal range. The generalized delta-sigma modulator is described by a two input loop-filter given by [23]

$$Y(z) = L_0(z)U(z) + L_1(z)V(z) \tag{6.1}$$

where $U(z)$ is the input signal and $V(z)$ is the quantized output fedback through a DAC. The output of the modulator ($V(z)$) is related to the loop-filter's output ($Y(z)$) by [23]

$$V(z) = Y(z) + E_Q(z) \tag{6.2}$$

where $E_Q(z)$ is the additive linearized model of the quantization noise added by the quantizer. Using the above two equations the modulator's linearized output is given in

terms of the inputs as

$$Y(z) = STF(z)U(z) + NTF(z)E_Q(z) \tag{6.3}$$

where we have the noise and signal transfer functions given by [23]

$$\begin{aligned} NTF(z) &= \frac{1}{1-L_1(z)} \\ STF(z) &= \frac{L_0(z)}{1-L_1(z)} \end{aligned} \tag{6.4}$$

On the other hand, we can express the loop transfer functions in terms of NTF and STF as

$$\begin{aligned} L_0(z) &= \frac{STF(z)}{NTF(z)} \\ L_1(z) &= 1 - \frac{1}{NTF(z)} \end{aligned} \tag{6.5}$$

The above described generalized modulator structure is shown in the block diagram in Figure 6.1.

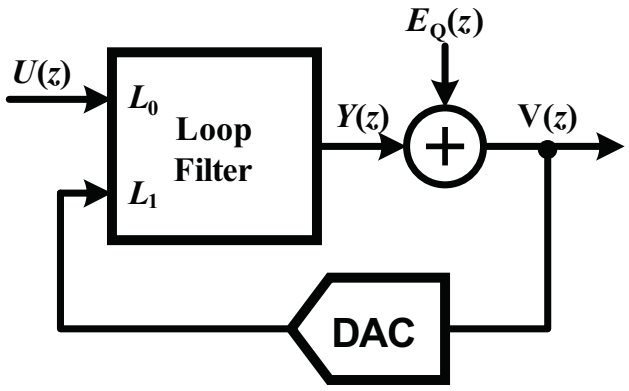

Figure 6.1: A generalized structure of a delta-sigma modulator.

From Equation 6.5, we can deduce that for the NTF to be low in the signal band ($f = 0$ to f_B, where $f_B = \frac{f_s}{2 \cdot OSR}$) $L_1(z)$ must be large in the signal band with a low-pass response. Also $L_0(z)$ should be large in the signal band so as to maintain the STF response close to unity. This implies that both L_0 and L_1 must have poles in the same vicinity. Since L_0 and L_1 share the same circuitry, these poles are usually co-incident and form the zero of the NTF. However, the zeros of L_0 and L_1 are generally distinct. In the simplest case, for a L^{th} order modulator, where the $NTF(z) = \left(1 - z^{-1}\right)^L$ differentiates the quantization noise M-times and $STF(z) = z^{-k}$, $k < L$. This leads to the expressions

$$\begin{aligned} L_0(z) &= z^{-k}\left(1 - z^{-1}\right)^{-L} \\ L_1(z) &= 1 - \left(1 - z^{-1}\right)^{-L} \end{aligned} \tag{6.6}$$

where the poles of both L_0 and L_1 are located on the unit circle , at $z = 1$. On the other hand, for L_0, the $(L-k)$ zeros are located at $z = 0$ while the remaining k zeros are located at infinity [23]. The zeros of L_1 are given by the roots of the equation $\left(1 - z^{-1}\right)^L = 1$ and are expressed by the expression

$$z_l = \left(1 - e^{-\frac{j2\pi l}{L}}\right) = \frac{(1 + j\cot(\pi l/L))}{2},\ l = 1, 2, ..., L-1 \tag{6.7}$$

For this modulator and with $OSR \gg 1$, the in-band noise power is given by

$$\sigma_n^2 = \frac{\sigma_q^2 \pi^{2L}}{(2L+1)\, OSR^{2L+1}} \tag{6.8}$$

and the maximum signal-to-quantization noise ratio (SQ NR) is expressed as [23]

$$SQNR = 6.02N + 1.76 + (20L + 10)\log_{10}(OSR) - 10\log_{10}\left(\frac{\pi^{2L}}{2L+1}\right) \tag{6.9}$$

From the above equation, it can be deduced that for a higher oversampling ratio (*OSR*), the SQNR increases by $\left(L + \frac{1}{2}\right)$ bits per doubling in *OSR*. Thus increasing the order of the modulator has a direct impact on the achievable resolution.

6.1.1 Stability Considerations and Multi-Bit Modulators

Equation 6.3 depicts the linearized model of the delta-sigma modulator where the stability of the modulator depends only upon the loop-gain $L_1(z)$ and thus the NTF. However, we need to accommodate the non-linear behavior of the quantizer in order to gain further insight into the modulator stability. Also the stability depends upon the amplitude of the input signal, $u(n)$, as a large enough input can lead to integrator saturation and quantizer overload, which in turn destabilizes the modulator loop. This effect of unbounded input signal amplitude on the modulator stability has been discussed earlier in Section 5.1.1 for the second-order modulators.

For the delta-sigma modulators with single-bit quantizer, a heuristic result called *Lee's criterion* states that modulator is likely to be stable if the out-of-band gain (*OBG*) follows the condition that $OBG = \max\left|NTF\left(e^{j\omega}\right)\right| < 1.5$ [24]. However, this is neither necessary nor sufficient condition but it serves as a simple design rule [23] and the modulator stability must be confirmed through extensive simulations.

So far we have assumed that the gain (k_q) of the quantizer is constant and equal to unity. However the gain of the quantizer strongly depends upon its input. As illustrated in Figure 6.2, the gain of a single-bit quantizer varies widely with its input due to the hard non-linearity. However for the multi-bit quantizer case, the quantizer gain is restricted to a narrower range, which gets tighter as the quantizer levels are increased. The statistics of the quantizer gain depends upon the PD of its input, $f_Y(y)$, in the closed-loop operation of the modulator, and the average gain is estimated from the simulations as $k_q = \frac{E[|y|]}{E[y^2]}$ [23].

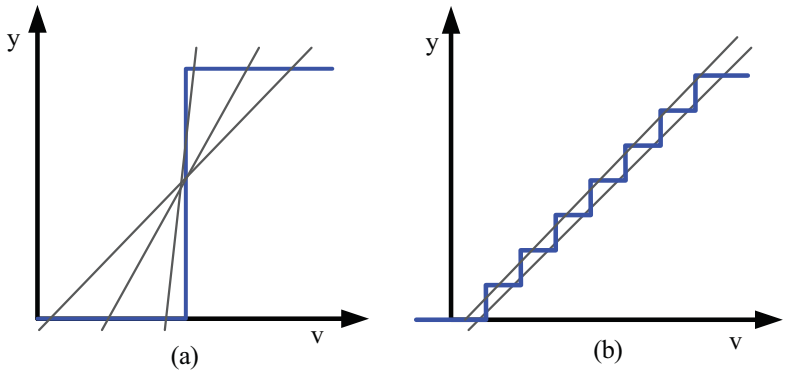

Figure 6.2: Illustration of the variation of quantizer gain with respect to the input signal for (a) a single-bit quantizer and (b) a multi-bit quantizer.

The modified NTF response after accommodating the quantizer gain variation is given as

$$NTF_{k_q}(z) = \frac{1}{1 - k_q L_1(z)} = \frac{NTF_1(z)}{k_q + (1 - k_q)\, NTF_1(z)} \tag{6.10}$$

where $NTF_1(z)$ is the noise-transfer function with a constant quantizer gain of 1. Figure 6.3 shows the root locus of a third-order modulator with the quantizer gain k_q varying from 0 to 1. We can observe that the for values of $k_q < 0.34$, a pair of poles of NTF are

out of the unit circle and thus rendering the modulator unstable. The low quantizer gain results due to quantizer overload, when the amplitude of the quantizer input exceeds its output range. Also, we can observe that a large variation in quantizer gain undermines the stability of a higher-order modulator.

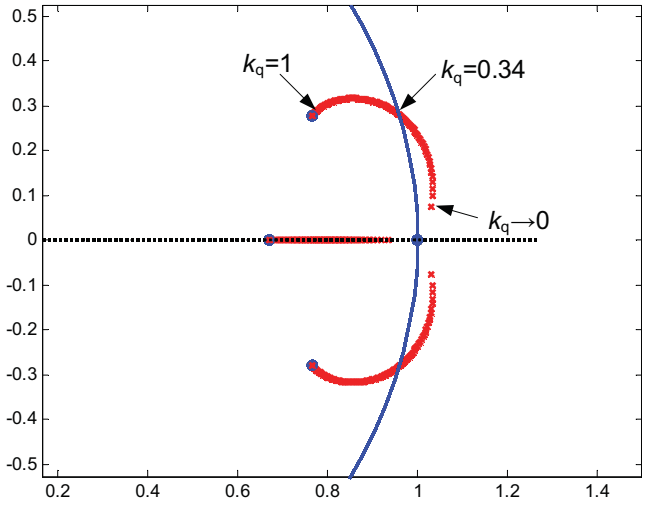

Figure 6.3: Root locus of the NTF for a third-order modulator with varying quantizer gain.

A single-bit modulator results in a simple quantizer design where only a single comparator is employed for quantization. A single bit quantizer does away with the circuitry required for offset cancellation and bubble correction in a Flash ADC. Also the corresponding single-bit DAC is inherently linear due to only two possible output levels which further does away with logic and element redundancy dedicated to dynamic element mismatch shaping (DEM). Thus, the KD1S modulators discussed in the dissertation employ single-bit quantizers. Also notice that the use of multi-bit quantizers for each path in a KD1S will be prohibitive due to large layout area and power

consumption. However, it is instructive to cover the benefits of the multi-bit quantizers to complete the discussion on higher-order modulators. The advantages offered by the multi-bit quantizer over their single-bit counterparts are as follows [23]:

1. *Lower In-Band Quantization Noise*: The multi-bit quantizer increases the modulator SQNR by 6 dB for every bit increase in its resolution. This correspondingly lowers the quantization noise floor and directly increases the SNDR. Also the roll-off requirements on the decimation filter, used to suppress the out of band noise, are relaxed.

2. *Linear Loop Filter Behavior*: As illustrated earlier, the variations in the gain are reduced in a multi-bit quantizer. This makes the modulator loop more linear and stable. Also, now the real modulator response closely follows the predicted performance of the linearized model and the design is more robust. This is also useful in the case of the cascaded (or MASH) modulator, where the design of the noise cancellation filter (NCF) can be done using the simple linear analysis and the noise leakage due to the variations in the effective NTFs is minimized. Thus, from a system design perspective multi-bit quantizers are preferable.

3. *Aggressive Noise Shaping*: Since the loop stability is more robust with a multi-bit quantizer, an aggressive NTF can now be employed in the design with an out-of-band gain (*OBG*) greater than 1.5. This fact is extremely useful when designing 5^{th} or higher order modulators where significantly large resolution is desired with

a relatively lower *OSR* (i.e. wideband high-resolution conversion). Here a 11 to 16 level quantizer can help achieve over 60 dB SNDR with an OSR of 8 [10].

4. *Lower Slew Rate Requirements in the Loop-Filter*: Since the DAC feedback to the loop filter changes in smaller steps ($LSB = V_{range}/2^N$) when using a multi-bit design, the slew rate requirements on the input op-amp (the *golden* op-amp which sets the overall linearity of the modulator) are reduced. This also relaxes the linearity requirements on the input loop filter $L_0(z)$.

5. *Higher Maximum Stable Amplitude*: When using multi-bit quantizer, the maximum stable amplitude (MSA) of the input tolerated by the modulator can be large. This is due to the fact that the smaller LSB values result in higher tolerance to loop-filter saturation and quantizer overload.

6. *Reduced Jitter-Noise Sensitivity*: In the case of continuous-time modulators, the in-band noise due to clock jitter with NRZ DAC pulse shape is given by [41]

$$IBN_{\sigma_{jt}}|_{NRZ,MB} \approx \frac{V_{range}^2}{(2^N-1)^2}\left(\frac{\sigma_{jt}}{T_s}\right)^2 \frac{2}{OSR} \tag{6.11}$$

which is clearly reduced when higher quantizer resolution is employed. This is due to the fact that the amount of DAC pulse-width difference ($\delta y[n] = y[n] - y[n-1]$) modulated by the clock jitter is reduced when more quantization levels are used. Thus multi-bit quantizers have become ubiquitous in CT DSM design [41, 42].

6.2 NTF Pole and Zero Optimization

NTF pole and zero optimization is an important technique for synthesis of high-resolution, higher-order modulators. In the simple example seen in Section 6.1 the NTF was of the form $\left(1-z^{-1}\right)^{L}$ and all the zeros were located at $z=1$ and the poles were at $z=0$. Now if we intelligently spread these zeros around in the signal band and also move the poles to surround the zeros while being within the unit circle, significant improvements in SQNR can be achieved. This NTF pole and zero optimization is done using the delta-sigma toolbox [25] in Matlab and is its algorithm is detailed in [23]. Figure 6.4 compares the spectra of a single-bit third-order DSM with $OSR=64$ with and without NTF (zero and pole) optimization. The locations of the NTF zeros as the result of the SQNR optimization are shown in Figure 6.5.

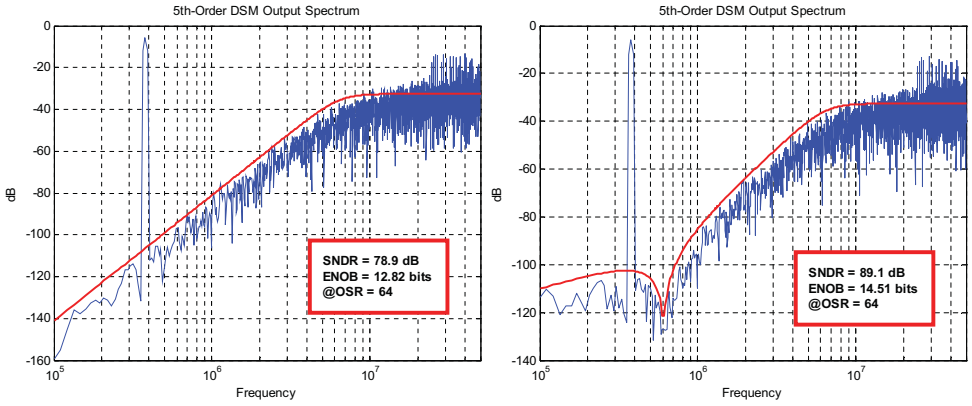

Figure 6.4: Example of NTF zero and pole optimization. Here a third-order single-bit delta-sigma modulator is synthesized for $OSR=64$.

Here, we can observe that the SQNR is increased by roughly 10 dB resulting in 1.7 bits increase in resolution. Further, we observe that the noise floor in the later case

is raised and the NTF notch in the signal band is flattened out. This relaxes the gain requirements on the op-amps in the loop-filter.

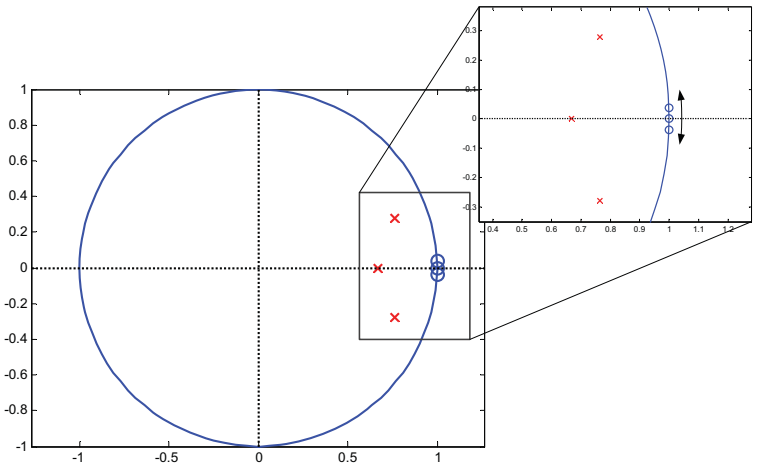

Figure 6.5: NTF zero spreading in the signal band with SQNR optimization.

6.3 Loop-filter Architectures

There are many generalized structures to realize the higher-order delta-sigma modulators. We know that the KD1S modulators utilize K-path integrators which result in a delay of T_s/K_{path} (or z^{-1}) for the partial settling. Thus in this section two topologies employing delaying integrators, which are pertinent to the KD1S implementation, are described. The first loop-filter architecture, shown in Figure 6.6, is called Cascade of Integrators with Distributed FeedBack (CIFB) [23]. This topology comprises of a cascade of L delaying integrators. The feedback and signal inputs are fed into each of the integrators with weight factor coefficients a_i and b_i ($a_i, b_i > 0$). For now, assume that we have $g_i = 0$ and $c_i = 1$. The transfer function for the input loop-filter L_0 is given by

[23]

$$\begin{aligned} L_0(z) &= \sum_{i=1}^{N+1} \frac{b_i}{(z-1)^{N+1-i}} \\ &= \frac{b_1 + b_2(z-1) + \cdots + b_{N+1}(z-1)^N}{(z-1)^N} \end{aligned} \tag{6.12}$$

and the loop-filter seen by the feedback is given as [23]

$$\begin{aligned} L_1(z) &= \sum_{i=1}^{N} \frac{-a_i}{(z-1)^{N+1-i}} \\ &= -\frac{a_1 + a_2(z-1) + \cdots + a_N(z-1)^{N-1}}{(z-1)^N} \end{aligned} \tag{6.13}$$

Thus the noise transfer function NTF of the modulator is given by [23]

$$NTF(z) = \frac{1}{1 - L_1(z)} = \frac{(z-1)^N}{D(z)} \tag{6.14}$$

where the denominator is expressed as

$$D(z) = a_1 + a_2(z-1) + \cdots + a_N(z-1)^{N-1} + (z-1)^N \tag{6.15}$$

From the above two equations, we can observe that the zeros of the NTF are located at $z = 1$ which is at DC. The locations of the poles is controlled by the coefficients a_i. The signal transfer function is given as

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)} = \frac{b_1 + b_2(z-1) + \cdots + b_{N+1}(z-1)^N}{D(z)} \tag{6.16}$$

Here we see that the poles of the STF are same as that of the NTF and are determined by a_i. On the other hand, the zeros of the STF are determined by b_i [23].

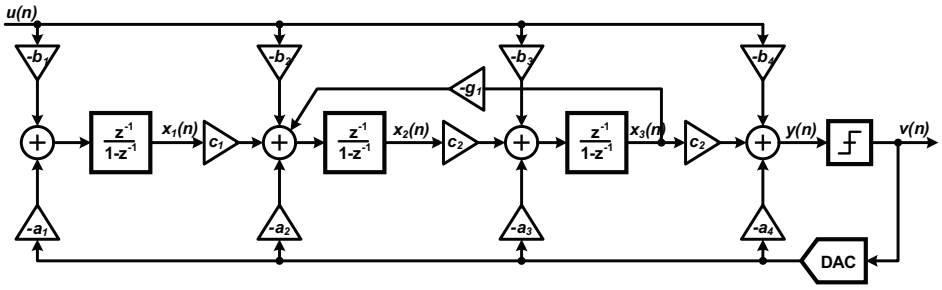

Figure 6.6: CIFB (Cascade of Integrators with Distributed FeedBack) modulator topology.

An important case is when $b_i = a_i$ for $\forall i \leq N$ and $b_{N+1} = 1$, then the STF is exactly equal to 1 and the modulator's output is equal to

$$V(z) = U(z) + NTF(z)E_Q(z) \tag{6.17}$$

For this condition, the modulator input signal $u[n]$ is not processed by any of the integrators. The loop filter only acts on the quantization noise $e(n)$. Due to this the integrator swings are reduced and the integrator non-linearities do not introduce distortion into the signal path. The amount of quantization noise processed by the loop-filter is further reduced when multi-bit quantizers are employed [23].

So far the NTF zeros have been designed to be located at DC ($z = 1$). In Section 6.2, it was shown that by distributing these zeros appropriately in the signal band, significant improvements in SQNR can be achieved. Now, in Figure 6.6, consider g_i to be non-zero. Now, we observe that the middle two integrators, together form a second-order resonator with the locations of the zeroes being determined by g_1. The transfer function of the first resonator in the figure is given by [23]

$$R_1(z) = -\frac{a_1 z + a_2(z-1)}{z^2 - 2z + (1+g_1)} \tag{6.18}$$

here the zeroes are located at $z = 1 \pm j\sqrt{g_1}$. Even though the resonators are individually unstable, when embedded in a well designed feedback system, they do not exhibit local oscillations. In Figure 6.6, the coefficients c_i are obtained as a result of dynamic range scaling (DRS), discussed later in Section 6.4.4. A systematic loop-filter design method with NTF zero optimization is detailed in [23] and is implemented in the delta-sigma toolbox [25].

Instead of using a feedback structure to realize the loop-filters L_0 and L_1 given by Equations 6.12 and 6.13 respectively, a feed-forward structure can also be employed. Figure 6.7 shows a third-order modulator with delaying integrators and feed-forward branches. This topology is called **C**hain of **I**ntegrators with **F**eed-**F**orward summation (CIFF) .

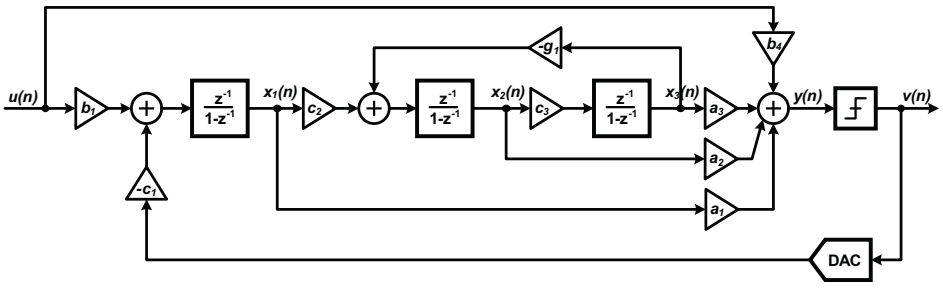

Figure 6.7: CIFF (Cascade of Integrators with distributed FeedForward) modulator topology.

We can observe that the feedback filter transfer function is given by [23]

$$L_1(z) = -a_1 I(z) - a_2 I^2(z) - \cdots - a_N I^N(z) \tag{6.19}$$

where $I(z) = \frac{z^{-1}}{1-z^{-1}}$ is the transfer function of the delaying integrator. Similarly, the input transfer function is given by [23]

$$L_0(z) = b_1 \left(\sum_{i=1}^{N} a_i I^i(z) \right) + b_2 \left(\sum_{i=2}^{N} a_i I^i(z) \right) + \cdots + b_{N+1} \tag{6.20}$$

For this structure when $b_i = 0$, $i = 2, \ldots, N$ and $b_1 = b_{N+1} = 1$, we have $L_0(z) = 1 - L_1(z)$ which leads to $STF(z) = 1$. Again, for this condition, the input to the loop-filter satisfies

$$U(z) - V(z) = -NTF(z)E_Q(z) \tag{6.21}$$

which implies that the loop-filter processes only the quantization noise and not the input signal. Thus, this loop-filter has the property of low distortion and relaxed performance requirement for the op-amps. The branches g_i are added for NTF zero optimization and coeffcients c_i are introduced to accommodate dynamic range scaling.

6.4 Synthesis Procedure for KD1S Modulators

The delta-sigma toolbox in Matlab is widely used to rapidly synthesize and simulate delta-sigma modulator topologies. The synthesis process yields the loop-filter coefficients for the modular topology designed for a given set of specifications. These resulting filter co-efficients are mapped to a switched-capacitor filter for discrete-time implementation, and to either op-amp-R or g_m-C filter for the continuous-time implementation of the modulator. The toolbox internally employs constructs and techniques from linear systems theory to describe the loop-filter topologies. In this section, a short

background on the working of the toolbox is provided. Further this toolbox is extended to synthesize and simulate generalized higher-order KD1S modulators.

6.4.1 The ABCD Matrix

The delta-sigma toolbox internally uses ABCD matrix to represent the linear part of the modulator, which are the loop-filters L_0 and L_1, as illustrated in 6.8. The ABCD matrix representation of the loop-filter is indispensable for linear operations like dynamic range scaling, automated design mapping and for rapid discrete-time simulation of the modulator architectures. The ABCD matrix is a combination of four sub-matrices which describe the dynamics of any discrete-time linear system. The state-space equations for the DSM loop filter are described as

$$\begin{aligned} \mathbf{x}[n+1] &= A\mathbf{x}[n] + B \begin{bmatrix} u[n] \\ v[n] \end{bmatrix} \\ \mathbf{y}[n] &= C\mathbf{x}[n] + D \begin{bmatrix} u[n] \\ v[n] \end{bmatrix} \end{aligned} \tag{6.22}$$

where $\mathbf{x}(n) \in R^{M\times 1}$ is the state vector at time n for an M^{th}-order modulator. The matrix $A \in R^{M\times M}$ defines the interconnections withing the loop filter. The matrix $B \in R^{M\times 2}$ describes how the modulator input $u[n]$ and the feedback DAC output $v[n]$ are applied to the loop filter $H(z)$. The matrices $C \in R^{1\times M}$ and $D \in R^{1\times 2}$ describe the computation of the output $y[n]$ from the states $\mathbf{x}[n]$ and the loop filter inputs $\begin{pmatrix} u[n] & v[n] \end{pmatrix}^T$ [23].

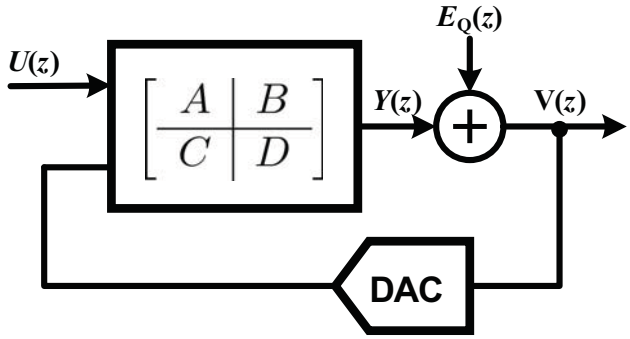

Figure 6.8: The ABCD Matrix representation of the loop-filter in a delta-sigma modulator.

The loop transfer functions are obtained from the ABCD matrix as

$$\begin{bmatrix} L_0(z) \\ L_1(z) \end{bmatrix} = C\left(z^{-1}I - A\right)^{-1}B + D \tag{6.23}$$

The delta-sigma toolbox evaluates the equivalent closed-loop ABCD matrix, $ABCD_{cl}$ as

$$\begin{aligned} A_{cl} &= A + k_q B_2 C \\ B_{cl} &= \begin{bmatrix} B_1 + k_q B_2 D_1 & B_2 \end{bmatrix} \\ C_{cl} &= k_q C \\ D_{cl} &= \begin{bmatrix} k_q D_1 & 1 \end{bmatrix} \end{aligned} \tag{6.24}$$

where $B_{1,2}$ are columns of $B = \begin{bmatrix} B_1 & B_2 \end{bmatrix}$ and D_1 is the first column element of $D = \begin{bmatrix} D_1 & D_2 \end{bmatrix}$. Here, it is assumed that the quantizer delay ($z^{-1/2}$) has been absorbed into the last integrator delay of $z^{-1/2}$ and thus the quantizer only introduces a gain of k_q and has zero delay. Consequently, from the $ABCD_{cl}$ matrices the STF and NTF are

evaluated as

$$\begin{bmatrix} STF(z) \\ NTF(z) \end{bmatrix} = C_{cl}\left(z^{-1}I - A_{cl}\right)^{-1} B_{cl} + D_{cl} \tag{6.25}$$

6.4.2 *K*-path Integrator Modeling

Discrete-time loop-filter topology is comprised of ideal integrators holding the state of the linear system, and the loop-filter topology is defined by their cross-connections. So far we assumed that the integrators have an ideal frequency response. However, in reality these integrators are implemented using real op-amps which introduce their characteristic non-idealities. The linear non-idealities of the op-amps can in turn be modeled using a state space model with order greater than unity. This concept was introduced for continuous-time loop-filter in [54]. However, here we try to model the *K*-path integrator with a discrete-time linear state space model. The behavior of all the *K*-SCIs in the loop-filter can be described by the generalized state-space model

$$\begin{aligned} \mathbf{x}[n+1] &= A_{int}\mathbf{x}[n] + B_{int}\mathbf{P}[n] \\ \mathbf{O}[n] &= C_{int}\mathbf{x}[n] \end{aligned} \tag{6.26}$$

where $\mathbf{x}[n]$ is now the new state vector of the KD1S loop-filter with the *K*-SCI non-idealities. Here, $\mathbf{P}[n]$ is a vector containing the inputs to all the integrators, and $Q[n]$ is a vector of the outputs of each of the integrators. From Eq. 4.22, the transfer function of the *K*-SCI is given by $H_1(z) = \frac{C_I}{C_F}\frac{z^{-1}}{1-z^{-1}}\frac{1-\alpha_0}{1-\gamma_0 z^{-1}}$. This transfer function is modeled with a combination of delaying and non-delaying integrators as shown in Figure 6.9. The

output q of the integrator is a linear combination of the internal states x_1 and x_2, and is given by

$$q[n] = (1-\alpha_0)\,x_1[n] + \gamma_0 x_2[n] \tag{6.27}$$

Thus, the ABCD matrix for the a single K-path integrator is given by 6.9

$$\left[\begin{array}{c|c} A & B \\ \hline C & D \end{array}\right]_{int} = \left[\begin{array}{cc|c} 1 & 0 & 1 \\ 1-\alpha_0 & \gamma_0 & 0 \\ \hline 1-\alpha_0 & \gamma_0 & 0 \end{array}\right] \tag{6.28}$$

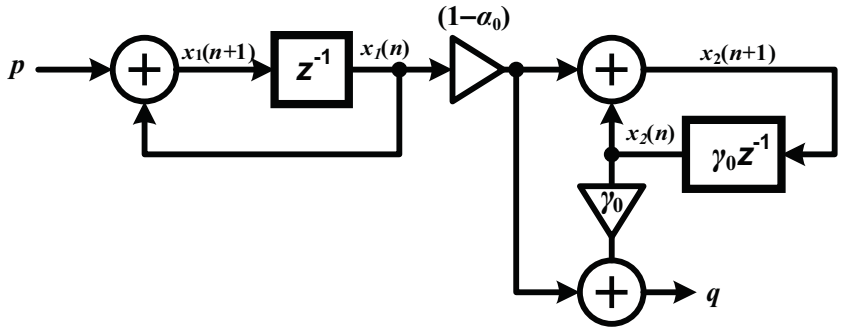

Figure 6.9: A discrete-time linear system representation of the K-path integrator.

Note that if we just picked the output as $q[n] = x_2[n]$, an additional delay would have been introduced with the transfer function becoming $\frac{C_I}{C_F}\frac{z^{-1}}{1-z^{-1}}\frac{(1-\alpha_0)z^{-1}}{1-\gamma_0 z^{-1}}$. For this case, the ABCD matrix will be given by

$$\left[\begin{array}{c|c} A & B \\ \hline C & D \end{array}\right]_{int} = \left[\begin{array}{cc|c} 1 & 0 & 1 \\ 1-\alpha_0 & \gamma_0 & 0 \\ \hline 0 & 1 & 0 \end{array}\right] \tag{6.29}$$

We can further modify this model to include the effects of the finite op-amp gain given by Equation 4.34. The resulting ABCD matrix for an integrator is given by

$$\left[\begin{array}{c|c} A & B \\ \hline C & D \end{array}\right]_{int} = \left[\begin{array}{cc|c} p & 0 & p \\ 1-\alpha_0 & \gamma_0 & 0 \\ \hline 1-\alpha_0 & \gamma_0 & 0 \end{array}\right] \tag{6.30}$$

where $p = \frac{1}{1+\frac{C_I}{C_F}\cdot\frac{1}{A_{OL}}} \approx 1 - \frac{C_I}{C_F}\cdot\frac{1}{A_{OL}}$.

For a system with more than one integrator, the combined state-space representation for the K-path integrators can be derived from the ABCD representation for a single integrator. This is illustrated in Figure 6.10. Here, each of the non-ideal integrators have individual inputs p_i and outputs q_i forming the input vector P and output vectors Q respectively. The equivalent A matrix for all the op-amps is obtained by doubling the system order and then by substituting the A_{int1} matrix (which was derived in Equation 6.28 for a single integrator) along the diagonals. The remaining B, C, and D matrices are obtained by observing the connectivity of the vectors P and Q to each of the op-amps.

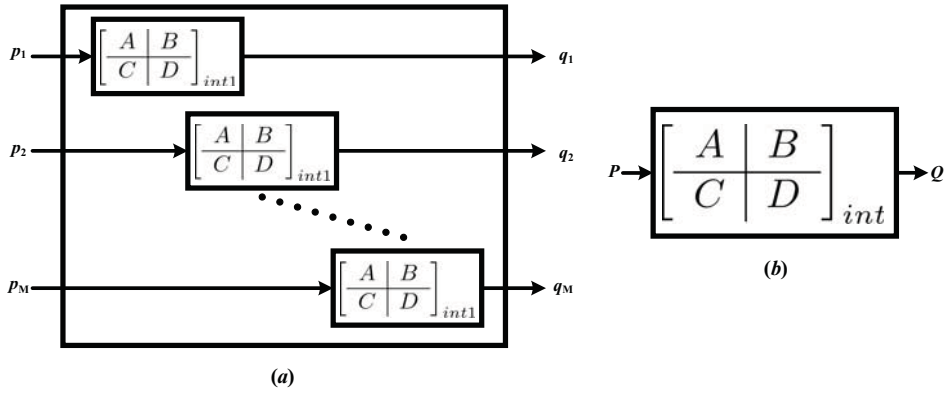

Figure 6.10: Illustration of the generalized ABCD matrix for a set of M integrators, (a) individual ABCD matrices for the integrators with individual inputs and outputs, (b) combined ABCD matrix for all the integrators.

For example, for a second-order KD1S modulator the integrator, the loop-filter ABCD matrix is obtained to be equal to

$$\left[\begin{array}{c|c} A & B \\ \hline C & D \end{array}\right]_{int} = \left[\begin{array}{cccc|cc} 1 & 0 & 0 & 0 & 1 & 0 \\ 1-\alpha_{0_1} & \gamma_{0_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1-\alpha_{0_2} & \gamma_{0_2} & 0 & 0 \\ \hline 1-\alpha_{0_1} & \gamma_{0_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 1-\alpha_{0_2} & \gamma_{0_2} & 0 & 0 \end{array}\right] \tag{6.31}$$

Note that the order of this state-space representation of the K-path op-amps in a second order modulator has an order equal to 4, which is double the order of the ideal second order modulator system. Similarly, the for a third-order KD1S loop-filter the ABCD matrix can be deduced to be given by

$$\left[\begin{array}{cccccc|ccc} p_1 & 0 & 0 & 0 & 0 & 0 & p_1 & 0 & 0 \\ 1-\alpha_{0_1} & \gamma_{0_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & p_2 & 0 & 0 & 0 & 0 & p_2 & 0 \\ 0 & 0 & 1-\alpha_{0_2} & \gamma_{0_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & p_3 & 0 & 0 & 0 & p_3 \\ 0 & 0 & 0 & 0 & 1-\alpha_{0_3} & \gamma_{0_3} & 0 & 0 & 0 \\ \hline 1-\alpha_{0_1} & \gamma_{0_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1-\alpha_{0_2} & \gamma_{0_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1-\alpha_{0_3} & \gamma_{0_3} & 0 & 0 & 0 \end{array}\right] \tag{6.32}$$

Here, α_{0_i}, γ_{0_i} and p_i are the settling coefficient α_0, additional pole γ_0 and the pole modification due to the finite op-amp gain p for the i^{th} K-path integrator used in the modulator.

6.4.3 The State-Space Embedding Method

The KD1S modulator can be designed by appropriately modifying an equivalent single-path DSM and by incorporating the analytical results for the K-path switched-capacitor integrator (K-SCI). It can be observed that in a KD1S modulator, there is always a delay of T_s/K time-slice (or z^{-1} delay for Kf_s clock rate). Due to this, the KD1S modulator can only be realized by using the **CIFB** (cascade of integrators, feedback form) and **CIFF** (cascade of integrators, feed-forward form) topologies. Now, we need to account for the charge-spreading filter in the K-SCIs used in the modulator. This problem is analogous to the simulation of continuous-time (CT) delta-sigma modulators where op-amp non-idealities are an important concern. A 'lifting' or 'embedding' method has been devised for continuous-time state-space of the CT-DSMs in [54]. Here, the linear state-space model for the non-ideal op-amp is embedded into the ideal loop-filter state-space representation. This method has been applied to the discrete-time case of KD1S in order to incorporate the non-idealities (i.e. the additional pole at $z = \gamma_0$, gain scaling by $(1-\alpha_0)$ and the effect of finite op-amps gain) of the K-SCI. This method leads to quick system level simulation of the KD1S modulators without going through the full-fledged behavioral or circuit level implementation. The embedding of the K-SCI state-space model into the overall loop-filter is graphically illustrated in Figure 6.4.3.

Lets say that the input to all the integrators in the DSM loop-filter is $\mathbf{P}[n]$ and the output of all the integrators is $\mathbf{O}[n]$. This changes the state-space representation of the loop-filter to

$$\begin{aligned} \mathbf{P}[n] &= \mathbf{x}[n+1]-\mathbf{x}[n] = (A-I)\mathbf{O}[n]+B\mathbf{U}[n] \\ y[n] &= C\mathbf{O}(n)+D\mathbf{U}(n) \end{aligned} \tag{6.33}$$

where $\mathbf{U}[n] = \begin{bmatrix} u[n] & v[n] \end{bmatrix}^T$. Here, the relation ($x[n+1] = x[n]+\mathbf{P}[n]$) is utilized to relate the states $x[n]$ of the loop-filter and the inputs $P[n]$ to the integrators. This relationship is illustrated in Figure 6.11. Combining Equations 6.33 and 6.26, we obtain the state-space model for the overall KD1S modulator as

$$\begin{aligned} \mathbf{x}[n+1] &= [A_{int}+B_{int}(A-I)C_{int}]\mathbf{x}(n)+B_{int}B\mathbf{U}[n] \\ \mathbf{y}(n) &= CC_{int}\mathbf{x}(n)+D\mathbf{U}[n] \end{aligned} \tag{6.34}$$

Thus, the embedding process on a first-order KD1S modulator results in the ABCD matrix (named $ABCD_1$) to be given as

$$\left[\begin{array}{c|c} A_1 & B_1 \\ \hline C_1 & D_1 \end{array}\right] = \left[\begin{array}{c|c} A_{int}+B_{int}(A-I)C_{int} & B_{int}B \\ \hline CC_{int} & D \end{array}\right] \tag{6.35}$$

The resulting KD1S modulator, after the embedding process, is shown in Figure 6.12. The modified state-space model for KD1S, as specified in Eq. 6.34, has been implemented in Matlab by extending the delta-sigma toolbox functionality. A representative Matlab code for a third order KD1S modulator is presented in Appendix A.1.

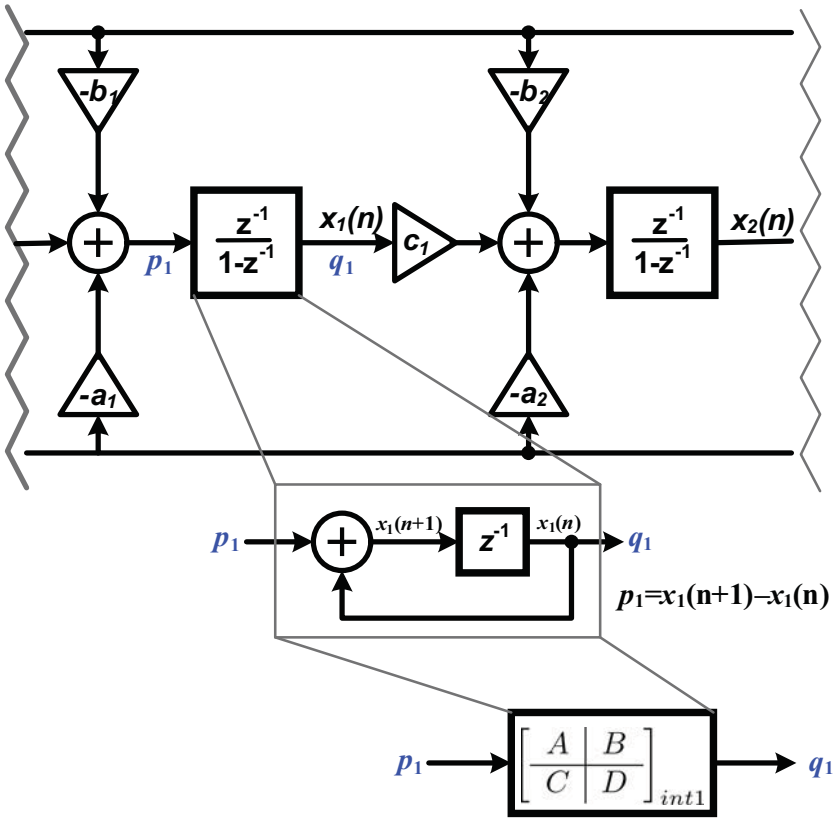

Figure 6.11: Illustration of the state-space embedding method for the non-ideal integrator.

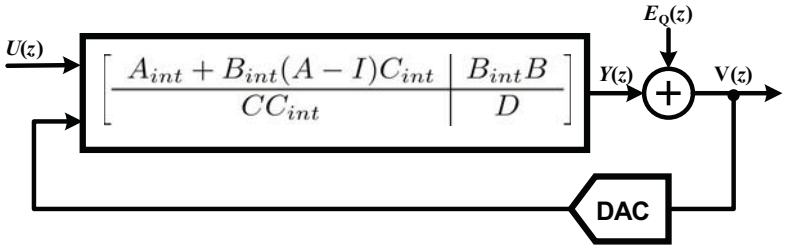

Figure 6.12: The equivalent ABCD matrix representation for a KD1S loop-filter after incorporating the integrator non-idealities.

The quantizer delay is modeled in the toolbox simulation code where a delay of z^{-1} can be inserted. However, fractional comparator delay (i.e. $0 < T_c < T_s/K_{path}$) is not currently implemented as it is difficult to model the effects of a variable quantizer delay in a discrete-time simulation. A method for simulation of excess loop-delay (ELD) effects in continuous-time DSMs has been proposed in [54], which can be ported for KD1S modulators in future. At present, Spectre simulation is recommended on the synthesized KD1S modulator to study the effects of quantizer non-idealities.

6.4.4 Dynamic Range Scaling

Dynamic range scaling (DRS) is an important step when designing practical delta-sigma modulators. In DRS, the ABCD matrix of the loop-filter is scaled so that the individual state maxima are bounded by a specified limit x_{lim}. The value of x_{lim} is selected such that the op-amp outputs lie within the $x_{lim} \cdot V_{DD}$ range and linear operation of the loop-filter is assured. This value is usually selected to be around 0.5 to 0.7 depending upon the op-amp design. The maximum stable amplitude (u_{max}) is also obtained as a result of this scaling process. In the range scaling process, first the ratios $r_i = \frac{x_{max,i}}{x_{lim}}$ of the state maxima $x_{max,i}$ to x_{lim} are estimated through simulations. Then, the diagonal scaling matrix S is formed with the inverse these ratios and is given as [25]

$$S = \begin{bmatrix} \frac{1}{r_1} & 0 & \cdots & 0 \\ 0 & \frac{1}{r_2} & \cdots & \vdots \\ \vdots & \vdots & \ddots & 0 \\ 0 & \cdots & 0 & \frac{1}{r_M} \end{bmatrix} \tag{6.36}$$

Then S is applied on the state vector to obtain the scaled state vector $\mathbf{x_s} = S\mathbf{x}$. This ensures that all the states are bounded within x_{lim}. The resulting ABCD matrix after range scaling is given by

$$ABCD_s = \left[\begin{array}{c|c} SAS^{-1} & SB \\ \hline CS^{-1} & D \end{array}\right] \tag{6.37}$$

The above described range scaling process is illustrated in Figure 6.13 where a single state in the loop-filter is range scaled by r.

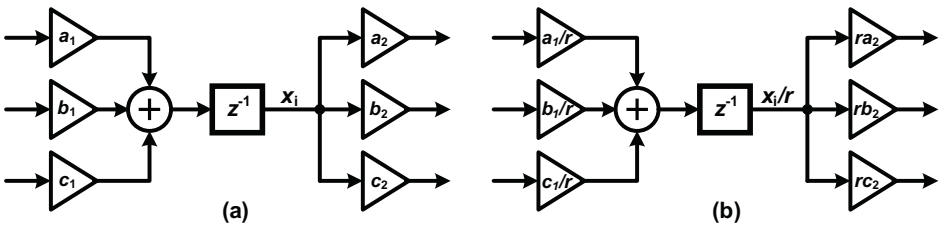

Figure 6.13: Dynamic range scaling of a loop-filter state from x_i to x_i/r.

6.4.5 Mapping to a Loop-filter Architecture

To summarize the synthesis procedure developed in the chapter, the process of designing a generalized higher-order KD1S modulator can be summarized as follows:

1. Using the modified delta-sigma toolbox, synthesize a NTF zero optimized, single-path modulator for a given order with an effective oversampling ratio equal to $K_{path} \cdot OSR$.

2. Apply dynamic range scaling on the *ABCD* matrix of the synthesized loop-filter to restrict the loop-filter states to x_{lim}.

3. Map the scaled *ABCD* matrix to either CIFB or CIFF modulator topology.

4. Find the $ABCD_{int}$ matrix to represent all the K-path SCIs in the loop-filter.

5. Use the $ABCD_{int}$ matrix to find the overall *ABCD* matrix for the KD1S modulator (i.e. $ABCD_1$) using Eq. 6.34.

6. Simulate the modulator with the loop-filter defined by $ABCD_1$. If the simulated integrator states exceed x_{max}, revisit Step 2 with a lower value of x_{max}.

7. Using simulations, estimate the effective gain of the quantizer (k_q) employed in the modulator as $k_q = \frac{E[|y|]}{E[y^2]}$.

8. Evaluate the NTF and STF for the synthesized KD1S modulator using the estimated k_q value.

9. Plot their pole-zero plot (root locus) and simulate the modulator to test for its stability.

10. Iteratively adjust the f_{un} of the op-amps to optimize the power consumption and stability of the designed KD1S modulator.

6.5 Simulation Results

In order to demonstrate the efficacy of the higher-order KD1S modulator synthesis procedure, outlined in the last section, a second-order CIFB and a third-order CIFF KD1S modulators with NTF zero optimization have been synthesized. For these modulators a $K_{path} = 8$ paths are employed with an effective oversampling ratio of $K_{path} \cdot OSR = 64$. An 8-phase clock operating at a frequency of $f_s = 100MHz$ is used which results in an effective sampling frequency $f_{s,new} = 800MHz$. Here, the signal bandwidth in equal to 6.25 MHz. The comparators in the quantizer are assumed to be able to settle completely in $T_s/K_{path} = 1.25ns$ with negligible small-input metastability. However, the unity gain frequency of each of the op-amps is constrained to a small multiple of the clock frequency f_s.

6.5.1 A Second-order CIFB KD1S Modulator with NTF Zero Optimization

A second-order NTF-zero optimized CIFB KD1S modulator block diagram is shown in Fig. 6.14. The synthesis procedure described in the last section is applied to obtain the loop-filter parameter vectors **a**, **b**, **c** and **g**. Here $a_1 = 0.125$, $a_2 = 0.1$, $b_1 = 0.125$, $c_1 = 0.223$, $c_2 = 7.66$ and $g_1 = 0.04 \approx 0$. For this design, the op-amp gain-bandwidths are chosen to be equal to $3f_s = 300MHz$). The design is dynamic range scaled so as to bound the integrator state within $x_{lim} = 0.6$ times the supply voltage. The simulation results for the designed modulator are illustrated in Fig. 6.15. The simulation shows an SNDR equal to 73.7 dB or a resolution of 11.94 bits. The maximum stable amplitude was found to be equal to $u_{max} = 0.96$.

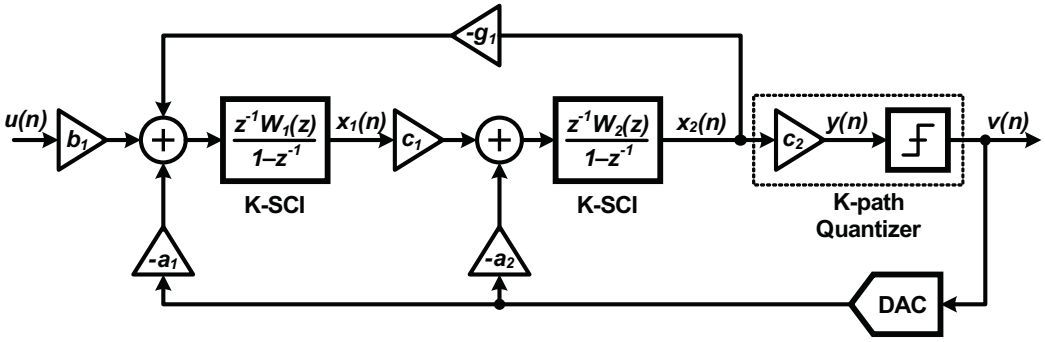

Figure 6.14: The synthesized second-order, single-bit, NTF-zero optimized CIFB KD1S modulator.

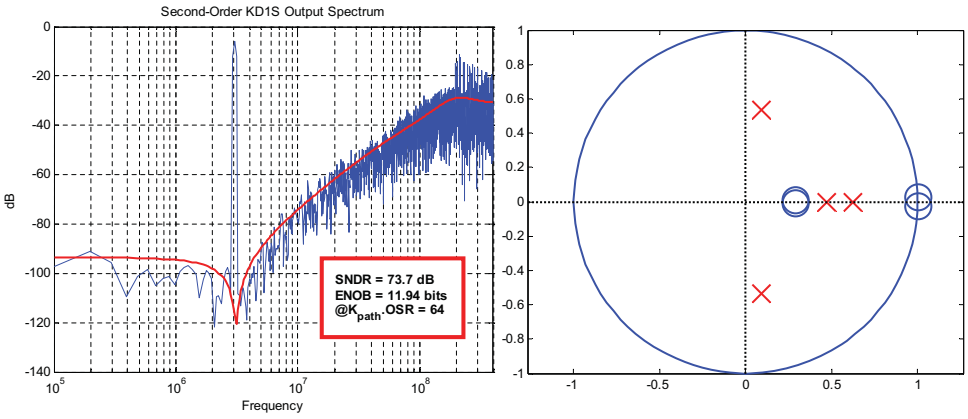

Figure 6.15: Simulated PSD of the output and the NTF pole-zero plot for the second-order CIFB-type KD1S modulator. Here, $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz, $OSR = 8$, and $BW = 6.25$ MHz.

In order to verify the conformance of the state-space model with the real circuit implementation, the second-order KD1S modulator was implemented using switched-capacitors and with an op-amp $f_{un} = 300\,MHz$ and gain $A_{OL} = 60\,dB$ (see Fig. 6.16). The resulting Spectre simulation results are illustrated in Fig. 6.17. The resulting noise transfer function, with finite op-amp gain-bandwidth, is very close to the analytical modeling and results in 12-bits of resolution.

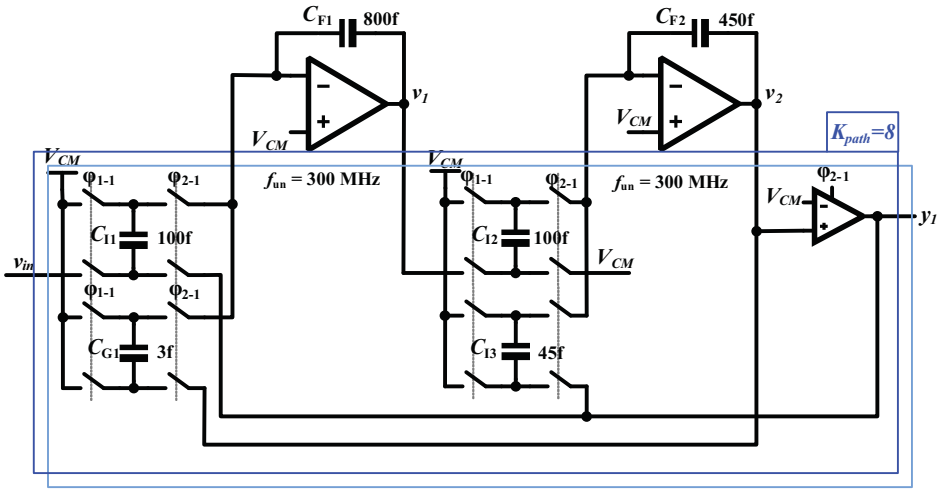

Figure 6.16: A concise representation of the singly-ended, switched-capacitor implementation of the second-order KD1S modulator seen in Fig. 6.15.

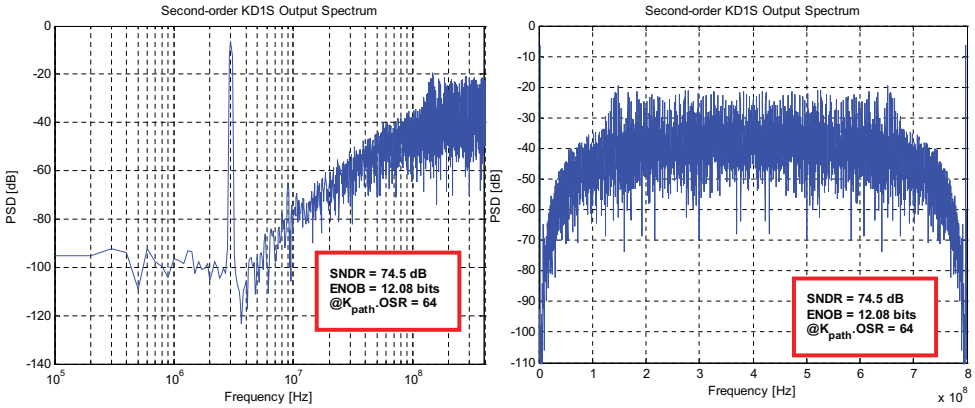

Figure 6.17: Spectre simulated spectrum for the second-order KD1S modulator implemented with switched-capacitors and f_{un} limited op-amp (log and linear frequency axes). Here, $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz, $OSR = 8$, and $BW = 6.25$ MHz.

6.5.2 A Third-order CIFF KD1S Modulator

Feed-forward type (CIFF) modulators have been widely employed to realize wide-band (low-OSR) data-conversion with lower signal distortion. However the CIFF topologies require a fast, low-distortion adder at the input of the quantizer [23]. A third-order

KD1S modulator has been synthesized and illustrated in Fig. 6.18 to further demonstrate the synthesis algorithm. Here $a_1 = 2.85$, $a_2 = 2.85$, $a_3 = 2.35$, $b_1 = 2.8$, $b_4 = 1$, $c_1 = 0.28$, $c_2 = 0.36$, $c_3 = 0.18$ and $g_1 = 0.008 \approx 0$. In order to stabilize the modulator the op-amps are designed with a gain-bandwidth equal to $5f_s = 500\,MHz$ to keep the poles well within the unit circle.

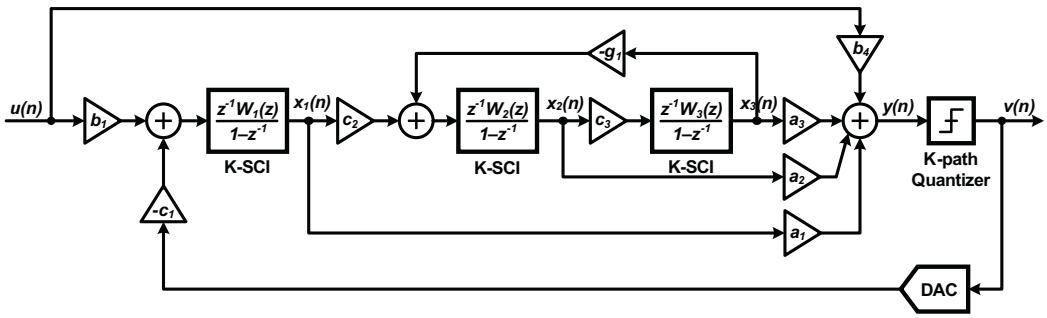

Figure 6.18: The synthesized third-order, single-bit CIFF KD1S modulator.

The simulation results for the third-order modulator show an SNR equal to 77.3 dB or a resolution of 12.55 bits. The maximum stable amplitude was estimated to be equal to $u_{max} = 0.84$. Note that the NTF poles are closer to the unit circle and for low quantizer gain, may move out and thus render the modulator unstable.

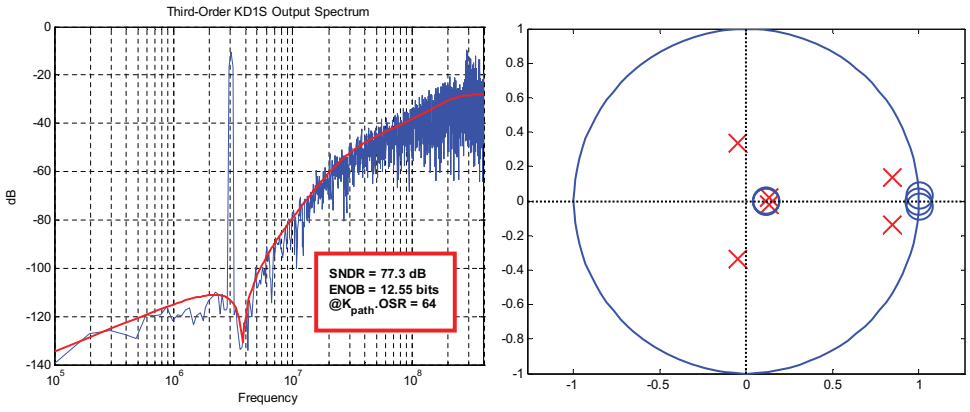

Figure 6.19: Simulated output PSD and the NTF pole-zero plot for the third-order CIFF-type KD1S modulator. Here, $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz, $OSR = 8$, and $BW = 6.25$ MHz.

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6.6 Comparison with conventional DSMs

Table 6.1 compares the contemporary Delta-Sigma modulator topologies with the KD1S modulator topology. An attempt has been made to relate process, transistor transition frequency (f_T) to the maximum attainable sampling frequency. The expressions and values for the continuous-time DSM are from [48]. Here, the increase in number of bits N_{inc} with K_{path} and OSR is assuming that the quantizer delay is small compared to T_s/K_{path}.

It must be noted that due to the irregular NTF spectrum of the KD1S, cascading (or MASH-ing) of KD1S stages is difficult. This is due to the fact that it is untenable to design the noise cancellation filter (NCF) for the NTF response with irregular ripples. However, further time-interleaving or cross-coupling of KD1S modulators is possible due to the switched-capacitor implementation. Moreover, since the KD1S modulator employs a single-bit (time-interleaved) quantizer, the stability of the third or higher-order KD1S with inherently large variation in quantizer gain is an important concern.

Table 6.1: Comparison of the KD1S Modulator with DT- and CT-DSMs.

	Discrete-time DSM	**Continuous-time DSM**	**KD1S Modulator**
Output code rate	f_s	f_s	$f_{s,new} = K_{path} f_s$
N_{inc} **(ideal)**	$(M+0.5)log_2(OSR)$	$11.5+0.5log_2(OSR)$	$(M+0.5)log_2(K_{path} \cdot OSR)-1$
Op-amp f_{un} **requirements**	$2.5f_s$ to $5f_s$ (90% to 99% SC settling)	$\simeq f_s$	$\frac{3}{8}f_{s,new}$ to $\frac{5}{8}f_{s,new}$ (99% settling in $T_s/2$ interval)
$f_{s,max}$ **is limited by**	Op-amp f_{un}: $\approx \frac{f_T}{50}$	Excess loop delay and modulator stability: $\approx \frac{f_T}{20}$	Only comparator delay and metastability: GHz sampling possible.
Frequency scalability	Good	Poor, need to adjust feedback coefficients	Good
Stability	Good	Good with multi-bit quantizer	Good for 2^{nd} order, single-bit quantizer problematic for higher-order designs
Clock jitter sensitivity	Insensitive to clock jitter	Sensitive to clock jitter	Low sensitivity to clock jitter
Process variation	Ratio of Capacitors: < 0.1%	RC time constant: 30%	Ratio of Capacitors: < 0.1%
Inherent AAF	No	Yes, $L_0(s)$ acts like AAF	No
Power Consumption	High	Low	Low
Delay Allocation	Easy	Complicated	Moderate
Parallel and Cross-coupled Designs	Possible	Difficult	Possible
MASH Topology	Easy	Difficult, noise leakage issues	Difficult, tough to design noise cancelling filter
Clocking	Two non-overlapping clocks	Simple clocking	K_{path} non-overlapping phases
Path mismatch and Phase skew	Absent. Leads to noise folding when using double-sampling	Absent	Capacitor mismatches and phase skew lead to noise folding into signal band
Timing issues	None as long as the integrators in the modulator settle	Excess loop delay issues, may need to adjust filter coefficients	Minimal as long as comparator delay is smaller than $1/2f_{s,new}$.

6.7 Conclusion

A novel state-space based synthesis method has been proposed to realize higher-order KD1S modulators with any generalized topology. This method enables rapidly synthesis wideband KD1S modulators without designing their circuit level implementation and then simulating them to determine their stability. Second- and third-order feedback and feed-forward type KD1S modulators are designed to demonstrate the proposed synthesis method.

CHAPTER 7 CHIP DESIGN AND TESTING

7.1 Introduction

This chapter presents the design of the prototype chips used to evaluate the performance of the KD1S modulators presented in the earlier chapters. The prototype chips were implemented using On Semiconductor's 500-nm CMOS technology with a minimum drawn length of 600-nm for NMOS and PMOS operating at a nominal supply voltage of 5 V. The threshold voltages for the NMOS and PMOS are 880 mV and 925 mV respectively. This process provides 3- metal layers for routing and features poly1-poly2 capacitors with a density of 2.5 $fF/\mu m^2$. The fabricated chips contain single-ended first- and second-order KD1S modulators. The KD1S modulators on the chips employed multi-phase non-overlapping clock generation circuits. The design of the circuit blocks employed in the KD1S modulator chips are described below.

7.2 Delay-Locked Loop for Multi-phase Clock Generation

A delay-locked loop (DLL) is employed for generation of multiple clock phases which are equally spaced in time. The block diagram of the DLL is shown in Figure 7.1. The DLL employs a negative feedback loop that keeps the input reference clock CLK_{in} (with phase ϕ_{in}) synchronized with the delayed clock CLK_{out} (with phase ϕ_{out}). The phase frequency detector (PFD) in the feedback loop compares the input and output

clock phases and outputs 'UP' or 'DN (i.e. Down)' digital signals depending whether the rising edge of the clock input (CLK) leads or lags the delayed clock input (DCLK). The UP and DN outputs of the PFD are combined using a charge pump (CP) and low-pass filtered (or averaged) using the loop-filter. The output of the loop-filter controls the delay in the voltage-controlled delay line (VCDL).

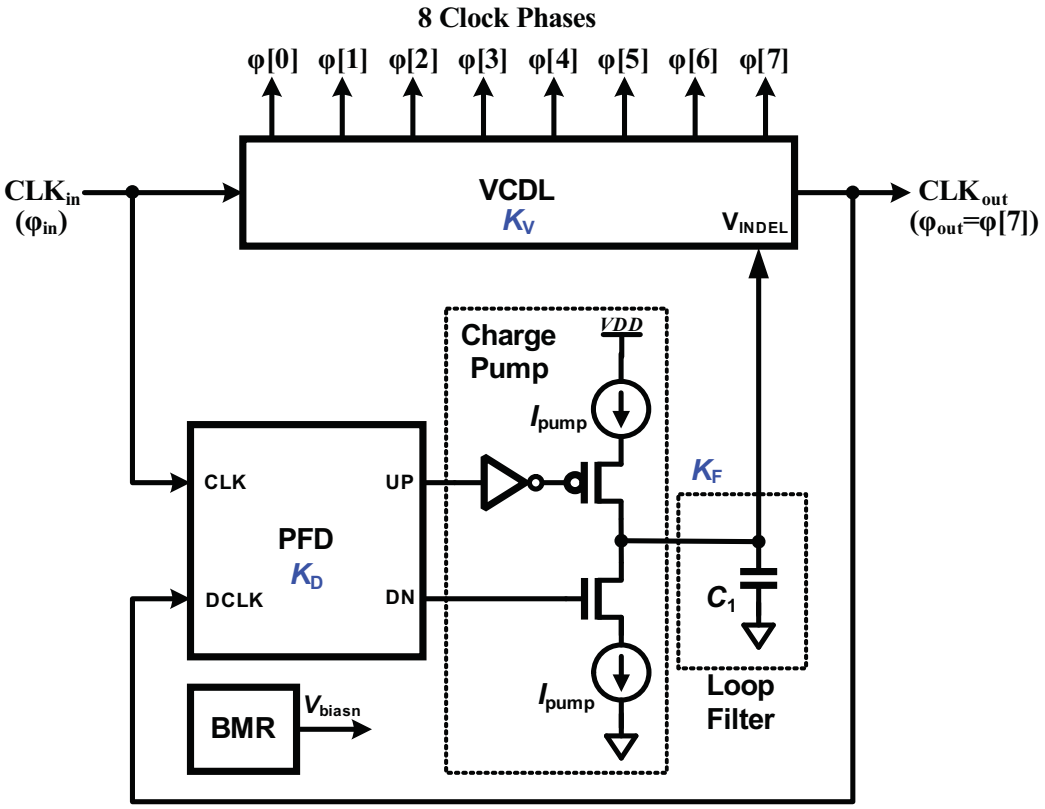

Figure 7.1: Block diagram of the delay-locked loop (DLL) used for multi-phase clock generation.

The input clock (CLK_{in}) is delayed using a VCDL by time t_0 until the output phase ϕ_{out} is synchronized with the input phase ϕ_{in}. The large loop-gain of the feedback loop forces the phase error $(\phi_{in} - \phi_{out})$ to be close to zero which results in the phases ϕ_{in} and ϕ_{out} to be perfectly aligned. After synchronization is achieved, the delay in the VCDL

is equal to the time-period of the input clock i.e. $t_0 = T_{clk}$, where T_{clk} is the time-period of the input clock. The VCDL is comprised of eight identical delay elements in series and thus after synchronization, the delay across each of the delay elements is equal to $\frac{T_{clk}}{8}$. These delayed clock phases tapped from the VCDL form the 8-phase clock with the clock phases $\phi[0:7]$ that are equi-spaced in time [46].

Since the DLL uses a VCDL as opposed to a VCO (voltage-controlled oscillator), the resulting jitter in clock phases due to the phase noise of the VCO is avoided. Also, when using a VCO, the power and supply ground noise modulate the oscillation frequency which leads to a significant amount of clock jitter. This can be understood by the fact that the clock phase is an integral of the frequency and any variation in the VCO frequency will cause larger variation in the phase. On the other hand, VCDL is less susceptible to supply noise induced jitter than a VCO as the supply noise linearly modulates the phase and the corrupted clock edges (zero crossings) disappear at the end of the delay line instead of being recirculated into the loop [46].

The output phase ϕ_{out} is related to the input phase ϕ_{in} to the VCDL as

$$\phi_{out} = \phi_{in} + \frac{2\pi t_0}{T_{clk}} = \phi_{in} + \omega_{clk} t_0 \tag{7.1}$$

where $\omega_{clk} = \frac{2\pi}{T_{clk}}$. The delay, t_0, offered by the VCDL is related to its analog control voltage (V_{indel}) as

$$t_0 = K_V \cdot V_{indel} \tag{7.2}$$

where K_V is the VCDL gain. The gain of the PFD with the charge pump output is given by

$$K_D = \frac{I_{pump}}{2\pi} \tag{7.3}$$

where I_{pump} is the bias current in the charge pump current source and sink. The loop-filter is formed with a capacitor (C_1) with a transfer function given by [46].

$$K_F = \frac{1}{sC_1} \tag{7.4}$$

The transfer function of the DLL relating its input and output phases is

$$\begin{aligned} \frac{\phi_{out}}{\phi_{in}} &= \frac{1}{1+K_D K_F K_V \omega_{clk}} \\ &= \frac{1}{1+\frac{I_{pump}}{2\pi}\frac{1}{sC_1}K_V \omega_{clk}} \\ &= \frac{s}{s+K_V \frac{I_{pump}}{C_1 T_{clk}}} \end{aligned} \tag{7.5}$$

which is a first-order response. If there is a step change in the input clock phase given by $\frac{\Delta\phi_{in}}{s}$, then the change in the output phase of the DLL is given by

$$\triangle\phi_{out} = \frac{\triangle\phi_{in}}{s+\frac{K_V I_{pump}}{C_1 T_{clk}}} = \frac{\triangle\phi_{in}\cdot\tau}{1+s\tau} \tag{7.6}$$

where τ is the time-constant of the first-order loop. The time taken for the DLL to respond to the step in phase is

$$T_r = 2.2\tau = 2.2\cdot\frac{C_1 T_{clk}}{K_V I_{pump}} \tag{7.7}$$

which means that the DLL takes $2.2\frac{C_1}{K_V I_{pump}}$ clock cycles to lock. The DLL response time can be reduced by decreasing the ratio $\frac{C_1}{I_{pump}}$ which will increase the ripple in the VCDL

control voltage and hence causing larger clock jitter. This presents a fundamental trade-off between the DLL response time and the output clock jitter [46]. The individual blocks employed in the DLL are described in the following sub-sections.

7.2.1 Phase Frequency Detector (PFD)

A block diagram of the phase frequency detector (PFD) is shown in Figure 7.2. The outputs of the PFD depend upon both the phase and frequency difference of the inputs. The PFD essentially compares the rising edges of the clock (CLK) and the delayed version of the clock (DCLK). If the rising edge of CLK leads the rising edge of DCLK, the UP output goes high and the DN output stays low. Conversely, if the rising edge of CLK lags the rising edge of DCLK, the DN output goes high and the UP output stays low. Both the outputs stay low when the DLL is locked and the rising edges of CLK and DCLK are very close. Thus there is no ripple in the VCDL control voltage when the DLL is in lock condition. Also, the PFD doesn't allow the DLL to lock on the harmonics of CLK [46].

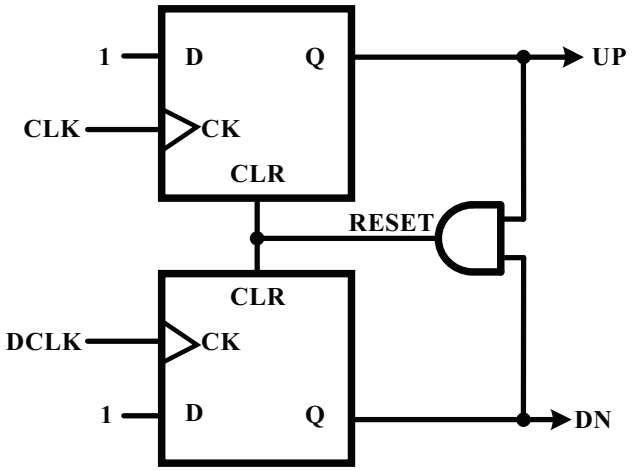

Figure 7.2: Block diagram of the phase frequency detector (PFD).

A CMOS implementation of the PFD seen in Figure 7.2 is presented in Figure 7.3. The PFD comprises of two SR latches with clear and a reset logic. When the rising edges of CLK and DCLK move close together, then the outputs of the PFD shows small glitches. The delay through the two inverters in the PFD determines if the outputs are glitch free when the PFD inputs move close together. However, a large delay will lead to static phase error as the outputs will not respond unless the input phases are separated by large enough delay [46].

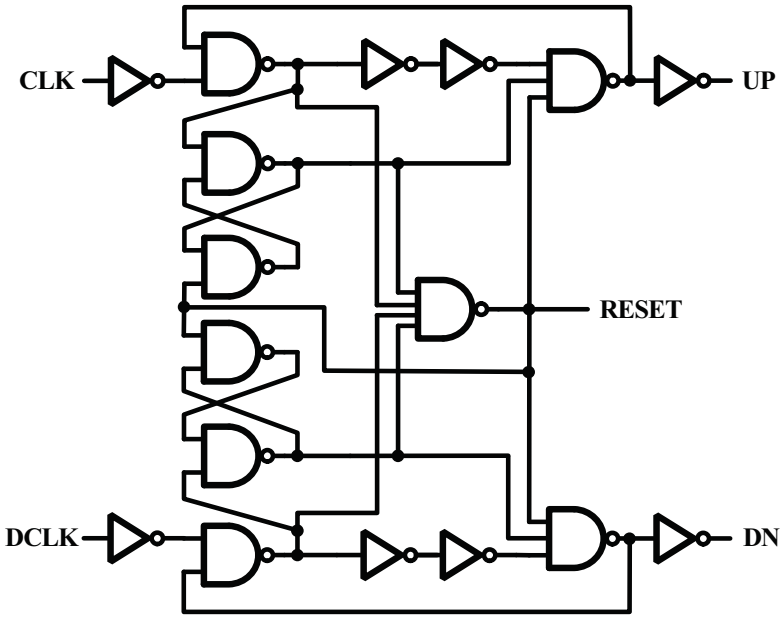

Figure 7.3: CMOS implementation of the PFD seen in Figure 7.2.

The operation of the designed PFD is demonstrated using the simulation results shown in Figure 7.4. Here, when CLK leads DCLK, the UP output goes high and when CLK lags DCLK, DN output goes high. When CLK and DCLK move close together, the outputs exhibit small glitches.

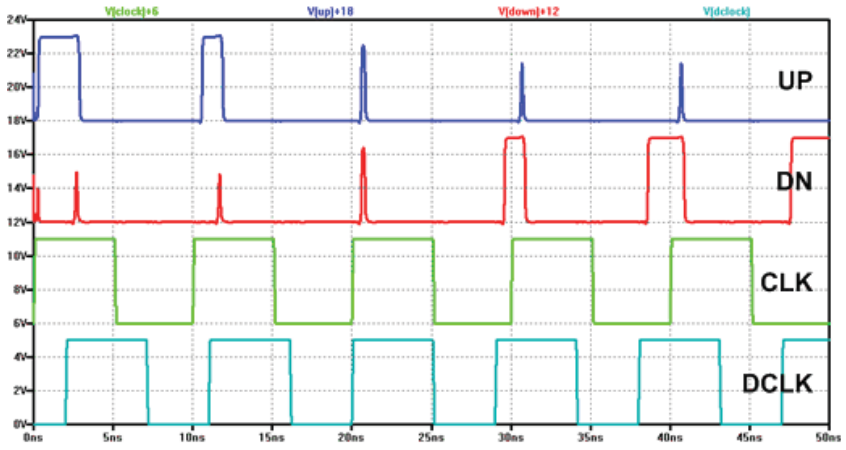

Figure 7.4: Simulation results for the PFD seen in Figure 7.3.

7.2.2 Charge Pump and Loop-Filter

The UP and DN outputs of the PFD are combined into a single analog output using the charge pump topology shown in Figure 7.5. The charge pump output drives the loop-filter formed using a single capacitor ($C_1 = 2.8\,pF$). A bias current of $I_{pump} = 10\,\mu A$ is used for the current source and the sink that pump charge in and out of the loop-filter capacitor.

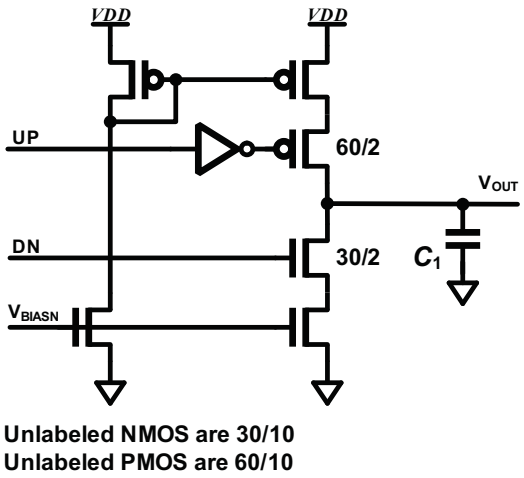

Figure 7.5: Charge pump employed in the DLL.

As seen earlier, the effective gain of the PFD with the charge-pump output is given by $K_D = \frac{I_{pump}}{2\pi} = 1.59 \times 10^{-6} A/rad$ and the loop-filter transfer function is $K_F = \frac{1}{sC_1}$. A self-biased beta multiplier reference (BMR), shown in Figure 7.6, is used for generating the bias voltage V_{biasn} for the charge pump current mirrors.

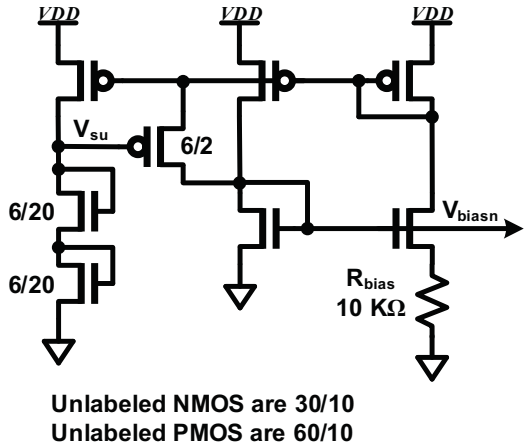

Figure 7.6: The self-biased reference (BMR) used in the DLL.

7.2.3 Voltage-Controlled Delay-Line (VCDL)

The voltage-controlled delay line (VCDL) is the most important component of the DLL. Figure 7.7 illustrates the circuit implementation of the VCDL. The VCDL contains eight delay adjustable inverting stages, each employing a current starved inverter with buffer to drive the output load. Here, single-ended delay stages have been preferred over fully-differential stages in order to avoid the skew introduced by the inverters used to regenerate full logic levels. The delay of each delay stage is adjusted by changing the bias currents by controlling the input V_{INDEL}. A delay bias generator circuit is used to generate the bias levels V_{bp} and V_{bn} for the current mirrors in the current starved inverters in the delay stages. The VCDL has been designed to accommodate an input clock frequency range of 40 MHz to100 MHz. From simulations, the gain of the VCDL was found to be roughly equal to $K_V = 10\,\frac{ns}{V}$ [46].

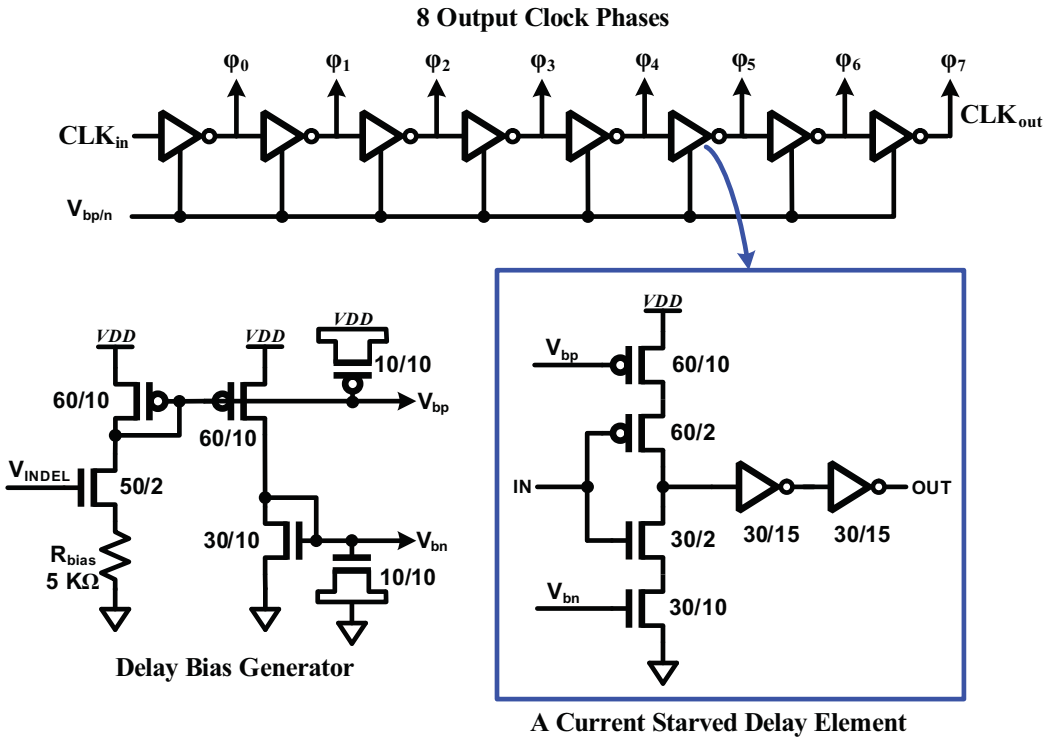

Figure 7.7: The voltage controlled delay-line (VCDL) with the delay bias generator used in the DLL.

7.2.4 Non-overlapping clock generator

A non-overlapping clock generation circuit, shown in Figure 7.8, is used for deriving the four clock phases $\phi_1[i]$, $\overline{\phi_1[i]}$, $\phi_2[i]$ and $\overline{\phi_2[i]}$ from the DLL outputs $\phi[i]$, where $i = 0, 1, ...7$. Note that since the VCDL employs inverting delay stages, the correct multi-phase clock sequence is $\phi[0]$,$\phi[5]$, $\phi[2]$, $\phi[7]$, $\phi[4]$, $\phi[1]$, $\phi[6]$ and $\phi[3]$.

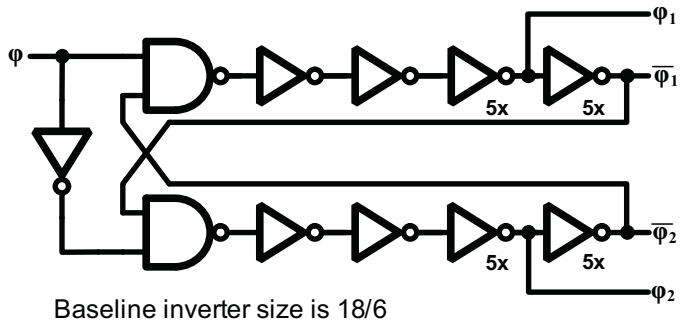

Figure 7.8: The non-overlapping clock generator for generating phases $\phi_1[i]$, $\overline{\phi_1[i]}$, $\phi_2[i]$ and $\overline{\phi_2[i]}$ from the DLL outputs $\phi[i]$, where $i = 0, 1, ...7$.

Figure 7.9 below shows complete eight-phase clock generation block employing the DLL. Eight non-overlapping clock generators are used for each of the eight phases tapped from the DLL.

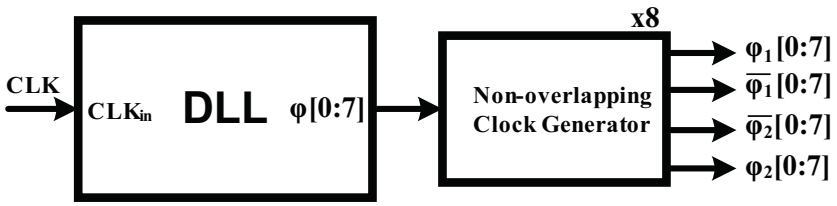

Figure 7.9: The complete DLL based multi-phase clock generation circuit .

The layout of the DLL based clock generator, designed in 500-nm CMOS process, is shown in Figure 7.10. The VCDL and the corresponding non-overlapping clock generators are laid out in a manner which facilitates the symmetric routing of the multi-phase clocks to the modulator with minimum skew due to trace length mismatch. Sufficient amount of bypass capacitors are connected between the supply and ground rails to mitigate the power supply noise and its deleterious effects on the output clock jitter.

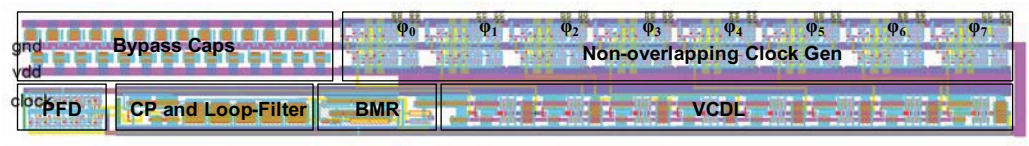

Figure 7.10: Layout of the multi-phase clock generator using a DLL designed in 500-nm CMOS process.

7.2.5 DLL Simulation

Simulation results are shown for the DLL to lock to an input clock frequency of 100 MHz. Figure 7.11 shows the VCDL control voltage (i.e. V_{INDEL}). We can observe that the DLL exhibits first-order settling. The response time of the DLL is calculated as $T_r = 2.2 \cdot \frac{C_1 T_{clk}}{K_V I_{pump}} = 618\,\mu s$ which is equivalent to 35 clock cycles. The simulated response time of the DLL is roughly $710\,\mu s$, which is close to the calculated value. The rms ripple in the VCDL input is $100\,\mu V$ which translates into roughly $800\,fs$ of systematic jitter. However, the contribution to jitter from the device noise and the power supply noise will dominate the jitter in the output clocks.

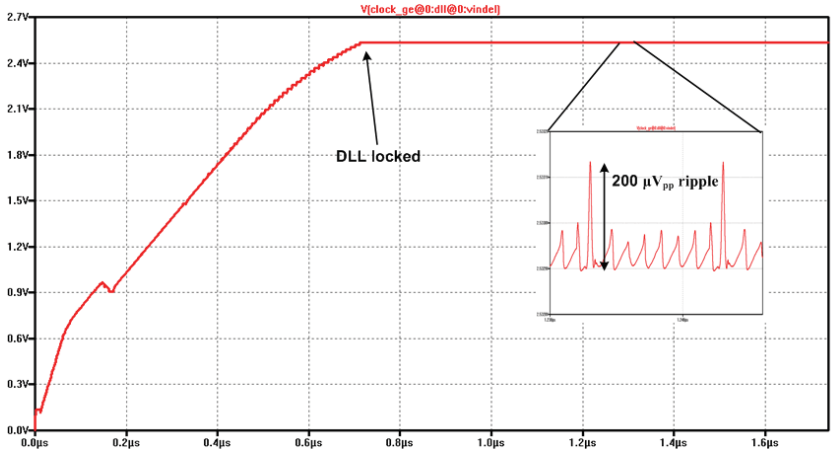

Figure 7.11: Transient simulation of the DLL showing the input of the VCDL (V_{INDEL}). Sub-plot shows the peak ripple in the VCDL input in the locked state.

Figure 7.12 show the eye diagram for the eight output phases of the DLL when locked to an 100 MHz input clock. We can observe that the clock phases are evenly distributed and the perceptible clock jitter is negligible compared to the time-period.

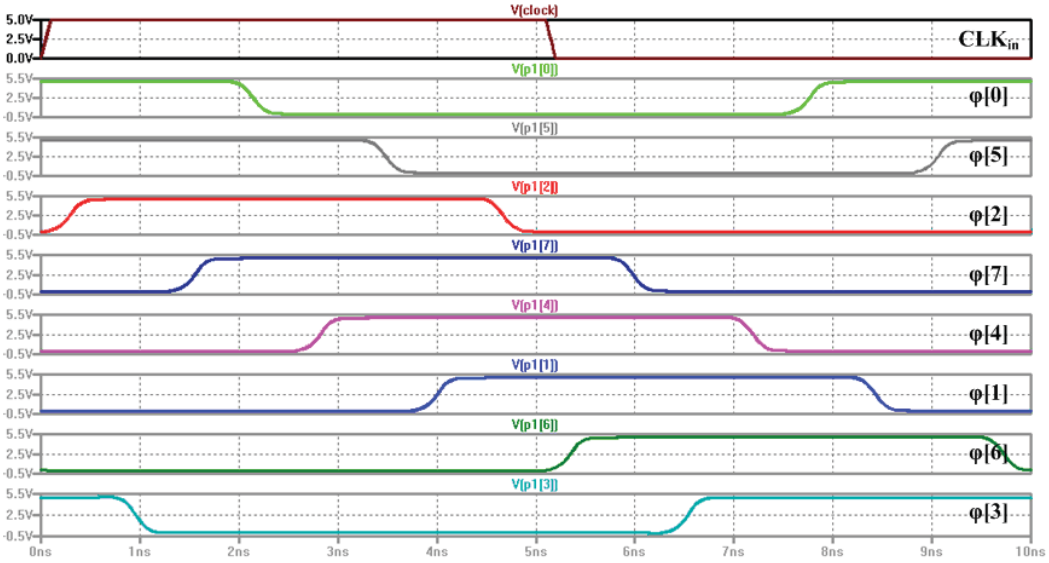

Figure 7.12: Eye diagram for the eight clock phases generated from the DLL in the locked condition. Here the input clock frequency is 100 MHz.

7.3 First-Order KD1S Modulator

Figure 7.13 shows a concise schematic representation of the first-order KD1S modulator designed in a 500-nm CMOS process. The design comprises of a 8-path KD1S modulator employing first-order noise-shaping. A DLL is employed to generate the multi-phase clocks used for time-interleaved sampling in the KD1S modulator [13]. A simple single-ended modulator prototype has been designed to demonstrate the KD1S noise-shaping. A capacitance of $100\,fF$ is employed for the sampling capacitors in the KD1S modulator. As seen in Section 4.5, the kT/C noise for these $100\,fF$ sampling

capacitors in the KD1S topology (with averaging by K_{path}), limits the modulator resolution to roughly 67 dB SNR or 10.8 bits resolution. The synthesis procedure for the first-order KD1S modulator resulted in integrating capacitor of 860 fF Figure 7.13.

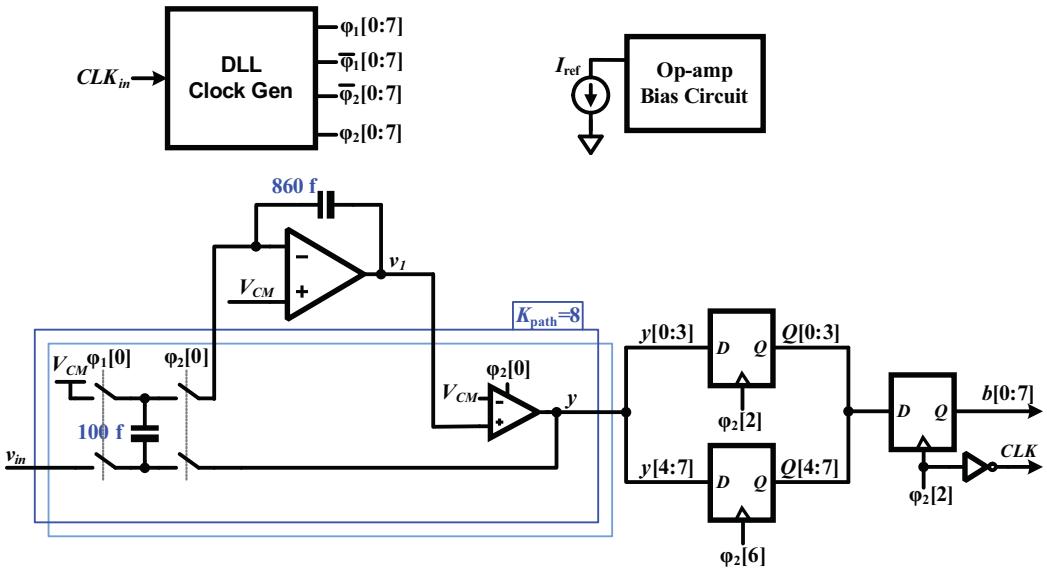

Figure 7.13: A concise schematic representation of the single-ended first-order KD1S modulator with the clock and bias generation circuits.

7.3.1 KD1S Output Synchronization

In order to effectively serialize the K_{path} digital outputs ($b[0:7]$) from the chip, the K_{path} outputs are synchronized with the third phase of the clock (i.e. $\phi_2[2]$) . This synchronization is illustrated in Figure 4.5, where the clock phase $\phi_2[2]$ registers the first four outputs ($y[0:3]$) and the phase $\phi_2[6]$ registers the remaining four outputs $y[4:7]$. This arrangement allows sufficient setup time for each of the paths and avoids flip-flop metastability. The paths are again registered together on the phase $\phi_2[2]$. The phase $\phi_2[2]$ is also delayed to realize the output CLK signal. Thus all the buffered

outputs $b[0:8]$ form a data frame of length $K_{path} = 8$ with the *CLK* signal acting like a frame marking signal. The *CLK* output signal is used to reconstruct the serial data frames when digital processed after data acquisition. The individual circuit blocks are described in the following sub-sections.

7.4 Second-Order KD1S Modulator

Figure 7.14 illustrates a concise schematic representation of the second-order KD1S modulator designed in a 500-nm CMOS process. Again, the second-order design consists of 8-paths clocked using non-overlapping multi-phase clocks derived from a DLL. The design procedure, explained earlier in Chapter 6, was employed to design the modulator in order to achieve bounded states so that the integrators always operate in linear region. Again a single-ended modulator was designed to quickly demonstrate the second-order noise-shaping using a KD1S modulator. A capacitance of $C_{I1} = 100\,fF$ is employed for the sampling capacitors in the first integrator in the modulator, which sets the input referred noise for the whole modulator. The noise contribution from the second stage is attenuated by the large in-band gain of the first integrator and is negligible. From Section 4.5, the kT/C noise for these $100\,fF$ sampling capacitors limits the modulator resolution to roughly 10.8 bits. The sampling capacitors in the second integrator are chosen to be $C_{I2} = 25\,fF$ in order to optimize the power consumption in the second stage op-amp. A third feedback branch with $C_{I3} = 10\,fF$ capacitors is used to set the required feedback gain at the second stage input. The synthesis procedure

for the second-order KD1S modulator resulted in integrating capacitors of 790 fF and 142 fF as shown in Figure 7.14.

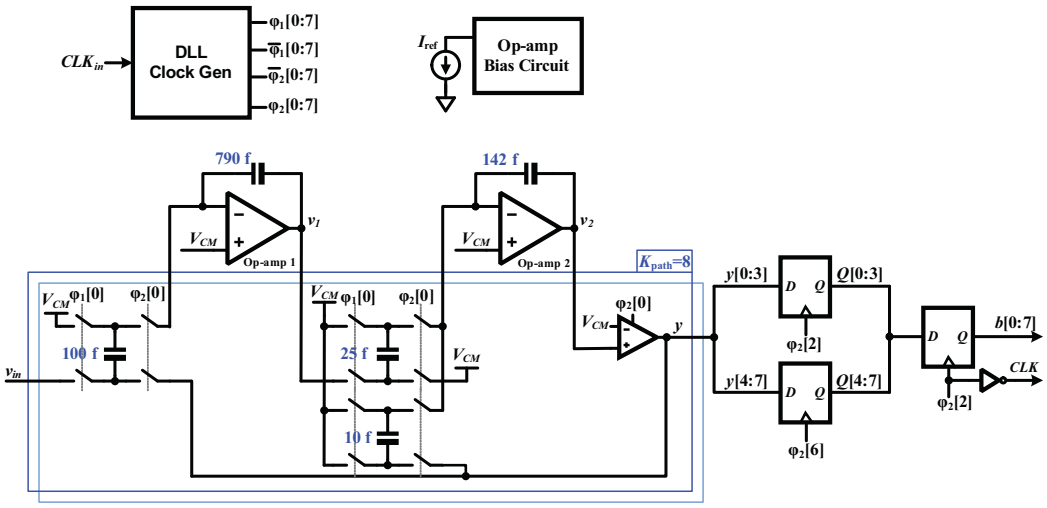

Figure 7.14: A concise schematic representation of the single-ended second-order KD1S modulator with the clock and bias generation circuits.

The 8 outputs of the second-order KD1S modulator have been synchronized similar to the first-order KD1S modulator discussed in Section 7.3.1 earlier.

7.5 KD1S Modulator Circuit Blocks

The first- and second-order KD1S modulators presented in Sections 7.3 and 7.4 use shared circuit-level blocks which are described in this section.

7.5.1 Switched-Capacitors

The delta blocks of the KD1S modulators are implemented using the switched-capacitor shown in Figure 7.15. The transistor sizing for the switch is determined by the transient settling and thermal noise considerations described earlier in Section 4.5. The value

of the sampling capacitance C_I is also set by the kT/C noise considerations. In the prototype KD1S modulator designs, a sampling capacitance value of $100\,fF$ has been selected which limits the resolution to roughly 10.8 bits. Poly1-Poly2 capacitors have been used to realize the $100\,fF$ sampling capacitors. From Section 4.5, the optimal value for the switch resistance is given by $R_{on} = \frac{1}{g_{m_1}}$, where g_{m1} is the transconductance of the first-stage of the op-amp employed in the integrator. This leads the transmission-gate (TG) switch sizing of $\frac{W}{L} = \frac{100}{2}$ for the PMOS as well as the NMOS with an switch on-resistance of $200\,\Omega$. For the first integrator of the second-order KD1S modulator a TG with $\frac{100}{2}$ NMOS and PMOS sizing is used. For the second integrator, a relaxed TG sizing of $\frac{50}{2}$ is employed. For the first-order KD1S modulator design, a TG size of $\frac{50}{2}$ is used to reduce the effects of large parasitic capacitances in the switch.

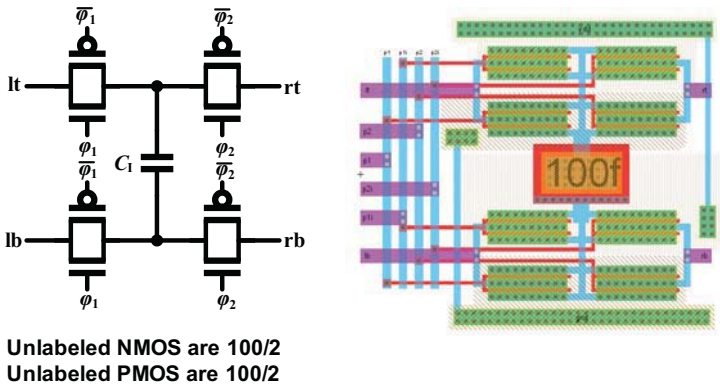

Figure 7.15: Switched-capacitor block with the corresponding layout.

7.5.2 Op-amps and Bias Generation Circuit

In the first- and second-order KD1S modulator prototypes, single-ended op-amps are employed to implement the K-path integrators. Since the first op-amp in the modulator determines the linearity for the whole modulator, larger bias current is used in the first op-amp better slew-rate, noise and settling performance. From Section 4.4, for a KD1S modulator a lower op-amp unity gain frequency f_{un} can be used than the effective sampling rate $K_{path}f_s$. However, the op-amp can not be allowed to slew for the whole time-slice of T_s/K_{path}. The slew-rate requirement on the op-amp is determined by the maximum amount of charge which is transferred from the input capacitors (C_{I1}) to the integrating capacitor (C_{F1}). This charge for partial settling is given by $C_{I1}\alpha_0 V_{DD}$. If we allow 25% of the time-slice for slewing, it requires a bias current of

$$I_{SS1} = 4Kf_sC_{I1}\alpha_0 V_{DD} \tag{7.8}$$

which is equal to 1.6 mA for the modulators designs. Thus, the bias current requirement on the op-amps is set by the slew-rate rather than the f_{un} requirements. For the large amount of bias current in the first stage, in 500-nm CMOS process, it is hard to stabilize a two-stage op-amp. In order to meet the stringent slew-rate requirement with assured stability, simple single-stage op-amps are employed in the KD1S modulators.

Figure 7.16 shows the folded-cascode op-amp used in the first-order KD1S modulator and in the first stage of the second-order KD1S modulator. The op-amp has a total tail bias current of 1.6 mA and has a maximum slew-rate for an effective load of 340 fF

given by

$$SR = \frac{I_{SS}}{C_{L1}} = \frac{1.6mA}{340fF} = 4.7V/ns \tag{7.9}$$

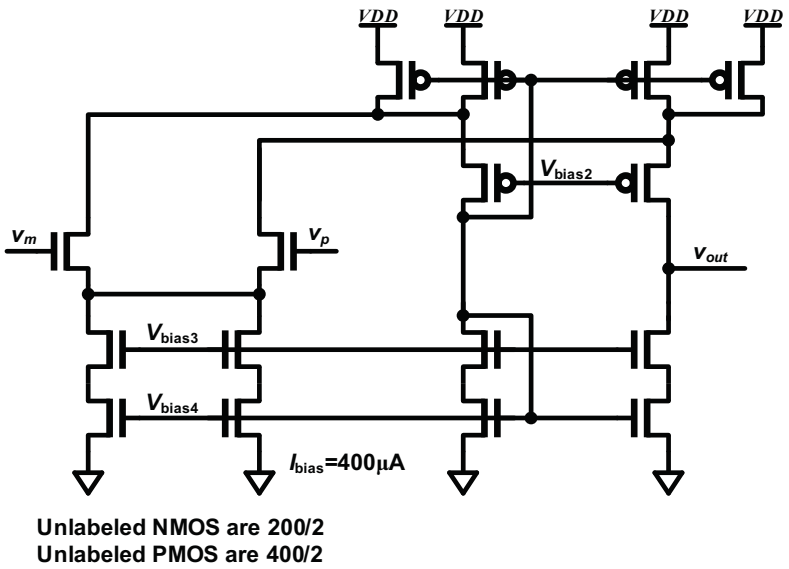

Figure 7.16: Single-ended op-amp employed in the first switched-capacitor integrator.

Figure 7.17 shows the magnitude and phase response for the designed op-amp with 340 fF load. The op-amp exhibits a DC gain of $A_{OL} \approx 44\,dB$, a unity gain frequency of $f_{un} = 940\,MHz$ and a phase margin of $PM = 60$º. The gain of the op-amp is sufficient for an OSR of 64 which requires a minimum op-amp gain of 36 dB.

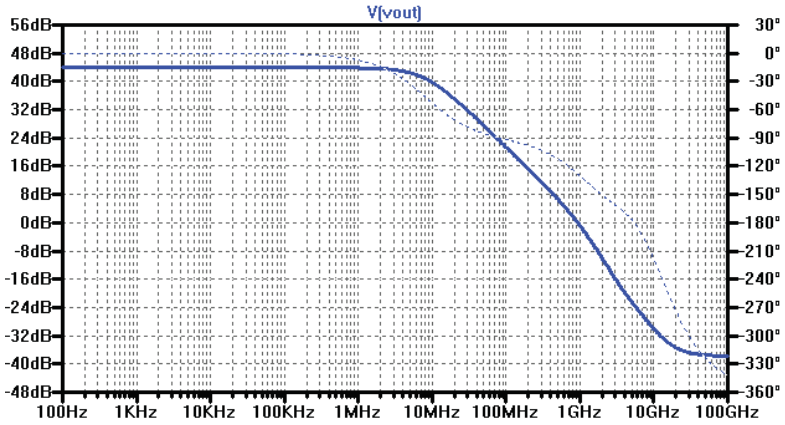

Figure 7.17: Magnitude and phase response of the op-amp seen in Figure 7.16 with 340 fF load. Here, $A_{OL} = 44$dB, $f_{un} = 940$ MHz, and $PM = 60$º.

In the second-order KD1S modulator, the input and the integrating capacitors for the second integrator were scaled down by 4. Thus the slew-rate and requirements on the second op-amp in the modulator are relaxed by 4 times. Figure 7.18 shows the folded-cascode op-amp employed in the second stage of the second-order KD1S modulator. Here a total tail bias current of $400\,\mu A$ is used.

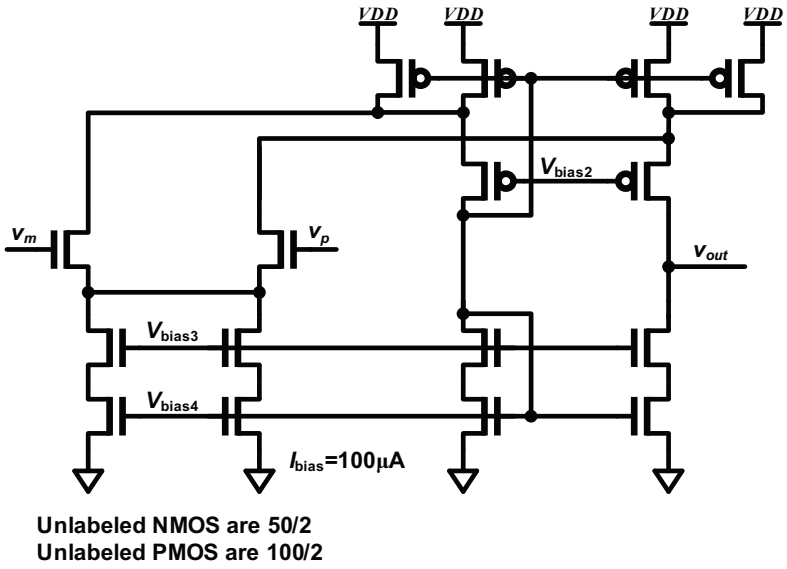

Figure 7.18: Single-ended op-amp employed in the second switched-capacitor integrator.

Figure 7.19 shows the magnitude and phase response for the second op-amp with 200 fF load. The op-amp exhibits a DC gain of $A_{OL} \approx 45\,dB$, a unity gain frequency of $f_{un} = 1.15\,GHz$ and a phase margin of $PM = 58º$.

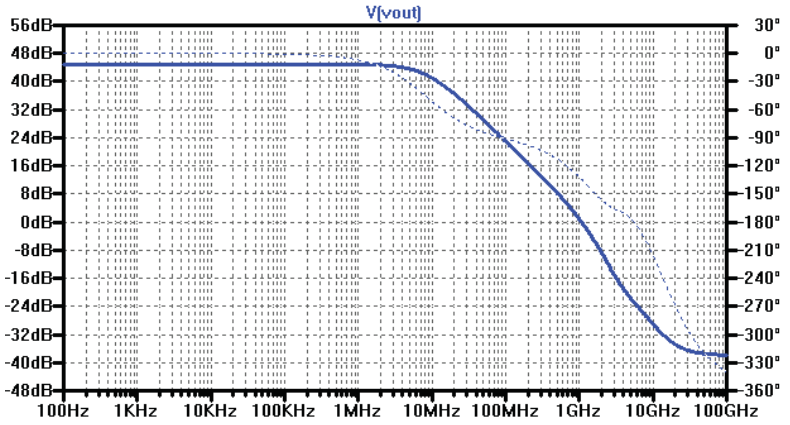

Figure 7.19: Magnitude and phase response of the op-amp seen in Figure 7.16 with 200 fF load. Here, $A_{OL} = 45$dB, $f_{un} = 1.15$ GHz and $PM = 58º$.

The layout of the op-amps employed in the KD1S modulator designs is shown in Figure 7.20.

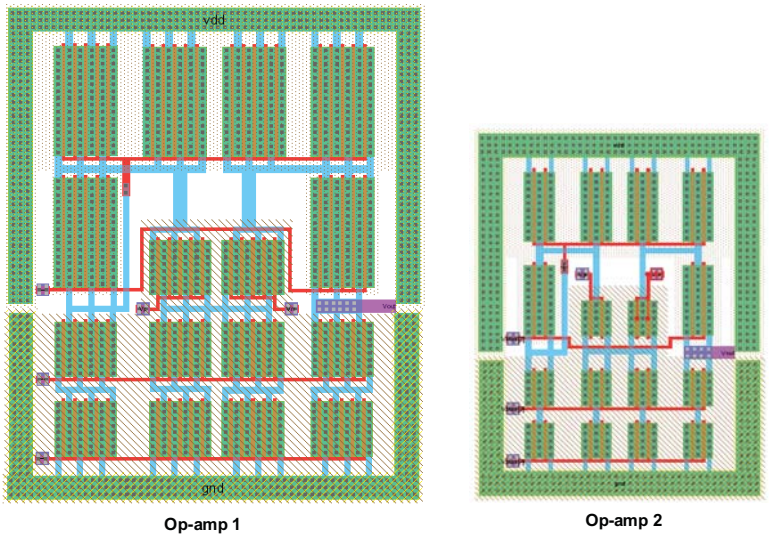

Figure 7.20: Layouts of the op-amps used in the KD1S modulators and designed in 500-nm CMOS.

The bias circuit used for generating the bias references used in the above op-amps is shown in Figure 7.21 [46].

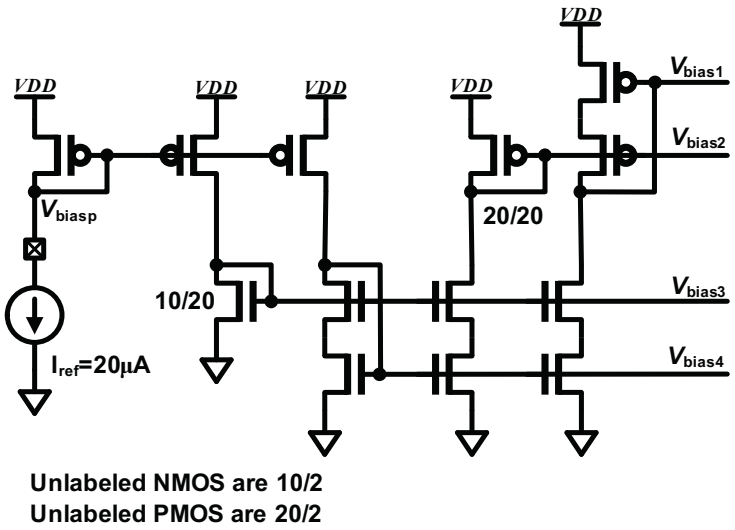

Figure 7.21: Bias generation circuit for the op-amps.

7.5.3 Comparators and Flip-Flop

The clocked comparator used in the KD1S design is shown in Figure 7.22 [13, 55]. A pre-amp is employed in the comparator to increase the gain and thus the resolution of the comparator. The pre-amp is followed by a cross-coupled latch. The comparator regenerates the input signal present at the rising edge of the clock. The top PMOS are used to erase the memory in the latch when the clock goes low. The regenerative latch is followed by a static S-R latch which ensures that the outputs (Q and $\overline{Q}$) change only when the state of the comparator changes. The comparator is designed to drive up to $200\,fF$ load offered by the switched-capacitors. The transistors are sized for minimum delay of the comparator.

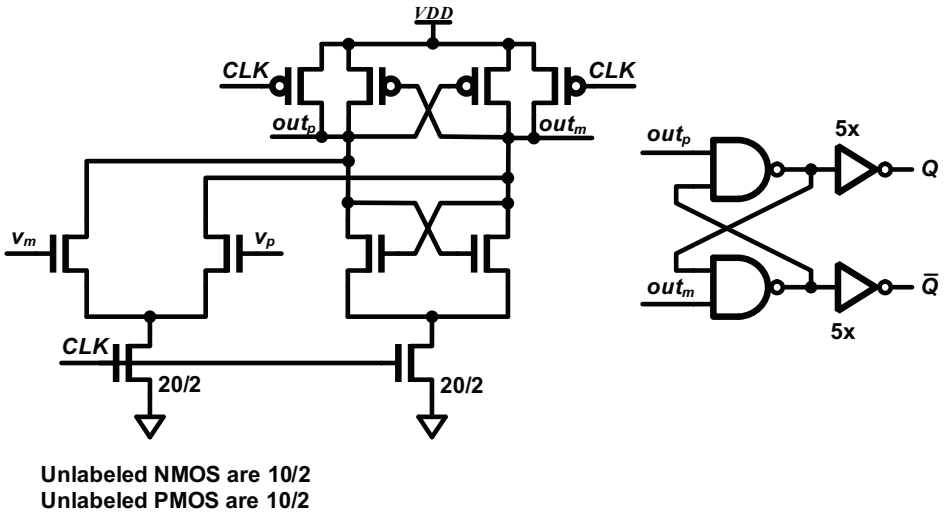

Figure 7.22: The clocked comparator with a static latch.

Figure 7.23 shows the transient simulation of the clocked comparator. For an input signal of 1 mV around the common-mode voltage $V_{CM} = 2.5\,V$, the comparator exhibits

a total delay of roughly 800 ps. This delay varies with the initial input signal used for regeneration.

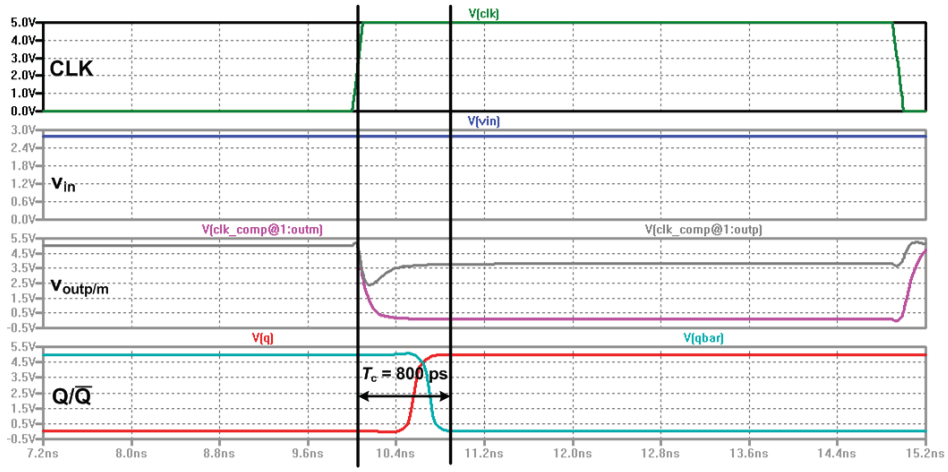

Figure 7.23: Transient simulation of the clock comparator seen in Figure 7.22.

Figure 7.24 shows the layout of the clocked comparator employed in the KD1S modulators.

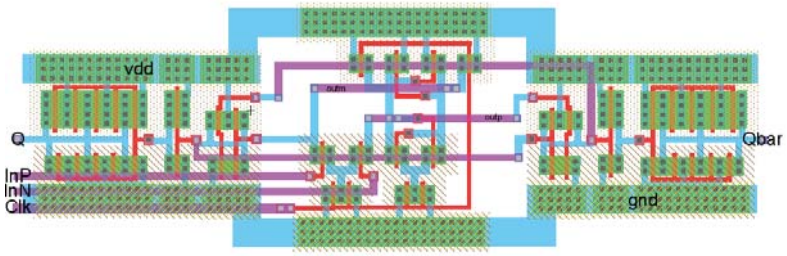

Figure 7.24: Layout of the comparators employed in the KD1S modulators.

For faster operation and smaller layout footprint, true single phase clocking (TSPC) dynamic latches (shown in Figure 7.25) are employed for synchronizing the *K*-path modulator outputs with the output clock [13].

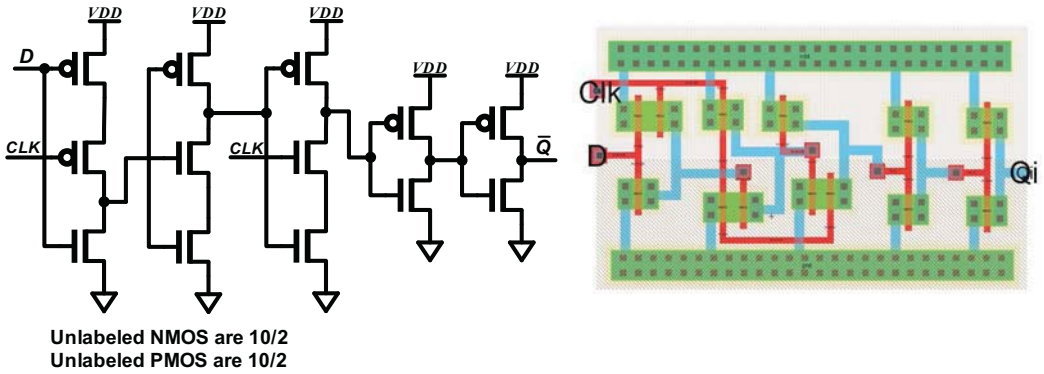

Figure 7.25: Schematic and layout TSPC Latch used for synchronizing the KD1S outputs.

7.6 Chip Layouts

The chips were designed and taped-out using the Electric VLSI CAD system [56]. The layout of the designed first- and second-order KD1S modulators is shown in Figures 7.26 and 7.27. The layout was systematically done using component arrays for a closely packed layout. The multi-phase clocks from the DLL based clock generator have been routed to the switched-capacitors with equal trace length to minimize clock-phase skew.

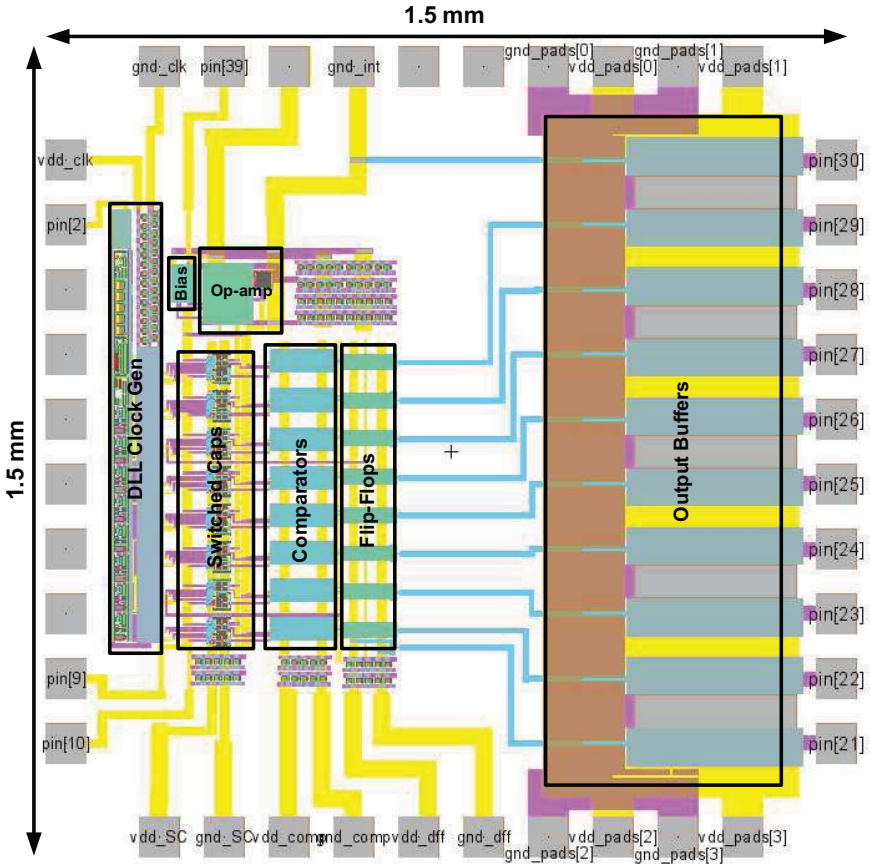

Figure 7.26: Labeled layout of the first-order KD1S modulator design in the 500-nm CMOS process.

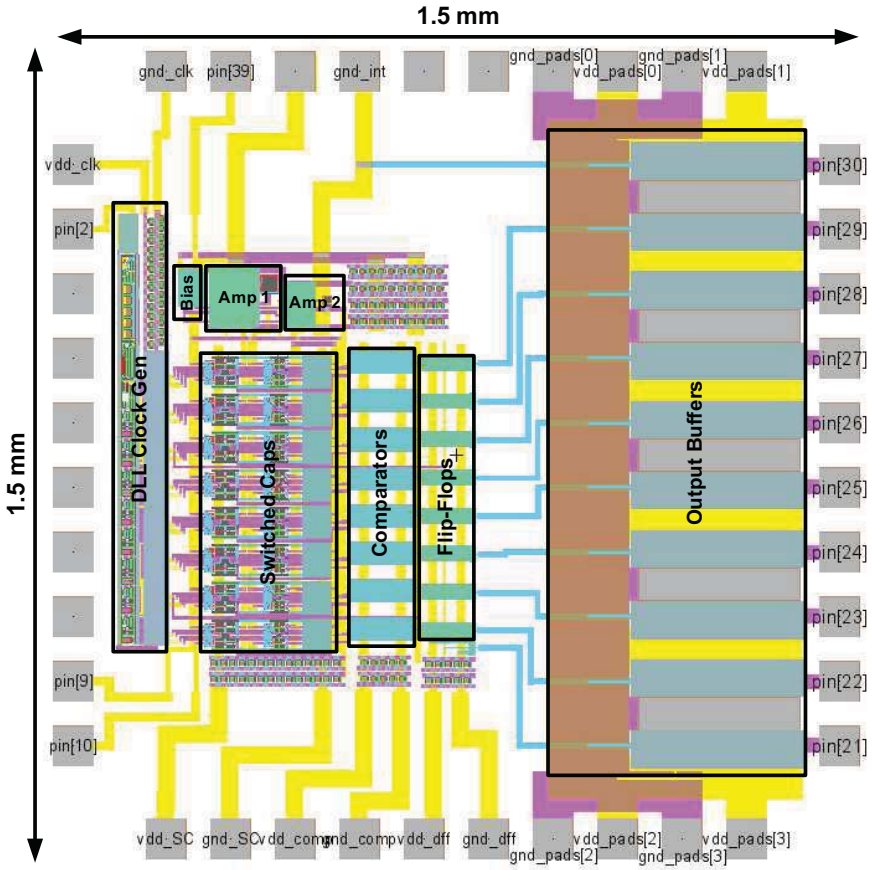

Figure 7.27: Labeled layout of the second-order KD1S modulator design in the 500-nm CMOS process.

In the designed chips, clock buffers sufficient to drive 30 pF off-chip load have been used to for the 8 parallel outputs from the modulator and the reference clock *CLK*. The power and ground pins for all the distinct blocks have been separated and exported using distinct bond pads. MOSCAPs have been amply used between all the local supply and ground rails on the chip to minimize supply and ground noise coupling.

An earlier test-chip micrograph of a second-order KD1S modulator designed in 500-nm CMOS, is shown in Figure 7.28.

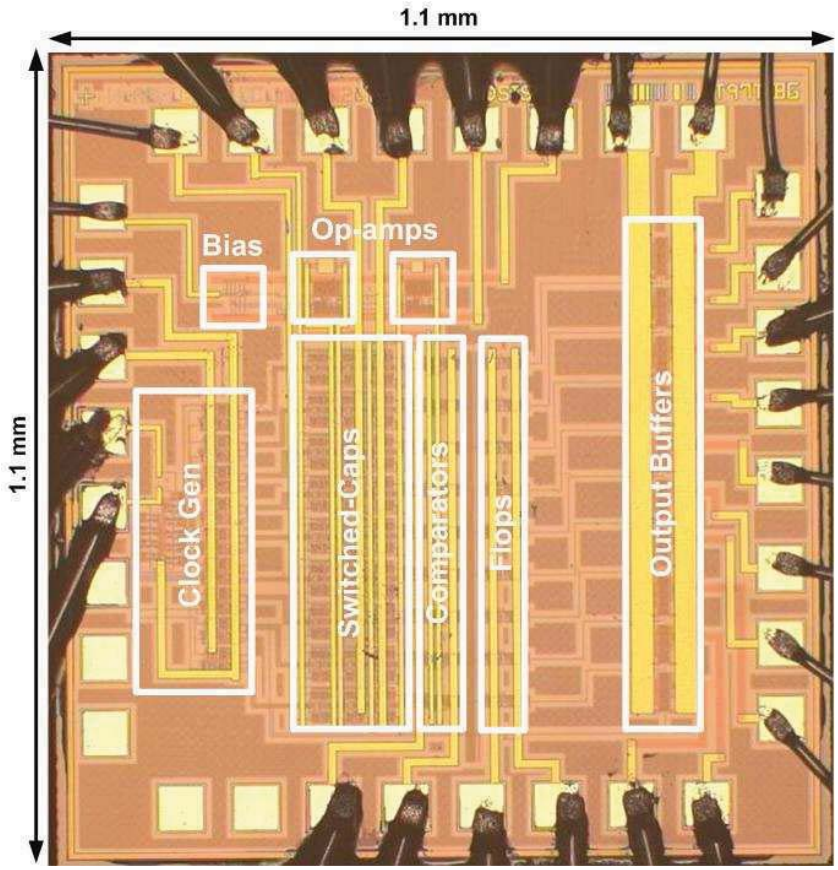

Figure 7.28: Die micrograph for a second-order KD1S test chip designed in 500-nm CMOS process.

7.7 Chip Simulation

7.7.1 First-Order KD1S Modulator

The first-order KD1S modulator, implemented in 500-nm CMOS and described earlier in Section 7.3, was simulated using the SPICE simulator. For the simulation an input clock frequency of 100 MHz is used for the DLL. Since we employ $K_{path} = 8$ paths, the effective sampling frequency set by the sampling phases is equal to 800 MHz. A sinusoidal input of $2V$ amplitude and 2.67 MHz frequency is applied to the modulator.

The effective signal bandwidth for this simulation is equal to $f_B = 6.25$ MHz. The digital outputs from the simulated chip are re-sampled and processed using the MATLAB code shown in Appendix A.2. The received digital outputs of the KD1S modulator are shown in Figure 7.29 below. The plot shows the serial mode-output (v_{out}) with $K_{path}f_s$ rate and the parallel-mode decimated output with f_s data rate.

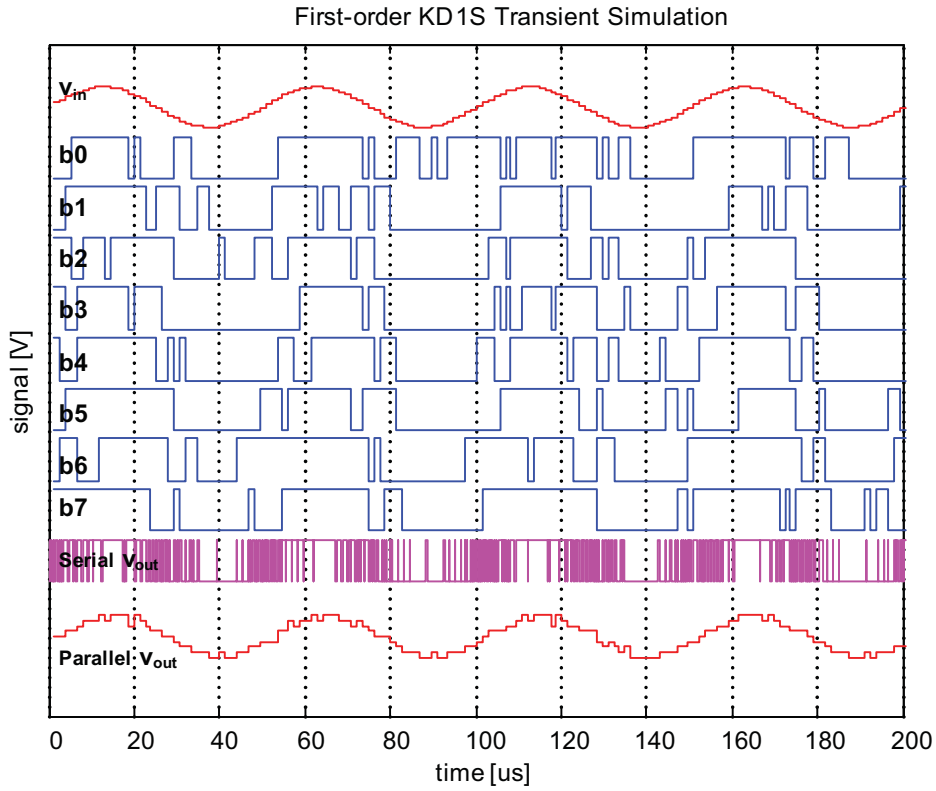

Figure 7.29: Plot illustrating the sampled KD1S outputs $Q[0:8]$, along with the reconstructed serial and parallel output stream (v_{out}).

The simulation results were processed using the MATLAB code shown in Appendix A. Figure 7.30 shows the processed SPICE simulation results for the 500-nm first-order KD1S design. It's important to note that the transistor-level SPICE simulation results are limited to less than 50 dB (<8-bits) to keep the simulation time reasonable. Due to

this limitation MATLAB based system-level modeling is usually employed to design and simulate delta-sigma data converters [23].

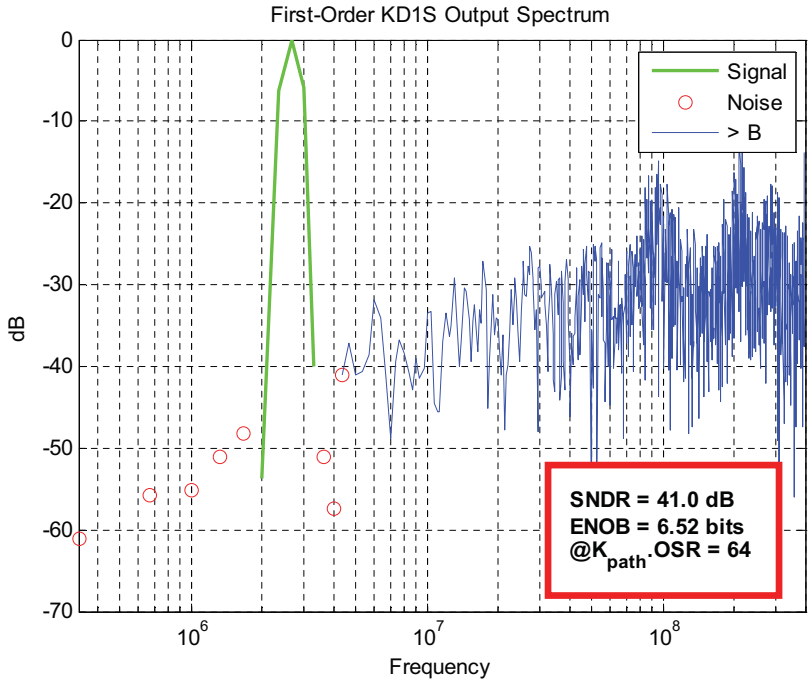

Figure 7.30: Simulation results for the first-order KD1S modulator designed in 500-nm CMOS. In these results, f_{in} =2.67 MHz, f_s = 100 MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz, $K_{path} \cdot OSR = 64$, and $BW = 6.25$ MHz.

A Hann window, with a size equal to the simulation record length (N_{FFT} =2048) is used for spectral estimation using FFT. The simulated signal to noise and distortion ratio (SNDR) is 41 dB, which corresponds to 6.52 bits resolution. As discussed in Section 4.4.4, the NTF response for the modulator exhibits ripples in frequency which are due to the fact that the comparator takes a fraction of the time-slice T_s/K_{path} to evaluate its result while the feedback switches remain open. Due to this some amount of the information from the previous cycle (with T_s loop-delay) is fed-back into both the integrators. This causes these ripples to be formed at odd multiples of $f_s/2$ and they

are superposed over the wideband noise shaping response as discussed in Section 4.4.4. The simulated SNR is plotted with respect to the input sinewave amplitude in Figure 7.31. From this plot, the maximum stable amplitude (MSA) is roughly 80% of the full range which is equal to 2 V.

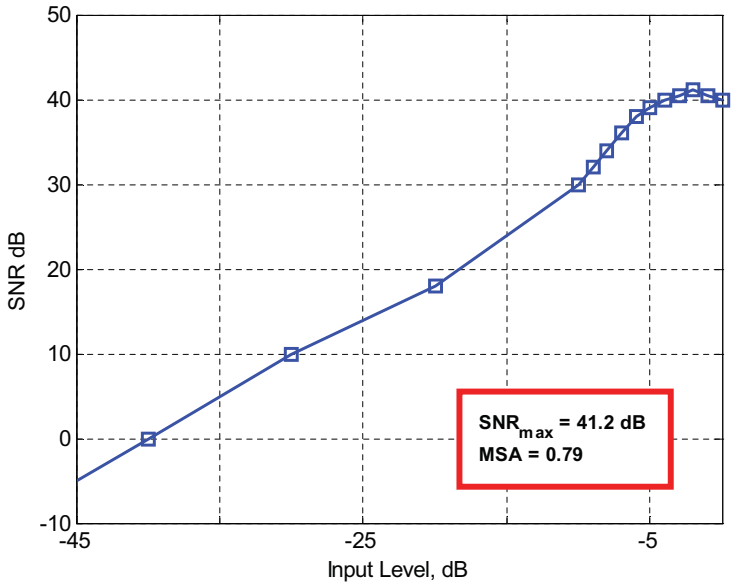

Figure 7.31: Simulated SNR vs input sinewave amplitude for the second-order KD1S modulator.

The average current consumption of the first-order modulator is 2.6 mA from the 5 V supply. The average current consumed in the DLL clock generator is 8 mA.

7.7.2 Second-Order KD1S Modulator

The second-order KD1S modulator, described earlier in Section 7.4, is simulated using SPICE. For the simulation an input clock frequency of 100 MHz is used for the DLL based clock generator. The effective sampling frequency set by the multi-phase clocks

is 800 MHz. A sinusoidal input of $2V$ amplitude and 2.67 MHz frequency is applied to the second-order KD1S modulator. The effective signal bandwidth for this simulation is equal to $f_B = 6.25$ MHz. The simulation result for the 500-nm second-order KD1S design is shown in Figure 7.32. Again, a Hann window with a size equal to the simulation record length (N_{FFT} =2048) is used for spectral estimation. The simulated SNDR is 44.5 dB which is equivalent to 7.1 bits resolution. The NTF response of the second-order modulator shows ripples in the spectrum due to the finite comparator delay as discussed in Section 4.4.4.

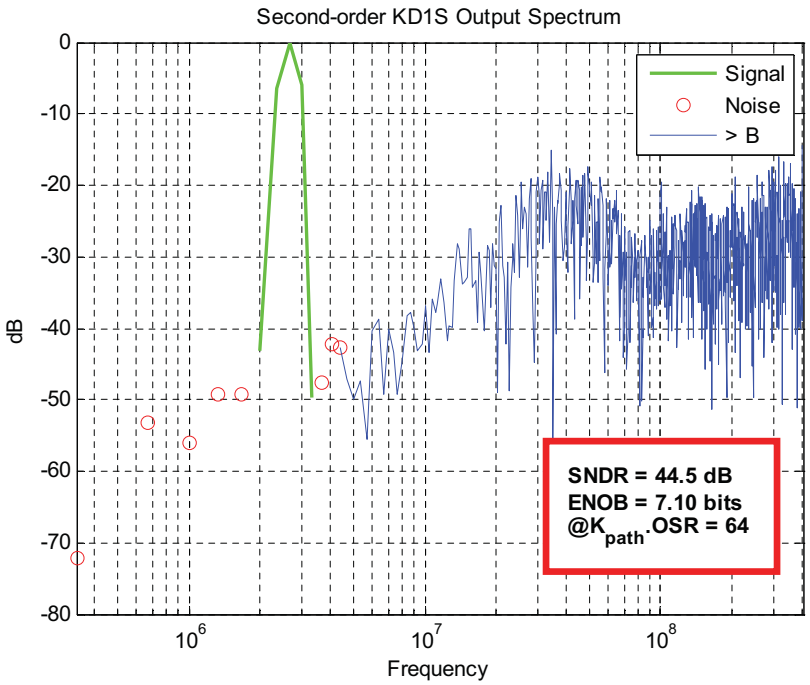

Figure 7.32: Simulation results for the second-order KD1S modulator designed in 500-nm CMOS. IIn these results, f_{in} =2.67 MHz, $f_s = 100$ MHz, $K_{path} = 8$, $f_{s,new} = 800$ MHz, $K_{path} \cdot OSR = 64$, and $BW = 6.25$ MHz.

The received digital outputs of the second-order KD1S modulator are shown in Figure 7.33 below. The plot shows the serial mode-output (v_{out}) with a $K_{path}f_s$ data rate.

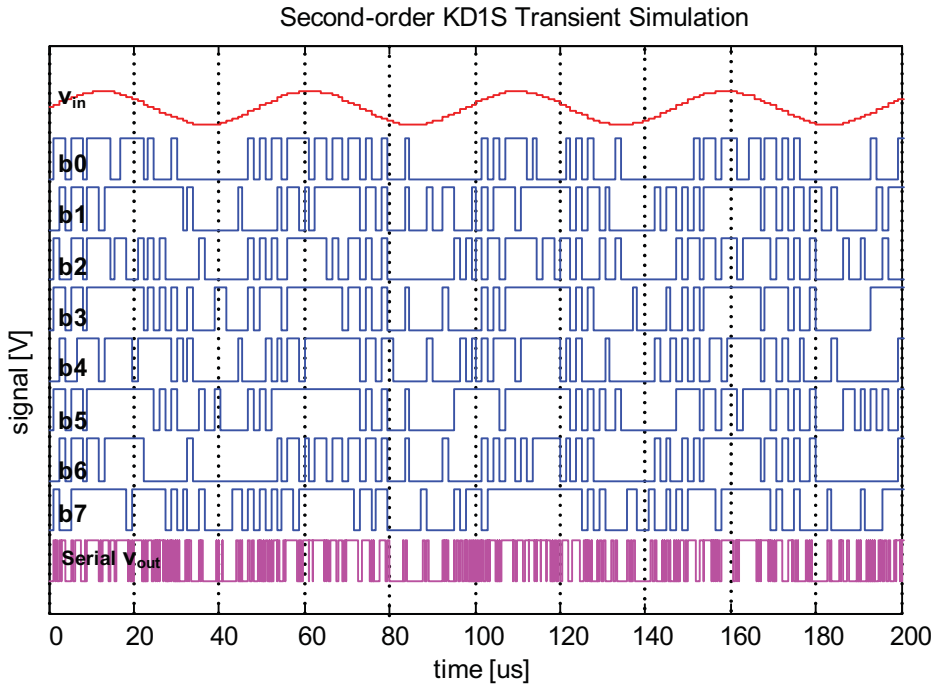

Figure 7.33: Plot illustrating the sampled KD1S outputs $b[0:8]$, along with the reconstructed serial and parallel output stream (v_{out}).

The simulated SNR is plotted with respect to the input sinewave amplitude in Figure 7.34. From this plot, the maximum stable amplitude (MSA) for the input sinewave is 80% of the full range which is equal to 2 V.

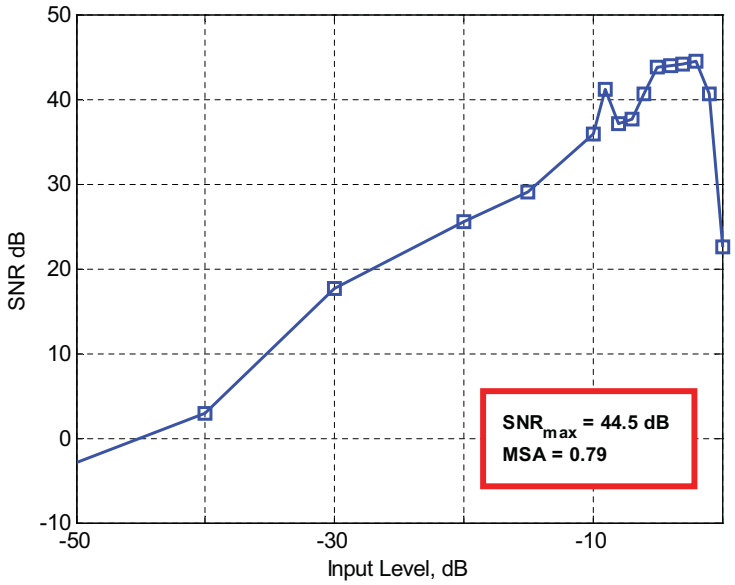

Figure 7.34: Simulated SNR vs input sinewave amplitude for the second-order KD1S modulator.

The average current consumption of the second-order modulator is roughly 3 mA from the 5 V supply while the average current consumed in the DLL clock generator is 8 mA.

7.8 Test Setup and Procedure

Figure 7.35 shows the test setup employed for testing the KD1S modulators. The chip power supply ($VDD = 5$ V) and the common-mode reference voltage ($V_{CM} = 2.5$ V) are externally supplied. A precision current reference LM334 is used for the bias current reference of $20\,\mu A$ employed in the op-amps. An external clock source (CLK_{in}) with a typical frequency of 100 MHz is used for the DLL to lock on and generate the on-chip multi-phase clocks.

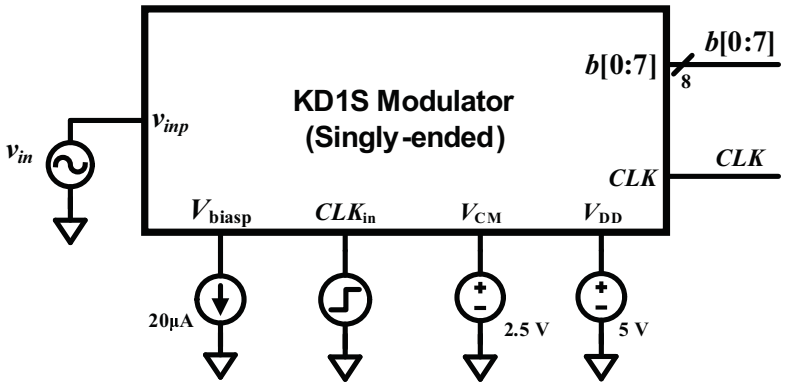

Figure 7.35: Test Setup used for data acquisition from the single-ended KD1S Modulators on the chip.

The $b[0:7]$ and *CLK* outputs from the chip are acquired using an Agilent Mixed-Signal Oscilloscope (Infinivision 7000 Series MSO). The MSO has a maximum of 2 Giga-samples per second rate and allows simultaneous acquisition of up to 16 digital channels along with 4 analog channels. The MSO is remotely controlled through a PC using the IO libraries provided by Agilent. A software, called Intuilink, is used to simultaneously acquire up to 1 million contiguous samples on all the channels. This acquired data is post-processed using the MATLAB script shown in Appendix A. The MATLAB script uses the *CLK* signal to resample the digital outputs $b[0:7]$, and then re-aligns with respect to their individual clock phases (i.e. K_{path} phases per clock frame). This process is essentially converting the K_{path} parallel outputs clocked on f_s to a single-bit serialized stream clocked at $K_{path}f_s$ resulting in the serial mode output v_{out}.

7.8.1 Test Board Design

A simple two-layer prototype board, shown in Figure 7.36, was fabricated to test the 500-nm KD1S chip. The top layer of the board was dedicated to the power supply (V_{DD})

and the lower plane is used for ground (See Figure 7.37). The fabricated die was bonded in-house at Boise State in a 40-pin DIP package. The input signal to the modulator is applied using a SMA to BNC connector. An array of bypass capacitors ($0.1\,\mu F||1\,nF$) is soldered close to the supply pins on the back side of the board to attenuate the supply and ground noise. Tantalum capacitors of $2.2\,\mu F$ value were connected between the power and ground planes for overall effective bypassing.

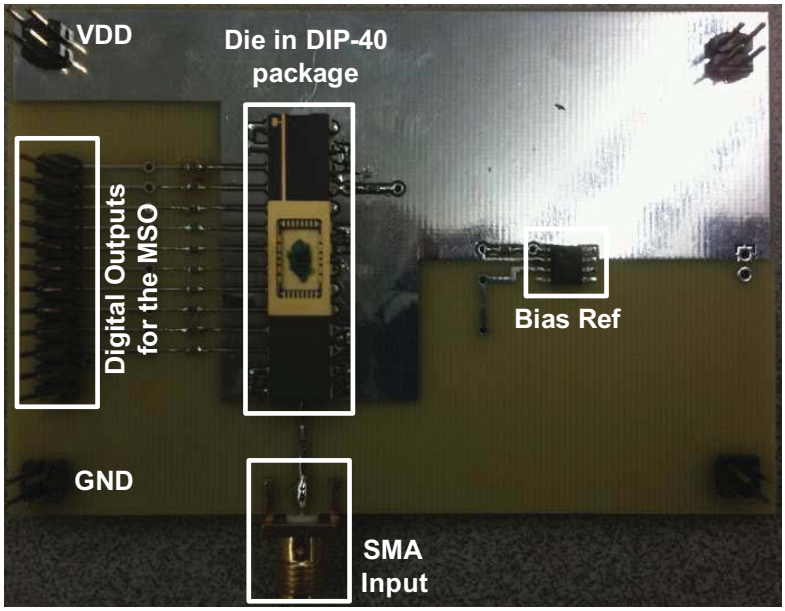

Figure 7.36: Labeled photograph of the test board used for the 500-nm chip.

The modulator outputs and the clock signal from the chip are connected to the digital pods of the MSO using the 12X2 header pins on the board.

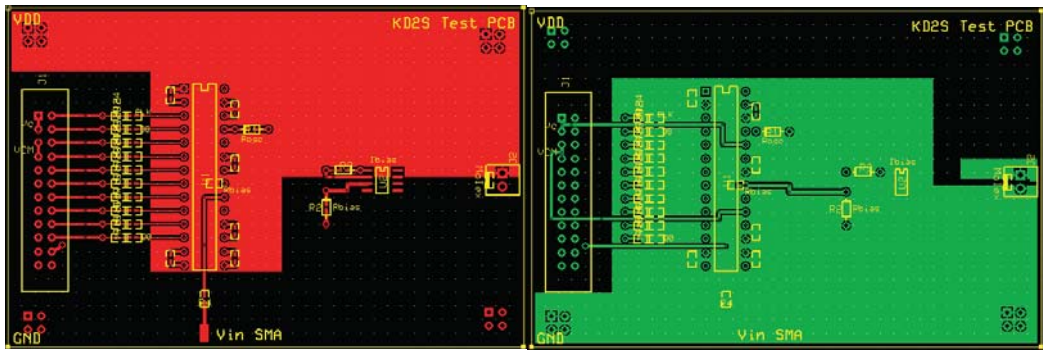

Figure 7.37: (a) Top layer (power plane) and (b) bottom layer (ground plane) of the test board.

7.9 Experimental Results

Using the test setup described in the last section, 1 million data points corresponding to 1 ms of run time were collected. The harvested data was processed with the MATLAB script shown in Appendix A.3. The MATLAB script reconstructs the serial bit stream (v_{out}) from the 8 parallel outputs and the clock acquired from the test chip. Then FFT of the output v_{out} is evaluated using the Blackman-Harris window [17]. Blackman-Harris window has a slightly wider central lobe but much lower sideband leakage than the Hann window. Due to the lower sideband leakage, this window is appropriate for a large data set acquired from the test chip. From the FFT of the serial output, the signal and noise power are evaluated in the signal band which is then used to estimate the SNDR and the bit resolution.

The measured spectrum of the fabricated second-order modulator is shown in Figure 7.38. The peak SNDR corresponding an input signal with -2 dBFS amplitude is 42.7 dB (or 6.81 bits in resolution). The output clock from the chip showed roughly 100 ps

rms jitter which, along with the thermal noise, sets the noise floor in the signal band. We can observe the distortion tones, due to phase skew, appearing at the frequency locations given by $f_{in} + kf_s$ and $f_s - (f_{in} + kf_s)$, $k = 1, ..., K_{path} - 1$ as described in the Section 2.2.3. However, these out-of-band tones are filtered out by the decimation filter following the modulator. The measure SFDR for this modulator is approximately 55 dB.

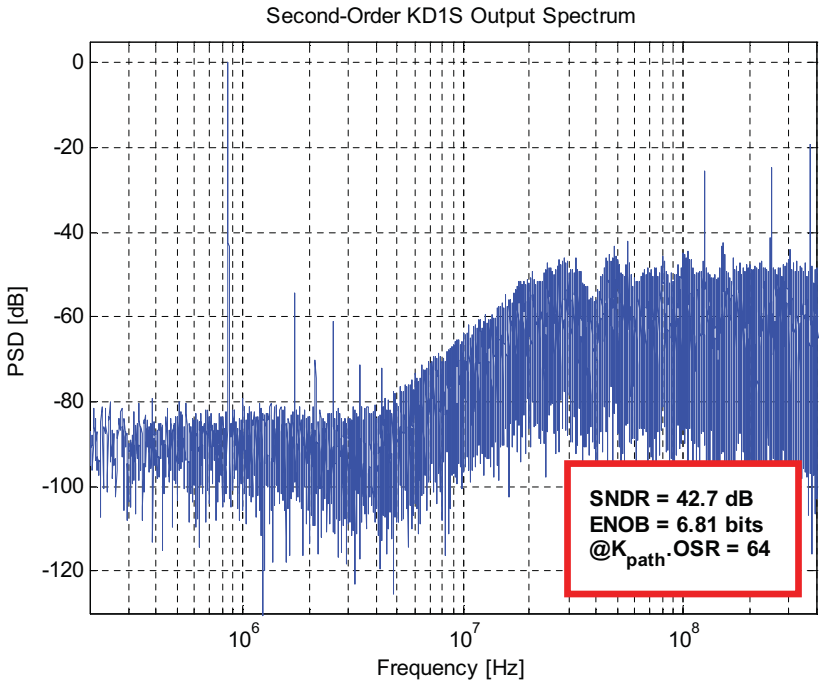

Figure 7.38: Measured PSD of the second-order KD1S modulator fabricated in 500-nm CMOS. Here, $f_{in} = 870$ KHz, $f_s = 100$ MHz, $f_{s,new} = 800$ MHz, $K_{path} = 8$, $K_{path} \cdot OSR = 64$, and $BW = 6.25$ MHz.

The measured SNDR performance of the fabricated second-order KD1S modulator is close to the performance predicted by the behavioral modeling and the transistor level simulation.

7.9.1 Performance

The tested performance of the 500-nm second-order KD1S modulators is summarized in Table 7.1. For delta-sigma modulators, the figure of merit (FoM) metric is defined as

$$FoM_{SNR} = \frac{P}{2 \cdot f_B \cdot 2^{(SNR-1.76)/6.02}} \tag{7.10}$$

where P, f_B and SNR denote the power dissipation, signal bandwidth and peak SNR (in dB) [57]. For the fabricated second-order KD1S modulator, the FoM is 8.74 pJ/level.

Table 7.1: Typical performance of the second-order KD1S modulator (5 V and 25° C).

Process/Supply Voltage	500-nm CMOS/5 V
Number of paths (K_{path})	8
Effective sampling rate ($K_{path} \cdot f_s$)	800 MHz
Signal Bandwidth	6.25 MHz
Input amplitude for peak SNR	-2 dBFS
peak SNDR	42.7 dB
Spur-free Dynamic Range (SFDR)	55 dB
Power Dissipation (Modulator)	15 mW
Power Dissipation (Clock generation block)	35 mW
Active Area	0.55 mm^2
Figure of Merit (FoM_{SNR})	8.74 pJ/level

We can observe that the KD1S modulator achieves high sampling rate and signal bandwidth even in a 500-nm CMOS process. When compared to other switched-capacitor delta-sigma implementations, KD1S modulator achieve significantly higher signal bandwidth. However, for the presented KD1S modulators, the peak SNDR

is lower as only second-order noise shaping is employed. The KD1S SNDR performance can be improved by extending the KD1S concept to third- or higher-order noise-shaping. The power efficiency of the KD1S modulators will be significantly improved when designed in a smaller (and faster) CMOS technology.

7.10 Conclusion

The behavioral level first- and second-order KD1S modulator designs were translated into a circuit level implementation in a 500-nm CMOS technology. The second-order KD1S exhibits wideband noise shaping and a high signal conversion bandwidth of 6.25 MHz with a modest 6-bit resolution, even in a 500-nm CMOS process. The large conversion bandwidth can be digitally traded for a higher resolution by increasing the oversampling ratio. The experimental results for the second-order KD1S modulator closely follow the analytical and simulation results. The performance degradation is likely caused by the higher clock jitter in the on-chip multi-phase clocks which can be improved by optimizing the noise performance of the clock generation circuit. Furthermore, a fully-differential implementation of the the KD1S modulator will also improve the achievable performance.

CHAPTER 8 CONCLUSIONS

8.1 Summary

The contributions and conclusions of this dissertation can be listed as follows to summarize the work's contribution to the state-of-the-art in delta-sigma data converter design:

- The first-order KD1S modulator, proposed in [12, 13], was analyzed for the circuit non-idealities and the errors due to time-interleaving. The KD1S modulator can potentially achieve much higher sampling rates without a significant increase in the gain-bandwidth requirement on the op-amps. This is achieved by employing K_{path} sampling paths and allowing the integrators to settle over a longer period of time set by the base clock. The effective sampling rate is set by the phase spacings of the multi-phase clock and equals $K_{path} \cdot f_s$. Due to the unity-gain bandwidth (f_{un}) of the op-amp can be set to a small multiple of f_s and thus introduces an extra pole in the integrator's response. However, the large fan-out of K_{path} sampling capacitors on the op-amps does not translate it into a reduction in power by K_{path}. Also, the time-interleaved operation of KD1S does not relax the linear settling requirements on the op-amps which should be designed for slew-free settling in the T_s/K_{path} interval.

- In order to achieve wideband noise-shaping using the KD1S modulator, the loop-delay can not exceed T_s/K_{path} which entails that the comparators in each of the

paths settle within $T_s/2K_{path}$ time-interval. It has also been shown that the mismatch in the K_{path} sampling capacitors and the clock phase skew between the clock phases causes noise folding from the multiples of frequency f_s to the baseband. Even though the variance of the noise due to capacitor mismatch is averaged by $K_{path}/2$, the effects of the folding of the shaped quantization noise to the baseband are detrimental for the performance of the practical KD1S design.

- Detailed thermal noise analysis of the KD1S modulator was presented. In summary, the kT/C noise (or sampled thermal noise) is set by the sampling capacitors (C_I) and is averaged by $K_{path}/2$. However for a fixed *OSR*, the achievable *SNR* is independent of K_{path} as the conversion bandwidth is increased by K_{path} times due to time-interleaving.

- The concept of the first-order KD1S modulator has been extended to design higher-order KD1S modulators. A state-space synthesis method has been introduced for rapid design and system-level simulation of the KD1S modulator. The synthesis method takes into account the effects of the additional poles added due to the K-path integrators.

- The developed synthesis method was applied to the design of a second-order KD1S modulator. The prototype modulator was implemented using singly-ended circuitry in 500-nm CMOS process. The modulator employed a DLL to generate the multi-phase clocks locked on an external reference clock. The second-order

resulted in a SNDR of 42.7 dB or 6.8 bits in resolution $K_{path} = 8$ paths, an effective sampling rate of $f_{s,new} = 800MHz$, effective oversampling ratio $K_{path} \cdot OSR = 64$ and a signal bandwidth of 6.25 MHz. The second-order modulator consumes an average current of 3 mA from the 5 V supply and has a layout footprint of 0.55 mm^2 for the single-ended design.

8.2 Future Work

The future work to further improve the performance of the KD1S modulator entails the following :

- The fabricated KD1S modulator designs will be implemented using fully differential circuits. The fully differential circuits will improve the achievable performance by canceling the effects of charge injection from the switches and even order harmonics.

- The timing of the KD1S modulator must be improved in order to accommodate for the finite comparator delay in order to eliminate the ripples in the resulting noise-shaping spectral response. This will require doubling the number of clock phases to allow controllability up to $T_s/2K_{path}$ delay.

- Since each of the comparators in the KD1S modulator have a utilization factor of $1/K_{path}$, it would be beneficial if the number of comparators in KD1S modulator can be reduced by sharing one or two comparators across all the paths. Such an architecture will be result in reduced layout area and possibly less power

consumption. Also this reduced comparator architecture will pave the way for compact multi-bit KD1S design for better stability with higher-order noise shaping.

- Since the clock rate of the KD1S modulator is only limited by the comparator delay, integration of devices like tunnel diodes can be done into the standard CMOS to realize much faster (multiple GHz rate) comparators.

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APPENDIX A

The Matlab code for the KD1S synthesis and digital processing of simulation and test results are listed below:

Listing 8.1: Matlab code for synthesis of second-order KD1S Modulator.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% A second-order KD1S with dynamic range scaling
% Vishal Saxena
% BSU 2009
% Uses Richard Schreier's Delta-Sigma Toolbox
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clear all; clc; close all;

% Synthesize a single-bit second order DSM
order = 2;  % First order
OSR = 64;   % OSR
opt = 0;    % Dont optimize the zeros
nLev = 2;   % Number of quantizer levels
H_inf = 2;
xLim = 0.6; % Limits on integrator output level
f0 = 0;     % Center frequency

% Define Circuit Parameters
fs = 100e6;     % Sampling frequency (slow clock)
fun = 3*fs;     % Opamp unity-gain frequency
Beta = 0.8;     % Feedback factor for the SC Integrator
K = 8;          % Number of parallel paths

% Find Charge Spreading Filter (W(z)) Coefficients
alpha0 = exp(-pi*Beta*fun/(K*fs));
c0 = 1-alpha0;
beta0 = ((K/2-1)/(K/2))*alpha0;

%Spreading function for the K-SCI
W = filt(c0, [1 -beta0]);

% Integrator ABCD Matrix
ABCDint = [1 0 0 0 1 0; c0 beta0 0 0 0 0; 0 0 1 0 0 1; 0 0 c0
  beta0 0 0; c0 beta0 0 0 0 0; 0 0 c0 beta0 0 0];
[Aint,Bint,Cint,Dint] = partitionABCD(ABCDint, order);

% Synthesize the initial design
H = synthesizeNTF(order, OSR, opt);
```

```
form = 'CIFB';  % CIFB modulator structure

% Find the coefficients a,g,b,c.
% Use only single input feed-forward path
[a,g,b,c] = realizeNTF(H, form);
b(2:3) = 0;

% Find ABCD Matrix
ABCD = stuffABCD(a,g,b,c,form);

% Scale the ABCD matrix
[ABCDs umax] = scaleABCD(ABCD, nLev, f0, xLim);
% Map the scaled design back to the coefficients
[a,g,b,c] = mapABCD(ABCDs, form);

% Apply integrator ABCD matrix
[A0,B0,C0,D0] = partitionABCD(ABCDs); % Find ABCDs for the
  scaled design
A1 = Aint + Bint*(A0-eye(size(A0)))*Cint;
B1 = Bint*B0;
C1 = C0*Cint;
D1 = D0;
ABCD1 = [A1 B1; C1 D1];

umax1 = findUmax(ABCD1,nLev,f0,xlim)

% Simulate the DSM in time using ABCD1 matrix
Nfft = 2^13;
tone_bin = 31;
t = [0:Nfft-1];

u = 0.5*(nLev-1)*sin(2*pi*tone_bin/Nfft*t);
u1 = u;
[v,xn,xmax,y] = simulateDSM(u,ABCD1,nLev);
% Find quantizer gain
kq = mean(abs(y))/mean(y.^2)

% Find NTF and STF
[Ha Ga] = calculateTF(ABCD1, kq);

plotPZ(Ha,'b',20,0);
plotPZ_VS(Ha,{'r','b'},20,0)

f = linspace(0, 0.5, 1000);

z = exp(2i*pi*f);
figure();
f1 = f*K*fs;
plot(f1, dbv(evalTF(Ha,z)), 'lineWidth',2);
semilogx(f1, dbv(evalTF(Ha,z)), 'lineWidth',2);
xlim([1e6 K*fs/2]);
hold on; grid on;
```

```
89 semilogx(f1, dbv(evalTF(Ga,z)),'r','lineWidth',2);
90 plot(f1, dbv(evalTF(Ga,z)),'r','lineWidth',2);
91 legend('NTF','STF');
92 xlabel ('Frequency'); ylabel ('dB');
93 title ('Second-Order KD1S NTF and STF');
94
95 sigma_H = dbv(rmsGain(Ha, 0, 0.5/OSR));
96
97 % Plot time-domain simulation results
98 figure(2)
99 n=1:1000;
100 stairs(t(n), u(n), 'r');
101 hold on; grid on;
102 stairs(t(n), v(n), 'g');
103
104 % Simulate the Spectrum
105 spec = fft(v.*ds_hann(Nfft))/(Nfft*(nLev-1)/4);
106 snr = calculateSNR(spec(1:ceil(Nfft/(2*OSR))+1), tone_bin)
107 Neff = (snr-1.76)/6.02
108
109 NBW = 1.5/Nfft;
110 f = linspace(0, 0.5, Nfft/2+1);
111 Sqq = 4*(evalTF(Ha, exp(2i*pi*f))/(nLev-1)).^2/3;
112
113 figure()
114 f1 = f*K*fs;
115 plot(f1, dbv(spec(1:Nfft/2+1)), 'b')
116 hold on; grid on;
117 plot(f1, dbp(Sqq*NBW), 'r', 'Linewidth', 2);
118 xlim([1e5 K*fs/2]);
119 xlabel ('Frequency'); ylabel ('dB');
120 title ('Second-Order KD1S Output Spectrum');
121 text_handle = text(floor(K*fs/3),-100, sprintf('SNDR = %4.1f dB
    \nENOB = %2.2f bits \n@K_{path}.OSR = %2.0f',snr,Neff,OSR),'
    FontWeight','bold','EdgeColor','red','LineWidth',3,'
    BackgroundColor',[1 1 1],'Margin',10);
122
123 figure()
124 semilogx(f1, dbv(spec(1:Nfft/2+1)), 'b')
125 hold on; grid on;
126 semilogx(f1, dbp(Sqq*NBW), 'r', 'Linewidth', 2);
127 xlim([1e5 K*fs/2]);
128 xlabel ('Frequency'); ylabel ('dB');
129 title ('Second-Order KD1S Output Spectrum');
130 text_handle = text(floor(K*fs/40),-110, sprintf('SNDR = %4.1f dB
    \nENOB = %2.2f bits \n@K_{path}.OSR = %2.0f',snr,Neff,OSR),'
    FontWeight','bold','EdgeColor','red','LineWidth',3,'
    BackgroundColor',[1 1 1],'Margin',10);
131
132 % Print out synthesis result
133 a,b,g,c,umax
134 CI1 = 100;
```

```
CF1 = CI1/b(1)
CI2 = 100;
CF2 = CI2/c(1)
CI3 = a(2)*CF2
CG1 = g(1)*CF1

% Plot the Integrtator Output Histograms
figure();
x1 = -1:0.05:1;

subplot(1,2,1);
hist(xn(2,:),x1); grid on;
xlabel ('Vint1 [V]'); ylabel ('Count');
title ('First Integrator Output Histogram');
h = findobj(gca,'Type','patch');
set(h,'FaceColor','r','EdgeColor', 'w');
xlim([-1 1]);

subplot(1,2,2);
hist(xn(4,:),x1); grid on;
xlabel ('Vint2 [V]'); ylabel ('Count');
title ('Second Integrator Output Histogram');
h = findobj(gca,'Type','patch');
set(h,'FaceColor','r','EdgeColor', 'w');
xlim([-1 1]);

%% EOF
```

Listing 8.2: Example Matlab code for plotting the results from Spice/Spectre simulations.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Plotting the output spectrum of the KD1S modulator from
% the simulation results obtained from Spectre or Ultrasim
% Vishal Saxena
% BSU 2009
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all; close all; clc;
% Link Matlab and Cadence Spectre by setting the environment
  variables

% Result Directory of Spectre/Ultrasim
% Check for schematic or config view
rdir = '/home/students/vsaxena/simulation/sim_KD2S/UltraSim/
  config/psf';
% rdir = '/home/students/vsaxena/simulation/sim_KD2S/Spectre/
  config/psf';

% Pick transient data-set
dataset_name = 'tran';           % for Ultrasim
% dataset_name = 'tran-tran';    % for Spectre

```

```
%% User defined params
VDD = 1.2;
VCM = VDD/2;
Kpath = 9;
tprobe = 50e-12;     % 50ps probe time
OSR = 64;            % BW = (fs/2)/OSR

%% Extract all the signals
% signals = cds_srr(rdir, dataset_name);

% Extract required signals and convert them to voltages
Q0 = cds_srr(rdir, dataset_name, 'q0'); q_0 = Q0.V;
Q1 = cds_srr(rdir, dataset_name, 'q1'); q_1 = Q1.V;
Q2 = cds_srr(rdir, dataset_name, 'q2'); q_2 = Q2.V;
Q3 = cds_srr(rdir, dataset_name, 'q3'); q_3 = Q3.V;
Q4 = cds_srr(rdir, dataset_name, 'q4'); q_4 = Q4.V;
Q5 = cds_srr(rdir, dataset_name, 'q5'); q_5 = Q5.V;
Q6 = cds_srr(rdir, dataset_name, 'q6'); q_6 = Q6.V;
Q7 = cds_srr(rdir, dataset_name, 'q7'); q_7 = Q7.V;
Q8 = cds_srr(rdir, dataset_name, 'q8'); q_8 = Q8.V;
CLK = cds_srr(rdir, dataset_name, 'clk'); clk = CLK.V;

%% Process data
clk_sliced = clk>VCM;
clktrans = find(clk_sliced(2:end)-clk_sliced(1:end-1) == 1);
b_c(1,:) = (q_0(clktrans)) > VDD/2;
b_c(2,:) = (q_1(clktrans)) > VDD/2;
b_c(3,:) = (q_2(clktrans)) > VDD/2;
b_c(4,:) = (q_3(clktrans)) > VDD/2;
b_c(5,:) = (q_4(clktrans)) > VDD/2;
b_c(6,:) = (q_5(clktrans)) > VDD/2;
b_c(7,:) = (q_6(clktrans)) > VDD/2;
b_c(8,:) = (q_7(clktrans)) > VDD/2;
b_c(9,:) = (q_8(clktrans)) > VDD/2;
Nc = length(b_c(1,:));

vout = VDD*reshape(b_c, Nc*Kpath, 1);
vout=vout*VDD;
vout=vout-mean(vout);

% effective sampling rate
fs = Kpath/(tprobe*(clktrans(5)-clktrans(4)));
fmax = fs;  % Plot only till fmax
N = length(vout);
BW = (fs/2)/OSR
dt = 1/fs;
t1 = 0:dt:(N-1)*dt;  %time array
frange = 1/dt; % estimate the frequency range of the data

%% Apply Hann Window
w = hann(N);
w1 = norm(w,1);
```

```
Y = fft(w.*vout)/(w1/2); %Apply window to estimate FFT
N1 = floor(N*fmax/frange); %Plot range (up to fmax)
Yl = Y(1:N1); %lower half of fft
DC1=Yl(1);  DC2 = mean(vout);  %Scaling test: DC1 should equal DC2
%remove DC component
Yl(1)=Yl(3);
Yl(2)=Yl(3);

%% Estimate PSD
Py = abs(Yl).^2; %Power spectrum
[Pmax, Pindex] = max(Py); %The tone power and index
fbin = Pindex;
fres = frange/N;  %freq step size and resolution
f = 0:fres:(N1-1)*fres;  %freq array

%% Estimate SNR and Neff
nb=5;
signal_bins = fbin + [-(nb-1)/2:(nb-1)/2];
inband_bins = 0:N1/(2*OSR);
noise_bins = setdiff(inband_bins,signal_bins);
second_tone_bins = 2*fbin-1 + (-(nb-1)/2:(nb-1)/2);
noise_bins = setdiff(noise_bins,second_tone_bins);
third_tone_bins = 3*fbin-1 + (-(nb-1)/2:(nb-1)/2);
noise_bins = setdiff(noise_bins,third_tone_bins);
SNR = dbp(sum(Py(signal_bins+1))/sum(Py(noise_bins+1)))
Neff = (SNR-1.78)/6.02

%% Plot Spectrum
figure(1)
plot(f, 10*log10(Py));  %plot spectrum
xlim([0 fs/1]); ylim([-80 0]);
xlabel ('Frequency [Hz]'); ylabel ('PSD [dB]');
title ('Second-order KD1S Output Spectrum');
grid on;
text_handle = text(floor(5*fs/8),-70, sprintf('SNDR = %4.1f dB \
  nENOB = %2.2f bits \n@K_{path}.OSR = %2.0f ',SNR,Neff, OSR),'
  FontWeight','bold','EdgeColor','red','LineWidth',3,'
  BackgroundColor',[1 1 1],'Margin',10);

figure(2)
semilogx(f, 10*log10(Py), 'b');  %plot spectrum
xlim([0 fs/2]); ylim([-90 0]);
xlabel ('Frequency [Hz]'); ylabel ('PSD [dB]');
title ('Second-order KD1S Output Spectrum');
grid on;
text_handle = text(floor(fs/40),-75, sprintf('SNDR = %4.1f dB \
  nENOB = %2.2f bits \n@K_{path}.OSR = %2.0f ',SNR,Neff,OSR),'
  FontWeight','bold','EdgeColor','red','LineWidth',3,'
  BackgroundColor',[1 1 1],'Margin',10);

%% EOF
```

Listing 8.3: Matlab code for processing data acquired from the MSO.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Process MSO acquired CSV Data
% Use the Agilent Intuilink GUI to capture data
% Vishal Saxena
% BSU 2009
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clc; clear all;

%% Chip Test Parameters
VDD = 1.2;          % Chip VDD
VCM = VDD/2;        % Chip VCM
x_inc = 1e-9;       % X increment in data acquisition
clk_pwidth = clktrans(5)-clktrans(4);  % Find the clock pulse
  width in terms of samples
fs = 1/(x_inc*clk_pwidth);
Kpath = 9;          % Num of paths
fmax = Kpath*fs;    % Plot only till fmax
OSR = 64;           % OSR per path
BW = (Kpath*fs/2)/OSR

%% Read binary coded Mixed Signal ouputs D0-D7
% Import the file
importfile('pod1.csv');
y1 = pod1;
% Decode the digital outputs
n=8; % number of lines D0-D7
str = dec2bin(y1,n); % produces a binary representation with at
  least n bits.

D0 = str2num(str(:, n));
D1 = str2num(str(:, n-1));
D2 = str2num(str(:, n-2));
D3 = str2num(str(:, n-3));
D4 = str2num(str(:, n-4));
D5 = str2num(str(:, n-5));
D6 = str2num(str(:, n-6));
D7 = str2num(str(:, n-7));

%% Read binary coded Mixed Signal ouputs D8-D15
importfile('pod2.csv');
y2 = pod2;

% Decode the digital outputs
n=8; % number of lines D7-D15
str = dec2bin(y2,n); % produces a binary representation with at
  least n bits.

D8 = str2num(str(:, n));
D9 = str2num(str(:, n-1));

%% Process data
```

```
Vth = 0.5;  % Digital threshold used in MSO
clk = D9;
clk_sliced = clk > Vth;
clktrans = find(clk_sliced(2:end)-clk_sliced(1:end-1) == 1);

b_c(1,:) = (D0(clktrans)) > Vth;
b_c(2,:) = (D1(clktrans)) > Vth;
b_c(3,:) = (D2(clktrans)) > Vth;
b_c(4,:) = (D3(clktrans)) > Vth;
b_c(5,:) = (D4(clktrans)) > Vth;
b_c(6,:) = (D5(clktrans)) > Vth;
b_c(7,:) = (D6(clktrans)) > Vth;
b_c(8,:) = (D7(clktrans)) > Vth;
b_c(9,:) = (D8(clktrans)) > Vth;
% Keep b_c in memory

%% Process acquired data
Nc = length(b_c(1,:));

% Combine Yi arrayes into a single output stream
vout = VDD*reshape(b_c, Nc*Kpath, 1);
vout = vout-mean(vout);
N=length(vout);
dt = 1/(Kpath*fs);
t1 = 0:dt:(N-1)*dt;  %time array
frange = 1/dt; % estimate the frequency range of the data

%% Apply Blackman Window
w = blackman(N);
w1 = norm(w,1);
Y = fft(w.*vout)/(w1/2); %Apply window to estimate FFT
N1 = floor(N*fmax/(frange*1)); %Plot range (up to fmax)
N2 = ceil(N1/OSR);  % In-band signal range
Yl = Y(1:N1); %lower half of fft
DC1=Yl(1);  DC2 = mean(vout);  %Scaling test: DC1 should equal
  DC2
%remove DC component
Yl(1)=Yl(3);
Yl(2)=Yl(3);

%% Estimate PSD
Py = abs(Yl).^2; %Power spectrum
[Pmax, Pindex] = max(Py(1:N2)); %The tone power and index
fbin = Pindex;
fres = frange/N;  %freq step size and resolution
f = 0:fres:(N1-1)*fres;  %freq array

%% Estimate SNR and Neff
nb = 5;
signal_bins = fbin + [-(nb-1)/2:(nb-1)/2];
inband_bins = 1:N1/(2*OSR);
noise_bins = setdiff(inband_bins,signal_bins);
```

```
100
101 % Calculate SNR
102 SNR = dbp(sum(Py(signal_bins))/sum(Py(noise_bins)))
103 Neff = (SNR-1.78)/6.02
104
105 %% Plot Spectrum
106 figure(1)
107 plot(f, 10*log10(Py));  %plot spectrum
108 xlim([0 Kpath*fs/1]);
109 xlabel ('Frequency [Hz]'); ylabel ('PSD [dB]');
110 title ('KD1S Output Spectrum');
111 grid on;
112 text_handle = text(floor(5*Kpath*fs/8),-90, sprintf('SNDR = %4.1
    f dB \nENOB = %2.2f bits \n@K_{path}.OSR = %2.0f ',SNR,Neff,
    OSR),'FontWeight','bold','EdgeColor','red','LineWidth',3,'
    BackgroundColor',[1 1 1],'Margin',10);
113
114 %%
115 figure(2)
116 semilogx(f, 10*log10(Py), 'b');  %plot spectrum
117 xlim([0 Kpath*fs/2]);
118 xlabel ('Frequency [Hz]'); ylabel ('PSD [dB]');
119 title ('KD1S Output Spectrum');
120 grid on;
121 text_handle = text(floor(Kpath*fs/100),-90, sprintf('SNDR = %4.1
    f dB \nENOB = %2.2f bits \n@K_{path}.OSR = %2.0f ',SNR,Neff,
    OSR),'FontWeight','bold','EdgeColor','red','LineWidth',3,'
    BackgroundColor',[1 1 1],'Margin',10);
122
123 %% EOF
```