Instrumentation Requirements for Fast 130+ V/ns Switching of 1700 V, 35 mΩ SiC MOSFETs

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Abstract

This paper demonstrates the benefits, downsides, and instrumentation requirements of switching 1.7 kV, 35 mΩ SiC MOSFETs at 130+ V/ns, beyond the speed used by the device manufacturer for datasheet characterisation. Experimental results are obtained in a 1200 V, 50 A bridge leg, and comparisons are made between passive voltage probes, optically isolated differential probes, shunt current measurement, Rogowski coils, and Infinity Sensors. At 130 V/ns, a 24% improvement over the datasheet characterised switching loss is found, however the limitations of Rogowski coils and passive probes become significant. The methods demonstrated should permit design engineers to explore switching speed and efficiency limitations in their applications.

1 Introduction

Wide bandgap switches can reduce switching losses compared to traditional silicon switches due in part to their short switching duration. However, switching speeds must sometimes be limited in order to avoid reliability concerns through unwanted waveform features, including: excessive drain-source voltage overshoot leading to breakdown, power loop current overshoots and ringing [1] [2] [3] leading to EMI concerns [4], gate pick up leading to cross-talk [5], gate voltage overshoot leading to gate breakdown concerns [6], and excessive *dv/dt* potentially leading to latchup of the parasitic BJT [7]. By switching SiC MOSFETs faster, with gate resistors that are smaller than those used by the manufacturer for datasheet characterisation, significant efficiency and power density improvements could be achieved, but only if unwanted switching waveform features can be addressed, e.g. by improved layout, assist circuits, or advanced gate driving. This requires suitable instrumentation to observe unwanted, high-bandwidth features in switching waveforms. This paper demonstrates experimental switching speeds that are beyond those used for the datasheet characterisation of the 1700 V, 35 mΩ TO-247-4 SiC MSC035SMA170B4 MOSFET (Fig. 1), and shows where probes excel or run into limitations. The paper's contributions are:

- In Section 2, an analysis of the measurement requirements for fast SiC power converters, to include the key signals that need to be measured, bandwidth requirements, and voltage/current deskewing accuracy required to maintain power loss measurement accuracy.
- Different probing options, suitable for measurement in high-speed SiC circuits, are discussed and summarised in Section 3, including a helpful tip that can allow a Rogowski coil to be placed to measure source current without overlapping the switch node trace.
- In Section 4 a 1200 V, 50 A bridge-leg is demonstrated, switching at up to 3× datasheet characterisation speeds, reaching voltage slew rates of 200+ V/ns. Simultaneous measurements are demonstrated with different current and voltage probes, to allow comparison of different probe types and technologies. High-fidelity gate current measurements are shown using magnetic-field-based and shunt-based measurements.
- Limitations on switching speed are discussed in Sections 4.2 – 4.3, in terms of gate driver capability, device reliability and EMI.

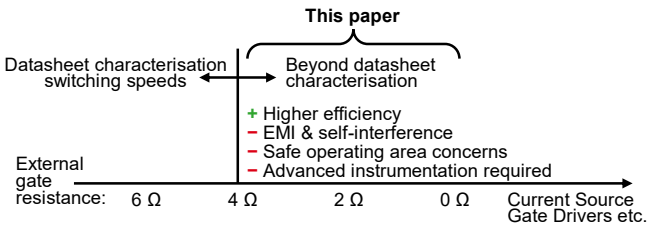

Fig. 1 Scope of this paper: switching beyond datasheet speeds.

2 Measurement considerations for fast transients of SiC MOSFETs

2.1 Target Measurements

Fig. 2 shows a simplified schematic of a half-bridge switching circuit, with an inductive load and the low-side device as the active switch. Fig. 3 demonstrates some of the unwanted features that can be observed in the switching waveforms of such half-bridge legs, especially when they are switched at high speed. Accurately observing these unwanted features is an important prerequisite for diagnosing whether a converter will have reliability issues, and a first step in resolving them.

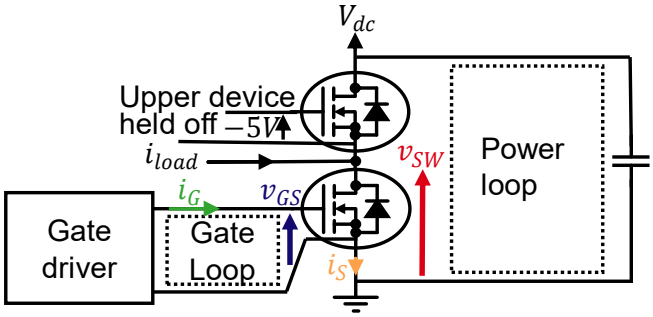

Fig. 2 Simplified circuit diagram of a half bridge switching under an inductive load.

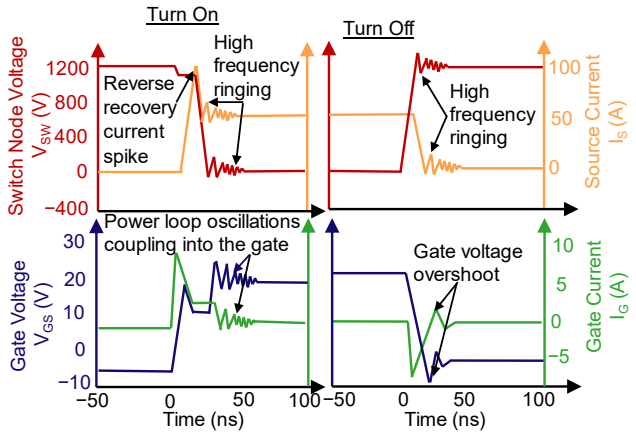

Fig. 3 Concept diagram showing waveform features at high switching speed. Left: low-side device turn-on. Right: low-side device turn-off.

A significant contributor to the current overshoot that occurs in the turn-on process of the active device, is the reverse recovery of the intrinsic body diode of the opposing MOSFET (in this case, the high-side MOSFET) [8]. The overshoot and subsequent oscillation can cause EMI concerns [1]. The peak source current may breach the maximum transient current capability of the MOSFET which combined with large *dv/dt* can lead to BJT latch-up concerns [7].

High frequency ringing appears under fast switching transients due to the power devices' output capacitance resonating with the power loop inductance. For low-side switching the high side device's output capacitance resonates at turn-on, and the low-side capacitance at turn off. Increased switching speed increases the oscillation magnitude and duration.

When gate resistance is reduced, the gate loop can become underdamped causing transient gate voltage overshoot and subsequent gate loop ringing [6], observable with gate current and gate voltage instrumentation. Overshoot and oscillations from the power loop can be coupled into the gate loop via the reverse transfer capacitance, which may cause abnormal turn-on behaviour, and ultimately damage to the device. Additionally, in 3 pin packages, source current *di/dt* couples into the gate via the inductance of the common source pin. In packages with a Kelvin source, there will be some *di/dt* coupling, due to the gate loop encircling some area which will have some mutual coupling with the power loop. Peak gate current limitations were proposed in [6].

In order to observe these behaviours, to aid the design engineer in the optimisation process, the following waveforms should be measured: v_{SW}, i_S, v_{GS}, and i_G. Further, switching loss can be calculated from measured v_{SW} and i_S.

2.2 Measurement requirements

In this section some of the key requirements for accurate switching measurements are evaluated. Satisfying these requirements enables accurate power device characterisation which can mitigate converter failure.

When evaluating measurement apparatus, it must be taken in the wider context of the measurement system [9], including the signal, the measurement connection, the probe, the recording device - typically an oscilloscope, and the external environment that the measurement system is operating in. How a probe is connected to a circuit critically impacts its performance [10], therefore the probes and connection method will be evaluated together, where appropriate. As switching speed increases, the measurement environment becomes harsher, with larger *di/dt* and *dv/dt*, which can disrupt measurement. Faster switching edges require more bandwidth to observe, can induce common mode voltages that disrupt measurement, require higher magnetic-field and electric-field immunity and an increasingly accurate deskew for accurate loss characterisation.

2.2.1 Measurement Bandwidth

As switching speed increases, higher bandwidth probes and scopes are required to observe the resulting waveforms.
Firstly, considering the risetime of the signal of interest, the required measurement bandwidth is given by:

$$f_{3db} = 3 \times 0.35/T_{rise}, \quad (1)$$

where f_{3db} is the required measurement bandwidth and T_{rise} is the 10%-90% rise time [10].
For a 1200 V dc-link, a measurement bandwidth of 110 MHz is required to observe a transient slewing at 100 V/ns and 220 MHz for 200 V/ns.
Secondly, the frequency of any post-edge ringing should be considered. For example, the power devices under investigation here have an output capacitance of 150 pF at 1200 V, which when coupled with the power loop inductance of approximately 20 nH can produce ringing at 92 MHz.
Thirdly, in respect of EMI performance, high frequency interference sources can reside in small waveform features [11], which will be filtered out of the measurement if low bandwidth instrumentation is used.

2.2.2 Common-mode rejection for gate-source measurements

When measuring the gate-source voltage, the common-mode performance of the probe used can be critical. Commonly, this requirement is considered in relation to the measurement of a high-side device, where the reference node (the source of the high-side MOSFET) is slewing rapidly relative to the negative side of the DC link. However, common-mode rejection can also be important for low-side devices. MOSFETs with kelvin connections can induce transient common-mode voltages between the kelvin and power ground, due to the source inductance of the MOSFET and the large *di/dt* under switching [12]. For example, 5 nH of source inductance can induce 50 V under a fast 10 A/ns switching event. To attenuate this common mode signal to 0.5 V error, a common-mode rejection ratio (CMRR) of 40 dB will be required [12] at up to 100 MHz as shown in equ. 2 [9].

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\frac{V_{cm}}{V_{err}}\right| \quad (2)$$

Where A_{dm} is the differential mode gain and is assumed to be 1, A_{cm} is the common mode gain, V_{cm} is the common mode signal, and V_{err} is the acceptable error in the measurement. As switching speed is increased, more common-mode rejection is required. High side gate measurements have a much stricter common mode immunity requirement due to the high side source voltage rapidly slewing during switching.

2.2.3 Limitation of gate voltage measurement

There are inherent limits on the accuracy of gate voltage measurements taken at the package terminals, due to the packaging inductance between the device terminals and the die, which in this case is 9 nH according to the manufacturer's SPICE model [13]. Gate *di/dt* has been measured in later sections to be 0.37 A/ns, which can induce 3.33 V across the packaging inductance, causing a misreading at the measurement terminals [14]. At low external gate resistance, the internal gate resistance of 0.85 Ω dominates, which complicates evaluation of the state of charge of the internal capacitance of the device. Gate current measurements can provide a useful alternative as the measurement is not impacted by these parasitics.

2.2.4 Magnetic-field and electric-field immunity

Voltage measurements require high magnetic-field immunity from the source current during switching, due to the ability of large *di/dt* events to radiate magnetic fields, in turn inducing a voltage in measurement loops. For a power loop with peak oscillation *di/dt* of 10 A/ns, mutual loop inductance must be less than 100 pH to ensure the interference induced in the measurement loop is less than 1 V. Mutual coupling is highly dependent on specific orientation and geometry. Similarly, the electric-field immunity of current probes should be considered, to minimise errors induced by high *dv/dt* in the vicinity of the probe. Immunity can be increased through specific probe design, shielding, and careful probe placement and orientation.

2.2.5 Probe features to reduce invasiveness of measurements

Measurement techniques should always strive to minimise the effects that they can have on the behaviour of the circuit under test.
Voltage probes should have low input capacitance to reduce current flowing into the front-end of the oscilloscope and to reduce loading on the circuit, whilst current probes should have as low insertion inductance as possible.

2.2.6 Considerations to maximise accuracy of switching-loss calculations derived from electrical signal measurements

Fast switching is primarily focused on reducing switching loss. Switching loss can be calculated

from measured device voltage and current. Accurate characterisation requires the propagation delay of the current and voltage signals to be matched – i.e. the measured waveforms must be deskewed before their product is calculated to give the instantaneous power waveform. Increasingly accurate deskewing is required as switching speed increases [15], [16]. In Fig. 4, probe skew has been added to a 1200 V, 50 A low-side turn-on switching event as shown in Fig. 2. The increasing slope for different slew rates demonstrates how the deskew requirement becomes stricter as switching speed increases. For a ±5% switching loss accuracy, with the datasheet-employed 4 Ω gate resistance, probes must be deskewed to ±750 ps whereas at 0 Ω, ±250 ps deskew is required. In this work, all the waveforms are deskewed to within ±160 ps, giving <±5% error.

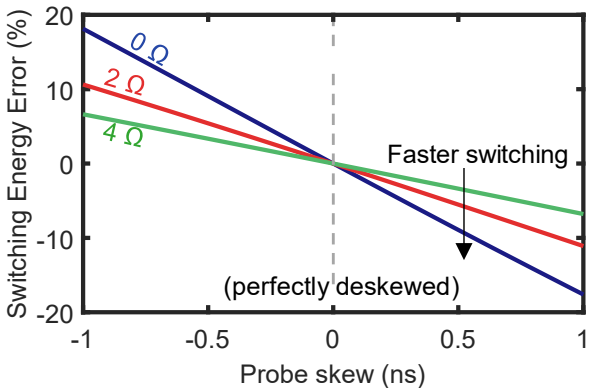

Fig. 4 Impact of deskewing current and voltage waveforms on derived switching energy, using experimental example data of a turn-on switching transient at 1200 V & 50 A at various switching speeds: 4 Ω: 70 V/ns & 7 A/ns; 2 Ω: 90 V/ns & 9 A/ns; 0 Ω: 130 V/ns & 12 A/ns.

3 Hardware Implementation

A double-pulse rig was used to test MSC035SMA170B4 1700 V 35 mΩ TO-247-4 SiC MOSFETs [17] at 1200 V and a load current of 50 A. The devices were driven by an Infineon Eicedriver 1ED3124MU12HXUMA1 [18] with +20 V and −5 V rails. The gate driver internal resistance is 0.45 Ω at turn on and 0.35 Ω at turn off, whilst the power device has an internal gate resistance of 0.85 Ω.

To reduce the power loop inductance the pins of the TO-247-4 package have been bent so that the package can be soldered onto the surface, eliminating through holes and thus allowing the return current to flow on an uninterrupted continuous ground plane on a close inner layer of the PCB. The power loop inductance was estimated from the ringing frequency to be 22.9 nH.

3.1 Comparison of measurement options

In this paper probing is reviewed using single-ended passive voltage probes, optically isolated voltage probes, commercial Rogowski coils and Infinity Sensors, which are types of a miniature magnetic field current sensor that is galvanically isolated, with high bandwidth, low cost, and low insertion inductance [19].

To demonstrate the trade-off of different measurement technologies, duplicate measurements of current and voltage on gate and power terminals are compared on a single capture of an 8 channel 2 GHz Tektronix MSO58B oscilloscope for two switching speeds. Fig. 5 details which probes were used in which locations of the circuit; the specific connections are shown in the photograph of Fig. 6. A summary of the probes and their specifications is provided in Table 1.

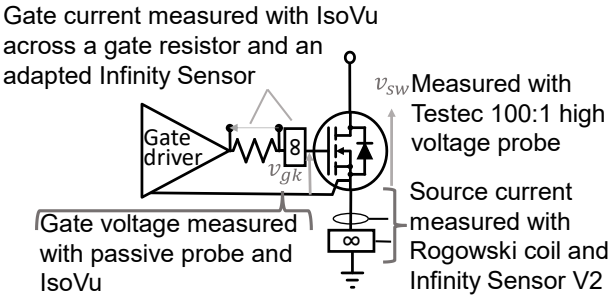

Fig. 5 Measurement diagram.

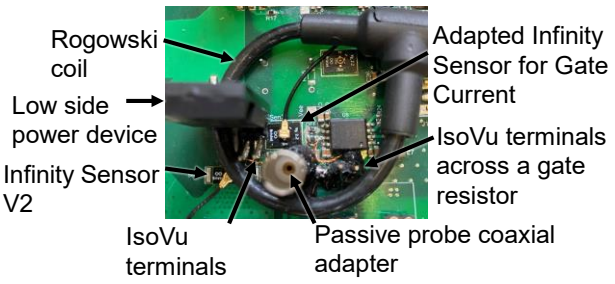

Fig. 6 Duplicate measurement for current and voltage on gate and power terminals.

3.1.1 v_{SW} measurement

A high-voltage passive probe is used to measure the low side switch node voltage. The probe has been used in a high-voltage coaxial probe adaptor from PMK to reduce the measurement loop inductance and improve its immunity to *di/dt* [10].

3.1.2 i_S measurement

The low-side source current is measured with a Rogowski coil and an Infinity Sensor.

To reduce the degree of *dv/dt* pick-up of the Rogowski coil, careful placement is required. In this circuit, enclosing only the source pin of the device would inevitably force the coil to be in close

Signal	Probe	Specification
v_{SW}	Testec HV250 passive probe	300 MHz 100:1 attenuation 2.5 kV max
i_S	Infinity Sensor V2	1 MHz to 1 GHz 100 mV/(A/ns) sensitivity 600 A/ns max
	Rogowski coil CWTMini 50HF 06 PEM	75 Hz – 50 MHz 50 mV/A sensitivity 8 A/ns max
v_{GS}	Tektronix IsoVu TIVP1L	1 GHz 50 V max tip 100 MHz CMRR: 92 dB
	PMK Firefly (Section 4.5)	>1.5 GHz 50 V max tip 100 MHz CMRR: 75 dB
	Keysight N2890A Passive Probe	500 MHz 10:1 attenuation 300 V max
i_G	Adapted Infinity Sensor	1 MHz – 300 MHz 1 V/(A/ns) sensitivity
	Infinity Gate Sensor (Section 4.5)	1 MHz – 500 MHz 0.67 V/(A/ns) sensitivity
	IsoVu TIVP1L across a gate resistor	1 GHz 50 V max 100 MHz CMRR: 92 dB

Table 1 Probes used in the study.

proximity to the switch node, which would increase the amount of *dv/dt*-induced noise in the measurement. If instead, the source, gate and Kelvin source pins are enclosed, the coil can be oriented away from the circuit switch node. As both the gate and Kelvin source pins are enclosed, the gate current cancels out and only the power-circuit source current is measured.
The Infinity Sensor is placed between the source and the power ground [19]; this arrangement minimises *dv/dt* seen by the sensor.

3.1.3 v_{GS} measurement

The gate voltage is measured with a passive probe in a coaxial adapter from PMK and using short enamel pair of jumper wires [10]. A second measurement is made via an IsoVu connected to the circuit using 2.54 mm pin-headers soldered into the gate and Kelvin terminals of the TO-247-4 package.

3.1.4 i_G measurement

The gate current is measured with an IsoVu across an SMD gate resistor, via a twisted pair of thin enamel wire [10], to 2.54 mm pin headers. The *di/dt* immunity is less strict for the gate current interconnects due to the gate resistor being 15 mm away from the noise source. The gate current is also measured with an adapted Infinity Sensor design, based on the V2 design but with 10× the gain and 300 MHz bandwidth (measured with a Rhode & Schwarz ZVL Vector Network Analyser).

4 High Speed Switching Results

4.1 Comparison of measurement waveforms

Fig. 7 shows experimental waveforms of the turn-on transients in double pulse tests at 1200 V and 50 A. Two switching speeds are compared to show the measurement discrepancies of using different probes.

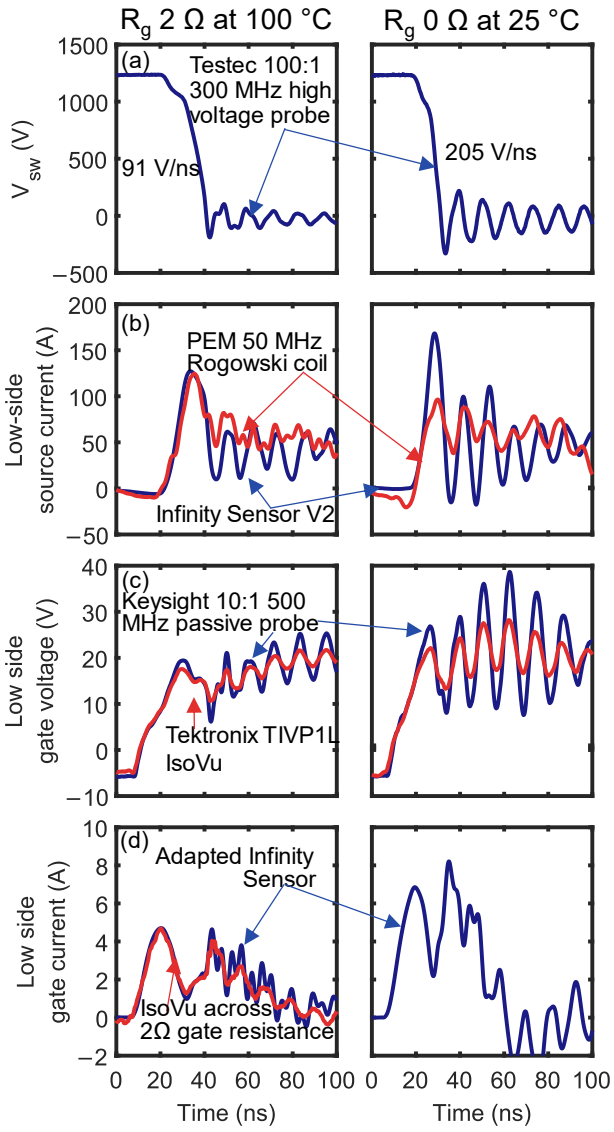

Fig. 7 Comparison of measurement technologies in circuit switching at 1200 V, 50 A, with case temperature at 100 °C and gate resistor of 2 Ω, to represent fast switching at a realistic converter temperature (left), and at 25 °C with gate resistor of 0 Ω, to achieve the maximum observed speed (right).

In Fig. 7(a), the switch node voltage is measured with a 300 MHz Testec HV250 100:1 passive probe. By reducing the external gate resistance and device temperature, the switching speed is greatly increased. The *dv/dt*, calculated from the 60% to 40% values of the swich node voltage, is 91 V/ns at 2 Ω, 100 °C, and 205 V/ns at 0 Ω, 25 °C. The ringing frequency is approximately 86 MHz for both speeds. Meanwhile, larger overshoot and oscillations are measured with the increased switching speed.

In Fig. 7(b), source current measurements are compared between a PEM CWTMini 50 MHz Rogowski coil and a Bristol 1 GHz Infinity Sensor V2 [19]. Significant discrepancies can be observed between these two current measurement instruments in both the current overshoot and ringing. At 2 Ω, 100 °C, there is a good match at the first peak of current, but the ringing captured by the Rogowski coil is attenuated. At 0 Ω, 25 °C, the discrepancy is more significant, where both peaks and ringing are mismatched. Such discrepancies may be caused by the limited bandwidth of the Rogowski coil used (50 MHz). In addition, some of these problems are a function of size, causing the Rogowski coil to overlap the switch node when enclosing the pin of the TO-247 device, leading to *dv/dt* pickup.

In Fig. 7(c), the low-side gate voltage to Kelvin source is compared for a simultaneous measurement with a Gen 2 IsoVu and a 500 MHz 10:1 N2890A passive voltage probe. Approximately 3× more ringing is observed with the passive probe than the IsoVu. This is likely due to the IsoVu probe's higher common-mode rejection of the voltage oscillations between Kelvin source and power ground and the improved magnetic-field immunity.

In Fig. 7(d), the gate current at 2 Ω is measured with an adapted Infinity Sensor V2 and an IsoVu connected across the 2 Ω SMD gate resistor. The gate current profiles of two measurements have a good match, proving the accuracy of using a modified Infinity Sensor to measure the gate current. More oscillations exist on the Infinity Sensor measurement result than the IsoVu voltage probe due to the IsoVu having high CMRR. At 0 Ω, 25 °C, the external gate resistance is completely removed, and the measurement by IsoVu is not viable anymore. As can be seen from the figure, the gate current profiles are similar, and the peak of gate current increases from 5 A to 7 A when reducing the external resistance from 2 Ω to 0 Ω.

Considering the measurement accuracy, the following probes are used in later tests: a passive voltage probe for switch node voltage, an Infinity Sensor V2 for source current, an IsoVu for gate voltage, and the adapted Infinity Sensor for the gate current.

4.2 Impact of gate resistance with case temperature of 100°C

4.2.1 Turn-on

Double-pulse switching waveforms, for low side turn-on are shown in Fig. 8, with gate resistance being swept from of 4 Ω to 0 Ω, where 4 Ω is the value used by the manufacturer for datasheet characterisation. The power devices are held at 100°C, to emulate continuous operation. The results demonstrate how high bandwidth probing can identify onset of unwanted features in switching waveforms.

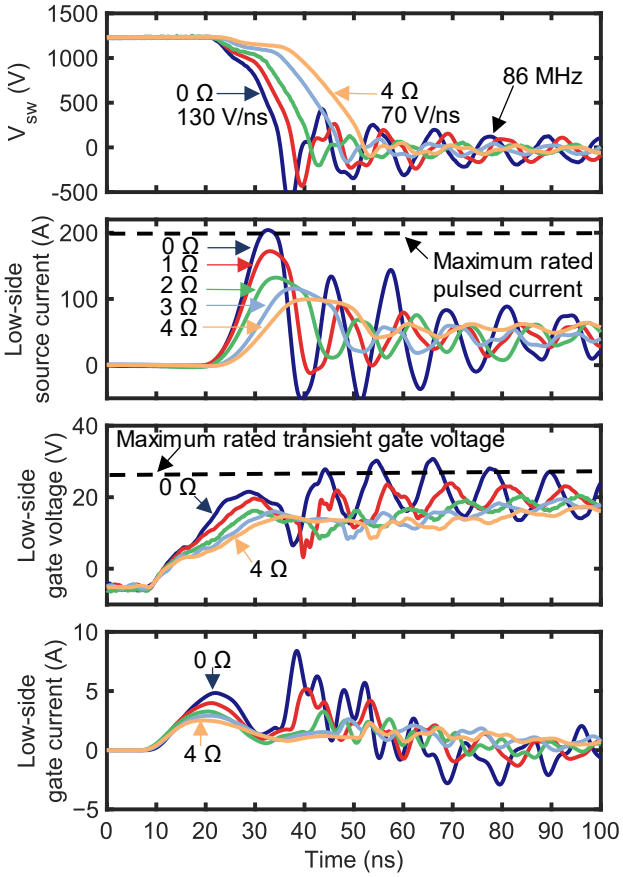

Fig. 8 Measured turn-on transients with external gate resistance of 4 Ω down to 0 Ω, and 100 °C case temperature.

The measured peak reverse recovery current is seen to increase from 90 A to 204 A; the maximum rated pulsed current limit in the datasheet is 200 A. The *dv/dt* increases from 68 V/ns at 4 Ω external gate resistance to 130 V/ns at 0 Ω, whilst the *di/dt* increases from 7 A/ns to 12 A/ns. The switch-node voltage undershoot becomes increasingly large

with switching speed, raising concerns of exceeding the voltage rating of the high side device. The transient gate voltage increases from 20 V at 4 Ω to 30.7 V at 0 Ω; the transient limit of the gate voltage is 23 V, raising reliability concerns [6]. As gate resistance is minimised, the internal gate resistance becomes the dominant limitation in increasing switching speed at turn on, when using a step gate driver [20]. At room temperature (Fig. 7), significantly faster switching speed was observed (205 V/ns).

4.2.2 Turn-off

Double-pulse switching waveforms for low side turn-off are shown in Fig. 9, with gate resistance being swept from 4 Ω to 0 Ω.

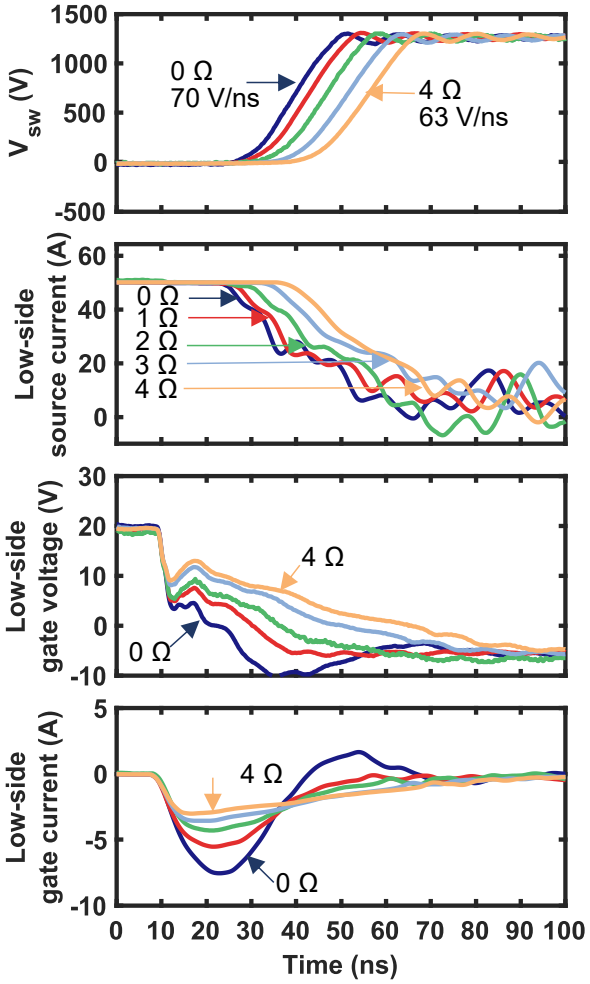

Fig. 9 Measured turn-off transients with external gate resistance of 4 Ω down to 0 Ω, and 100 °C case temperature.

Voltage slew rate increases from 63 V/ns at 4 Ω to 70 V/ns at 0 Ω, an increase in *dv/dt* of 14%. The relative lack of increase in switching speed, in comparison to turn on, is because the slew rate here is determined mainly by the device output capacitance and the load current [21].
As gate resistance is reduced below 1 Ω, the gate becomes visibly underdamped leading to gate voltage undershoot raising gate oxide degradation concerns. The results suggest that operating the device with reduced gate resistance at turn off is not advisable due to a relative lack of improvement in switching energy with added reliability concerns due to the increased current oscillation and underdamping of the gate.

4.3 Spectral Analysis

The frequency spectrum of the switch node voltage was calculated by taking an FFT of the switching edges at full load current, turn off + turn on, in a single capture. This data is representative of a converter switching at 500 kHz with 50 % duty cycle.
Spectra are shown at different gate resistance in Fig. 10, demonstrating how the increased switching speed increases energy in the radiated emissions band 30 MHz to 1 GHz, as per EN 61000-6-3:2007 [22]. Two discernible ringing frequencies are apparent in the switch node voltage: 86 MHz and 236 MHz. These high-frequency oscillations raise EMI concerns as they may radiate efficiently, with ¼ wavelengths of 870 mm and 320 mm respectively.

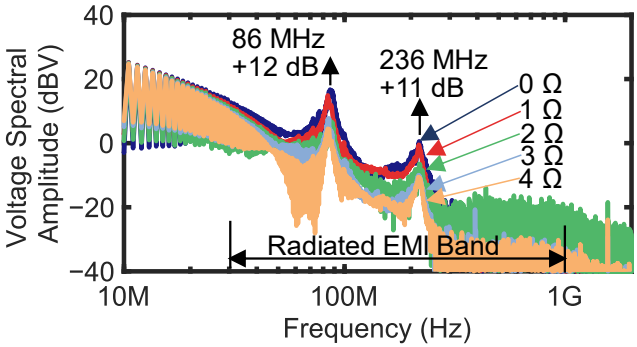

Fig. 10 FFT of switch node voltage shown in Fig. 8 and Fig. 9. The radiated emissions band 30 MHz to 1 GHz EN 61000-6-3:2007 is highlighted.

It can be observed from the switch node voltage waveforms that the slope increases with decreased gate resistance. As observed in the voltage spectrum Fig. 10, increased switching speed increases the −40 dB/dec corner point of the spectral components (f), as expected from the relationship shown in equ. 3.

$$f = 1/(\pi t_r) \quad (3)$$

Where t_r is the rise time, increasing the total spectral content with increasing switching speed [23]; the bandwidth limit of the voltage probe and noise

floor of the scope limit the accuracy of the high frequency measurements above 300 MHz.
Fig. 11 demonstrates the impact of gate resistance on turn-on switching energy; a 24% improvement was observed over datasheet values, when the device was driven with zero external gate resistance. It has been shown here that a conventional voltage source gate driver can deliver much higher performance than datasheet characterisation for a 1700 V 35 mΩ device. However, as such improvements come at the cost of reliability and EMI concerns, care must be taken in PCB layout and filter design to mitigate these issues.

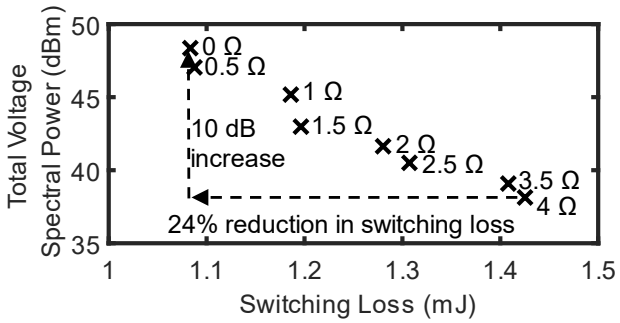

Fig. 11 Turn-on switching loss vs switch node voltage spectral power in a radiated emission zone from 30 MHz to 100 MHz *[24]*.

4.4 Demonstration of fast switching in a different power circuit

A new power board has been designed to demonstrate the measurement methods validated in Section 4.1. The new board utilises gate drivers on daughter boards connected through 8 × 2.54 mm pin headers. MSC035SMA170B4 SiC MOSFETs are used as in the preceding sections, in a half bridge topology with the low-side switch being driven in a double pulse test. The devices switch 1200 V and 50 A at a 25 °C case temperature, with 4.5 Ω or 0.5 Ω external gate resistances.
The measurement setup is shown in Fig. 12. The switch node voltage is measured with a Testec HV250 passive probe and source current is measured with an Infinity Sensor V2.
Gate voltage is measured with a PMK Firefly, a scope-agnostic optically-isolated voltage probe with >1.5 GHz bandwidth. This board uses MMCX connectors to connect the optically-isolated voltage probes into the circuit, to give the best measurement performance [25].
Gate current is measured with a 0.5 Ω current shunt using an IsoVu in an MMCX connector and using an Infinity Gate Sensor [26]. The sensor is an improved gate *di/dt* sensor compared to the sensor used in subsections 4.1-4.3. It is a vertically-mounted PCB sensor with an improved sensing coil geometry to provide high external *di/dt* immunity [26].

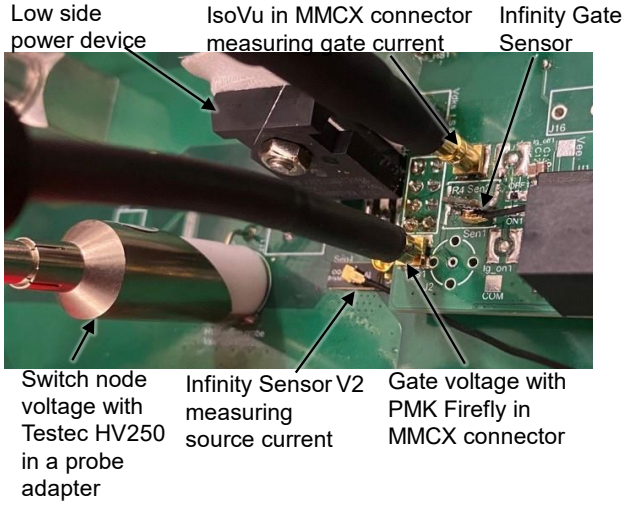

Fig. 12 Demonstration of probing in a different power board.

The measured performance is shown in Fig. 13. With 4.5 Ω gate resistor, v_{SW} slew rate is 41 V/ns and i_S slew rate is 5.1 A/ns, whilst with 0.5 Ω gate resistor, the slew rates increase to 130 V/ns and 11.2 A/ns. The Infinity Gate Sensor measurement is well correlated to the shunt+IsoVu measurement, delivering similar measurement fidelity for vastly reduced cost.

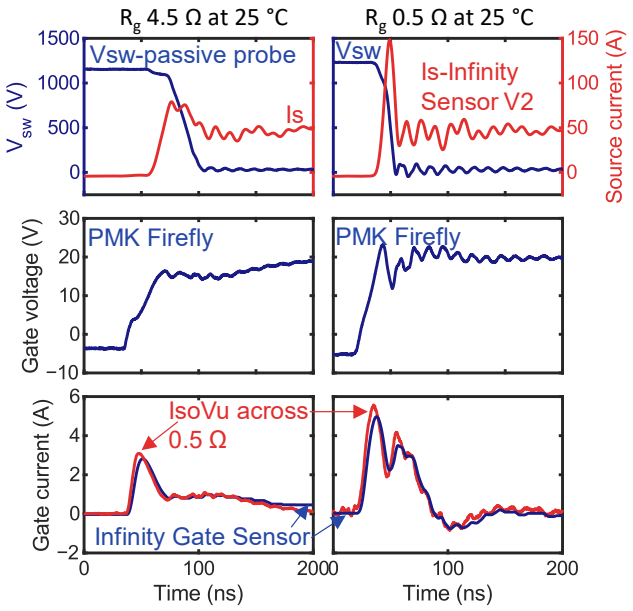

Fig. 13 Demonstration of switching waveforms at 1200 V, 50 A and 25 °C. Left: with 4.5 Ω gate resistance; Right: with 0.5 Ω gate resistance.

5 Conclusions

This paper has analysed measurement requirements for accurate characterisation of fast-switching SiC circuits, including bandwidth, radiated field immunity, common-mode rejection, and deskew accuracy. Various techniques have been demonstrated on a 1200 V, 50 A SiC MOSFET bridge leg switching at 130+ V/ns.

It has been shown that for fast-switching SiC devices with Kelvin source pins, a probe with high common-mode rejection is required in order to resolve the gate to source voltage with high fidelity, as the measurement delivered by a standard passive probe will be corrupted by the large common-mode voltage induced between power and Kelvin source pins. Further, it has been shown that in packages with relatively large gate-loop inductance, there can be a large discrepancy between the voltage measured at the terminals, and the actual gate-source voltage seen by the device at the die level. As such, it can be helpful to supplement the gate voltage measurement with a gate current measurement, so that, for example, the gate charge displacement may be accurately determined. Modified Infinity Sensors offer a low-cost means to make this measurement.

It has also been shown that commercially-available Rogowski coils may lack the bandwidth necessary to fully capture the high-frequency features of switching waveforms, requiring the use of alternatives such as the Infinity Sensor V2.

Unwanted switching features, such as overshoot and ringing, and their impact on SiC bridge legs have been analysed. Increasing switching speed beyond that used by the manufacturer for datasheet characterisation, by reducing the gate resistance down to 0 Ω, has been shown to reduce turn-on loss by over 24%. The internal gate resistance was found to be the dominant restricting factor in further increasing switching speed. However, such fast switching increases measurement demands and increases unwanted switching features, which would require mitigation through advanced techniques such as active gate driving.

Infinity Sensors are available from infinitysensor.com.

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