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## Development and Integration of MEMS Based Inductive Sensors

Luyang Zhang

*The University of Western Ontario*

Supervisor

Dr. Jun Yang

*The University of Western Ontario*

Graduate Program in Mechanical and Materials Engineering

A thesis submitted in partial fulfillment of the requirements for the degree in Master of Engineering Science

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Development and Integration of MEMS Based Inductive Sensors

(Thesis format: Monograph)

by

Luyang Zhang

Graduate Program in Mechanical and Material Engineering

A thesis submitted in partial fulfillment  
of the requirements for the degree of  
Master of Engineering Science

The School of Graduate and Postdoctoral Studies  
The University of Western Ontario  
London, Ontario, Canada

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## Abstract

Inductive sensors are one of the most widely used sensors especially in automotive. However, with the current PCB manufacture process, the large size of the sensor limits its usage in different applications. In this thesis, a novel method of fabricating bi-layer copper micro inductive sensor is demonstrated to solve the size issue. The two coil layers were built by UV LIGA process respectively, and a polyimide insulation film sandwiched in between. At the beginning, seeding layer was deposited on the substrate as electrode, and then the copper coil layer was created through electroplating in the patterned micromold. The coil was prepared after stripping off the seeding layer and micromold. Lately, the fabricated coil chips, ASIC, and capacitors were integrated together through PCB board by using wire bonding and SMT process. A reliable procedure of building robust micro inductive sensor was developed with the consideration of future mass production possibility. The good test results compared with simulation proved the feasibility of developing and fabricating miniaturized micro inductive sensor.

## Keywords

Miniaturized micro inductive sensor, microfabrication process, photolithography, electroplating, optimization, integration

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## Chapter 1

### 1 Introduction

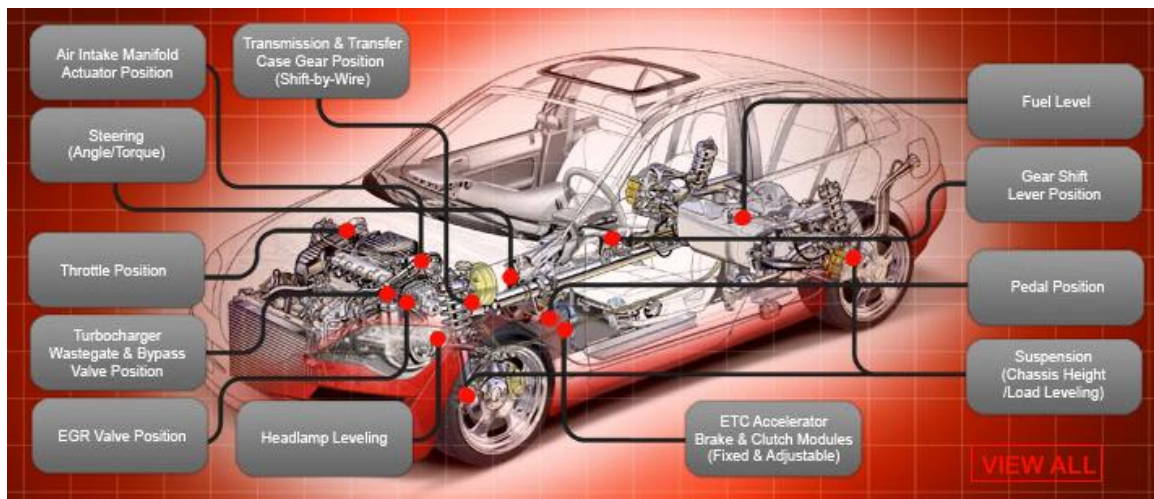
#### 1.1 Background

Sensors are often defined as devices that detect and transform the certain type of physical, chemical, and biological quantities into a measureable signal are playing a very important role in our daily life [1]. Taking automotive industry as an example, when an automobile is in operation, electronic control systems collect all the data from sensors (mostly physical quantities) convert the data into electrical signal that can be processed by the chips. At the meantime, all the information is presented to the driver so that the feedback is given immediately for controlling the movement of automobile. With the improvement of technology, more and more sensors have been placed into new model automobiles. As shown in **Table 1-1**, research shows that it is estimated that there are more than 70 different of sensors in one car nowadays, and the number was around 40 and 24 back to the year of 2007 and 2002 respectively [2-4]. In this regard, There is no need to address more about how it is important to keep those sensors working, especially to those directly related to our safety, such as position sensors for steering wheels, transmissions, throttle control and gas pedal position sensing. Those sensors are usually

required to work under very severe circumstance, come along with extraordinary robustness and accuracy.

**Table 1-1 Automotive sensor market growth [2,3,4]**

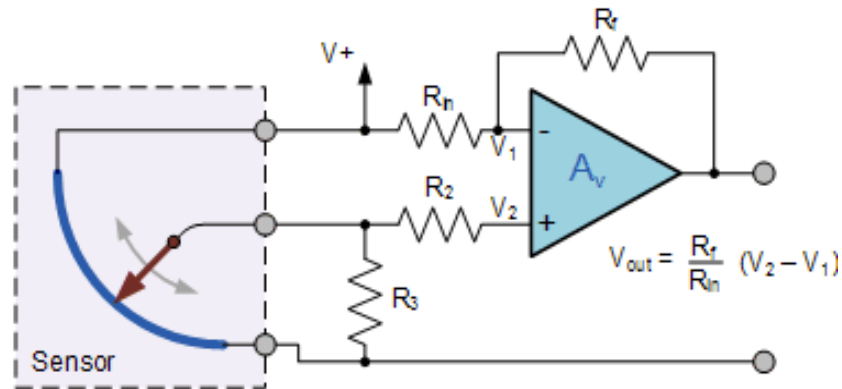
Sensor Statistic	1995	2002	2013
Total sensor production	200M	400M	1100M
Average number of sensors per vehicle	24	40	70



**Figure 1-1 Scheme of position sensors are placed in an automobile (Adapted from [5])**

Position sensor acts a vital role in an automotive, in a lot of situations, the position of some parts of the automotive need to be determined and given appropriate instructions. As shown in **Figure 1-1**, more than 10 position sensors are used in each car for safety, performance and comfort, such as electronic steering, active suspension, automatic

headlight adjustment, pedal position, throttle control, air control valve measurement and so on, and it is one of the most widely used sensors in automotive. There are three main different kinds of technology trends can be found in the market:



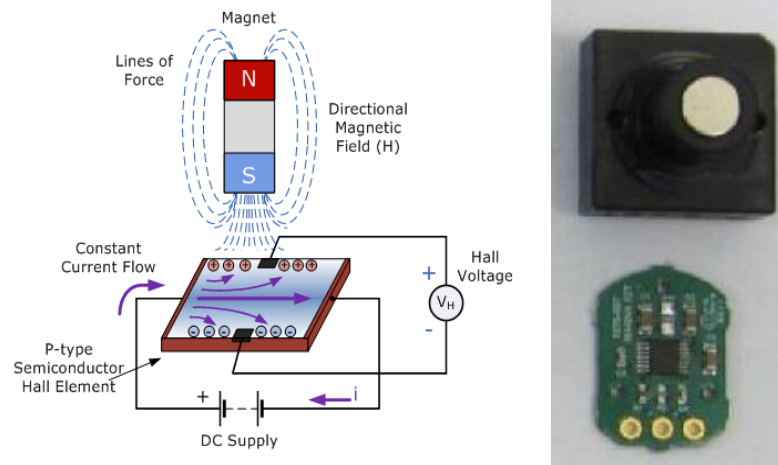
**Figure 1-2 Configuration of a simple potentiometer position sensor (Adapted from [6])**

It is known that potentiometer is the simplest position sensor, and historically, the most widely used commercialized position sensor. As shown in **Figure 1-2**, a wiper arm is contacted with the resistor, the output electrical signals is proportional to the shaft position indicates how much the angle or position change [6,7]. The biggest advantage of this configuration is its low cost. However, the incapability of robustness makes it very hard to fit in automobile circumstance where requires devices have fairly long life span. Moreover, the resolution and noise issue limit its usage in my applications. In this regard, potentiometer is a decent solution for most applications where the cost is the top issue by sacrificing reliability.



**Figure 1-3 Two examples of gas pedals with non-contacting sensors: using an inductive principle (left) and a design using the Hall effect (right) (Copied from [8])**

Nearly all the position sensors in the vehicle are considered having close relevance with safety, new sensors such as magnetic sensors and inductive sensors are developed base on contactless principles, as illustrated in **Figure 1-3**. A Hall Effect sensor takes the advantages from the Hall Effect, which was discovered by the American physicist Edwin Hall in 1879. It can be simply explained as shown in **Figure 1-4**, with the DC supply on, when there is no magnetic field applied, the output voltage is none. When a magnetic field is applied, the electrons and electron holes in the semiconductor are driven to the different sides [9]. As a result, the potential difference then can be measured and indicates how the position between magnet and semiconductor are changed. The non-contact design of Hall Effect sensor solved the issue.



**Figure 1-4 Scheme of Hall effect [6] and a typical Hall effect sensor**

For magnetic sensors, the Hall Effect sensing element is used to determine the magnetic field variable applied to the target. While for inductive sensor, the position of the target is determined by measuring mutual inductance between excitation coil and the sensing coil [3, 8]. Given these points, the inductive sensor is more reliable due to its immunity from magnetic disturbance from its environment. Also, it is more cost-effective without requiring magnets as core part compared to magnetic sensors. However, due to the large antenna area is designed from ensure the signal strength, the inductive sensors usually have larger size [10].

The **Table 1-2** [8,11] gives an overview of comparison among different position sensing principles. It is not hard to draw the conclusion that magnetic sensor and inductive sensor have better performance over contacting based sensor, the cost advantage of potentiometer position sensor can not be traded off in the applications where high performance is needed. Comparing inductive sensor with magnetic sensor along, the relatively large size of inductive sensor fabricated by current PCB (Printed Circuit Board) technology becomes its main limitation, even though according to the **Table 1-2**, the



inductive sensor has better overall performance and a lower price. Hence, it can't be more vital to investigate if it is possible to shrink down the size of inductive sensor without sacrificing the performance.

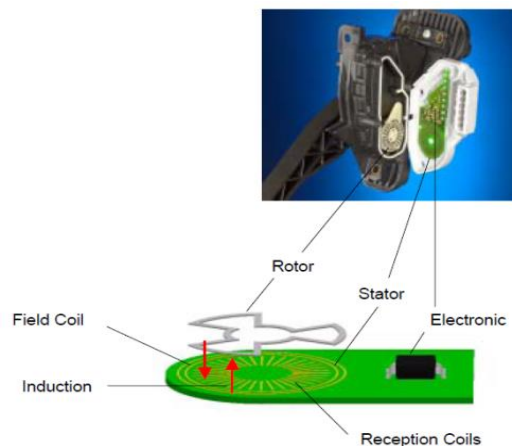
**Table 1-2 An overview of comparison among different position sensing principles [8, 13]**

	Potentiometric	Magnetic	Inductive
Reliability	Contacting principle, prone to wear	Contactless, good	Contactless, good
Cost	Low	High	Medium
Size	Large	Medium	Large, with possibility to miniaturize
Calibration	Easy	Medium	Medium
Temperature Drift	Negligible	Medium, can be compensated	Small
Noise	Poor	Good	Good
Resolution	Bad	Good	Good

## 1.2 Research Motivation

With the question we have in the last section, a detailed investigation is conducted focusing on whether it is possible to substantially reduce the size of inductive sensors while keeping their outstanding performance.

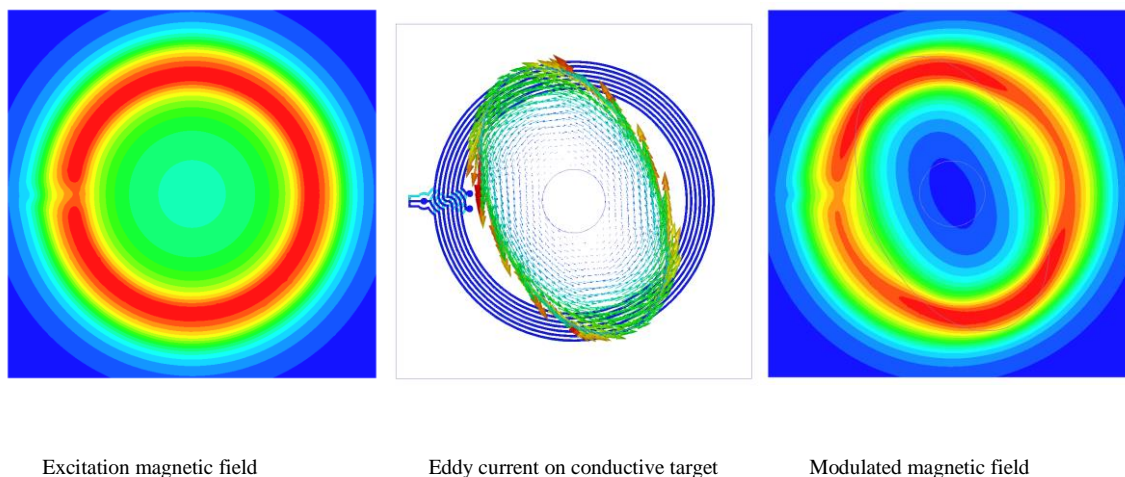
The inductive sensors, with their unique features, are widely used in applications such as geophysics research [12], earth research [13], aerospace investigation [14], biomedical devices [15] and most importantly in automobiles [16]. The inductive sensor consists of four main parts: An induction/excitation coil, a coupler/rotor, a reception coil and ASIC (Application-specific Integrated Circuit). A typical gas pedal inductive sensor is shown in **Figure 1-5**. The induction coil generates MHz level RF signal. According to Faraday's law, the RF signal generates an alternating magnetic field so that the eddy current is generated in the rotor. At the meantime, the eddy current also generates another alternating magnetic field, which can be sensed by the reception loop. Thus, the position/angular change can be detected precisely. Given their solid reputation, inductive sensors can work in the extremely harsh environment due to the sensing loops part can be separated from the circuitry. Unlike magnetic sensor, in Hall Effect sensors some doped semiconductor based electronics have to be placed at their sensing part.



**Figure 1-5 A typical structure of gas pedal inductive sensor (copied from [17])**

The working principle of inductive sensor is demonstrated in **Figure 1-6**. The theory is conducted from Faraday's law. As shown, in **Equation 1-1**, where  $\Phi$  represents the magnetic flux passing through coils with area  $A$  and turns  $n$ . Excitation coil generates an alternating magnetic field. Eddy current is induced on the rotor. Eddy current generates a secondary magnetic field pattern. A voltage is induced on the reception coil by this magnetic pattern. When the rotor rotates, the magnetic field pattern rotates accordingly, the induced voltage changes proportionally to the rotor angle position.

**Equation 1-1:** 
$$\mathbf{V} = -\mathbf{n} \cdot \frac{d\Phi}{dt} = -\mathbf{n} \cdot \mathbf{A} \cdot \frac{dB}{dt} = -\mu_0 \cdot \mathbf{n} \cdot \mathbf{A} \cdot \frac{dH}{dt}$$



**Figure 1-6 The working principle of inductive sensor**

As known for their robustness and reliability, most of the position sensors are fabricated through PCB technology, including those coil parts for excitation and reception. The excitation loop needs a lot of turns to generate the magnetic field strong enough to drive the sensor. However, the resolution of the commercialized high density PCB technology is around 50um [18]. With this limitation of the current fabrication technology, it is very difficult to shrink down the size of the device significantly.

In this thesis, the micromachining technology is introduced to fabricate the inductive loops after reviewing the drawbacks of the current PCB fabrication process.

### 1.3 Research Objective

The purpose of this thesis is to develop the next generation micro-inductive sensor based on the state of the art MEMS fabrication technology. The current PCB technology with its low cost is the most widely used fabrication method for inductive sensor. However, the backward of the size limitation makes it fails to match nowadays applications. The idea of the micro-inductive sensor initially started from the development of

micromachining technology, where the diameter limitation is no longer the parliamentary concerns, is the perfect solution of this issue. Thus, it is necessary to build this new type of sensor based on the cutting edge micromachining technology. The following steps will be carefully studied during the research:

- Design and optimize the next generation micro-inductive sensor based on MEMS fabrication process
- Simulate the prototype design in its working condition with professional simulation software supervising the later fabrication process.
- Develop a series of novel MEMS fabrication process suitable for the design. This includes wafer selection, seeding layers growth, photolithography, electroplating, etching process.
- System integration, the standard integration process will be investigated including wafer dicing process, wire bonding process, and surface mounting technology.
- Testing, compare the result with simulation and evaluate the performance.

## 1.4 Thesis outline

In this thesis five chapters are provided. In each chapter, one main topic is discussed and is organized as follow:

Chapter 1 mainly discusses the pros and the cons of current position sensors, and the possibility of miniaturization; why the state of art MEMS fabrication technology is introduced to take place of PCB technology. Lastly, the research objective and outline of

the thesis are given respectively in different sections to guide the readers for having better reading experiences.

Chapter 2 introduces the design principle, design and its optimization, and prototype simulation. Firstly, the design principles are investigated as a guideline for the later design. Based on the principle, different versions of devices are designed and compared with each other. A detail simulation is conducted on the optimized version, and results are listed for the future validation.

In chapter 3, the fabrication processes of miniaturized antenna coils are discussed, including sputtering, photolithography, etching and electroplating process. In the first half of the chapter, a brief introduction of microfabrication technology and how to take advantage of those technologies to our research are introduced. The fabrication procedures are introduced in details in the second half of this chapter.

The chapter 4 is divided into two halves. The first half introduces the system integration process upon fabrication. The testing part is performed in the second half where the probe station, LCR meter and impedance analyzer are used for corresponding inductance and resistance measurement and oscilloscope is utilized for the final test.

In chapter 5, a summary of the thesis' work is discussed; future work and suggestions are given as well.

## Chapter 2

### 2 Prototype Design, Optimization and Simulation

#### 2.1 Prototype design principles

The chief goal is to miniaturize inductive sensor into 10% of its original size. The sensor size is directly related to its coil diameter. With the drawbacks of the current PCB technology, the diameter of the coils are fabricated around 26mm and the room of largely downsizing the diameter is very limited. In this regard, with the benefit that MEMS fabrication technology brings to us, the diameter can be miniaturized to around 9mm with the proper process. Therefore before designing, guidelines of the design principles need to be established.

The quality factor  $Q$  that determines the behavior of oscillators is the most important parameter for the sensor: a low  $Q$  indicates large percentages of energy loss from the resonator. In other words, a high  $Q$  is always pursued in the design. The resistance  $R$  and inductance  $L$  that reflect the physical mechanisms directly are also very important characteristics in the sensor design and simulation. [19]  $Q$  is defined as:

$$\text{Equation 2-1: } Q = 2\pi \frac{\text{Energy stored}}{\text{Energy dissipated per cycle}} = 2\pi f \times \frac{\text{Energy Stored}}{\text{Power Loss}}$$

$$\text{Equation 2-2: } Q = Q(x) = \frac{\omega L(x)}{R(x)}$$

From the equation, in order to get high quality factor value, high inductance and low resistance is required. Low resistance can be gained through increasing the dimension of the wires and traces. Meanwhile, the high inductance can be gained through building more turns for the coil, increasing the diameter of the coil, or adding a ferrite core.

Besides, the cable length and the operation frequency also affect the performance of the sensor. The relatively low Q factor and large coil area are the two biggest issues of any RF microfabricated inductors. In different studies, to improve the Q factor, non-conductive and thicker substrate are applied to reduce the substrate loss [20-22]; bi-layer inductor are created to reduce the area size [23, 24]; high conductivity material and low-k dielectrics layer are used to reduce the resistive loss [25- 27]; magnetic materials are integrated to the coils to reduce the signal loss [28- 30]. Therefore, the following are the factors we take into first consideration [31]:

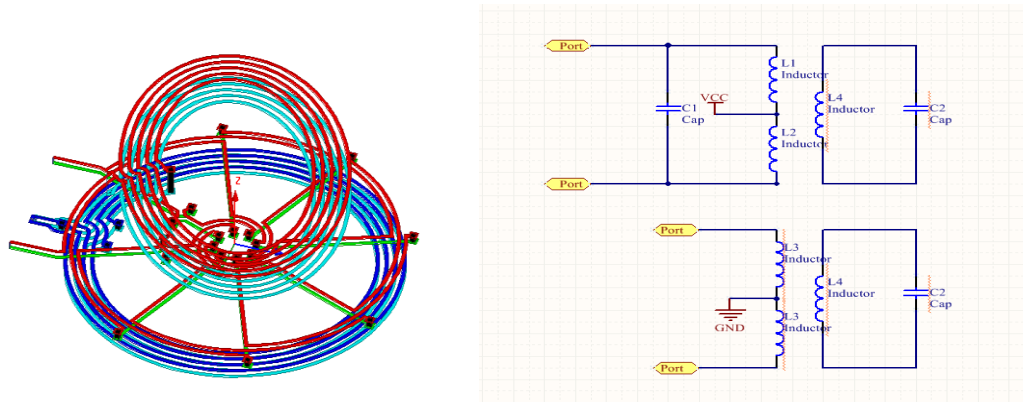
**Table 2-1 Factors in inductive sensor design**

<b>Factor</b>	<b>Why</b>	<b>How</b>
High quality factor	Fundamental factor of power consumption, noise	Increase working frequency; Increase inductance; Decrease resistance
High inductance	Increase Q and lower the power consumption	Increase the number of turns or diameter of the coil;  Add ferrite in order to increase magnetic field
Low resistance	Increase Q and lower the power consumption	Pick better conductive material for coil; Larger wire or thicker traces
Operate at high frequency	Increase Q and reduce the power consumption in the sensor	Reduce the system capacitance
Minimize cable length	Reduce the noise, and cost	Optimize circuitry arrangement



With these criteria above, details of prototype design and simulation will be discussed in the next section.

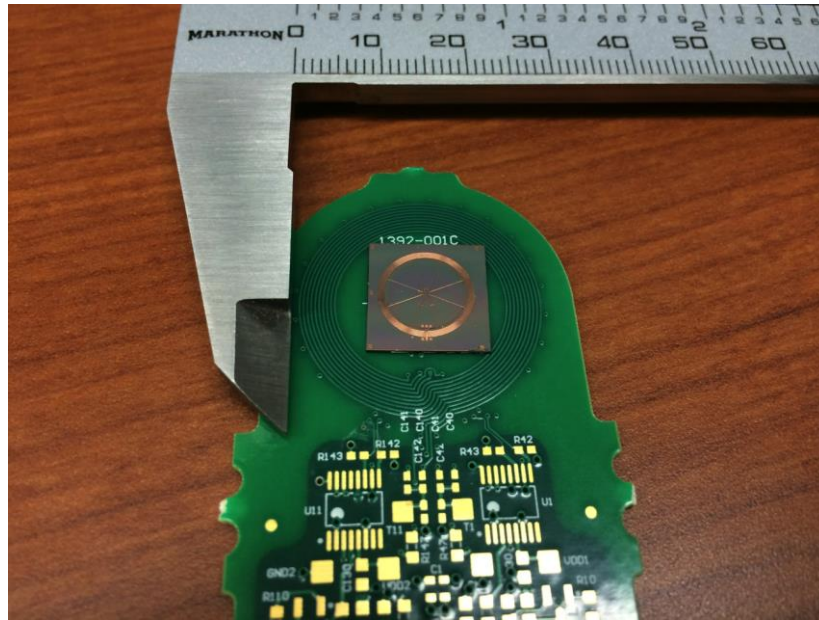
## 2.2 Prototype design and optimization



**Figure 2-1 Design of the inductive sensor coil and its circuit configuration**

The primary design is provided by KSR International Co. The round coil in blue color is the excitation coil, the round coil in red is the reception coil and the ellipse coil is the coupler, which functions as the rotor in position sensing. The excitation coil can generate oscillating magnetic field driven by LC resonant circuit under 4MHz frequency. The ellipse coil/rotor with another LC loop will induce the oscillating signal from the excitation coil and another oscillating magnetic field is induced. This oscillating magnetic field can generate the oscillating signal on the sensing coil and processed by ASIC. The sketch map of the device design is shown in **Figure 2-1**.

With primary design version 1.0, the diameter of the excitation coil is successfully reduced to 10.06mm from 26mm on high intensity PCB. Hence, the coil size is around 14.8% of the coil on the PCB. However, there are lots of issues with the primary design. Firstly, in its testing section, not significant level of signal can be detected from the sensing coil, which means the signal strength has to be improved. Secondly, there is still space to further shrink down the size to meet the target size. Thirdly, the good product rate is less than 30% with relatively high cost. The improvements need to be focused on the quality issue and the cost at the same time.



**Figure 2-2 Comparison of diameter between PCB fabricated coil and MEMS based coil**

With the possibility of miniaturization based on MEMS technology, in the following design, the diameter of the coil is reduced to around 8mm to 9mm. This will lead to a further miniaturization on size, comparing with PCB product, the size will reduce to its 9.5% to 12%. As previously mentioned, the tradeoff of the miniaturization will result in

higher resistance and lower inductance of coils. In this matter, increasing number of turns, width and thickness of the coil can offset the characteristics.

The dimension change on excitation coil can be roughly calculated by using Burkett's inductance equation [32].

$$\text{Equation 2-3:} \quad \mathbf{L = 7.88 \times \frac{(r_o+r_i)^2 n_1^2 \text{layers}^2}{13r_o-7r_i}}$$

For the version 1.0 design, the radius of the outer excitation coil,  $r_o=5.03\text{mm}$ , the radius of the inner coil,  $r_i=4.38\text{mm}$ , the number of turns per layer is 7, and two layers are designed to maintain enough signal strength. From **Equation 2-1**, the inductance of excitation coil in design version 1.0 is appropriately  $3.95\mu\text{H}$ .

Assume the width of the trace and the gap between traces are both equal  $50\mu\text{m}$ , then we know the relationship between  $r_o$  and  $r_i$  are:

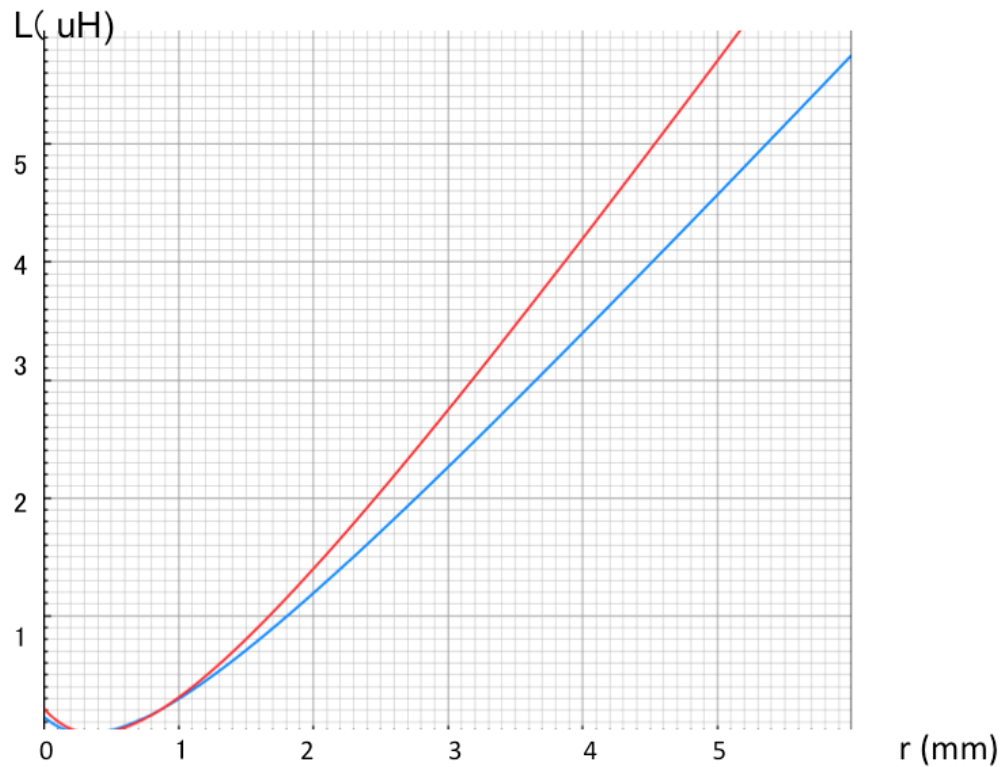
$$\text{Equation 2-4:} \quad \mathbf{r_o = r_i + (2 \times n_1 - 1) \times 50\mu\text{m}}$$

With the boundary conditions applying, when  $n=7$ ,  $\text{layers}=2$  the Burkett's inductance equation can be further simplified as:

$$\text{Equation 2-5:} \quad \mathbf{L = 7.88 \times \frac{(r_o+r_i)^2 n_1^2 \text{layers}^2}{13r_o-7r_i} = \frac{6177.92 \times (r_i+325)^2}{6r_i+8450}}$$

When  $n=8$ ,  $\text{layers}=2$  **Equation 2-6:**

$$\mathbf{L = 7.88 \times \frac{(r_o + r_i)^2 n_1^2 \text{layers}^2}{13r_o - 7r_i} = \frac{8069.12 \times (r_i + 375)^2}{6r_i + 9750}}$$



**Figure 2-3 Plot of coil inductance in different conditions**

**The blue curve describes the equation 2-5, where  $n=7$  and layers=2; the red curve describes the equation 2-6, where  $n=8$  and layers=2**

As shown in **Figure 2-3**, the blue curve indicates the equation 2-5, where  $n=7$  and layers=2; the red curve describes the equation 2-6, where  $n=8$  and layers=2. The value of the unloaded inductance is proportional to the outer coil size. If the coil diameter is reduced to 8.08mm, the coil size becomes 9.5% of the original size. Based on **Equation 2-3**, with the same condition of the trace and turns, the inductance is less than 3.2 $\mu$ H. With one more turn of coils added, the inductance becomes around 4.2 $\mu$ H. However, this kind of large size reduction in micro dimension brings device low efficiency and higher complexity in the fabrication process. From **Figure 2-3**, it is estimated that when the

diameter of the outer coil is around 8mm with 8 turns in total is the best condition for our design. Thus, adding one more coil turn after miniaturization compensates the induction of the excitation coil. For the same reason, one more turn will be added to reception coil. This conclusion will be verified and further discussed with more detailed simulation and fabrication process in the following chapters.

Another major improvement which has been made is that the size and the shape of pads and vias on the sensor are correspondingly optimized for enhancing fabrication quality. First of all, to avoid cracks and material peeling off from the device, sharper corners are usually avoided in micromachining process for the consideration of stress concentration. Therefore, all the pads corners are modified to round. Meanwhile, all the vias are redesigned as round for the sake of miniaturization. Additionally, all the pads size are increased from  $0.1\text{mm}\times 0.1\text{mm}$  to  $0.3\text{mm}\times 0.3\text{mm}$  so that capacitors can be directly implanted on the coil pads for packaging. By doing this, the cabling length is reduced; hence the noise in the circuitry is reduced.

Equally important, the excitation loops are optimized. In the design version 1.0, the later integration was a big issue for several reasons: in order to connect reception coil to the ASIC, three wires have to cross over the excitation coil, this action would potentially lead to mutual interference between excitation coil and sensing coil. Thus, the efficiency and the sensitivity of the sensor will be reduced. If the lengths of those wires are too short, the wire might touch the excitation coil and cause short circuit. In the working condition, the coupler is required to be placed very close to the excitation and reception coil for the better signal strength. In this case, the efforts that have been done to prevent short circuit between connecting wire and excitation coil may lead to another possible short circuit

situation between wire and coupler. Knowing this fact, the loops need to be optimized. To achieve this goal, part of the excitation loops at the top layer will be placed to the bottom layer and connected through extra vias with careful design.

With all the improvement, two more Versions, 2.0 and Version 3.0 of the design are developed as shown in **Table 2-2** below:

**Table 2-2 The major parameters of the different versions of design**

<b>Major improvement</b>	<b>Version 1.0</b>	<b>Version 2.0</b>	<b>Version 3.0</b>
<b>Coil size compared to PCB coil</b>	14.8%	9.47%	11.9%
<b>Key parameter of excitation coil</b>	Two layers  7 turns  $r_o=5030\mu\text{m}$  $r_i=4380\mu\text{m}$  Trace width= $50\mu\text{m}$  Trace gap= $50\mu\text{m}$	Two layers  8 turns  $r_o=4040\mu\text{m}$  $r_i=3290\mu\text{m}$  Trace width= $50\mu\text{m}$  Trace gap= $50\mu\text{m}$	Two layers  8 turns  $r_o=4540\mu\text{m}$  $r_i=3640\mu\text{m}$  Trace width= $50\mu\text{m}$  Trace gap= $50\mu\text{m}$
<b>Key parameter of reception coil</b>	Two layers  1 turn  Trace width= $20\mu\text{m}$  Trace gap= $30\mu\text{m}$	Two layers  2 turns  Trace width= $30\mu\text{m}$  Trace gap= $30\mu\text{m}$	Two layers  2 turns  Trace width= $30\mu\text{m}$  Trace gap= $50\mu\text{m}$
<b>Pad and vias design</b>	Pad size: $300\mu\text{m}$ $\times 300\mu\text{m}$ square  Via size: $100\mu\text{m}$ $*100\mu\text{m}$ square	Pad size: $600\mu\text{m}$ $\times 600\mu\text{m}$ square  Via size: $100\mu\text{m}$ diameter circle	Pad size: $600\mu\text{m}$ $\times 600\mu\text{m}$ square  Via size: $100\mu\text{m}$ diameter circle
<b>Noise reduction optimization</b>	No	Yes, with enhanced loops design	Yes, with enhanced loops design
<b>Predicted Inductance</b>	$4.6\mu\text{H}$	$4.26\mu\text{H}$	$4.86\mu\text{H}$

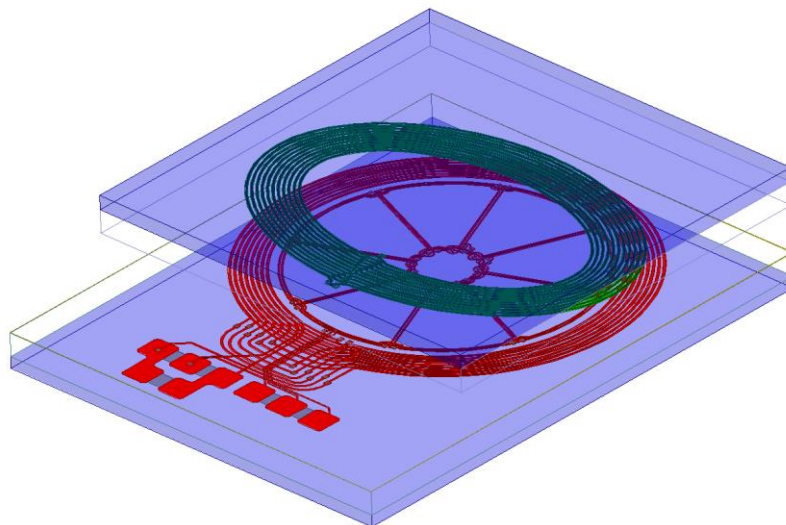
The design version 3.0 with the best balance of the pros and cons is the blue print of the final prototype. The design Version 1.0 and Version 2.0 are both given up due to the difficulties in fabrication and integration process, more details will be demonstrated and investigated in the chapter 3 and chapter 4. In the next section, the discussion of the simulation will only base on the final prototype design version 3.0.

## 2.3 Prototype simulation

A detailed simulation was conducted based on HFSS software. HFSS is electromagnetics simulation software using finite element method. With its excellent analytic function, the simulation result can be used to verify the design and the fabrication process [33]. A real scale model of the prototype was designed in HFSS and the simulation of excitation coil and coupler coils' physics quantities in different frequency was created as well. By using Maxwell equations, the electromagnetic field in different medium can be calculated. In the prototype model, the coils facing with other are sandwiched through substrates and ferrite layers. The substrate, ferrite and coil layers were created in sheet model with different adjustable thickness. The frequency response under different frequency was analyzed through adding sweeping function in analyzing settings. The coil simulation results are shown with 20 $\mu$ m thickness copper thickness. The fact that the inductance was slightly smaller than the former estimation by Burkett's inductance equation was due to the irregular circle design on the version 3.0. The purpose of this simulation was to



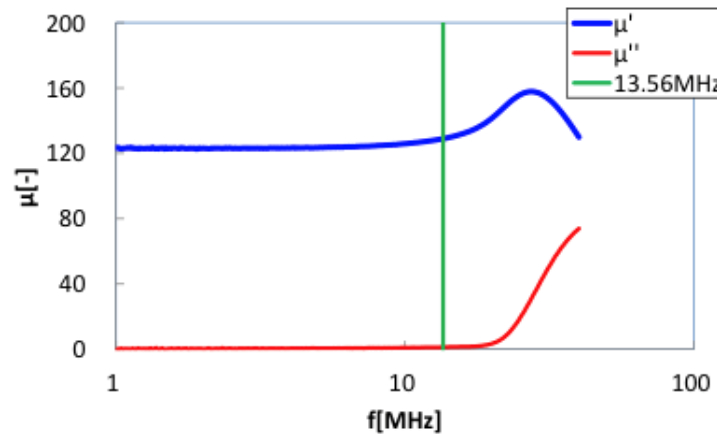
introduce the coils into the real working condition, record the resistance and inductance in simulation and use them for the fabrication.



**Figure 2-4 Simulation of prototype model in HFSS environment**

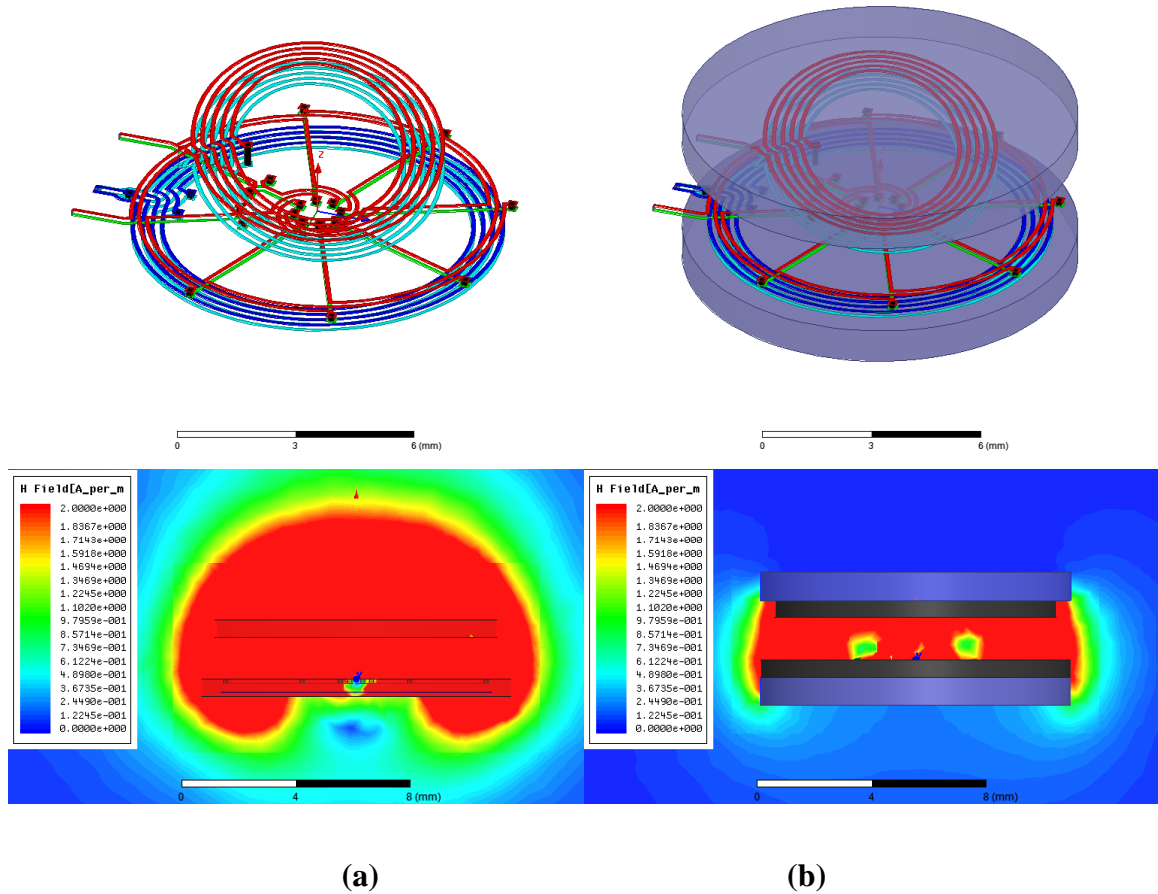
It is known that the magnetic material can increase the inductance and signal strength [34, 35]. For spiral coil it is not easy to add a traditional magnet core, so it is better to integrate the magnet underneath the coil to act as magnetic sheet. For ferromagnetic alloys, due to their low ferromagnetic resonance, their magnetic property cannot be sustained in high frequency. Also, eddy current may be generated in the alloys due to their low resistivity. Ferrite draws our attention due to its high permeability, low resistivity, and low cost [36]. Unlike ferromagnetic alloys, the high ferromagnetic resonance and low imaginary part of permeability  $\mu''$  can keep high Q factor in MHz and even in GHz range [37, 38]. Beside, this non-conductive ceramic materials known as its low eddy current losses in electronics, so it is an ideal material in our case to enhance the signal strength without producing unwanted eddy current [39]. The ferrite can be

fabricated on the substrate through spin coating or inkjetting technology, however, considered the difficulties in fabrication and characterization the ferrite model was from MARUWA-FSF131 series. The **Figure 2-5** displayed the permeability characteristics of FSF131, the imaginary part of permeability  $\mu'' = 0$ , and the real part of permeability  $\mu' = 120$  in the 1-10MHz range.



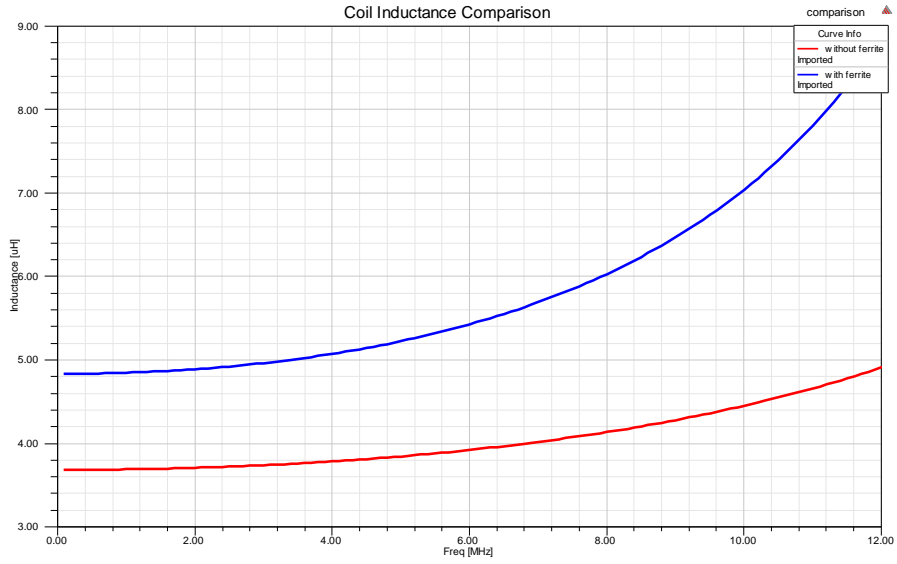
**Figure 2-5 Permeability characteristics of ferrite FSF131**

To verify this theory, the simulation of H field between coils was conducted. As shown in **Figure 2-6**, compared with the simulation without ferrite layer, the device with ferrite had better signal strength. The magnetic fluxes between two layers were confined, and the ferrite layers acted as shield. Thus, the device efficiency would increase by adding ferrite shield. And this would be further verified by simulating the inductance, resistance and Q factors on the excitation coil and coupler individually.

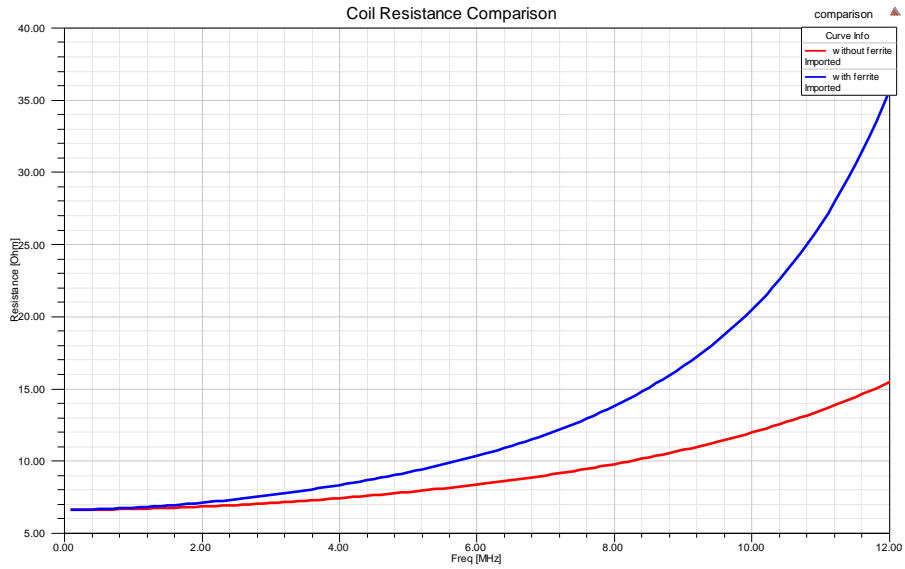


**Figure 2-6 Plot of magnetic field between coils: (a) without ferrite shield; (b) with ferrite shield.**

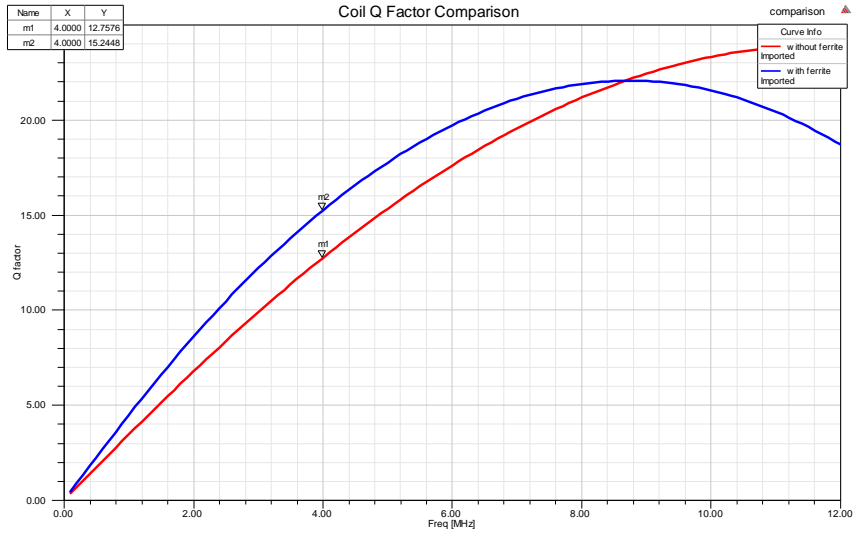
The simulation results showed that with ferrite layer attached, the inductance of the coil was increased significantly. And also in designated frequency, adding ferrite layer can result in 20% improvement in Q factor under the frequency of 4MHz. The importance of high Q factor in this research has been clearly discussed and stated. In chapter 4, the test results will be used to verify the simulation.



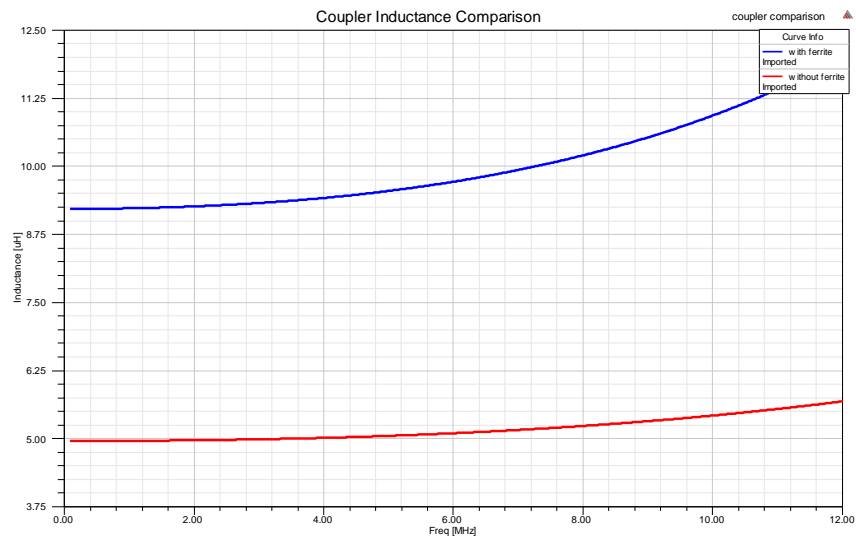
**Figure 2-7 Excitation coil inductance comparison**



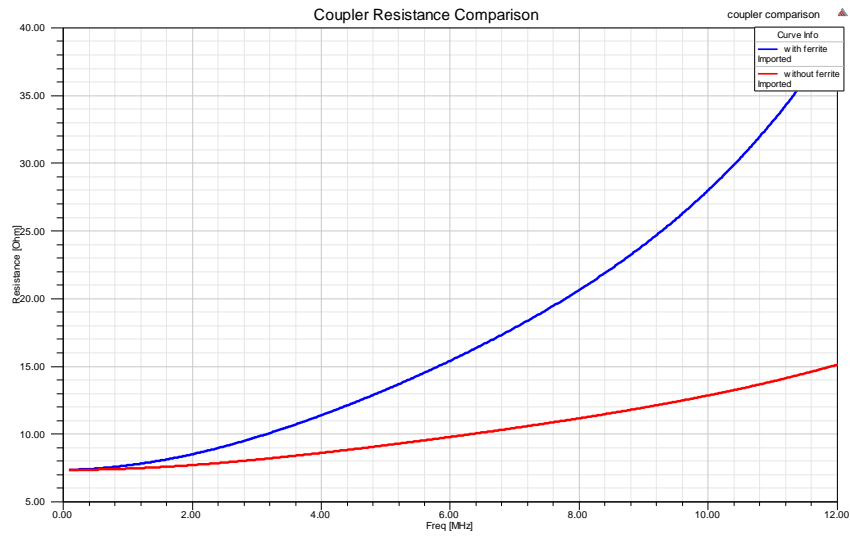
**Figure 2-8 Excitation coil resistance comparison**



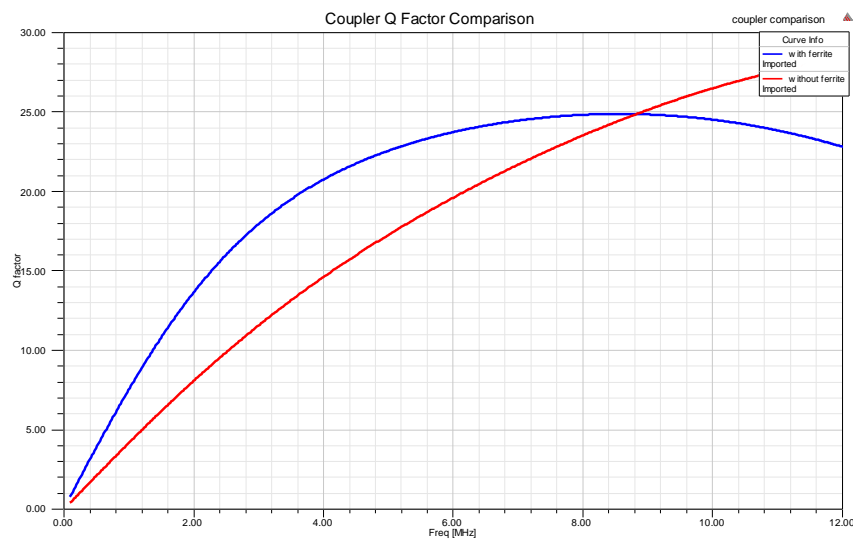
**Figure 2-9 Excitation coil Q factor comparison**



**Figure 2-10 Coupler coil inductance comparison**



**Figure 2-11 Coupler coil resistance comparison**



**Figure 2-12 Coupler coil Q factor comparison**

## 2.4 Conclusion

The design principle was introduced at the beginning of the chapter. With the design goal determined—to achieve higher Q factor value, low resistance and high inductance were needed. With the factors and criteria stressed in the design principle section, the miniaturized prototype design was successfully conducted with three different versions

displayed. The inductance quantities were firstly estimated by using Burkett's inductance equation, the version 3.0 has higher inductance and better overall package were selected to conduct further simulation. In the simulation part, the simulation was done by ANSYS HFSS. The advantage of adding ferrite layer was verified by simulation. Also, for the future evaluation, the inductance, resistance and Q factor of the excitation coil were calculated and displayed in different frequency response from **Figure 2-7** to **Figure 2-12**.

## Chapter 3

### 3 Microfabrication

#### 3.1 Introduction to microfabrication technology

Microfabrication is a process that builds structures on devices in the dimension of micrometer scale, or even down to nanometer. The earliest microfabrication refers to integrated circuit fabrication in microelectronics. In the last 30 years, this process has been developed to match with various applications, such as MEMS and lab-on-a-chip technology. Miniaturization is always a challenging task in all different fields. Taking advantages of micromachining methods like photolithography, thin films, electroplating, etching, bonding, the microstructure with certain functions are manufactured, for example, microcantilevers, microfluid inkjet head, microtransistors and so on [39, 40]. Many different microfabrication processes are performed for building a device, usually they include growing thin films, patterning the films with certain structure, etching away the undesired part.

In our research, double layer coils are needed to generate significant signal strength. Considering the complexity of the structure every step has to be well designed. So it is extremely important to understand the mechanisms of each fabrication process. In this section, the processes related to our research are introduced.

##### 3.1.1 Substrates

The microfabricated devices are usually built on thick substrates. A matched substrate not only support material growth but also easy the process handling. Silicon wafer is the most widely used substrate and has been playing a big role in microelectronics. Almost all the

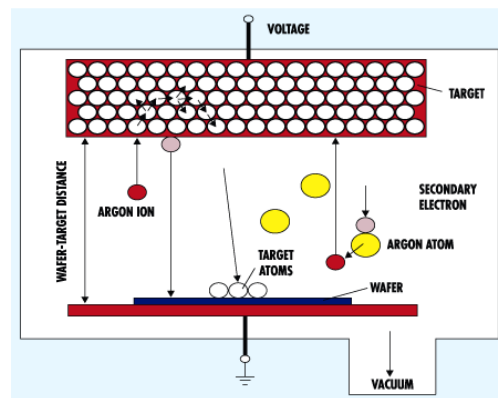


integrated circuits are fabricated on the silicon. Varieties of the microdevices are fabricated by taking the advantages of the outstanding electrical and mechanical properties from silicon [42, 43]. In addition, the possibilities of integrating devices with circuitry on silicon lead to its popularity in MEMS. Glass, with its unique optical features, is another commonly used substrate mostly in optical applications [44]. Polymers are mainly used in the fabrication of flexible devices or in clinical applications with the consideration of human body compatibility [45].

### 3.1.2 Thin film deposition

#### Sputtering

In microfabrication, sputtering and evaporation are the most important physics vapor deposition process. Unlike evaporation, during the deposition process sputtering generates much less amount of heat. This makes it becomes ideal for more applications that requires high melting point material thin films and substrate cannot stand the high temperature. Moreover, thin films deposited by sputtering are usually have better adhesion to the substrate.



**Figure 3-1 Schematic of sputtering deposition process (Adopted from [46])**

Sputtering refers to the phenomenon where the atoms escape from the target surface due to the momentum exchange with high-energy ions [47]. The sputtering deposition process is usually conducted in a highly vacuumed space with an inert (usually argon) gas flow. The Argon is ionized when the high voltage is applied on the anode and cathode in the chamber. Driven and accelerated by the electrical field, argon ions with high energy hit the cathode surface where the target is set. The ions with high energy collide with atoms hit on the target and the momentum exchanges occur. Similar to raindrops hit a pool, the atoms on the surface obtain enough energy to escape from the surface and land on the anode where the substrate is placed. As the time pass, more and more atoms from the target will gather on the substrate, thus the thin film is formed. The deposition rate varies from different targets, and can be adjusted thorough controlling the power, Argon flow flux and vacuum rate. The typical deposition rate of sputtering is around 10 to 20nm/min for metals. Usually sputtering is used for building thin films under the thickness of 5 $\mu$ m.

### **Electroplating**

In microfabrication, the electroplating has been widely used for metallization and interconnection in IC since the IBM first published the paper in 1998, called Damascene process [48]. Electroplating refers to the deposition process that takes advantages of electrical current to coat metal on conductor through reduction reaction.

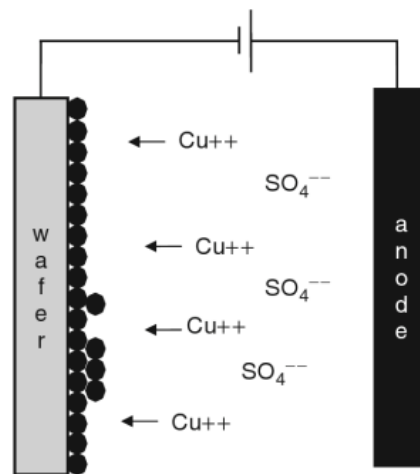
For the electroplating process, a simple kit consists of a power source, electrodes, bath container, electrolyte and connecting wires. Taking copper electroplating as an example. The substrate acts as a cathode in copper electrolyte solution. The anode can be either copper metal or passive electrode materials such as platinum or graphite. As shown in **Figure 3-2**, the electrodes are connected to the power supply and immersed into

electrolyte solution. As the process starts, the current helps the copper anode dissolved into the electrolyte solution, at the same time, the same amount of Cu ions in the solution gather at cathode, forming copper thin film [49]:

At the cathode:



At the anode:



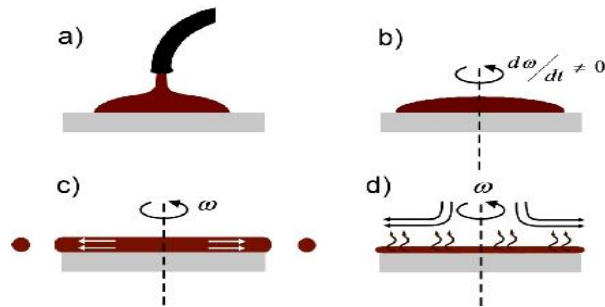
**Figure 3-2 Simplified schematic of electroplating process**

In really usage, the mixture of electrolytes is very complex. It also contains a lot of additives, such as acid, salt, modifiers. For instance, a good Cu bath includes copper sulfate, sulfuric acid, hydrochloric acid, carrier and brightener. The copper sulfate supplies Cu ion for deposition. The acids in the solution balance the PH. And the other

additives such as modifiers can improve the Cu growth quality by controlling the nucleation size. Equally important, in some applications, the pulse-reverse power source can also be used to improve the thin film quality. The deposition rate of electroplating process is from 0.1  $\mu\text{m}/\text{min}$  to 100  $\mu\text{m}/\text{min}$  depending on the current intensity. With this flexible feature, the electroplating takes place of the other deposition process especially when a relatively thick metal thin film (more than 5 $\mu\text{m}$ ) needs to be deposited. However, for microfabrication, a balance between deposition rate and film quality need to be considered.

### **Spin Coating**

Spin coating is another method that is commonly used in microfabrication. With the conventional microfabrication deposition process, inorganic films can only be deposited no more than few micron meters. Polymers are the main materials for this process to take place of the inorganic film can reach up to 1000 $\mu\text{m}$ . The typical applications include photoresist spinning and spin on dielectrics. The photoresist spinning is usually used to create micromold pattern by photolithography at later stage, is essential in MEMS and microelectronics. And the spin on dielectrics is for creating insulation film in micro devices. Polymers are the main materials for this process [49]. **Figure 3-3** gives the idea of spin coating process. The coating material is dissolved into a special solvent and put on the substrate chunked on a spinner. The spinner can spin in a very high speed from 1000rpm to 5000rpm. Rotating in such high speed, the solvent is well distributed on the substrate. Lastly, the coating process is done after the solvent evaporated by baking. The film's thickness can be controlled by adjusting the speed and the acceleration of the spinner. At the meanwhile, the concentration of the solution also affects the thickness.

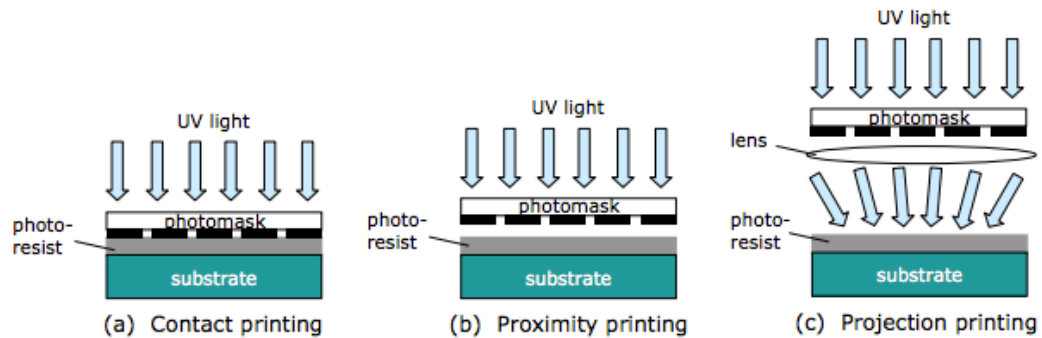


(a) Solvent dispense; (b) Spread process; (c) Spinning process; (d) Baking

**Figure 3-3 Schematic illustration of the steps of spin coating (Adapted from [50])**

### 3.1.3 Photolithography

Photolithography, in microfabrication, refers to a process that is used to transfer pattern onto substrate. The diameter of the pattern usually can down to few nanometers. With the high precision, this cutting edge technology is the most important pattern technology in manufacturing chips and MEMS devices. Taking the standard CMOS process as example, usually more than 50 times of photolithography process are done on any contemporary computer integrated circuits [51]. The patterns are transfer onto photosensitive materials with a series of steps. Firstly, the photosensitive chemical is spun on the substrate. Then the UV light in certain wavelength goes through a mask with desired pattern reaching on the surface. The pattern is transferred onto the photosensitive materials after chemical treatments and is really for the subsequent process.



**(a) contact printing; (b) proximity printing; (c) projection printing**

**Figure 3-4 Illustration of three different types of photolithography (Adapted from [52])**

There are three different types of photolithography technologies: projection, proximity and contact. As shown in **Figure 3-4**, they are categorized by the way the photomask and photoresist contact. For contact and proximity printings, they are the most commonly used style in research institutions. The resolution can reach to a few micrometers. The term “contact” and “proximity” mean the photoresist and the mask are in contact or are very close to each other during exposure. The projection printing photolithography allows the UV light passes through a special optical system can improve the resolution up to 10 times. However, this system is very pricy because of the complexity of the optical system.

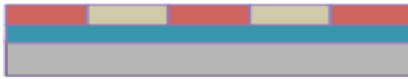
There are three main different processes after the patterns are transferred on the substrate: LIGA, etch-back and lift-off process. Each of them with their unique features as shown below:



1. Deposit the thin film of desired material



2. Coat and pattern photoresist



3. Deposit thin film in the pattern



4 Remove the photoresist

### (a) LIGA process



1. Deposit the thin film of desired material



2. Coat and pattern photoresist

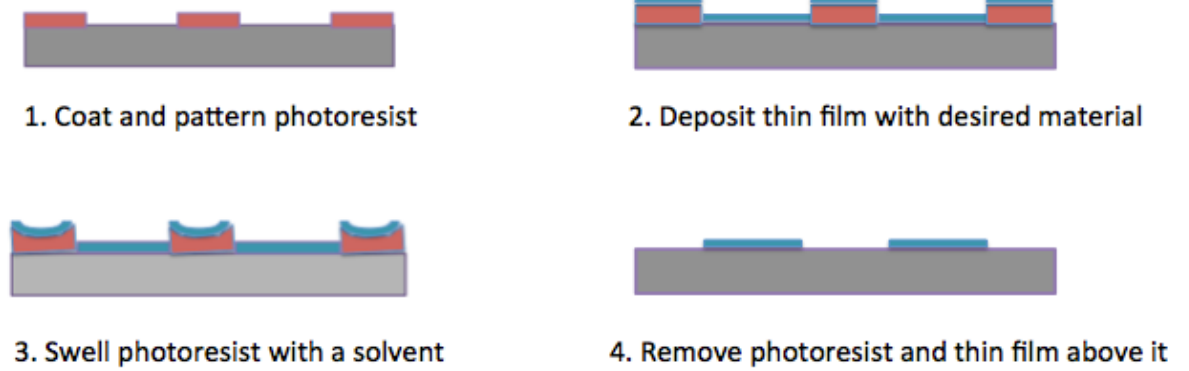


3. Etch film using photoresist as mask



4 Remove the photoresist

### (b) Etch back process

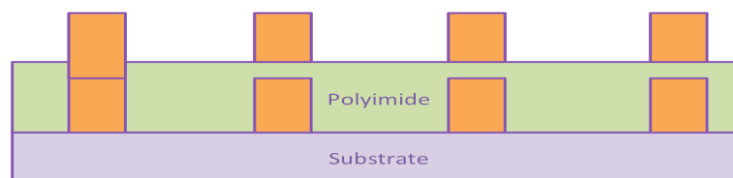


### (c) Lift-off Process

**Figure 3-5 Schematic of (a) LIGA process; (b) Etch back process; (c) Lift-off process (Adapted from [49], [53], [54])**

## 3.2 Process design

Several microfabrication process mechanisms are illustrated and reviewed in the last section. The equipment we can access in this project is in Western Nanofab, Macmaster Nanofab and KSR research center. The key factor for the design is to develop a simple and reliable procedure that can be finished with accessible resources. In addition, the procedure later can be adapted to mass production.



**Figure 3-6 Cross-sectional diagrams of the device structure**



As shown in **Figure 3-6**, the device consists of 4 different layers: the substrate, bottom coil layer, insulation layer with via, and the upper coil layer.

### 3.2.1 Substrate selection

In our application, to match with copper coil fabrication, the substrate has to be non-conductive and non-reactive with acid. Si seems to be an ideal substrate in the beginning.

However, Si is a semiconductor material can become conductive when doped.

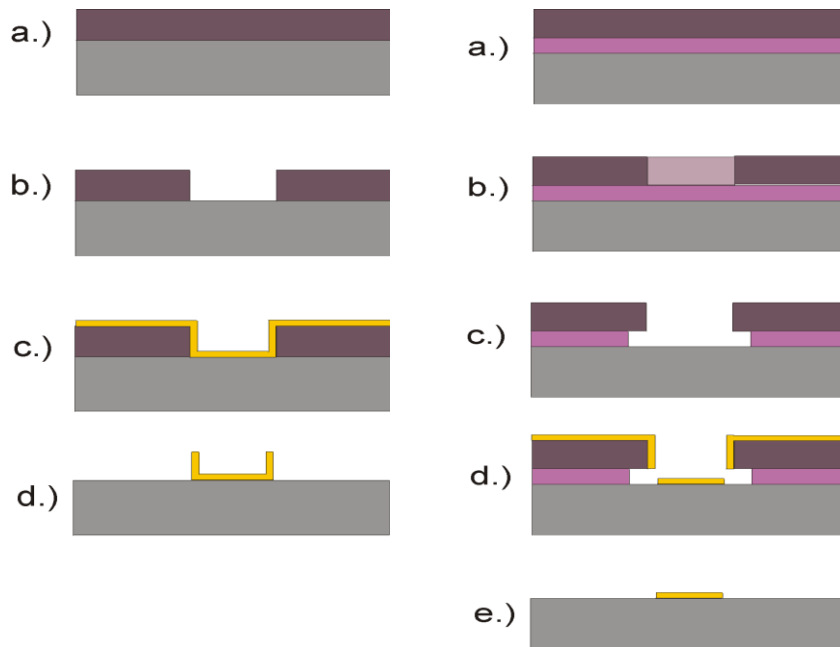
Considering the future possibility of integrating coils with circuitry, Si substrate will be inevitably doped and gain unwanted conductivity. So Si is not the suitable substrate here.

To solve this potential issue, Si substrate with SiO<sub>2</sub> layer is the ideal solution. With all the advantages of Si substrate, the SiO<sub>2</sub> layer can prevent Si from being doped. In the end, the 4-inch Silicon wafer with 2 $\mu$ m Silicon dioxide is selected as substrate in this project.

### 3.2.2 Coil fabrication process selection

In micrometric scale, lift-off process is commonly used to create patterns using sacrificial layers. In this process, a sacrificial layer is fabricated firstly by using an inverse mask pattern. Then the metal is deposited on the substrate and the sacrificial layer is removed.

By doing this, any unwanted metal on the sacrificial layer is washed away at the same time. Thus, the certain metal pattern is created. However, the retention issue in lift-off process occurs time to time. Unwanted metal patterns sometimes stick on the substrate and couldn't be lifted off.



**Figure 3-7 Illustration of lift off process and bi-layer lift off process**

To improve this issue bi-layer lift off process is investigated as shown in **Figure 3-7**. The two sacrificial layers have different dissolve rate in the developer and the undercuts can be formed in this case. The undercuts can help lift-off solution to infiltrate, so the retention issue can be solved. All the lift-off processes are compatible with e-beam and sputtering deposition. However, both of the two technologies have relatively slow deposition rate which will largely lower the fabrication efficiency. Another promising method is LIGA. It is possible to produce elaborate metal patterns on wafer through electroplating. The **Figure 3-5 (a)** illustrates the process: a conductive thin seeding layer is fabricated on the substrate. Photoresist is spun, exposed and developed on the wafer. Then the wafer is put into the bath and plated. The metal pattern can be formed after removing the photoresist and etching away the seeding layer [48].

Compared to lift-off process, LIGA process is supreme to our application. First of all, to form 20 $\mu$ m thickness copper, it takes electroplating process about 1-2 hours. At the meanwhile, it takes e-beam and sputtering deposition 5-10 hours to achieve corresponding thickness. Secondly, the cost is very little by using electroplating. Last but not the least, the electroplating process has the potential of gaining thicker coils. The electroplating process allows metal over plating, but with lift-off process the metal thickness should not exceed the photoresist.

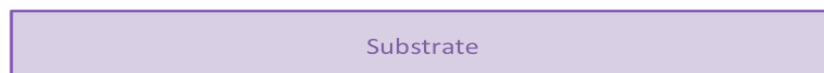
### 3.2.3 Photoresist selection

Before electroplating process, the inverse photoresist pattern needs to be arranged on the substrate. This requires the photoresist to (1) have good adhesion with the seeding layer; (2) ability to stand in the solution without damaging the pattern; (3) have enough thickness to support the coil deposition. SU-8, KMPR and AZ 9260 can satisfy our demand, the other common photoresist we can access, such as Shipley series, in Western Nanofab are given up due to the thickness dimension limitation. Considered the photoresist has to be removed after deposition, SU-8 [55] and KMPR [56] are negative photoresist with their reputation of being removed. AZ9260 [57] is positive photoresist, and can be easily removed by Acetone or PG remover afterwards. Thus, AZ9260 is the ideal photoresist for our electroplating process.

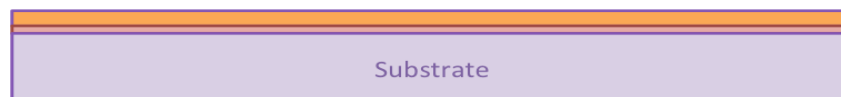
After successfully building the copper coil, the coil needs to be covered by a thin insulation layer. This layer has to (1) be non-conductive material to separate the bi-layer coil from each other (2) Compatible with the photolithography process to form vias collection (3) have excellent mechanical property to support the device structure. Though research, polyimide and SU-8 are the ideal polymer materials providing features we need.

Polyimide and SU-8 are vital materials used as insulation layer in MEMS and Microelectronics technology. Both the materials have excellent physics properties, are compatible with electroplating process. Initially, it is very difficult to pick one from the other. However, the polyimide has its unique advantages in implantable devices and flexible devices. And the key of this project is the multiple coils fabrication process that is known having potential to play a very big role in biomedical devices and flexible electronics [47]. Based on this fact, considering the future research opportunities, polyimide is chosen as insulation layer. Therefore, photoresist HD 4100 is purchased for the fabrication.

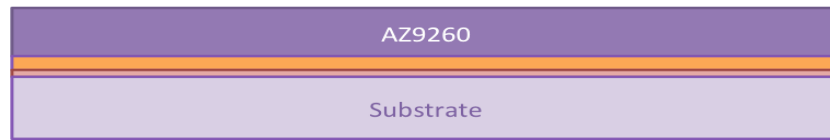
After the substrate, deposition methods, patterning technology, types of photoresist are all determined, the fabrication process can be summarized as below:



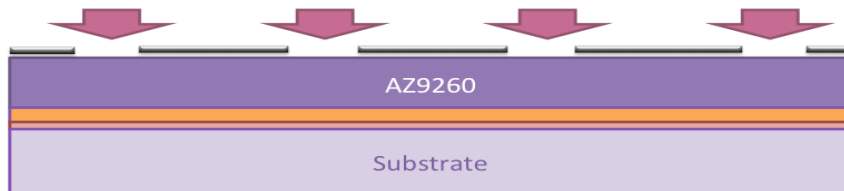
**1. The Silicon oxide wafer is cleaned through pretreatment**



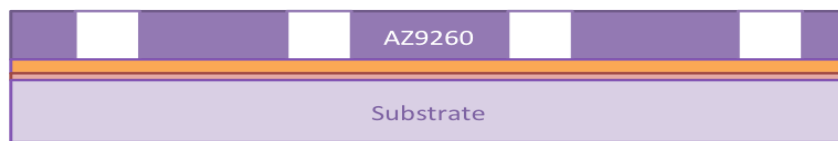
**2. Ti/Cu seeding layer is deposited by sputtering**



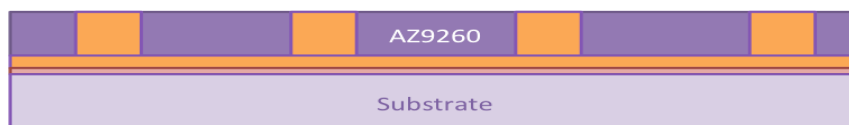
### 3. Spin coat AZ9260 photoresist



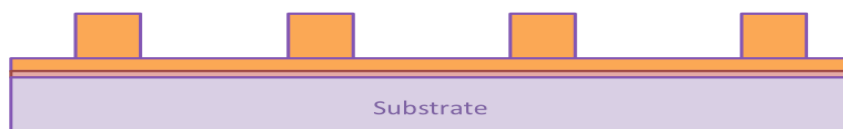
### 4. Exposure by photolithography



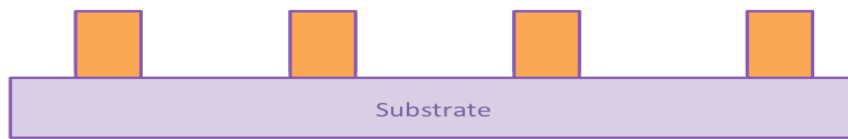
### 5. Pattern developing



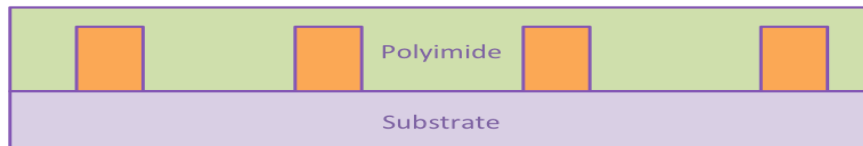
### 6. Grow copper by electroplating



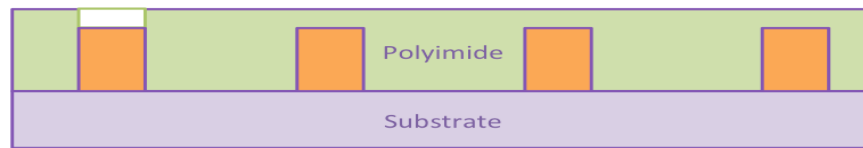
### 7. Strip photoresist



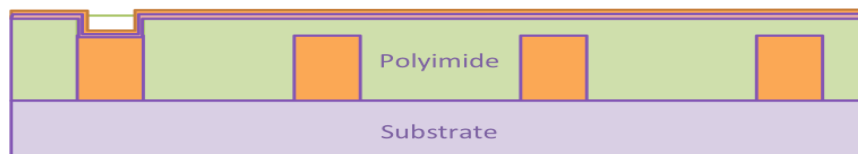
**8. Remove seeding layer by Ti and Cu etchant**



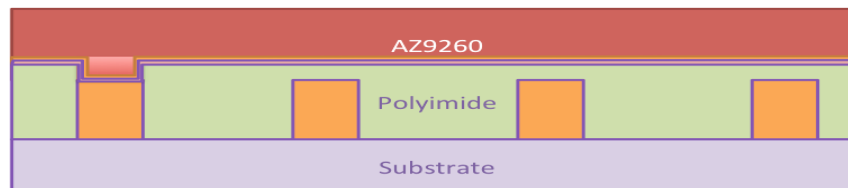
**9. Spin coat HD4100 photoresist as insulation film**



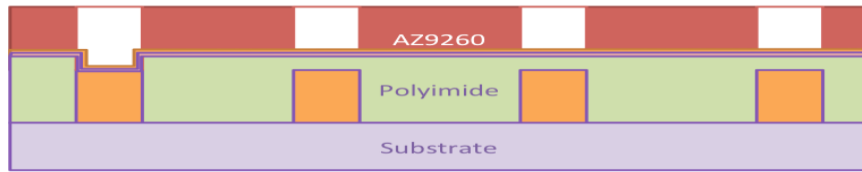
**10. Exposure, development and cure**



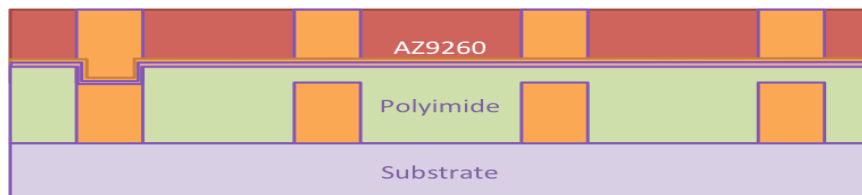
**11. Deposit the Ti/Cu seeding layer**



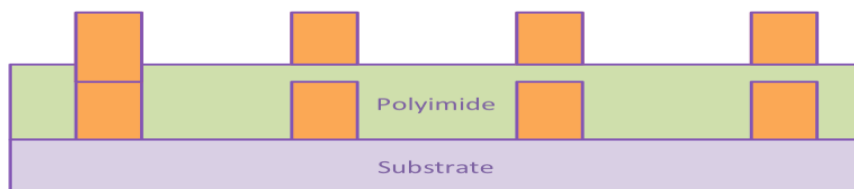
**12. Spin coat the second AZ9260 photoresist**



### 13. Micromold for electroplating is created by photolithography



### 14. Copper electroplating



### 15. Strip photoresist and seeding layer

Figure 3-8 Diagrams of the fabrication process steps

## 3.3 Microfabrication Process

In this section, the manufacture procedures were investigated in detail. This section is divided into 3 small sections: the first coil layer fabrication, the insulation layer and via fabrication and the second layer fabrication.

### 3.3.1 First coil layer fabrication

#### **Substrate Pretreatment**

As discussed, the 2 $\mu$ m silicon dioxide 4-inch Si substrate was chosen for this process. Before manufacturing, the substrates had to be cleaned thoroughly to remove the any potential particles and chemical contaminations. This process can improve adhesion significantly between substrate and seeding layers. Unlike the cleaning process of Si wafer without dioxide, our wafer cannot be cleaned by RCA or HF process. Hence, the nanostrip solution was used to remove these contaminations.

Preheated the nanostrip up till 80 degree to maximize the effectiveness, immersed the wafer into solution for 90 seconds with proper agitation. Then the substrate was rinsed by deionized water thoroughly before putting into Semitool wafer cleaning machine. The clean machine helped removing all the residual chemicals, such as nanostrip. With designated receipt in the machine, the substrate was rinsed for 15min and blow dry.

#### **Seeding layer deposition**

The Edwards Auto500 series sputter deposition system in Western Nanofab was utilized to grow seeding layer. The Edwards Auto500 contains multiple targets in the chamber, and DC/RF power source individually. This feature allows multiple layers can be growth at one time without reopening the chamber reduces the risk of contaminating. The Edwards Auto500 is shown as below:

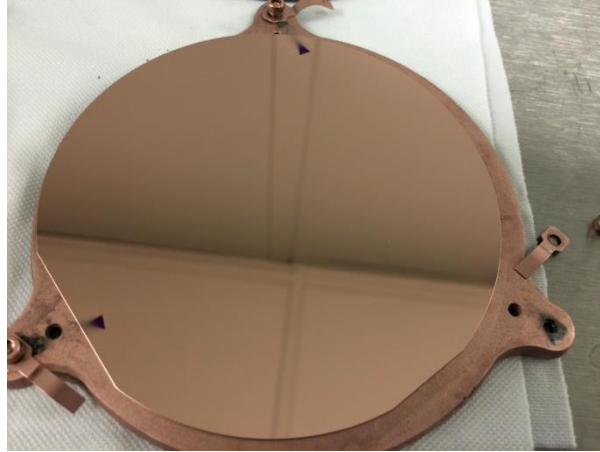




**Figure 3-9 The Edwards Auto500 sputtering system in Western Nanofab**

Each time 4 pieces of 4-inch wafers were placed into the chamber to reach the maximum capacity. The whole chamber was vacuumed down to  $5 \times 10^{-5}$  bar to make sure the deposition was under pure circumstances. Prior to the copper layer, a very thin Ti layer was usually grown. Ti was known for its good adhesion on both Silicon oxide and copper surface, so it was used as an adhesive layer between substrate and copper.

100 $\mu$ m thickness of Ti was sputtered by RF power source under the power of 100 watt with 15mins deposition time. Thereafter, switch to the DC power source and the corresponding copper target. 300 $\mu$ m thickness copper was prepared in 15mins under the 100watts DC power source. During the deposition process, all the samples were rotating at 15rpm to improve the uniformity of the seeding layer. The successfully fabricated wafers are shown:



**Figure 3-10 Ti/Cu seeding layer coated on the wafer**

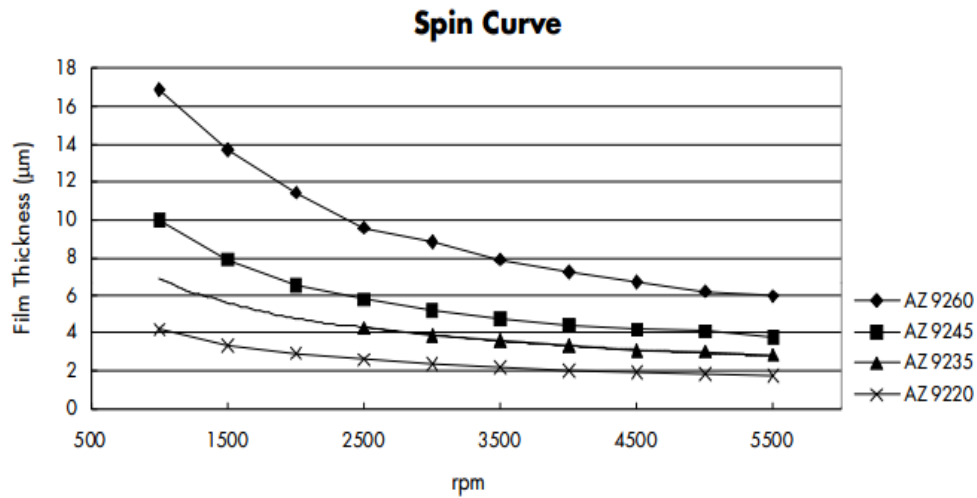
In the picture, the reflective surface indicates the seeding layer had been perfectly fabricated with very high uniformity and low roughness. Some part of the wafers were not covered by seeding layer was due to the design of the holder itself. However, in our research this uncovered surface helped us in the later etching process and this will be discussed later as well.

### **Spin Coating**



**Figure 3-11 Solitec 5110 spinner in Western Nanofab**

Upon photolithography process, certain thickness of photoresist needs to be spin on the substrate. This process is done by Spinner Solitec 5110 (**Figure 3-11**) in the yellow cleanroom, where there are very little particles and no UV for lighting in the room. In order to grow 20um thickness copper, the photoresist layer should be at least 16-18 $\mu\text{m}$  to support the growth. According to the data sheet below **Figure 3-12**, the thickest layer that AZ9260 can achieve is 18um can be done at the 1000rpm spin rate. As our research shows, lower the spin rate is possible to create a thicker layer, however, the uniformity of the layer cannot be guaranteed.



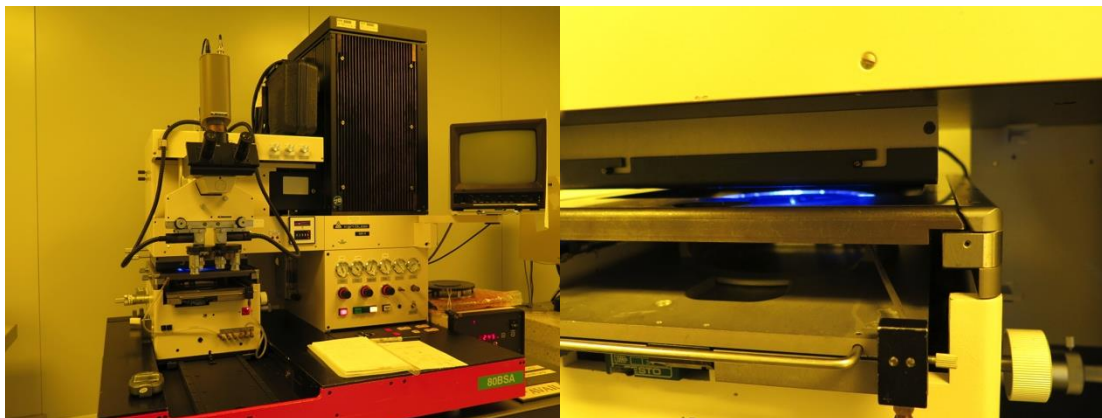
**Figure 3-12 The spinning speed vs film thickness relation of AZ series photoresist (Adapted from [57])**

First of all, the position of the substrate was adjusted and set at the center of the spin holder. If the wafer was not put properly, the uniformity could be largely decreased during spinning. Then, making sure there was no bubble in the photoresist and squeeze the resist to cover at least half of the wafer. Set the spread ramp to 500rpm with 100rpm/sec acceleration for 8 seconds, this step allowed the photoresist fully covered the

wafer. In the spin cycle, set the spin speed at 1000rpm with 500 rpm/s acceleration for another 55 seconds. For this formula, the thickness of the film was around 17 $\mu$ m.

The coated substrate was transferred onto a hot plate to evaporate the solvent, called soft bake process. In this process, the wafer needed to be gently moved to the hotplate right after the spinning finished. Turned on the hot plate and increase the temperature from room temperature to 110°C and bake for 3mins. After 3mins, turned off the hot plate, and let it cooled down to room temperature. This could prevent the unwanted bubbles generate due to the sudden temperature change.

### **Photolithography process**

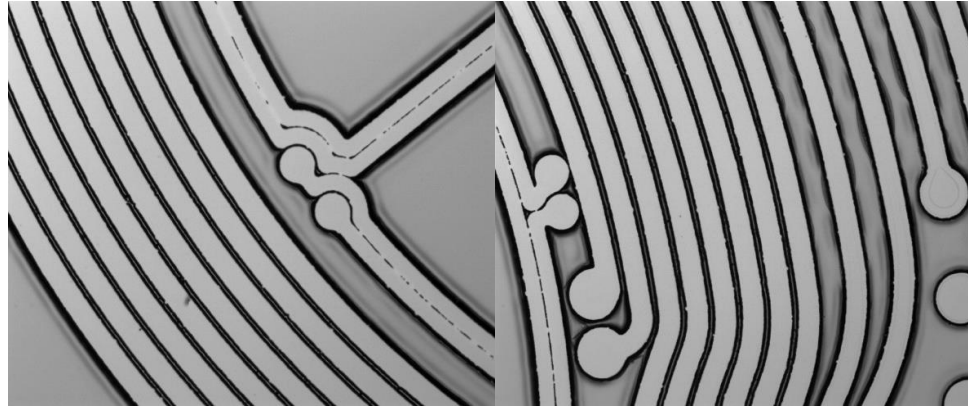


**Figure 3-13 Karl Suss MA6 Mask Aligner in Western Nanofab**

Photomask was plate with pattern that allowed light to go through and create pattern in photolithography technology was indispensable in this step. Our photomask was designed on AutoCAD software and manufactured by CAD/Art Service Inc. For the cost consideration, during device developing we ordered plastic mask instead of chrome mask.

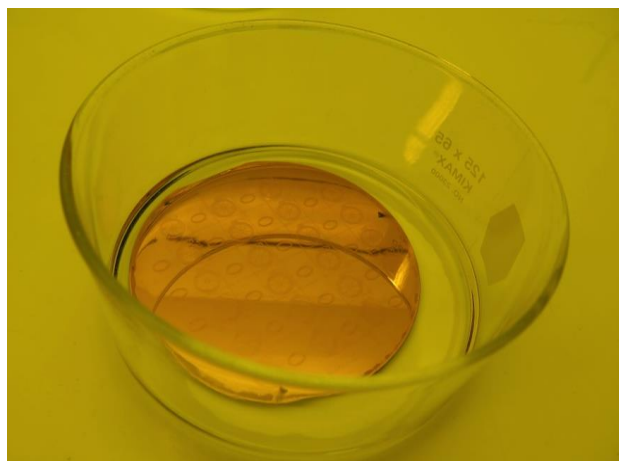
MA6 Mask Aligner by Karl Suss was used to make alignment between wafer and photomask as well as providing UV light and creating the desired pattern. The MA6 mask aligner used a proximity expose type system required direct contact between photoresist and mask. The mercury lamp on top generated parallel UV light in desired wavelength, this UV light passed through the mask and reached the photoresist.

Theoretically, the exposure dose was around  $2100\text{mJ}/\text{cm}^2$  to create the  $17\mu\text{m}$  thick pattern. The exposure time can be calculated by overall dose/light intensity. The MA6 mercury light provided  $\text{mJ}/\text{cm}^2$  and  $\text{mJ}/\text{cm}^2$  two different channel. With  $12\text{mJ}/\text{cm}^2$  channel, the exposure time was 177 seconds. However, the primary testing result showed with the calculated time, the photoresist was largely over exposed as shown in **Figure 3-14**. In our design, both the channel and the gap distance were  $50\mu\text{m}$ . The over exposure made most of the gaps became very thin, and the sequent steps cannot be done with this poor condition of photoresist microfold. There was a lot of different reasons affect the exposure, such as the humidity and temperature of the circumstance, the condition of the mercury bulb. So it was necessary to customize the parameter according to the samples situation. After different tests, the best exposure time was around 150s to 156s.

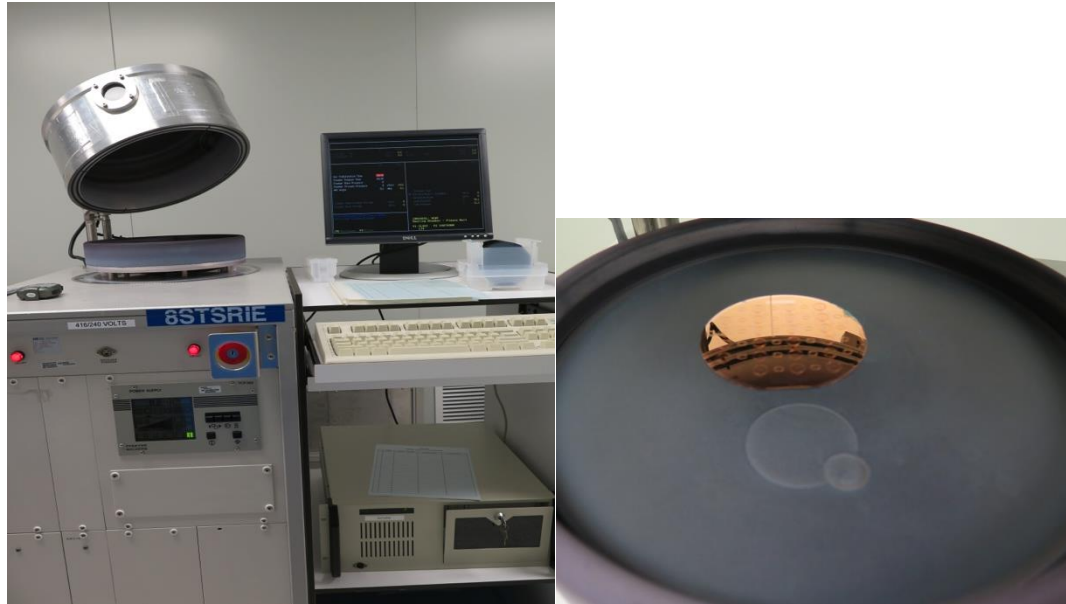


**Figure 3-14 Over exposure on the AZ9260 photoresist layer**

After exposure, the wafer was put into AZ400K developer. With agitating thoroughly, it took around 10mins to finish the developing process. **Figure 3-15** shows the wafer with AZ9260 photoresist in AZ400K developer, the pattern can be clearly seen on the wafer. In this step, the time also varies from 4min developing time on datasheet due to a lot of different reasons as above. Whether the developing process finished or not can be determined under the microscope. Then the wafer was washed by DI water and blow dry by compressed air.

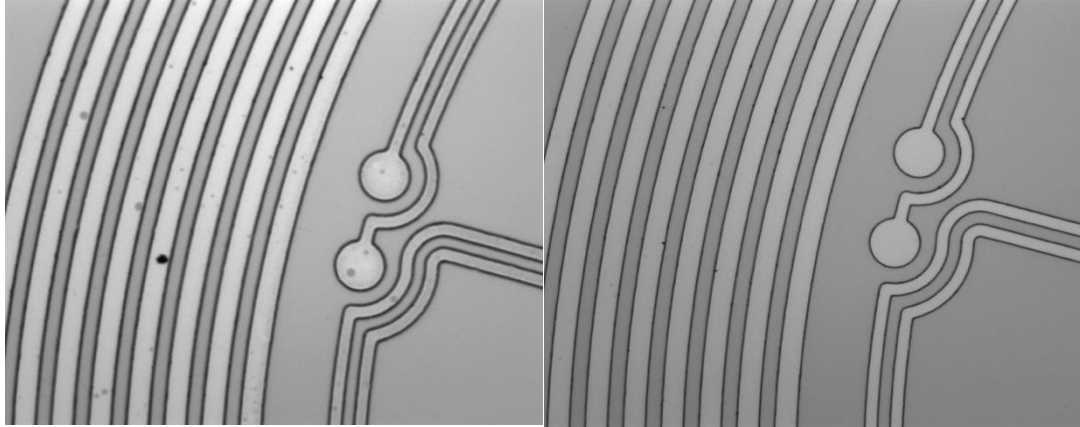


**Figure 3-15 Picture of AZ9260 coated wafer in its post photolithography developing process**



**Figure 3-16 STS oxygen plasma RIE in Western Nanofab**

Since the copper coil can only be electroplated if there is no residual photoresist covered on the pattern. The copper coil may be deposited if the photoresist is only partially removed, however, poor adhesion between copper coil and substrate will not be able to stand the other process. In this case, the wafer was cleaned again by STS oxygen plasma RIE (**Figure 3-16**) for 2mins treatment with 1.7 standard cubic centimeters per minute CF<sub>4</sub> flow. After RIE, the micromold was successfully patterned. From the microscope inspection, the process removed all the residuals and solvents that stuck in the micromold. The thickness of photoresist film was 17 $\mu$ m measured by profiler meter.



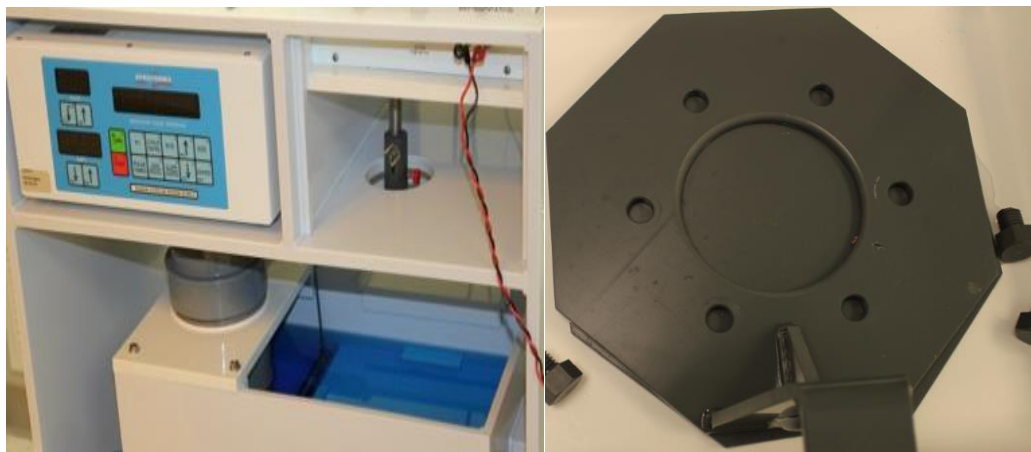
**Figure 3-17 Comparison of wafers before and after Oxygen plasma RIE cleaning**

### **Electroplating process**

Prior to deposition, the electroplating bath solution was prepared. The sulfuric, copper sulphate pentahydrate, chloride, and additives such as brighter and carrier were the main ingredients. The copper sulphate brought sufficient copper ions in the solution. The sulfuric acid was added to increase the conductivity of the solution and inhibit forming cuprous and cupric crystals. The Hydrochloric here was to prevent rough nodular plate. The additives like carrier and brightener were used to increase the grain structure and other copper features. The concentration of each ingredient had to be properly determined. For example, the less concentration of copper sulphate pentahydrate led to high resistivity in the solution and reduced the polarization between cathode and anode. Insufficient amount of sulfuric acid might lead to nodular growth. In this process the formula of the bath solution was: 50g  $H_2SO_4$ , 225g  $H_2SO_4$ , 10ml Brightener, 6ml Carrier, 50ppm HCl mix with every liter of water.



The IKO Classic Electroplating System in Western Nanofab (**Figure 3-18**) was used for conducting this process. The system consisted of bath, programmable rectifier, wafer holder, reciprocating inert cathode, and filtration system.



**Figure 3-18 Photograph of IKO Classic Electroplating System in Western Nanofab**

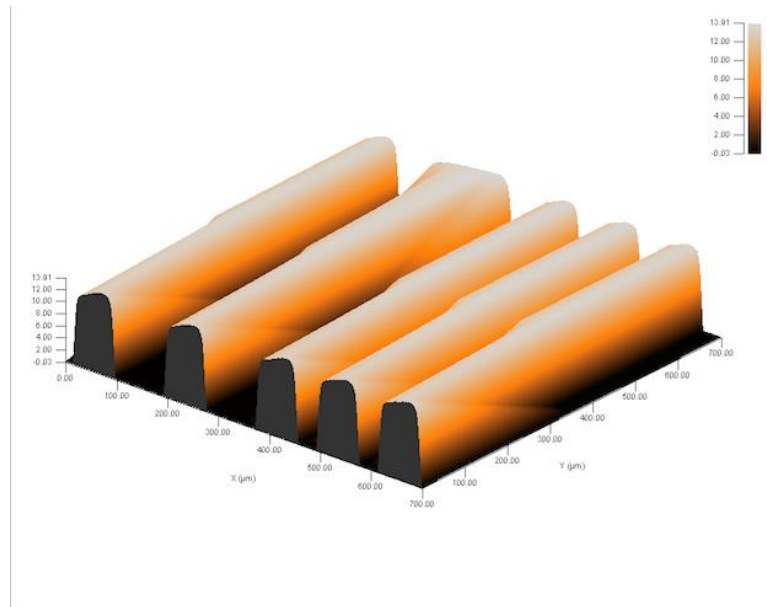
To get start, turned on the kit and keep filtration system working to mix the solution. The wafer was stabilized on the wafer holder with screws and immerse completely into bath solution. The process was started after connecting the cathode and anode to the rectifier and turning on the power supply. At the meantime, reciprocator on the cathode was turned on to agitate solution around wafer.

Our experiments showed, the reciprocator could increase the bulk quality as well as deposition quality. However, the side effect of reciprocator was if the wafer is not well cleaned in the former steps the low adhesion between seeding layer and deposited copper would result in coil peer off. So the handing of each steps needed to be carefully done and that was also the reason for RIE cleaning.

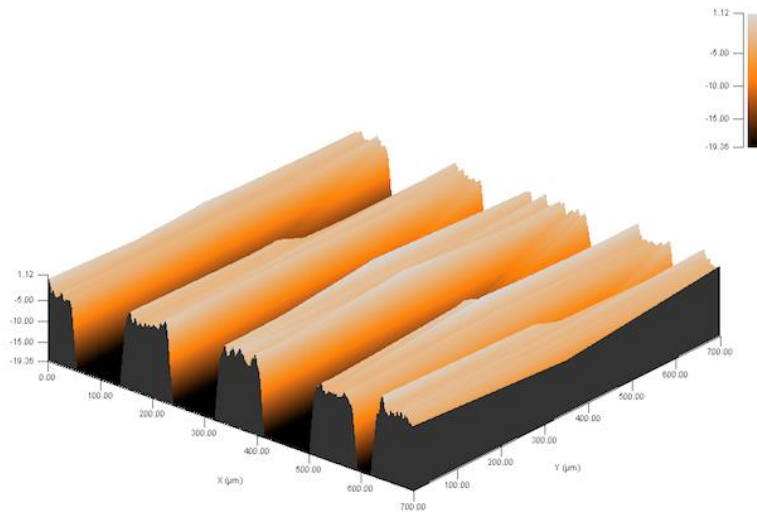
The main advantage of electroplating process among the other deposition processes is the fast deposition rate. A balance between deposition time and copper quality was always sought in our research. Since when the current was increased, the opportunity of growing defects was increased as well. For better control of the plating rate, the rectifier was regulated through current instead of voltage. As copper growth, the changing solution concentration over time resulted in the changes of voltage between cathode and anode. As we know, the exposed seeding layer size was  $3\text{cm}^2$ , and the recommend current density was around 10 to  $50\text{mA}/\text{cm}^2$ . So the current setting on the power source varied from 30mA to 150mA were tried out as below:

**Table 3-1 Different recipes for Cu electroplating**

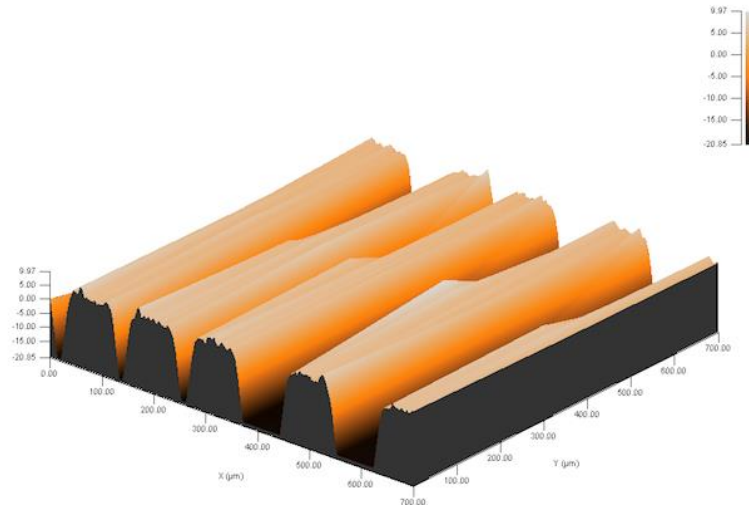
Deposition process	Current	Current density	Brightener added	Time	Thickness of the coil
1	60mA	$20\text{mA}/\text{cm}^2$	30ml	3 hours	$13\mu\text{m}$
2	120mA	$40\text{mA}/\text{cm}^2$	40ml	1.5 hours	$18\mu\text{m}$
3	150mA	$50\text{mA}/\text{cm}^2$	50ml	2 hours	$25\mu\text{m}$



(a)



(b)



(c)

**Figure 3-19 The profile meter analysis in 3D model: (a) recipe 1; (b) recipe 2; (c) recipe 3**

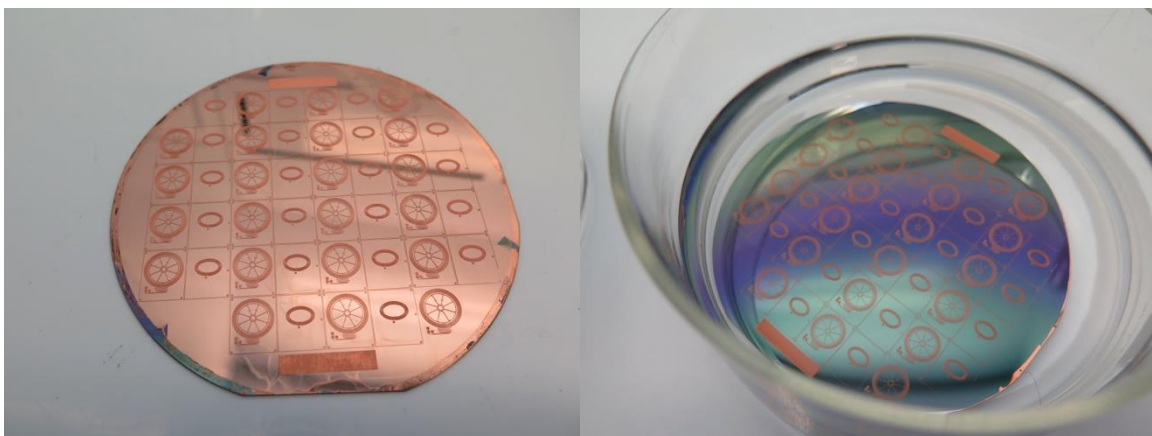
Profile meter analysis showed the coils manufactured in different recipes all had good average thickness. However, the copper deposited under low current had better uniformity. Consider the time issue, it was estimated that deposition through recipe 1 would take at least 4 hours to get at least  $17\mu\text{m}$  thickness, and the other processes could achieve the same result by using only half of the time amount. Although the thickness of the photoresist mold was only  $17\mu\text{m}$ , experiment showed that the coil could actually grow till  $25\mu\text{m}$  without having any interconnection. From **Figure 3-19 (c)**, it was clear to see the coil turns still separated from each other. The relatively rough surface was the only down side. However, this could be trade off by the benefit of having thicker coils. Since the inductance only related to the shape and turns of the coil, and less resistance

came with the thicker coil. Therefore, the overall Q factor was improved by having thicker coils and the recipe 3 was the first choose.

### **Photoresist and seeding layer removal**

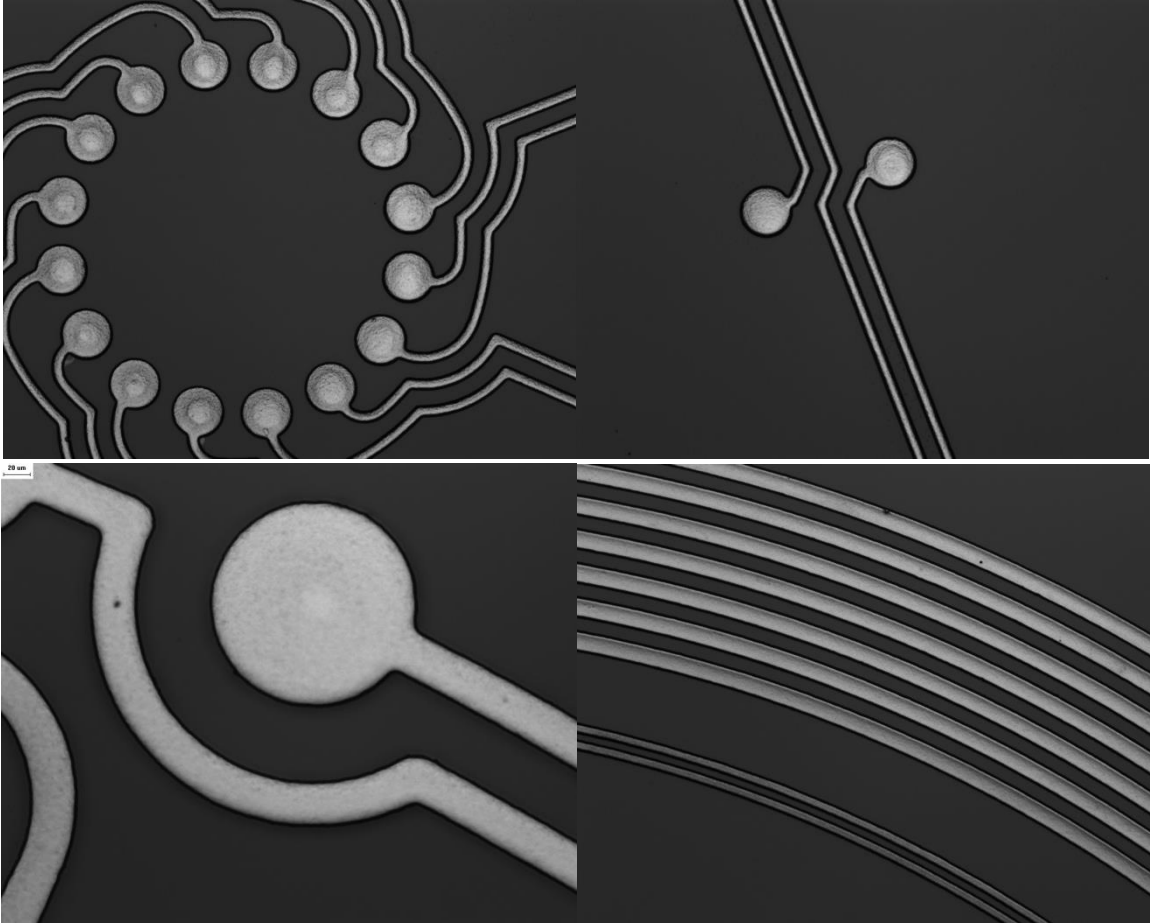
These two steps were the last steps of the first coil layer fabrication process. Both the photoresist and the seeding layer had to be striped completely to create the functional coil circuit. The coil was grown on the exposed seeding layer on the substrate, so they were all connected with each other due to the Cu/Ti seeding layer. As we know, the seeding layer was around 300nm, compared with 25 $\mu$ m thickness coil, it was very thin. Thus, wet etching method was introduced for this process. Prior to wet etching, Actone was used as photoresist stripper.

In the photoresist removal step, the wafer was firstly immersed into Actone with agitation for at least 90 seconds. Then the wafer was rinsed thoroughly by Isopropyl alcohol and deionized water. Lastly, blew dry carefully and inspected if any residual photoresist on the wafer. Repeated the process until the clean wafer was obtained.



**Figure 3-20 Illustration of wafer before and during Cu etching process**

APS-100 copper etchant and Titanium etchant TFTN were used for the wet etch process. The solutions were diluted to allow longer handling time. To start with, the wafer was put into diluted APS solution with gentle agitation till eyes cannot observe the copper layer anymore. **Figure 3-20** showed the wafer before and during its etching process. The wafer was rinsed by DI water and blew dry carefully. Then the further inspection was done under microscope to make sure there were no residual copper remains in the coils gaps, which might cause short circuit. Repeated this process until the coils were separated. After that, the Ti etching process was performed in ceramics container with rubber gloves. Since TFTN contains HF, the handling was strict with safety instruction. The thickness of the Ti was only around 50nm-100nm. Unlike the copper, the thin Ti layer was almost the same color as Silicon oxide was very difficult to observe even under microscope. So the inspection method that used on copper layer etching might not apply to Ti. However, there was a good way to distinguish if the process was already finished. During sputtering process, the wafers were stabilized on the special holder. Some parts of the wafer got covered by the holder couldn't be deposited with Ti/Cu seeding layer, and it was obvious even from eyes to observe the color difference on the edges. During the Ti etching process, with the etching ongoing, the color difference on the edges will disappear. This indirectly indicated the Ti layer was etched off.

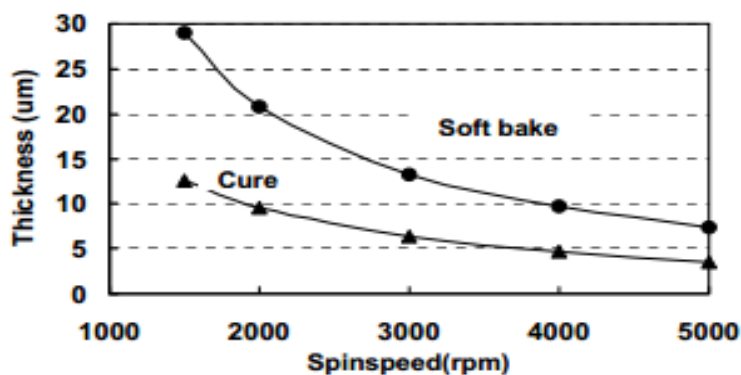


**Figure 3-21** Microscope images of the details of the first coil layer

### 3.3.2 Insulation film fabrication

Polyimide with its excellent characteristics is widely used in microelectronics and MEMS system devices as insulation film. HD4100, the negative tone polyimide photoresist was purchased from Dupont.

### Pre-photolithography treatment



**Figure 3-22 The spinning speed vs film thickness relation of HD4100 photoresist  
(Adapted from [58])**

According to the HD4100 series bulletin [58], 25 $\mu$ m thickness HD4100 photoresist could be spun at the spinning speed of 1700rpm. After placing the wafer on the holder of the spinner, turn on the vacuum for stabilization. Try run the spinner to make sure the wafer is placed at the center of the holder. Squeeze HD4100 on the wafer can cover all the patterned area. Set the spread ramp to 500 rpm with 100rpm/sec acceleration for 8 seconds, this step allows the photoresist fully cover the wafer. In the spin cycle, set the spin speed at 1700rpm with 500 rpm/s acceleration for another 50 seconds. Similar with before, the wafer was then transferred onto a hot plate for the soft-bake process. The wafer was initially heated up from the room temperature to 90°C, and stayed at 90°C for 90 seconds. Then increased the temperature to 110°C and baked the wafer for another 90 seconds.

### Photolithography process for vias and pads

The polyimide here function as insulation film between two coil layers. The exposure was needed for creating vias and pads that allowed the connection between two layers.

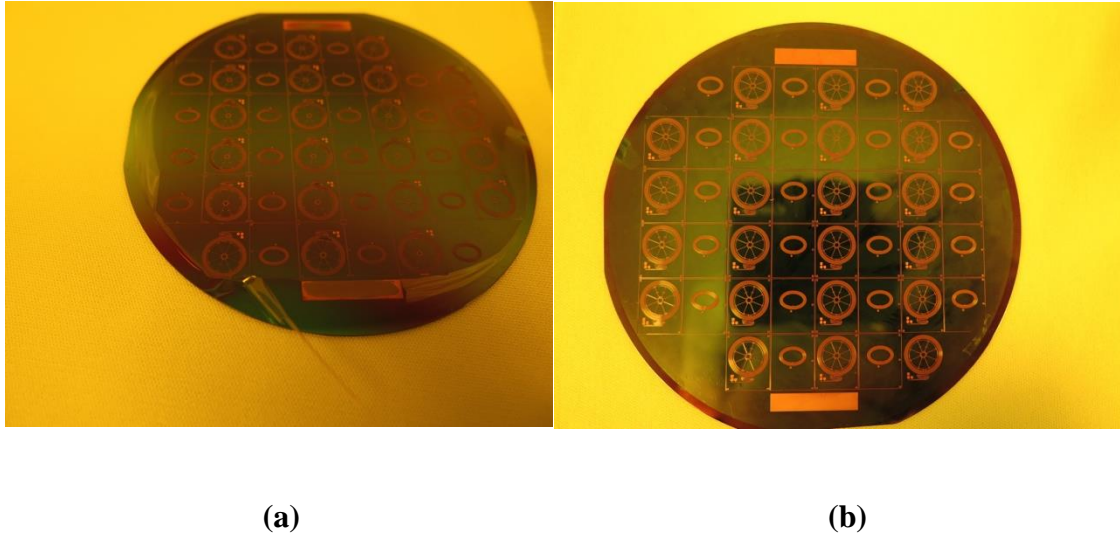


Different from the previous photolithography, the pattern alignment was required in this step. After loading the wafer, the alignment was conducted through microscope on the MA6. In the previous steps, the first coil layer was successfully patterned as well as the alignment marks on each corner of the devices. Those features would be used as references. Adjusted the wafer position carefully to allow the marks on the mask fully cover the references patterns. Checked different reference marks in different locations, if all of them were fully covered by the mask the alignment was done. The wafer was exposed under  $6\text{mJ}/\text{cm}^2$  UV light for 40 second to reach desired 240mJ dose.

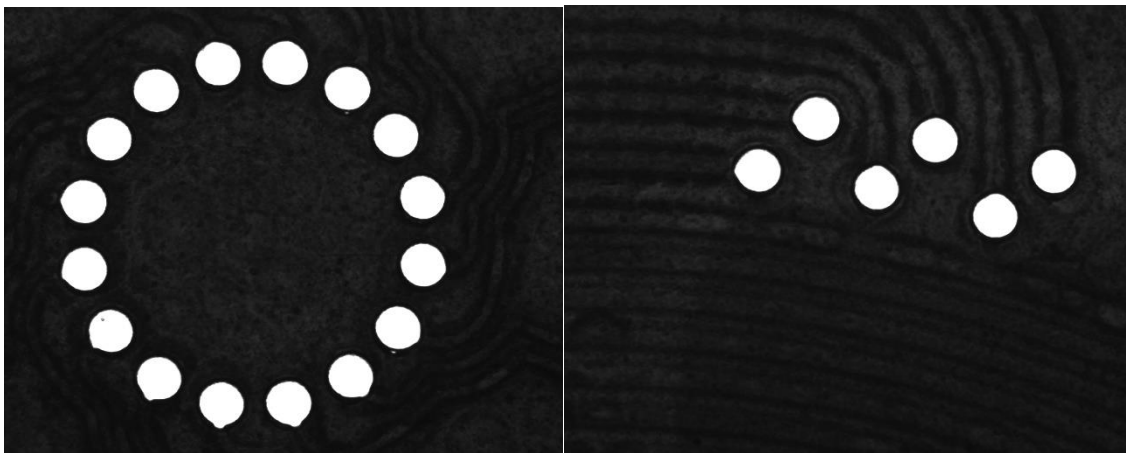
### **Post-photolithography treatment**

After photolithography process, the wafers should be held at least 5 mins before move to post exposure bake process, which could significantly lower the exposure energy. The post exposure bake condition for this experiment was  $110^\circ\text{C}$  for 90 seconds. Cold down to the room temperature and immersed into PA-401D developer with agitation for another 10mins. Same as before, microscope inspection was necessary to judge if the via channels were open already. The shining copper underneath could be clearly seen if the residual were removed. Then rinsed the wafer in PA-400R and blew dry.

Lastly, the final cure process was performed on hot plate at  $220^\circ\text{C}$  for 30min. The objectives of final cure were: removed the residual solvents and photosensitive materials; imidized the HD4100 photoresist into polyimide; finished the adhesion process. In a lot of situations, if the temperature directly ramped up to over  $200^\circ\text{C}$  the polyimide layer would face the risk of cracking. The typical cracks showed in **Figure 3-23 (a)**. For better handling, the wafer was heated from the room temperature to  $180^\circ\text{C}$  first and held for 15min. Then increased the temperature to  $220^\circ\text{C}$ .



**Figure 3-23 Image of (a) cracked insulation film sample and (b) a well-developed sample**



**Figure 3-24 Microscope image of the HD4100 photoresist vias**

### 3.3.3 Upper coil layer fabrication

The parameter of the subsequent coil is same as the first layer coil. They are connected to each other through the vias on the insulation film. However, the substrate is different as

the first seeding layer was fabricated on 2 $\mu$ m thickness Silicon oxide, and the subsequent seeding layer would be built on the 30 $\mu$ m thickness insulation film-the polyimide film we just made. Since the fabrication process was almost the same as the first layer as we introduced in detail in previous. The procedures are summarized as below:

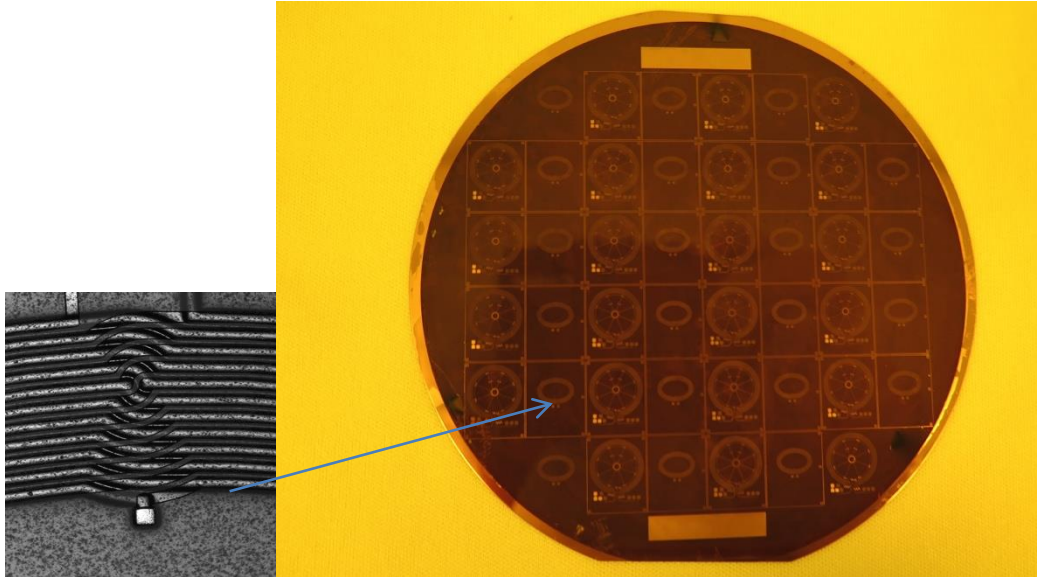
1. Wafer pretreatment: The oxygen plasma RIE was used again to clean up the any potential remains. According to the HD4100 product bulletin, even the uncured polyimide shows good dry etch resistance. The etching rate was around 0.1 $\mu$ m/min, so a 5mins process was designed for the dry etch. Also, at the same time of etching away the residuals, the etched polyimide resulted in high roughness surface. And the roughness could improve the adhesion between polyimide and the next seeding layer.

2. Sputtering: Same as before, the Ti/Cu seeding layer was deposited on the wafer surface. For the Ti sputtering, with the same power and Nitrogen flow, increased the time from 20mins to 30mins to create a thicker Ti thin film. This could increase the adhesion bond between insulating film and the copper layer, as well as compensating the surface roughness of the polyimide. The Cu was also deposited right away after Ti layer with the same condition applied as previous.

The mask had different pattern with the first layer, other than that the following procedures were totally same as previously discussed in this chapter are summarized as below:

3. Spin coating: The AZ9260 photoresist was spun on the wafer to create a 17 $\mu$ m thickness layer.

4. Photolithography: After the alignment mark on the mask and the reference mark on the wafer were completely aligned. The wafer was exposed under  $12\text{mJ}/\text{cm}^2$  UV mercury light for 156 seconds.



**Figure 3-25 Image of the upper patterned micromold under microscope**

5. Developing: The wafer was immersed into AZ400K developer with proper agitation for 10mins to create micromold pattern for the electroplating deposition. The developing process should continue till the seeding layer was exposed to the air in the patterned area.

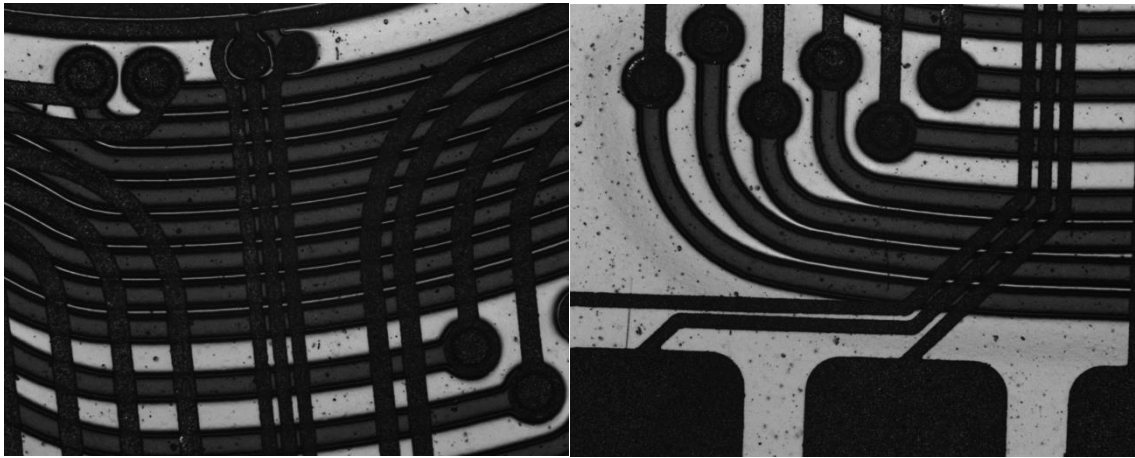
6. Oxygen plasma RIE: This process was to remove the possible residual photoresist in the micromold, creating good growth condition for the next step.

7. Electroplating process:  $25\mu\text{m}$  thickness patterned copper coil were fabricated again.

8. Strip photoresist: Used Acetone to stripes off the remaining AZ9260 photoresist, then the wafer was rinsed by IPA. It was important to remove all the photoresist on the wafer. Otherwise, the residuals might block the later etching process.

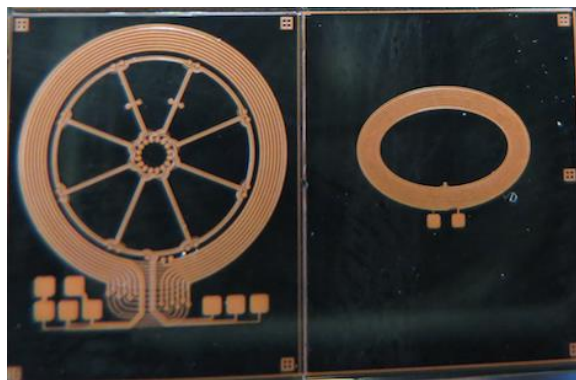
9. Seeding layer etching: The Ti/Cu seeding layer was removed by immersing into corresponding Cu and Ti etchant.

The fabrication process was finished. The images of the devices under microscope were shown as below, Bi-layer coil structure could be observed in the pictures with good alignment through round vias.



**Figure 3-26 Microscope images of bi-layers coil structure**

On each 4-inch wafer, twenty pairs of the devices can be fabricated. The devices will be diced and the electrical property of the devices will be tested in the next chapter.



**Figure 3-27 Image of one pair of device on the wafer**

### 3.4 Conclusion

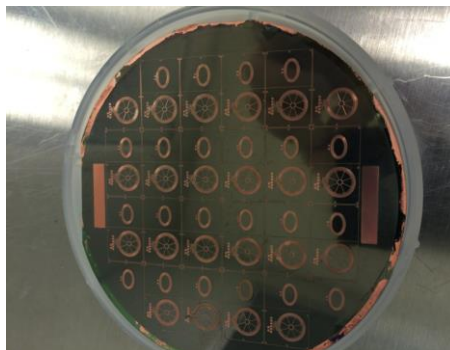
In this chapter, the manufacture process of bi-layers copper coil pairs were introduced and the prototypes were successfully fabricated. The Ti/Cu seeding layer was deposited by sputtering on the 2 $\mu$ m SiO<sub>2</sub> silicon wafer, the coils was fabricated through electroplating process within the AZ9260 microfold which was patterned by photolithography process. The first layer was successfully made after the photoresist and seeding layer are striped off through a series of chemical treatments. Patterned Polyimide was spun coated on top of the first layer to act as insulation layer. The upper coil layer was fabricated by the same way as the first layer. For each wafer, 20 pairs of devices could be manufactured at the same time.

## Chapter 4

### 4 Device integration and testing

#### 4.1 Introduction

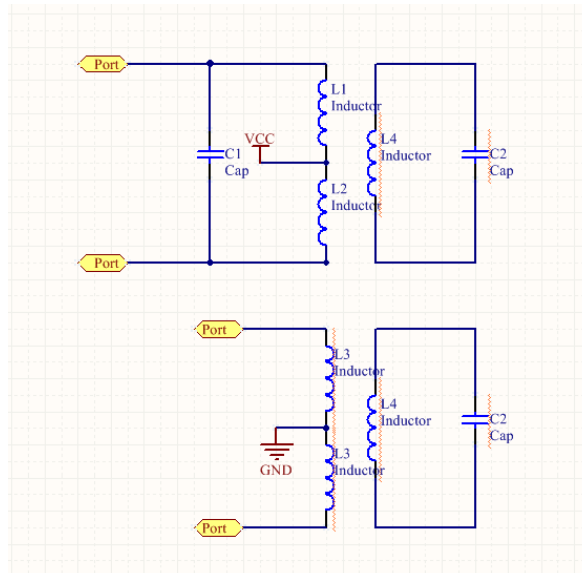
Upon finishing the fabrication process, the whole wafer is displayed as shown in **Figure 4-1**. In this chapter, the electrical properties of the coils, such as resistance and inductance will be measured. The system integration process is introduced, and the final testing on the device level will be done and compared with the simulation. During the fabrication process, the microscope and profile meter are used to make sure the coils are grown following the designated parameter. However, the electrical properties are still unknown and need to be further reviewed for the system integration. The preliminary tests are performed on LCR meter. The purpose is to determine and mark good samples from wafer before dicing. After the dicing process, the more detailed test is conducted on impedance analyzer at MHz level. The results will be compared with the simulation results on HFSS in chapter 2. Lastly, good samples will be integrated to corresponding electronic components and measured by oscilloscope under working condition.



**Figure 4-1 Photograph of a fabricated wafer sample**

## 4.2 Preliminary test by LCR meter on probe station

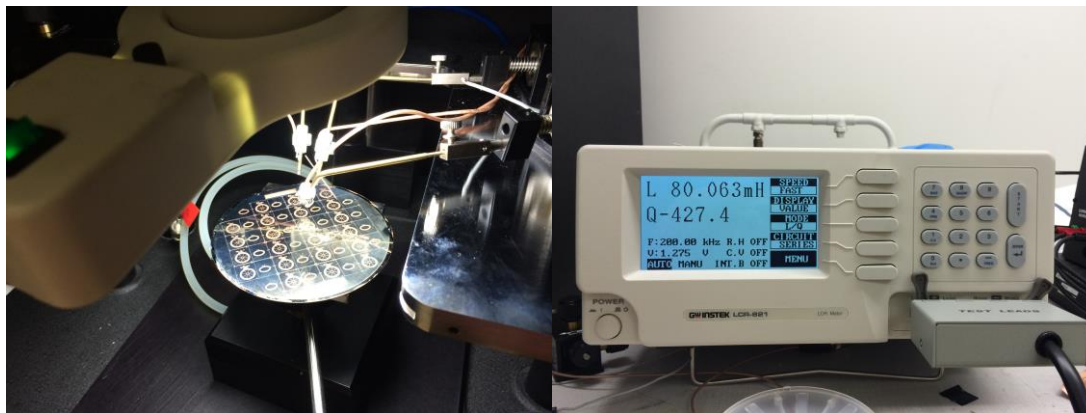
The purpose of the preliminary test was to quickly determine the good samples from the wafer. The preliminary test consisted two steps. In the first step, the resistance and inductance of excitation coil, coupler, and reception coil were measured individually. In the second step, the resistance and inductance of L1 to L4, as shown in **Figure 4-2** were measured to make sure the uniformity of two different layers. L1 and L2 represent two inductors on the different two layers.



**Figure 4-2 Circuit configuration of excitation coil, coupler and reception coil**

Due to the small size pads on the coil, a probe station and LCR meter were needed to conduct this measurement. The experiment was set up as shown in Figure 4-3, the probe station was connected to the LCR meter, GWINSTEK LCR-821 to measure the resistance and inductance.





**Figure 4-3 Probe station and GWINSTEK LCR-821 for the measurement**

The inductance of the coils is considered around  $\mu\text{H}$  level, which was very small compared to the cables' own inductance. So, before conducting the test, the open circuit compensation test and short circuit compensation test had to be utilized. Then the needles of the probe station were connected to the corresponding pads. As mentioned, the designated device working frequency was 4MHz. In our set up the LCR meter could only provide 200KHz frequency as maximum. The result could be compared with the simulation under 200KHz frequency to verify if the whole wafer was successfully developed.

L1 and L2 represented the first and the second layer of the excitation coil, and they were integrated through series connection. Both L1 and L2 were fabricated under the same procedure and the measurement result of L1 and L2 should be the same. The overall resistance between L1 and L2 was the sum of their individual resistance. The overall inductance of L1+L2 was the sum of their self-inductance plus two mutual inductance. L4 represents the coupler coil inductor.

**Table 4-1 Preliminary test result of the device**

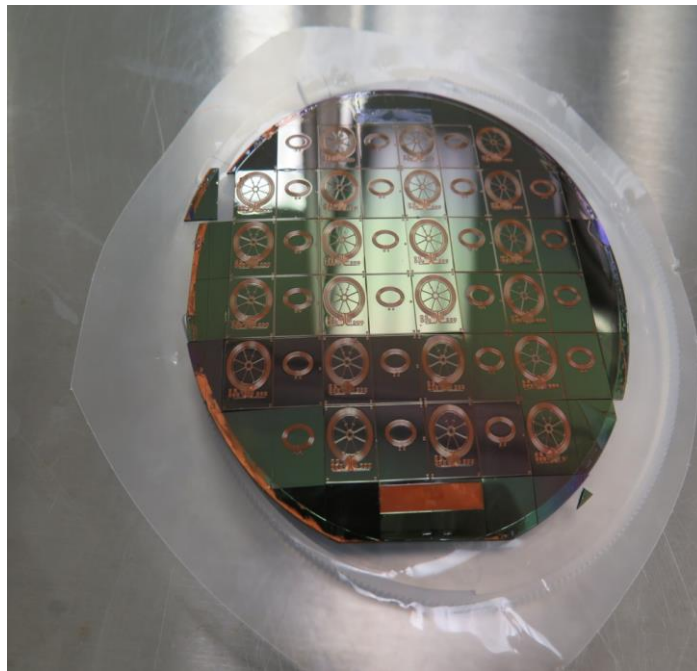
Excitation coil						Coupler coil	
L1		L2		L1+L2		L4	
Inductance	Resistance	Inductance	Resistance	Inductance	Resistance	Inductance	Resistance
0.80 $\mu$ H	3.90 $\Omega$	0.80 $\mu$ H	3.90 $\Omega$	3.20 $\mu$ H	7.80 $\Omega$	3.50 $\mu$ H	8.50 $\Omega$

Compared with the simulation result, the preliminary test result showed the coils are fabricated successfully. In our new wafers samples, more 90% of the devices on the wafer matched the simulation result. Therefore, with the process we developed in chapter 3, the product has very good quality. The matched result indicates there were no unwanted interconnection and crosslink in the developed wafers. The mass manufacture of this coil in future with same process we developed is possible.

Also the test result can be used to problem shooting for the micofabrication process. Here are few typically examples. If the resistance of devices on the wafer is different from each other but still in reasonable level, it may be caused by the poor uniformity of the micromold during spinning. This is because copper coil with different thickness can be grown through this micromold, which result in the resistance difference among individuals.

### 4.3 System integration and final testing

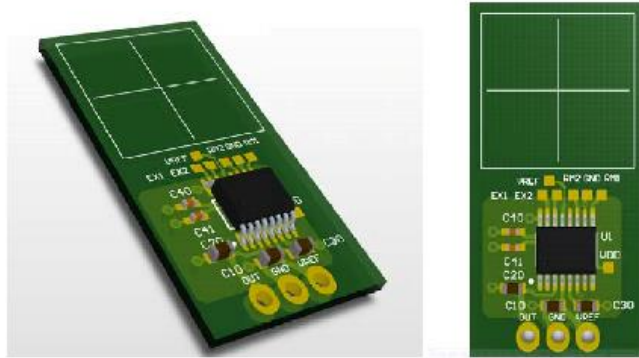
The good samples were marked and diced for the further examination. K & S 780 dicing saw in Western Nanofab was used for our cutting process. Upon cutting, the sample needed to be covered by a protecting layer to prevent the device from being contaminated through cutting. The particles generated during cutting including Si and Cu. If the Cu particles landed on the coil, the short circuit might happen which would affect the performance and reliability of the devices. AZ9260 photoresist was spun on the wafer as protecting layer. After dicing, good samples were collected and placed gently in sample case from the next step.



**Figure 4-4 Diced wafer sample**

In order to match with the miniaturized sensor coils, a new PCB board was designed and provided by KSR. The coils, resistors, capacitors and ASIC chips were integrated on the

PCB to function as device. The coils samples and magnetic sheet are attached to the square area.



**Figure 4-5 Miniaturized PCB Layout**



**Figure 4-6 Photograph of Leica wire bonding machine in McMaster University**

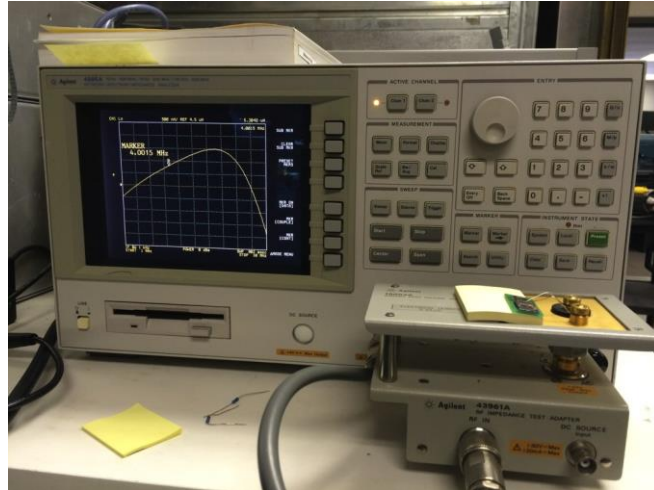
To connect the coil with ASIC through PCB, a wire bonding process was conducted in McMaster University. Wire bonding process is considered as the most effective interconnect technology, is widely used to making interconnections in IC during packaging. It also can be used to integrate IC to PCB. In this process, gold to gold bond and gold to copper bond were practiced. Two materials were bonded to each other through ultrasonic energy, force and heat applied. The common method was to wedge bond to the PCB and ball bond to the substrate. 35 $\mu$ m gold wire was used as connection material with its extraordinary electrical property. The sample was firstly placed and stabilized on the perform platform. The gold wire passed through the capillary. A high voltage charge was applied to the tip of the wire to form a gold ball. Then under microscope the capillary was firstly moved on top of copper pad. After alignment, the capillary was pushed down and hit on the pad on chip with ultrasonic energy. The weld between the wire ball and the pad was created. For the next step, the wire was passed out through the capillary and moved over to the location on PCB side where the connection was needed. Unlike the first bond the ball cannot be made this time, so the shape of the weld was very different from the first ball bond, called wedge bond. In the bonding process, the force, time, and ultrasonic energy level can be adjusted to match with different bonding contact situation. Due to the transportation issue, those bonds were enhanced by using sliver paste.

**Table 4-2 Bonding parameter**

	Search	Force	Time	Ultrasonic power
Chip bond	4	1	5	2
PCB bond	4	7	5	4

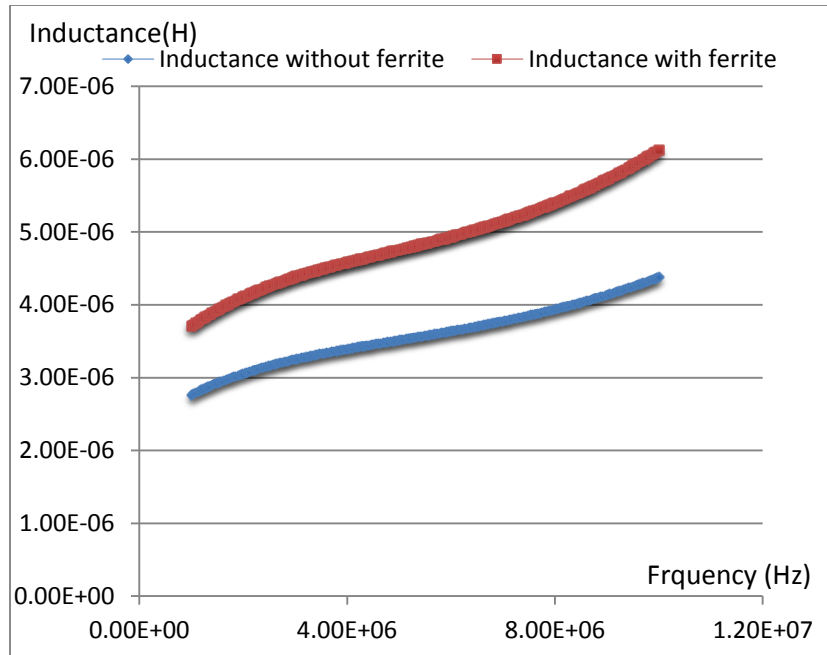
**Figure 4-7 Microscope image of bonded device**

Before integrating with the other electronics components on PCB, high frequency test was conducted in the research center of KSR International Co. The Agilent 4294A, with its wide working frequency range from 40Hz to 11MHz, was used for the measurement. The purpose of this test was to compare the inductance and resistance data of the coil measured under 4MHz with simulation. The result was used to pick corresponding capacitors for the coils to form LC oscillator.

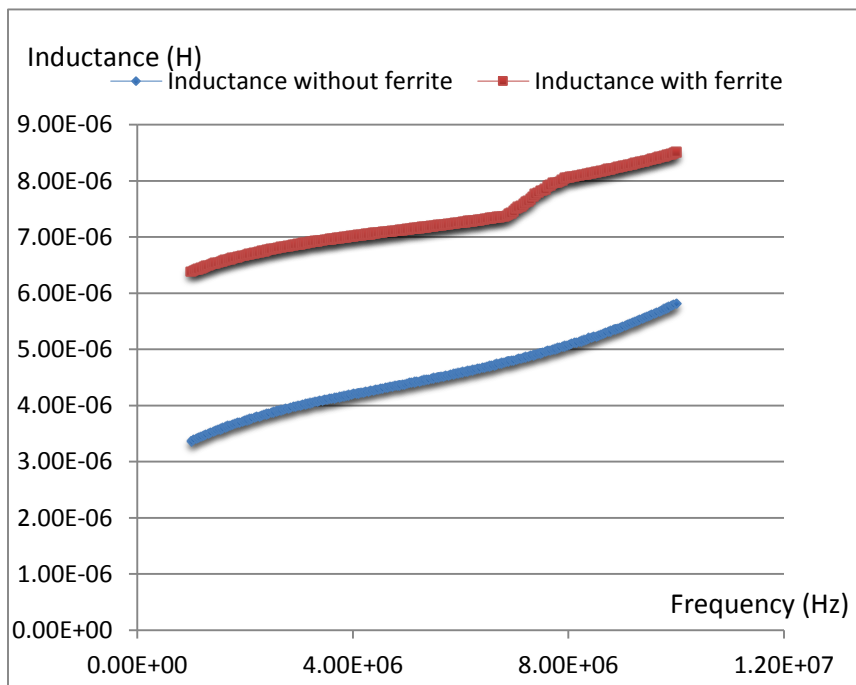


**Figure 4-8 Agilent 4294A impedance analyzer in KSR**

To begin with, the Agilent 4294A system needs to be calibrated upon testing. A standard resistor was used in the open compensation and short compensation. Experiment was set up as shown in **Figure 4-7**. The device was tested by the analyzer from 1MHz to 6MHz. Comparing the inductance data with the simulation in chapter 2, it is easy to find out the result matches well with simulation result. The bi-layer coil inductor shows good enhancement when integrated with ferrite sheet. The inductance gains under 4MHz are 35% and 66% respectively on excitation coil and coupler coil. And the enhancement is valid in all measured frequency range.



**Figure 4-9 Inductance of excitation coil under different frequency**



**Figure 4-10 Inductance of reception coil under different frequency**



On the device, each excitation coils and couplers are connected with capacitors in series working as LC oscillator. With power supply, the ASIC drives the excitation LC loop to oscillate at designated frequency. When the coupler is put at proper distance, usually 1mm from excitation coil. The LC loop on coupler will resonance at the same frequency with excitation coil. The alternating resonance magnetic field generated by coupler will induce voltage in sensing coil. When the coupler changes its position, the amount of magnetic flux goes through sensing coil changes at the meantime. Therefore, the induced voltage changes periodically when the coupler rotates.

To form the LC oscillator at the designated frequency. The capacitance of the capacitor can be calculated by **Equation 4-1**. As we know the system frequency is under 4MHz, and the value of the corresponding inductance of excitation coil and coupler coil under the same frequency. The value of the capacitors can be calculated as 350pf and 300pf respectively.

**Equation 4-1** 
$$f = \frac{\omega}{2\pi} = \frac{1}{2\pi\sqrt{LC}}$$

With the calculated capacitance, the ASIC chip and capacitors were soldered on the PCB. Surface mount technology method was used on this step. The solder paste, a mixture of solvent and solder particles, was applied to all the pads on PCB. Then the chip and capacitors were placed on the pads and exposed under 400 degree air gas flow. After cooling down, the device was successfully built. On the coupler chip, the capacitor was glued on the pads under microscope by using sliver paste.



**Figure 4-11 Image of the device**

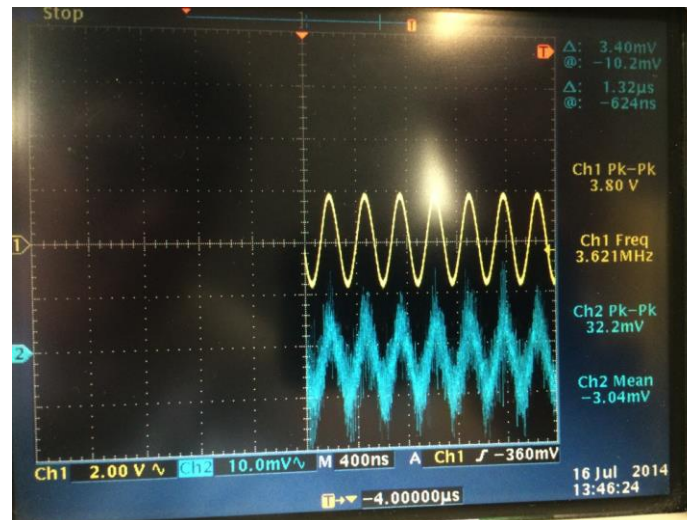
1	KD	DGDC	16	
2	GDC	EX1	15	EX1
3	PPS	EX2	14	EX2
4	VHV	MOSI	13	MOSI
5	VDD	MISO	12	
6	GD	RM2	11	RM2
7	Cosine	GDC_CL	10	
8	Sine	RM1	9	RM1

**Figure 4-12 Pin definition of KSR-I809**

In the device, VHV pin connects with power source. The excitation coil connects to EX1 and EX2 pin; receiver coil connects to RM1 Pin and RM2 Pin. Output of excitation coils and receiver coils are measured through channel 1 and 2 respectively on oscilloscope.

When the power is on, in channel 1 the Sin waveform can be seen on oscilloscope. This

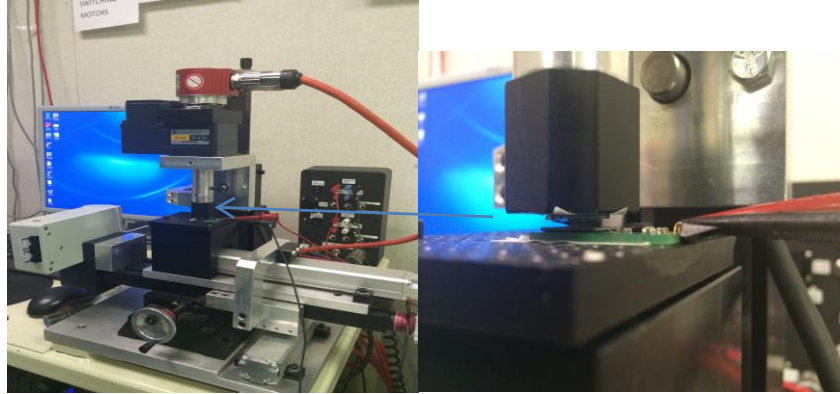
means the excitation chip is driven by the ASIC to oscillate. The resonance frequency of the excitation coil is 3.62MHz with 3.8V peak to peak output voltage. When the excitation coil and coupler coil approach to each other, the output voltage of the receiver coil is around 30mV. This means, the LC loop of coupler coil is induced by the excitation coil. And the signal is successfully transmitted back and picked up by receiver coil (sensing coil). The signal strength is as the same level as current PCB product. By changing the position, height of the coupler, magnetic flux passes through the receiver coil changes. Therefore, the induced voltage level of the receiver coil changes accordingly. This result shows the coil chip and PCB are successfully integrated with each other.



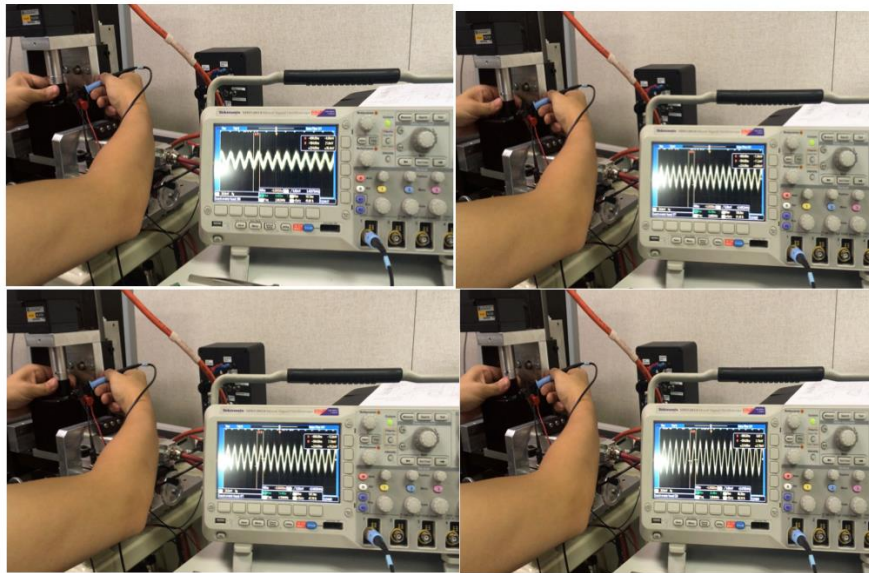
**Figure 4-13 Screenshot of the waveform of the excitation coil and coupler coil**

The output and angular relationship was carried out through XYZ tester (**Figure 4-13**). The excitation coil part was stabilized on the platform. After alignment, the coupler was set on the rotor facing the excitation coil with 1mm distance. With power on, an oscilloscope was connected to the RM1 to track the data. As shown in **Figure 4-14** and

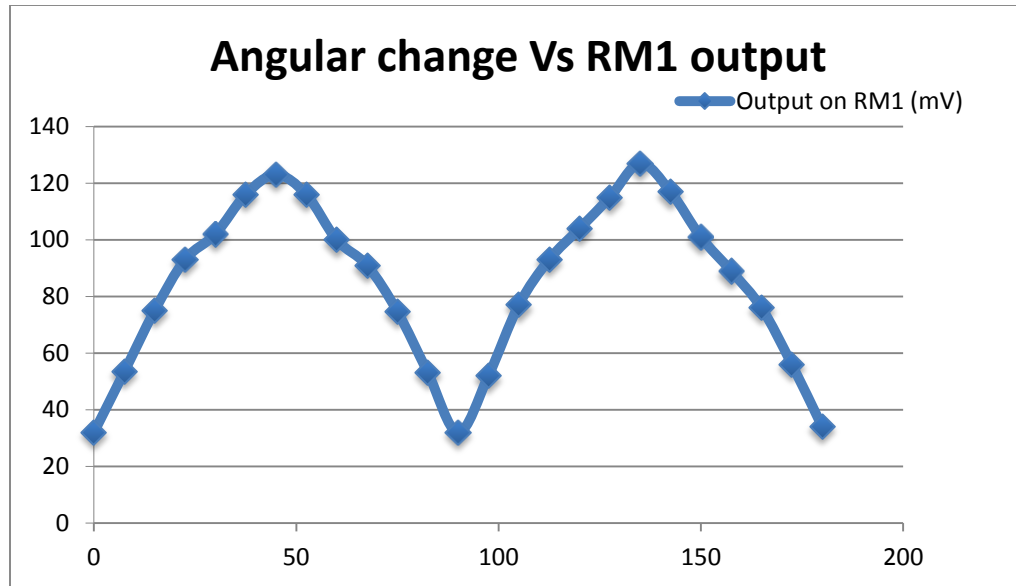
**Figure 4-15**, through rotating the coupler, the output signal on RM1 changed accordingly with angular.



**Figure 4-14 XYZ tester in KSR**



**Figure 4-15 Output on RM1 through rotating the coupler**



**Figure 4-16 Plot of measurement result of angular-output relation**

With calibration, the signal picked up by receiver coil can be further processed by ASIC. After filtering, modulation and demodulation, the Sin waveform from receiver coil (from 30mV to 120mV level) can be transformed and amplified to a 0-5V range DC signal to represent the position changes of the coupler coil. However, the key point of our experiment is to develop the prototype of this MEMS based micro inductive sensor. Since the key point has been achieved by using microfabrication process and verified by several of test methods, the system calibration will be listed as future work.

## 4.4 Conclusion

Upon integration, the wafer samples were tested by LCR meter. The purpose of this preliminary test were two: (1) problem shooting and improve the fabrication process; (2) mark out the good samples for later integration. For instance, if the resistance of devices is different from each other but still in reasonable level, it maybe caused by the poor

uniformity of the micromold during spinning. This is because copper coil with different thickness can be grown through this micromold, which result in the resistance difference among individuals. If the value of the inductance is minus, it maybe because of interconnection issue due to the: (1) unfinished seeding layer etching; (2) poor coverage of the insulation film. The accuracy and efficiency of the procedures developed in chapter 3 were improved through the preliminary test section. Then the good samples were diced and integrated with PCB through wire bonding process. The process included a first gold to copper ball bond and a gold to gold wedge bond. Then the wedge bonds were enhanced by sliver paste to endure transportation vibration. The devices were tested again by impedance analyzer at high frequency. The carried out test results showed that the resistance and inductance of the device matched with the simulation result, which means the coils fabrication process was successfully developed and the contribution of adding ferrite sheet was proved. The devices were integrated with capacitors and ASIC using SMT method. The measurement result of oscillating frequency and pk-to-pk voltage showed: (1) the LC loop of excitation coil can be driven by the ASIC and generate Sin waveform signal; (2) when approached the excitation LC loop and coupler LC loop can resonance; (3) corresponding signal generated in the sensing coil, the signal strength changed when coupler changed its position; (4) The output signal changed accordingly with angular change; (5) all the signals measured matched the simulation. This means the working principle of micro inductive sensor is feasible and mostly importantly the fabrication process is successful.

## Chapter 5

### 5 Conclusion and future works

#### 5.1 Conclusion

In this research, the feasibility of building the next generation inductive sensor by using the state of art MEMS microfabrication process has been investigated. By taking advantages of microfabrication technology, the size of the coils is successfully miniaturized down to 10% compared with the current PCB product. The conclusion of this research is summarized as follows:

Firstly, the design was optimized and simulated based on the design principle in chapter 2. The design principles were purposed as a guideline for the design. The high Q factor was always pursuit while miniaturization. The higher Q factor results in less energy loss during oscillating, and can be achieved by bring high inductance and low resistance to the coil. Moreover, The mechanism of the inductive sensor was studied to help the design. Based on the guideline, several different versions of designs were given. The Q factors of each version were roughly calculated using Burkett model equation. Considering the facts such as performance, easiness to fabrication, dimension, accessible to mass production, the best version was selected for the detail simulation. The simulation was conducted on HFSS and given for comparing with test result.

Secondly, a novel method of fabricating miniaturized micro inductive sensor was successfully developed in chapter 3. At the first half of chapter 3, the prevailing microfabrication technology were introduced including substrate, thin film deposition,

patterning. The common process such as LIGA and lift-off were also discussed with their pros and cons. The LIGA was chosen as the coil fabrication method due to its capability of growing thick coil and excellent compatibility with mass manufacture. As a result, electroplating was selected as the coil deposition method instead of sputtering to match with the process. The fabrication process includes three stages: the first coil layer fabrication; insulation film fabrication and the second layer fabrication. For building the first coil layer, Silicon wafer with 2 $\mu$ m silicon oxide was chosen as substrate. After cleaning, Ti/Cu seeding layer was deposited on the substrate respectively. AZ9260 photoresist was selected and spun on the substrate for later electroplating process due to its good compatibility with Copper electroplating process. The photoresist film then was exposed and developed to form a 17 $\mu$ m thick patterned micromold. The electrochemical deposition was used to deposition Copper in the micromold. The quality and deposition rate can be tuned through adjusting the amount of additives, the intensity of current and applying proper agitation. The photoresist was removed by Actone, and seeding layer was stripped off respectively by Cu and Ti etchant. Although the Cu etchant removes not only the seeding layer, but also the fabricated Cu coils, the etch rate can be controlled by changing the concentration of the solution. To prevent coils from peeling off, a more diluted solution was used with slow etch rate. Patterned Polyimide is spun coated on top of the first layer to act as insulation layer. The upper coil layer is fabricated by the same way as the first layer. For each wafer, 20 pairs of devices can be manufactured at the same time.

Upon integration, the wafer samples were tested by LCR meter. The purpose of this preliminary test were two: (1) problem shooting and improve the fabrication process; (2)



mark out the good samples for later integration. For instance, if the resistance of devices is different from each other but still in reasonable level, it maybe caused by the poor uniformity of the micromold during spinning. This is because copper coil with different thickness can be grown through this micromold, which result in the resistance difference among individuals. The accuracy and efficiency of the procedures developed in chapter 3 were improved through the preliminary test section. Then the good samples were diced and integrated with PCB through wire bonding process. The process included a first gold to copper ball bond and a gold to gold wedge bond. Then the wedge bonds were enhanced by sliver paste to endure transportation vibration. The devices were tested again by impedance analyzer at high frequency. The carried out test results showed that the resistance and inductance of the device matched with the simulation result, which means the coils fabrication process was successfully developed and the contribution of adding ferrite sheet was proved. The devices were integrated with capacitors and ASIC using SMT method. The measurement result of oscillating frequency and pk-to-pk voltage showed: (1) the LC loop of excitation coil can be driven through the ASIC and generate periodical Sin waveform signal; (2) when approached the excitation LC loop and coupler LC loop can resonate; (3) corresponding signal generated in the sensing coil, the signal strength changed when coupler changed its position; (4) The output signal changed accordingly with angular change; (5) all the signals measured matched the simulation. This means the working principle of micro inductive sensor is feasible and mostly importantly the fabrication process is successful.

In conclusion, a reliable procedure of building micro inductive sensor was developed with the consideration of future mass production possibility. The good test results

compared with simulation proved the feasibility of developing and fabricating micro inductive sensor. Through continuously optimization and improvement, the samples diameter was further miniaturized. The unit device pair per wafer was increased from 12 to 20 pairs. At the meantime, the good sample rate was increased from 30% to 90% in the latest version. Precious hands on experiences were gained and abundant data were collected for the future studies.

## 5.2 Future works

Based on this research, following suggestions are made for future studies. In the thesis, the importance of having high Q factor was discussed. The higher Q factor results in less energy loss during oscillating, and it can be increased by either increasing the value of inductance or lower the resistance of the coils. The most effective method of lowering the resistance is to increase the thickness of the copper coil. In our research, 25 $\mu$ m thickness copper coil was built through 17 $\mu$ m thickness micromold. In the experiment the thickness of the copper coil reached its limit due to the risk of forming interconnection between over plated copper. In this regard, a thicker micromold is needed to provide support for deposition. For AZ9260, although the spinning rate under 1000rpm will result in poor uniformity of the surface, micromold with higher thickness may still be obtained by using double spinning method. Also, other photoresists can be considered as well. In our research, the upper coil layer was deposition on the first coil layer covered by insulation film. With the same fabrication process apply, a third coil layer can be added. The overall inductance will increase accordingly since the third layer brings more coil turns.

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## Curriculum Vitae

**Name:** Luyang Zhang

**Post-secondary Education and Degrees:** University of Electronic Science and Technology of China  
Chengdu, China  
2005-2009 B. Eng

The University of Western Ontario  
London, Ontario, Canada  
2012-2014 M.ESc

**Honours and Awards:** Connect Canada Internship Program  
2013

Western Research scholarship  
2012-2014

**Related Work Experience** Research Assistant  
The University of Western Ontario  
2012-2014