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## Fault Location in Series Compensated Transmission Lines

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A thesis submitted in partial fulfillment of the requirements for the degree in Master of  
Engineering Science  
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FAULT LOCATION IN SERIES COMPENSATED TRANSMISSION LINES  
(Thesis format: Monograph)

by

Tirath Pal Bains

Graduate Program in Electrical and Computer Engineering

A thesis submitted in partial fulfillment  
of the requirements for the degree of  
Masters in Engineering Sciences

The School of Graduate and Postdoctoral Studies  
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London, Ontario, Canada

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# Abstract

Due to the integration of modern technology such as electric vehicles, the emphasis is expected to shift from mechanical to electric power. Therefore, the need of increasing the power transmission capacity of the electric grid gets highlighted. Since, the construction of transmission lines is a tedious task owing to legalities, environmental impacts and high costs, the series compensated transmission lines are gaining popularity due to lesser costs and faster construction time. The series capacitor compensated transmission lines are very crucial lines due to the greater power being transmitted through them. Therefore, an accurate fault location becomes a prerequisite for limiting the loss of revenue and power continuity. However, fault location in series capacitor compensated transmission lines face multifaceted challenges due to the variety of factors including but not limited to the presence of sub-synchronous frequency components in the measured signals, interdependence of the fault current level and operation of series capacitor protection unit, presence of non-linear element, i.e., metal-oxide varistor as a part of series capacitor protection unit and dependence of the existing fault location algorithms on zero-sequence parameters of the series capacitor compensated transmission line which cannot be estimated accurately. In this thesis, the task of fault location in series capacitor compensated transmission lines has been explored in detail covering the entire spectrum of challenges starting from signal processing to how to obtain the fault location value with the least amount of uncertainty.

In this thesis, firstly a phasor estimation technique called the Enhanced Prony-DFT based on analysis in discrete-time domain has been proposed which identifies and completely removes the transients present in the measured signal, thus yielding highly consistent and accurate phasors. Fault location in series compensated transmission line is used as metric for the verification of the accuracy of estimated phasors. Thereafter, the focus is shifted towards the fault location algorithms for series compensated transmission lines. All the studies found in literature have considered the location of series capacitor in the middle of the transmission line. Therefore, secondly the configuration of series compensated line when series capacitor is located at one of its ends is also studied. It is discovered that the well-known fault location algorithms for series compensated transmission lines yield significantly higher errors when the series capacitor is located at the end of a transmission line. Therefore, rendering the already existing fault location algorithms useless for practical applications. Thirdly, the impact of series capacitor protection unit on fault location has been investigated which leads to a significant observation that MOV may get bypassed before the interruption of the fault for numerous fault scenarios. Therefore, a new complimentary fault location technique is proposed which provides more precise and accurate fault location results for the fault scenarios where MOV gets bypassed before fault interruption. The proposed complimentary technique is relatively more immune to the adverse effects of measurement errors and errors in the estimation of zero sequence components as compared to the existing techniques.

**Keywords:** Fault Location, Phasor Estimation, Series Compensation, Sub-synchronous Frequency Components.

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# Dedication

I dedicate this work to my family.

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## List of Abbreviations, Symbols, and Nomenclature

**ABC:** Phase A, Phase B and Phase C Fault

**AG:** Phase A to Ground Fault

**BC:** Phase B to Phase C Fault

**BCG:** Phase B and Phase C to Ground Fault

**CVT:** Capacitor Voltage Transformer

**CT:** Current Transformer

**DDCs:** Decaying DC Components

**DFT:** Discrete Fourier Transform

**DTFT:** Discrete Time Fourier Transform

**FACTS:** Flexible AC Transmission System

**FSC:** Fixed Series Capacitor

**HV:** High Voltage

**MOV:** Metal Oxide Varistor

**RSD:** Relative Standard Distribution

**SCCTL:** Series Compensator Compensated Transmission Line

**SCU:** Series Compensator Unit

**SCPU:** Series Capacitor Protection Unit

**SSFCs:** Sub-synchronous Frequency Components

**SSR:** Sub-synchronous Resonance

**SSSC:** Static Synchronous Series Capacitor

**TCSC:** Thyristor Controlled Series Capacitor

**THD:** Total Harmonic Distortion

**TSSC:** Thyristor Switched Series Capacitor

# Chapter 1

## Introduction

The growing use of modern technology has caused society's dependence on electrical power to expand rapidly, and consequentially it has led to the ever increasing electrical power demand. In order to meet the demand, newer generation plants including conventional and non-conventional power plants have already or have been proposed to be built. However, construction of power plants has little significance if there is no transmission capacity available to transport the power from generation centers to load centers. Therefore, bigger corridors of bulk power transmission, i.e., transmission lines are needed for connecting newer generating power stations to load centers. Transmission lines are the largest components of a power system which stretch out over large distances passing through various geographical and environmental backgrounds. Therefore, the construction of newer transmission lines is a tedious task owing to laws, environmental impacts, and prohibitive capital requirements. Therefore, the need arises to explore the various avenues for enhancing the power transfer capacity of the transmission lines. The power transfer capacity of a transmission line is given by (1.1),

$$P = \frac{|V_S| |V_R|}{|X_L|} \sin \delta \quad (1.1)$$

where,  $V_S$  is the sending end voltage;  $V_R$  is the receiving end voltage;  $X_L$  is the transmission line reactance, and  $\delta$  is the power angle as shown in Figure 1.1. The power transfer capacity

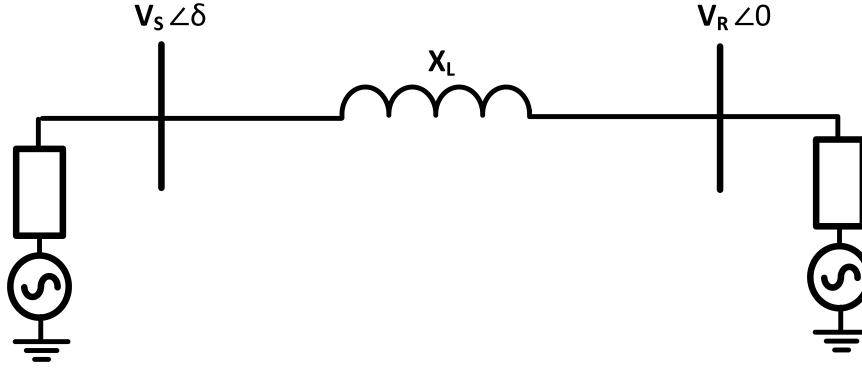


Figure 1.1: Simplified representation of a conventional transmission line

of the transmission line cannot be increased significantly by elevating the voltage levels as it could result in the failure of the insulators while excessive increase in  $\delta$  compromises the steady state as well as the transient stability of the power system. However, knowing the fact that  $X_L$  is inductive in nature,  $X_L$  can be reduced, as shown in Figure 1.2, by installing a capacitor in series with the transmission line in order to compensate the inductive voltage drop across the transmission line. The degree of capacitive compensation that can be put in a transmission line varies from 20% to 70%. Such transmission lines have been referred to as series capacitor compensated transmission lines (SCCTLs) in this thesis.

Since the inclusion of series capacitor compensates the inductive reactance of the line, the expression for power being transferred across a SCCTL becomes as represented in (1.2),

$$P = \frac{|V_S| |V_R|}{|X_L - X_C|} \sin \delta \quad (1.2)$$

where,  $X_C$  is the reactance of the series capacitor. Since the denominator of the (1.2) is smaller than that of (1.1), it results in a higher power transfer for the same value of  $V_S$ ,  $V_R$ , and  $\delta$ .

## 1.1 Series Capacitor Compensated Transmission Line

Different types of series compensation devices such as fixed series capacitor (FSC) and thyristor controlled series capacitor (TCSC) are available for increasing the power transfer capability

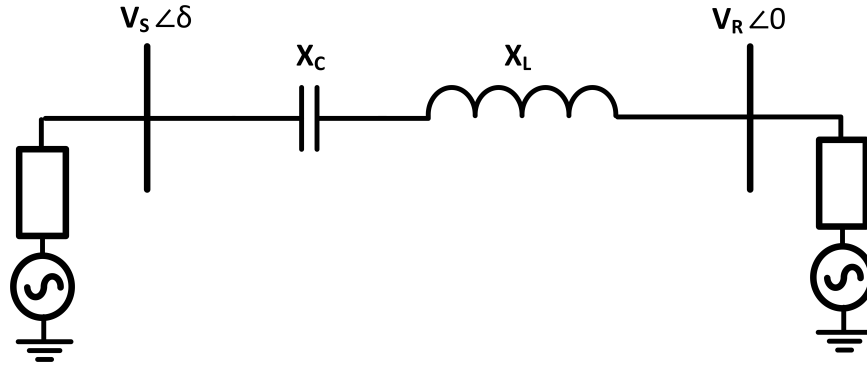


Figure 1.2: Simplified representation of a SCCTL

of a transmission line. TCSC provides variable series compensation which also provides dynamic power flow control, dampens the inter-area oscillations, and suppresses sub-synchronous resonance (SSR) [1]. However, if the above-mentioned controls are not of primary concern, FSC could be a more economical solution. Consequentially, series compensation using a fixed capacitor has gained popularity as it enhances the power transferred across a transmission line [3]-[4] with relatively less capital investment than to construct a new transmission line. Series capacitors also improve the steady state as well as transient stability of the power system [5]. The testament to the wide popularity of SCCTLs can be established from Figure 1.3 which shows the large number of SCCTLs present in the Hydro Quebec network. It could be noted here that installation of a series capacitor in a transmission line could potentially result in sub-synchronous resonance (SSR) if the predominant way of power generation is through turbo-alternators. Since the main source of power generation in Hydro Quebec network is through hydro-generators, the problem of SSR does not arise. Recently, two SCCTLs have been employed in Hydro One network in Ontario in the two single-circuit transmission lines between Hanmer at Sudbury and Essa at Barrie [5].

## 1.2 Series Capacitor Protection Unit

Since the voltage drop across series capacitor is directly proportional to the current flowing through it, the need arises to protect the series capacitor against the over-voltages due to heavy

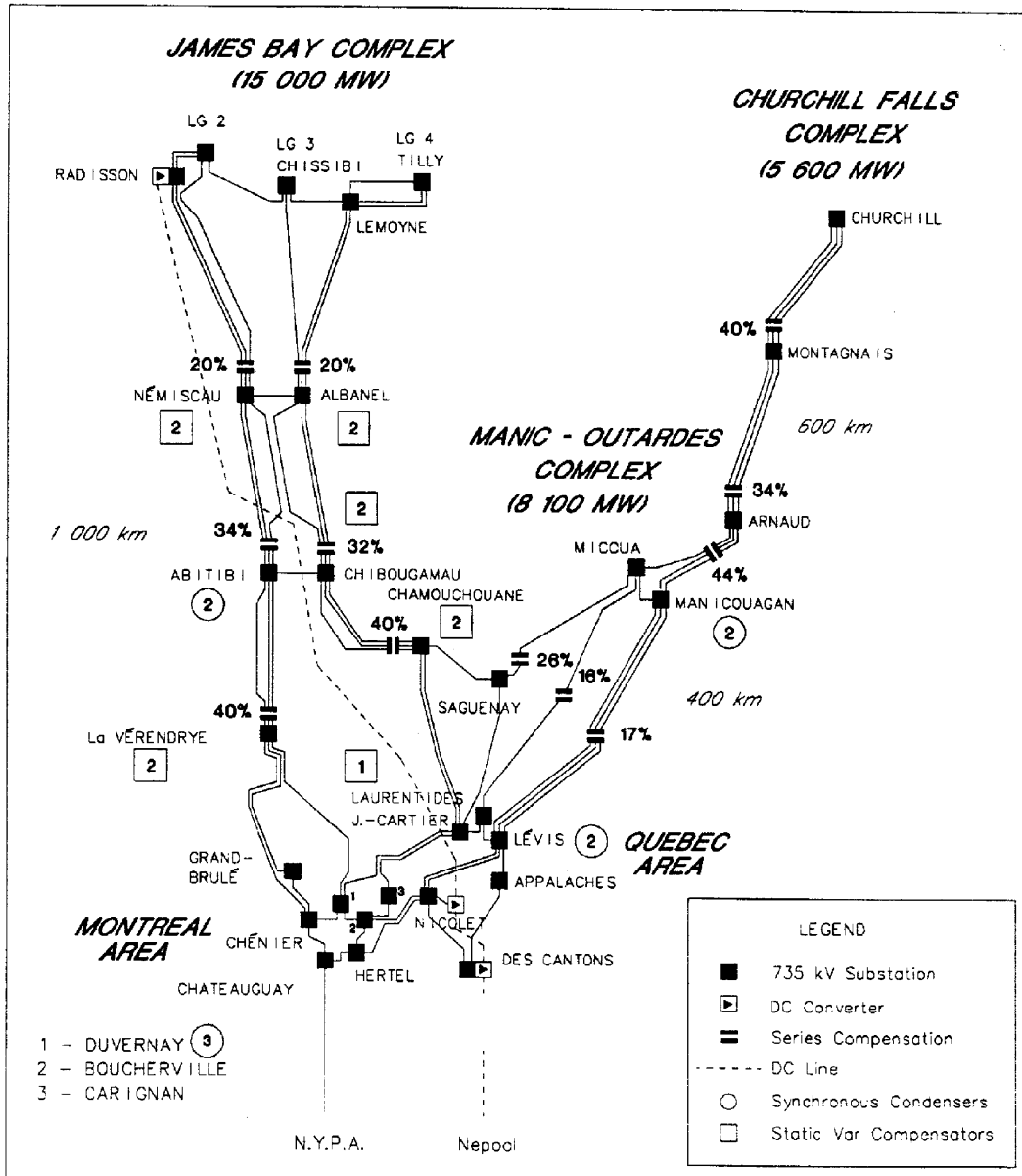


Figure 1.3: SCCTLs in Hydro Quebec network

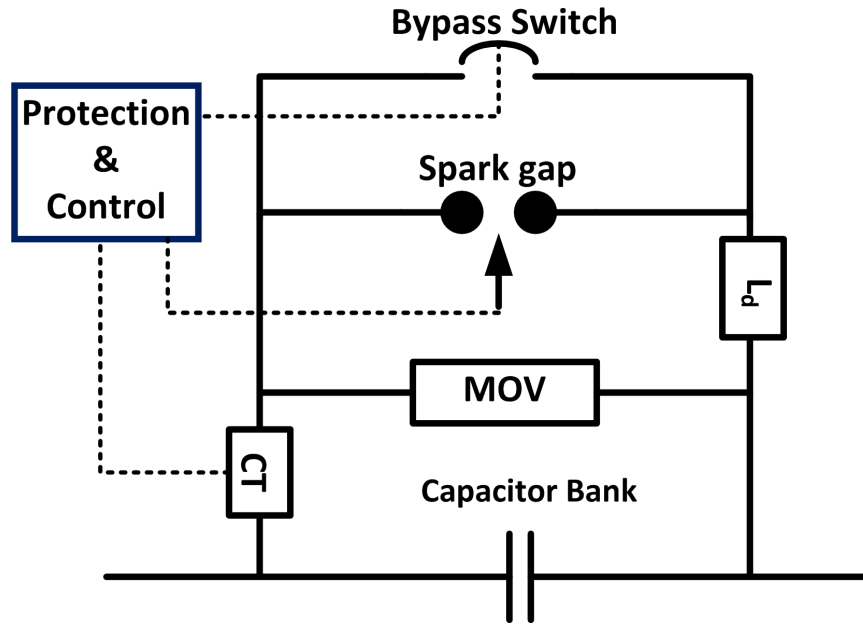


Figure 1.4: Series Capacitor Protection Unit (SCPU)

line loading conditions or faults in the system. Thus, in order to limit the voltage drop across series capacitor during a fault, a sophisticated protection system including metal oxide varistor (MOV), spark-gap and a bypass switch controlled by a digital protection and control system is employed [6] which is called series capacitor protection unit (SCPU) in this thesis while SCPU along with the series capacitor is referred to as series capacitor unit (SCU).

The most general form of SCPU is shown in the Figure 1.4. It consists of MOV, spark gap, bypass switch controlled by a dedicated protection and control system [6]. However, SCPU can be broadly categorized into three categories as follows: 1- Spark gap only configuration, 2- Gapless or MOV only scheme, 3- MOV-spark gap configuration. In the spark gap scheme of SCPU, there is no MOV while in MOV only scheme there is no spark gap present in SCPU. The MOV-spark gap scheme as shown in Figure 1.4 includes both, MOV and spark gap.

The spark gap only configuration has been used in the older installations of SCPU. During the fault event if the voltage across SCU exceeds the protective level, spark gap operates immediately. However, with the advancement of technology, MOV based SCPU configurations have replaced the spark gap only schemes. In the case of MOV based configurations of SCPU,



the protection of SCU is achieved by the partial conduction of fault current by MOV when the voltage across SCU reaches a predetermined level. In this way, MOV conduction limits the current flowing through series capacitor as well as the voltage drop across SCU at a safe level. However, MOV starts dissipating energy during the process of fault current conduction, resulting in the heating of MOV. If the energy dissipated by MOV reaches the predetermined threshold, MOV is immediately bypassed. MOV is also set to be bypassed if the fault current encountered is excessively high and greater than the bypass current threshold of MOV, thereby avoiding the unnecessary heating of MOV. The way this bypassing operation of MOV is done serves as the main distinction between MOV-spark gap and gapless scheme configuration of SCPU. The bypassing of MOV is achieved either by an ignition of spark gap in MOV-spark gap configuration or by the closing of bypass switch in gapless configuration of SCPU. However, bypass switch operates with a time delay of around two-three cycles of fundamental frequency as compared to only about 1-4 *ms* for spark gap. Therefore, this longer operating time of bypass switch translates into higher MOV energy dissipation requirements in the gapless scheme [7].

### **1.3 The Importance of Fault Location in SCCTLs**

The high power transfer capacity of SCCTLs makes them critical lines from the perspective of profitable operation of a power system. Though fault in a transmission line is a rare event, but it tends to be very severe whenever it occurs. Its severity is even higher in the case of a SCCTL. The line protection system of the faulted SCCTL clears the fault by isolating the faulted transmission line from the power system. The amount of lost revenue due to the tripping of a transmission line is proportional to the time it remains out of service. Therefore, tripping of a SCCTL would result in higher revenue losses due to greater loss of the power to be transmitted. For the quick restoration of the service, precise location of the fault is needed. Visual scanning of the transmission line for the location of fault is not feasible due to the sheer size

of the line. Hence, the mechanism of fault location is needed based on the voltage and current measurements to accurately estimate the location of a fault, thereby greatly improving the time required by maintenance crew to put line back into service.

## **1.4 Fault Location Algorithms**

Fault locations algorithms utilize the measured voltage and current at the terminals to yield the fault location. Fault location algorithms can be classified in number of ways. Depending on the domain in which the calculations are being performed, the fault locations can be categorized as time-based and phasor-based algorithms. They can also be classified into one-terminal or two-terminal fault location algorithms depending on whether it utilizes the measurements from one or both terminals of the transmission line. For two-terminal fault location algorithms, they can further be classified into synchronized or non-synchronized algorithms, relying upon the synchronization of the measurements obtained from both ends.

### **1.4.1 Time-based or Phasor-based Fault Location Algorithm**

Various instantaneous-time-based or differential-equation-based fault location algorithms have been proposed in [8], [9], [10] and [11]. Such algorithms are based on solution to the transmission line differential equations obtained using instantaneous values of the measured current and voltage signals in time domain, making them sensitive to the noise and harmonics present in the measured signal. Time-based algorithms are also sensitive to current transformer (CT) and capacitor voltage transformer (CVT) errors or any other unseen sources of error which hinders the faithful representation of the primary signal at the secondary side of the instrument transformer.

Phasor-based fault location algorithms, on the other hand, utilize the estimated phasors from the measured signals. The phasor estimation algorithms such as Discrete Fourier Transform (DFT) are able to attenuate noise and completely eradicate integer harmonics, thereby,

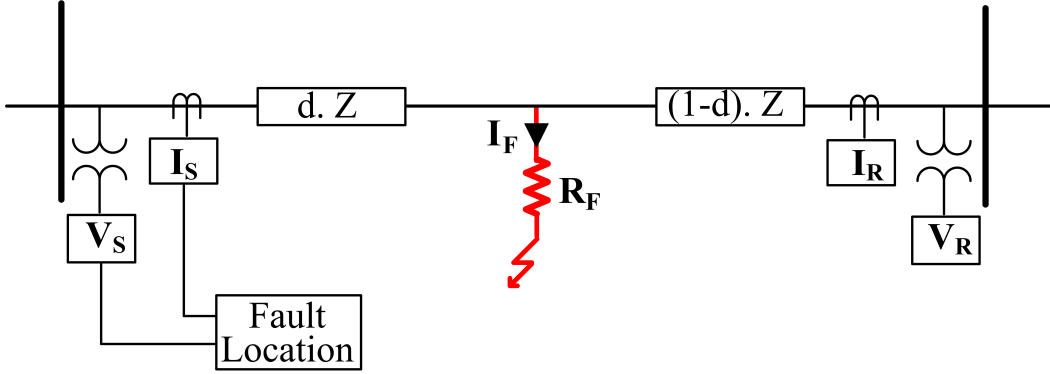


Figure 1.5: Schematic: Single-terminal Fault Location

making phasor based fault location, immune to the noise and integer harmonics in the measured signal. Phasor-based fault location algorithms have been applied successfully to the conventional transmission lines [12], [13].

#### 1.4.2 Single-terminal or Two-terminal Fault Location Algorithm

The single-terminal fault location algorithms can be found in older protection system, and less critical lines where no communication link is available between the two ends of the transmission line. Single-terminal fault location algorithms use the signals from only one end of the transmission line as shown in Figure 1.5 to estimate the seen impedance and corresponding fault location, very similar to a distance relay. Like a distance relay, single-terminal algorithms are also prone to errors for high impedance faults as can be justified from (1.3) where, the current fed from the other terminal of the transmission line impacts the fault location algorithm through term  $(II)$  as follow.

$$d' = \frac{V_S}{Z I_S} = \underbrace{d}_I + \underbrace{\frac{R_F(I_S + I_R)}{Z I_S}}_{II} \quad (1.3)$$

where,  $V_S$  and  $I_S$  are the sending end voltage and current, respectively;  $V_R$  and  $I_R$  are the receiving end voltage and current, respectively;  $d$  is the actual fault location;  $d'$  is the estimated fault location;  $R_F$  is the fault impedance and  $Z$  is the impedance of the entire line. Since,  $R_F$  is

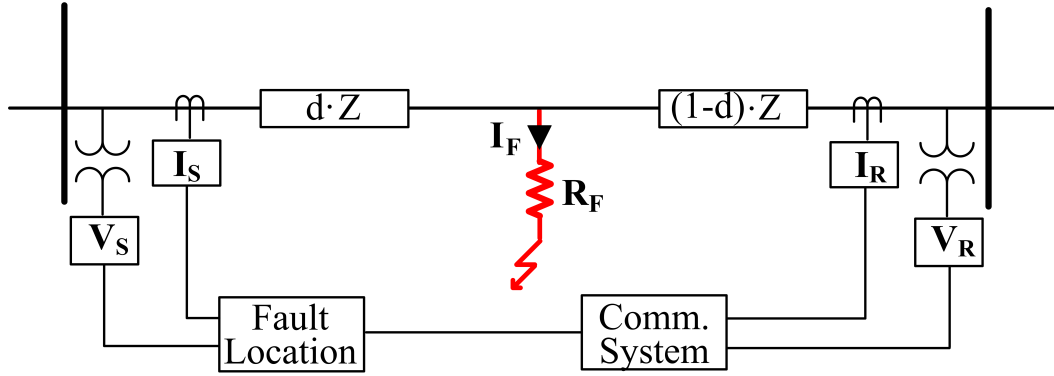


Figure 1.6: Schematic: Two-terminal Fault Location

unknown, the effect of term  $(II)$  on fault location result cannot be estimated.

It should be noted here that for the sake of simplicity in explaining the concept of single and two-terminal fault location algorithms, series RL model of the transmission line is used, and the mutual coupling between the phases is also ignored.

For the transmission lines where a communication system is available as depicted in Figure 1.6, two-terminal fault location algorithms are used invariably. In the case of two-terminal fault location algorithms, two equations can be written using the measured signals from both ends of the transmission line. In this way, the term containing fault impedance ( $R_F$ ) can be completely removed from the fault location equation as shown in (1.4); thus, eradicating the effect of fault impedance on the fault location result. In this way, the two-terminal fault location algorithm overcomes the limitations of the single-terminal algorithm.

$$d' = d = \frac{V_S - V_R + I_R Z}{(I_S + I_R) Z} \quad (1.4)$$

It should be noted here that the RL model of the transmission line has been used in the above elaboration only due to its simplicity. However, in order to make fault location more accurate, more precise model of transmission lines is utilized.

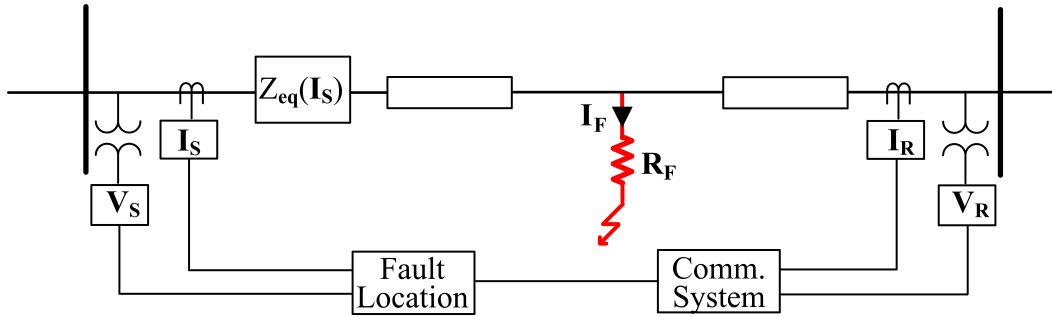


Figure 1.7: Fault Location in SCCTLs: MOV model based

### 1.4.3 Synchronised or non-Synchronised

In two-terminal fault location algorithms, it is important for measurements from both the ends of the line to correspond to the same time-instant. If the measurements have already been synchronized, the fault location algorithm can be applied directly. However, if the measurements have not been synchronized, then the measurements can be synchronized using pre-fault measured data [14].

## 1.5 Fault Location Algorithms for SCCTLs

In the presented thesis, only phasor-based, two-terminal algorithms have been discussed due to their higher accuracy and robustness, as already mentioned in the Section 1.4. The fault location in SCCTLs becomes more complex because of the presence of MOV as a part of SCPU. Now, due to the non linearity of MOV, the voltage drop across the MOV cannot be estimated accurately. Therefore, leaving the fault location algorithms for SCCTLs with two options, i.e., either to use the fault current dependent model of the MOV or to consider the natural fault loops of the system under fault. Ruling out one option comes with the compulsion of using the other. In [15] and [16], attempt has been made to predetermine V-I characteristics of MOV using its model in ATP-EMTP simulations for fundamental frequency which can then be used for fault location as shown in Figure 1.7. However, V-I characteristics of MOV can vary for different manufacturers, ambient temperature, and aging of MOV. Therefore, such

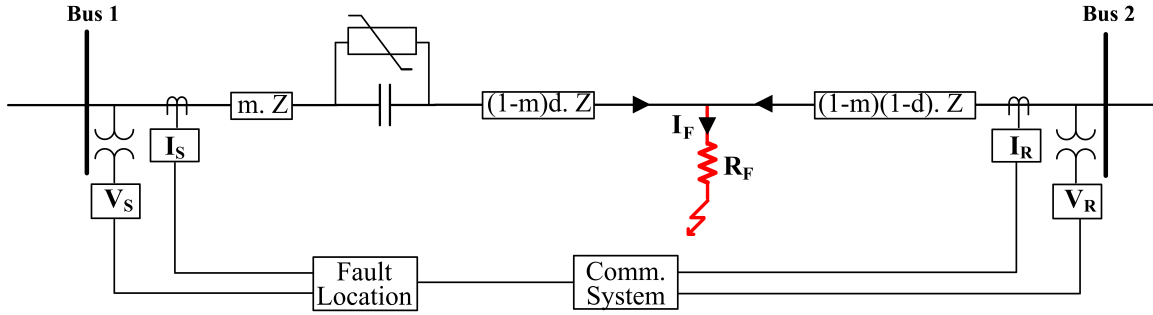


Figure 1.8: Schematic diagram of a faulted transmission line

algorithms would be very project specific and are subject to errors since various factors that affect MOV vary.

In [14], authors have avoided the use of MOV model in the fault location algorithm; therefore, consideration of natural fault loops becomes a necessity, forcing the usage of zero-sequence parameters. The fault location algorithm proposed in [14] is being used for the purpose of analysis in Chapter 3 and 4. A brief description of the algorithm is presented here for understanding the underlying principle, ignoring the mutual coupling among the phases and using the RL model of the transmission line. The detailed examination of the proposed fault location algorithm is presented in Chapter 3. The total fault current ( $I_F$ ) and fault loop voltage ( $V_F$ ) for any fault in a transmission line are given by (1.5) and (1.6), respectively. It should be noted that in this section, equations are written only for the faults lying in the section of the transmission line in between SCU and receiving end (Bus2) called Subroutine 1. For the faults lying in the section of transmission line between sending end bus (Bus1) and SCU, equations can be written analogously called Subroutine 2.

$$I_F = I_S + I_R \quad (1.5)$$

$$V_F = V_R - (1 - d)(1 - m) Z I_R \quad (1.6)$$

where,  $V_S$  and  $I_S$  are the sending end voltage and current, respectively;  $V_R$  and  $I_R$  are the receiving end voltage and current, respectively;  $Z$  is the total impedance of the line;  $l$  is the

length of the transmission line,  $d$  is the p.u. distance of the fault from SCU;  $m$  is the p.u. distance of the location of SCU from the sending end bus (Bus 1).

The fault loop equation, i.e., (1.7) can now be solved for fault location ( $d$ ) and fault resistance ( $R_F$ ) by separating real and imaginary parts, assuming that all the faults are purely resistive in nature [14], [16].

$$V_F(d) - R_F I_F(d) = 0 \quad (1.7)$$

The methodology of solving (1.7), by separating it into real and imaginary parts under the assumption that faults in a transmission lines are purely resistive in nature, makes the proposed algorithm essentially an argument comparison algorithm of the analytically estimated fault loop voltage and current as demonstrated later in the Chapter 3.

## 1.6 Challenges and Motivations

### 1.6.1 Phasor Estimation

Any SCCTL is essentially an under-damped RLC circuit owing to the presence of line inductance, series capacitor and small line resistance. Any fault in the power system acts as disturbance and triggers the transients which comprises of noise, harmonics, decaying DC (DDC) along with sub-synchronous frequency components (SSFC). The frequency of the oscillation is given by (1.8)

$$f_o = f_n \sqrt{\frac{X_C}{X_L + X_S}} \quad (1.8)$$

where,  $f_o$  is the sub-synchronous frequency component;  $X_C$  is the reactance of the series capacitor;  $X_S$  is the inductive reactance of the source;  $X_L$  is the inductive reactance of the line.

In order to obtain accurate phasors and, therefore, fault location, it is important for a phasor estimation technique to attenuate the transients significantly including SSFCs. Many techniques can be found in literature for filtering out DDC [17], [18], [19], [20]; however, very

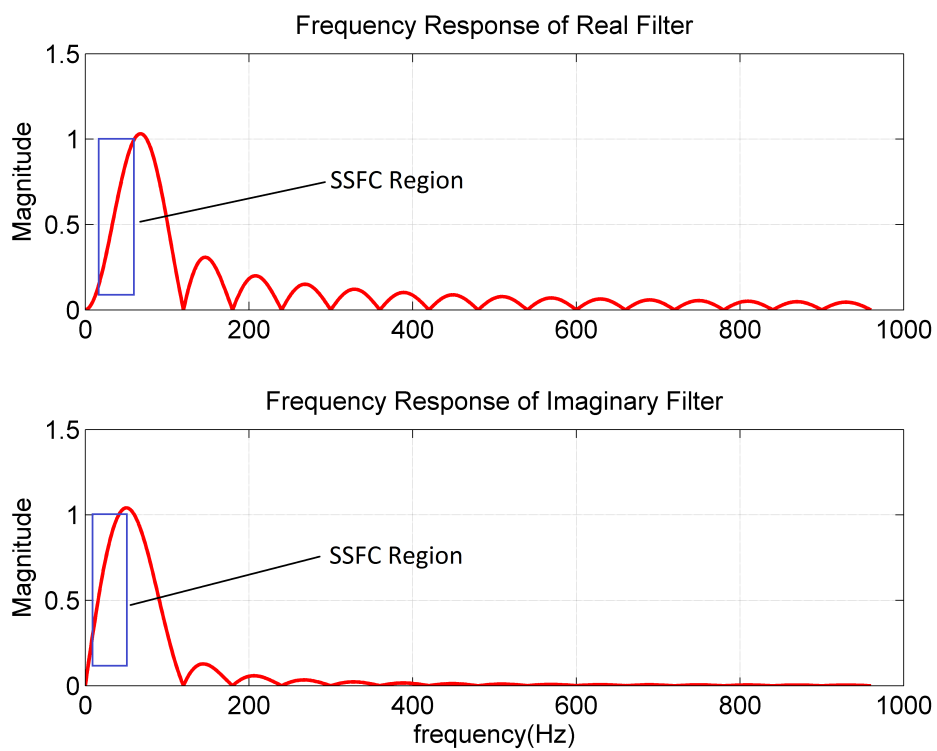


Figure 1.9: Frequency response of DFT: Real and imaginary filters



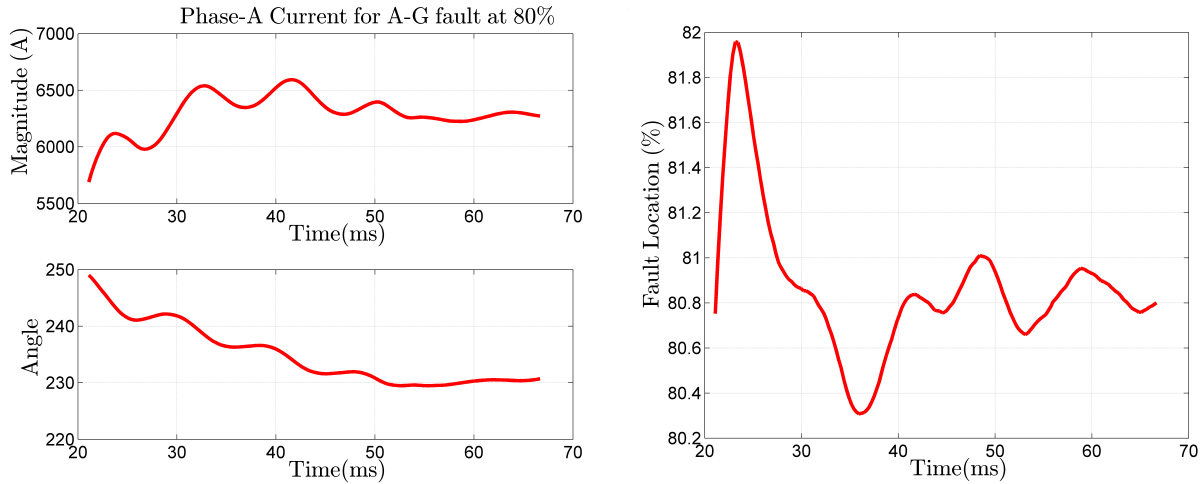


Figure 1.10: Oscillations: Estimated Phasor and Fault location

limited research has been reported regarding the attenuation of SSFCs. Figure 1.9 shows the frequency response of real and imaginary filters of DFT. Now, examining Figure 1.9, it can be observed that both real and imaginary filters are not able to attenuate SSFCs considerably. Therefore, leading to the oscillatory and erroneous phasor estimation as observed in the previous section. Figure 1.10 shows phasor estimation and fault location for AG fault at 80% of line length in a SCCTL obtained from simulation in PSCAD and Matlab. It can be clearly observed that the oscillations in the phasor estimation are further reflected in the fault location results. Various phasor estimation techniques have been proposed in literature to deal with SSFCs. In [22], it has been proposed to use reiterative short-window-DFT for estimating and eliminating SSFCs and DDCs from the measured signals. However, the proposed technique assumes that the measured signal would either contain a SSFC or a DDC for a given fault scenario for thyristor controlled series capacitor (TCSC) compensated transmission lines. However, it may not be true for fixed capacitor compensated transmission lines as PSCAD simulations justify that transients consisting of both SSFCs and DDCs are injected into the system at the incidence of the fault. Moreover, the accuracy of the proposed technique in [22] depends upon signal to noise ratio (SNR). Similarly, a Fourier filter algorithm has been proposed in [23] based on the assumption that the transients found in the measured signals of the SCCTLs after the fault in-

idence consist either of three DDCs or one SSFC and one DDC. Again, this assumption may not hold for all the system configurations and fault types. Moreover, both above techniques are based on differentiation of the measured signals which makes them sensitive to the higher noise level.

To overcome these problems, a long window offline phasor estimation technique has recently been proposed in [24] which has been referred to as Prony-DFT. The Prony-DFT involves estimating the transients present in the measured signals through Prony analysis and eradicating the transients from the measured signals to get a clean transient free waveform. However, Prony analysis is applied to the averaged measured signals rather than the actual signal because the Prony analysis is sensitive to noise and averaging of the signals removes the noise from the signal. Moreover, averaging also reduces the order of the signal by removing the fundamental frequency and its integer harmonics from the signal. The transients identified from the averaged signal are, thereafter, linked to the transients present in the actual measured signal using the equations derived in [24]. However, the mathematical analysis that leads to the derivation of these equations has been performed in continuous time domain while the implementation of the algorithm is carried out in discrete time domain. This makes the proposed technique in [24] vulnerable to the error of discretization. In order to limit the adverse impacts of the error of discretization, a dedicated averaging filter has been proposed in [24]. Nevertheless, the proposed technique still depends upon the high sampling frequency of the measured signal for its accuracy.

## 1.6.2 Fault Location Algorithm

The most promising phasor-based fault location algorithm for SCCTLs is proposed in [14] which avoids the use of MOV model, therefore, making the use of natural fault loops imperative [25]. However, the proposed fault location has some shortcomings which are discussed in this section.

1. A study has been done in [14], when SCU is located in the middle of a SCCTL as shown



in Figure 1.11(a). Although, the 'SCU in the middle' arrangement seems to be more general and the equations are more complex, including two subroutines and selection algorithm. However, as shown in Chapter 2, the algorithm shows undesired sensitivity when SCU is located at one of the ends of a transmission line as depicted in Figure 1.11(b). Also, when the SCU is located in the middle, all faults that occur in transmission line always lie at least 50% of the line length away from the bus that sees the same fault current as the SCU. However, when the SCU is located on the side of a line, the faults close to the SCU would result in higher involvement of MOV in the system, which affects the accuracy of the fault location algorithm as demonstrated in Chapter 3

2. The proposed algorithm in [14] uses the natural fault loops for fault location which necessitates the use of zero-sequence parameters of the transmission line for the ground faults, which are the most common faults in a transmission line. The zero-sequence parameters of the transmission lines are highly dependent on the soil resistivity which further depends on the continuously varying weather conditions, such as temperature, precipitation, and in particular moisture content of the soil. thus, ambiguity always remains about the accuracy of the estimated zero-sequence parameters. Moreover, the proposed algorithm involves argument comparison of the analytically calculated fault voltage and current using line end CT and CVT measurements [25]. CT and CVT errors may make the proposed algorithm to be prone to errors when gradient of the argument of voltage along the faulted section of the transmission line is very small. No evaluation was carried out in [14] regarding the effects of zero-sequence parameters error and CT and CVT errors on the performance of the proposed fault location algorithm.
3. All the proposed fault location algorithms found in the literature do not take into account the status of MOV in the power circuit, i.e., it is assumed that MOV is always in the power circuit during the entire duration of the fault. However, there is a possibility as discussed in Chapter 4 that MOV may get bypassed before the fault gets cleared. Bypassing of

MOV of the faulted phases before fault isolation actually opens a window of opportunity for developing a new complimentary fault technique, which could enhance the accuracy of the fault location in SCCTLs.

## 1.7 Research Objectives

### 1.7.1 Phasor Estimation

1. In this thesis, it is intended to develop an enhanced Prony-DFT method, so as to overcome the “mis-match” between the mathematical analysis and derivation of equations carried out in continuous time domain while the implementation being done in the discrete time domain as presented in [24]. The equations, relating the parameters of the transients present in the average signal as obtained by Prony analysis to the parameters of the actual transient components, would be derived in the discrete time domain. Therefore, the proposed technique becomes immune to the error of discretization. This thesis is also aimed at replacing the special averaging filter as proposed in [24], with a conventional averaging filter. The performance of the new enhanced approach would be evaluated through simulations in PSCAD and compared to the already existing Prony-DFT and 4-cycle DFT technique.
2. Prony-DFT is an off-line complex phasor estimation technique which requires long data window of 3-4 cycles. It is intended to study the fault location based on conventional and online phasor estimation techniques.

### 1.7.2 Fault Location

A comprehensive analysis of the established fault location algorithm proposed in [14] in lieu of the following factors is carried out in this thesis:

1. Location of SCU in the transmission line:

In order to expand the scope of fault scenarios, the SCU is moved from the middle of the transmission line to one of its ends. The proposed fault location algorithm in [14] is then studied for the effects of SCU location in a SCCTL on the fault location results. The detailed description and prognosis of the resulting errors are presented in Chapter 3.

## 2. Preposition of a new complimentary fault location algorithm for SCCTLs:

It is intended to develop a new complimentary fault location algorithm which gives a better performance than the well known fault location algorithm presented in [14] for the cases when MOV in the faulted phase(s) gets bypassed within the fault period.

## 1.8 Thesis Outline

This thesis is organized in to five chapters:

In the first chapter, an introduction to the research is presented along with the importance of the research to the area of fault location in SCCTLs. In the second chapter, an offline phasor estimation technique with special focus on the phasor based fault location in SCCTLs is discussed. An enhanced approach to the already existing technique is also presented. In the later part of the Chapter 2, the fault location obtained through conventional phasor estimation techniques is discussed. The enhanced approach proposed in Chapter 2, is compared with the existing technique and 4-cycle DFT through simulations in PSCAD and Matlab.

In Chapter 3, a well-known fault location algorithm is analyzed for the different locations of SCU in a transmission line as all the previous studies have limited their focus to the configuration when SCU is located in the middle of transmission line. The effects of interdependence of magnitude of fault current and SCPU operation on the fault location results in a SCCTL, are also presented in Chapter 3. The study performed is supported by PSCAD and Matlab simulations.

In Chapter 4, a complimentary fault location algorithm for SCCTLs is presented which improves the accuracy of the fault location results in the SCCTLs. The significance of the

complimentary technique has been elaborated through simulations in PSCAD and Matlab. The Chapter 5, summarizes the complete research work. Contributions and conclusion of the research work are presented. This chapter also discusses the scope for future research prospects.

## **1.9 Summary**

An introduction to the field of fault location in SCCTLs and the importance of the research conducted in this thesis was presented in this chapter. Then the various issues and existing proposed solutions associated with area of fault location in SCCTLs were discussed. Key contributions of the research work were highlighted. The research objectives and a detailed outline of the organization of the thesis was also provided in this chapter.

## **Chapter 2**

# **Enhanced Prony-DFT for Fault Location in Series Compensated Lines**

### **2.1 Introduction**

This chapter aims to explore and address the issues of oscillatory and imperfect phasor estimation of the measured signals in series capacitor compensated transmission lines (SCCTLs), with particular attention focused towards fault location. It has already been discussed in Section 1.6.1, that the attenuation of sub-synchronous frequency components (SSFCs), present in the measured signals of SCCTL, poses significant challenges for conventional phasor estimation algorithms used in protective relays. The techniques presented in [23] and [22] focus on the online attenuation of SSFCs. However, the scope of the proposed techniques remains limited as they are applicable to certain types and conditions of series compensated lines. Moreover, the techniques presented in [23] and [22] are based on the differentiation of the measured signals which makes them sensitive to the presence of noise in the signals. In this regard, a new offline technique, i.e, Prony-DFT has recently been presented in [24], where an attempt has been made to identify the parameters of the transients present in the measured signals using Prony analysis. Thereafter, the transient signal is regenerated and subtracted from the actual signal,



yielding a clear signal which contains only fundamental frequency and its integer harmonics. Phasors for the measured signal are then obtained by applying DFT to the resulting clear signal. Brief introduction to the methodology of the proposed technique of [24] referred to as Traditional-Prony-DFT is presented in this chapter. The area where Traditional-Prony-DFT might show susceptibility to the error has been identified and addressed through the preposition of Enhanced-Prony-DFT. The performance of the Enhanced-Prony-DFT is then compared with the Traditional-Prony-DFT and 4-cycle DFT through simulations carried out in PSCAD and Matlab, covering comprehensive fault scenarios. As proposed in [24], capacitor voltage transformer (CVT) is assumed to be present on the line side of SCU, so as to enable the use of the well known fault location algorithm proposed in [12].

Prony analysis forms the basis of Prony-DFT and Prony analysis needs 3-4 cycles of fault data to provide accurate phasors. However, as discussed later in the Chapter 3 and 4, such long window of data may not be always available due to the operation of series capacitor protection unit (SCPU). Therefore, fault location results obtained using the phasors estimated through conventional phasor estimation techniques such as the Cosine algorithm, have been studied in this chapter.

In this chapter, the Traditional-Prony-DFT is explained briefly in Section 2.2, covering the underlying concept, implementation and areas of further improvements. Enhanced approach to Prony-DFT is presented in Section 2.4 which is validated through fault location analysis carried out in PSCAD and Matlab in Section 2.5. The comparison of the Enhanced-Prony-DFT with existing Prony-DFT is also given in Section 2.5. The behavior of the fault location obtained using phasors estimated by Cosine algorithm is explored in Section 2.6.

## **2.2 Traditional-Prony-DFT**

It is proposed in [24] that due to the sensitivity of Prony analysis to noise, the direct use of Prony method to analyze fault current and voltage of a series capacitor compensated transmis-

sion line (SCCTLs) results in a considerable error. Therefore, a new Prony-DFT technique is proposed in [24] which first uses an averaging digital filter to attenuate the noise, remove the fundamental component and its harmonics from the measured fault current/voltage signal. Then, Prony analysis is applied to the averaged transient signal to identify the most accurate parameters of the transients present in the signal, by using the curve-fitting. The parameters of the original transient signal are then estimated from averaged parameters by using the mathematical relationship derived in the next section. After identifying the parameters, the original transient signals is re-constructed. The reconstructed transient signal is then subtracted from the original fault signal to obtain the fundamental signal. This fundamental signal is then fed to 1-cycle DFT to estimate phasors.

### 2.2.1 Mathematical Analysis

The mathematical analysis that form the basis of Traditional-Prony-DFT as given in [24] has been presented in this section.

In case of SCCTLs, fault current or voltage can be represented as a combination of fundamental frequency component (I), its integer harmonics (II), transient frequency components including SSFCs, DDCs and non-integer harmonics (III), and noise as denoted by (2.1). It is important to note here that  $f_r^s$  is 0 in case of DDCs.

$$i(t) = \underbrace{A_1 \cos(2\pi f_1 t + \phi_1)}_{\text{I}} + \underbrace{\sum_{k=2}^L A_k \cos(k 2\pi f_1 t + \phi_k)}_{\text{II}} + \underbrace{\sum_{r=1}^M B_r e^{\frac{t}{\tau_r}} \cos(2\pi f_r^s t + \phi_r^s)}_{\text{III}} + \text{noise} \quad (2.1)$$

where

$L$  is the total number of fundamental and its integer harmonics;  $M$  is total number of transient components;  $A_k$  and  $\phi_k$  are magnitude and angle of the  $k^{\text{th}}$  harmonic component, respectively;  $k=1$  represents the fundamental frequency component;  $f_1$  is the fundamental frequency;  $B_r$ ,  $\tau_r$ ,  $f_r^s$ , and  $\phi_r^s$  are magnitude, time constant, frequency, and angle of the  $r^{\text{th}}$  transient frequency

component, respectively.

The measured signal, i.e.,  $i(t)$  is passed through a moving average filter to obtain  $i_{avg}(t)$  as defined in (2.2). To simplify the use of Prony analysis, it is assumed that the first sample of  $i_{avg}(t)$  belongs to  $t=0$  rather than  $t=T$ . Hence, (2.2) is defined from  $t' = t$  to  $t + T$  instead of  $t' = t - T$  to  $t$  to compensate the time reference shift in the Prony analysis.

$$i_{avg}(t) = \frac{1}{T} \int_t^{t+T} i(t') dt' \quad (2.2)$$

It is a known fact that the average value of the fundamental and its harmonic components over the period of fundamental frequency component ( $T$ ) is zero. In addition, averaging significantly attenuates the noise present in the measured signal. Therefore, we can rewrite (2.2) by only considering the term (III) as below.

$$i_{avg}(t) = \frac{1}{T} \int_t^{t+T} \sum_{r=1}^L B_r e^{\frac{t}{\tau_r}} \cos(2\pi f_r^s t' + \phi_r^s) dt' \quad (2.3)$$

Integration by part theorem is employed to determine the analytical form of (2.3) which can be rewritten as in (2.4) [26].

$$i_{avg}(t) = \sum_{r=1}^L \tilde{B}_r e^{\frac{t}{\tau_r}} \cos(2\pi f_r^s t + \tilde{\phi}_r^s) \quad (2.4)$$

where

$$\tilde{B}_r = \frac{1}{T} \left( B_r \cdot \frac{\tau_r}{1 + (\tau_r 2\pi f_r^s)^2} \cdot \sqrt{X_r^2 + Y_r^2} \right) \quad (2.5)$$

$$\tilde{\phi}_r^s = \phi_r^s - \arg(X_r + jY_r) = \phi_r^s - \tan^{-1} \left( \frac{Y_r}{X_r} \right) \quad (2.6)$$

$$X_r = \tau_r 2\pi f_r^s \cdot e^{\frac{T}{\tau_r}} \cos(2\pi f_r^s T) - \tau_r 2\pi f_r^s - e^{\frac{T}{\tau_r}} \sin(2\pi f_r^s T) \quad (2.7)$$

$$Y_r = e^{\frac{T}{\tau_r}} \cos(2\pi f_r^s T) + \tau_r 2\pi f_r^s \cdot e^{\frac{T}{\tau_r}} \sin(2\pi f_r^s T) - 1 \quad (2.8)$$

It may be noted from (2.4) that the extracted signal through averaging filter, i.e.,  $i_{avg}(t)$ , preserves its oscillation frequencies and time constants. However, the magnitudes and phase angles undergo a change. The averaged signal i.e.  $i_{avg}(t)$  is now analyzed using Prony analysis,

the extracted signal's parameters ( $\tilde{B}_r, f_r^s, \tilde{\phi}_r^s$  and  $\tau_r$ ) are estimated. Using these parameters,  $X_r$  and  $Y_r$  are calculated from (2.7) and (2.8), respectively. The transient signal parameters  $B_r$  and  $\phi_r^s$  are calculated from (2.9) and (2.10). Equations (2.9) and (2.10) are directly derived from (2.5) and (2.6), respectively.

$$B_r = T \tilde{B}_r \cdot \frac{1 + (\tau_r 2\pi f_r^s)^2}{\tau_r \sqrt{X_r^2 + Y_r^2}} \quad (2.9)$$

$$\phi_r^s = \tilde{\phi}_r^s + \tan^{-1} \left( \frac{Y_r}{X_r} \right) \quad (2.10)$$

It can be observed from the Section 2.2.1 that the equations linking transients present in the averaged signal to those in the actual measured signals, are derived in the continuous time domain in [24]. However, the implementation of the algorithm is done in discrete time domain as given in Section 2.2.2.

### 2.2.2 Implementation

The process of obtaining accurate phasors for the proposed technique is shown in Figure 2.1. In the proposed algorithm, first, the sampled measured signal  $i[n]$ , represented by (2.11), is passed through an averaging digital filter.

$$i[n] = i\left(\frac{n}{f_s}\right) \quad n = 0, 1 \dots N_F - 1 \quad (2.11)$$

where  $N_F$  is the total number of measured signal samples and  $f_s$  is the sampling frequency. The conventional averaging filter is an  $N$  tap digital filter where  $N$  is the number of samples per cycle and filter taps are equal to  $1/N$ . Use of the conventional filter is an accurate estimate of (2.2) only if the sampling frequency is very high.

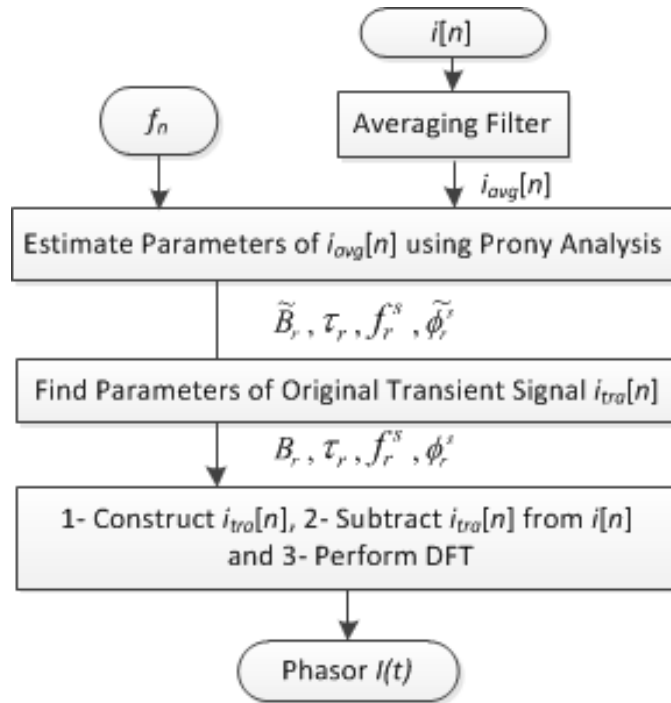


Figure 2.1: The flowchart depicting the flow process of Prony-DFT

In case of typical sampling rates in protective relays, a small difference is observed between the responses of averaging filter in continuous and discrete time domains. This can adversely affect the accuracy of phasor-based fault location algorithms. In order to avoid this problem, it is proposed to use an  $N + 1$  averaging filter as shown in (2.12) to achieve higher accuracy for a typical sampling frequency in protection relays. Figure 2.2 shows the percentage error of both the conventional (ideal) and proposed averaging filter, for a test signal, i.e.,  $5e^{\frac{-t}{0.02}} \cos(194t + 85.9^\circ)$ . Sampling rate is assumed to be 64 samples per cycle, i.e.,  $N = 64$  and  $f_s = N \times f_n$ . Fundamental frequency shown as  $f_n$  in Figure 2.1 is the estimated frequency to minimize the error during off-nominal frequency operation. As shown in Figure 2.2, the conventional averaging filter can introduce up to 1.8% of error while this is 0.02% in case of the proposed averaging filter. The performance of the proposed averaging filter is evaluated for test signals with different time constants, frequencies and initial angles.

$$i_{avg}[n] = \frac{1}{N} \sum_{r=1}^{N-1} i[n-r] + \left( \frac{i[n] + i[n-N]}{2N} \right) \quad (2.12)$$

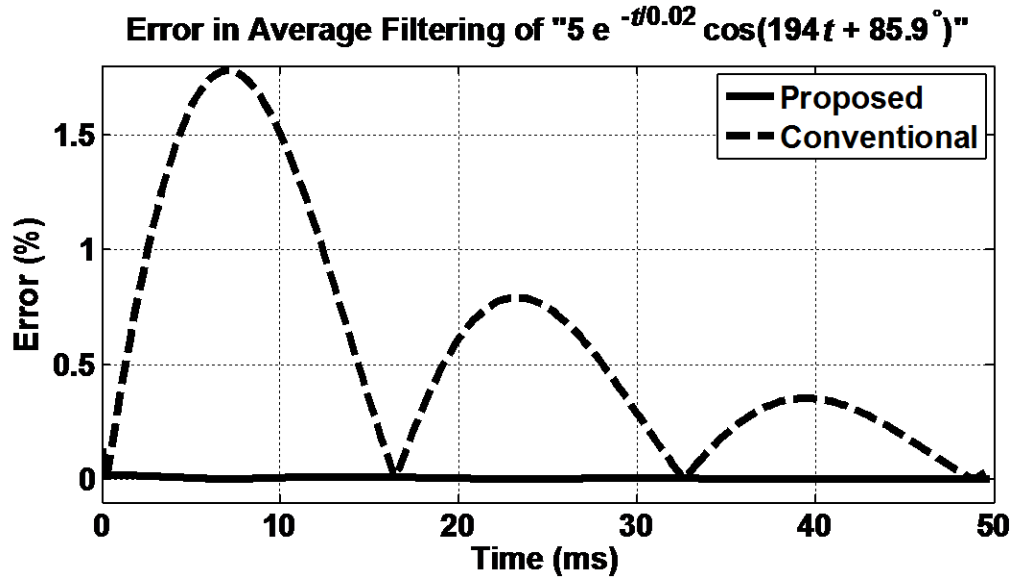


Figure 2.2: Error comparison of the ideal and proposed averaging filter

This filtered signal  $i_{avg}[n]$  contains information about transient frequency components including SSFCs, DDCs, and non-integer harmonics. These components are identified by Prony analysis and compensated by the proposed algorithm. The length of  $i_{avg}[n]$  after discarding initial one cycle of transient response of digital filter is  $N_F - N$ . Assuming that the measured signal length is four cycles and  $N$  is 64, the length of  $i_{avg}[n]$  after removal of the first cycle becomes 3 cycles =  $3 \times 64 = 192$  samples.

Prony function available in MATLAB signal processing toolbox is employed to identify and estimate parameters of different frequency components within  $i_{avg}[n]$ . Prony analysis can be carried out for different number of modes limited to half of the length of  $i_{avg}[n]$ , i.e., 96 in this case [27]. Lower number of modes results in less accurate estimation [28], therefore, minimum number of modes in the study carried out in [24] is 10. Consequently, Prony analysis is repeated for number of the modes between 10 and 96. Due to the error in frequency estimation, it is possible that the averaged signal contains modes with frequency close to the fundamental and its integral harmonics. Reconstruction of these modes is avoided by excluding all the modes with frequencies within range of  $(3\%) \times p \times f_1$  where,  $p = 1$  to 8 or the frequencies above 8<sup>th</sup> harmonic from the signal identification process. A threshold of 3% is

selected assuming maximum error of 3% in frequency tracking and 8<sup>th</sup> harmonic is selected to capture low frequency components generated during non-single-phase faults. In each mode, the residue of the input signal ( $i_{avg}[n]$ ) and the estimated signal by Prony analysis is computed. The parameters ( $\tilde{B}_r$ ,  $f_r^s$ ,  $\tilde{\phi}_r^s$ , and  $\tau_r$ ) corresponding to the mode which gives the minimum error or the best fit are chosen. If the minimum error is above the acceptable level, e.g., 5%, it is recommended to avoid signal compensation to avoid introducing any extra error.

$B_r$  and  $\phi_r^s$  are calculated as per (2.9) and (2.10). Finally, as shown in Figure 2.1, the transient signal ( $i_{tra}[n]$ ) is reconstructed for  $N_F$  sample and subtracted from the original measured signal  $i[n]$ . DFT is applied to the resulted signal to estimate the measured signal phasor.

## 2.3 Traditional-Prony-DFT: Areas for Improvement

The equations 2.3-2.10, used in order to convert the parameters of the extracted signal from the average signal to the actual transient signal, have been derived in continuous time frame. Whereas, the implementation of the proposed technique has been done in discrete time domain, assuming that the equations in continuous time domain are a close approximation of the equations in continuous time domain. However, as presented in Section 2.2.2, the conventional averaging in continuous time domain and in discrete time domain as represented by (2.4) and (2.11) respectively, yields slightly different results which may introduce error in the phasor estimation. Thus, a special averaging filter, as given in (2.12) has been proposed in [24] which lowers the error considerably, thus, enabling the use of the expressions derived in the continuous time domain.

Nevertheless, the parameters of the transients present in the averaged signal ( $\tilde{B}_r$ ,  $f_r^s$ ,  $\tilde{\phi}_r^s$ , and  $\tau_r$ ) are still being related to the parameters of the actual transients ( $B_r$ ,  $f_r^s$ ,  $\phi_r^s$  and  $\tau_r$ ) by using the expressions given in (2.9)-(2.10), which have been derived in continuous time domain. This mismatch between the mathematical analysis and implementation, being carried out in continuous and discrete time domains, respectively, may make the proposed technique vulnerable to

the error of discretization for other sampling rates.

In this chapter, the complete mathematical analysis is performed in discrete time domain, leading to the derivation of equations in discrete time domain. Since, no interlinking of two time domains is needed, therefore, the conventional averaging filter can now be utilized. Consequently, the actual implementation of the whole process is backed with the exact mathematical analysis, thereby, eradicating the possibility of error due to approximations and discretization.

## 2.4 Proposed Technique: Enhanced-Prony-DFT

The measured fault currents and voltages in SCCTLs, in discrete time domain, can be expressed as (2.13). The fundamental component is represented by I; II depicts the integer harmonics, and III represents all of the transients including DDCs and SSFCs. The noise encountered in the measurements is separately noted in (2.13).

$$i[n] = \underbrace{A_1 \cos\left(2\pi \frac{f_1}{f_s} n + \phi_1\right)}_{\text{I}} + \underbrace{\sum_{k=2}^L A_k \cos\left(2\pi k \frac{f_1}{f_s} n + \phi_k\right)}_{\text{II}} + \underbrace{\sum_{r=1}^M B_r e^{\frac{n}{f_s \tau_r}} \cos\left(2\pi \frac{f_r^s}{f_s} n + \phi_r^s\right)}_{\text{III}} + \text{noise} \quad (2.13)$$

where  $n = 0, 1, 2, \dots, N_T - 1$ ;  $N_T$  is the total of recorded samples;  $L$  is the total number of fundamental and its integer harmonics;  $M$  is the total number of transient components;  $f_s$  is the sampling frequency;  $f_1$  is the fundamental frequency;  $A_k, \phi_k$  are the magnitude and phase angle of  $k^{\text{th}}$  harmonic component;  $k = 1$  represents the fundamental component;  $B_r, \tau_r, f_r^s$  and  $\phi_r^s$  are the magnitude, time constant, frequency, and phase angle of  $r^{\text{th}}$  transient frequency component, respectively.

The measured signal is first passed through the conventional averaging filter as represented by (2.14). Since, averaging filtering takes one full cycle of fundamental frequency to yield the



first sample of the output, therefore, the first sample of  $i_{avg}$  will occur at  $n = N - 1$  where  $N = f_s/f_1$  is the number of data samples per cycle of the fundamental frequency. However, for making the implementation of the Prony analysis simpler, it is assumed that the first and last samples of  $i_{avg}$  corresponds to  $n = 0$  and  $n = N_T - N$  respectively, rather than  $n = N - 1$  and  $n = N_T - 1$ .

$$i_{avg}[n] = \frac{1}{N} \sum_{n'=n}^{n+N-1} i[n'] \quad (2.14)$$

It has already been mentioned in Section 2.2.2 that the average of the fundamental component and its integer harmonics over one cycle of the fundamental frequency is zero and averaging of sampled data also leads to the significant attenuation of the noise present in the measured signals. Therefore, the only term that appears in the expression for the output of the averaging filter as given in (2.15) is the term representing the average of transient components of the signal.

$$i_{avg}[n] = \frac{1}{N} \sum_{n'=n}^{n+N-1} \sum_{r=1}^M B_r e^{\frac{n'}{f_s \tau_r}} \cos(2\pi \frac{f_r^s}{f_s} n' + \phi_r^s) \quad (2.15)$$

Equation (2.15), when evaluated using Euler's formula and summation of the geometric series, leads to the expression depicted in (2.16). The significance of the result obtained from the averaging filter lies in the fact that the time constant ( $\tau_r$ ) and frequency ( $f_r^s$ ) of a each individual transient component remains unchanged after averaging as evident from (2.16). Whereas, the magnitude ( $B_r$ ) and the phase angle ( $\phi_r$ ) of the transient signals do undergo a change as per (2.17) and (2.18). Therefore, the application of Prony analysis to the average signal yields the parameters of the average of each transient component (i.e.,  $\widetilde{B}_r$ ,  $\widetilde{\phi}_r^s$ ,  $\tau_r$  and  $f_r^s$ ).

$$i_{avg}[n] = \sum_{r=1}^M \widetilde{B}_r e^{\frac{n}{f_s \tau_r}} \cos(2\pi \frac{f_r^s}{f_s} n + \widetilde{\phi}_r^s) \quad (2.16)$$

where

$$\widetilde{B}_r = B_r \times K \quad (2.17)$$

$$\widetilde{\phi}_r^s = \phi_r^s + \alpha \quad (2.18)$$

$$K = \frac{1}{N} \left( \frac{e^{\frac{2}{f_1 \tau_r}} - 2e^{\frac{1}{f_1 \tau_r}} \cos(2\pi \frac{f_s}{f_1}) + 1}{e^{\frac{2}{f_s \tau_r}} - 2e^{\frac{1}{f_s \tau_r}} \cos(2\pi \frac{f_s}{f_s}) + 1} \right)^{\frac{1}{2}}$$

$$\alpha = \tan^{-1} \left( \frac{e^{\frac{1}{f_1 \tau_r}} \sin(2\pi \frac{f_s}{f_1})}{e^{\frac{1}{f_1 \tau_r}} \cos(2\pi \frac{f_s}{f_1}) - 1} \right) - \tan^{-1} \left( \frac{e^{\frac{1}{f_s \tau_r}} \sin(2\pi \frac{f_s}{f_s})}{e^{\frac{1}{f_s \tau_r}} \cos(2\pi \frac{f_s}{f_s}) - 1} \right)$$

The parameters for the transients present in the actual signal i.e.  $(B_r, \phi_r^s, \tau_r$  and  $f_r^s)$  are obtained using Prony analysis in conjunction with expressions given in (2.19) and (2.20) as applied in [24]. The transient signal is regenerated by using the obtained parameters and is then subtracted from the measured signal, thereby, resulting in a transient free signal which contains fundamental frequency and its integer harmonics only. Phasor estimation techniques such as DFT can now be applied to the resulting clear signal which would yield very accurate phasors for fault location.

$$B_r = \frac{\widetilde{B}_r}{K} \quad (2.19)$$

$$\phi_r^s = \widetilde{\phi}_r^s - \alpha \quad (2.20)$$

## 2.5 Evaluation of the Proposed Method

Evaluation of the proposed technique is carried out through the signals obtained from the power system simulation in PSCAD rather than the theoretically generated signal, as non-linear characteristics of MOV cannot be represented accurately through theoretical signal. Figure 2.3 shows the 500 kV system considered in PSCAD for the study of the application of the proposed technique, i.e., Enhanced-Prony-DFT to fault location in SCCTLs. Frequency dependent model of transmission lines as available in PSCAD has been used for Line 1 and Line 2. A  $30\mu\text{F}$  series capacitor is located at the Bus A which corresponds to 67.5% series compensation of the Lines 1 and 2 equivalent inductance. The rated current for the series capacitor is 1180A. As per the methodology mentioned in [25], MOV rating after the consideration of overloading

is 153kV. The line positive and zero sequence impedances are  $Z_{L1} = (0.0179 + j0.3748) \Omega/\text{km}$ ,  $Z_{L0} = (0.3447 + j1.216) \Omega/\text{km}$ , respectively, and the line positive and zero sequence admittances are  $Y_{L1} = (0.1 \times 10^{-7} + j4.378 \times 10^{-6}) \text{U}/\text{km}$ ,  $Y_{L0} = (0.1 \times 10^{-7} + j2.747 \times 10^{-6}) \text{U}/\text{km}$ , respectively. Positive and zero sequence impedances for sending end source are  $Z_{S1} = (1 + j25) \Omega$ ,  $Z_{S0} = (8 + j50) \Omega$ , respectively and positive and zero sequence impedances for receiving end source are  $Z_{R1} = (1 + j38.5) \Omega$ ,  $Z_{R0} = (12 + j76) \Omega$ , respectively. Load angle is  $30^\circ$  with receiving end source voltage lagging.

Voltage and current signals are obtained by using Current transformer (CT) and Capacitor voltage transformer (CVT) models available in PSCAD. A second-order butter-worth low-pass anti-aliasing filter with a cutoff frequency of 1920Hz is applied to the output of each instrument transformer, and its output is recorded with the sampling rate of 20 kHz. The recorded signal is imported and resampled at 3840Hz in Matlab. Voltage and current signals corresponding to the fault duration are separated from the entire recorded data. The fault clearance interval in the presented study is presumed to be four cycles of the fundamental frequency.

The implementation of Enhanced-Prony-DFT has been elaborated through its application to phase A voltage of the sending end for a solid AG fault at 60% of the transmission line length from Bus A as shown in Figure 2.4. As evident from Figure 2.4 (a), considerable amount of SSFCs and other transients are embedded in the measured voltage signal. Figure 2.4 (b) depicts that the actual averaged signal which is applied to Prony analysis is identical to the average signal generated via parameters obtained through Prony analysis, thus, implying the high accuracy of Prony analysis. The transient signal as shown in Figure 2.4 (c) for the entire fault duration is generated, using Prony results and derived expressions in (2.19) and (2.20). The transient signal is then subtracted from the original signal to obtain the compensated signal. Figure 2.4 (a) shows that the compensated signal is independent of transient and other off nominal frequency components unlike original signal which is infested with a high degree of transients.

Compensated signal is fed to DFT while the original signal is fed to 4-cycle DFT phasor

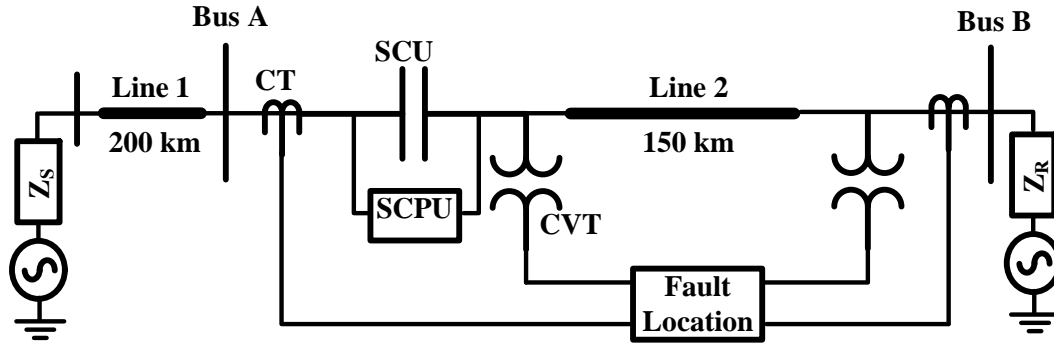


Figure 2.3: Single-line diagram of the simulated system in PSCAD

estimation algorithm. Basis for selecting the 4-cycle DFT for the comparative performance analysis of the Enhanced-Prony-DFT is its better ability to attenuate SSFCs than full-cycle DFT. Figure 2.4 (d) shows that the estimated phasor obtained by Enhanced-Prony-DFT remains consistent throughout the fault interval, therefore, implying that the proposed technique is able to effectively, attenuate SSFCs and other transients. Since 4-cycle DFT estimates only one phasor value for the entire fault data, the magnitude and angle of this phasor are depicted in Figure 2.4 (d). The results of both the phasor estimation techniques are fed to the fault location algorithm proposed in [12]. Since, the actual value of the voltage phasor is unknown, the accuracy of the respective phasor estimation techniques cannot be comprehended this way. Therefore, the fault location has been used as an indicator of the relative accuracy of the proposed phasor estimation algorithm. It should be noted that the final value for the fault location by Enhanced-Prony-DFT is obtained by averaging the fault location results over three cycles as proposed in [24]. In order to validate the performance of the Enhanced-Prony-DFT, a total number of 84 fault scenarios have been simulated in PSCAD using the system shown in Figure 2.3 for different fault locations ( from 0% to 100% with steps of 20%), fault types (AG, BC, BCG, ABC), fault resistances (AG: 0  $\Omega$  and 10  $\Omega$ , BC and BCG: 0  $\Omega$  and 6  $\Omega$  and ABC: 0  $\Omega$ ) and fault instances (zero and peak points on wave).

The fault location results obtained from the Enhanced-Prony-DFT, has been compared with the results obtained from Prony-DFT implemented as proposed in [24] (Traditional-Prony-DFT) and 4-cycle DFT. The fault location error is defined as percentage of the length of the

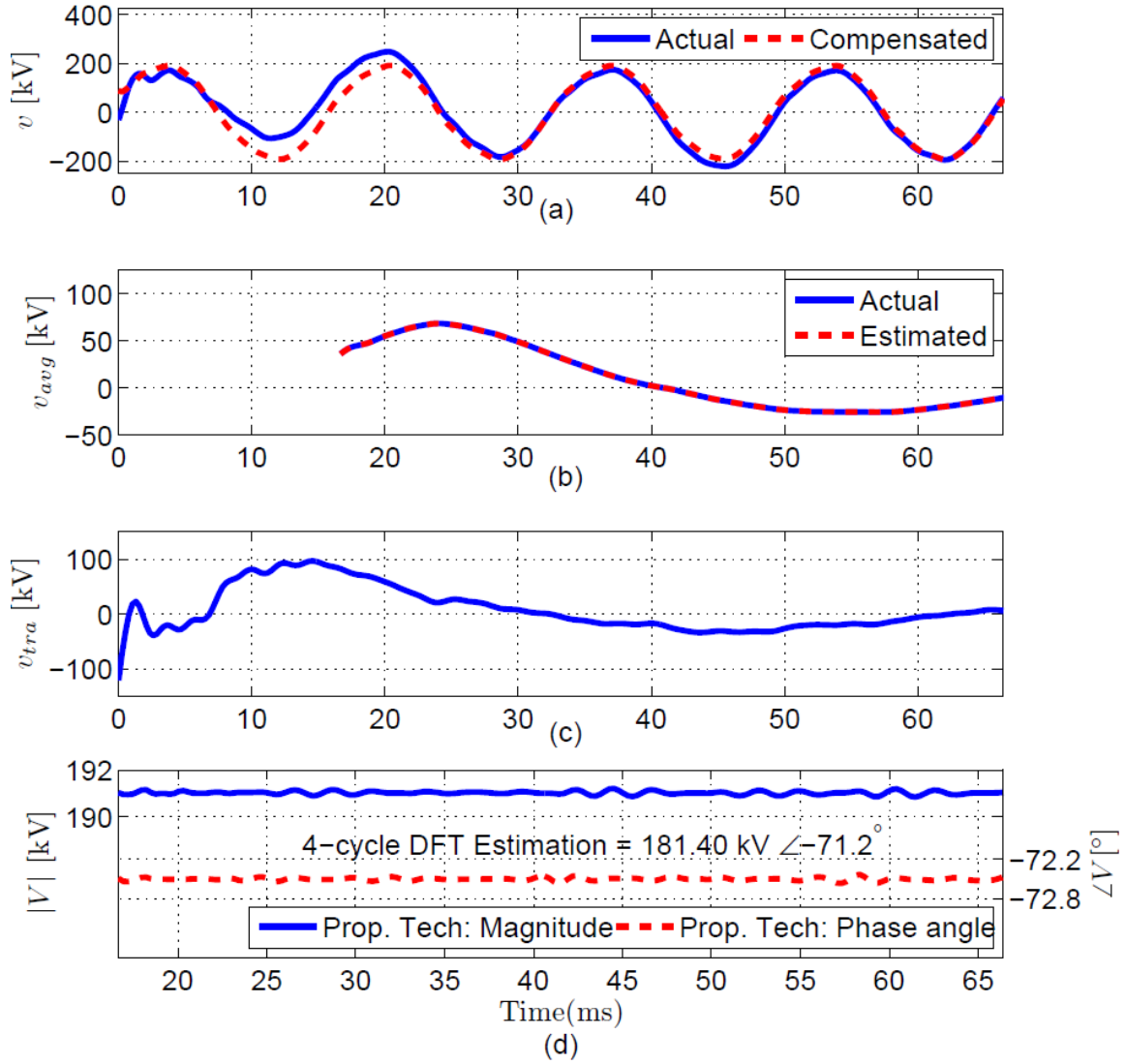


Figure 2.4: (a) Measured phase A voltage signal at sending end of Line 2 and its compensated output, (b) actual average signal and Prony estimated average signal, (c) transient signal as constructed by the proposed algorithm and (d) Phasor magnitude and angle of phase A voltage.

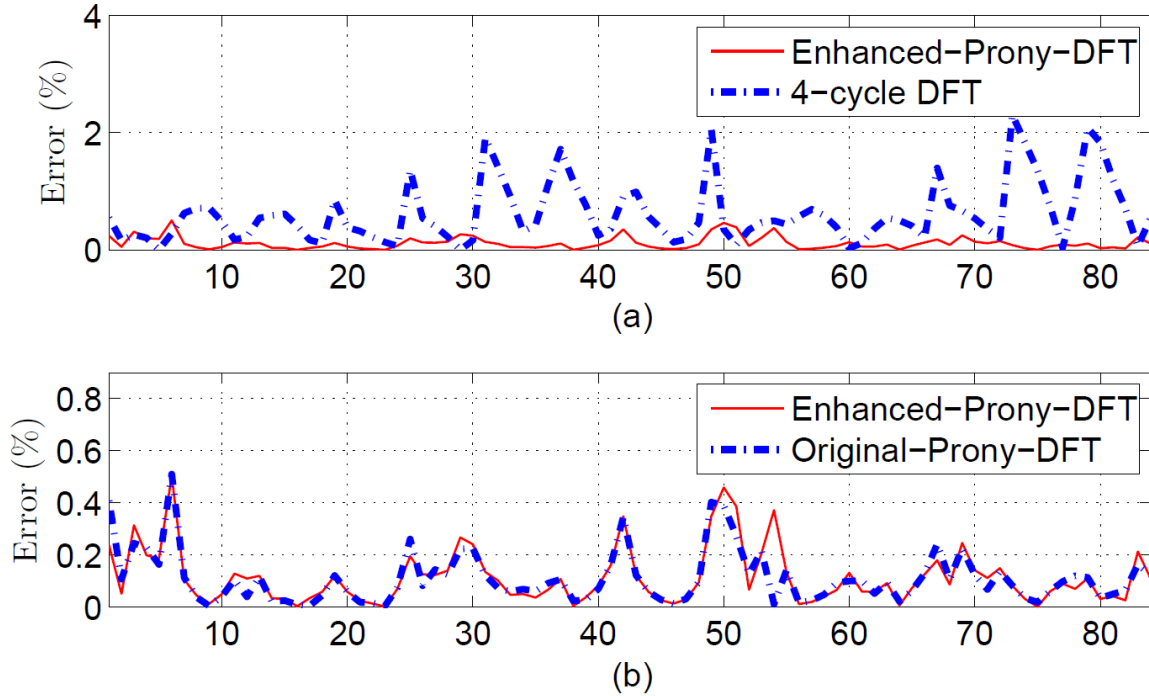


Figure 2.5: Error in fault location using (a) Enhanced-Prony-DFT and 4-cycle DFT, (b) Enhanced-Prony-DFT and Traditional-Prony-DFT

transmission line which is 350 km in this case. Figure 2.5 (a) shows that the fault location obtained from Enhanced-Prony-DFT is highly accurate as compared to that based on 4-cycle DFT. The maximum error in fault location is approximately 0.6% for Enhanced-Prony-DFT which is about 4 times less than that of 4-cycle DFT. Also, the fault location error remains below 0.5% consistently, except for 1 out of 84 cases in Enhanced-Prony-DFT, whereas fault location based on the 4-cycle DFT witnesses errors higher than 1% on numerous occasions.

Figure 2.5 (b) shows that Enhanced-Prony-DFT and Traditional-Prony-DFT have almost an identical performance at the fault location in SCCTLs. However, Traditional-Prony-DFT relies on the special averaging filter which uses more data samples than the conventional averaging filter and the availability of the high sampling frequency to achieve a high accuracy [24].

## 2.6 Fault Location: Cosine Algorithm

The Cosine algorithm and DFT are the most widely used phasor estimation algorithms. The Cosine as well as mimic-DFT algorithms are able to attenuate DDCs present in the current signal and have almost equivalent frequency response at SSFCs. In this chapter, the behavior of the fault location obtained from the phasors estimated through the Cosine filter is observed with respect to the one obtained from Traditional-Prony-DFT .

It can be observed from Figures. 2.6 and 2.7 that although the fault location obtained from Cosine algorithm was oscillatory, however, the mean position of oscillations was close to the actual fault location. Figures. 2.6 and 2.7 show that the fault location from phasors estimated by Cosine algorithm oscillates around the fault location obtained from Traditional-Prony-DFT. The ambiguity in the Cosine fault location that results from the oscillations can be reduced by averaging it over the entire fault duration after discounting the response time of the Cosine filter. Figure 2.8 shows that the error in the fault location obtained from the Cosine algorithm though is comparatively higher, still it is comparable in performance to Traditional-Prony-DFT for the system under study. Maximum error encountered using the Cosine algorithm is 0.62% while for Traditional-Prony-DFT is 0.5%.

The results obtained from the Cosine algorithm, attain significance because in order to yield accurate phasors, a window of 3-4 cycles is required by Prony-DFT which may not always be available due to SCPU operation as shown in Chapter 3 and 4. Nonetheless, the fault location obtained through Cosine filter may become erroneous, if the estimated phasors by the Cosine algorithm contains frequency in the range of 0-25Hz. The Prony-DFT on the other hand completely removes all the oscillations and yields consistent phasors, thus, resulting in the oscillation-free fault location.

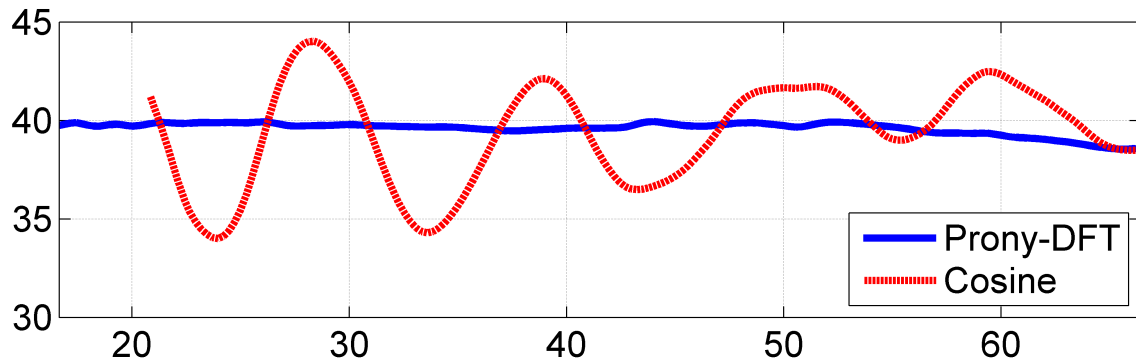
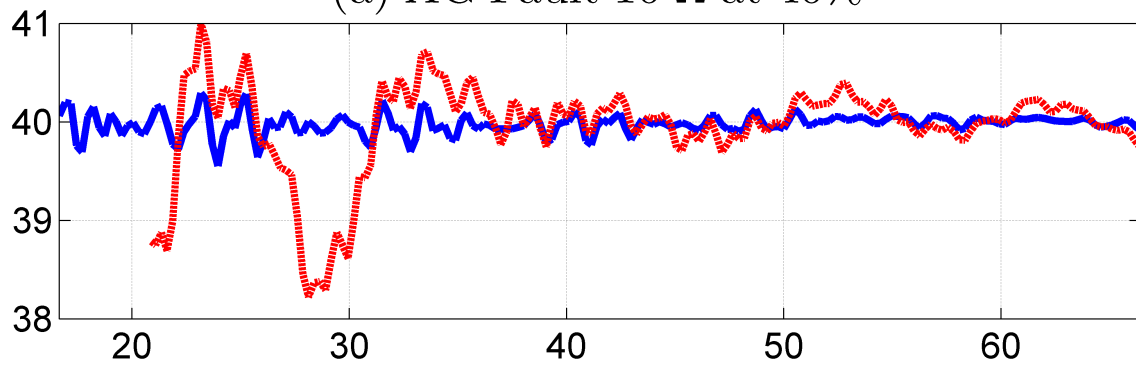
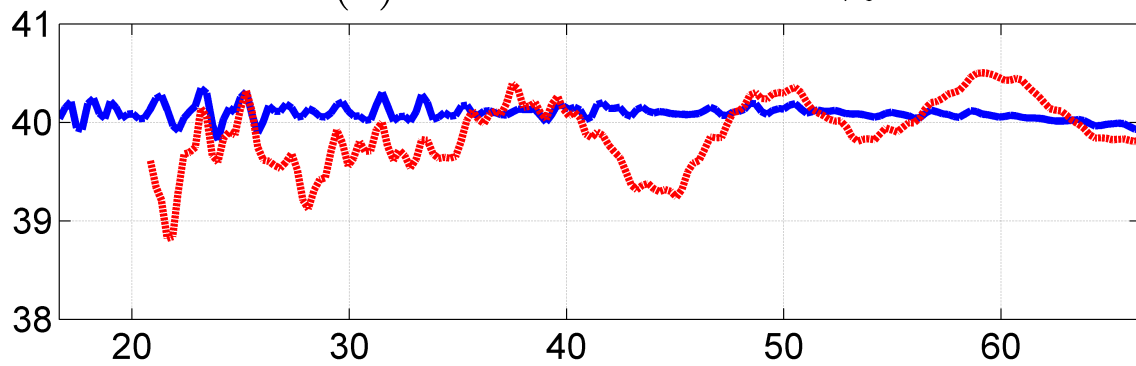
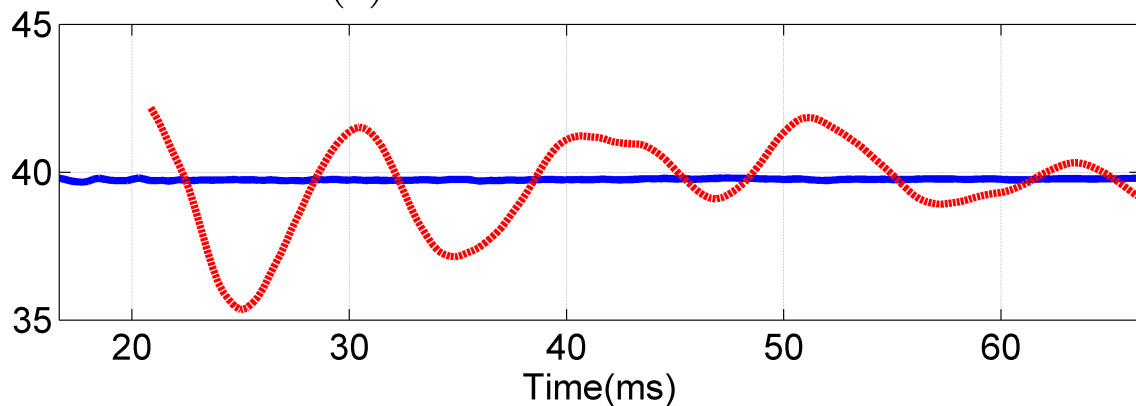
(a) AG Fault  $10 \Omega$  at 40%(b) BCG Fault  $6 \Omega$  at 40%(c) BC Fault  $6 \Omega$  at 40%(d) ABC Fault  $0 \Omega$  at 40%

Figure 2.6: Fault Location using Cosine algorithm at 40% of the line length for different fault types



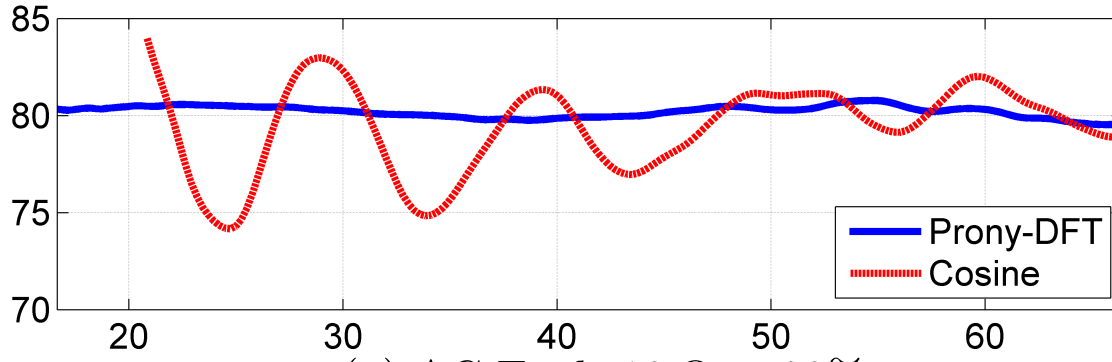
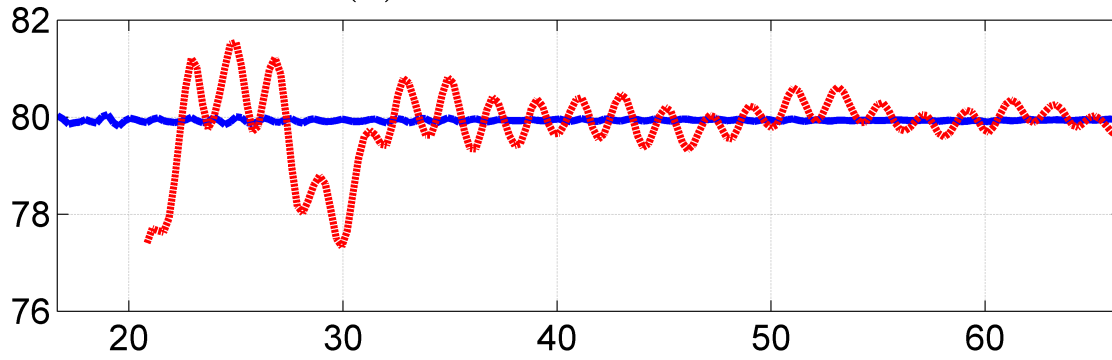
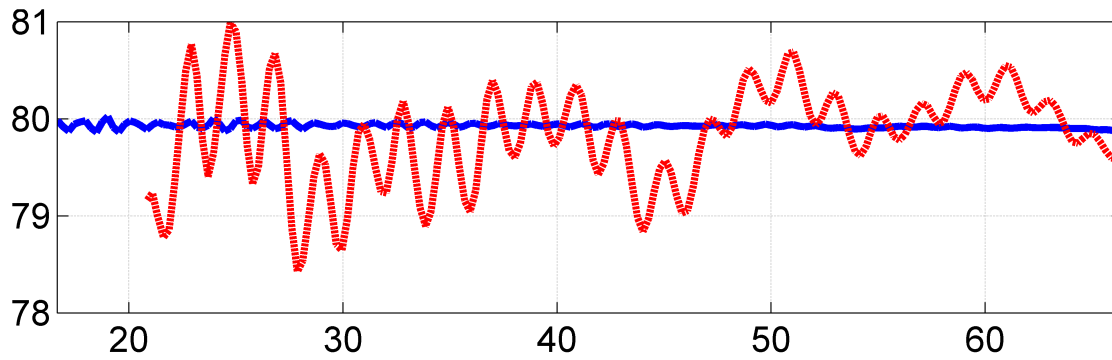
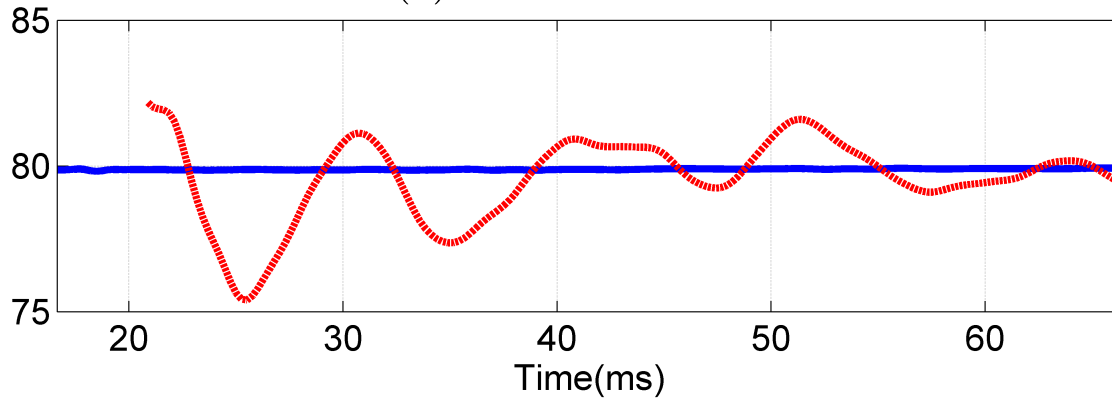
(a) AG Fault  $10 \Omega$  at 80%(b) BCG Fault  $6 \Omega$  at 80%(c) BC Fault  $6 \Omega$  at 80%(d) ABC Fault  $0 \Omega$  at 80%

Figure 2.7: Fault Location using Cosine algorithm at 80% of the line length for different fault types

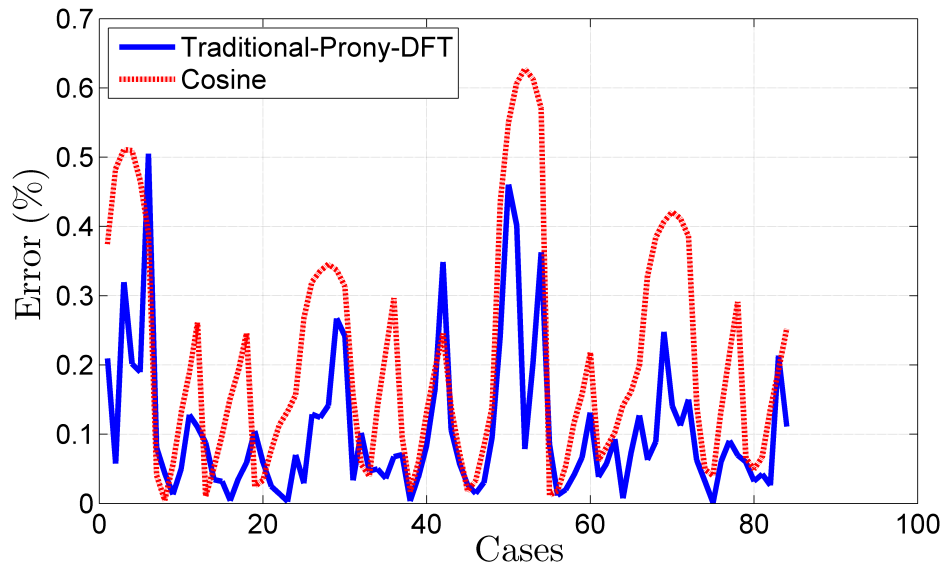


Figure 2.8: Error in fault location using Traditional-Prony-DFT and Cosine Algorithm

## 2.7 Summary

In this chapter, the Enhanced-Prony-DFT technique was proposed which estimates and removes the transients from the measured voltage and current signals of series capacitor compensated lines. The output of the proposed technique is very accurate phasors for the purpose of fault location in SCCTLs. Comprehensive fault location analysis carried out through simulations in PSCAD and Matlab has demonstrated that the proposed technique attenuates SSFCs effectively and provides very accurate phasor estimation and fault location as compared to the 4-cycle DFT. The avenue of obtaining fault location from phasors estimated by the Cosine algorithm has been explored in this chapter. It is observed that the error in averaged fault location obtained using the Cosine algorithm is slightly higher than the Prony-DFT for the particular system under study.

# Chapter 3

## Loss of Accuracy in Fault Location of SCCTLs

### 3.1 Introduction

Phasor-based fault location techniques have been applied successfully to traditional lines for fault location [12]. The fault location technique for SCCTLs proposed in [24] is focused on removing transients from measured signals. However, it is assumed that series capacitor unit (SCU) remains active in the system for the entire duration of fault, which is not the case for all internal faults. Also, the SCU is assumed to be located outside the zone lying in between the line end CVTs, thus, enabling the use of traditional fault location algorithms. However, in most of the applications of SCCTLs, SCU is located in the region lying between the end CVTs, i.e., voltage measured by CVTs contains the voltage drop across SCU. Since the accurate analytical estimation of the voltage drop across SCU is not possible due to the fault current conduction through MOV, therefore, preventing the use of traditional fault location algorithms. In [15] and [16], attempts have been made to predetermine V-I characteristics of MOV using ATP-EMTP simulations for the fundamental frequency component, but they do not take into account the variations in MOV characteristics due to the factors such as MOVs from different

manufacturers, aging of MOV and ambient temperature on MOV behavior. In [14] and [29], the authors have avoided the use of MOV model by considering the natural fault loops, thereby, avoiding any modeling inaccuracies. However, the performance of the fault location algorithms has not been evaluated for the configuration of a SCCTL, when the SCU is located near one of its ends. Moreover, the impact of spark gap and bypass switch operation has also not been considered in [14] and [29].

As a matter of fact, all of the existing publications have focused on the configuration when SCU is located in the middle of the line, however, the configuration of SCCTL when SCU is located at the end of the transmission line is being studied for the first time in this study. Both the configurations of a SCCTL, i.e., when SCU is located near the end and in the middle of a transmission line are studied in this chapter, under the influence of SCPU operation. Comparative analysis is done and presented to show the impact of SCU location on the fault location results.

In this chapter, SCPU and its functionality is described in Section 3.2. Test system and MOV sizing is described in Section 3.3. Brief description of a well-established fault location algorithm for SCCTLs [14] is presented in Section 3.4. Section 3.5 investigates the effects of SCPU operation on the results of fault location algorithm. Section 3.6 focuses on the effects of SCU location on fault location algorithm, phasor estimation errors and transients.

## **3.2 Series Capacitor Protection Unit**

To investigate the behavior of fault current in SCCTLs, first it is important to understand the operation of series capacitor protection unit (SCPU). SCPU has already been described briefly in Section 1.2, and here the details of SCPU have been discussed. In the early age of series capacitor technology, only spark-gaps were used for over-voltage protection of the series capacitors. As technology advanced, MOVs have replaced or complemented spark -gaps and newer installations are mostly equipped with MOV, spark-gap, bypass switch, and protection

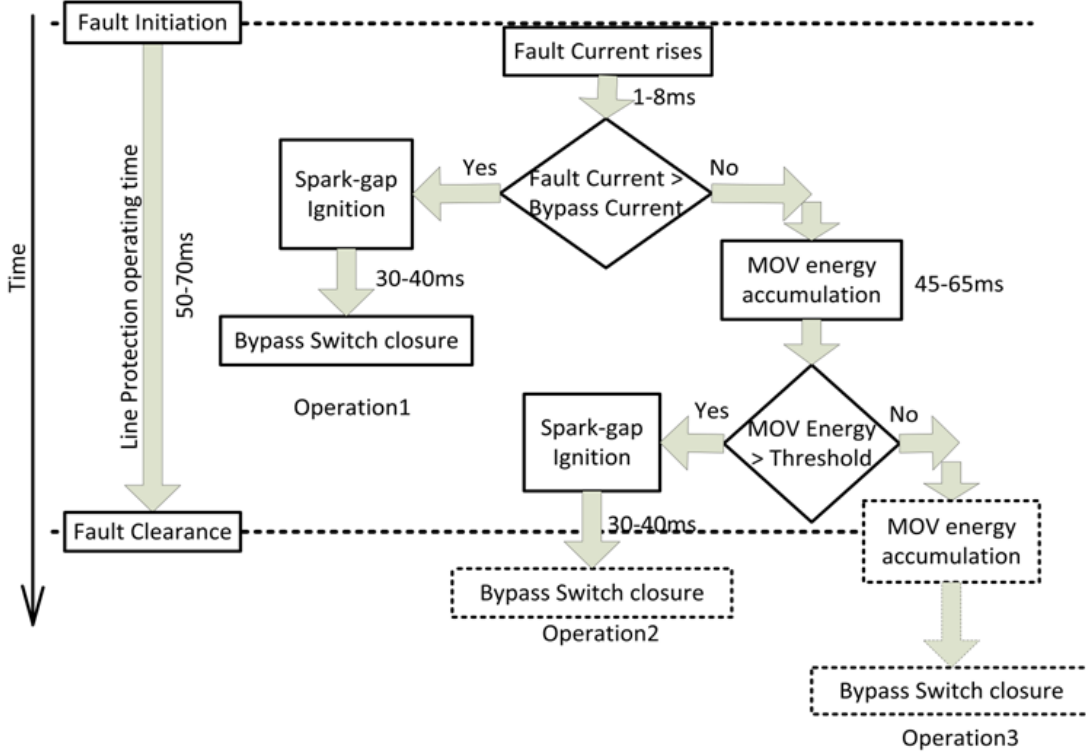


Figure 3.1: The flowchart depicting the operation of SCPU depending upon fault current level.

and control system. MOVs are preferred over spark-gaps as they enable fast and more precise bypass and re-insertion of the series capacitor [6]. SCPU scheme without spark-gap is also an option but in such schemes MOV is subjected to considerably higher duty [6]. Bypass switch is employed to protect air gap from prolonged conduction and for bypassing the capacitor and MOV unit during maintenance. Here, it is worth noting that operation of bypass switch could be a single or three-phase operation. Generally, three phase operation is applied to bypass switch while spark-gap is allowed to operate on faulted phase(s) basis for internal faults. [6]. SCPU operation can be categorized broadly into three categories as follows:

### 3.2.1 Operation 1

If very large fault current flows through SCU whose magnitude is greater than the bypass threshold of MOV, spark-gap flashes within 1 ms after high current detection saving the MOV from unnecessary heating and command is sent to close the bypass switch which operates with

a time delay of an order of two power system cycles. There is a high probability that SCU will be bypassed before the fault clearance occurs.

### **3.2.2 Operation 2**

For intermediate fault currents, when the current is unable to buildup to bypass threshold value but over-voltage occurs across SCU, MOV starts conducting and dissipating energy. If energy so dissipated reaches a preset threshold value, protection and control system of SCPU ignites the spark-gap. Fault usually gets cleared when the spark gap is still conducting. It should be emphasized here that MOV energy dissipation threshold is a design parameter and it is typically set such that MOV does not get bypassed for 3-phase close-in fault in the adjacent line for the zone one line protection operating time.

### **3.2.3 Operation 3**

When the fault current is comparatively low, neither MOV current nor energy reaches the threshold value during fault interval. MOV keeps conducting until the fault is cleared by the opening of line circuit breakers.

It can be observed that the behavior of different protection components is greatly governed by the amplitude of fault current as also depicted by the flowchart in Figure 3.1. At the same time, operation of each SCPU element alters the state of power system, thereby influencing the magnitude of fault current as well as introducing the transient conditions. Thus, it can be concluded that the operation of series capacitor protection unit and the magnitude of fault current are interdependent variables.

## **3.3 Test System and MOV Sizing**

It becomes easier to understand and observe the SCPU operation and its effects on fault location if it is demonstrated with simulated examples. Therefore, a test system is defined in the

following section and the procedure to size MOV for the test system is presented thereafter.

### 3.3.1 Test System

A 500 kV, 350 km SCCTL is considered in PSCAD as a test case in this chapter. As shown in Figure 3.2 (a), 70% series compensation which corresponds to an equivalent capacitance of  $29.11\mu\text{F}$  ( $91.1\Omega$ ) is assumed at the middle of the line for System 1 whereas for System 2 it is located adjacent to Bus1 (see Figure 3.2 (b)). The line positive and zero sequence impedances are  $Z_{L1} = (0.0155 + j0.3719)\Omega$  per km,  $Z_{L0} = (0.3546 + j1.0670)\Omega$  per km, respectively, and the line positive and zero sequence admittances are  $Y_{L1} = (0 + j4.4099 \times 10^{-6})\text{U}$  per km,  $Y_{L0} = (0 + j2.7844 \times 10^{-6})\text{U}$  per km, respectively. Positive and zero sequence impedances for sending end source are  $Z_{S1} = (1 + j15)\Omega$ ,  $Z_{S0} = (2.4 + j25)\Omega$  respectively. Positive and zero sequence impedances for receiving end source are  $Z_{R1} = (1.2 + j18)\Omega$ ,  $Z_{R0} = (2.6 + j26.5)\Omega$ , respectively. Load angle is  $30^\circ$  with receiving end source voltage lagging.

### 3.3.2 MOV Sizing

Rated current of 2000A, equivalent of (1750MVA), is considered for sizing SCPU. MOV rating after considering an overload factor of 1.5 is calculated as  $273\text{kV}$  (i.e.,  $1.5 \times 2000\text{A} \times 91.1\Omega$ ). MOV model of ASEA XAP-A, which is used in most of prior studies, is used in this chapter. The voltage at intersection of MOV and series capacitor characteristics ( $V_{PK} - I$ ) is the peak protective level voltage ( $V_{PK}$ ), i.e., 530kV in this case.  $V_{PK}$  signifies the instantaneous peak value of voltage across SCU at which MOV starts conducting, thereby limiting the voltage across SCU. Knowing  $V_{PK}$ , the protective level current ( $I_{PR}$ ) is calculated from

$$I_{PR} = \frac{V_{PK}}{\sqrt{2}X_c} = \frac{530}{1.414 \times 91.1} = 4.113 \text{ kA} \quad (3.1)$$

where  $I_{PR}$  is the RMS value of the minimum amount of the current through SCU that would lead to MOV conduction. For protecting MOV against large fault currents, SCPU is set to

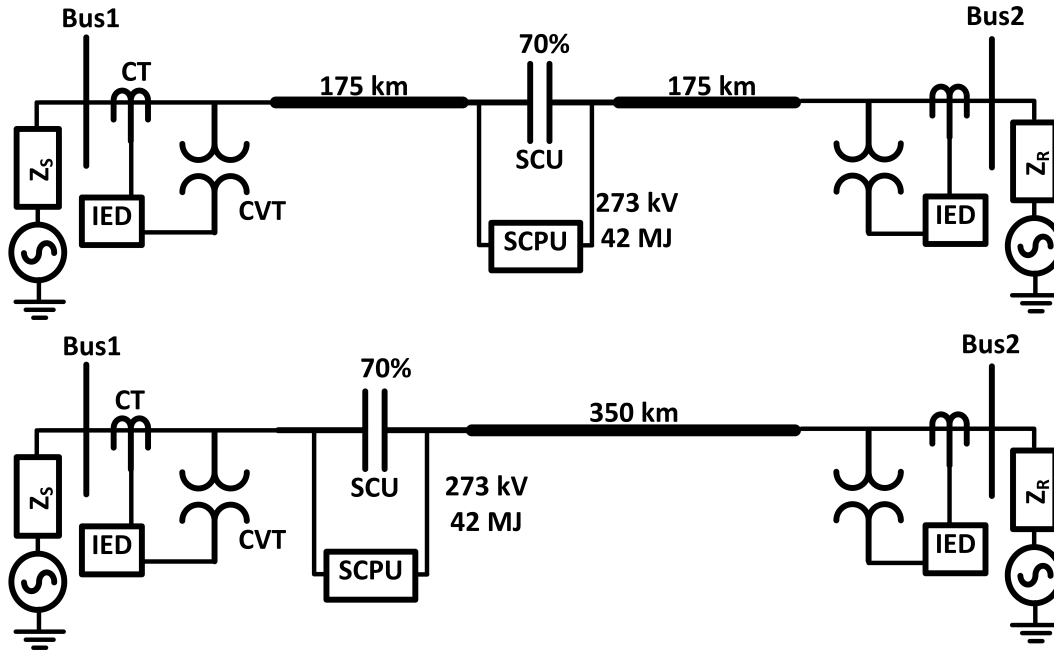


Figure 3.2: (a) System 1 with SCU in the middle (b) System 2 with SCU adjacent to Bus1

immediately bypass the MOV through spark-gap if the MOV instantaneous current is above the bypass current ( $I_{BP}$ ) where  $I_{BP} = K \times I_{PR}$ .  $K$  is a design parameter and is typically set to bypass the MOV for most of the solid internal faults. A typical value of 2.17 is used for  $K$  as per [30] which results in  $I_{BP} = 8.925$  kA for the test system under study.

### 3.4 Fault Location Algorithm

A well-known fault location algorithm for series compensated lines has been proposed in [14]. In the proposed fault location algorithm, the authors have avoided the use of MOV model, therefore, making the consideration of natural fault loops inevitable which further necessitates the usage of zero-sequence parameters of the transmission lines for ground faults [14]. Since the zero-sequence parameters of the transmission lines are dependent on the weather and geographical factors, it may introduce ambiguity in the fault location results as discussed in the Chapter 4.

Brief description of the algorithm is presented here for understanding the underlying prin-



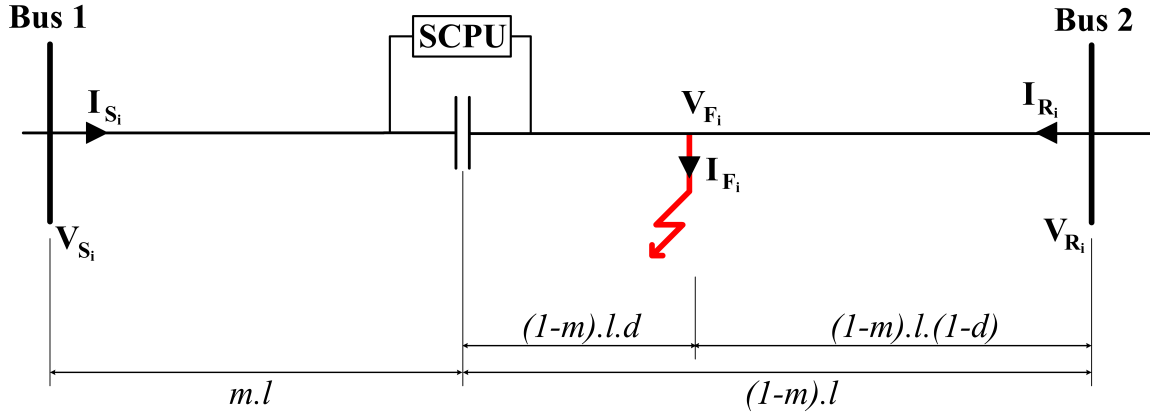


Figure 3.3: Schematic diagram showing the fault scenario in a SCCTL.

inciple. It should be noted that in this thesis, equations are written only for the faults lying in the section of the transmission line in between SCU and receiving end (Bus2) called Subroutine 1 for System 1 as shown in Figure3.2. For the faults lying in the section of transmission line between sending end bus (Bus1) and SCU, equations can be written analogously, called Subroutine 2.

In the proposed technique, the authors have derived the expressions for sequence components of fault current ( $I_{F_i}$ ) and fault voltage ( $V_{F_i}$ ) as the functions of fault location. Equations (3.2) and (3.3) represent the fault sequence current and voltage, respectively, for any fault occurring at per unit distance ( $d$ ) as shown in Figure 3.3.

$$I_{F_i} = \frac{I_{S_i} \cosh(\gamma_i l m) - \frac{V_{S_i}}{Z_{c_i}} \sinh(\gamma_i l m) + I_{R_i} \cosh(\gamma_i l (1 - m)) - \frac{V_{R_i}}{Z_{c_i}} \sinh(\gamma_i l (1 - m))}{\cosh(\gamma_i l (1 - m) d)} \quad (3.2)$$

$$V_{F_i} = V_{R_i} \cosh(\gamma_i l (1 - d)(1 - m)) - Z_{c_i} I_{R_i} \sinh(\gamma_i l (1 - d)(1 - m)) \quad (3.3)$$

where,  $i$ : 0, 1 and 2;  $V_{S_i}$  and  $I_{S_i}$  are the sending end voltage and current, respectively;  $V_{R_i}$  and  $I_{R_i}$  are the receiving end voltage and current, respectively;  $Z_{c_i}$  is the characteristic impedance of the line for  $i^{th}$  sequence;  $\gamma_i$  is the propagation constant of the line for  $i^{th}$  sequence;  $l$  is the length of the transmission line,  $d$  is the p.u. distance of the fault from SCU;  $m$  is the p.u. distance of

Table 3.1: Coefficients for finding Total Fault Current

Fault Type	$a_1$	$a_2$	$a_0$
AG	0	3	0
BCG	$\alpha^2 - \alpha$	$\alpha - \alpha^2$	0
BC	0	$\alpha - \alpha^2$	0
ABC	$1 - \alpha^2$	0	0
$\alpha = 1 \angle 120^\circ$			

Table 3.2: Coefficients for finding Fault-loop Voltage

Fault Type	$af_1$	$af_2$	$af_0$
AG	1	1	1
BCG	$\alpha^2 - \alpha$	$\alpha - \alpha^2$	0
BC	$\alpha^2 - \alpha$	$\alpha - \alpha^2$	0
ABC	$1 - \alpha^2$	0	0
$\alpha = 1 \angle 120^\circ$			

location of SCU from the sending end bus. Equations (3.2) and (3.3), therefore, represent the analytical calculated sequence fault current and sequence fault voltage using distributed model of transmission line, sending end sequence current ( $I_{S_i}$ ), receiving end sequence voltage ( $V_{R_i}$ ) and sequence current ( $I_{R_i}$ ). Now, using the identified fault type, (3.2) and (3.3), the analytical expression for the total fault current and fault loop voltage can be obtained as shown in (3.4) and (3.5).

$$I_F = a_0 I_{F_0} + a_1 I_{F_1} + a_2 I_{F_2} \quad (3.4)$$

$$V_F = af_0 V_{F_0} + af_1 V_{F_1} + af_2 V_{F_2} \quad (3.5)$$

where,  $a_i$  and  $af_i$  are the coefficients for calculating total fault current and fault loop voltage, respectively, and attain different values depending upon the fault type as represented in Tables (3.1) and (3.2).

After obtaining fault-loop voltage ( $V_F$ ) and fault current ( $I_F$ ), the fault loop model as given in (3.6) is solved under the constraint that the faults in a transmission lines are always resistive in nature i.e.,  $R_F$  is a pure real number.

$$V_F(d) - R I_F(d) = 0 \quad (3.6)$$

The methodology for solving (3.6) as presented in [14] is to separate it into real and imaginary parts and solve for fault resistance ( $R_F$ ) and fault location ( $d$ ) as shown in (3.7),

$$\begin{aligned} \operatorname{Re}(V_F(d)) - R_F \operatorname{Re}(I_F(d)) &= 0 \\ \operatorname{Im}(V_F(d)) - R_F \operatorname{Im}(I_F(d)) &= 0 \end{aligned} \quad (3.7)$$

Now, the other area where the authors have focused their attention is how to identify the faulted section of the line as any fault event can be thought of lying in the region between Bus1 and SCU or between SCU and Bus2. It is proposed in [14] that for any particular fault scenario both of the subroutines are run, therefore, yielding two fault location results. In order to find the correct fault location, firstly, the subroutine yielding results lying outside the section range or the negative value of fault location is rejected. Thereafter, the equivalent impedance of the SCU is calculated using the voltage drop across SCU and the fault current through SCU for both the subroutines. The equivalent impedance of SCU corresponding to the valid subroutine has to be R-C in nature due to the presence of MOV and series capacitor in the transmission line. Also, the degree of capacitive compensation should be less than that at the steady state value because at steady state SCU is purely capacitive in nature [14]. Set of equations in (3.7) when rearranged results in (3.8), which shows that the proposed fault location algorithm actually involves argument comparison of analytically obtained fault voltage ( $V_F$ ) and fault current ( $I_F$ ). Therefore, the proposed fault location algorithm in [14] is essentially very similar

to the one proposed in [29] as far as the working principle is concerned.

$$\begin{aligned}\frac{\text{Im}(V_F(d))}{\text{Re}(V_F(d))} &= \frac{\text{Im}(I_F(d))}{\text{Re}(I_F(d))} \\ \tan^{-1}\left(\frac{\text{Im}(V_F(d))}{\text{Re}(V_F(d))}\right) &= \tan^{-1}\left(\frac{\text{Im}(I_F(d))}{\text{Re}(I_F(d))}\right) \\ \angle V_F(d) &= \angle I_F(d)\end{aligned}\tag{3.8}$$

It can be concluded here that the proposed fault location algorithm for SCCTLs in [14] estimates the arguments of fault voltage ( $V_F$ ) and fault current ( $I_F$ ) as the function of fault location ( $d$ ). The value of  $d$  for which the arguments of both the analytically estimated quantities are the closest to each other is considered as fault location result.

### 3.5 Effects of Operation of SCPU on Fault Location

As discussed in Section II, the state of system can change at different points of time depending upon the level of fault current, energy dissipation threshold, operating time delay of bypass switch and line circuit breakers. Thus, it becomes imperative to follow the time line of occurrence of the state changes and correlate them with the fault location results. This has been elaborated in the following examples.

#### 3.5.1 Example 1

Case under consideration is a BC solid fault at 175 km from Bus1 or 50% of line length (i.e., just right-side of SCU) in System1. Placing the events in chronological order of occurrence, the following is obtained: 1-Fault initiation at 0 ms, 2-bypass threshold reached (phase B), 3-spark-gap ignition, 4-command for SCU bypass sent at 10.15 ms, 5-bypass threshold reached (phase C), 6-spark-gap ignition, 7-command for SCU bypass sent at 10.93 ms, 8-three phase SCU bypass at 43.48 ms, and 9-fault clearance at 66.66 ms. This case belongs to the Operation1 category of SCPU.

It is apparent that among all the time intervals between two successive events, the time intervals greater than the response time of the Cosine filter (i.e., 20.83 ms) are: 1- between spark-gap ignition for phase C and three-phase SCU bypass (10.93ms-43.48ms) 2- three-phase SCU bypass and fault clearance (43.48ms-66.66ms). Therefore, the steady state fault location results, as represented by a solid line in the Figure3.5(a) will be yielded in the above identified intervals after accounting for filter response time. It can be observed that steady state results are less fluctuating and more accurate as compared to the transient results. Averaging the steady state results over the total steady state time interval would yield the better fault location result.

### 3.5.2 Example 2

Case being considered is a BCG fault at 245 km from Bus1 or at 70% line length with fault resistance of 6 ohms. This case falls under the category of Operation2 of SCPU. Current does not cross the bypass current threshold but spark-gap gets ignited after the MOV energy crosses the threshold value. Events, in order of occurrence are given below: 1-Fault initiation at 0 ms, 2-MOV energy threshold reached (phase B), 3-spark-gap ignition, 4-command for SCU bypass sent at 62.24 ms, 5-MOV energy threshold reached (phase C), 6-spark-gap ignition, 7-command for SCU bypass sent at 62.76 ms and 8-fault clearance at 66.66 ms.

The time interval between fault initiation and spark-gap ignition (Phase B) would give steady state results before slipping into a transient state as shown by the solid line in Figure3.5(b). It is observed that after spark-gap gets ignited at 62.24 ms, the fault location results depicted by a dashed line show a sudden departure from steady-state values which, if considered, could lead to an erroneous fault location.

### 3.5.3 Example 3

Now let us consider a solid AG fault at 315 km from Bus 1 or at 90 % of the line length. As evident from event occurrence and their time frame, this case falls under the Operation3 category. Current as well as MOV energy fail to reach the threshold for spark-gap ignition,

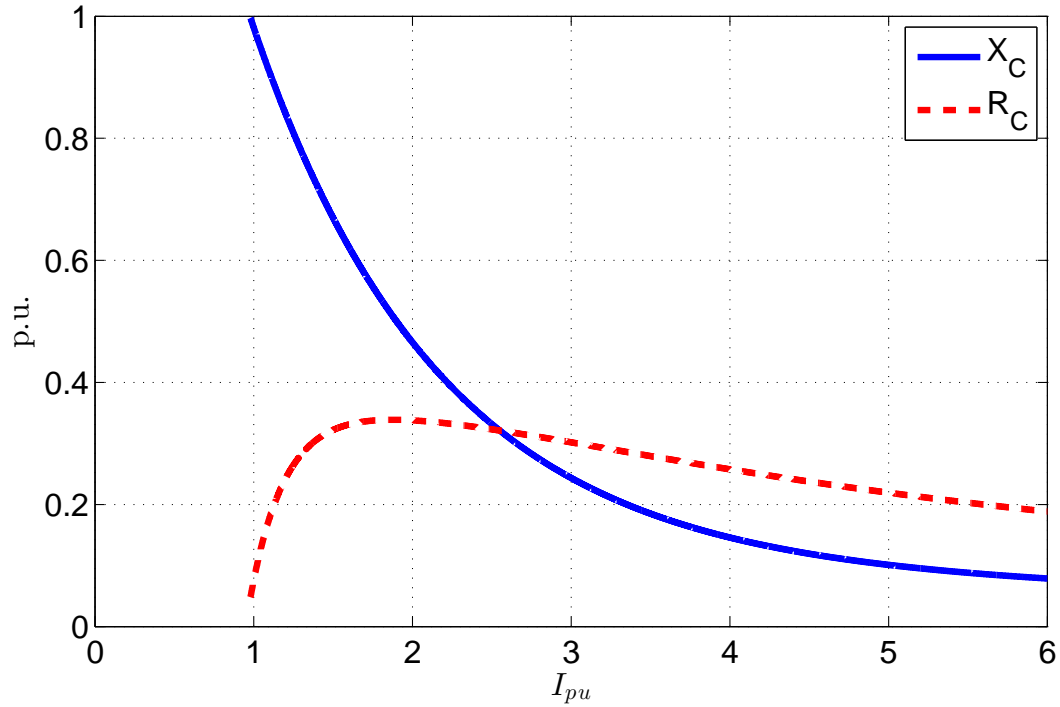


Figure 3.4: Equivalent impedance of the parallel combination of MOV and series capacitor with respect to the fault current.

leading directly to a fault isolation. 1-Fault initiation at 0 ms, 2-fault clearance at 66.66 ms. The entire fault duration interval yields steady-state but oscillatory results as depicted in Figure 3.5(c). Therefore, averaging them over the entire fault duration interval would result in the least uncertainty in the fault location.

Effects of different sets of SCPU behaviors on fault location have been studied in this section. It can be concluded here that with proper identification of SCPU operating sequence along with its time line, better fault location results can be achieved.

### 3.6 Effects of SCU Location on Fault Location

From power transfer capability perspective, the location of SCU in the middle of transmission line is better but from installation and operation perspective, installing SCU at the line ends is more practical and economical. In the process of investigating the performance of the fault

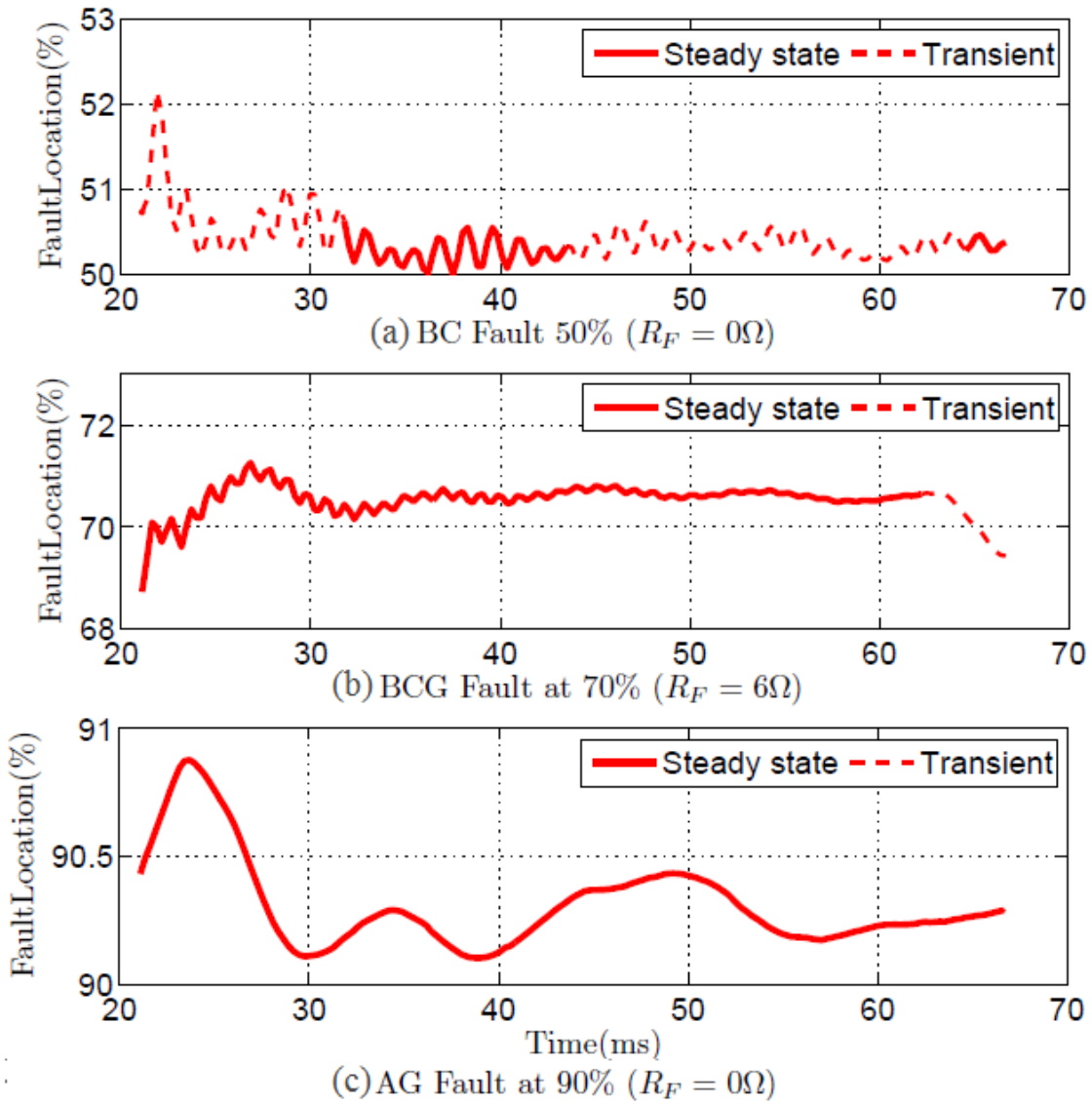


Figure 3.5: Fault Location (a) B-C Fault at 50% (b) B-C-G Fault at 70% (c) A-G Fault at 90% for System 1

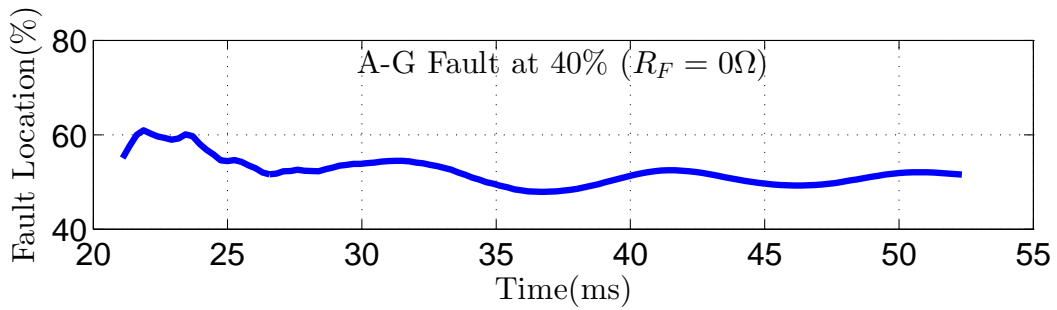


Figure 3.6: Fault Location for A-G Fault at 40% for System 2

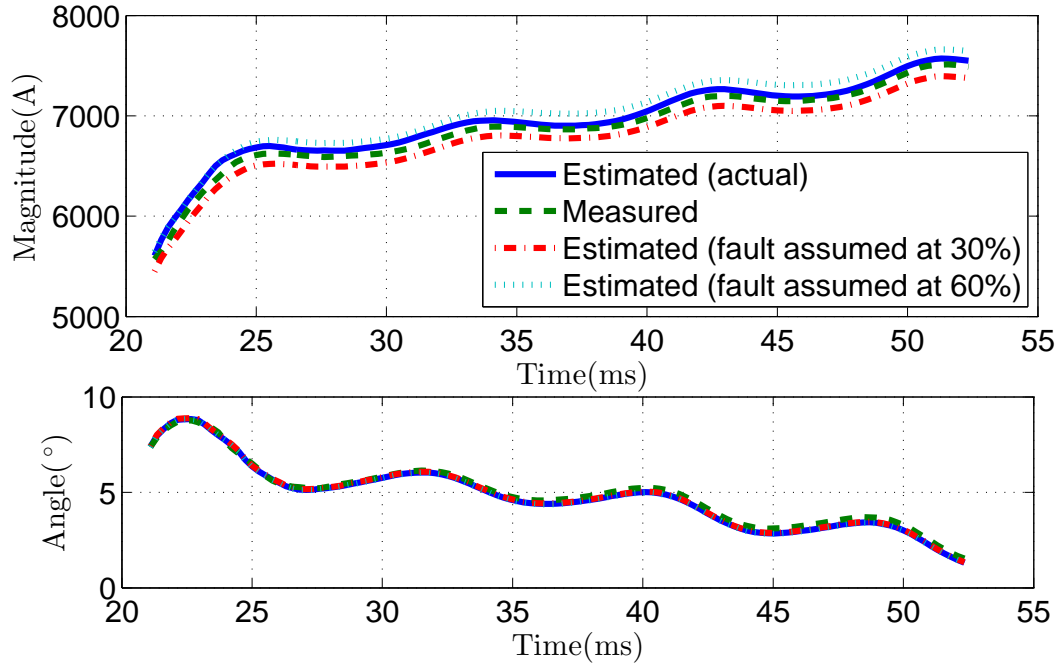


Figure 3.7: Phasor estimation of fault current for a given fault scenario of AG fault for different values of fault location ( $d$ )

location proposed in [14], for the configuration where the SCU is installed at the line end, it was discovered that the fault current magnitude and angle remains almost constant as the fault location is changed within 30% to 50% region. This happens due to the non-linear behavior of the MOV. Figure 3.4 shows the variation of the impedance of parallel combination of series capacitor and MOV, with respect to the per unit fault current. The reactive and resistive part of the equivalent impedance are denoted by  $X_C$  and  $R_C$ , respectively. The closer faults tend to have higher fault currents while SCU presents smaller capacitive impedance, therefore resulting in lower line compensation and thereby lowering the fault current while the farther faults tend to have lower fault currents while SCU presents higher capacitive impedance as shown in Figure 3.4, resulting in higher line compensation and thereby increasing the fault current.

In order to justify the above statement, consider the case of a solid A-G fault at 140 km from Bus1 or 40% of the line length in System 2. In this case, the spark-gap gets ignited after the energy dissipation in MOV of phase A crosses the threshold value at 52.34 ms after the fault incidence time. Results yielded by the fault location algorithm before it slips into a transient



behavior due to the spark-gap conduction, are shown in Figure3.6. Note the significant error and oscillatory behavior of the fault location.

The basic assumption in [14] that all the faults are purely resistive (i.e., imaginary part of  $(R_F) = 0$ ) in nature essentially implies that the arguments of  $V_F$  and  $I_F$  are equal as shown in 3.8. Therefore, the proposed way of solving (3.6) for  $d$  and  $R_F$  by separating (3.6) into real and imaginary parts is analogous of equating the analytically obtained arguments of  $V_F$  and  $I_F$  as obtained by (3.4) and (3.5). As regards to the magnitudes, the magnitude of  $V_F$  is obtained by multiplying the magnitude of  $I_F$  by a scaling factor  $R_F$ . So, understanding the behavior of (3.4) and (3.4) under the influence of transients and non-linear characteristics is necessary for analyzing the fault location algorithm.

It can be observed from the Figure3.7 that magnitude and in particular argument of  $I_F$  does not undergo a considerable change, when value of  $d$  is varied from 30% to 60% for the same fault at 40%. Therefore, (3.4) is not sensitive to the deviations in  $d$ . In other words, for a given set of measurements of  $V_R$ ,  $I_S$  and  $I_R$ , significant deviations in  $d$  do not affect the magnitude and argument of  $I_F$ . Now let us examine (3.5) which essentially represents the analytical estimation of  $V_F$  using the Bus2 measurements, i.e.,  $V_R$  and  $I_R$  as mentioned earlier in Section IV. As the fault is moved near to the SCU, two phenomena occur simultaneously: 1- MOV starts conducting for longer time intervals, thus making system more non-linear. 2- Elevation of error in phasor estimation of  $V_R$  and  $I_R$  due to increased non-linearity of the system. Therefore, the process of finding  $V_F$  using (3.5) now involves estimating highly non-linear  $V_F$  using the erroneous phasors of  $V_R$  and  $I_R$ . Figure3.8 shows the measured fault voltage and analytically estimated fault voltage phasor angle using (3.5). Note the eloquent error incurred in angle estimation as expected.

Now, the fault location algorithm compares the insensitive argument of  $I_F$  to the erroneous argument of  $V_F$  as calculated by (3.4) and (3.5) to determine the fault location. So it has been demonstrated that the above fault location technique is highly susceptible to transients, non-linear characteristics of the system or any other condition which produces error in phasor

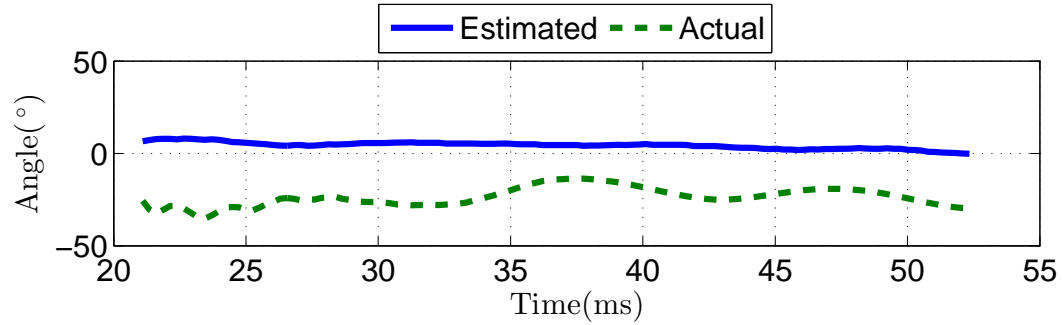


Figure 3.8: Argument of fault voltage for A-G Fault at 40%

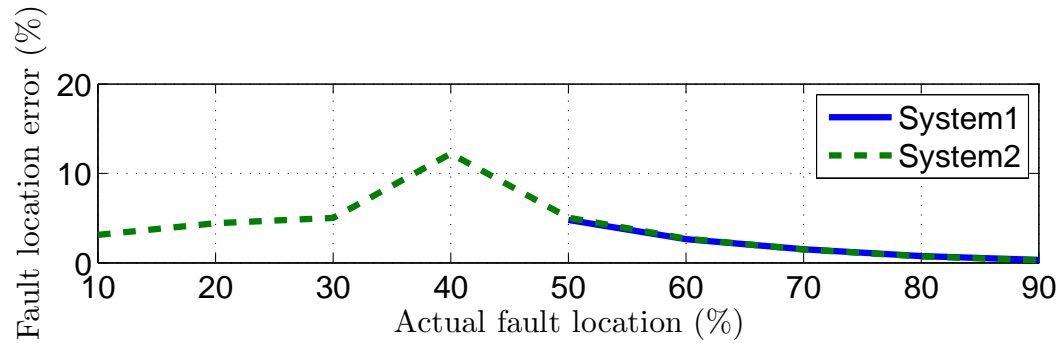


Figure 3.9: Comparison of fault location error in System 1 and System2

estimation. Given technique remains accurate as long as the estimated phasors remain accurate.

Though System 1 configuration seems mathematically more complicated and general, System 2 configuration is the one where possibility of encountering severe faults and MOV interaction with the system is greater. In System 1, all of the faults lie at 50% or at higher length in the fault loop that contains SCU, thereby reducing the effects of CVT transients on the phasor estimation. Moreover, there is always some amount of line impedance available to compensate for the capacitive and non-linear behavior of MOV. In this way, the severity of fault is much less in System 1 when compared to System 2. Above statements are further justified by the fault location results shown in Figure3.9. Seeing that less than 50% faults are not possible for System 1 configuration, Figure3.9 shows only 50-90 % faults as depicted by solid line. It can be observed that as the fault moves towards SCU from Bus2, the error in fault location keeps on increasing and for System 2 the results become highly inaccurate because of the above mentioned reasons as represented by dashed line in Figure3.9. It should be noted here that the

fault location results shown in Figure 3.9 have been obtained by averaging steady state fault location values over the total steady state fault time interval. Thus, it can be concluded that the worst possible conditions for fault location algorithm for SCCTLs in terms of accuracy would arise when SCU is located near the source and fault occurs at less than 50% of the line length from SCU. Also any major changes in SCPU element thresholds and delays may result in a different operation category of SCPU and consequently may change the fault location results. It however, does not affect the inference of the study presented.

### **3.7 Summary**

This chapter has been able to provide a practical insight into the functionality of SCPU and how the operation of SCPU and fault current magnitude are interdependent events. Various issues encountered by a fault location algorithm of SCCTLs such as operation of SCPU and location of SCU in a line have been comprehensively studied. It has been demonstrated that errors in fault location can be minimized by knowing the operating sequence of SCPU elements. It has been observed that the most promising fault location algorithm for SCCTLs is susceptible to errors in phasor estimation, which are more severe when the SCU is located near the line ends. In conclusion, we can infer that fault location in SCCTLs needs to be approached as a comprehensive task considering the aforementioned factors.

# Chapter 4

## Complimentary Fault Location Algorithm for Series Compensated Lines

### 4.1 Introduction

As discussed in Chapter 1, the non-linear characteristics of MOV force the phasor-based fault location algorithms to make a choice between use of an imprecise MOV model or the utilization of zero-sequence parameters of the transmission line. Exclusion of one option comes with the compulsion of using the other one. The approach presented in [15] and [16] is aimed at the predetermination of MOV V-I characteristics for all the fault current levels by using ATP-EMTP model of MOV. This technique has advantage of avoiding the usage of zero-sequence parameters when SCU lies at one end of the line (i.e., the case in majority of the configurations), but predetermination of MOV behavior through an approximate model may not be true in all conditions such as different ambient temperature and MOV pre-condition in case of reclosing and aging.

In [14] and [29], authors have avoided the use of MOV model in fault location algorithm. Therefore consideration of natural fault loops becomes a necessity, forcing the usage of zero-sequence parameters of the transmission lines which are highly dependent on the soil resistivity.

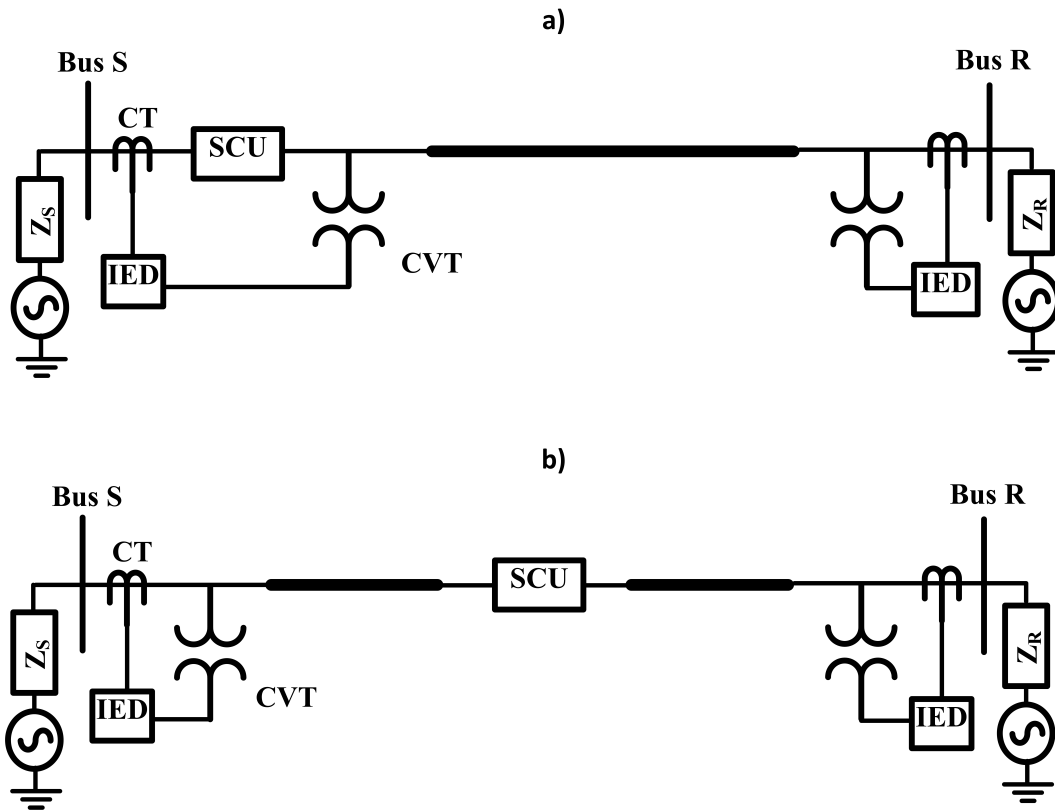


Figure 4.1: Location of SCU with respect to SCU in a SCCTL with SCU lying (a) outside the zone between CTVs (System A) (b) inside the zone between CTVs (System B)

The soil resistivity varies widely depending upon the soil contents, the weather conditions such as temperature, precipitation and in particular moisture content of the soil. Thus, accurate estimation of zero-sequence parameters is not possible. Also such algorithms are essentially a comparison of arguments of fault loop current and voltage, therefore the equation for finding fault becomes a non linear equation. Also it has been shown by the author in the previous chapter that such techniques become sensitive to measurement and phasor estimation errors under specific fault conditions [25].

At the incidence of a fault in a SCCTL, MOV starts conducting to limit the over-voltage caused by the high fault currents across SCU. In this process, it starts dissipating energy which may result in the overheating of MOV and causing MOV to get bypassed before the fault gets cleared through ignition of spark gap or bypass switch operation. MOV may also get bypassed if MOV is reinserted onto the fault at the time of the reclosing. Such bypassing operation of MOV, makes it possible to estimate the voltage on the line side of SCU, accurately. Therefore, a new fault location technique is presented in this chapter, for the fault scenarios where MOVs in the faulted phases get bypassed before the clearance of the fault. The significance of the proposed technique lies in the fact that it obtains the fault location by very limited use of the zero-sequence parameters of the transmission line. It can be indicated here that the proposed technique complements the existing fault location techniques to enhance the accuracy, if MOV gets bypassed before the interruption of the fault by the line circuit breakers.

In this chapter, Section 4.2 describes the configurations and functionality of SCPU. The proposed fault location technique is described in Section 4.3. Test system is described in 4.4. Evaluation and validation of the proposed technique is presented in Section 4.5.

## **4.2 SCPU Operation: MOV Bypassing**

As described in Section 1.2, SCPU can be broadly categorized into three categories: 1- spark gap only configuration, 2- Gapless or MOV only scheme, 3- MOV-spark gap configuration.

Spark gap only configuration has been used in the older installations of SCPU. During the fault event if the voltage across SCU exceeds the protective level, spark gap operates immediately. In the modern applications, the MOV-spark gap configuration is utilized where very high fault current levels are expected or MOV with abundantly high energy capacity is unavailable. Therefore, for MOV-spark gap configuration the bypassing of MOV before the isolation of the fault by line circuit breakers, is a fairly probable event. Bypassing of MOV is also very likely in the event of reinsertion of SCU onto a fault in gapless scheme during reclosing. One key point that can be brought forward here is that this bypassing of MOV can be effected on faulted phase basis or on a three phase basis depending upon the operating philosophy of the utility.

As stated earlier, the proposed technique aims to analytically estimate the voltage drop across SCU in the case of MOV bypass, therefore, making it applicable to all the SCPU configurations. The proposed technique can also be applied to spark gap only scheme as the proposed technique considers the presence of series capacitors in the non-faulted phases.

### 4.3 Proposed Fault Location

In the event of a fault, if a SCPU is designed to allow non-three-phase bypass of the series capacitor and MOV through spark gap or by-pass switch, only the MOVs located in the faulted phase(s) conduct, while MOVs in the healthy phase(s) remain non-conducting. In other words, series capacitors are exclusively responsible for the current conduction in the healthy phases, thus, making the accurate analytical estimation of voltage drop across series capacitors possible. For faulted phases however, MOV along with series capacitor conducts the fault current. Due to the fact that the impedance of MOV is a time varying non-linear quantity, accurate estimation of voltage drop across SCU cannot be obtained in the faulted phase. Consequently, the positive-sequence voltage obtained at the fault side of SCU becomes inaccurate which prevents the successful application of traditional fault location algorithms to SCCTLs.

As it has already been discussed in the text above that a MOV gets bypassed due to ex-

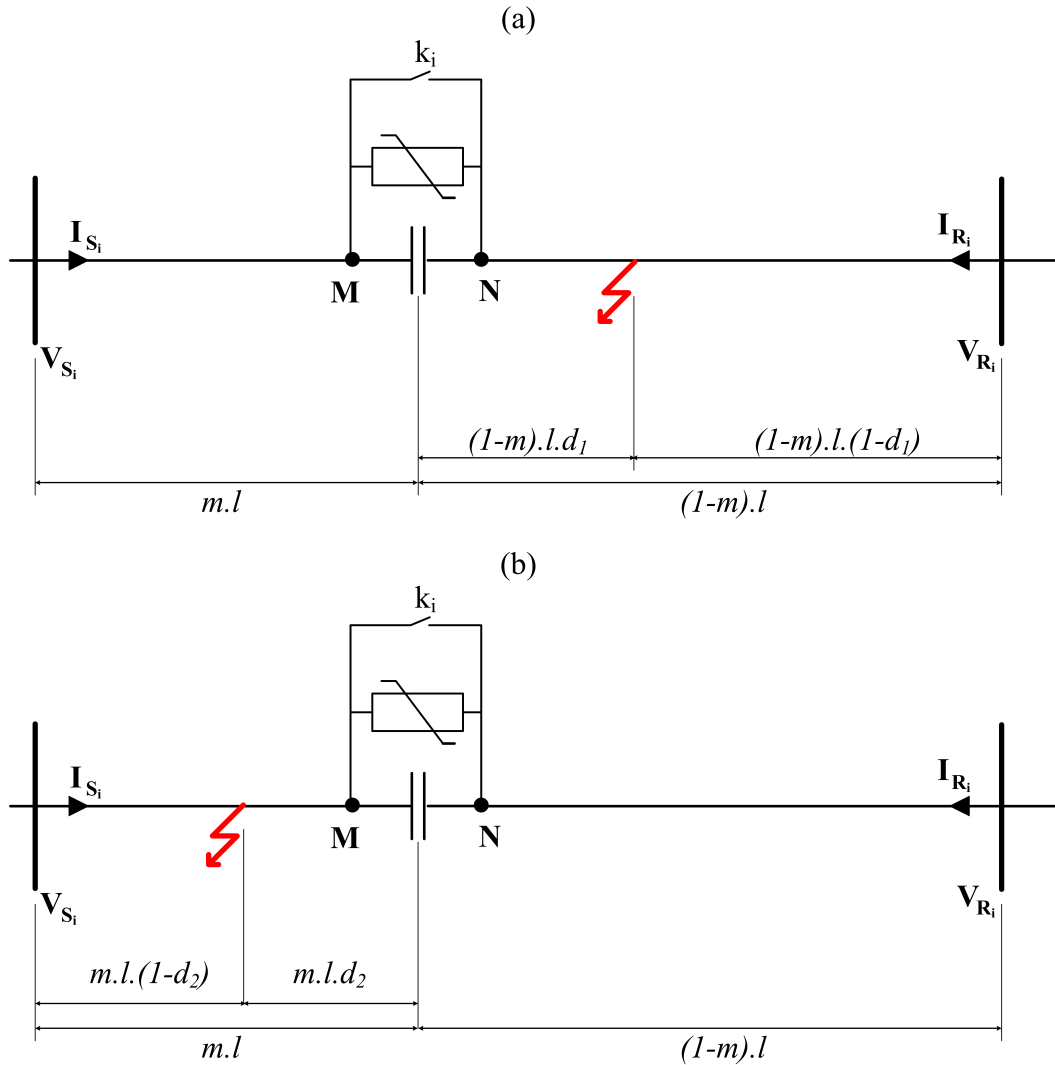


Figure 4.2: Schematic representation of SCCTL under fault conditions (a) Subroutine 1 (b) Subroutine 2

cessive energy dissipation or due to the high fault current. Such bypassing operation either through bypass switch or spark gap, results in the removal of series capacitor and MOV from the power circuit in the faulted phase. Hence, making the analytical estimation of voltage at the faulted end of SCU, feasible. The technique proposed in this chapter referred to as Method A, is focused on obtaining voltage at the faulted end of SCU under such condition when MOV in the faulted phase is bypassed and to use it towards the application of fault location in SCCTLs.

For the elaboration of the proposed fault location technique, the SCU is assumed to be located at the per-unit-distance of  $m$  from the sending end bus (Bus S) as shown in Figure



(4.2). The expressions for the proposed technique have been derived corresponding to the fault at per-unit-distance of  $d_1$  in the section between SCU and the receiving end bus (Bus R) referred to as Subroutine 1 in this chapter. Also,  $k_a, k_b$  and  $k_c$  are the coefficients which attain the value 0 when the MOV in the corresponding phase has been bypassed and 1 if it has not been bypassed. Expressions for the fault in the section between SCU and Bus S i.e., Subroutine 2 can be derived, similarly.

Firstly, the sequence components of voltage and current phasors at non-faulted side of SCU i.e. Node M are obtained from the sequence components of the measured voltage and current signals at Bus S through (4.1) and (4.2), respectively [31].

$$V_i^M = V_i^S \cosh(m\gamma_i l) - I_i^S Z_{c_i} \sinh(m\gamma_i l) \quad (4.1)$$

$$I_i^M = I_i^S \cosh(m\gamma_i l) - \frac{V_i^S}{Z_{c_i}} \sinh(m\gamma_i l) \quad (4.2)$$

where  $i$  is 0,1 and 2 represent zero, positive and negative sequence components, respectively;  $V_i^S$  and  $I_i^S$  are  $i^{th}$  sequence voltage and current at Bus S;  $V_i^M$  and  $I_i^M$  are  $i^{th}$  sequence voltage and current at Node M;  $Z_{c_i}$  is  $i^{th}$  sequence characteristic impedance of the line;  $\gamma_i$  is  $i^{th}$  sequence propagation constant of the line;  $l$  is length of the transmission line;  $m$  is per unit distance of SCU from Bus S.

Since the Node N is in the vicinity of Node M, the current at both Nodes is identical i.e.  $I_i^N = I_i^M$ . Now the voltage at Node N is related to the voltage at Node M through (4.3). Mathematical analysis shown below represents the derivation process of the expression given

in (4.3).

$$\begin{aligned}
V_1^N &= \frac{1}{3}(V_A^N + \alpha V_B^N + \alpha^2 V_C^N) \\
&= \frac{1}{3}((V_A^M - k_1 I_A^M X_C) + \alpha(V_B^M - k_2 I_B^M X_C) \\
&\quad + \alpha^2(V_C^M - k_3 I_C^M X_C)) \\
&= \frac{1}{3}(V_A^M + \alpha V_B^M + \alpha^2 V_C^M - X_C(k_1 I_A^M \\
&\quad + k_2 \alpha I_B^M + k_3 \alpha^2 I_C^M)) \\
&= V_1^M - \underbrace{\frac{X_C}{3}(k_1 I_A^M + k_2 \alpha I_B^M + k_3 \alpha^2 I_C^M)}_{\Delta V_1^{MN}} \\
V_1^N &= V_1^M + \Delta V_1^{MN} \tag{4.3}
\end{aligned}$$

where  $V_A^M, V_B^M, V_C^M$  and  $V_A^N, V_B^N, V_C^N$  are phase voltages at Node M and N, respectively;  $I_A^M, I_B^M, I_C^M$  and  $I_A^N, I_B^N, I_C^N$  are phase currents at Node M and N, respectively;  $V_i^N$  and  $I_i^N$ :  $i^{th}$  are sequence voltage and current at Node N;  $X_C$  is impedance of the series capacitor.

Equation (4.3) can be simplified to (4.4), (4.5) and (4.6) depending upon the fault type and corresponding MOV getting bypassed.

Phase-A MOV bypassed:  $k_a = 0, k_b = 1, k_c = 1$

$$\begin{aligned}
\Delta V_1^{MN} &= -\frac{X_C}{3}(\alpha I_B^M + \alpha^2 I_C^M) \\
&= -\frac{X_C}{3}(I_A^M + \alpha I_B^M + \alpha^2 I_C^M - I_{AS}^M) \\
&= -\frac{X_C}{3}(3I_1^M - (I_0^M + I_1^M + I_2^M)) \\
&= -\frac{X_C}{3}(2I_1^M - I_0^M - I_2^M) \tag{4.4}
\end{aligned}$$

Phase-B and C MOVs bypassed:  $k_a = 1, k_b = 0, k_c = 0$

$$\Delta V_1^{MN} = -\frac{X_C}{3}(I_A^M) = \frac{X_C}{3}(I_0^M + I_1^M + I_2^M) \tag{4.5}$$

Phase-A, B and C MOVs bypassed:  $k_a = 0, k_b = 0, k_c = 0$

$$\Delta V_1^{MN} = 0 \quad (4.6)$$

The positive sequence voltage so obtained at Node N i.e.  $V_1^N$  can now be utilized to obtain fault location ( $d_1$ ) as a fraction of line length between Node N and Bus R using as shown in (4.7), using the fault location algorithm proposed in [14].

$$d_1 = \frac{1}{\gamma_1(1-m)l} \tanh^{-1} \left( \frac{N_{r1}}{D_{r1}} \right) \quad (4.7)$$

where

$$\begin{aligned} N_{r1} &= V_1^R \cosh((1-m)\gamma_1 l) - Z_{c1} I_1^R \sinh((1-m)\gamma_1 l) - V_1^N \\ D_{r1} &= V_1^R \sinh((1-m)\gamma_1 l) - Z_{c1} I_1^R \cosh((1-m)\gamma_1 l) - Z_{c1} I_i^N \end{aligned}$$

$V_1^R$  and  $I_1^R$  are the positive sequence voltage and current at Bus R, respectively. The final fault location as yielded by Subroutine 1 ( $d_1^F$ ), can now be calculated as shown in (4.8).

$$\begin{aligned} d_1^F &= m + d_1 \times (1-m) \\ &= m + \frac{1}{\gamma_1 l} \tanh^{-1} \left( \frac{N_{r1}}{D_{r1}} \right) \end{aligned} \quad (4.8)$$

For the same fault, Subroutine 2 would yield fault location ( $d_2$ ) as a fraction of the line length between Node M and Bus S as represented in (4.9).

$$d_2 = \frac{1}{\gamma_1 m l} \tanh^{-1} \left( \frac{N_{r2}}{D_{r2}} \right) \quad (4.9)$$

where

$$\begin{aligned} N_{r2} &= V_1^S \cosh(m\gamma_1 l) - I_1^S Z_{c1} \sinh(m\gamma_1 l) - V_1^M \\ D_{r2} &= V_1^S \sinh(m\gamma_1 l) - Z_{c1} I_1^S \cosh(m\gamma_1 l) - Z_{c1} I_1^M \end{aligned}$$

Similarly, the final fault location obtained from Subroutine 2 is given by (4.10).

$$\begin{aligned} d_2^F &= 1 - (d_2 \times m + (1 - m)) \\ &= m - \frac{1}{\gamma_1 l} \tanh^{-1} \left( \frac{N_{r2}}{D_{r2}} \right) \end{aligned} \quad (4.10)$$

Now, the numerators and denominators of (4.8) and (4.10) are expanded using (4.1), (4.2) and (4.3). It results in the expressions shown in (4.11) and (4.12).

$$\begin{aligned} N_{r1} &= V_1^R \cosh((1 - m)\gamma_1 l) - Z_{c1} I_1^R \sinh((1 - m)\gamma_1 l) - \\ &V_1^S \cosh(m\gamma_1 l) + I_1^S Z_{c1} \sinh(m\gamma_1 l) - \Delta V_1^{MN} \\ D_{r1} &= V_1^R \sinh((1 - m)\gamma_1 l) - Z_{c1} I_1^R \cosh((1 - m)\gamma_1 l) + \\ &V_1^S \sinh(m\gamma_1 l) - Z_{c1} I_1^S \cosh(m\gamma_1 l) \end{aligned} \quad (4.11)$$

$$\begin{aligned} N_{r2} &= V_1^S \cosh(m\gamma_1 l) - I_1^S Z_{c1} \sinh(m\gamma_1 l) - \\ &V_1^R \cosh((1 - m)\gamma_1 l) + I_1^R Z_{c1} \sinh((1 - m)\gamma_1 l) - \Delta V_1^{NM} \\ D_{r2} &= V_1^S \sinh(m\gamma_1 l) - Z_{c1} I_1^S \cosh(m\gamma_1 l) + \\ &V_1^R \sinh((1 - m)\gamma_1 l) - Z_{c1} I_1^R \cosh((1 - m)\gamma_1 l) \end{aligned} \quad (4.12)$$

It can be observed from (4.4), (4.5) and (4.6) that  $\Delta V_1^{MN}$  and  $\Delta V_1^{NM}$  depend upon the current in the non-faulted phases only.  $\Delta V_1^{MN}$  is calculated using the current through Node M to N while  $\Delta V_1^{NM}$  using current through Node N to M in the non-faulted phases. Since the current in both the cases is equal in magnitude but opposite in direction, therefore implying that for

any particular fault scenario  $\Delta V_1^{NM} = -\Delta V_1^{MN}$ . Examining (4.11) and (4.12) in lieu of the fact that  $\Delta V_1^{NM} = -\Delta V_1^{MN}$ , leads to the observation that  $N_{r1} = -N_{r2}$ . It can also be observed that  $D_{r1} = D_{r2}$ . Now, using the identity:  $\tanh^{-1}(-x) = -\tanh^{-1}(x)$  in (4.8) and (4.10), it can be inferred that  $d_2^F = d_1^F$ .

Therefore, the above mathematical analysis shows that Method A as proposed in this chapter yields the fault location through the usage of only one Subroutine, irrespective of the section of the line in which the fault is lying. It can also be highlighted here that the Method A is able to provide the accurate fault location results only if the time gap between bypassing of MOV and fault interruption is more than the time response of the phasor estimation algorithm being utilized. It is due to the fact that the bypassing operation of MOV changes the state of the system and consequently alters the measured current and voltage signals which get reflected fully in the estimated phasors only after the passage of the response time of the phasor estimation filter.

It is important to note here that, expressions given in (4.4) and (4.5) highlight the dependence of positive-sequence voltage at Node N on the positive, negative and zero-sequence components of the current and positive-sequence voltage at Node M for single-phase to ground, double-phase to ground and phase to phase faults. Thus, forcing the involvement of the zero-sequence parameters of the transmission line in the computation of voltage at Node N. Since the zero-sequence parameters are sensitive to many environmental and geological factors, ambiguity always remains in their accuracy. However, the significant observation that can be made here is that zero-sequence components of only current at Node M are involved in (4.4) and (4.5). It is a known fact that the current in a transmission line changes very less as we move from one end of the line towards the fault point whereas the voltage gradient is very high over the same distance. Therefore, error in the estimation of zero-sequence parameters of the transmission line is not going to incur considerable error in estimated zero-sequence fault current at Node M. Thus, making Method A to be less sensitive to the variations in zero-sequence parameters as compared to the fault location algorithms using fault loop analysis as further

demonstrated in this chapter.

## 4.4 Test System and MOV Sizing

In order to evaluate the performance of Method A, a test power system is considered in PSCAD while fault location algorithm has been modeled in Matlab. Phasor estimation technique used in this text is Cosine algorithm. Also brief methodology for sizing the MOV for the power system specified in the PSCAD is presented thereafter. For the comparative analysis, the performance of Method A has been compared with the fault location technique proposed in [14], which is referred to as Method B in this chapter, hereafter.

### 4.4.1 Test System

A 500 kV, 350 km SCCTL is considered in PSCAD/EMTDC as a test case in this manuscript. As shown in Figure4.3, 70% series compensation which corresponds to an equivalent capacitance of  $29.11\mu\text{F}$  ( $91.1\Omega$ ) is assumed at the sending end of the line for System A and in the middle for System B. The line positive and zero-sequence impedances are  $Z_{L1} = (0.0155 + j0.3719)\Omega$  per km,  $Z_{L0} = (0.3546 + j1.0670)\Omega$  per km, respectively, and line positive and zero-sequence admittances are  $Y_{L1} = (0 + j4.4099 \times 10^{-6})\text{U}$  per km,  $Y_{L0} = (0 + j2.7844 \times 10^{-6})\text{U}$  per km, respectively. Positive and zero-sequence impedances for sending end source are  $Z_{S1} = (.5 + j7.5)\Omega$ ,  $Z_{S0} = (1.2 + j12.5)\Omega$  respectively. Positive and zero-sequence impedances for receiving end source are  $Z_{R1} = (1.2 + j18)\Omega$ ,  $Z_{R0} = (2.6 + j26.5)\Omega$ , respectively. Load angle is  $30^\circ$  with receiving end source voltage lagging. The basis for the low impedance values of sending end source is that the spark gap configuration of SCPU is used for strong SCU buses as mentioned in Section 4.2.

Further, current and voltage signals are obtained by using CT and CVT models, respectively, available in PSCAD. A  $2^{nd}$  order anti-aliasing filter with a cutoff frequency of 1920 Hz is applied to the output of each instrument transformer and its output is recorded with the sam-

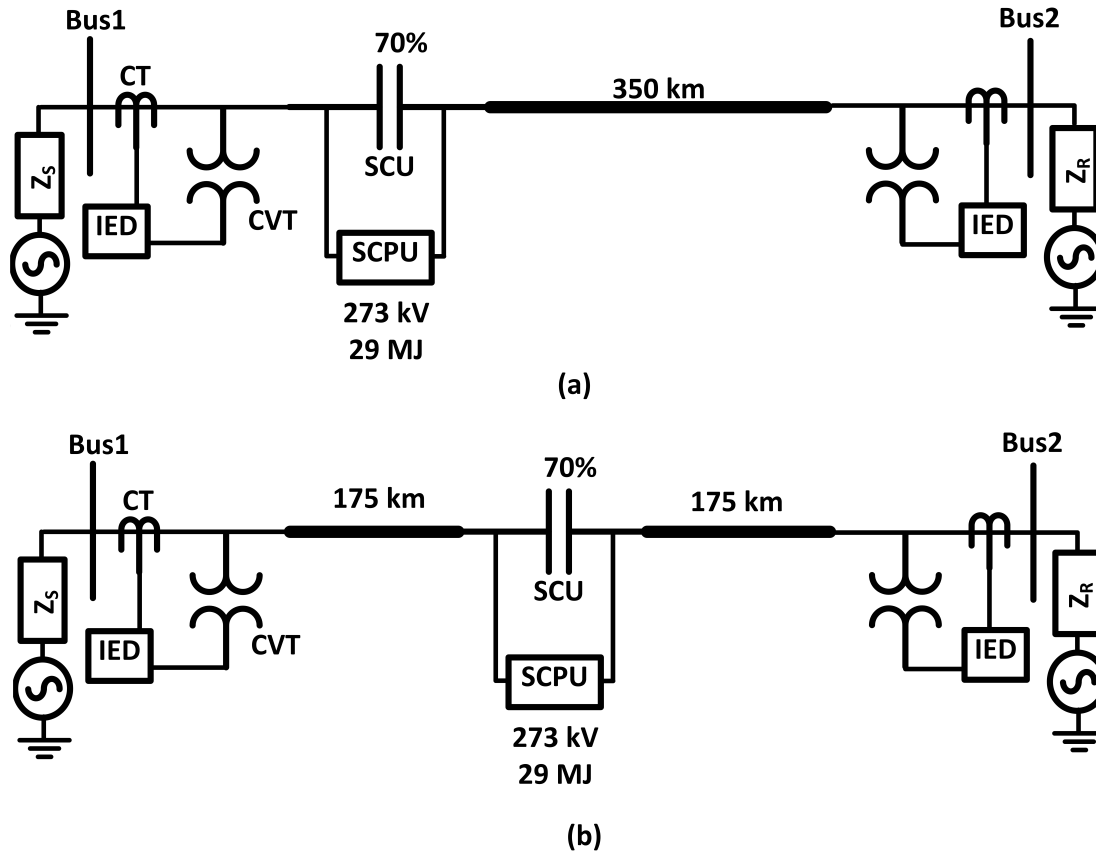


Figure 4.3: Single-line diagram of the simulated systems in PSCAD/EMTDC (a) System A (b) System B

pling rate of 20 kHz. The recorded signal is imported and resampled at 3840 Hz in Matlab. The resampled voltage and current signals are applied to cosine algorithm for phasor estimation, the results of which are fed to the fault location algorithm. Nominal operating times of SCPU elements have been considered for the purpose of analysis which are as: Fault clearance time by line breakers: 4 cycles of fundamental frequency, operating time delay of bypass switch: 2.5 cycles of fundamental frequency, operating time delay of spark gap: 1ms.

## 4.4.2 MOV Sizing

### Maximum MOV Current Threshold

The rated current of 2000A, equivalent to the transmission line capacity of 1750 MVA, is considered for sizing SCPU. Detailed procedure for sizing MOV has been presented in [25]. For the sake of simplicity, only threshold values and their significance has been presented in this chapter. MOV rating after considering an overload factor of 1.5 is calculated as 273 kV. The protective level current of MOV ( $I_{PR}$ ) corresponding to MOV rating of 273 kV is 4 kA.  $I_{PR}$  is the RMS value of the minimum amount of the current through SCU that would lead to MOV conduction. For protecting MOV against large fault currents, SCPU is set to immediately bypass the MOV through spark gap if the MOV instantaneous current is above the bypass current ( $I_{BP}$ ) which is equal to 8 kA for the test system under the study.

### Maximum MOV Energy Threshold

For practical applications, MOV in spark-gap configurations is designed to tolerate the energy storage for four cycles of the worst possible case of external fault conditions without getting bypassed while for gapless scheme MOV is sized corresponding to the most severe internal fault. As already mentioned that in gapless scheme, MOV is immediately bypassed if SCU is reinserted onto a fault at the time of reclosing. However, the only criteria for Method A to yield accurate fault location results is that MOV in faulted phase should be bypassed. Therefore, the maximum energy dissipation capacity of MOV has been put at 29 MJ as it would result in the bypass of MOV for considerable number of fault scenarios and is in the range of practical applications. The value of 29 MJ for the maximum energy dissipation capacity of MOV was arrived at after running PSCAD simulation for different types and locations of the faults.



## 4.5 Evaluation

It can be seen from Figure 4.3 that System A offers higher range of fault scenarios than System B because any fault in System B is located at 50% or greater length from the bus that sees the SCU current. That is precisely the reason that System A configuration is selected for the elaboration of the immunity of Method A to the errors in zero-sequence parameters and CT-CVT measurements. However, to present the fact that only one subroutine is sufficient to locate the fault in both segments of transmission line split by SCU, few fault cases have been simulated in System B configuration of SCCTL. It should be noted here that the final value of fault location is arrived at after averaging fault location results over the entire steady state interval.

### 4.5.1 Effect of error in zero-sequence parameters

As already discussed in Chapter 3, Method B utilizes the fault loop current ( $I_F$ ) and voltage ( $V_F$ ) for the purpose of fault location and consideration of natural fault loops comes with the compulsion of using zero-sequence parameters of transmission line for fault location in SCCTLs [25]. As explained earlier in the Section 4.1, ambiguity in the accuracy of zero-sequence parameters always remains due to their dependence on environmental conditions, therefore, Method B is expected to be prone to errors. Though, the authors in [14] have tried to minimize the usage of zero-sequence currents in the fault location algorithm but still the usage of zero-sequence voltage remains unavoidable for the single phase to ground faults which are the most common fault events encountered in a transmission system [14].

The Method A however, uses only zero-sequence currents and signals from both ends of a transmission line for fault location as shown in (4.4),(4.5) and (4.6). As pointed out earlier that the current in a transmission line does not undergo a considerable change from line terminal to the fault point. Therefore, the current is not affected considerably, by the error in zero sequence parameters. Consequently, making the Method A, more robust as also illustrated by

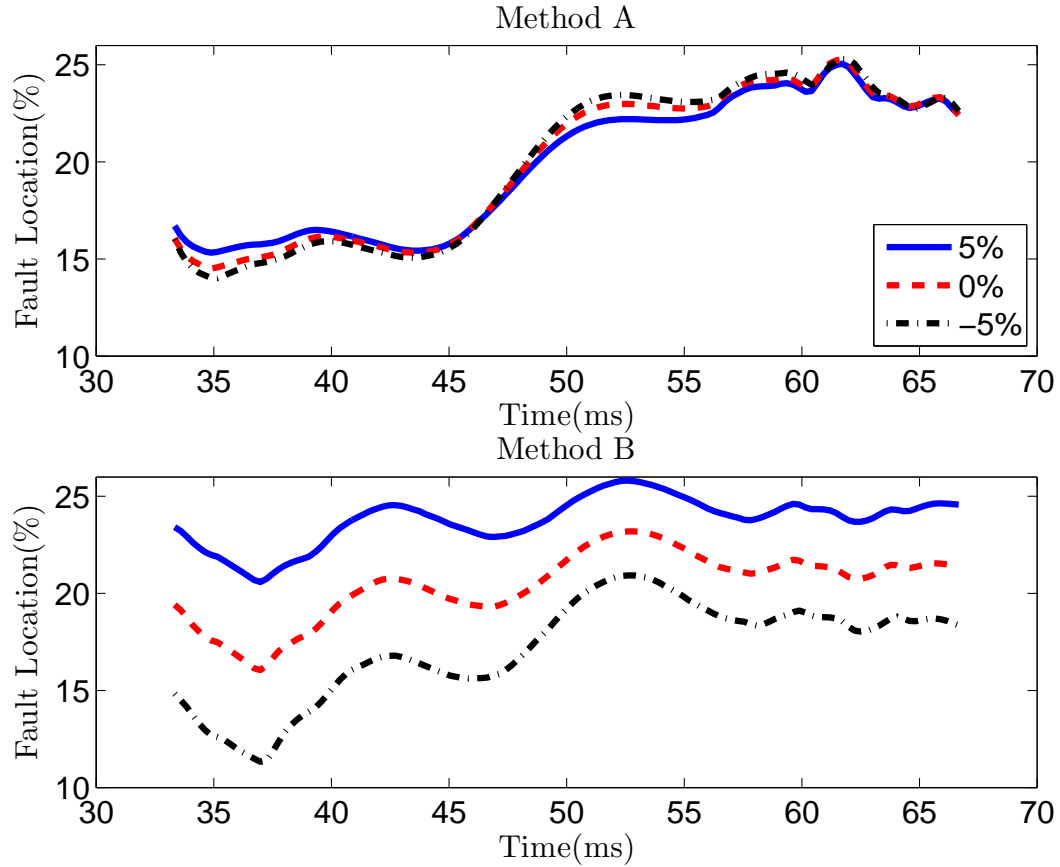


Figure 4.4: Effect of erroneous zero-sequence parameters on fault location

the simulation results.

In order to show the impacts of erroneous estimation of zero-sequence parameters of the line on the fault location results yielded by the Method A and Method B, three sets of AG fault were simulated. Deliberate errors of +5% and -5% were added to the zero-sequence parameters for the two sets of simulations while third set had accurate zero-sequence parameters. Figure 4.4 shows the fault location obtained by both the techniques for A-G fault at 20% of the line length for different errors in zero-sequence parameters of the system. As observed from Figure 4.4 that fault location results yielded by the Method A technique are almost identical to each other irrespective of the error in zero-sequence parameters while Method B yields different results depending upon the amount of error in zero-sequence parameters. It therefore, implies that Method A is secure against the errors in zero-sequence parameters of the line while Method

Table 4.1: Error in Fault Location for Solid AG Faults due to Erroneous Zero-sequence Parameters (%) )

Errors in Zero seq(%)	Technique	Fault Location(%)				
		10	20	30	40	50
0%	Method A	0.10	1.94	0.26	0.15	1.60
	Method B	0.38	0.01	0.95	0.82	0.31
-5%	Method A	0.92	1.96	0.72	0.49	1.49
	Method B	3.90	3.55	3.68	3.31	2.34
5%	Method A	0.17	1.89	0.32	0.55	2.28
	Method B	4.23	3.53	1.43	1.68	1.77

B remains susceptible to such errors.

Table 4.1 compares the fault location results for both the techniques for different errors in zero-sequence parameters and different fault locations. It can be seen that as the zero-sequence parameters of the transmission line are changed, the Method A shows a lower error as well as lesser fluctuations in fault location results while those obtained from the Method B have higher deviations and errors due to its higher dependency on zero-sequence parameters. Since the Method B relies on the consideration of natural fault loops for fault location, the fault loop voltage in the case of BCG i.e.,  $V_F = V_B - V_C$  is independent of the zero-sequence voltage of the system. That is precisely the reason that BCG faults were not studied in this study. The blank columns in the tables mean that for that particular fault scenario, there is no MOV bypass achieved or the time gap between bypassing of MOV and fault interruption was less than the response time of the phasor estimation technique.

#### 4.5.2 Immunity to CT/CVT errors

Due to the presence of internal leakage reactance and relay burden, the instrument transformers are unable to reproduce exact signals at their output terminals. These errors become more prominent when the system is passing through a transient state, which may lead to the phenomena of CVT transients and CT saturation which further exacerbates the error in output of instrument transformers. Therefore, phasors estimated from the secondary side measurements of instrument transformers are unable to represent the signal at the input of the instrument

Table 4.2: Maximum Error in Fault Location for CT-CVT errors (%)

Fault type	Technique	Fault Location(%)				
		0	20	40	60	80
AG	Method A	–	3.24	1.39	–	–
	Method B	–	5.76	2.87	–	–
BCG	Method A	–	0.39	1.01	1.65	–
	Method B	–	3.91	2.96	2.05	–
BC	Method A	0.22	0.54	0.84	–	–
	Method B	4.60	3.60	2.72	–	–
ABC	Method A	0.16	0.34	0.53	0.55	0.58
	Method B	3.54	3.70	3.05	2.19	1.12

transformer exactly.

In this section, both the techniques i.e. Method A and Method B have been analyzed for the effects of errors in phasor magnitude and phase angle on the fault location results. In order to show the effects of instrument transformer errors on fault location, deliberate error of  $3^\circ$  in the phase angle and 2% error in phasor magnitude was added to the different combinations of current and voltage phasors from sending and receiving end in the series of simulation runs. Total of 288 cases were generated by repeating the fault conditions under the different sets of erroneous phasors.

Two indices that have been used here to present the comparative analysis are: maximum error and standard deviation of the fault location results for each set of simulations. Table 4.2 shows the maximum error encountered while Table 4.3 shows the standard deviation of the fault location results for different types of faults at a particular fault location. Higher maximum error found in the fault location results yielded by Method B translates into extra time needed to scan the larger section of the transmission line for the faults. Similarly, higher standard deviation for Method B results indicates the difficulty in calibration of fault location algorithm, as the fault location results vary widely when error gets introduced in different sets of estimated phasors.

Therefore, it can be concluded that performance of the Method A is superior as compared to Method B under the influence of CT/CVT errors.

Table 4.3: Standard Deviation in Fault Location for CT-CVT errors (%)

Fault type	Technique	Fault Location(%)				
		0	20	40	60	80
AG	Method A	–	1.63	2.15	–	–
	Method B	–	6.74	4.26	–	–
BCG	Method A	–	0.84	1.25	1.29	–
	Method B	–	4.15	3.32	2.36	–
BC	Method A	0.27	1.25	1.83	–	–
	Method B	4.25	3.94	3.20	–	–
ABC	Method A	0.14	0.67	0.97	1.01	0.78
	Method B	3.31	5.27	4.13	2.84	1.45

Table 4.4: Results for Subroutine 1 and 2 of Method A

Actual Fault Location(%)	Subroutine: Method A	Fault Type			
		AG	BCG	BC	ABC
60	Subroutine 1	60.2847	60.1018	60.3695	60.4918
	Subroutine 2	59.4021	59.4191	59.5901	60.0211
80	Subroutine 1	–	80.1299	80.6173	80.2812
	Subroutine 2	–	79.3847	79.6329	80.0159

### 4.5.3 One subroutine for both line segments

Method A requires only one subroutine to locate the fault in both the sections of the transmission line resulting from the bifurcation of the transmission line by the location of SCU. As shown in Table 4.4 that both of the Method A subroutines i.e. Subroutine 1 and 2 yield very close fault location results. However, in [14] two separate subroutines have been proposed for the faults in both the sections of the line. Both of the subroutines are run for a fault scenario and result of one of the two subroutines is selected as per criterion given in [14].

## 4.6 Summary

In this chapter, operational concept of SCPU was explored in synchrony with the fault location in SCCTLS. In depth analysis of SCPU behavior led to the identification of the possibility of accurate analytical estimation of line voltages from the bus measurements. Hence, resulting in the preposition of a new fault location technique for SSCTLS. The proposed fault technique

was verified and validated through comprehensive simulation runs in PSACD/Matlab. The proposed technique is highly accurate and precise, though it does not cover all the possible fault scenarios. In conclusion, it is a salient and straightforward enhancement to the existing fault location techniques for SCCTLs.

# Chapter 5

## Summary and Conclusion

### 5.1 Summary

In Chapter 1, different aspects of series capacitor compensated transmission lines (SCCTLs) and fault location in SCCTLs were discussed in detail. In the later part of the chapter under Section 1.6, the problem was defined and available solutions were discussed. Chapter 1 also presented the insight to literature survey and author's objectives and contributions of the thesis. In Chapter 2, a recently proposed offline phasor estimation technique, Prony-DFT was discussed and an enhanced approach to Prony-DFT was presented for the application in the field of fault location in SCCTLs. The Cosine algorithm was also discussed in lieu of the fault location in SCCTLs and was compared relative to Prony-DFT. The study conducted in Chapter 2 was supported by simulations in PSCAD and Matlab.

In Chapter 3, it was demonstrated that the well-known fault location algorithm for SCCTLs as proposed in [14] yields highly inaccurate results when the location of SCU is changed from the middle of the line to one of its end. It was also presented that the proposed algorithm is essentially an argument comparison of the fault voltage and current. In Chapter 3, it was proposed that in order to get the most accurate fault location results, it is important to follow the time-line of operation of each element of SCPU. Simulations in PSCAD and Matlab were

conducted to demonstrate the observations.

In Chapter 4, a new complimentary fault location algorithm for SCCTLs was proposed which considerably improves the fault location results when MOV gets bypassed before the interruption of the fault. Another significant highlights of the proposed technique is that it is highly independent of zero sequence parameters of the transmission lines and is immune to the CT/CVT errors. The proposed complimentary algorithm was further evaluated through comprehensive simulations run in PSCAD and Matlab .

## 5.2 Contribution

This research study has resulted in the following key contributions:

1. An enhanced approach to Prony-DFT was proposed and implemented in discrete time domain; therefore, making it independent of any assumptions needed to relate the discrete time processes to its continuous time domain counterpart.
2. Fault location algorithms found in literature were only tested for the scenario when SCU was located in the middle of the line. In this study, a widely used algorithm as proposed in [14] was evaluated by putting it at the end of the transmission line. It was shown that it becomes highly erroneous for certain fault scenarios in SCCTLs.
3. A new complimentary fault location algorithm for SCCTLs was proposed which considerably improves the fault location results when MOV gets bypassed before the interruption of the fault.

## 5.3 Future Research Work

1. As demonstrated in this thesis, the existing fault location algorithms for SCCTLs yield highly inaccurate results due to the fact that they use voltage from only one end of the



transmission line along with the current from both ends. Therefore, research can be conducted towards devising a fault location algorithm for SCCTLs, which uses the voltage and current information from both ends of the transmission line to achieve a higher degree of robustness and accuracy.

2. Since the study so far has been focused entirely on the transmission lines compensated with fixed series capacitor (FSC). The scope of the study can be extended by testing the algorithm and possibly proposing new techniques when the line is compensated by FACTS-based series compensation such as TCSC and SSSC.

# Bibliography

- [1] R.M. Mathur, R.K. Varma, "Thyristor based FACTS controllers for electrical transmission system", Wiley IEEE Press, February 2002.
- [2] V.Cook, "Fundamental aspects of fault location algorithms used in distance protection," *Proc.IEE*, vol. 133, no. 6, Sept. 1986.
- [3] R. Grunbaum, J.Samuelsson, "Series capacitors facilitate long distance AC power transmission," *Proc. 2005 IEEE PowerTech*, St. Petersburg, Russia.
- [4] "Series Capacitors for increased power transmission capacity in the Finnish 400 kV grid," ABB AB, Vasteras, Sweden, Application Note A02-0222 E, Nov. 2010.
- [5] R. Grunbaum, J. Samuelsson, C.Li, "Series capacitors for increased power transmission capacity of a 500 kV grid intertie," *EPEC*, pp. 164-169, 2012.
- [6] Series Capacitor Bank Protection Tutorial, 1<sup>st</sup> ed., IEEE Power System Relaying Committee WG K13, Piscataway, NJ, 1997, pp. 1-35.
- [7] G.E. Lee, D.L. Goldsworthy, "BPA's pacific AC intertie series capacitors: experience, equipment and protection," *IEEE Transactions on Power Delivery*, vol.11, no.1, Jan. 1996.
- [8] J. Sadeh , A. Adinehzadeh, "Accurate fault location algorithm for transmission line in the presence of series connected FACTS devices. *Int. J. Elect. Power Energy Syst.*, vol. 32, no. 4, pp. 323328, May 2010.

- [9] M. Al-Dabbagh , S. K. Kapuduwage, “Using instantaneous values for estimating fault locations on series compensated transmission lines. *Elect. Power Syst. Res.*, vol. 76, pp. 2532, Sept. 2005.
- [10] J. Sadeh, N. Hadjsaid, A.M. Ranjbar, R. Feuillet, ”Accurate fault location algorithm for series compensated transmission lines,” *IEEE Transactions on Power Delivery*, vol.15, no.3, pp.1027-1033, Jul 2000.
- [11] M.G. Ahsae, J. Sadeh, ”A Novel Fault-Location Algorithm for Long Transmission Lines Compensated by Series FACTS Devices,” *IEEE Transactions on Power Delivery*, vol.26, no.4, pp.2299-2308,Oct.2011.
- [12] J. Izykowski, E. Rosolowski, P. Balcerek, M. Fulczyk and M.M. Saha, “Accurate non iterative fault-location algorithm utilizing two-end unsynchronized measurements,” *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 547-555, Apr. 2011.
- [13] I. Voloh, Z. Zhiying, S. Picard, “Fault locator based on line current differential relay synchronized measurements,” *10th IET International Conference on Managing the Change, Developments in Power System Protection (DPSP 2010)*, pp. 1-5, Mar.-Apr. 1 2010.
- [14] J. Izykowski, E. Rosolowski, P. Balcerek, M. Fulczyk, M.M. Saha, “Fault location on double-circuit series-compensated lines using two-end unsynchronized measurements,” *IEEE Trans. on Power Delivery*, vol. 26, no. 4, pp. 2072-2080, Oct. 2011.
- [15] M.M. Saha, J. Izykowski, E. Rosolowski, B. Kasztenny, “A new accurate fault locating algorithm for series-compensated lines,” *IEEE Trans. on Power Delivery*, vol. 14, no. 3, pp. 789-797, Jul. 1999.
- [16] M.M. Saha, K. Wikstrom, J. Izykowski, E. Rosolowski, “Fault location in uncompensated and series-compensated parallel lines,” in *Proc. IEEE Power Eng. Soc. Winter Meeting*, Singapore, Jan. 2000, vol. 6, pp. 23-27.

- [17] G. Benmouyal, "Removal of DC-offset in current waveforms using digital mimic filtering," *IEEE Transaction on Power Delivery*, vol. 10, no. 2, pp. 621-630, Apr 1995.
- [18] Y.S. Cho, C.K. Lee, G. Jang, H.J. Lee, "An innovative decaying dc component estimation algorithm for digital relaying," *IEEE Transaction on Power Delivery*, vol.24, no.1, pp.73-78, Jan. 2009.
- [19] S.H. Kang, D.G. Lee, S.R. Nam, P.A. Crossley, Y.C. Kang, "Fourier transform-based modified phasor estimation method immune to the effect of the dc offsets," *IEEE Transaction on Power Delivery*, vol. 24, no. 3, pp. 1104-1111, July 2009.
- [20] M.R.D. Zadeh, Z. Zhang, "A New DFT-based Current Phasor Estimation for Numerical Protective Relaying", *IEEE Transaction on Power Delivery*, 2013.
- [21] E.O. Schweitzer and D. Hou, "Filtering for protective relays," *19th Annual Western Protective Relay conference*, Spokane,WA, 1992.
- [22] C. S. Yu, "A reiterative DFT to damp decaying dc and subsynchronous frequency components in fault current," *IEEE Trans. Power Del.*, vol. 21, no. 4, pp. 1862-1870, Oct. 2006.
- [23] J. C. Gu , K.Y. Shen, S.L. Yu and C.S. Yu, "Removal of DC offset and subsynchronous resonance in current signals for series compensated transmission lines using a novel fourier filter algorithm," *Elsevier Electric Power Systems Research*, vol. 76, pp. 327-335, Mar. 2006.
- [24] R. Rubeena, M. R. D. Zadeh and T. P. S. Bains, "An Accurate Offline Phasor Estimation for Fault Location in Series Compensated Lines," *IEEE Trans. Power Del.*, vol. 29, no. 2, pp. 876-883, Apr. 2014.

- [25] T. P. S. Bains and M. R. D. Zadeh, "Challenges and Recommendations for Fault Location in Series Compensated Transmission Lines," presented at IEEE PES General Meeting, National Harbor, MD, 2014.
- [26] U.L. Rohde, G.C. Jain, A.K. Poddar and A.K. Ghosh, "Introduction to Integral Calculus: Systematic Studies with Engineering Applications for Beginners," First Edition, John Wiley and Sons, 2012, pp. 97-120.
- [27] S.L. Marple, Digital Spectral Analysis with Applications, Englewood Cliffs, New Jersey: Prentice-Hall Inc., 1987, pp. 304.
- [28] T. Maekawa, Y. Obata, M. Yamaura, Y. Kurosawa, H. Takani, "Fault location for series compensated parallel lines," *IEEE/PES Asia Pacific Transmission and Distribution Conference and Exhibition*, vol. 2, pp. 824-829, 6-10 Oct. 2002.
- [29] C. S. Yu , C. W. Liu , S. L. Yu , J. A. Jiang , "A new PMU-based fault location algorithm for series compensated lines," *IEEE Trans. on Power Delivery*, vol. 17, no. 1, pp. 33-46, Jan. 2002.
- [30] D. L. Goldsworthy, "A linearized model for MOV-protected series capacitors," *IEEE Trans. Power Syst.*, vol.-2, no. 4, pp. 953-958, Nov. 1987.
- [31] J. D. Glover, M. S. Sarma, T. J. Overbye *Transmission Lines: Steady-state Operation*, in *Power System Analysis and Design*, 5th ed. Stamford, USA: Cengage Learning, 2012, ch. 5, sec. 2, pp. 254-258

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1. R. Rubeena, M. R. D. Zadeh and T. P. S. Bains, "An Accurate Offline Phasor Estimation for Fault Location in Series Compensated Lines," *IEEE Trans. Power Del.*, vol. 29, no. 2, pp. 876-883, Apr. 2014.
2. T. P. S. Bains and M. R. D. Zadeh, "Challenges and Recommendations for Fault Location in Series Compensated Transmission Lines," presented at IEEE PES General Meeting, National Harbor, MD, 2014.
3. T. P. S. Bains and M. R. D. Zadeh, "Enhanced Phasor Estimation Technique for Fault Location in Series Compensated Lines," *IEEE Trans. Power Del.* (submitted on April 26, 2014)