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Experimental Study Of Cmos Structures: Design For Reliability In Hostile Environments

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Experimental Study of CMOS Structures: Design for Reliability in Hostile Environments

by

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ABSTRACT

Complementary Metal Oxide Silicon (CMOS) technology has been the fastest growing fabrication process for the Very Large Scale Integrated (VLSI) circuits in the last few years, and long term predictions confirm its future importance. The minimum CMOS feature size is presently about one micron and it is certain that feature dimensions will reach the submicron range in mid nineties.

Smaller dimensions yield advantages, namely greater speed, higher device complexity and performance, and disadvantages such as greater susceptibility to electrical damage. During the past few years, the reliability of CMOS integrated circuits has received much attention, matched by publications on the subject. Higher reliability hardened integrated circuits have been developed as a response to demands for simplified shielding and demands for more reliable systems operating in hostile environments. The key step in developing hardened integrated circuits is the study of the mechanisms that make them fail. By understanding the failure conditions one can design more reliable components, select more suitable materials, and improve in-process control and screening. Also, it allows to develop test patterns, or accelerated test strategies for the evaluation of the integrated circuits susceptibility to damage.

In this study, a series of measurements were performed on a variety of custom fabricated CMOS Charge-Coupled Devices (CCDs) and dedicated modular test structures to investigate the latent mode of failure due to Electrostatic Discharge (ESD). Test devices were stressed using the current injection method and measurements of the quiescent current were used to detect the failure thresholds. The fault sites were further isolated and the failure mechanisms studied by measuring the electrical characteristics

before and after thermal and optical interaction. The measurements of oxide trapped charge was performed using capacitance-voltage profiles. A model was proposed to explain the observed phenomena, based on charge injection and trapping in the gate oxide. The experimental methods developed for locating, measuring and analysis of the failure sites have been found sufficiently robust to be generally useful.

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ABBREVIATIONS AND SYMBOLS

BCCD	Bulk-channel charge-coupled device
CCD	Charge-coupled device
CMOS	Complementary metal-oxide semiconductor
C-V	Capacitance-Voltage
ehp	Electron-hole pair
G-R	Generation-recombination
HF	High-frequency
LF	Low-frequency
MOS	Metal-oxide semiconductor
MOS-C	Metal-oxide-semiconductor capacitor
MOSFET	Metal-oxide-semiconductor field-effect transistor
SCCD	Surface channel charge-coupled device
scr	Space-charge region (depletion region)
Si	Silicon

NOMENCLATURE

A	Gate area (cm^2)
C_D	Depletion layer capacitance per unit area (pF/cm^2)
C_{FB}	Flatband capacitance per unit area (pF/cm^2)
C_g	Gate-to-substrate capacitance per unit area (pF/cm^2)
C_{ox}	Oxide capacitance per unit area (pF/cm^2)
d_{ox}	Oxide thickness (cm)
D_{it}	Interface-state density ($cm^{-2}eV^{-1}$)
E_c	Minimum conduction band energy (eV)
E_F	Fermi energy or Fermi level (eV)
E_i	Intrinsic Fermi level (eV)
E_N	Electron quasi-Fermi level (eV)
E_P	Hole quasi-Fermi level (eV)
E_{si}	Electric field strength of silicon (V/m)
E_v	Maximum valence band energy (eV)
E_{vacuum}	Vacuum level, minimum energy an electron must process to completely free itself from a material (eV)
g_m	Transconductance of MOSFET
I_{DS}	Drain-to-source current (A)
K_o	Oxide dielectric constant (3.9 for SiO_2)
K_s	Semiconductor dielectric constant (11.8 for Si)
L_{ch}	MOSFET, CCD gate length (cm)
L_D	Intrinsic Debye length (cm)
n	Number of elemental CCD transfers
n	electron concentration (cm^{-3})

NOMENCLATURE (Cont.)

N_A	Acceptor doping concentration (cm^{-3})
N_D	Donor doping concentration (cm^{-3})
q	Magnitude of electron charge ($1.602x10^{-19}$ C)
Q	Charge density (C/cm^2)
Q_f	Fixed oxide charge (C)
Q_{it}	Interface trapped charge (C)
Q_m	Mobile ionic charge (C)
Q_{ot}	Oxide trapped charge (C)
Q_{Si-SiO_2}	Charge in $Si-SiO_2$ system (C)
V_{DS}	Drain voltage (V)
V_{DD}	Supply voltage (V)
V_{GS}	Gate-to-source voltage (V)
V_G	Gate voltage (V)
V_{out}	Output voltage (V)
V_{sub}	Substrate voltage (V)
V_S	Input signal voltage (V)
V_{SS}	Ground
V_T	Threshold or turn-on voltage (V)
W	Depletion width (cm)
W_{ch}	Width of channel in MOSFET(cm)
ε	CCD elemental transfer inefficiency
ε_0	permittivity of free space ($8.85x10^{-14}$ F/cm)
ε_{Si}	permittivity of silicon ($1.035x10^{-12}$ F/cm)

NOMENCLATURE (Cont.)

ε_{SiO_2}	permittivity of silicon dioxide (0.345×10^{-12} F/cm)
η	CCD transfer efficiency
λ	CCD charge loss
ρ	Charge density (C/cm^3)
ψ_B	Bulk potential (V)
ϕ_i	CCD gate connection as phase
ϕ_S	Semiconductor surface potential (V)
ϕ_{ms}	Metal-semiconductor work function difference (V)
ϕ_{FN}	Electron quasi-Fermi potential (V)
ϕ_{FP}	Hole quasi-Fermi potential (V)
ϕ_R	Reset gate phase

Chapter 1

The Physics and Reliability of Charge-Coupled Devices (CCDs)

This chapter describes the physics and technology of charge-coupled devices. It includes a review of ideal and non-ideal MOS capacitors, a description of the basic principles of charge-coupled devices (CCDs), and an investigation of the reliability of CCDs. Finally, the objectives of this project are presented.

1.1 Introduction

After the invention of charge-coupled devices (CCDs) in the early 1970s, the technology has been extensively employed in the fields of image sensing, analog signal processing and analog memories. However, CCDs have had most significant impact in the field of imaging. CCD Linear Imaging Devices (LIDs) and Area Imaging Devices (AIDs) are used in many applications ranging from lightweight, low-power television cameras to spectrometers. CCDs are simple to fabricate and are suitable for a variety of applications; relatively standard silicon wafer manufacturing technology is employed in their manufacture. In principle, the CCD array is a microelectronic structure consisting of MOS capacitors (MOS-C) connected in parallel, that use diodes on the input and the output for injecting or detecting the capacitor charges. In the following sections, the physical properties of MOS-C are reviewed and the basic principles of charge-coupled devices discussed.

1.2 Review of Metal-Oxide-Semiconductor Capacitor (MOS-C)

Most modern integrated circuits are based on the metal-oxide-semiconductor (MOS) technology. Among MOS devices, the simplest structure is the MOS-Capacitor. It can be used as a test structure or as the fundamental building block in more complex MOS systems. As a building block, it is used as the unit cell of the Dynamic Random Access Memory (DRAM) and Charge-Coupled Devices (CCDs). If used as a test structure, it provides detailed information about the oxide and the semiconductor. The MOS-C, as shown in Figure 1.1, is a two terminal device consisting of a thin silicon dioxide (SiO_2) layer sandwiched between an electrode and a silicon substrate. The electrode can be aluminum or heavily doped polycrystalline silicon (polysilicon). The silicon substrate is grounded by an ohmic contact. The ohmic contact on the substrate, called the back contact, is normally grounded. MOS capacitors are different from the capacitors made by two conducting parallel plates; characteristics strongly depend on the voltage applied on the gate.

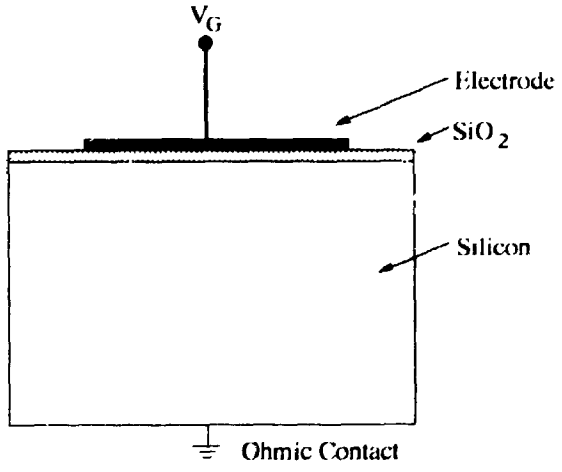


Figure 1.1 Metal-Oxide-Semiconductor Capacitor

In an ideal MOS-C structure, one assumes that: (1) the oxide is a perfect insulator and therefore no current flows through the oxide layer under all bias conditions; (2) there are no recombination-generation (R-G) centers located at the oxide-semiconductor interface and inside the oxide; (3) the semiconductor is uniformly doped; (4) the gate electrode is sufficiently thick to be considered as equipotential under all bias conditions. In the following discussion, the MOS-C is assumed to be an ideal structure.

The energy band diagrams for the individual components of the MOS structure are shown in Figure 1.2. The vacuum level, shown at the top of the vertical line, denotes the minimum energy that an electron must possess to completely free itself from the material. E_c, E_F, E_i and E_v correspond to the energy level for the conduction-band, Fermi energy, intrinsic energy and valence-band, respectively. In a metal, the energy difference between the vacuum and the Fermi energy ($E_{vacuum} - E_F$) is called the metal work function, ϕ_M, and is constant for a specific metal. However, for semiconductors, the Fermi energy level is a function of doping and if voltage is applied to the gate, the energy bands bend accordingly. Therefore, the height of the surface energy barrier is defined in terms of the electron affinity which is defined as the energy difference between the vacuum level and the conduction band edge at the surface of the semiconductor.

A MOS structure is formed when the metal, oxide and semiconductor are brought together. Since under equilibrium conditions, the Fermi level inside a material, or a group of materials in contact, is invariant of position, it must line up inside the MOS structure. From Figure 1.2, the metal work function is defined as the electron affinity plus the difference between the conduction-band and the Fermi level in the

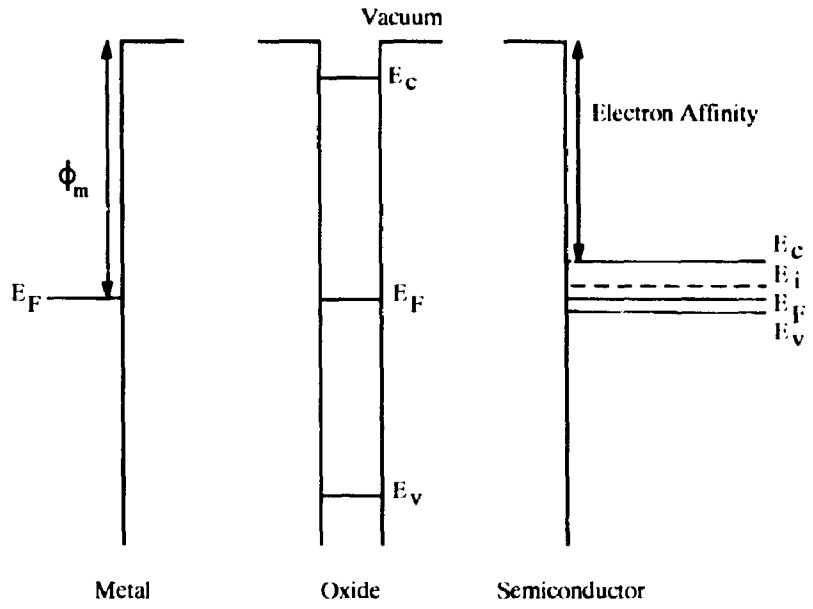


Figure 1.2 Individual Energy Band Diagram for the Different Components of the MOS Structure

semiconductor at infinity. The vacuum levels of the metal and semiconductor components must be in perfect alignment. The energy band diagram for an ideal MOS structure in equilibrium is shown in Figure 1.3.

The charge and potential distribution of MOS capacitor can be determined by solving Laplace's and Poisson's equations:

$$\nabla^2 V = 0 \qquad \text{(oxide)} \qquad \ldots(1.1)$$

$$\nabla^2 V = -\frac{\rho}{\varepsilon_{Si}} \qquad \text{(semiconductor)} \qquad \ldots(1.2)$$

where ε_{Si} = permittivity of semiconductor

V = electrostatic potential

ρ = charge density

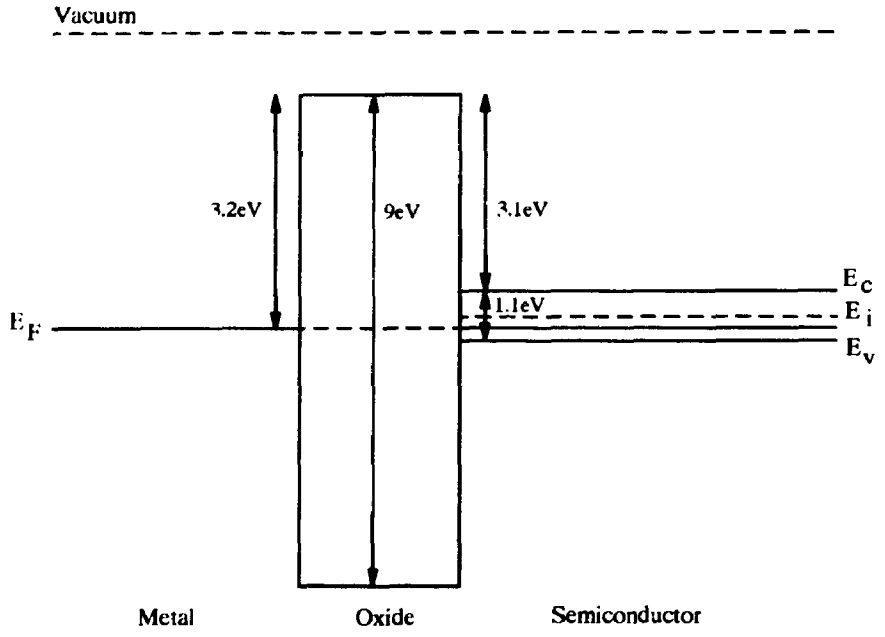
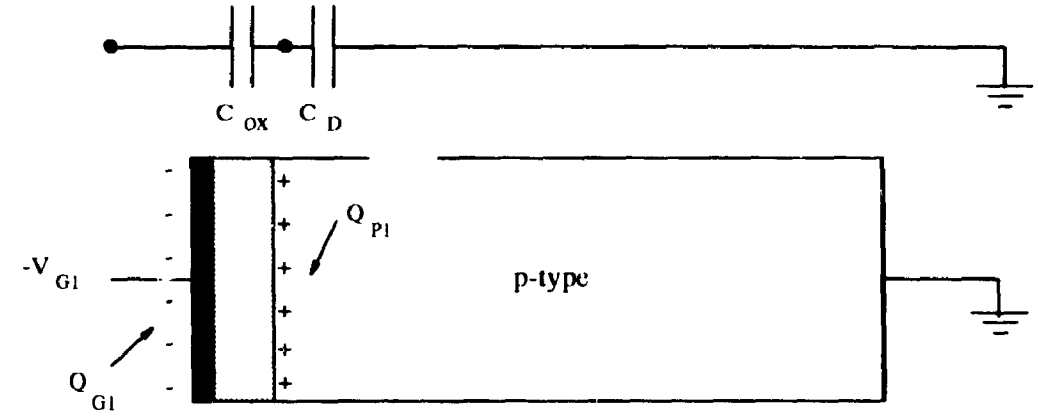


Figure 1.3 Energy Band Diagram for an Ideal MOS Structure in Equilibrium

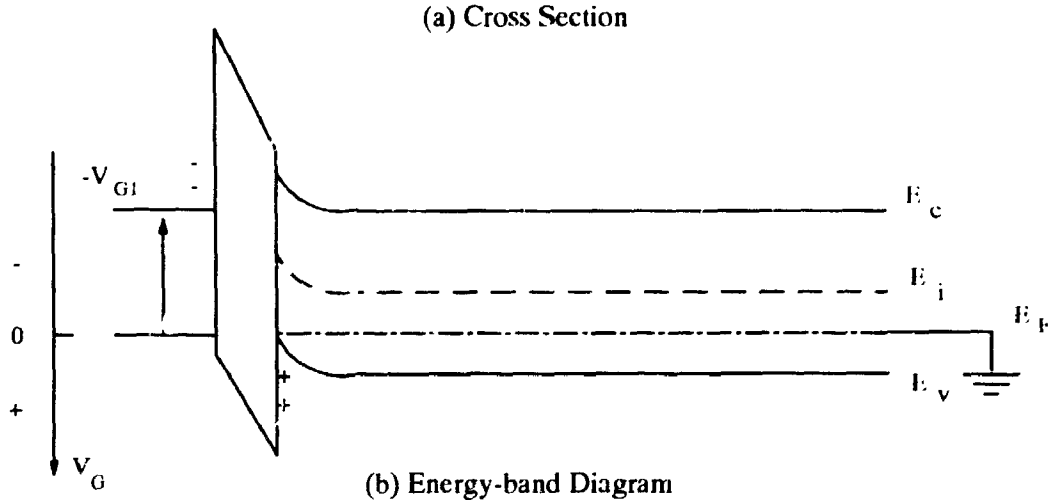
1.2.1 The Equilibrium MOS-C

Consider Figure 1.4 which shows the cross section, energy-band diagram and charge-distribution plots of a p-type substrate MOS-C under a negative gate voltage. The negative gate voltage, $-V_{G1}$, causes the gate surface to accumulate electrons. This is indicated in Figure 1.4(a) and Figure 1.4(c) by "-" and by the charge density Q_{G1}, respectively. If one assumes that the structure is ideal, *i.e.* there are zero oxide charges and interface states and no metal-semiconductor work-function difference, there will be an equal density of holes in the surface of semiconductor. This is shown in Figure 1.4(b) and Figure 1.4(c) by "+" and the charge density Q_{P1} respectively.

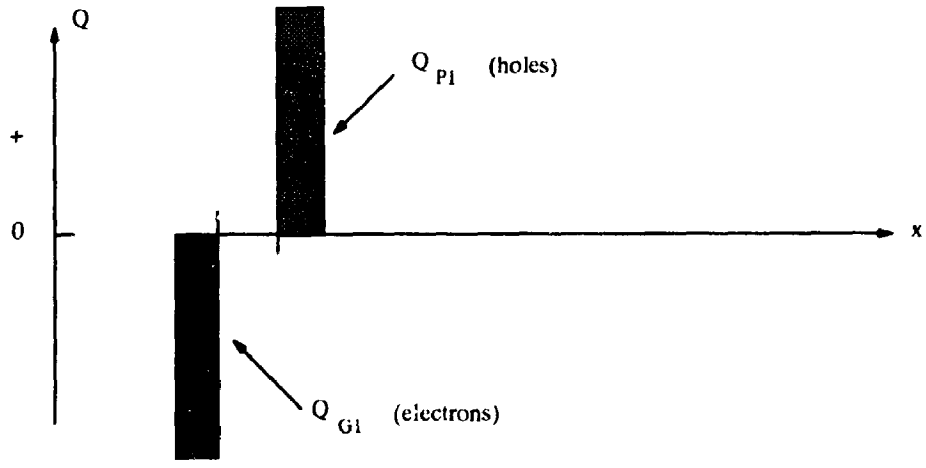
As a negative voltage is applied to the gate, the energy bands are bent upward and the majority carriers, holes in this case, accumulate near the semiconductor surface.



(a) Cross Section



(b) Energy-band Diagram



(c) Charge-distribution Plot

Figure 1.4 P-Type Substrate MOS Capacitor

An "accumulation" layer is formed underneath the gate oxide. In terms of its electrical characteristics, this MOS capacitor behaves like a parallel plate capacitor, with the gate electrode forming one plate and the substrate forming the other plate. The oxide capacitance per unit area can be calculated using Laplace's Equation [Appendix A].

$$C_{ox} = \left(\frac{\varepsilon_{SiO_2}}{d_{ox}}\right) \qquad \ldots(1.3)$$

where C_{ox} = oxide capacitance per unit area
ε_{SiO_2} = permittivity of SiO_2
d_{ox} = oxide thickness

Since there is no depletion layer formed, the depletion capacitance per unit area, C_D, is 0. Therefore, the total gate-to-substrate capacitance per unit area, C_g, of the MOS-C in the accumulation mode is C_{ox}.

$$C_g = C_{ox} = \frac{\varepsilon_{SiO_2}}{d_{ox}} \qquad \ldots(1.4)$$

where C_g = gate-to-substrate capacitance per unit area
C_{ox} = oxide capacitance per unit area
ε_{SiO_2} = permittivity of silicon
d_{ox} = oxide thickness

If the gate voltage varies from negative to positive, the behaviour of the p-type substrate MOS-C is shown in Figure 1.5 and 1.6. At a gate voltage of $-V_{G1}$, the device is in the accumulation mode and the gate-to-substrate capacitance is given by the oxide capacitance C_{ox}. This is shown in Figure 1.6(a). If the gate voltage is zero, the device

is at flatband and the capacitance is C_{FB}; no energy bands bend at flatband voltage. As the gate voltage becomes positive, i.e. at V_{G2}, the energy bands bend downward and the majority carriers are depleted. This region is called the depletion region or space-charge region (scr). The depletion region consists of negatively charged acceptor ions and an equal amount of positive gate charge. The width of depletion region, W, increases as the magnitude of the gate voltage is increased. The magnitude of the charge density per unit area in the depletion region depends on the doping concentration, electron charge and the depth of the scr. In general, the depletion capacitance per unit area, C_D, is obtained by solving Poisson's Equation [Appendix A].

$$C_D = \frac{\varepsilon_{Si}}{W} \qquad \ldots(1.5)$$

where C_D = depletion layer capacitance per unit area
ε_{Si} = permittivity of silicon
W = depletion width

The total gate-to-substrate capacitance, C_g, under depletion conditions can be approximated by the gate oxide capacitance, C_{ox}, in series with C_D.

$$C_g = \left(\frac{1}{C_{ox}} + \frac{1}{C_D}\right)^{-1} \qquad \ldots(1.6)$$

where C_g = gate-to-substrate capacitance per unit area
C_D = depletion layer capacitance per unit area
C_{ox} = oxide capacitance per unit area

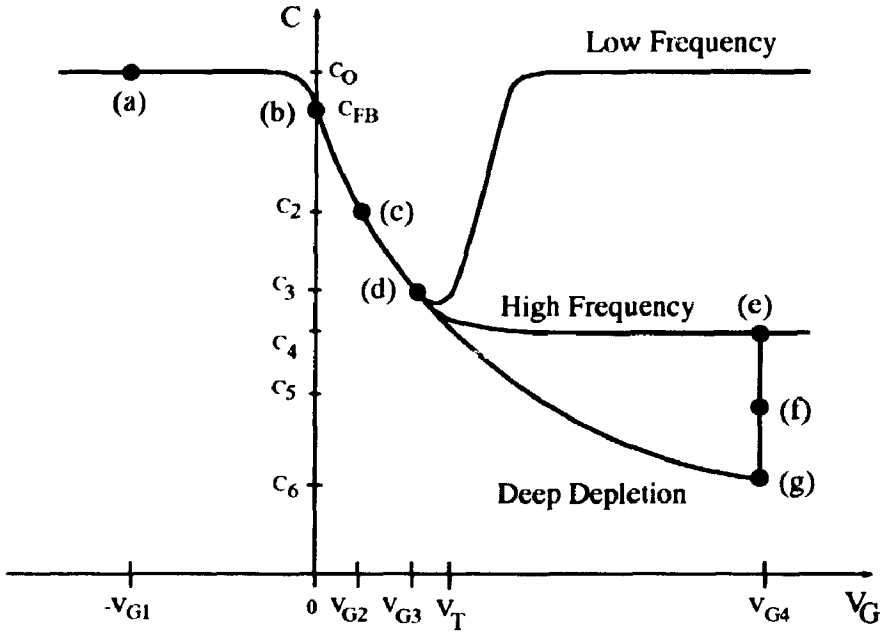


Figure 1.5 Capacitance-Gate Voltage Curves for a p-Type MOS-C

As the gate voltage increases, the energy bands bend downward and eventually the intrinsic level, E_i, at the semiconductor surface touches the Fermi level, E_F. At this particular point, the semiconductor surface is inverted, i.e. from p-type to n-type.

An additional increase in gate voltage will further bend the energy bands downward and attract more minority carriers to the semiconductor surface. The point where the intrinsic energy at the semiconductor surface moves below the Fermi energy level by one bulk potential ($\phi_B = E_i - E_F$), is called the onset of inversion. The surface electron volume concentration equals the hole volume concentration in the bulk and the corresponding gate voltage is called threshold voltage, V_T [Appendix A].

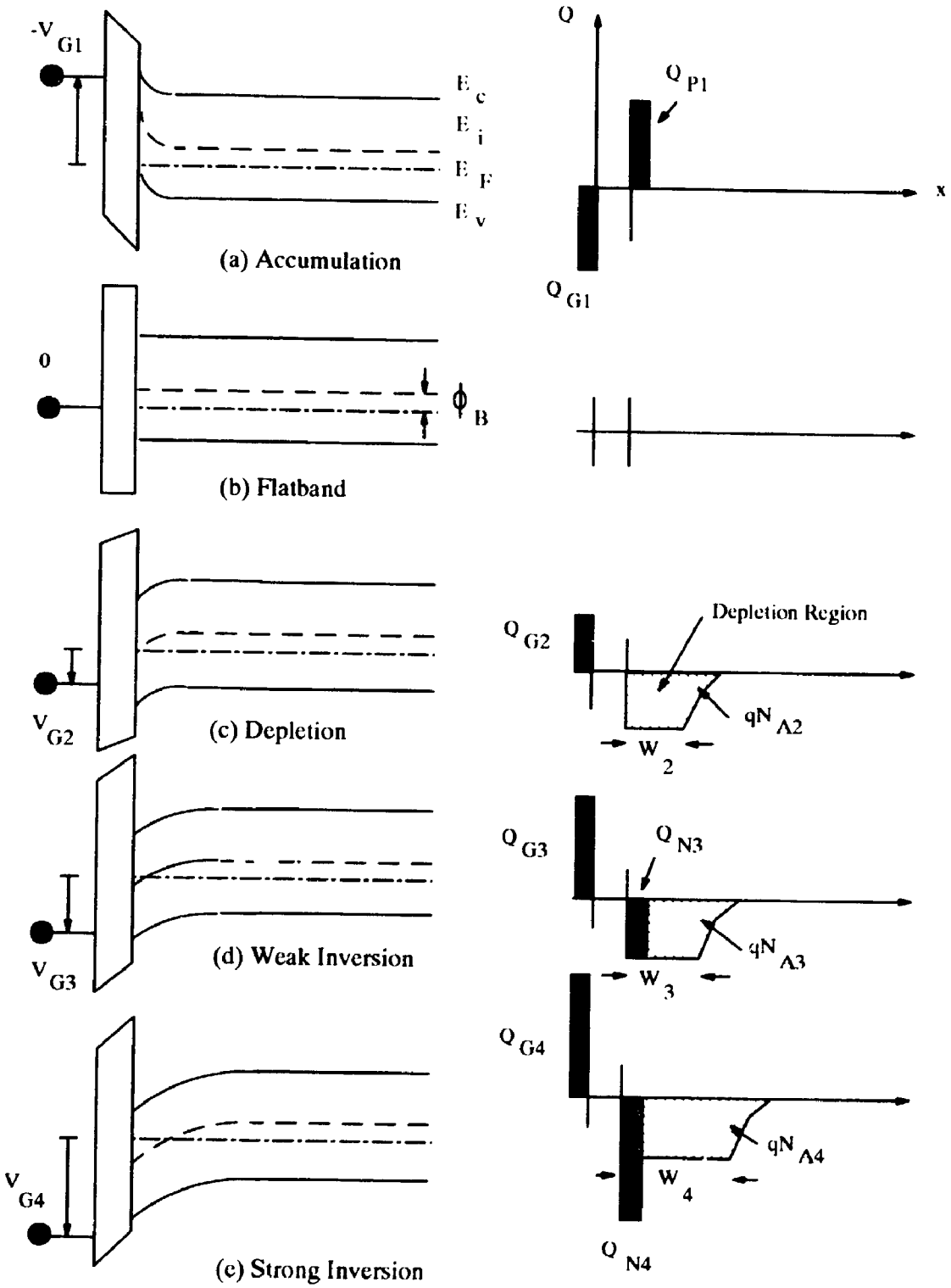


Figure 1.6 Energy-Band and Charge-Distribution Diagram for a p-Type MOS-C

$$V_T = \frac{\sqrt{4\varepsilon_{si} q N_A \phi_B}}{C_{ox}} + 2\phi_B \qquad \ldots(1.7)$$

where V_T = threshold voltage
ε_{si} = permittivity of silicon
q = charge of electron
N_A = acceptor impurity density
ϕ_B = bulk potential

A further increase in the gate voltage will attract more minority electrons towards the surface, but will not widen the depletion region significantly because the inversion layer shields the substrate from further gate voltage changes. Under low frequency conditions, the MOS-C behaves like a parallel plate capacitor, since the surface charge created by the inversion layer is able to respond to the slowly changing gate voltage. The dynamic or high-frequency capacitance remains the same as for the maximum depletion condition, since the surface charge cannot respond to the rapidly changing gate voltage.

$$C_g = C_{ox} \qquad \text{for low frequency (<10Hz)} \qquad \ldots(1.8)$$

$$C_g = \left(\frac{1}{C_{ox}} + \frac{1}{C_D}\right)^{-1} \qquad \text{for high frequency} \qquad \ldots(1.9)$$

where C_g = gate-to-substrate capacitance per unit area
C_{ox} = oxide capacitance per unit area
C_D = depletion layer capacitance per unit area at maximum depletion width

1.2.2 The Deep-Depletion MOS-C

The capacitance-voltage curve (a) to (e) or (e) to (a) in Figure 1.5 is obtained by changing the bias from negative to positive very slowly so that the capacitor under test can be considered to be in a quasi-equilibrium state. However, if a positive voltage is suddenly applied to the gate, *i.e.* during pulse excitation, majority holes are repelled from the semiconductor surface. Generation-recombination processes are not possible due to insufficient time. The device in this condition is said to be in a deep depletion (DD) mode; this is the operational condition for charge-coupled devices (CCDs). This corresponds to point (g) in Figure 1.5.

Consider the situation shown in Figure 1.7 where the capacitor under test is initially biased at zero volts. At t=0, a positive voltage, V_{G4}, is applied to the gate. At this particular moment, majority holes are repelled from the semiconductor surface; the corresponding depletion width is W_4.

From the energy-band diagrams and charge-distribution plots shown in Figure 1.8, one can discover that the Fermi level has divided into the hole and electron quasi-Fermi levels. The only minority carriers which are attracted to the surface after the voltage is applied are the ones in the depletion region before the voltage is applied. The MOS-C will return to an equilibrium state from the deep-depletion state through electron-hole pair generation. The electrons generated by this process drift to the surface and are accumulated. At some intermediate level, as shown in Figure 1.7(b), an inversion layer is formed. The capacitance, as shown in Figure 1.7, can range anywhere from C_{D4} to C_{D6} in the deep-depletion state. As this process continues, the width of the depletion region and the bulk charge, qN_{A4}, decreases as the inversion charge , Q_{N4}, increases. Finally, the capacitor is returned to equilibrium.

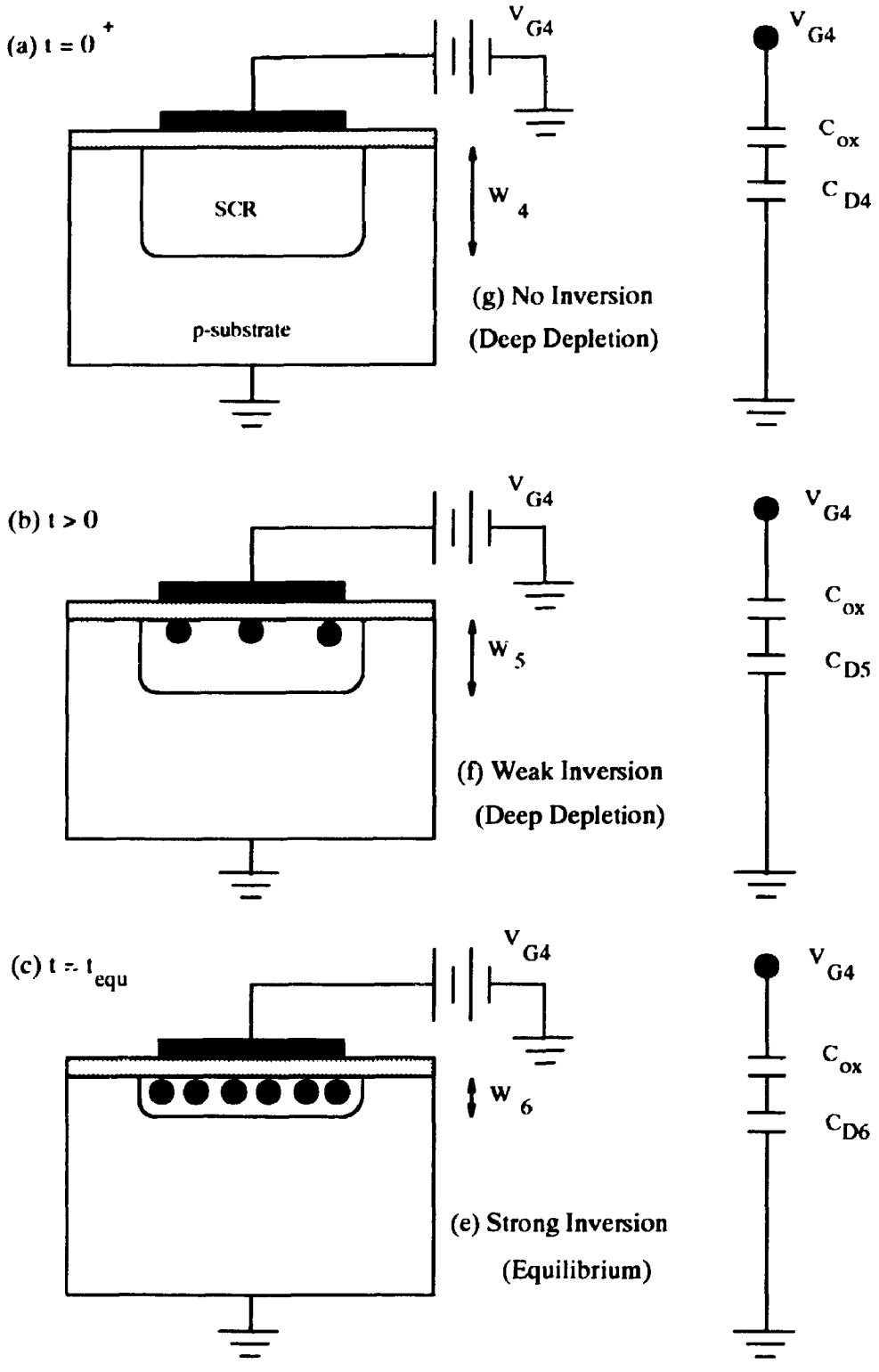


Figure 1.7 Space-Charge Region for a p-Type MOS-C in Deep Depletion Mode

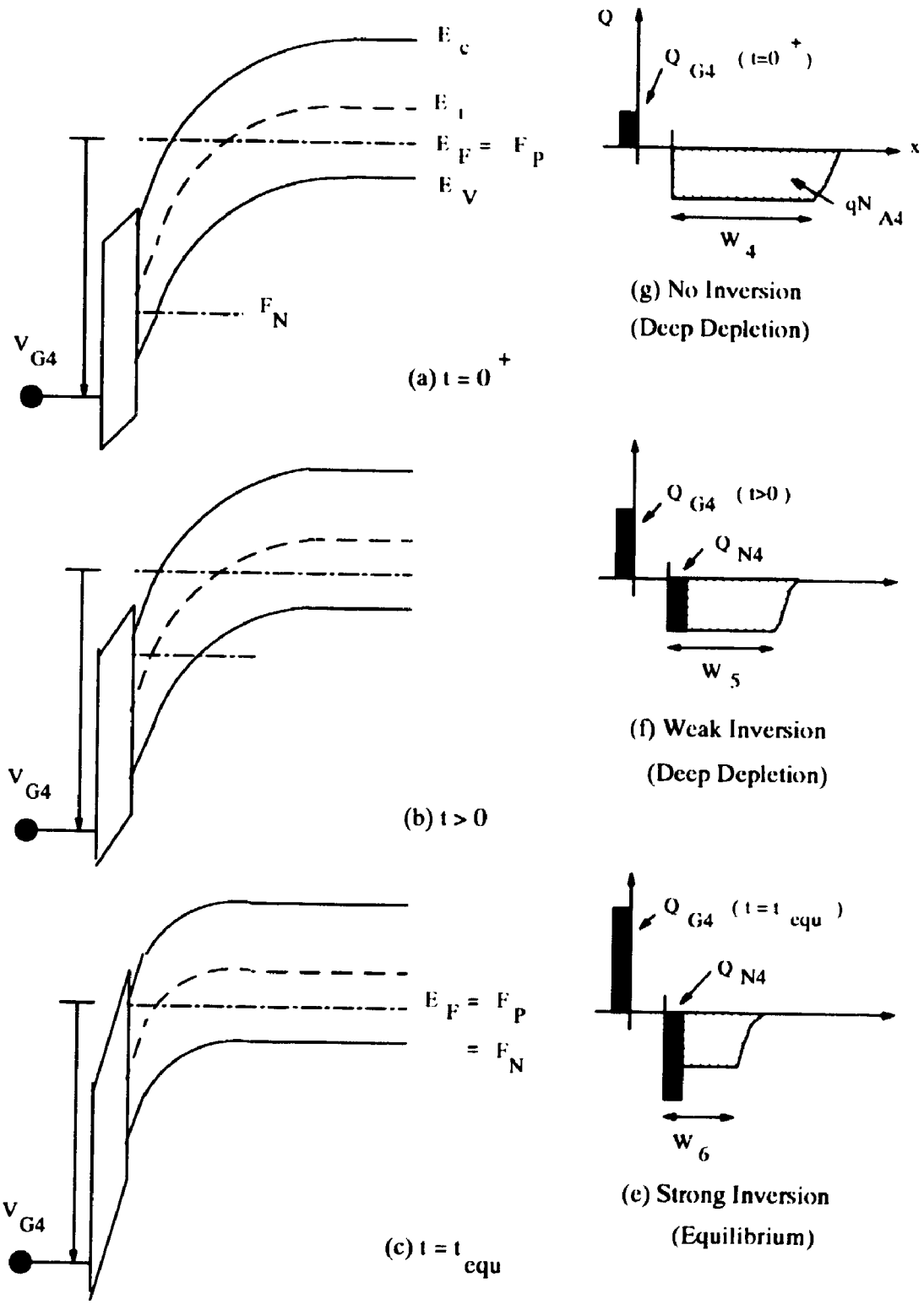


Figure 1.8 Energy-Band and Charge-Distribution Diagram for a p-Type MOS-C in Deep Depletion Mode

1.2.3 Non-ideal MOS Structures

Ideal silicon-silicon dioxide systems consist of a crystal, silicon, and a glassy material, silicon dioxide. The interface between these two materials is often characterized as a continuous random network structure because of the flexibility of silicon dioxide. In reality, the situation is more complex. Real Si-SiO_2 systems differ from ideal systems in electrical properties which are influenced by the processing technology. For example, large concentrations of hydrogen and chlorine ions often exist near the interface and cause defects in the structure.

There are two classes of trapping states in the real silicon-silicon dioxide system. Interface traps capture and release electrons and holes with time constants, at room temperature, in the range from picoseconds to hours. These affect a number of device properties, such as leakage current and MOS capacitor storage time. On the other hand, bulk oxide traps usually have very large time constants (years) and these affect device stability. If electrons or holes are captured in these traps, the charge in the oxide will change and device properties will be modified. The induced charge will last almost indefinitely.

In an ideal MOS system, there is no band bending at zero gate voltage; the flatband voltage, *i.e.* the voltage which has to be applied on the gate to achieve the flat band condition, is zero. As shown in Figure 1.9 [1][2], for a real MOS system, the work function difference, and the charges in the oxide and the traps at the Si-SiO_2 interface, can cause a non-zero flatband voltage. The flatband voltage for a non-ideal MOS system is equal to the work function difference and the voltage shift generated by the charges in the Si-SiO_2 system.

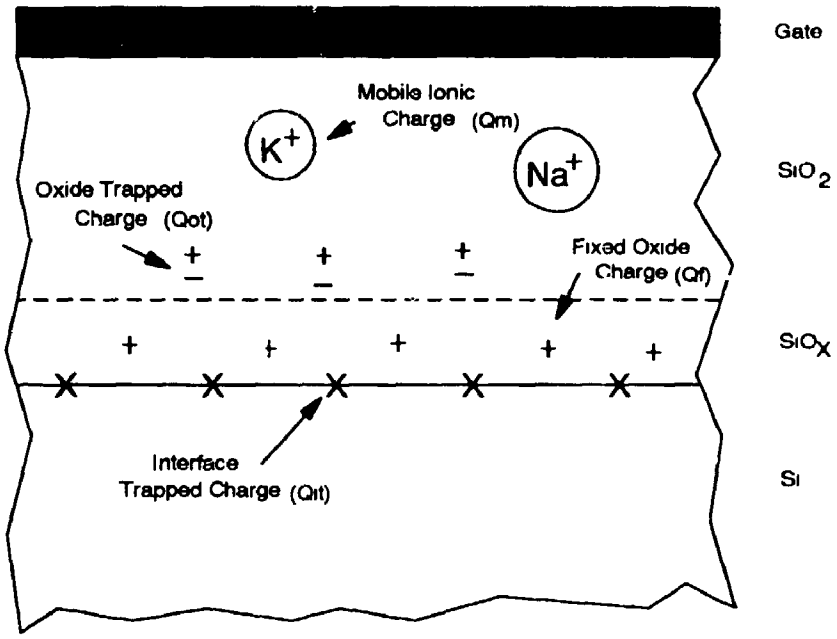


Figure 1.9 Charges in the Si-SiO_2 Interface System

$$V_{FB} = \phi_{ms} - \frac{Q_{Si-SiO_2}}{C_{ox}} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot} + Q_{it}}{C_{ox}} \qquad \ldots(1.10)$$

where
- V_{FB} = flatband voltage
- ϕ_{ms} = metal-semiconductor work function difference
- Q_{Si-SiO_2} = charges in Si-SiO_2 system
- Q_f = fixed oxide charge
- Q_m = mobile ionic charge
- Q_{ot} = oxide trapped charge
- Q_{it} = interface trapped charge

Therefore, the threshold voltage for a non-ideal MOS system is

$$V_T = V_{FB} + \frac{\sqrt{4\varepsilon_{si} q N_A \phi_B}}{C_{ox}} + 2\phi_B \qquad \ldots(1.11)$$

where V_T = threshold voltage
ε_{si} = permittivity of silicon
q = charge of electron
N_A = acceptor impurity density
ϕ_B = bulk potential

In an ideal MOS-C structure, one assumes that the semiconductor is uniformly doped. However, in practice, the doping profile in the semiconductor is seldom uniform; the dopant impurity distribution is not the same at the semiconductor surface as in the bulk. This may be caused by a dopant impurity redistribution during thermal oxidation or a diffusion/implantation of dopant ions into the surface region. The nonuniform doping profile can alter the electrical properties of the MOS-C structure. A review of the effect of various dopant impurity distributions, namely uniform, linear and exponential, on the threshold voltage of a basic p-type substrate MOS-C is discussed in Appendix A. The theoretical analysis presented in this thesis assumes an uniform distribution; the exact distribution, if required, could be obtained from the results of C-V measurements.

1.2.3.1 Silicon-Silicon Dioxide Interface Traps

Real $Si\text{-}SiO_2$ systems differ from ideal systems in various ways. The occurrence of different defects depends on the processing technology. The defects in the

interface can be caused by fixed oxide charges, interface trapped charges, oxide trapped charges and mobile ionic charges. The interface charges are shown in Figure 1.9.

1.2.3.1.1 Fixed Charges

The fixed charge is positive and located at the interface. It is independent of the oxide thickness, the semiconductor doping concentration and doping type. The fixed charge varies as a function of the Si surface orientation. Studies [1] have found that it is largest on {111} crystal surfaces and smallest on {100} crystal surfaces. The ratio of the fixed charge on the two surfaces is approximately 3:1. It affects the threshold voltage of the MOS transistor and the flatband voltage of MOS capacitors because it alters the semiconductor surface field. The fixed charge is usually very stable, not affected by hydrogen or water vapor in the oxidation, by annealing atmospheres, or by low-temperature hydrogen annealing. The fixed charge is controlled by device fabrication processes.

1.2.3.1.2 Interface Traps

Interface traps are electron or hole capture sites located at the silicon-silicon dioxide interface, with energy levels positioned inside the silicon forbidden gap. Interface traps are allowed energy states in which electrons or holes are localized in the vicinity of a material surface. Although detailed models for the electrical behaviour of the interface traps exist, the physical origin of the traps has not been satisfactorily explained. Experiments have shown that the interface traps arise primarily from unsatisfied chemical bonds at the surface of the semiconductor. The silicon lattice is disrupted at the Si-SiO_2 interface and some Si-surface bonds are

created, becoming the interface traps. The model of interface traps is shown in Figure 1.10 [3]. Filling of the interface traps is illustrated in Figure 1.11; the total amount of charge in these traps depends on the surface potential.

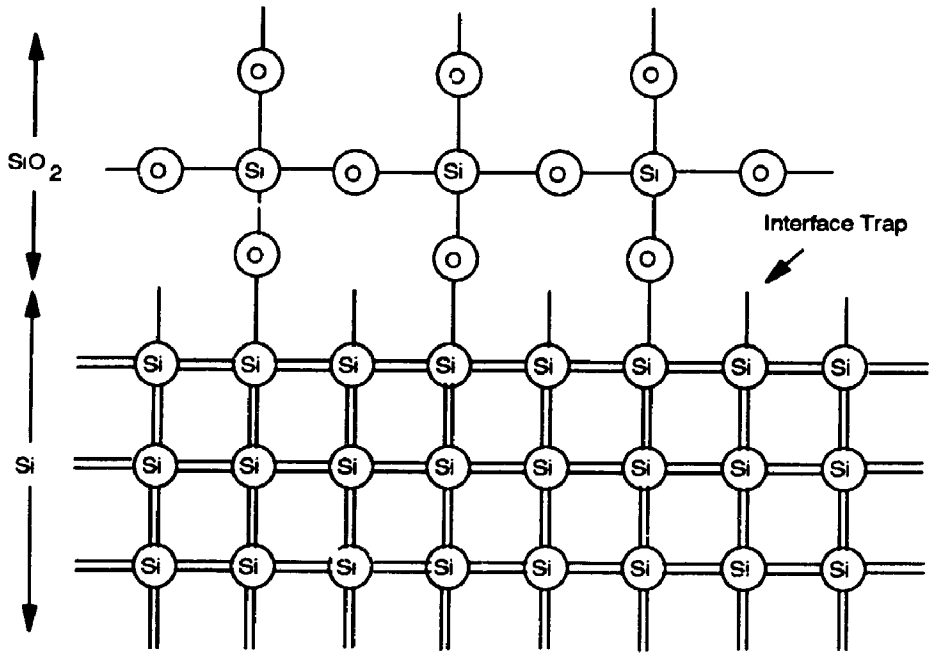


Figure 1.10 Physical Model of Interface Traps

The interface traps affect device characteristics in many ways. For example, the operation of a MOS transistor requires induction of charge carriers in the channel. However, in the presence of interface traps, some of the induced charges are captured by the interface traps, becoming thus unavailable to the current transport mechanism, as shown in Figure 1.12. Transistor gain decreases, since current versus voltage curve of the transistor is shifted along the voltage axis and becomes less steep. For MOS capacitors, this time dependent trapping phenomenon results in time or frequency dependent CV curves. The interface traps act as generation-recombination centres that affect all silicon devices and increase leakage

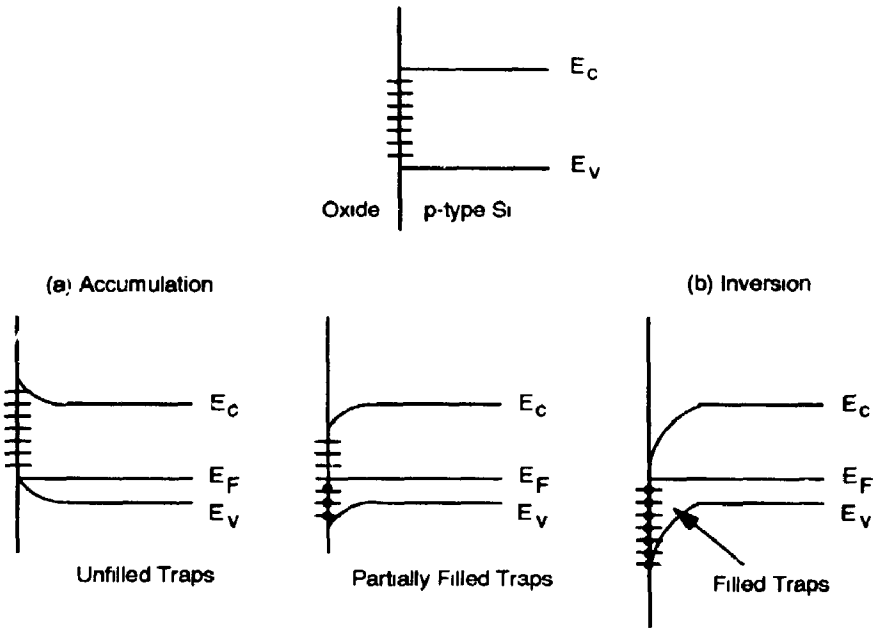


Figure 1.11 Electrical Model of Interface Traps

current in transistors, increase the loss in charge-coupled devices and increase noise.

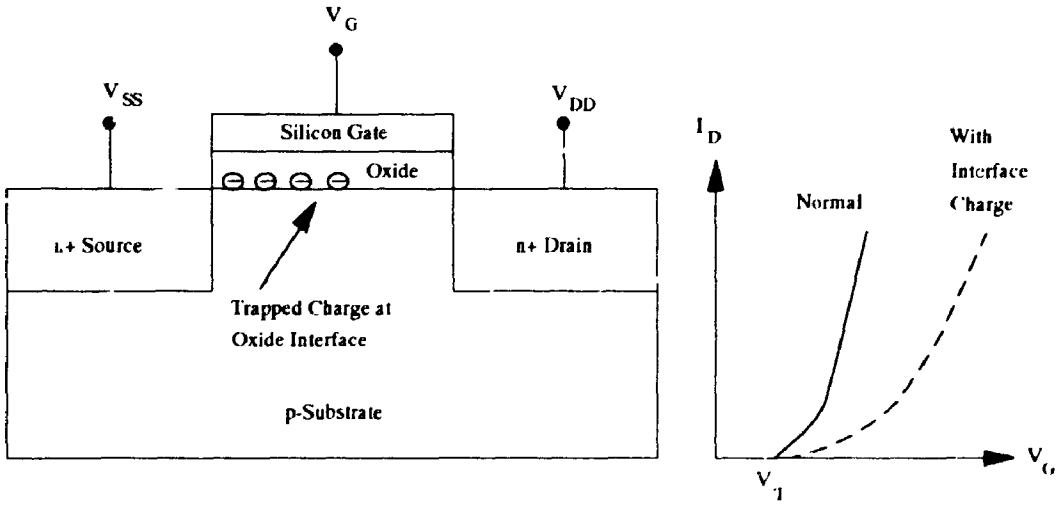


Figure 1.12 Charge Trapping by Interface Traps

1.2.3.2 Bulk Oxide Traps

The existence of bulk oxide traps is related to defects in this material. The oxide often has a large defect density near the interface because this is the first area reached by the electrons or holes injected from the substrate or the gate electrode.

In general, carriers can be injected into the bulk/oxide by photogeneration or hot-carrier injection. In the photogeneration process, electron-hole pairs are generated as a result of photon absorption. Since the bandgap of the silicon dioxide is about 9eV, photons with a wavelength of at least 130nm ($\lambda = hc/E$), are required for this process. Radiation usually has higher energy and, therefore, bulk generation and carrier trapping is mostly caused by the radiation effect. Other phenomena, such as electrical overstress/electrostatic discharge (EOS/ESD), can also result in induced charges in the bulk/oxide. Charges captured during these processes can create more interface traps and oxide traps because the primary charge may release considerable energy upon trapping. For example, if the charge originates from an electron-hole pair in the oxide with a latent energy of about 9eV, it may release up to 9eV upon recombination. Experiments [3] have shown that photons of 10eV energy (ultraviolet) are absorbed very effectively in the outer 30nm layer. For energy ranges from 3 to 10eV, the absorption is throughout the whole oxide. For ultrahigh energy photons, oxide damage, such as atom displacement and the generation of electron-hole pairs, can occur.

Similarly, if photons with an appropriate energy are absorbed in the semiconductor, they may excite electrons to an energy high enough for the electron to escape into the oxide conduction band. Usually photons of 3 to 5eV are needed to exceed the energy barrier.

Hot-carrier injection, as shown in Figure 1.13, occurs in cases where charge carriers are accelerated towards the interface in a high field region in the silicon. The charge carriers can be initiated by illumination, avalanche breakdown or high electric fields. The injection of holes occurs by a similar mechanism. Since the energy barrier for holes (about 5eV) is much higher than for electrons (about 3.1eV), it requires more energy to initiate the hole injection process.

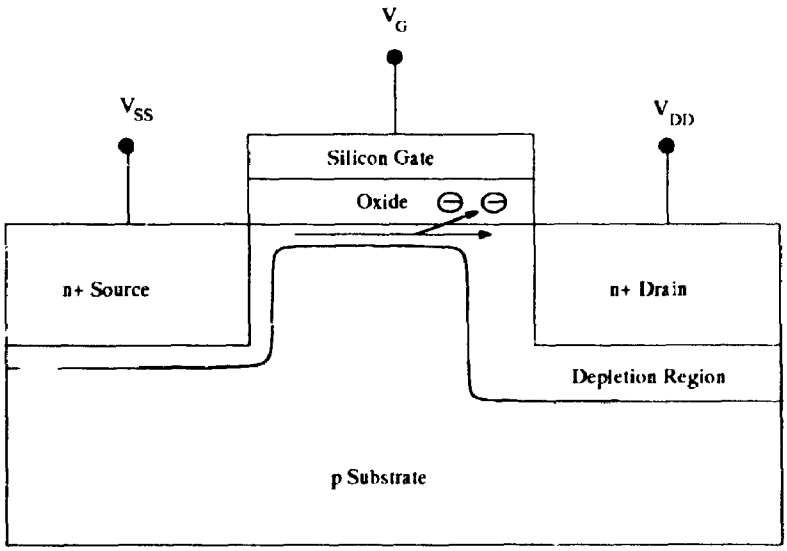


Figure 1.13 Hot-Carrier Injection

Charge injection and trapping can lead to oxide charging and cause MOS threshold voltages to change. Since the oxide is a good insulator, the trapped charges may be very stable and can lead to secondary phenomena such as the creation of additional interface traps and oxide traps.

1.3 Fundamentals of Charge-Coupled Devices (CCDs)

The fundamental structure of a CCD consists of a MOS capacitor (MOS-C), as shown in Figure 1.14, which operates in the deep-depletion region. When voltage is suddenly applied to the electrode and substrate, a depletion layer is created; if charges are now injected into this depletion layer, they will be temporarily stored and "memorized" as analog quantities.

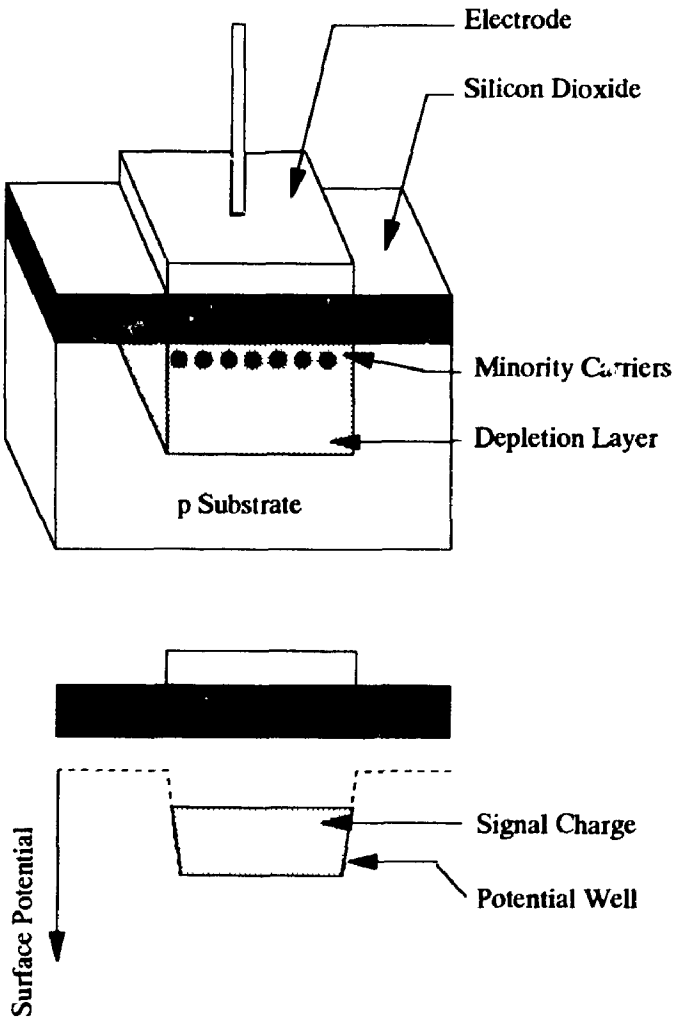


Figure 1.14 Basic Structure of a MOS-C

1.3.1 Input Configuration of CCDs

A charge coupled device is operated as an analog shift register which stores a signal in the form of charges on a series of capacitors. The transfer of charge from one capacitor to the next is controlled by an applied voltage pulse. This concept of charge transfer is illustrated in Figure 1.15 [4] that shows a series of closely spaced MOS capacitors fabricated in a p-type substrate. The charge packet is stored under the gate with the highest potential. By placing the storage elements, *i.e.* the MOS capacitors, adjacent to each other, voltages on the gate electrodes can be raised and lowered sequentially which causes the individual charge packets beneath them to be passed from one storage element to the next.

The charge is injected or removed from the depletion well by the n-type diffusion areas located at both ends of the capacitors. To inject charge, the phase one clock is held at positive potential while the phase two and three clocks are held at zero. This creates a surface potential shown in Figure 1.15(a). The input diode is initially reversed biased, then briefly grounded. During the sequence, the minority carriers flow from the diode region to the depletion well under the phase one electrode. The well under the phase one electrode "fills" with charge and overflows. This corresponds to Figure 1.15(b). When the diode is returned to a positive potential, any charge above the V_{G1} surface potential level "spills" back into the diode. The charge injected into the well is determined by the difference between the phase one clock and the input gate voltage. Similarly, the signal charge can be detected by a MOSFET connected to the output diode.

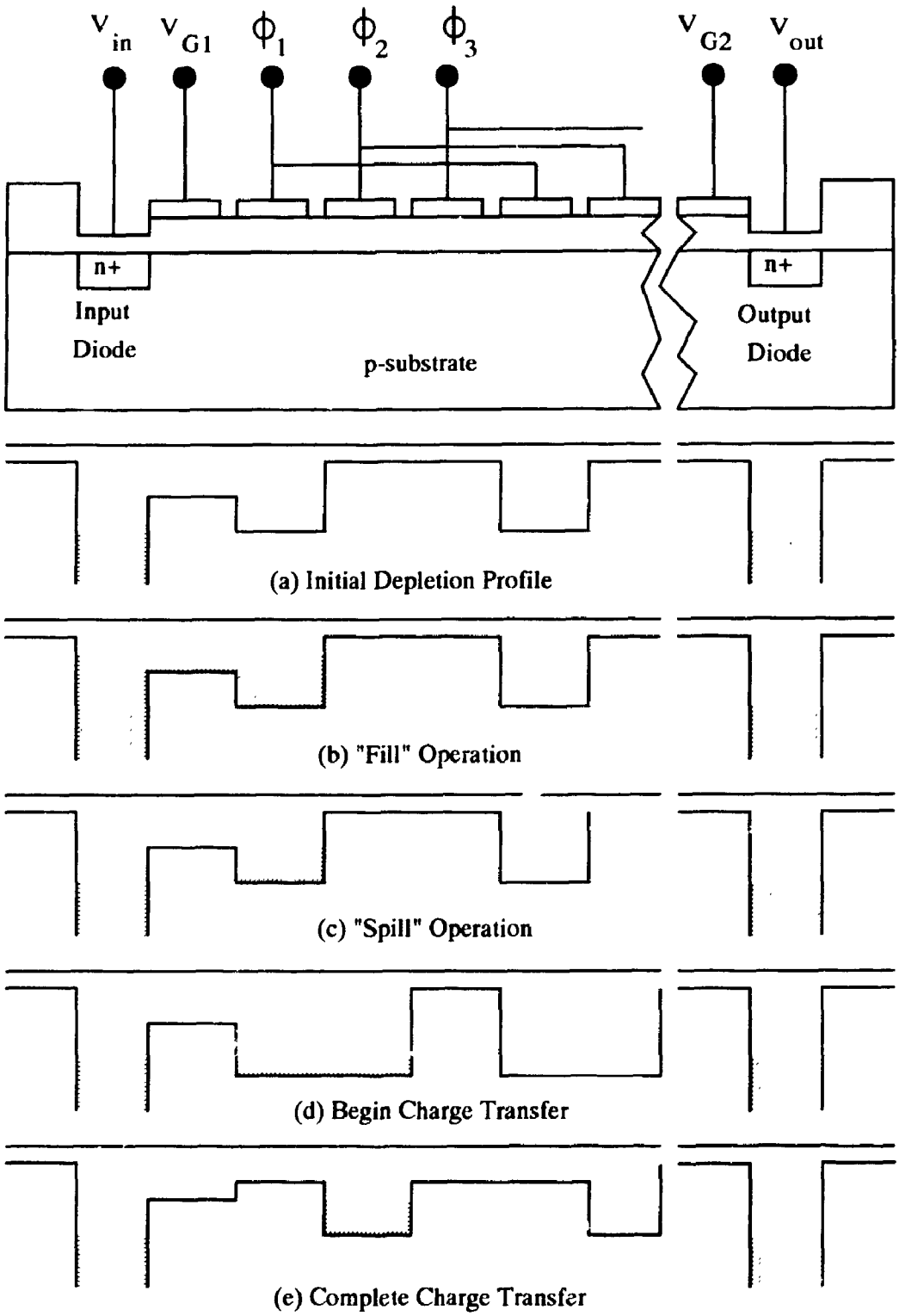


Figure 1.15 Operating Principle of a 3-Phase CCD

1.3.2 Multiphase CCD Structures

As shown in Figure 1.15, the minimum number of phases required to achieve a directional charge flow in a CCD with uniform oxide thickness is three. However, this scheme suffers from certain drawbacks. In order to prevent the stored charge from being transferred backwards or injected into the substrate, the fall time of the clock must be carefully controlled. A four-phase CCD eliminates some of these problems and can be effected by two different clock types. The first clocking scheme, similar to the one in a three-phase CCD, shown in Figure 1.17, can be implemented by using two flip-flops. The second clocking principle, as shown in Figure 1.16, is easier to implement because ϕ_3 and ϕ_4 are the inverse of ϕ_1 and ϕ_2. Moreover, the fall time requirement is relaxed and the charge storage capacity is approximately doubled. Using two layers of polysilicon, gap problems can be eliminated by the overlapping gate structure.

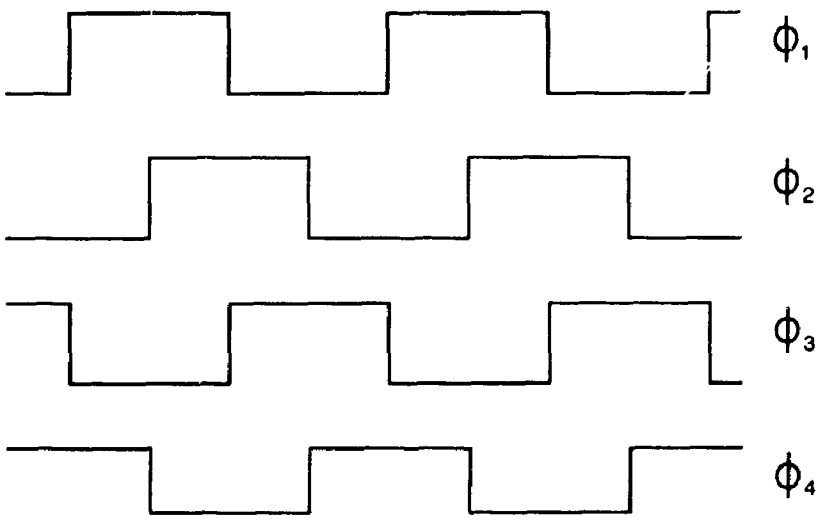


Figure 1.16 Operating Principle of a 4-Phase CCD with an Alternative Clocking

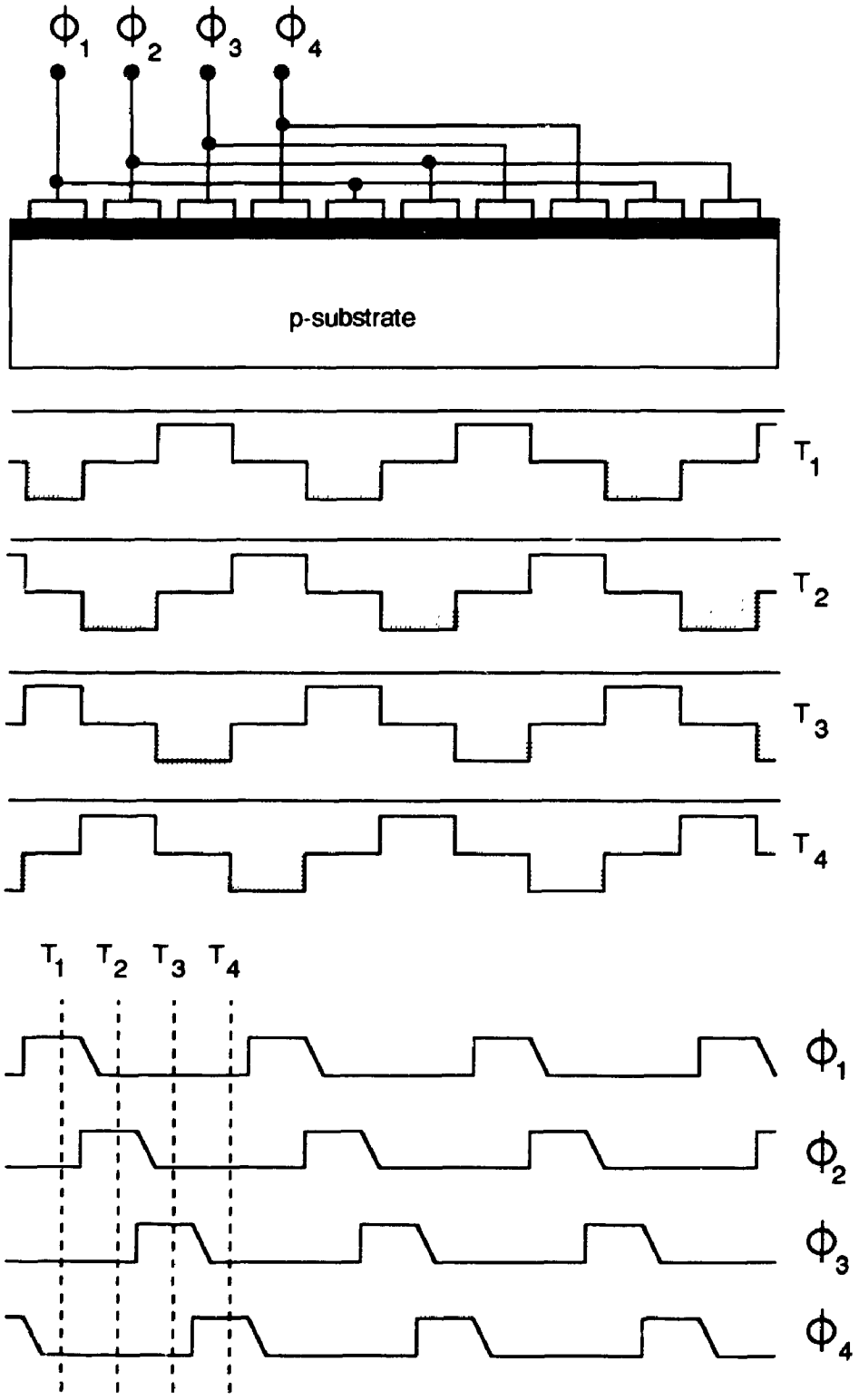


Figure 1.17 Operating Principle of a 4-Phase CCD

By varying the oxide thickness or heavily doping the region under half of each gate, a two-phase CCD can be implemented using the structure asymmetry. This basic structure and the operating principle of a two-phase CCD are shown in Figures 1.18 and 1.19 respectively.

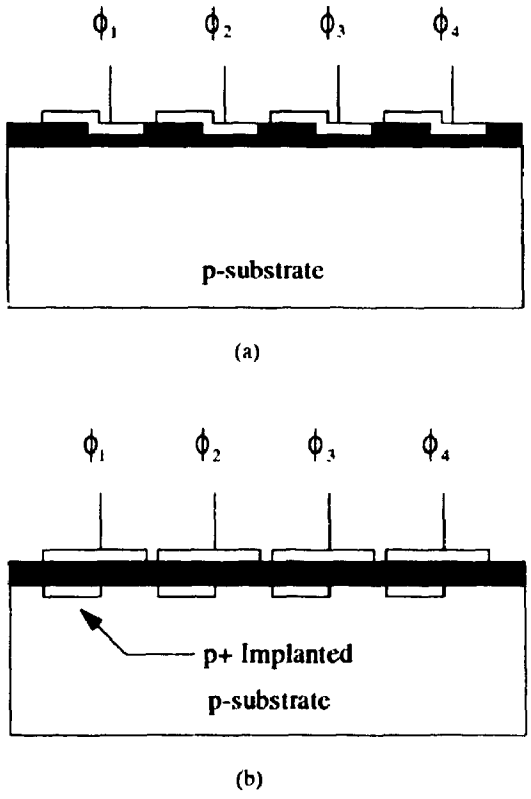


Figure 1.18 Basic Structure of a 2-Phase CCD

As shown in the preceding analysis, in a three/four-phase CCD with uniform oxide thickness, the direction of charge flow is externally controlled by the clocking scheme and can be bi-directional whereas an asymmetrical two-phase CCD is undirectional. The main differences between two and four-phase CCDs characteristics are summarized in Table 1.1.

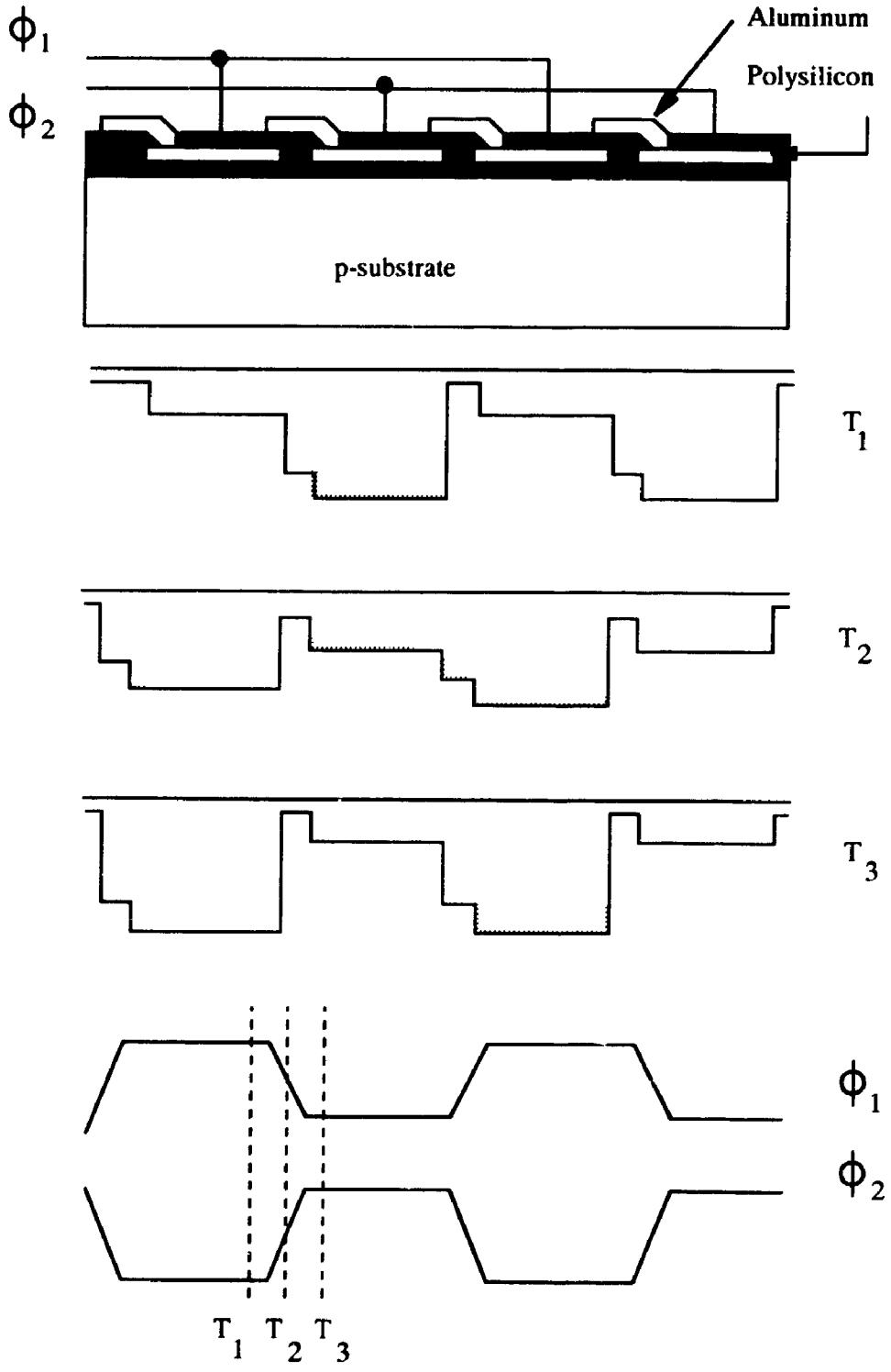


Figure 1.19 Operating Principle of 2-Phase CCD

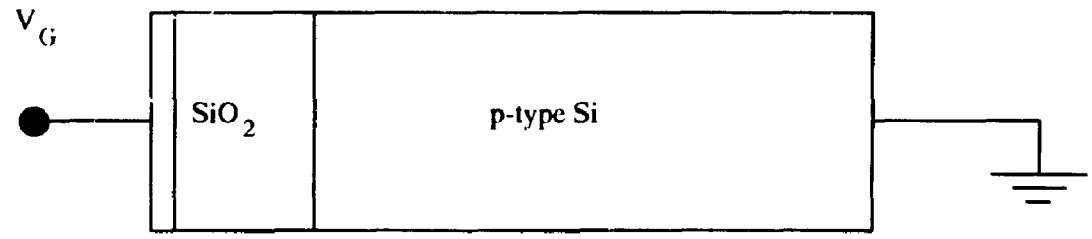
Table 1.1 Advantages of Two and Four Phase CCDs

Characteristics	Two-Phase	Four-Phase
High Charge Handling Capacity		*
High Dynamic Range		*
High Clocking Frequency	*	
Drive Circuit Simplicity	*	
Bidirectional Transfer Capability		*

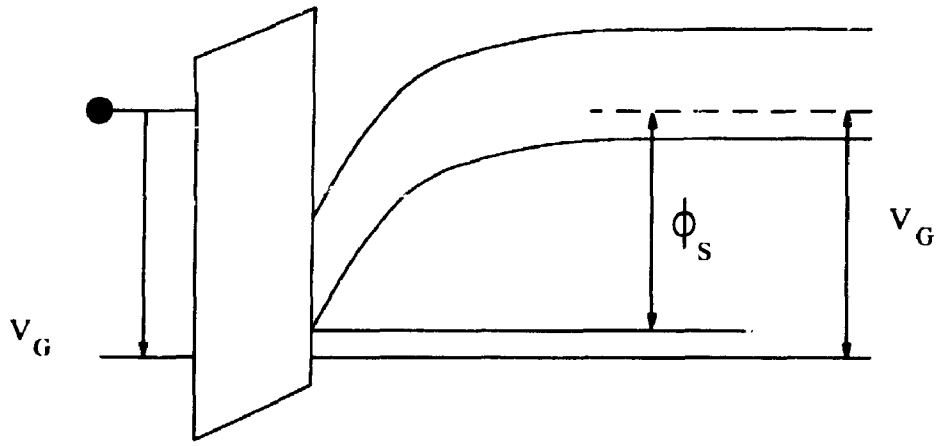
1.3.3 Surface and Bulk Channel CCDs

A surface channel CCD, shown in Figure 1.20, has a uniformly doped substrate. When the gate is biased, a depletion region is formed beneath the oxide layer. The lowest energy state for a photoelectron is at the oxide-substrate interface. Charges reside at the semiconductor surface as minority carriers and are exposed to the silicon-dielectric surface states. Since interface states act as active generation-recombination centres, some of the charge will be captured as charge packets are transferred through the device and cause charge loss or imperfect transfer efficiency.

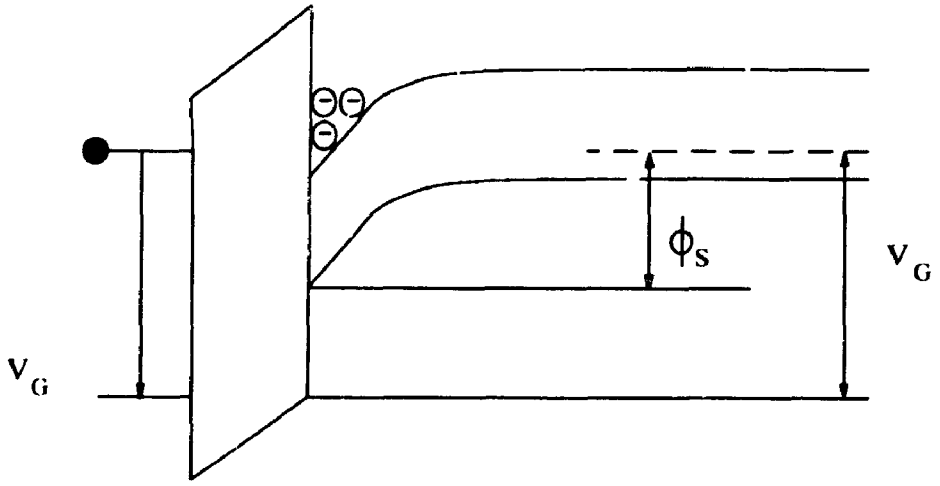
The problems encountered by the surface channel CCD devices can be solved by moving the charge packets away from the surface into a buried n-channel as illustrated in Figure 1.21. In this case, the charge packets reside as majority carriers and interact



(a) Cross-sectional View of a Surface Channel MOS-C



(b) Potentials Insider MOS-C (No Charge Packets)



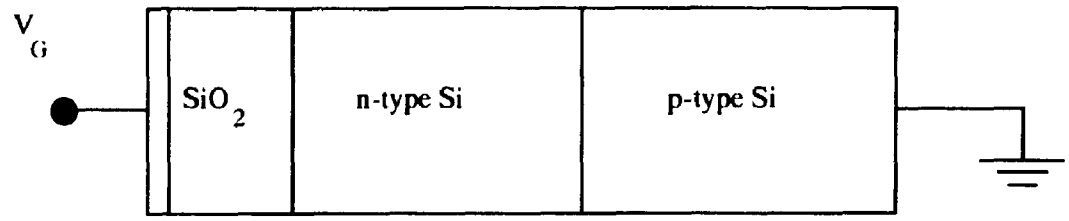
(c) Potentials Insider MOS-C (With Charge Packets)

Figure 1.20 Surface Channel CCD

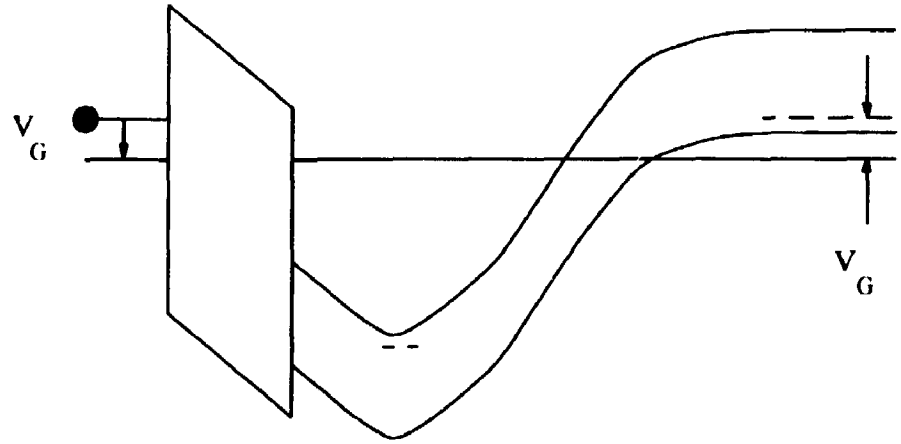
with the bulk generation-recombination centres. Usually, the bulk oxide traps can be more easily controlled than the silicon-silicon dioxide interface traps. For buried channel CCDs, the n-channel island is fabricated by ion implantation or epitaxial growth process, and the thickness is usually less than one micron.

As shown in Figure 1.21, a buried channel MOS structure has a thin n-type doped layer between the oxide interface and the p-type substrate. Therefore, the potential gradient beneath the biased gate reaches a maximum value within the n layer. Photoelectrons will reside in the lowest energy state which corresponds to the bottom of the potential wells and is inside the n zone. This means that the charge consists of majority instead of minority carriers and resides in the bulk, resulting in higher device performance.

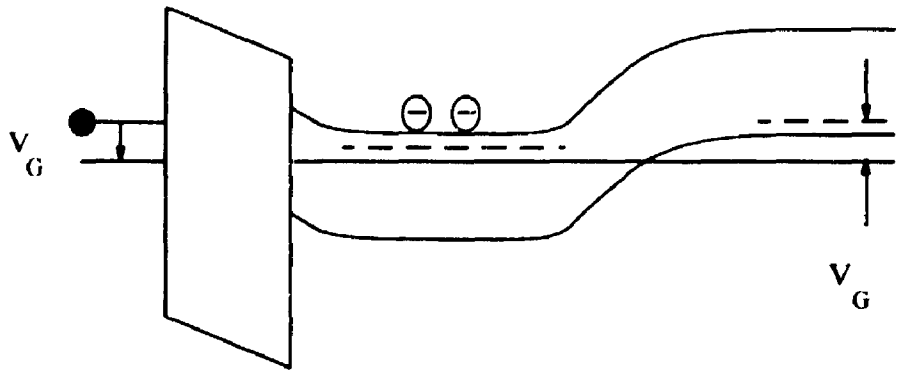
Although the bulk channel CCD increases the fabrication complexity and decreases the charge handling capacity, almost all of today's devices are BCCDs due to their enhanced performance. The characteristics of buried and surface channel CCDs are tabulated in Table 1.2.



(a) Cross-sectional View of a Bulk Channel MOS-C



(b) Potentials Insider MOS-C (No Charge Packets)



(c) Potentials Insider MOS-C (With Charge Packets)

Figure 1.21 Bulk Channel CCD

Table 1.2 Characteristics of Buried Channel and Surface Channel Structures

Characteristic	Buried Channel	Surface Channel
High Transfer Efficiency	*	
High Operating Frequency	*	
Low Intrinsic Noise	*	
Large Charge Handling Capability		*

1.3.4 Output Structure of CCDs

The signal charge is converted into voltage by means of a source-follower MOSFET connected to a floating n+ island. The output circuit, shown in Figure 1.22, consists of an output gate, a source-follower MOSFET connected to a floating diffusion, a reset gate (RS) and a voltage biased drain. An initial short reset pulse is applied to the reset gate to ensure the floating n+ island remains at V_D. Shortly afterwards, the surface potential of the output gate V_G is lowered to allow the signal charge to flow into the floating n+ island and is converted into a voltage by the source-follower MOSFET.

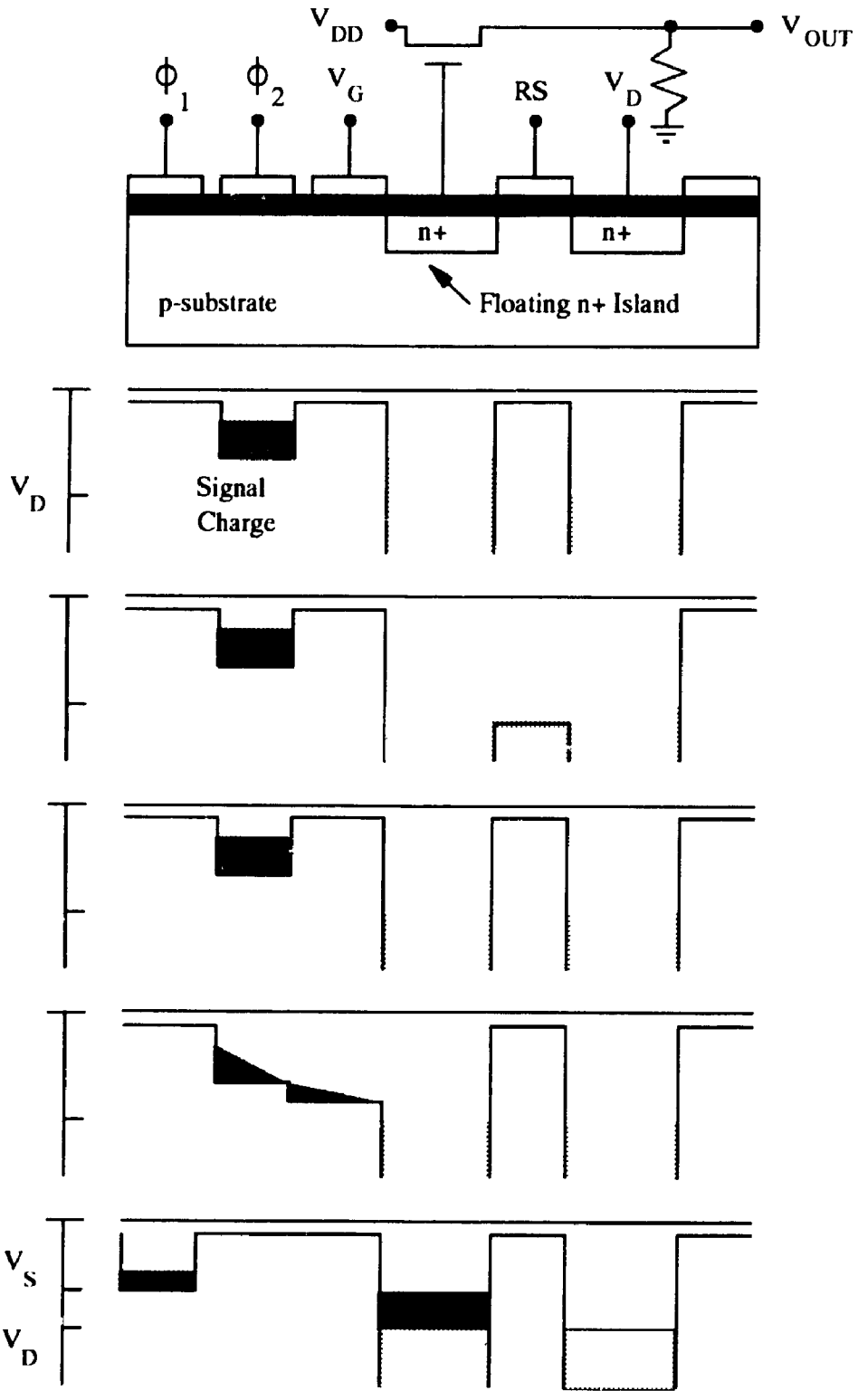


Figure 1.22 Output Structure of CCDs

1.4 Summary

In principle the CCD array is a MOS structure consisting of parallel capacitors (MOS-C) with diodes at the input and output that inject or detect the capacitor charges. Since the MOS capacitor (MOS-C) is the heart of the CCD device, its thorough understanding is important. In this chapter, the device physics of a MOS-C essential for CCD operation has been discussed. The charges associated with the silicon/silicon diode interface, surface states and the bulk are also studied. For MOS-C, the gate is separated from the rest of the circuit by a gate oxide; the input capacitance is very high and can be easily damaged by Electrostatic Overstress (EOS) or Electrostatic Discharge (ESD). In fact, CCDs are classified by the DOD-HDBK-263 [5] as the most susceptible device during EOS/ESD. The configuration of CCDs is similar to that of standard MOS devices and the failure mechanisms of MOS devices are also common to CCDs. In order to fully understand the nature these failure mechanisms, one must perform experiments at the chip and device levels, i.e. CCDs with input and output pads. The performance and reliability of the I/O pads are equally as important as those of the CCDs. A more detailed discussion on the failure mechanisms of MOS devices is presented in chapter 2.

1.5 Project Objectives

For a number of years, concerns have been expressed that low level electrical overstress and electrostatic discharge (EOS/ESD) can generate hidden damage in semiconductor devices. This type of "latent" damage can be defined as a flaw in the structure that is not apparent at the time of its onset, but that will reveal itself by facilitating a hard failure at a subsequent, normally nonfatal discharge stress to which the device is subjected during ordinary use. Accumulated statistical evidence supports the concerns, and mechanisms have been proposed explaining several simple types of latent damage, such as those associated with the semiconductor-dielectric interface or those related to packaging. However, explanations of the more complicated latent failure causes have remained controversial and leave much space for a more rigorous approach combining experiment and theory.

The fundamental objective of this project was to study the reliability of microelectronic structures with emphasis on latent failure mechanisms in CMOS CCDs, subjected to EOS/ESD. Since CCDs are classified as the most susceptible device during EOS/ESD, a model of the latent failure mechanism was postulated, formulated mathematically and verified by measurements in which protection circuit elements, CCDs and related designs were used as test devices. In addition, a more advanced failure analysis instrumentation method was devcloped to study and analyze microstructures in the failure region and their vicinity.

Chapter 2

Failure Mechanisms in Metal-Oxide-Semiconductor (MOS) Devices

This chapter describes various techniques used in the failure analysis of semiconductor devices. It begins with a discussion of the different failure mechanisms in semiconductor devices and the causes associated with these failures. Finally, various analytical techniques used in the experiments are presented.

2.1 Introduction

Failures in electronic components are an important issue. As the trends in the technology are towards higher complexity of components, increased packaging densities and thinner dielectric layers between active elements, the demand for higher reliability becomes more and more difficult to achieve. The submicron technology design and fabrication processes have resulted in structures which are more susceptible to failures, such as thermal and voltage failure modes associated with electrostatic discharge (ESD).

In most cases, failure models are used to estimate the expected lifetime or reliability of a component. However, developing a viable reliability model is not an easy task. For example, the estimation of reliability is obtained via various modelling methods which, in turn, are based on laboratory or field data. One drawback of this analysis is that it does not provide the cause of failure and the data obtained are only as good as the failure analysis of the defective devices. Therefore, the essential

requirement of the analysis is to study the failure mechanisms of the process. By understanding the conditions and the physics of these processes, one can then improve the reliability of components.

2.2 Failure Mechanisms

The failure mechanisms in semiconductor devices can be classified into three main categories, namely (1) electrical stress related failure mechanisms; (2) intrinsic failure mechanisms; (3) extrinsic failure mechanisms.

2.2.1 Electrical Stress Related Failure Mechanisms

These types of failures are usually caused by electrical overstress (EOS) and electrostatic discharge (ESD). The term electrostatic discharge refers to the sudden transfer of charge between objects at different electrostatic potentials. A familiar example is the spark generated when a person walks across a synthetic carpet on a dry day and then touches a metal door knob. Although this event seems insignificant and can occur frequently, it can have serious and harmful effects on microelectronic devices. For example, studies have shown that the minimum potential for a person to feel the discharge is about 3kV; during this discharge, the energy of several hundred microjoules is transferred from the metal doorknob to the human body. If an integrated circuit is in the path of this discharge, a current of several amperes will flow through the circuit's tiny silicon junction, gate oxide and interconnections. This is more than enough to melt silicon, rapture oxide layers, fuse the interconnection aluminum metallization, cause polysilicon to evaporate, create electromigration and change the surface state of the device. EOS/ESD can cause voltage and current induced failures. Voltage induced failures can cause dielectric breakdown predominantly in MOS

devices because the inputs of MOS devices are directly connected to gates which are separated from the rest of the circuit only by a thin gate oxide. The silicon dioxide will break down when electric fields are in the 5MV/cm to 10MV/cm range. For a typical 3 micron CMOS process with a 500 Å gate oxide, the oxide breakdown voltage is between 25V to 50V (or less because of oxide imperfections). These voltages are much lower than those due to the static charge build-up in a typical working environment. On the other hand, current induced failures are dominant in bipolar devices, where EOS/ESD creates hot-spots at a particular point in a semiconductor junction, due to an increase in current flow. As the junction temperature increases resistivity decreases and more current flow results which in turn heats the junction further.

Electrostatic charge can be generated by either triboelectrification or induction processes. Triboelectric charging occurs whenever two different materials come into contact and are then separated. The amount of charge transferred after contact and separation depends on the contact potential difference which exists at the time of contact; contact potential difference is proportional to the difference in work functions. The material with the higher work function becomes negatively charged while the material with the lower work function has an equal but opposite positive charge. If the materials are insulator/insulator or insulator/metal, the charge becomes trapped in surface states near the surface of the insulator during contact. After separation, the materials are left with equal but opposite charges. However, if two metals interact no charge is trapped and no net charge remains on either metal after separation, because of the charge "backflow" process. A material at the top of the triboelectric series table,

shown in Table 2.1 [5], will tend to charge positively with respect to materials below them because of their lower work function value. From Table 2.1, it is of interest to know that both insulators and conductors can be charged.

TABLE 2.1 Triboelectric Series

Material	Polarity	Material	Polarity
Air	+	Sealing Wax	↓
Human Hands	|	Hard Rubber	|
Asbestos	|	Nickel, Copper	|
Rabbit Fur	|	Brass, Silver	|
Glass	|	Gold, Platinum	|
Mica	|	Sulfur	|
Human Hair	|	Acetate Rayon	|
Nylon	|	Polyester	|
Wool	|	Celluloid	|
Fur	|	Orlon	|
Lead	|	Saran	|
Silk	|	Polyurethane	|
Aluminum	|	Polyethylene	|
Paper	|	Polypropylene	|
Cotton	|	PVC	|
Steel	|	KEL F	|
Wood	|	Silicon	↓
Amber	↓	Teflon	–

Similarly, a neutral object, such as an integrated circuit, can also become charged by induction. In this process, as shown in Figure 2.1, a neutral object is placed in an electric field produced by a static charge which residing on an insulator in the work

area. The field from this static charge will cause a charge separation on the neutral object. If the object is momentarily grounded, a discharge will occur and the object will acquire a net charge. This process will continue until the acquired net charge is dissipated into the air, or the object is grounded in a subsequent step.

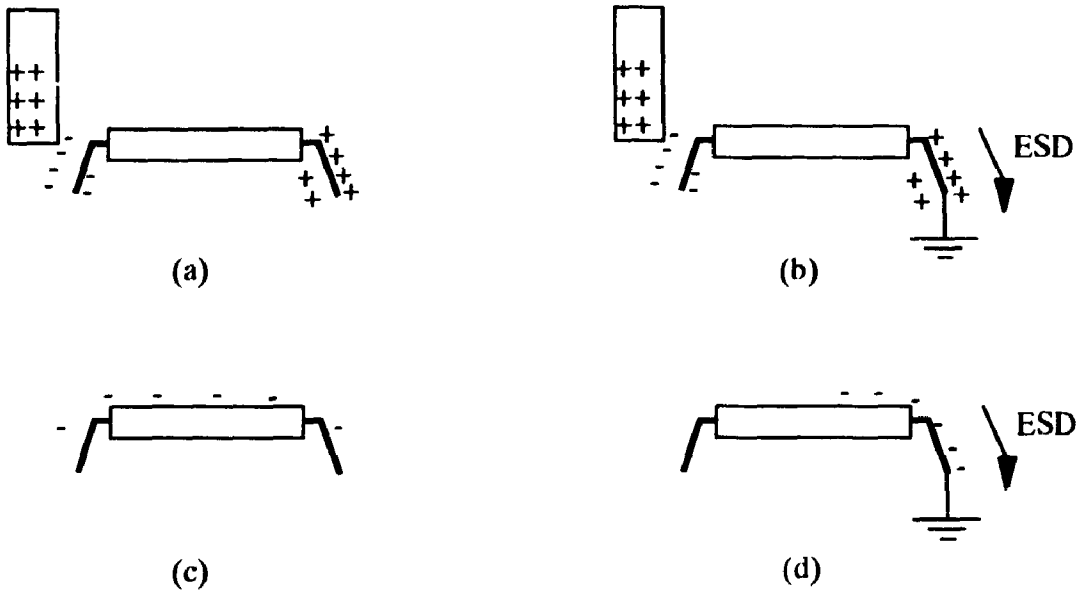


Figure 2.1 Static Induction

2.2.1.1 Types of Electrical Stress Related Damage

As the EOS/ESD can cause direct, indirect and latent failure in semiconductor devices [6], a protection network must be integrated with the device to provide some degree of immunity.

Direct or hard failure is defined as physical destruction or irreversible degradation of a device which results from a high amplitude current or voltage pulse during ESD.

For indirect failure, the faults, such as false triggering, are introduced as a result of conducted or radiated electromagnetic interference (EMI) from ESD. The damage is usually reversible; for example, it can be corrected by resetting the system.

Studies have shown that up to 90% of ESD damages are "soft" failures generated by a fraction of the ESD level required for direct destruction. These "soft" or "latent" failures can cause increased leakage current and reduced switching characteristics. Considerable controversy exists concerning the detection and nature of latency effects.

2.2.1.1.1 Latent Failures

Literature search of technical papers published on the subject of latent ESD failures shows that there are two different opinions. The first group of researchers believe that latency effects exist, but occur only with a very low probability. Other researchers, who have used simple MOS systems to investigate the physics of surfaces and interfaces, have reported evidence to support the existence of latency effects even though these results are not always directly applicable to the phenomena associated with real integrated circuits. The following is a brief review of important work related to latency effects in semiconductor devices.

Schwank *et al* [7] conducted a reliability analysis of CMOS integrated circuits and concluded that the probability of latent failures was low.

McAteer *et al* [8] performed an ESD failure study and found evidence to support latent failures.

Bowers *et al* [9] studied ESD latent effects in semiconductors and proposed that degradation due to ESD may be caused by trapped charge and micro diffusions.

Crockett *et al* [10] studied the ESD sensitivity and latency effects in some HCMOS integrated circuits. They found that initial high amplitude pulses enhance ESD sensitivity and reduce the incidence of subsequent latent damage while low amplitude ESD produces latent failures which cause hard failures at higher amplitude pulses.

Neelakantaswamy *et al* [11] proposed a model for latent failures due to the cumulative build up of thermoelastic strains induced by low level ESD pulses.

Gammill and Soden [12] documented two cases of latent failures due to ESD in CMOS integrated circuits. Failure analyses showed that the faults were initiated at gate oxide defects.

Hellström *et al* [13] reviewed different methods used to detect and analyze ESD failures, especially latent failures; these include the measurement of C-V, I-V and di/dt characteristics. The last method uses the magnitude of the "third harmonic" as a measurement of the non-linearity of a device to detect damage.

Jon and Welsher [14] performed a metallurgical study of ESD damage in 256K DRAM devices. It was concluded that only those pins whose leakage current was greater than 2 μA showed ESD latent failure, and ESD latency for devices stressed at a sub-threshold level was associated with a melt channel connecting hot spots.

Hull [15] observed a stress-hardening phenomenon after step-stress testing input protection structures in 1.5 μm CMOS gate array technology. Stress hardening

was seen as a phenomenon associated with the step-stress test; charge trapping in the field oxide was proposed as the cause. The results of life tests showed that latency of stress-hardened devices was not a problem.

Woodhouse and Lowe [16] performed a failure analysis investigation on a series of devices stressed at approximately 90% of their Human-Body-Model (HBM) ESD threshold; measurements showed no evidence of latency effects.

Krakauer and Mistry [17] used the charge-pumping technique to study the physical mechanisms underlying oxide damage due to ESD in n-channel MOSFETs. Low level ESD stress and snap back stress both resulted in significant hole trapping in the oxide, accompanied by interface state generation. Their evidence supports a latent failure mode.

Fong and Hu [18] studied operation of the thick field device/ grounded gate transistor combination input protection circuit under ESD stress. No significant latent damage was observed; no change in V_T and hot electron degradation rate were found after 1000 (500 mA/1 μs) pulses. The work suggests that the onset of latent damage may be predictable from measured internal waveforms.

Dumin *et al* [19] performed a study on the extrapolation of high-voltage stress measurements to low-voltage operation for MOS capacitors fabricated with 10 nm thick silicon oxide films on p-type silicon. Extrapolation of the high voltage stress measurements to 5V showed that easily detectable changes in the oxide properties would only occur after several years of 5V operation; extrapolation of charge-to-breakdown and time-to-breakdown data to 5V operation indicated that breakdown would occur only after hundreds of years of operation.

Doyle *et al* [20] demonstrated that reoxidized nitrited oxides have substantially better resistance to latent damage from ESD compared to conventional oxides.

Neelakantaswamy *et al* [21] discussed the susceptibility of on-chip protection circuits to latent failures caused by ESD; their results indicated that cumulative degradation at low or subcatastrophic thresholds of static exposure can be modelled using an equivalent aging principle; the method can be used to analyze test data on latent failures.

Amerasekera and Campbell [22] investigated the nature and mechanisms of ESD damage in nMOS transistors. Over 400 devices were tested; some evidence of latency effects was observed.

Determination of the physical mechanisms involved in the wearout and breakdown of thin oxides in MOS devices has been the subject of extensive research. Although there is no consensus concerning the breakdown mechanisms, it is generally accepted that breakdown is the result of charge trapping in the oxide. Various models have been proposed for the breakdown of SiO_2 [23-26] and the results of breakdown studies have been reported [27-30] which include the effect of oxide thickness [31-32] and voltage polarity [33]. Wolters [34-35] reviewed the electrical properties of oxide films in MOS devices. Dielectric breakdown of MOS capacitors occurs when significant charge is injected into the oxide, and an analogy can be made between this electrical breakdown and the mechanical breakdown of a solid when repeatedly stressed. They also proved that the key parameter in all measuring techniques they performed, namely, constant voltage or current, ramp voltage or current, is the charge required to breakdown. They showed that the charge to breakdown is the same as long as the conditions at breakdown are not too

different. An important factor in intrinsic breakdown is the time integral of leakage current until breakdown (Q_{bd}); Q_{bd} was observed to be approximately constant at low current densities.

With decreasing device dimensions (including oxide thickness) and the use of relatively constant power supply voltages, the electric field sustained by oxide films in either passive or active devices continues to increase. With the increasing electric fields, many degradation mechanisms begin to appear. Primary among these are bulk trap creation and interface state generation. The generation of interface and bulk traps has been studied [36-38]; the details of device processing have been shown to have a strong influence [39-40]. The effect of high temperature annealing on both bulk and interface traps has been investigated [41-42].

The problems associated with charge flow (Fowler-Nordheim or hot electron injection) through thin oxides is of interest. During injection, charges are generated in the oxide and eventually lead to breakdown [43-48]. The effect of various parameters on charge trapping/detrapping processes have been studied, including gate thickness [49], gate material [50] and temperature [51].

Hot carriers are generated near the drain of a device by the high electric field and may be injected into the oxide. The injected carriers can be trapped in the oxide and/or generated interface traps; hot-electron-induced device degradation has been extensively studied [52-56].

Aur *et al* [57] studied the impact of noncatastropic ESD stress on hot-electron reliability as well as the effect of hot-electron injection on ESD protection thresholds. Hot-electron-stress degraded the transistor performance but not the ESD

strength; the ESD latent damage will degrade the hot electron reliability. Latent damage to the gate dielectric due to low-level ESD stress was observed for LDD nMOS transistors clad with silicides. Techniques for characterizing hot-electron degradation were applied to measure damage due to ESD. Electrical evidence of filamentary conduction and localized charge injection was observed; the same results had been noted by Khurana et Al [58] using an infrared imaging technique.

Finally, it was found that snapback stress [59] during ESD events results in oxide damage that is, in many ways, similar to that found during hot-carrier stress.

The literature review has shown the necessity to study the fundamental properties of latency effects in semiconductor devices. It follows from the fact that there is no general agreement on the definition of latent failures. A device might be said to incorporate a latent failure if [60]:

(1) At least one parameter, such as leakage, has reached an out-of-specification condition.

(2) At least one parameter exhibits significant change from the initial value but has not reached any out-of-specification condition. The meaning of significant change can be arbitrarily defined as a 10%, 40% or 100% shift in the parameter value.

(3) No parameter has reached the conditions of either (1) or (2). However, from past experience, it is known that it has some likelihood of reaching (1) or (2) if subjected to what is considered reasonable additional stress, such as temperature, normal supply voltage, or repeated ESDs.

In other words, latent failures are also related to whether or not the designers have pushed device performance to reach published specification limits. A conservative designer can tolerate some device degradation due to latent failure while others cannot. As the size of static-sensitive devices, such as MOS, diminishes and their use grows, the problem becomes worse. However, due to the lack of knowledge and unavailability of an acceptable failure analysis, most people do not believe in latent failures, and many ESD-caused failures are not blamed on ESD.

2.2.1.2 ESD Protection Circuits

The purpose of a protection circuit is to increase the EOS/ESD immunity of a device. One of the basic requirements of protection circuitry is that it must not interfere with the normal operation of the circuit. The fundamental idea behind a protection circuit is to act as high speed switches, as shown in Figure 2.2. When the protection circuit senses an ESD pulse, it will shunt the pulse to ground and/or power line by closing switch #1 and/or switch #2, and immediately open the switches to resume normal operation after the transient has passed.

There are various types of protection circuits available today which utilize different combinations of basic electronic elements, namely, polysilicon resistors, diodes, diffused diodes, field plate diodes, thin oxide punch through transistors, thick oxide punch through transistors and spark gaps [6].

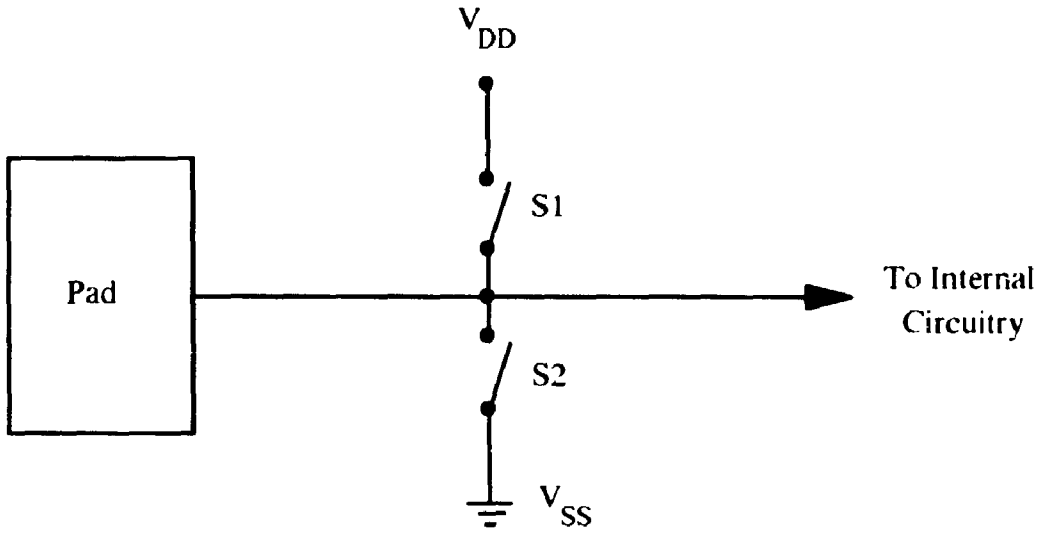


Figure 2.2 Basic Concept of a Protection Network

2.2.2 Intrinsic Failure Mechanisms

Intrinsic failure mechanisms, related to the semiconductor die itself, include crystal defects, dislocations and processing defects. The most common intrinsic failure mechanisms are related to gate oxide breakdown and charge effects. Gate oxide breakdown usually results from the high electric fields generated by EOS/ESD which exceed the oxide breakdown field strength. This is an electrical stress related failure and has been discussed in the previous section. Charge effects on devices will be considered next.

2.2.2.1 Charge Effects

MOS devices depend critically on the charge stored in the gate oxide capacitance, therefore any alteration of this charge can lead to failure of the devices, caused by physical defects or movements of charge through the damaged oxide. The

causes of charge effects failure can be ionic contamination, charge trapping or dislocations in the silicon-silicon dioxide interface. A detailed discussion of the charge effects on device electrical characteristics has been presented in Chapter 1.

2.2.3 Extrinsic Failure Mechanisms

Extrinsic failure mechanisms are related to the reliability of device packaging. The reliability can be influenced by the packaging, bonding and die attachment technology employed in the manufacturing process. Usually, the source of this failure are imperfections introduced at the physical interfaces between the different sections [1].

2.3 Failure Analysis Techniques

In experimental failure analysis it is vital to ensure that the examination process does not destroy evidence of the failure. If the cause of failure can be determined and studied, improvements can be made to the manufacturing process and the component reliability improved. Examination of both good and faulty devices can be advantageous to failure analysis, but in addition, the study of deliberately induced failure can be of great help.

2.3.1 Methodology for Failure Analysis

There are four basic steps in the analysis of the failure mechanisms of semiconductor devices. They are : (1) package decapsulation, (2) selective layer removal, (3) location of failure site and (4) identification of the cause of failure.

Before any attempt to investigate the failure mode of a device is made, the package has to be decapsulated. Ceramic packages are easily opened by mechanical means using a cutting edge which, however, introduces additional loose particles into the package. The method may obscure the evidence of loose particles already present in the device. For plastic/epoxy packages, a solution of fuming sulphuric, nitric or hydrofluoric acid is a very effective method of removing the encapsulant.

The techniques used to locate the failure site include optical examination, X-ray diffraction, microprobing and the scanning electron microscope. Visual examination can reveal defects such as pinholes, voids, small open circuits and fused silicon caused by EOS/ESD. Corrosion, burn-outs and bonding failures can also be detected by visual inspection. More detailed visual inspection can be accomplished by using the scanning electron microscopy (SEM) in which high magnification is available.

Parametric measurements on the faulty device such as detecting the threshold voltage shifts can be performed using microprobe techniques. The results are compared with those of good devices to provide information regarding the failure mechanisms.

2.3.2 Electrostatic Discharge Simulation

Although several models, such as the Human Body Model (HBM), the Charged Device Model (CDM), the Machine Model (MM) and the Field Induced Model (FIM), have been developed to simulate and characterize the behaviour of electrostatic discharge, the most common models are the HBM and CDM [61].

The HBM simulates a charged human body touching an uncharged object such as an integrated circuit. As shown in Figure 2.3, the human body resistance and capacitance are represented by a resistor (R_B, 150 to 10 kohms) and a capacitor (C_B, 50 to 500pF). The impedance of the integrated circuit to ground is represented by the parallel combination of R_T and C_T. The capacitor is charged to a certain voltage (V_{HBM}) by closing the "charge switch" with the "discharge switch" open. The charge (C_B x V_{HBM}) is then released to the device by opening the "charge switch" and closing the "discharge switch". The rise time for a HBM pulse is typically less than 10 nanoseconds with a decay time constant of 50 to 300 nanoseconds.

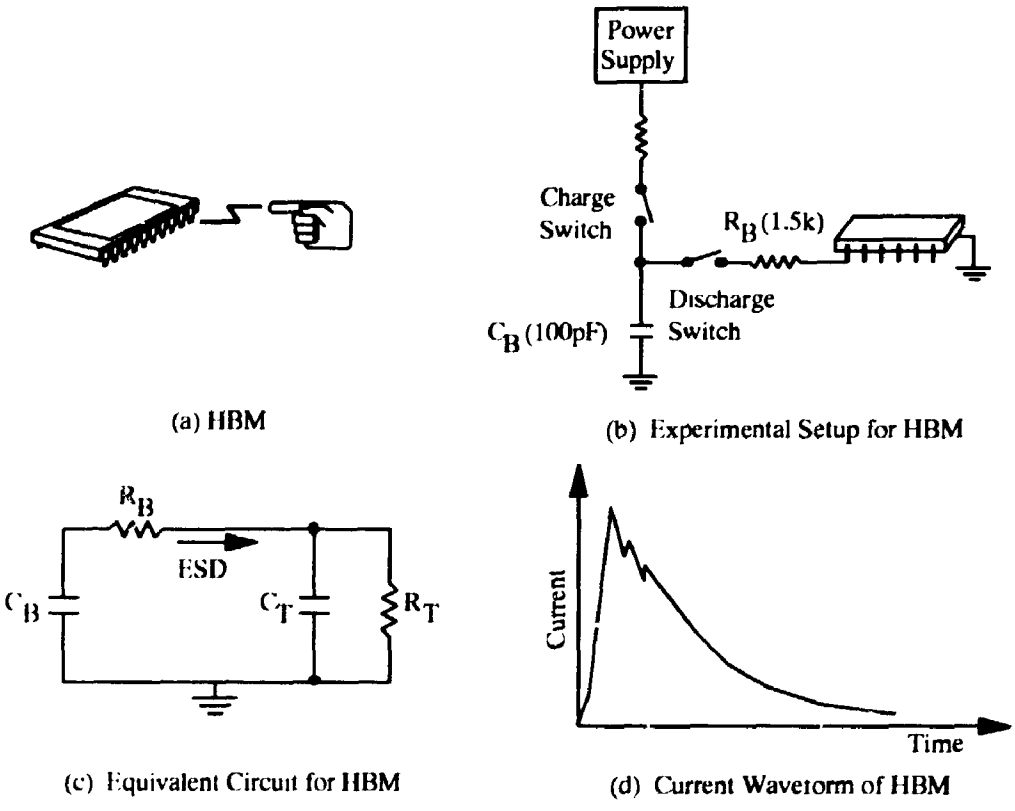


Figure 2.3 Human Body Model (HBM)

The Charged Device Model (CDM), shown in Figure 2.4, represents a discharge from an charged IC package. The device can become charged by contact electrification (triboelectrification) with another neutral body, by direct contact with another object having a higher electric potential, or by induction charging in the presence of an external electric field. The rise and fall times for CDM pulses are typically below 1 nanosecond because of the small parasitic impedance (C_T, R_T and L_T) of the device and discharge resistance (R_C).

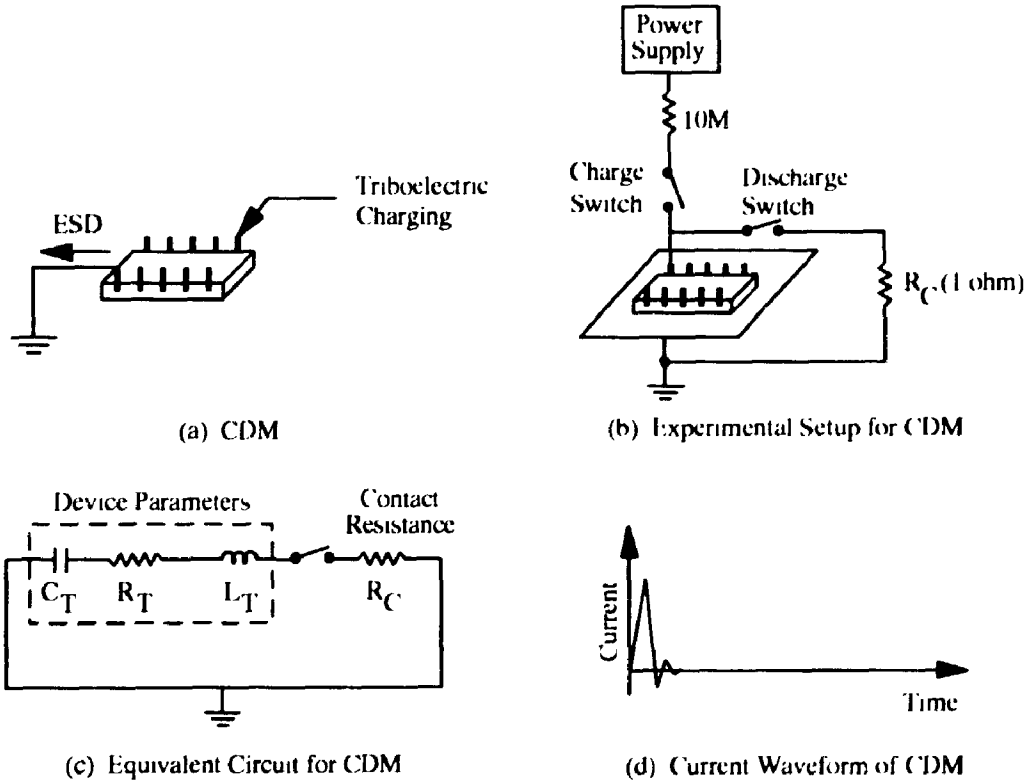


Figure 2.4 Charged Device Model (CDM)

Recently, the human-body current injection test method has become popular in device testing and reliability measurements. In this test procedure, as shown in Figure 2.5, the probe tip of the simulator is placed directly in contact with the pin of the device-under-test and the discharge energy is applied by closing the mercury relay.

The current injection test method was chosen since it gives more repeatable results compared to the air discharge test method, in which the charged simulator tip is brought in close vicinity to the device and an actual air discharge occurs. The current injection method was described in the second issue of IEC 802-2 [62]. It should be noted that the R-C values used in the simulator [R = 150 ohms, C = 150 pF] are different compared to the R-C network [R = 1500 ohms, C = 100 pF] used in conventional human body air discharge simulators [63]. Tests standards are in a stage of evolution; review articles have been published which summarize progress made to date [64-68].

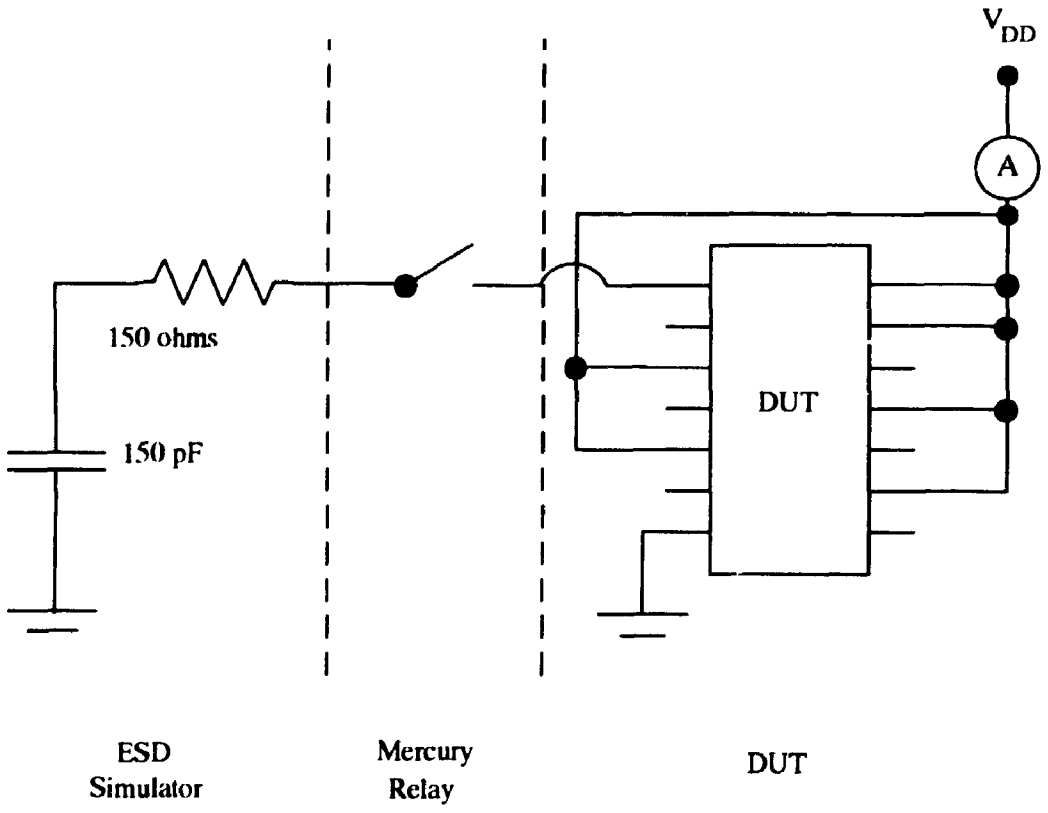


Figure 2.5 Test Circuit for Measuring the Electrical Characteristics of a Device

2.3.3 Quiescent Current Measurements

The quiescent current measurement method measures the power supply current during the circuit's quiescent state and is an effective method to detect defects in CMOS integrated circuits [69-70]. Typically, in CMOS technology, this current is less than 10 nanoamperes. As illustrated in Figure 2.6, defects such as charge trapping, gate oxide shorts, and parasitic transistor leakages in the circuit can increase the quiescent current. However, the output logic state of the device may remain unaffected. Studies have shown that conventional testing techniques, such as stuck-on and stuck-off models, are unable to detect physical failures in MOS circuits. In these tests, a series of logic patterns are generated and input to the integrated circuit; the corresponding output states are measured to verify proper operation and detect any faults. In comparison, the quiescent current measurement method can be used to directly detect defects; conventional tests often fail to yield this information.

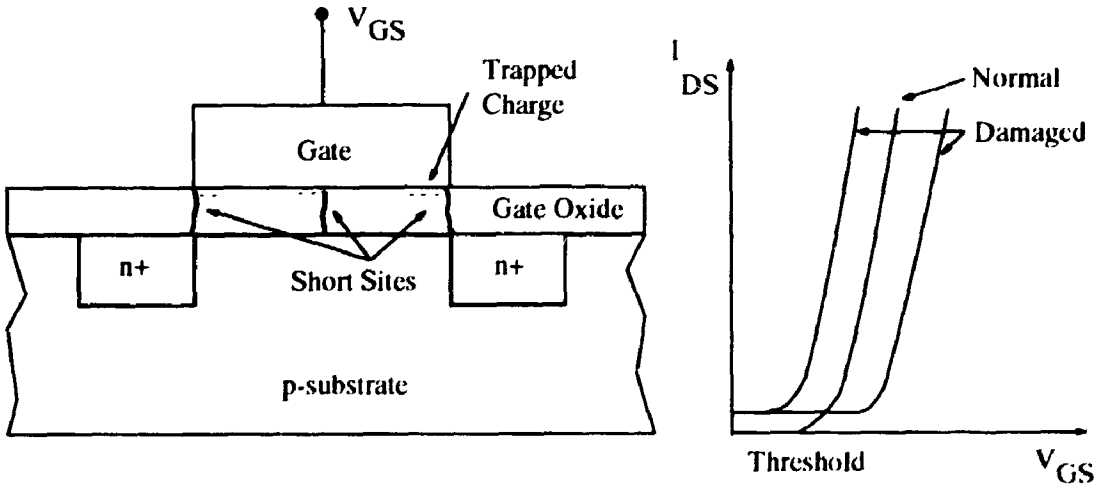


Figure 2.6 Typical Defects in MOS Structures

2.3.4 Capacitance-Voltage Measurements

Capacitance-Voltage measurements provide a powerful analysis tool [71-74]. CV measurements can disclose the doping profiles of the material used in the devices and the oxide and interface characteristics which may be influenced by stress, device damage, annealing, or interface traps. Figure 2.7 shows that information can be obtained from measuring the high frequency (C_{HF}) and quasistatic (C_{LF}) capacitance versus applied voltage characteristics. The high/quasistatic frequency equivalent circuit of a MOS capacitor is shown in Figure 2.8. The quasistatic capacitance must be measured at a sufficiently low frequency (mHz) such that all traps completely respond to the staircase voltage waveform. To measure the high frequency capacitance, a small sinusoidal (10mV) high frequency (1MHz) signal is superimposed on the voltage staircase. It is assumed that all traps completely respond to a step voltage applied to the MOS structure while none respond to the sinusoidal high frequency signal; the capacitance associated with the interface traps (C_{it}) can then be calculated by subtracting C_{HF} from C_{LF} in the depletion mode.

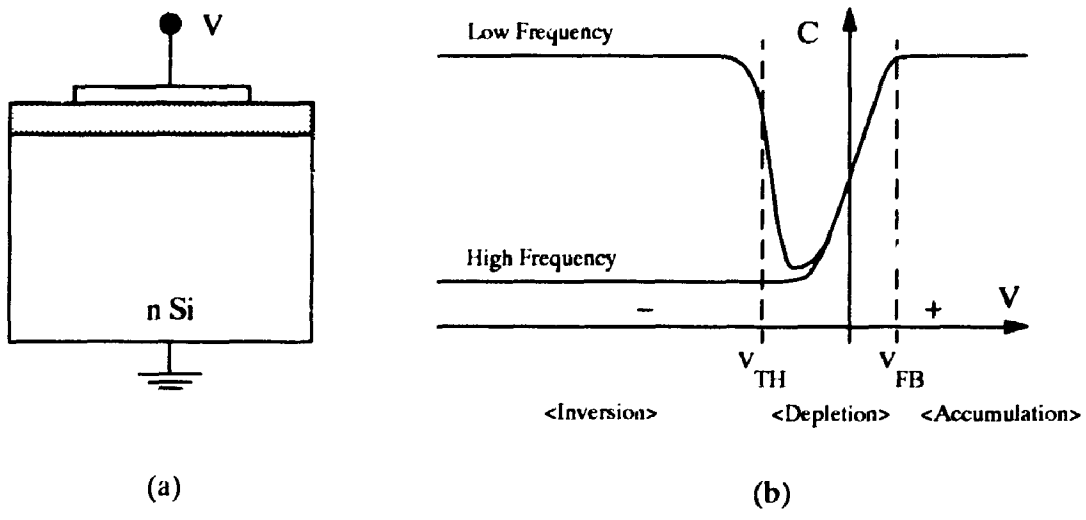


Figure 2.7 Typical C-V Characteristics of n-type Material

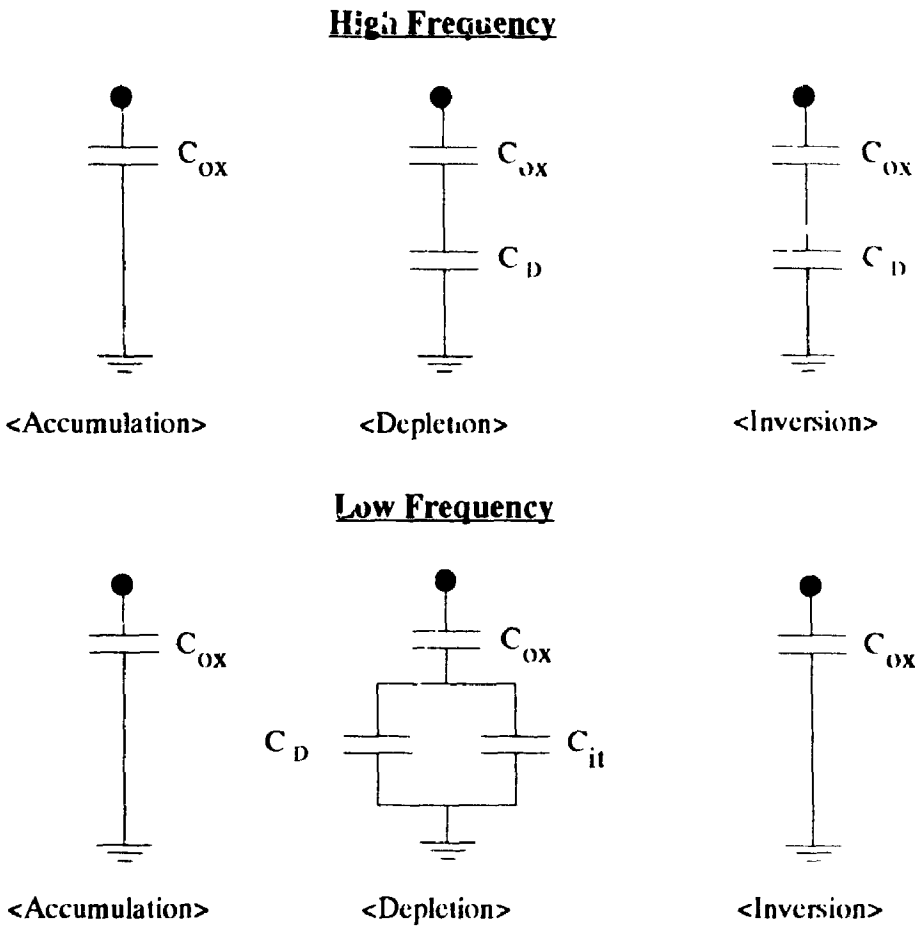


Figure 2.8 Equivalent Circuits of a MOS Capacitor

2.4 Summary

In this chapter, different failure mechanisms in semiconductor devices and various analysis techniques used in the experiments were discussed and a detailed review of research on ESD latency effects in MOS structures presented. It was found that considerable controversy exists concerning the detection and nature of latency effects. Due to the lack of knowledge and good failure analysis techniques, the existence of latent failures is often questioned. The techniques described here will be used for design and analysis in the following chapters.

Chapter 3

Circuit Design

A 3-micron single polysilicon, double metal P-well Complementary Metal Oxide Silicon (CMOS) technology was chosen for this project. This process [Appendix C] is used by Northern Telecom Electronics (Ottawa, Ontario) and is available to Canadian university researchers through the Canadian Microelectronics Corporation (Kingston, Ontario). The design rules and colours codes used in the project are listed in Appendix C. A number of CCDs and protection circuits were designed and analyzed. Those suitable for the fabrication process were selected for implementing the design. This chapter describes the design procedures of the circuits which were submitted for fabrication.

3.1 Charge-Coupled Devices

As mentioned in Chapter 1, the basic configuration of a charge-coupled device is an array of closely spaced MOS capacitors. By placing the storage elements, *i.e.* the MOS capacitors, adjacent to each other, the individual charge packets pass from one storage element to the next due to the application of an appropriate sequence of gate voltages.

In order to prevent charge losses and trapping that may occur from the defects in the depletion profile in the gap area between gates, an overlapping gate structure was used in this project. The two-level overlapping gate structure is constructed using polysilicon and aluminium, chosen for its compatibility with the fabrication process supported by the Northern Telecom Electronics.

Various CCD structures, such as four-phase, three-phase and two-phase CCDs, have been discussed in Chapter 1. Each has its unique advantages and disadvantages. In this project, a two-phase CCD structure, shown in Figure 3.1, was chosen based on its popularity in the market today. The asymmetric structure required in two-phase CCD is achieved inherently when polysilicon-aluminium is used as the overlapping gate structure. Due to the two different oxide thicknesses, the surface potential under the aluminium gate is lower than that under the polysilicon gate when a voltage is applied to the gate. A directional charge flow can be achieved by a two-phase clock shown in Figure 3.1; the layout of the shift register is shown in Figure 3.2.

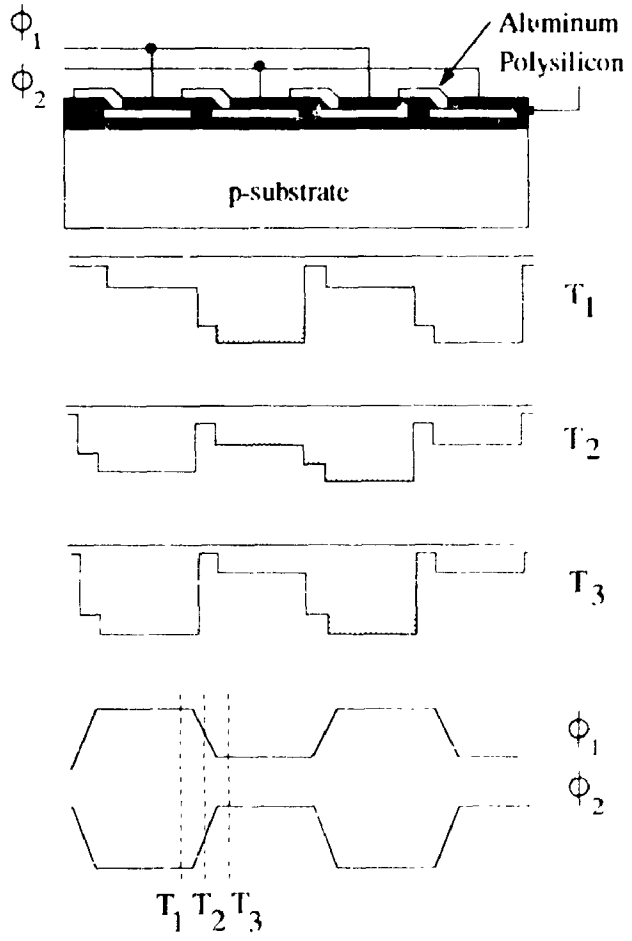


Figure 3.1 A Shift Register with Overlapping Gate Structure

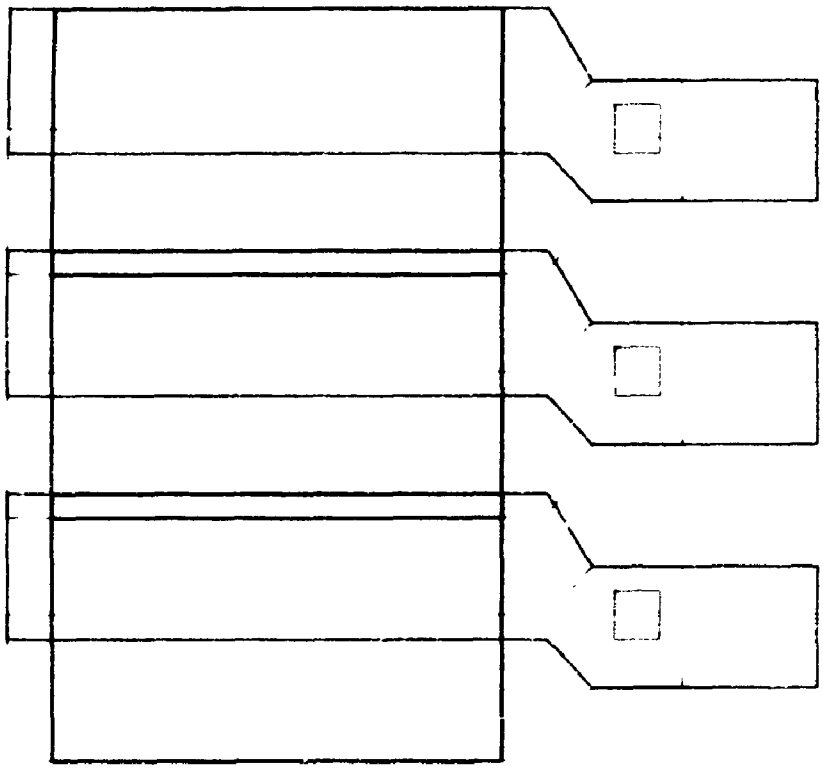


Figure 3.2 Layout of the Shift Register

The signal charge is injected into the shift register through an input diode which acts as a source of electrons. This method is usually referred to as the "Fill and Spill" method Consider the circuit illustrated in Figure 3.3, which consists of an input diffusion, two input gates and the first two phases of a CCD structure. Initially, the input diffusion (diode) is reverse biased to V_{D1} whereas gates G_1 and G_2 are at V_{G1} and V_{G2} respectively. The depletion profile is shown in Figure 3.3(a). As the diode is pulsed from V_{D1} to V_{D2}, the well under gate 2 is flooded with charge and overflows. This corresponds to the "fill" action in Figure 3.3(b). When the potential returns from V_{D2} to V_{D1}, any charge above V_{G1} will drain back into the diode, but the well beneath V_{G2} remains full. This corresponds to the "spill" operation in Figure 3.3(c). The amount of charge (Q_S) injected into the shift register is controlled by the surface potential under the two input gates and is given by:

$$Q_S = -C_{ox}(V_{G2} - V_{G1}) \qquad \ldots(3.1)$$

where :

Q_S = sampled signal charge
V_{G1} = voltage at gate 1
V_{G2} = voltage at gate 2
C_{ox} = oxide capacitance

For imaging applications, the charge stored and transferred within a CCD is injected into the device photoelectrically through photodiodes or photoMOS. The photoelements convert the energy of light into an electrical signal (electron-hole pairs) and temporarily store this signal charge in the parasitic capacitor. After integration, this charge is transferred to the shift register through the transfer gate. The equivalent circuit of the photo sensing region is shown in Figure 3.4

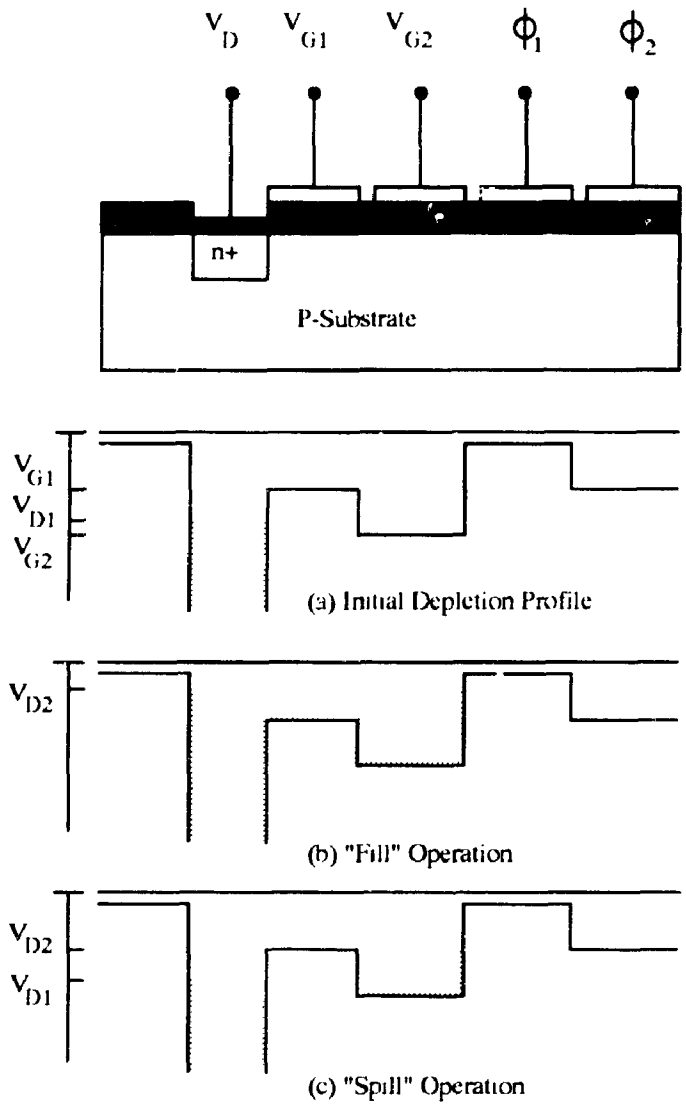


Figure 3.3 Input Configuration of CCD

As shown in Figure 3.5, in the photodiode structure, an n+ region is implanted in the p-type substrate to form a pn diode. This diode creates a space charge region in which photoelectrons are separated from holes. The photoelectrons are then accumulated in the n+ region.

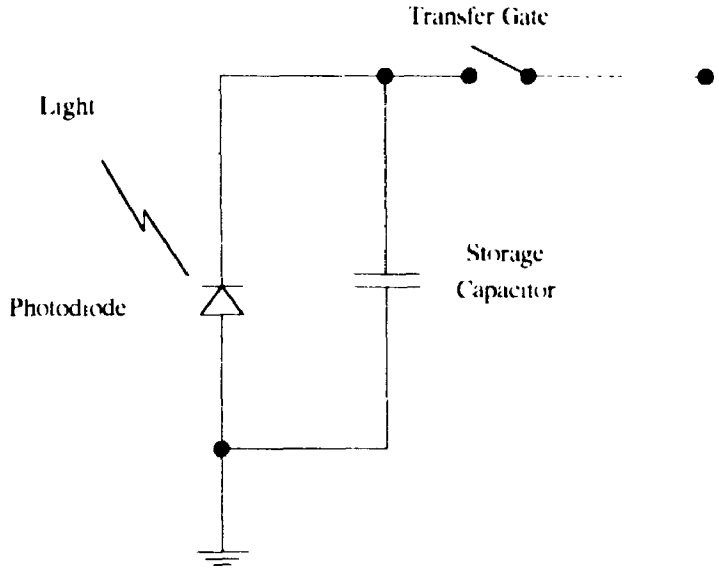


Figure 3.4 Equivalent Circuit of Photo Sensing Region

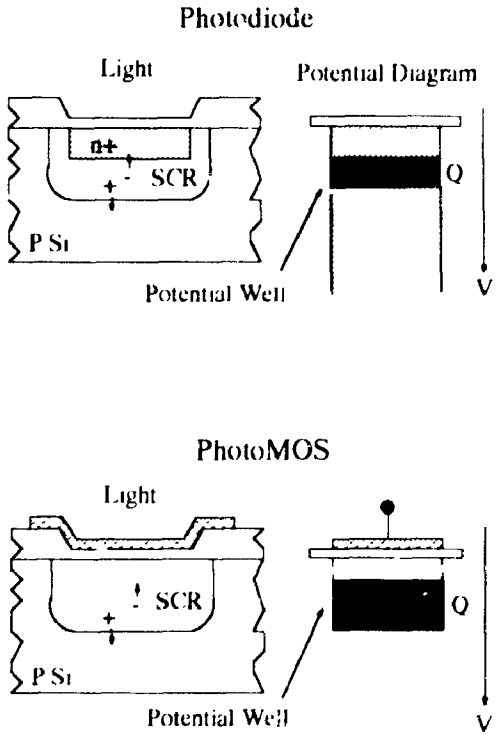


Figure 3.5 Photodetection Using Silicon

In the photoMOS structure, the space charge region is induced by a polysilicon gate overlying a thin oxide layer. Under favourable bias conditions, the photoelectrons, as shown in Figure 3.5, drift and accumulate in the inversion region. Therefore, the MOS structure can be used to generate photoelectrons and to transfer charges.

The typical spectral responses and the characteristics of these photoelements are tabulated in Table 3.1 [75] and Figure 3.6 [75].

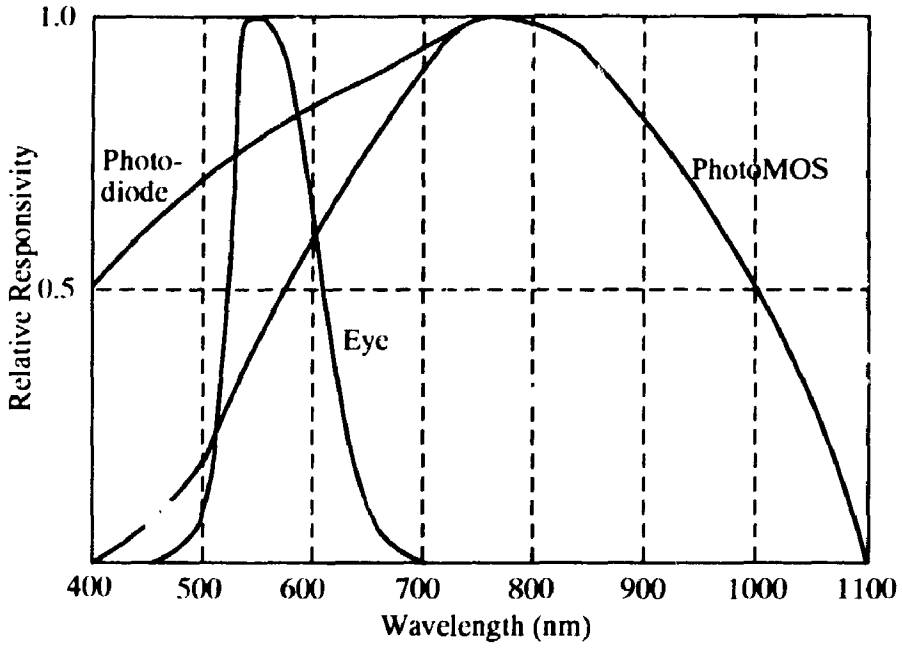


Figure 3.6 Typical Spectral Response for Photoelements

If the charge is injected to the shift registers by photoelements, a phenomenon called blooming can occur, if charge is spread from one site to its neighbors. This can happen when the scene being imaged contains very strong local light sources which exceed the lens aperture setting and/or the exposure period. The spread of photocharges appears as a white spot on the displayed image. To control this excess injected charge from spilling over to neighbouring sites, an antiblooming structure must be incorporated

Table 3.1 Comparison of PhotoMOS and Photodiode Elements

Characteristic	Photoelement Structure	
	Photodiode	PhotoMOS
Average Quantum Efficiency nm in the Visible Spectrum	60%	30%
Spectral Response	Uniform. Higher than photoMOS in the blue region (n=50%at 450nm)	Irregular and poor in the blue region (n=20% at 450nm)
Storage Capacity	Poor	Good
Image Lag	Yes (can be reduced by bias charge)	No

into the design. In this project, a horizontal antiblooming structure is used; an antiblooming diode is implanted at each photosite and is separated from the photodiode by a control gate. This gate is biased to adjust the potential barrier between the photocharges and the antiblooming diode to a level lower than the potential well separating two neighbouring wells, so that all excess charge will overflow into the antiblooming diode. Therefore, the bias of this gate determines the saturation level. A photodiode with an anti-blooming structure was chosen and fabricated. The cross sectional view and the layout of this structure are shown in Figures 3.7 and 3.8 respectively.

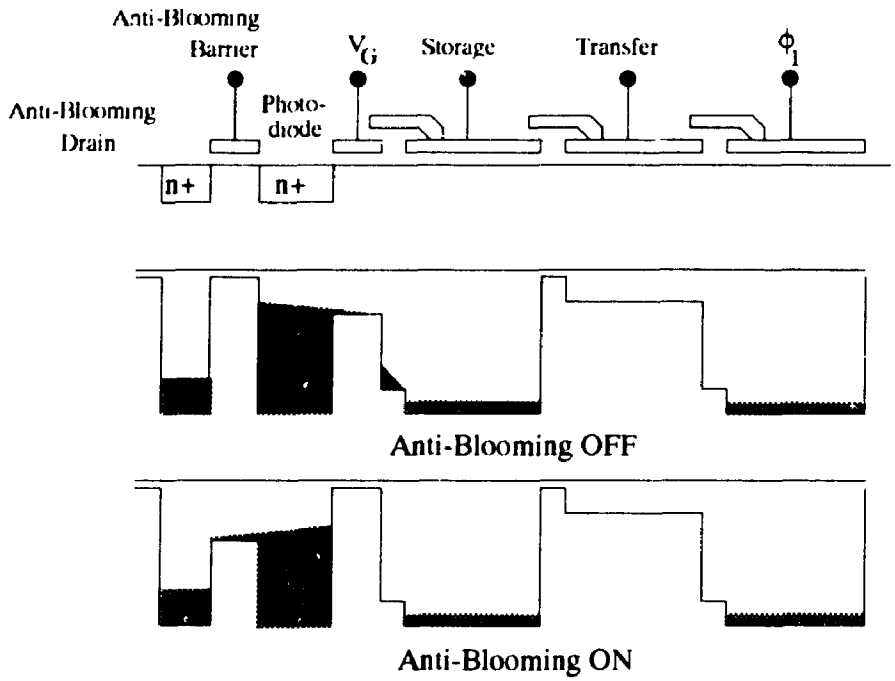


Figure 3.7 Photodiode Circuit with Anti-Blooming Control

Finally, the signal charges transferred by the CCD analog shift register are converted into a voltage signal in the charge detection region. The output circuit, as shown in Figure 3.9, consists of an output gate, a source-follower MOSFET connected to a floating diffusion, a reset gate (RS) and a voltage biased drain. The layout of this structure is shown in Figure 3.10.

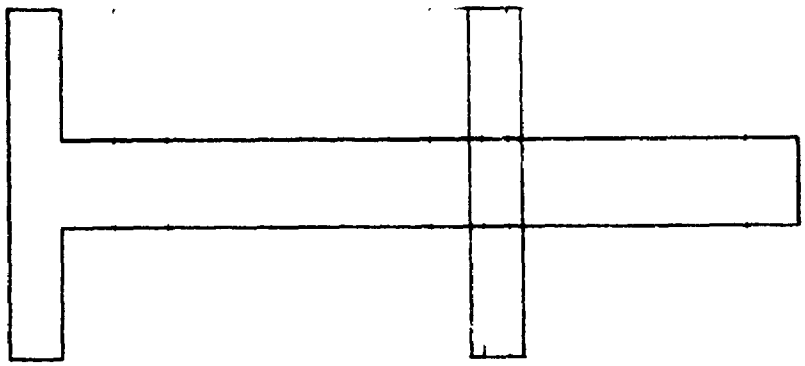


Figure 3.8 Layout of the Photodiode with Anti-Blooming Structure

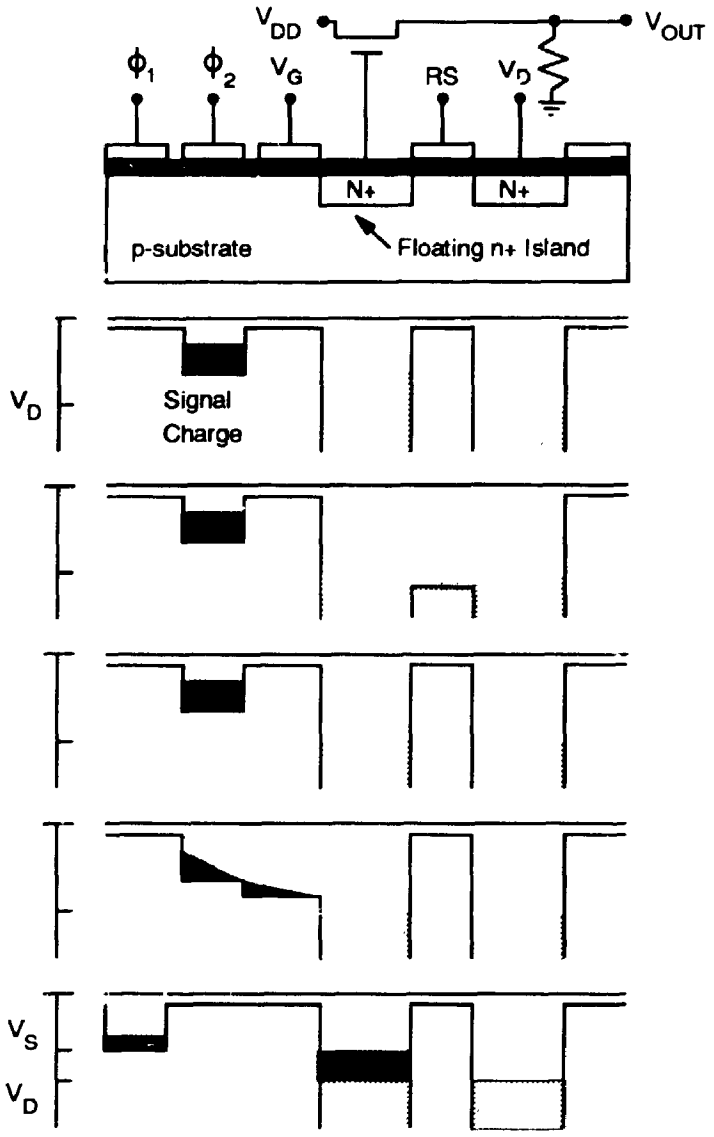


Figure 3.9 Output Structure of CCD

An initial short reset pulse is applied to the reset gate to ensure that the floating n+ island remains at V_D. Shortly afterwards, the surface potential of the output gate V_G is lowered to allow the signal charge to flow into the floating n+ island. The voltage change is detected by a source-follower MOSFET circuit and can be calculated by the amount of charge (Q_O) which flows into the island.

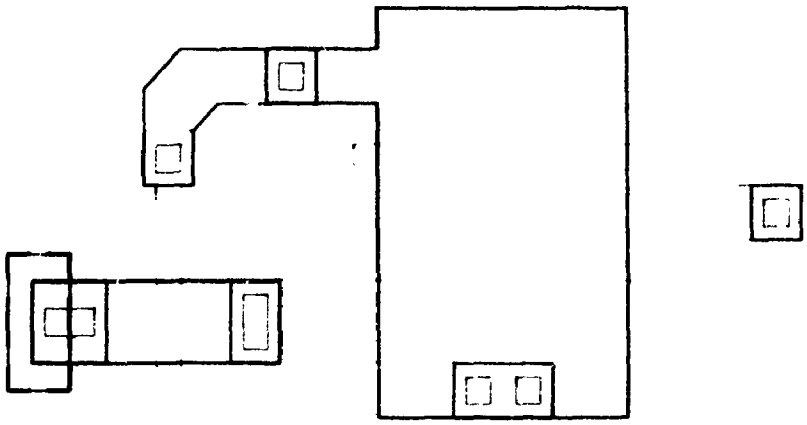


Figure 3.10 Layout of the Output Structure

$$\Delta V = \frac{g_m R_d}{1 + g_m R_d} \left(\frac{Q_O}{C_{fg}} \right)$$

$$= \frac{g_m R_d}{1 + g_m R_d} (V_D - V_S) \qquad \ldots(3.2)$$

Where :

ΔV = signal voltage
Q_O = signal charge
C_{fg} = floating gate capacitance
V_D = drain voltage
V_S = signal voltage
g_m = transconductance of MOSFET
R_d = effective load resistance

Using these basic structures as building blocks, a variety of CCDs have been designed and fabricated. Both the surface channel and buried channel CCDs are studied in this project. All the CCDs are 8-stage, two-phase devices with 16 gates (capacitors). Since the fundamental objective of this project was to study the reliability of CMOS structures subjected to EOS/ESD, electrical inputs are used to inject charge into the device. Figures 3.11 and 3.12 show the layouts of a surface channel CCD with electrical and optical inputs respectively. The electrical characteristics of the individual circuit elements are tested using the layout shown in Figure 3.13.

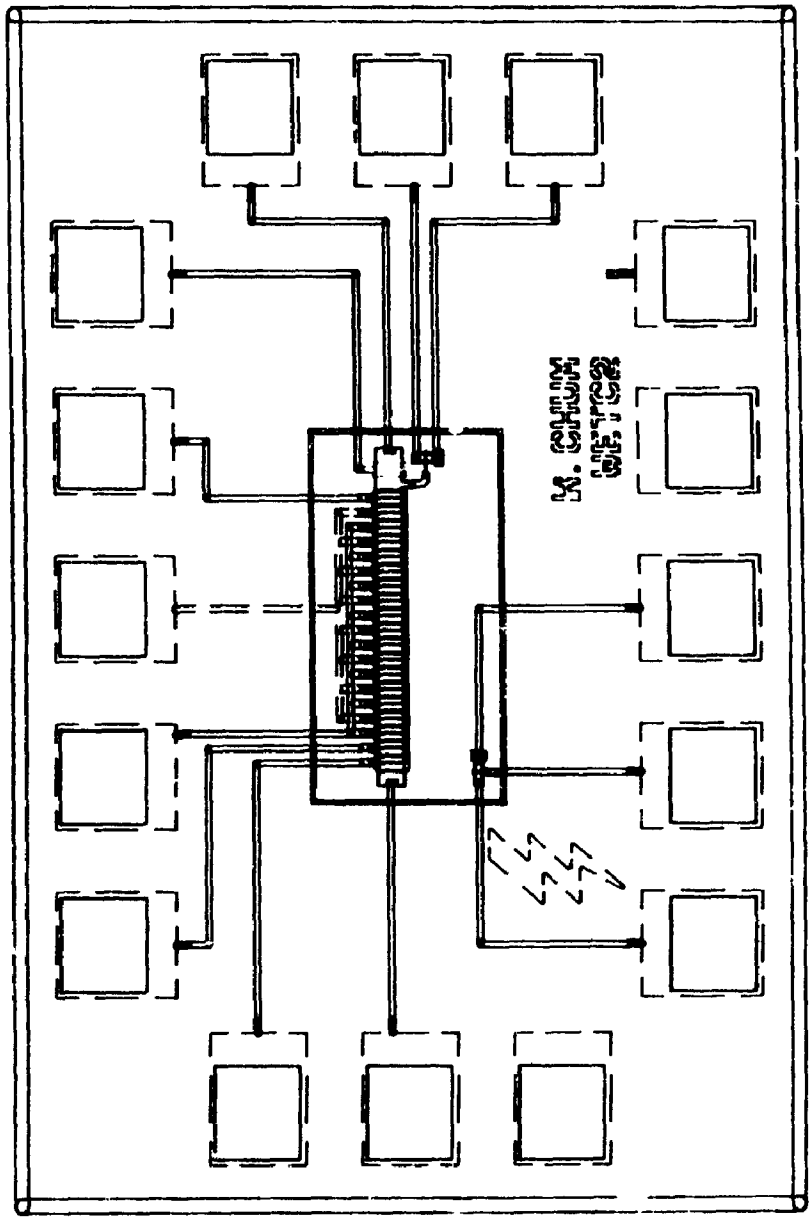


Figure 3.11 Layout of a 16-stage, 2-Phase Surface Channel CCD with Input Diode

3.2.2 Output Protection Circuits

It is important for an output pad driver to have sufficient power to meet the rise and fall time requirements for a capacitive load. The size of the driving gate can be increased to meet this requirement. However, the response time of the transistor is directly proportional to load capacitance and indirectly proportional to the width-to-length ratio. The increase in the driving gate dimension will eventually load the preceding gate, decreasing thus the speed. A set of cascaded inverters is used to solve the problem, where their size varies according to the position in the series structure. The width of the inverter is larger than that of the preceding one by a stage ratio "n". A cascaded set of four inverters is shown in Figure 3.24.

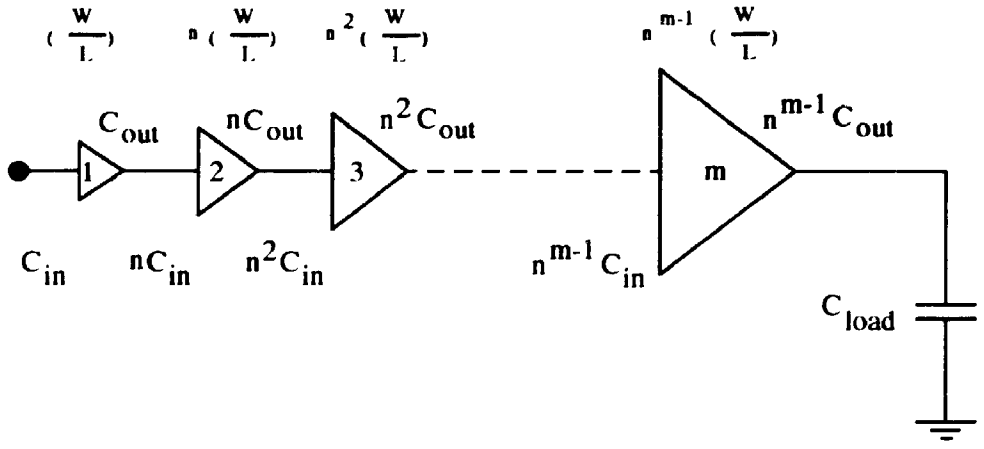


Figure 3.24 A Cascaded Output Buffer Circuit

Output pads, in general, inherently possess a reasonable degree of protection even though they are connected to layers separated by thin oxide from other nodes in the circuit. By their nature, the pads are directly connected to a diffused region which forms a parasitic diode, as shown in Figure 3.25. The circuit diagram and layout for the output pad are shown in Figures 3.26 and 3.27, respectively.

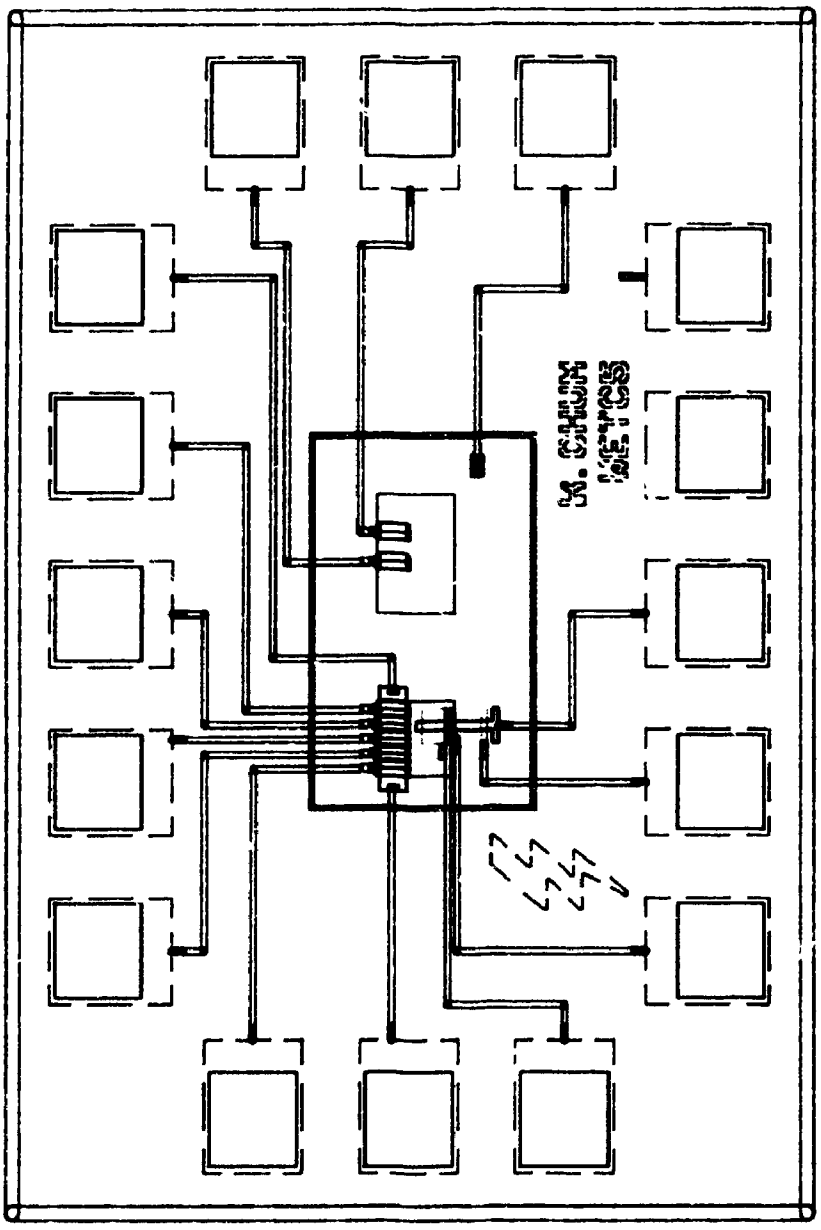


Figure 3.13 Layout of Individual Elements Used in the Surface Channel CCD

3.2 Protection Networks

Because the gate of a MOS transistor in CMOS technology is separated from the substrate by the gate oxide, the input impedance is very high (10^{12} to 10^{13} ohms). The voltage due to charge accumulation on a gate can be calculated from:

$$V = \frac{Q}{C_g} = \frac{I\Delta t}{C_g} \qquad \ldots(3.3)$$

where :

V = gate voltage
I = input current
Q = charges accumulation on the gate
Δt = time taken to charge the gate
C_g = gate capacitance

For a typical CMOS process, the gate oxide thickness is about 50 Å and the oxide breakdown voltage is between 30 to 80 volts. If C_g = 0.05pF, I = 10μA and Δt = 1 μsec, the voltage generated by this current will be approximately 200 volts. This is more than enough to destroy the transistor. Therefore, some overvoltage protection must be included whenever MOS transistors are required to interface with external signals.

3.2.1 Input Protection Circuits

The most common protection strategy employed in commercial devices today involves connecting the input pads through a small polysilicon resistor to a reverse-biased and a forward-biased diode that nondestructively breaks down or

conducts at voltages below the critical gate oxide breakdown voltage. The resistor provides a current limiting function for the protection diodes during discharge. The gate to be protected is connected to the protection resistor and the diodes. The schematic and the cross-sectional view of this input protection circuitry are shown in Figures 3.14 and 3.15 respectively.

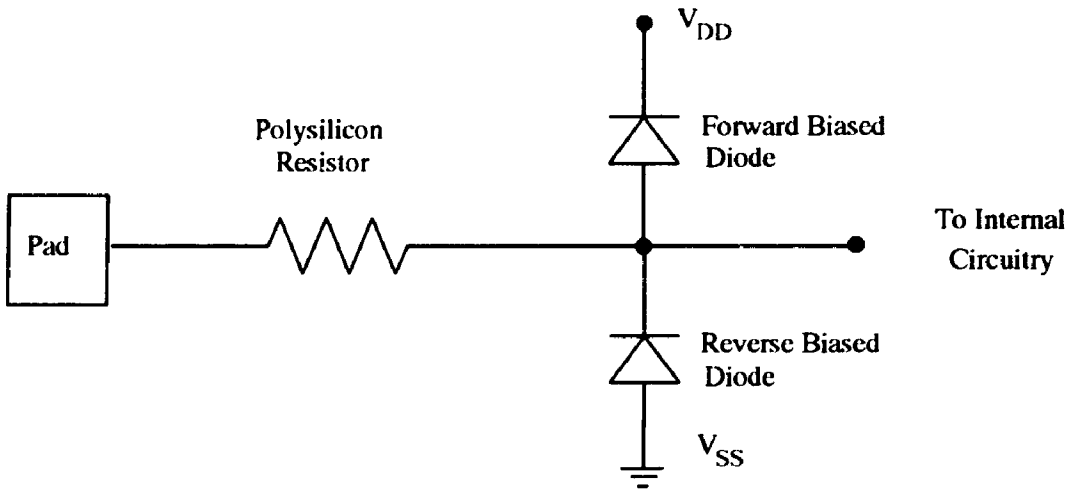


Figure 3.14 Schematic of the Input Protection Circuit

In the CMOS process chosen in this project, the reversed-biased diode is constructed by putting a n+ diffusion in a p-well. To protect the circuit from latch-up, a p+ guard ring is used to completely encircle the periphery of the well. This guard ring is connected to the lowest potential in the circuit, *i.e.* ground or V_{ss}. One end of the n+ diffusion is connected to the pad through the polysilicon resistor and the other end is connected to the gate that is to be protected. This particular diode provides protection through the reverse breakdown voltage if the input is positive, and through normal forward-biased conduction if the input is negative.

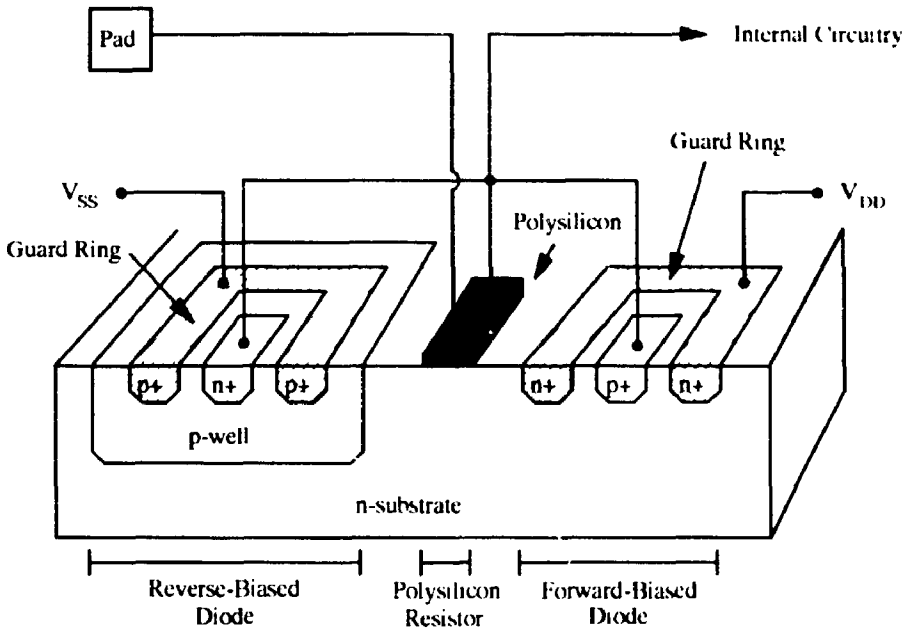


Figure 3.15 Cross-Sectional View of the Input Protection Circuit

The construction for the forward biased diode is from a p+ diffusion in the n-substrate. Similar to the reversed biased diode, this p+ diffusion is encircled by a n+ guard ring to provide latch-up immunity. The n-substrate and the guard ring is connected to the highest potential in the circuit and the p+ diffusion is connected to the intersection node of the reversed-biased diode and the polysilicon resistor.

Theoretically, using this protection principle under normal operation, the diodes do not conduct and, therefore, do not interfere with the operation of the circuit. Actually, the diodes do contribute a small amount of leakage current and parasitic capacitance.

One way to improve the protection network efficacy is to replace the diodes with diffused diodes. During an ESD transient condition, diffused diodes act as a distributed diode-resistor network and greatly reduce the threat of thermal overstress.

The diffusion area acts as a resistor, and the well and the diffusion form an effective diode. The schematic and the cross-sectional view of this input protection circuit are shown in Figures 3.16 and 3.17 respectively.

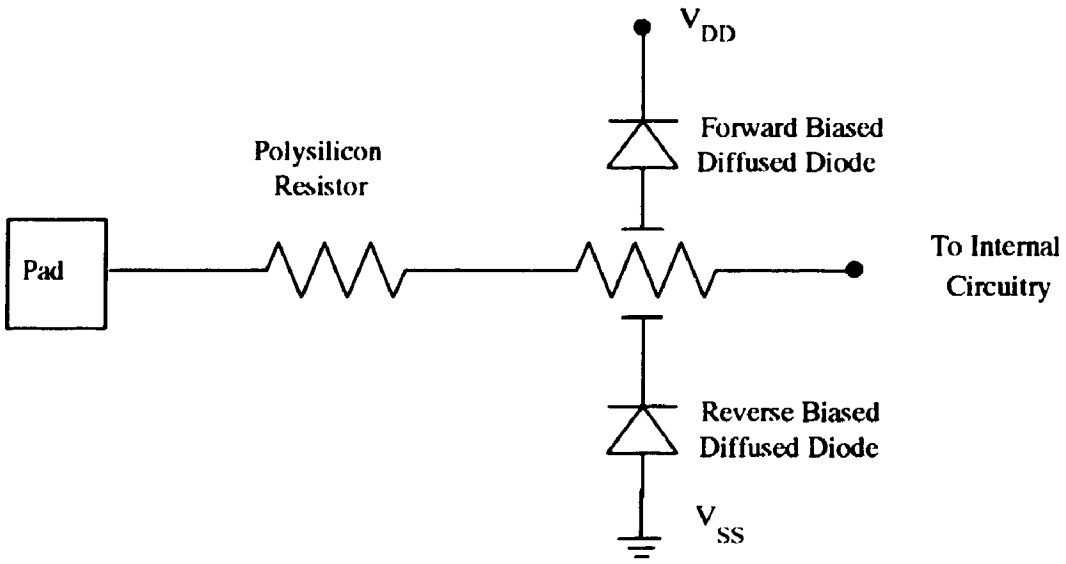


Figure 3.16 Schematic of the Diffused Diode Protection Circuit

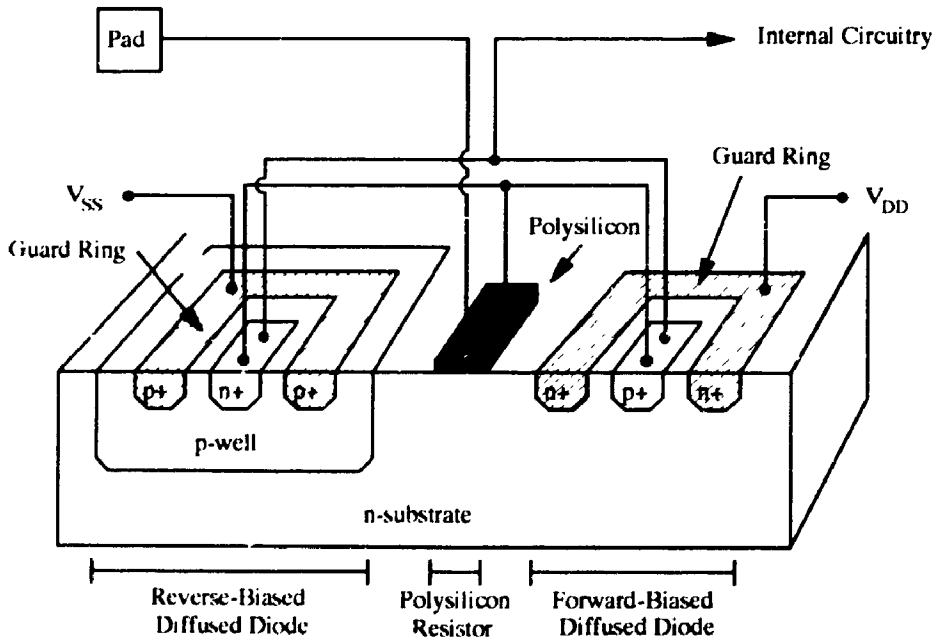


Figure 3.17 Cross-sectional View of the Diffused Diode Protection Circuit

Similar protection circuits with an input buffer were also investigated. The schematic, the cross-sectional view and the layout of a diffused diode input pad are shown in Figures 3.18, 3.19 and 3.20, respectively. The input buffers are used to recondition the input signal or to act as an interface for TTL to CMOS logic. TTL to CMOS logic conversion can be achieved by ratioing the inverter transistors or using a pull-up resistor. The schematic, the cross-sectional view and the layout of a diode input pad are shown in Figures 3.21, 3.22 and 3.23, respectively.

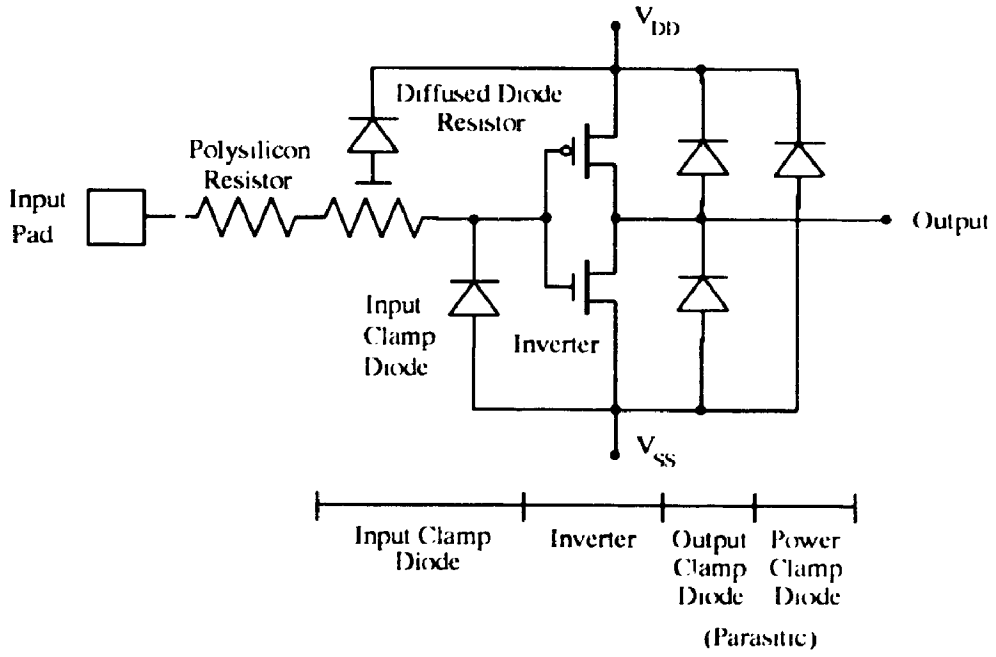


Figure 3.18 Schematic of the Diffused Diode Input Pad

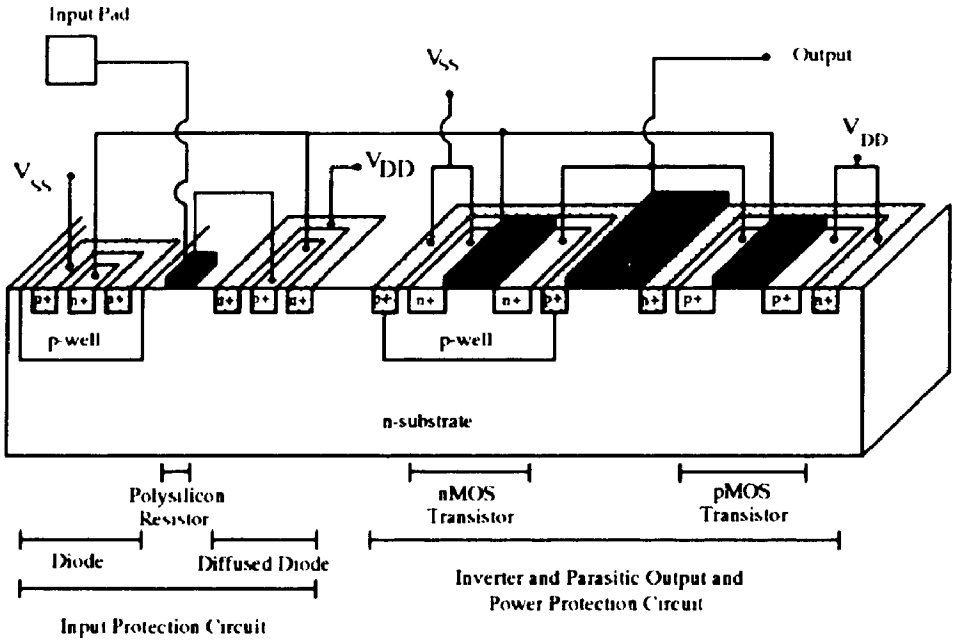


Figure 3.19 Cross-Sectional View of the Diffused Diode Input Pad

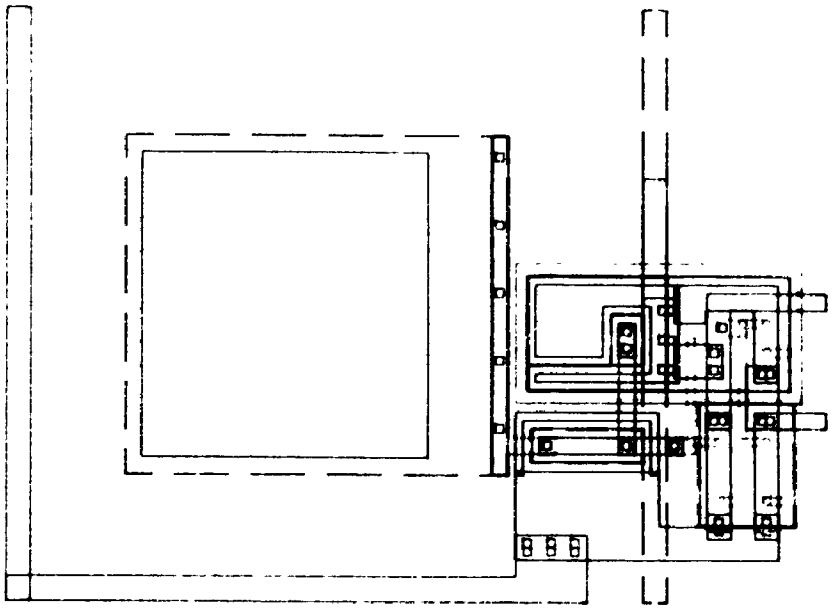


Figure 3.20 Layout of the Diffused Diode Input Pad

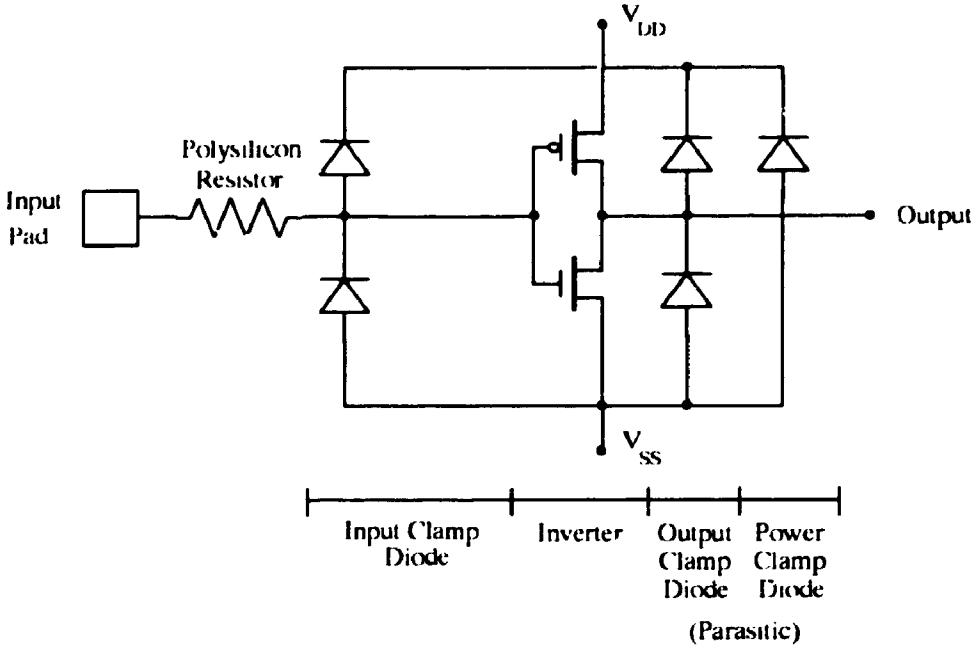


Figure 3.21 Schematic of the Diode Input Pad

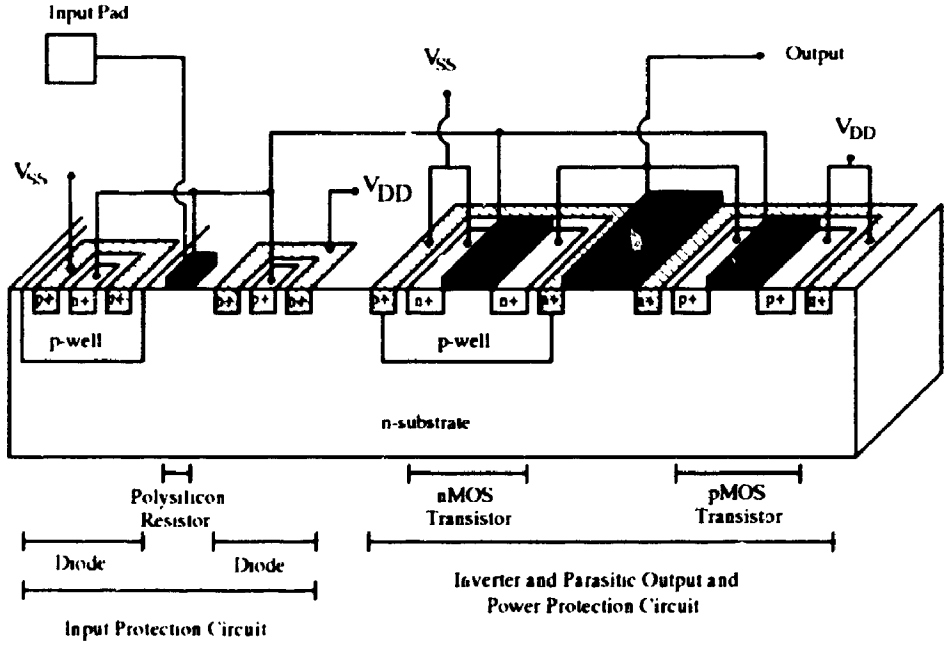


Figure 3.22 Cross-Sectional View of the Diode Input Pad

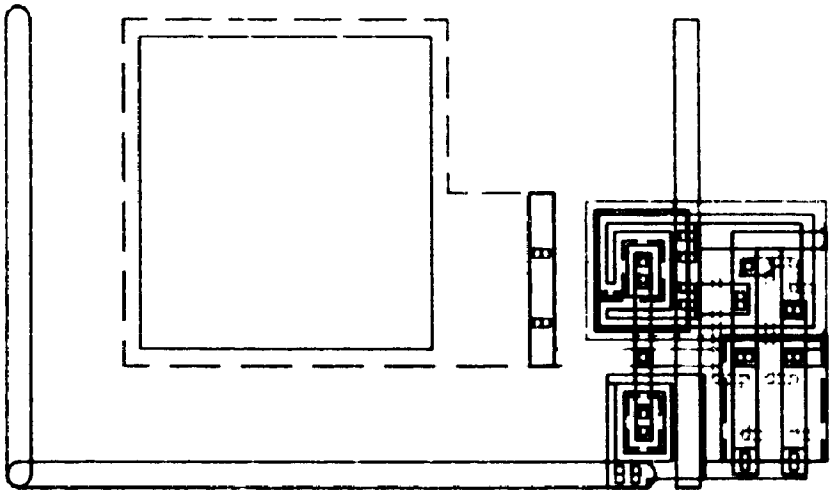


Figure 3.23 Layout of the Diode Input Pad

3.2.2 Output Protection Circuits

It is important for an output pad driver to have sufficient power to meet the rise and fall time requirements for a capacitive load. The size of the driving gate can be increased to meet this requirement. However, the response time of the transistor is directly proportional to load capacitance and indirectly proportional to the width-to-length ratio. The increase in the driving gate dimension will eventually load the preceding gate, decreasing thus the speed. A set of cascaded inverters is used to solve the problem, where their size varies according to the position in the series structure. The width of the inverter is larger than that of the preceding one by a stage ratio "n". A cascaded set of four inverters is shown in Figure 3.24.

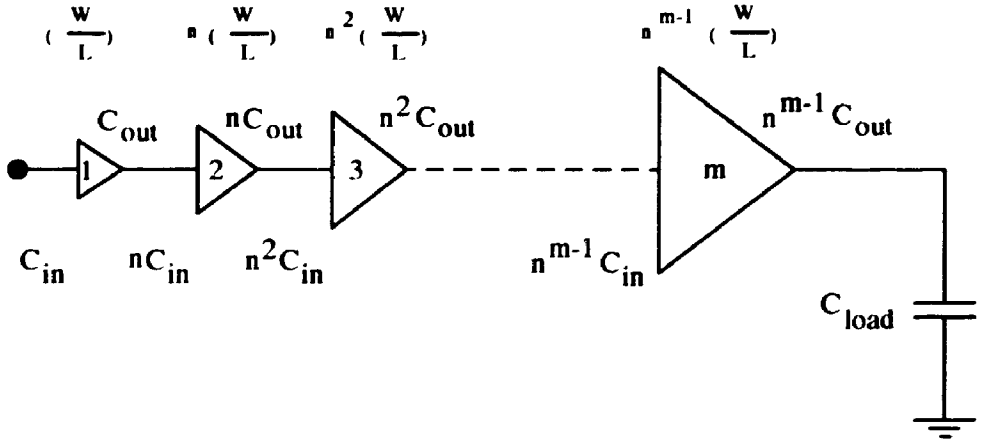


Figure 3.24 A Cascaded Output Buffer Circuit

Output pads, in general, inherently possess a reasonable degree of protection even though they are connected to layers separated by thin oxide from other nodes in the circuit. By their nature, the pads are directly connected to a diffused region which forms a parasitic diode, as shown in Figure 3.25. The circuit diagram and layout for the output pad are shown in Figures 3.26 and 3.27, respectively.

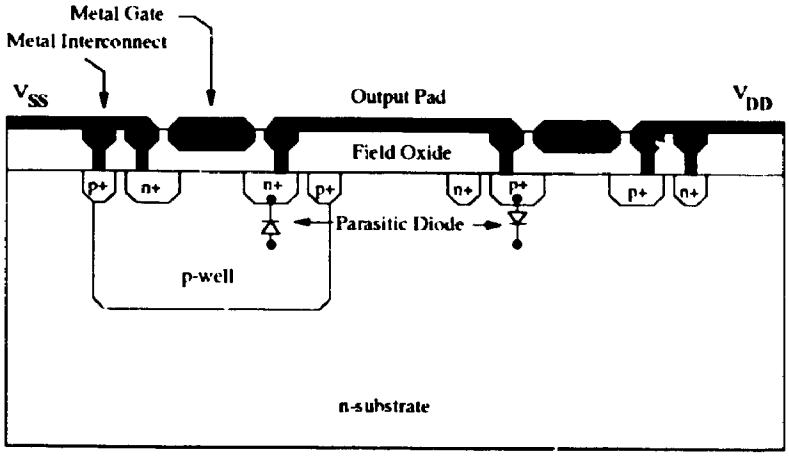


Figure 3.25 Parasitic Diodes in Output Pad

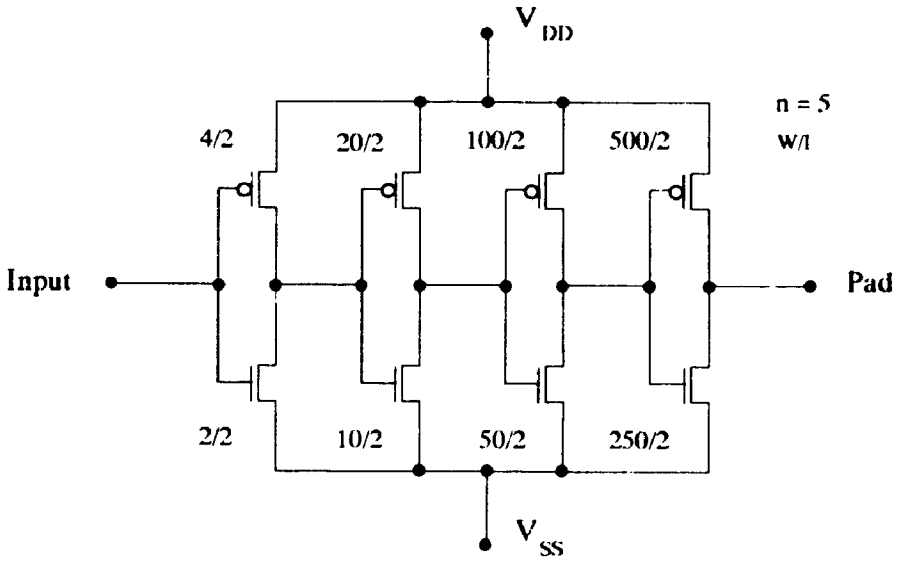


Figure 3.26 Circuit Diagram for the Output Pad

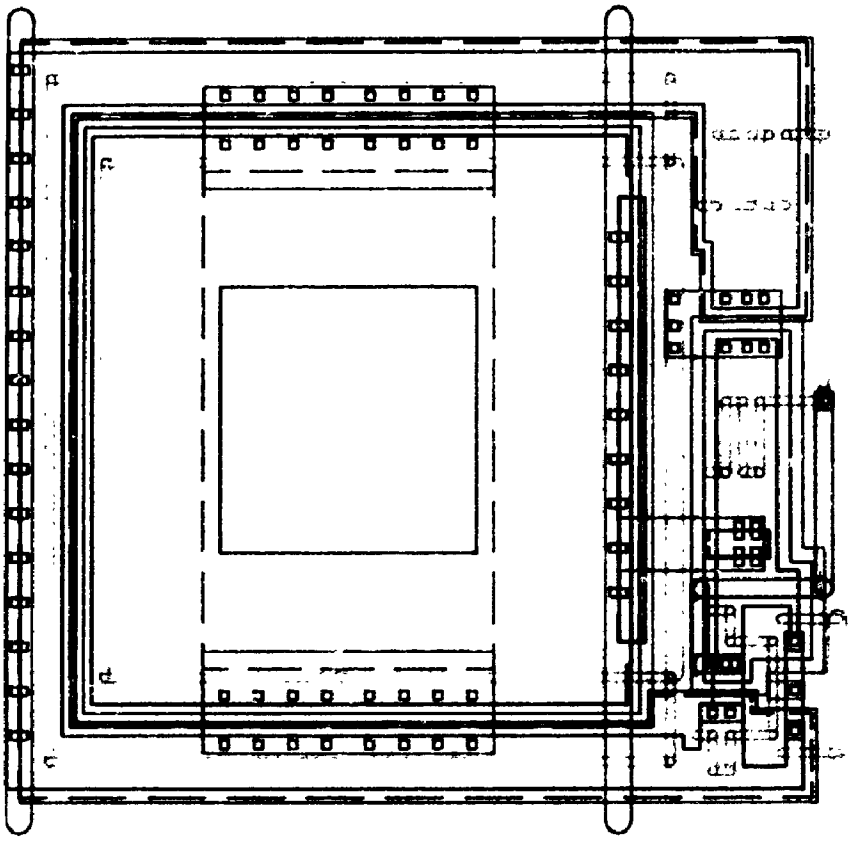


Figure 3.27 Layout of the Output Pad

3.3 Summary

Using the background developed in the previous chapters, a number of CCDs and protection circuits were designed and fabricated using a 3-micron single polysilicon, double metal p-well CMOS process. In order to prevent charge losses and trapping that may occur from the defects in the depletion profile in the gap area between gates, a two-level CCD gate structure was constructed using polysilicon and aluminium. Various 16-stage, two-phase CCDs with input diodes or photodiodes were fabricated for detailed analysis.

Since the inputs of MOS devices are separated from the rest of the circuit only by a thin oxide, a destructive voltage can be easily generated. Therefore, input protection circuitry must be used to prevent the thin oxide destructive breakdown due to overvoltage or overcurrent conditions. Several input protection structures were designed and fabricated to study the nature of the problem. In the next chapter, the static and dynamic electrical characteristics of these custom CMOS devices are examined in detail.

Chapter 4

Device Electrical Characteristics

Various tests were performed on the sample capacitors, diodes and transistors to measure the wafer electrical characteristics. Tests were divided into two groups to measure the static and dynamic electrical characteristics of the devices. The block diagram of the experimental setup is shown in Figure 4.1. The Hewlett-Packard 4145A semiconductor parameter analyzer was used as a programmable voltage and current source with built-in monitor units to analyze and display the DC characteristics of semiconductor devices. The Hewlett-Packard 4280A CV analyzer measured the capacitance and conductance of semiconductor devices and materials as a function of applied voltage or time. The Hewlett-Packard 8180A data generator and the Tektronix 7912AD programmable digitizer system were used to measure the dynamic characteristics of the samples. Similar arrangements were used to measure the properties of the protection networks. The following sections describe the main parameters that characterize the CCDs and protection networks fabricated in this project.

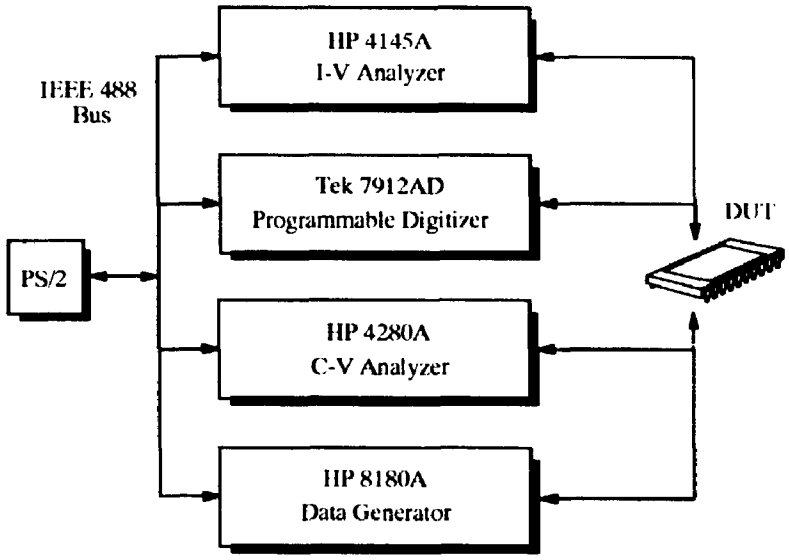


Figure 4.1 Block Diagram of the Experimental Setup

4.1 MOSFETs

Sample MOSFETs were tested to evaluate the electrical characteristics of the CMOS process. The channel width and length of the sample MOSFETs, as shown in Figure 4.2(a), were 18μm and 6μm, respectively. The size of these sample MOSFETs were the same as those used in the charge detection region (source-follower MOSFET) in the CCDs. Both n- and p-channel MOSFETs were studied.

The most important parameter for a MOS transistor is the threshold voltage, defined as the voltage at which a MOS device begins to conduct. The threshold voltage is a function of a number of parameters, namely:

(1) Gate insulator thickness

(2) Gate insulation material

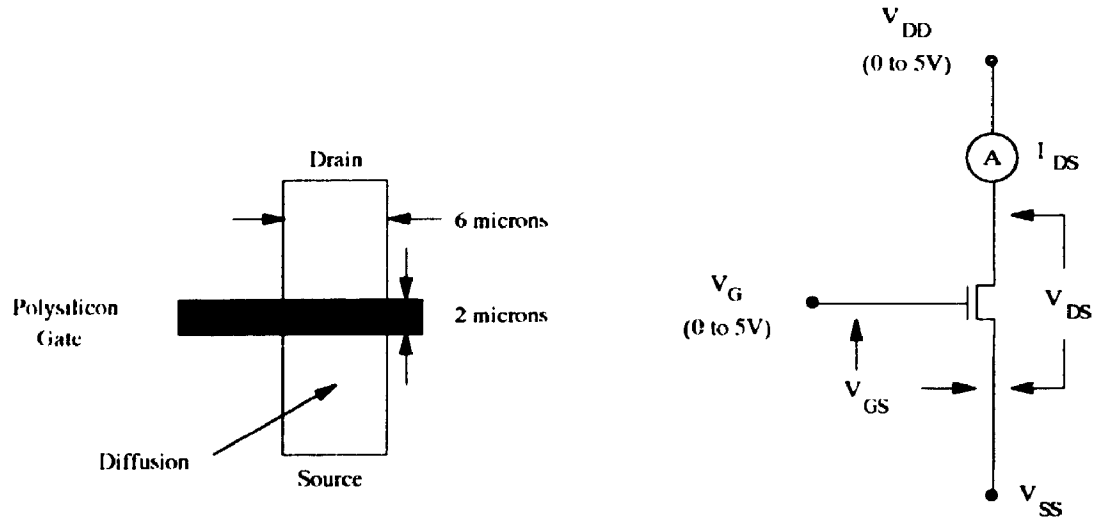


Figure 4.2 MOSFET Test Circuit

(3) Gate material

(4) Channel doping

(5) Impurities at the silicon-insulation or dielectric interface

(6) Voltage between the source and substrate

(7) Temperature

The threshold voltage for the n and p MOSFETs were obtained using the test circuit shown in Figure 4.2(b). Typical threshold voltages, as illustrated in Figures 4.3 and 4.4, were 0.7 and -0.8 volts respectively.

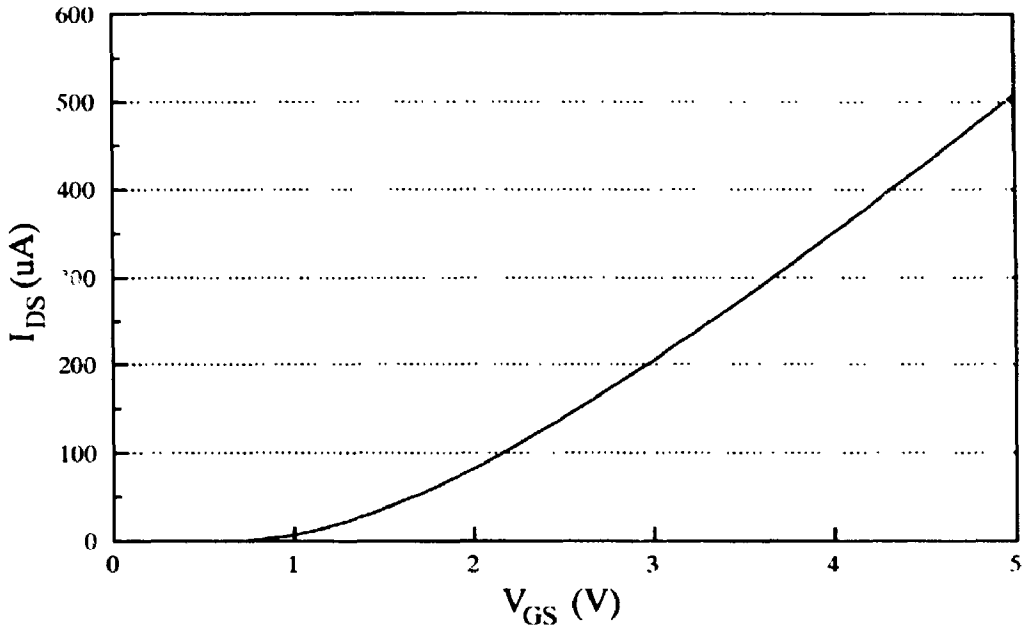


Figure 4.3 Typical Drain Current versus Gate-Source Voltage of the nMOSFET

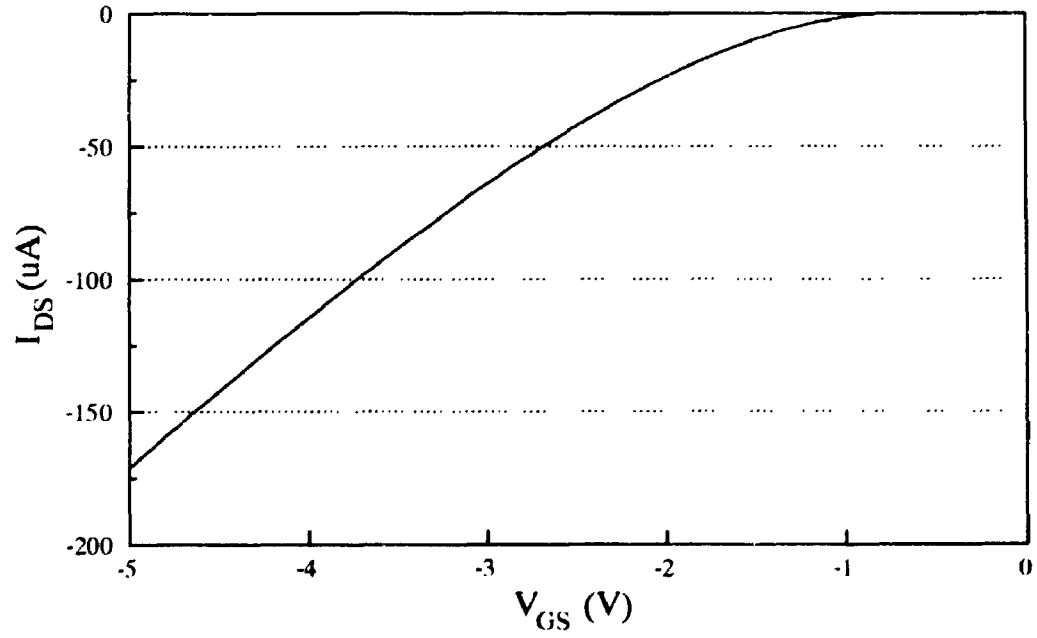


Figure 4.4 Typical Drain Current versus Gate-Source Voltage of the pMOSFET

The V-I characteristics of the MOSFET were also studied and results used as an aid in determining the electrical characteristics of the source-follower MOSFET used in the charge detection region in the CCDs.

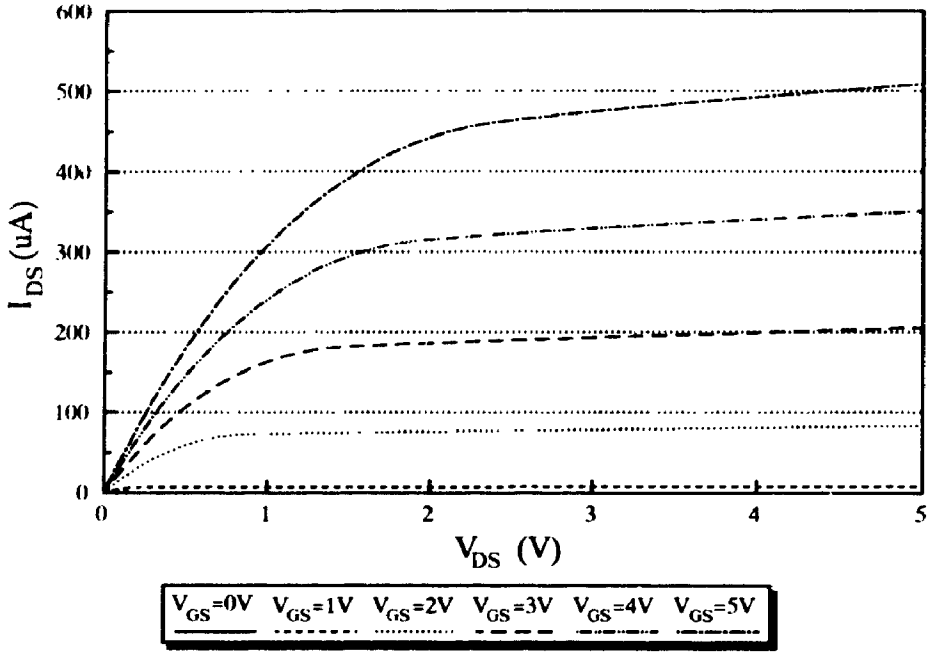


Figure 4.5 Typical V-I Characteristics of the nMOSFET

Using the data shown in Figure 4.5 and 4.6, the transconductance (g_m) and drain resistance (r_d) were derived for each type of MOSFET at V_{DS} = 5V. The electrical characteristics of the MOSFETs are tabulated in Table 4.1.

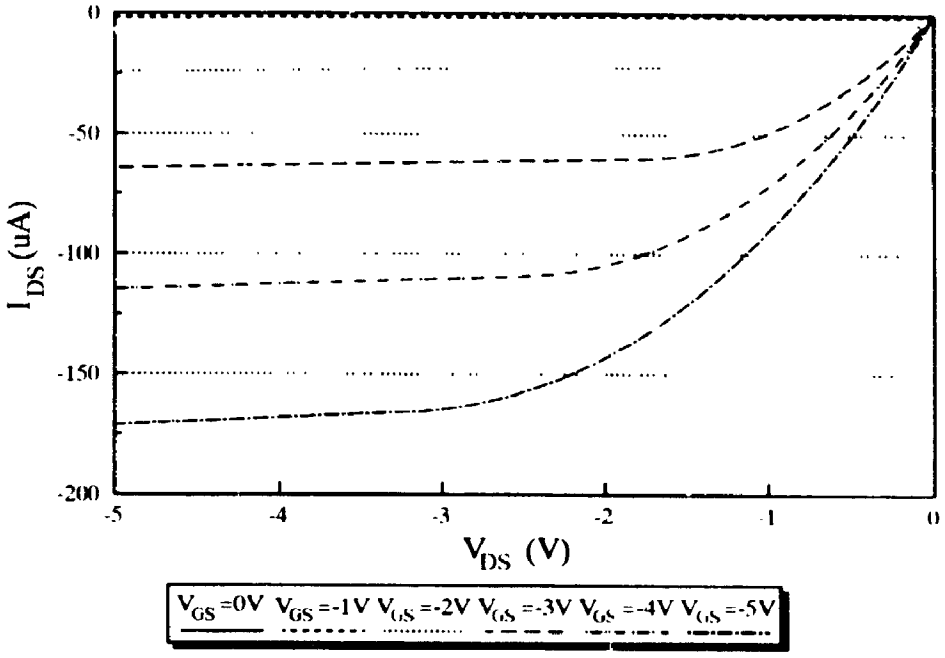


Figure 4.6 Typical V-I Characteristics of the pMOSFET

$$g_m = \frac{\Delta I_{DS}}{\Delta V_{GS}}\Big|_{V_{DS}=5V} \qquad \ldots(4.1)$$

$$r_d = \frac{\Delta V_{DS}}{\Delta I_{DS}}\Big|_{V_{GS}=constant} \qquad \ldots(4.2)$$

where :

g_m = transconductance

I_{DS} = drain current

V_{GS} = gate-to-source voltage

V_{DS} = drain-to-source voltage

r_d = drain resistance

Table 4.1 Electrical Characteristics of MOSFETs

	nMOSFET	pMOSFET
N_A ($1/cm^3$)	$1.7x10^{16}$	$5.0x10^{15}$
V_T (V_{sub} = 0V)	0.7	-0.8
g_m (μA/V)	140	55
r_d (kohm)	100	330

4.2 Charge-Coupled Devices

Tests were performed on shift register cells to determine their charge handling capacity, maximum storage time, maximum operating speed and transfer efficiency. The layout of a CCD shift register cell is shown in Figure 4.7.

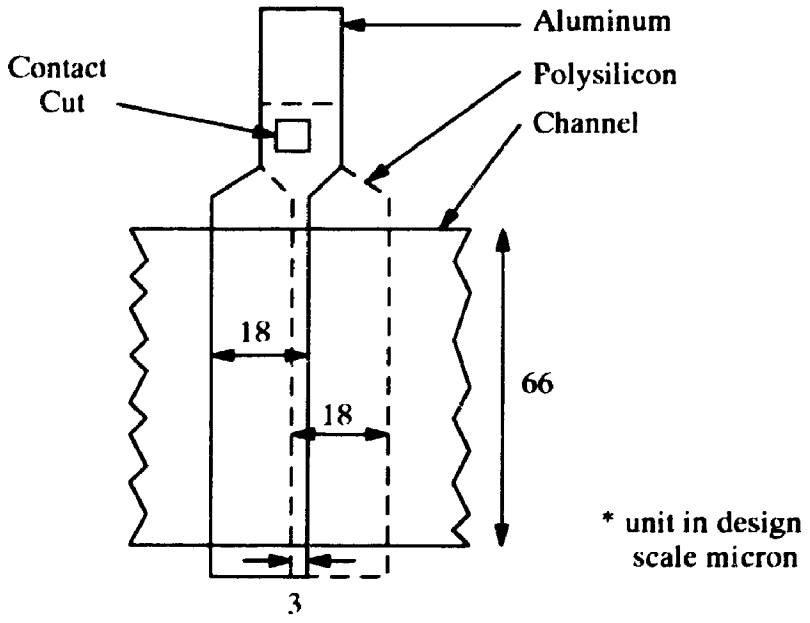


Figure 4.7 Layout of CCD Shift Register Cell

The maximum gate voltage that can be applied to a MOS-C depends on the integrity of silicon and silicon dioxide during the high electric field created by the gate bias pulse. The maximum electric field in the silicon occurs when the potential well generated by the gate bias pulse is empty. The typical breakdown field for silicon is $3x10^5$V/cm. From Appendix A, the substrate electric field strength is given by:

$$E_{si} = \left(\frac{2qN_A}{\varepsilon_{si}} (V_G - V_T) \right)^{1/2} \qquad \ldots(4.3)$$

where :

E_{si} = electric field strength in silicon

q = magnitude of electron charge

N_A = acceptor doping density

ε_{si} = permittivity of silicon

V_G = gate voltage

V_T = threshold voltage

From the previous measurements, the threshold voltage was measured to be 0.7 volts. The acceptor doping density, as provided by Northern Telecom Electronics, was $5x10^{15}/cm^3$. Using this data, the maximum gate voltage was calculated to be 59.1V. Although theoretically, a 51.9 volt clock signal would produce the maximum charge capacity, a lower voltage was chosen for testing the devices after taking in account the breakdown voltage of silicon dioxide. The maximum electric field for silicon dioxide is in the 5MV/cm to 10MV/cm range. For this particular CMOS process (with 50 nm gate oxide), the oxide breakdown occurs between 25V to 50V (or less because of oxide imperfections). Therefore, the "high" and "low" level voltages of the clock signal were set at 5V and 1V respectively. The "low" level voltage was chosen slightly above the

gate threshold voltage to prevent the depletion region under the gate from collapsing. This ensures that no signal charge is accidentally injected into the substrate. The timing diagram used to test the devices is shown in Figure 4.8.

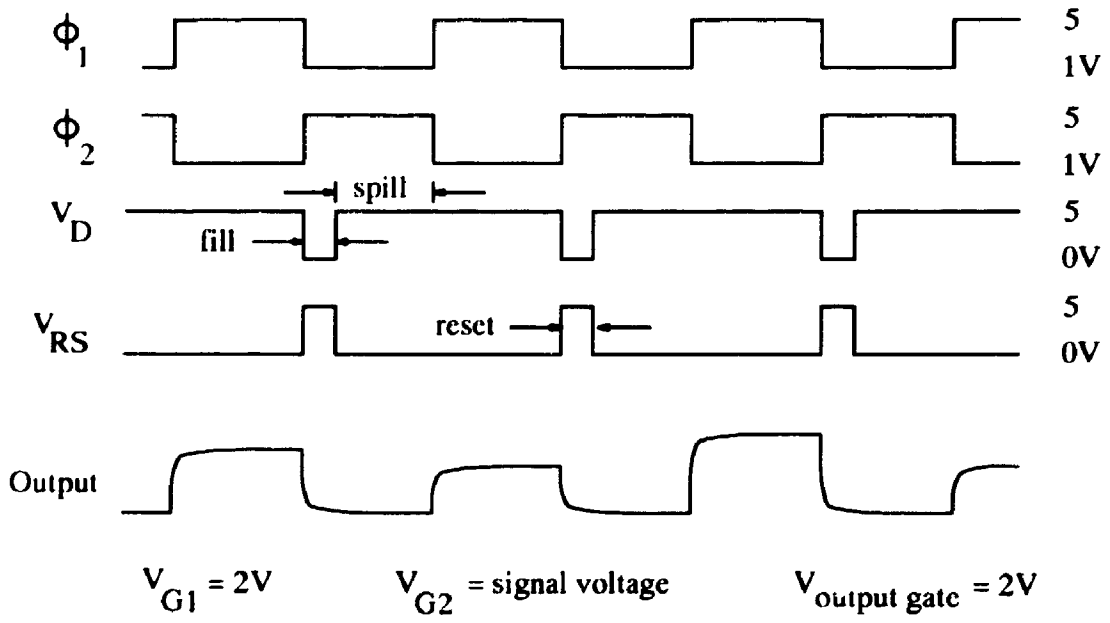


Figure 4.8 Operating Input and Output Voltage Waveforms

The signal charges shown in Figure 4.9 were injected into the device using the "fill and spill" method discussed in Section 3.1. The input signal voltage was applied to G2 with G1 as the reference node. In these experiments, G1 was set to 2V so that the region underneath the gate was sufficiently depleted to allow charge to flow from the input diode (D) to the well under G2. Since the input charge packet is proportional to the input voltage, the magnitude of the input voltage should be as large as possible. The timing relationship for the input signal voltage and the input diode voltage are shown in Figure 4.8.

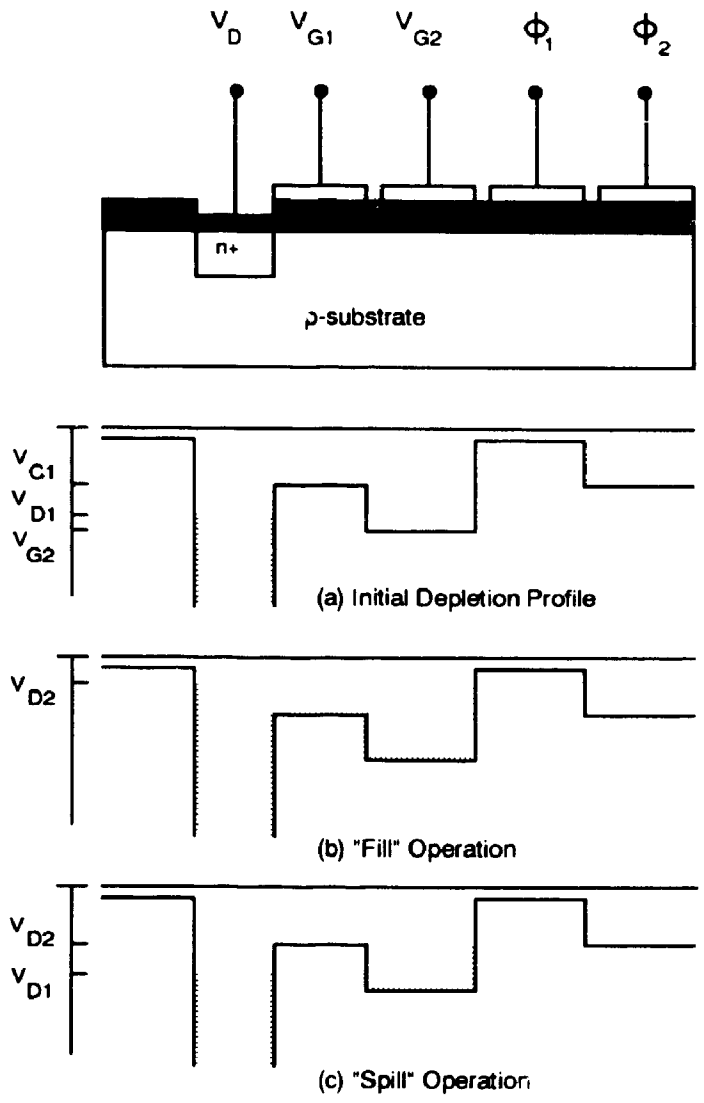


Figure 4.9 Input Structure of CCDs Used in the Experiments

The charge packets were converted into voltage by connecting the gate of a source-follower MOSFET to the floating diffusion island described in Section 3.2. In these experiments, the load resistor was 10 kohm and the supply voltage for the MOSFET was 5V. The reset drain was connected to a 5V supply. The voltage waveforms are shown in Figure 4.8. The capacitance of the floating diffusion island

was measured to be 0.1pF. Using equation (3.2), the charge to voltage conversion ratio is $V_{out} = 5.6 \times 10^{13} Q$. For the two-phase clocking scheme used in these experiments, the maximum charge capacity was calculated as follows:

$$Q = -C_{ox}(\phi_{s2} - \phi_{s1}) \qquad \ldots(4.4)$$

where :

- Q = signal charge
- C_{ox} = gate oxide capacitance
- ϕ_{s1} = surface potential underneath aluminium gate
- ϕ_{s2} = surface potential underneath polysilicon gate

The relationship between the applied gate voltage and the surface potential can be obtained using [APPENDIX A] :

$$\phi_s = V_G + \frac{Q_N}{C_{ox}} - V_0 \left\{ \left(1 + \frac{2\left(V_G + \frac{Q_N}{C_{ox}}\right)}{V_0} \right)^{1/2} - 1 \right\} \qquad \ldots(4.5)$$

where :

- V_G = gate voltage
- ϕ_s = surface potential
- C_{ox} = oxide capacitance per unit area
  = $\varepsilon_{SiO_2} / d_{ox}$
- d_{ox} = gate oxide thickness
- ε_{SiO2} = permittivity of silicon dioxide
- ε_{si} = permittivity of silicon
- N_A = acceptor doping concentration
- q = magnitude of electron charge
- V_0 = $q\varepsilon_{Si}N_A / C_{ox}^2$
- Q_N = inversion charge

When no inversion charge ($Q_N = 0$) is present, *i.e.* total deep depletion, the surface potential is at a maximum.

$$\phi_s(Q_N = 0) = V_G - V_0\left\{\left(1+\frac{2V_G}{V_0}\right)^{1/2} - 1\right\} \qquad \ldots(4.6)$$

The oxide thicknesses under the polysilicon and aluminum gates were measured to be 50 and 300 nm respectively. The gate oxide capacitance of the polysilicon and aluminum gate were calculated to be 69 x 10^{-9} and 11.5 x 10^{-9} F/cm^2, respectively. The surface potential versus gate voltage plot, for an acceptor doping concentration of 5.0 x 10^{15} cm^{-3}, is shown in Figure 4.10. During the "high" and "low" levels of the clock signal, the surface potential difference underneath the aluminum and the polysilicon gate were 2.2V and 0.3V respectively.. Using equation 4.4, the maximum charge which can be handled by this two-phase CCD structure using the clocking scheme is 1.52 x 10^{-7} C/cm^2. The storage area under the polysilicon gate was 428μm^2 (66 x 18 = 1188 design scale μm^2 = 1188 x 0.6 x 0.6 μm^2 = 428 μm^2) and the device charge capacity was calculated to be 0.65pC. The maximum theoretical output voltage was calculated to be 3.64V using the charge to voltage conversion ratio. The voltage waveforms shown in Figure 4.8 show the actual output voltage of 3.9V. The number of samples used in this measurement was 5; the standard deviation ± 0.11V.

The maximum and minimum clock frequencies were also investigated. The upper limit is determined by the charge-transfer inefficiency. The lower limit is determined by the thermally generated leakage current that adds charge to the potential wells, thus distorting the signal.

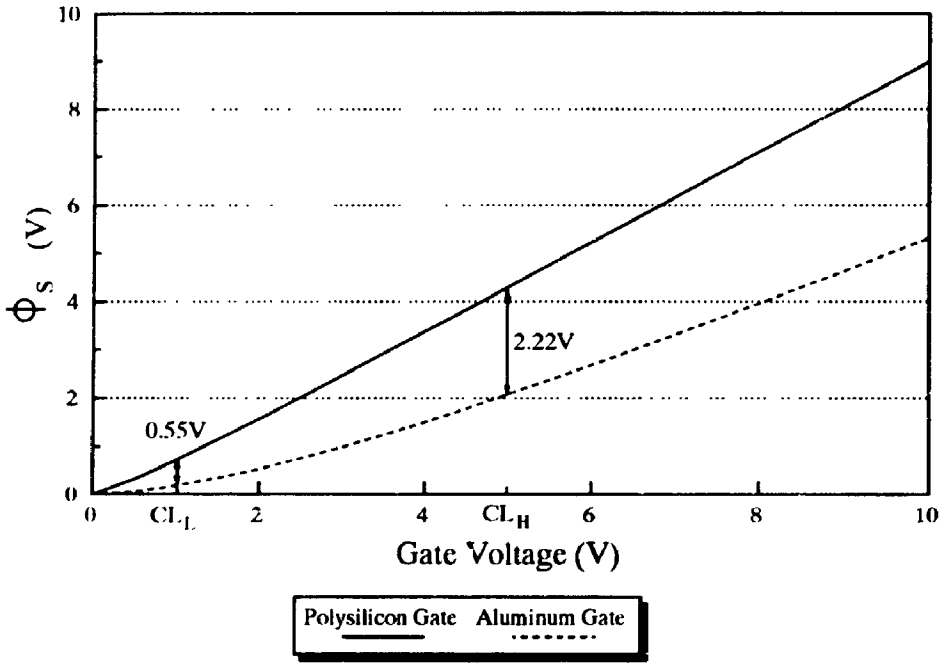


Figure 4.10 Surface Potential Versus Gate Voltage for $N_A = 5.0 \times 10^{15} cm^{-3}$

In the previous analysis, the charge transfer from one potential well to the next is assumed to be perfect, *i.e.* no charge loss occurs. However, in a real situation, charge loss can occur due to the following factors:

(1) Insufficient time for the charge to flow from one well to the next well, due to a high clock frequency,

(2) Charge is captured by interface states and the emission time is longer than the transfer time,

(3) Potential barriers between wells due to an improper gate voltage.

Under normal operation, there are no potential barriers between wells. Therefore, in most cases, the third mechanism is usually not considered. The charge transfer inefficiency, ε, or the charge transfer efficiency, $\eta = 1 - \varepsilon$, can be measured using the method shown in Figure 4.11.

$$\varepsilon = \left(\frac{V_i}{V_j}\right)\frac{1}{N} \qquad \ldots(4.6)$$

where :

ε = charge transfer inefficiency per stage

V_i = voltage in stage i

V_j = voltage in stage j

N = number of stages

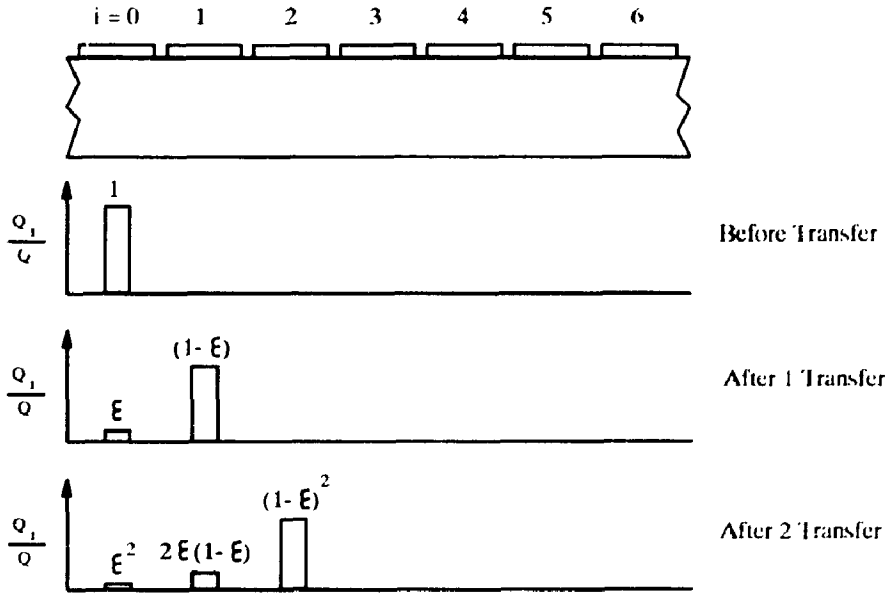


Figure 4.11 Measurement of Charge Transfer Inefficiency

Mechanism 1 can be separated from mechanism 2, since the charge transfer inefficiency due to a high clock frequency is frequency dependent, whereas the charge transfer inefficiency due to charge trapping is frequency invariant. At low and intermediate frequencies, the interface trapping dominates the inefficiency; at high frequencies, the carrier ballistics dominates. A typical charge transfer inefficiency versus clock frequency plot is shown in Figure 4.12.

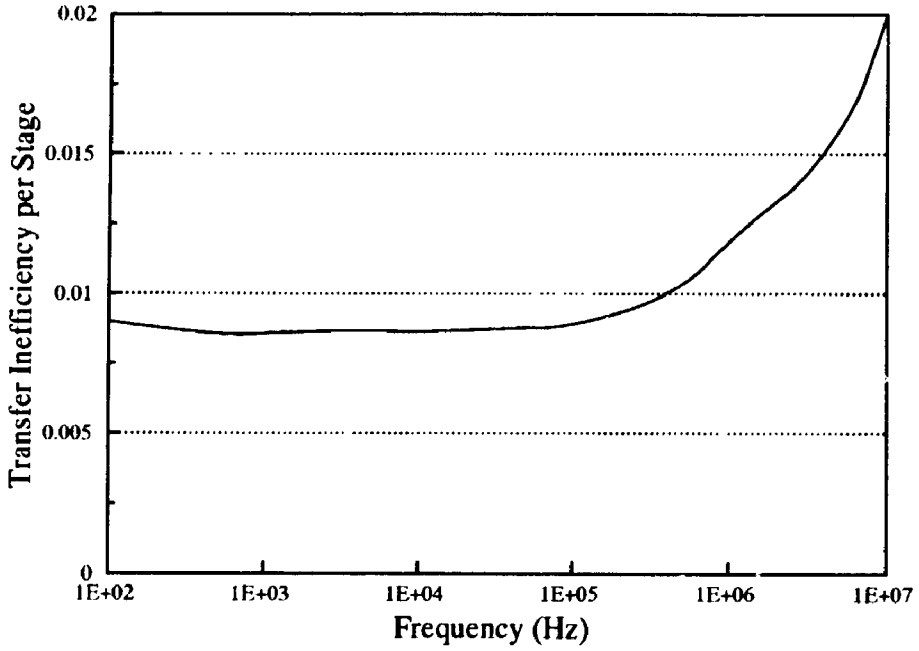


Figure 4.12 Typical Charge Transfer Inefficiency versus Clock Frequency

The minimum operating frequency of a CCD is limited by dark charge build-up in the photoelements and the transfer stages. The thermally generated electrons can add charge to the potential wells and distort the signal. In other words, the more thermal charge resides in the potential well, the less room remains for signal charges. The thermal charge build-up is proportional to time and strongly depends on temperature. Usually, the dark signal doubles for every 10°C increase in temperature. Both bulk

(within the depleted region) and the surface of the semiconductor contribute to the dark charge generation. Therefore, the performance of both buried-channel and surface-channel devices can be affected by dark charge. A typical plot of dark charge buildup versus integration time is shown in Figure 4.13.

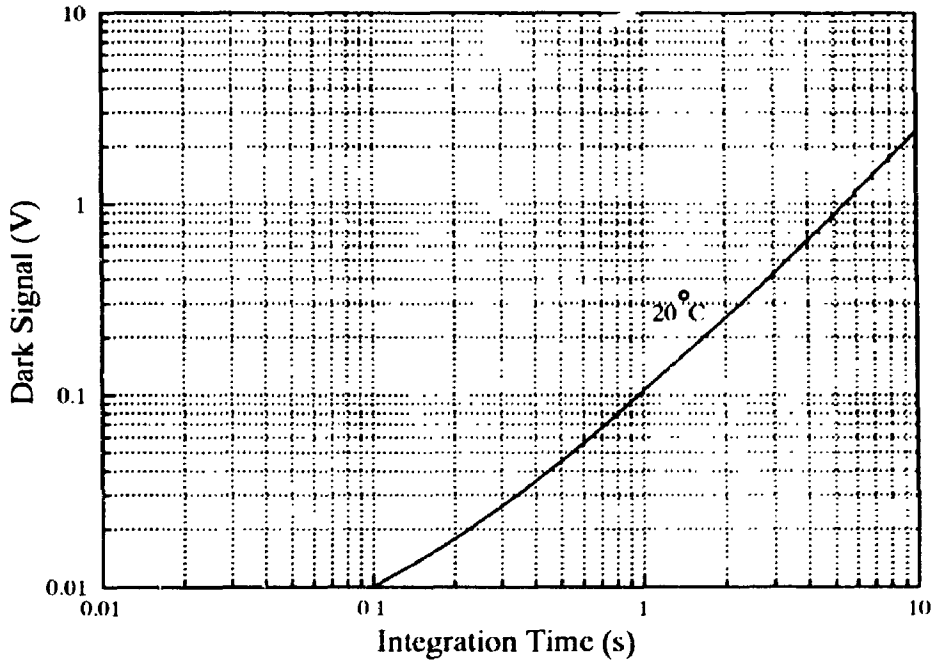


Figure 4.13 Typical Dark Charge Buildup versus Integration Time

4.3 Protection Circuits

Various tests were performed on individual protection elements and complete protection circuits to determine their ESD immunity. Both static and dynamic responses were studied and analyzed using the setup shown in Figure 4.1. A description of the electrical characteristics of the devices is presented.

4.3.1 Input Protection Circuits

The protection circuits used in this project are comprised of the input pads connected through a small polysilicon resistor to a reverse-biased and a forward-biased diodes that nondestructively break down or conduct at voltages below the critical gate oxide breakdown voltage. Typical V-I characteristics of a pn and pn diffused diode are shown in Figures 4.14 and 4.15, respectively. The input current was limited to 100mA to protect the diodes from destruction. These diodes provide protection through reverse breakdown or normal forward-biased condition. From measurements, the typical forward-biased conduction voltage was -0.8V and the reverse breakdown 20V. As shown in Figure 4.15, the diffused diode was more effective in protecting the internal circuit from over-voltage; the slope of the voltage curve was more gentle than that of the pn diode during the forward conduction.

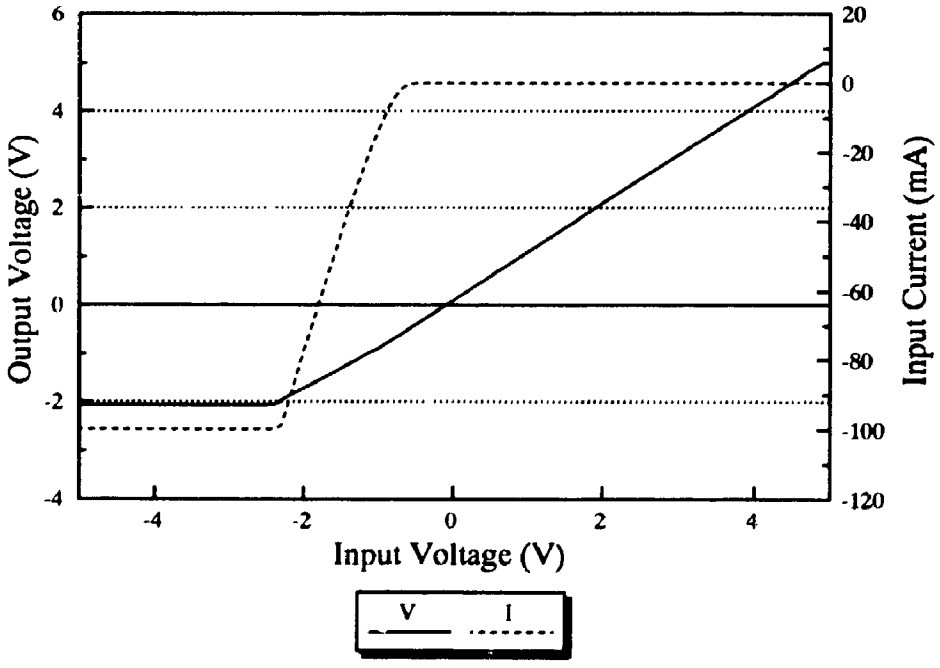


Figure 4.14 Typical I-V Characteristics of the Custom Fabricated pn Diode

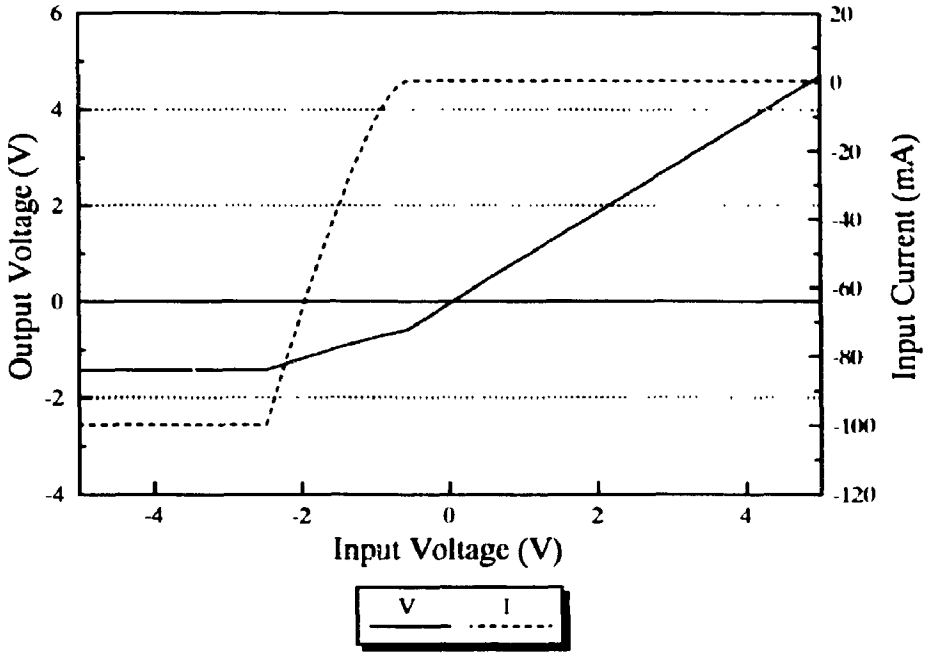


Figure 4.15 Typical I-V Characteristics of the Custom Fabricated pn Diffused Diode

The V-I characteristics of the np and np diffused diodes are shown in Figures 4.16 and 4.17 respectively. Opposite to the pn diodes, these diodes provide protection through normal forward-biased conduction if the input is positive, and through the reverse breakdown voltage if the input is negative. The forward-biased conduction and reverse breakdown voltages were 5.7V and -20V respectively. Similar to pn diffused diodes, np diffused diodes were more effective for clamping over-voltages.

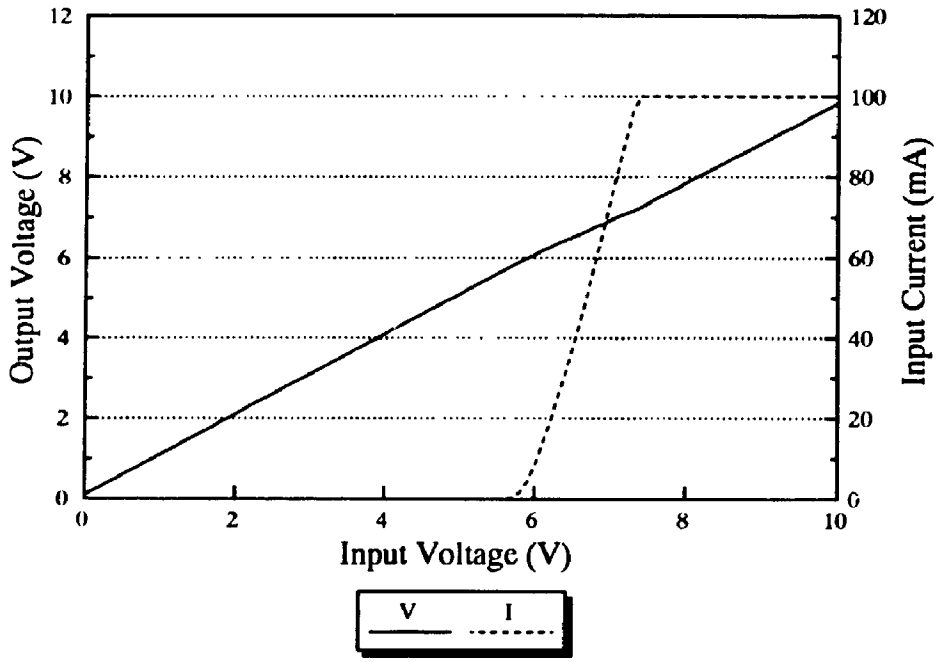


Figure 4.16 Typical I-V Characteristics of the Custom Fabricated np Diode

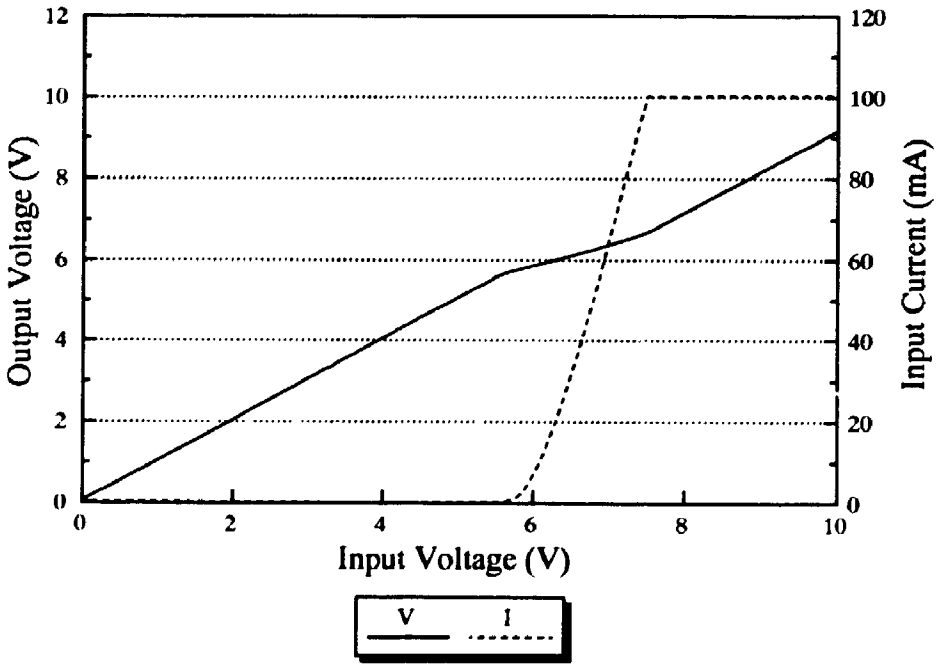


Figure 4.17 Typical I-V Characteristics of the Custom Fabricated np Diffused Diode

The measured static electrical characteristics of two types of input pads are shown in Figures 4.18 and 4.20. The V-I transfer characteristics of input pad #1 and #2 are shown in Figures 4.19 and 4.21, respectively. The transfer characteristics of both devices were quite similar because they had the same input buffer.

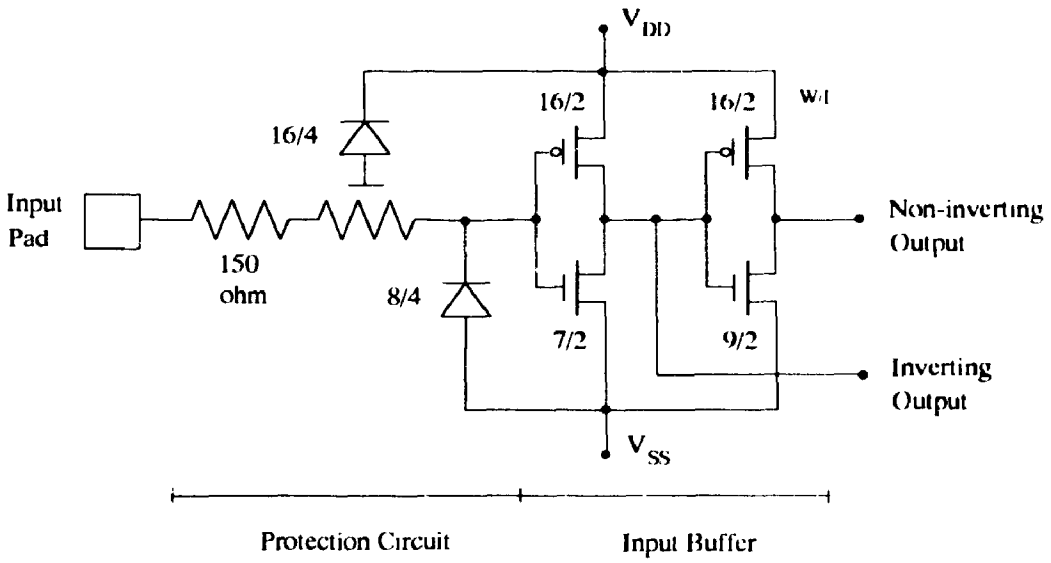


Figure 4.18 Circuit Diagram of the Input Pad #1

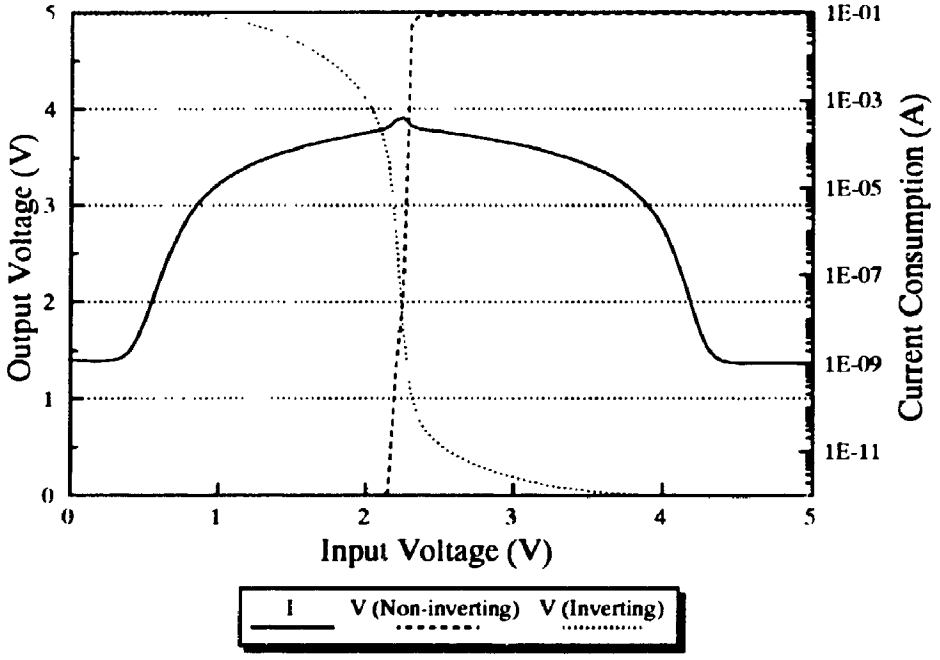


Figure 4.19 Typical I-V Characteristics of Input Pad #1

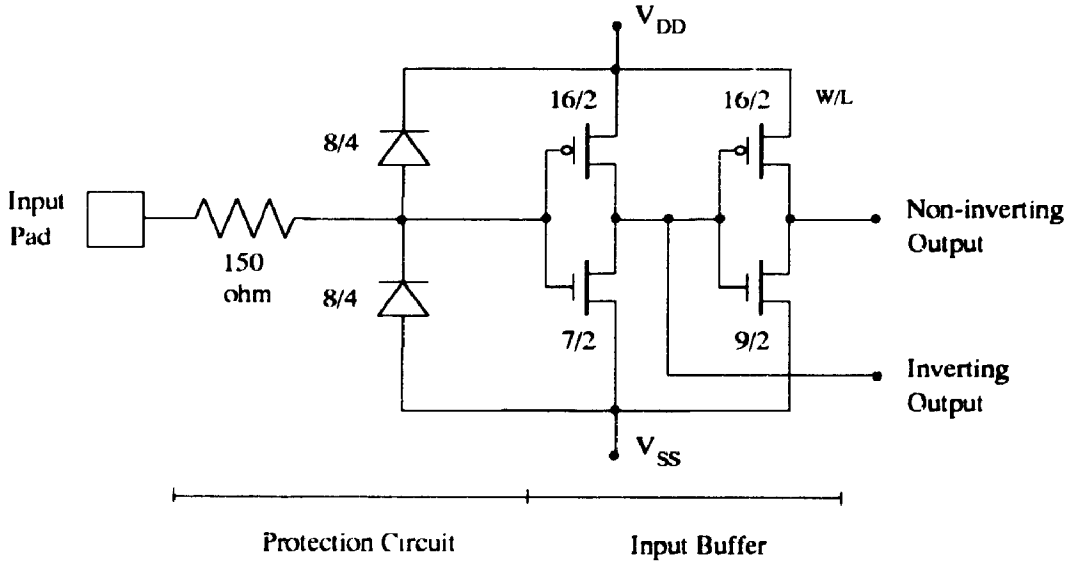


Figure 4.20 Circuit Diagram of the Input Pad #2

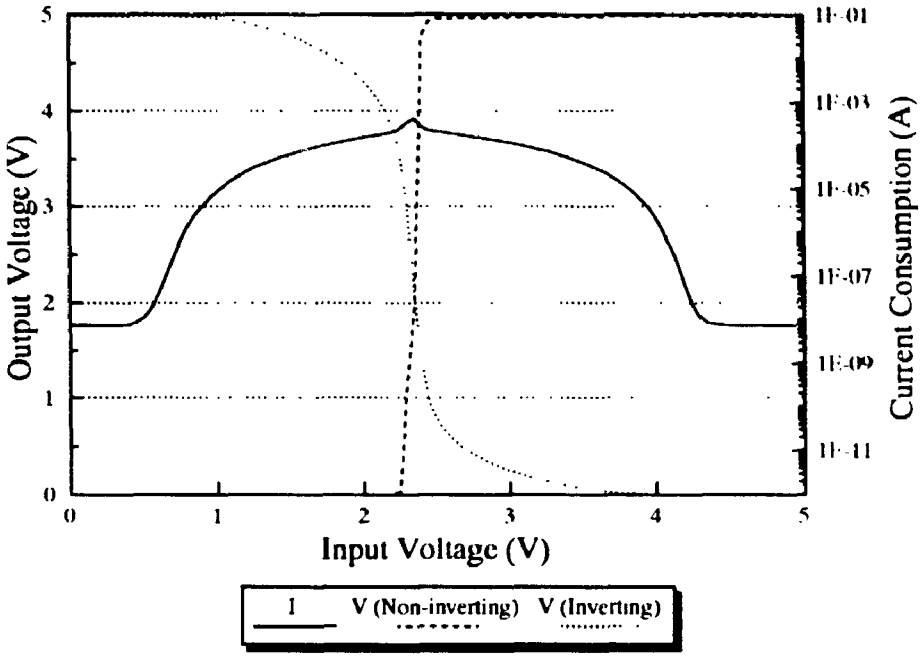


Figure 4.21 Typical I-V Characteristics of Input Pad #2

The dynamic characteristics of the input pads, as shown in Figures 4.22 and 4.23, were also studied using the setup shown in Figure 4.1. The results of both devices are tabulated in Table 4.2.

Table 4.2 Switching Characteristics of Input Pad

Input Pad	Transition Time (ns)		Propagation Delay (ns)	
	t_{Tr}	t_{Tf}	t_{Pr}	t_{Pf}
#1	80	50	20	20
#2	80	50	20	20

** T_A=25°C; V_{dd}=5V; Input t_r,t_f=10ns, Load Impedance=10pF

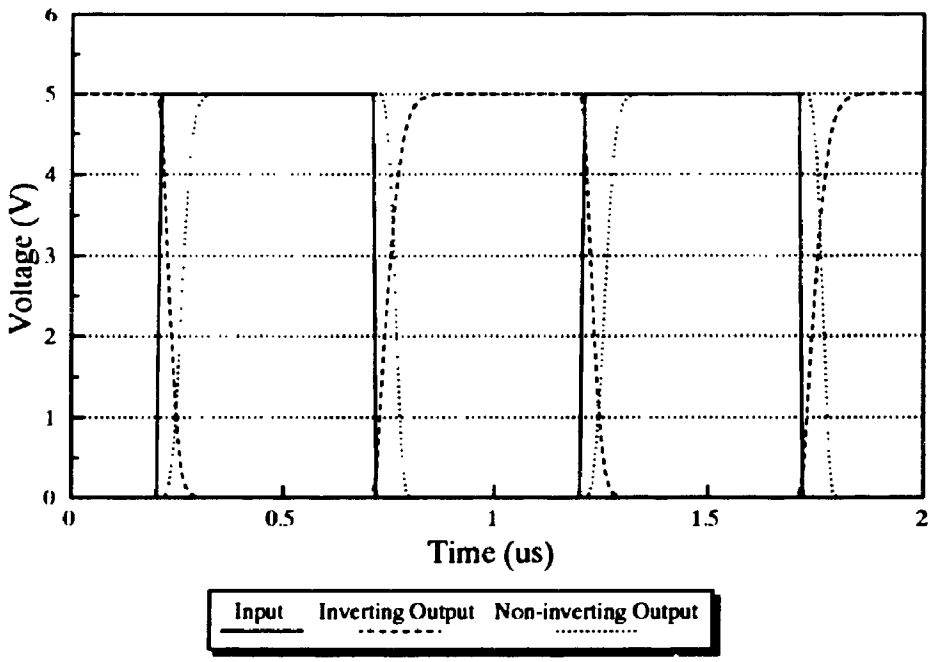


Figure 4.22 Typical Dynamic Response of Input Pad #1

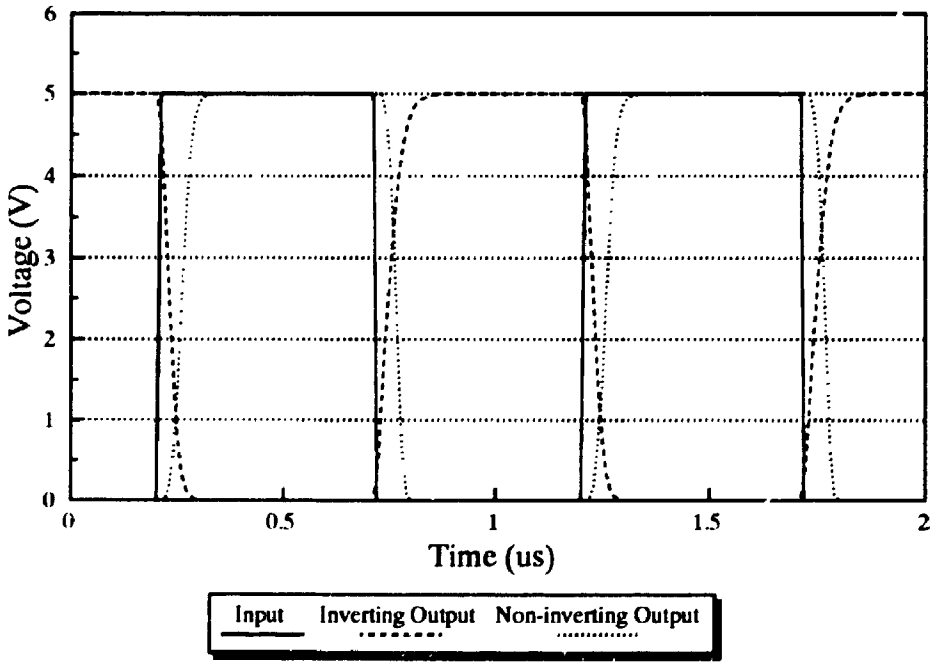


Figure 4.23 Typical Dynamic Response of Input Pad #2

4.3.2 Output Protection Circuits

Measurements of the static and dynamic characteristics were also performed on the output pad shown in Figure 4.24. The static characteristics of the output pad with a 4-stage buffer are shown in Figure 4.25, and the dynamic response of the output pad is shown in Figure 4.26 and tabulated in Table 4.3.

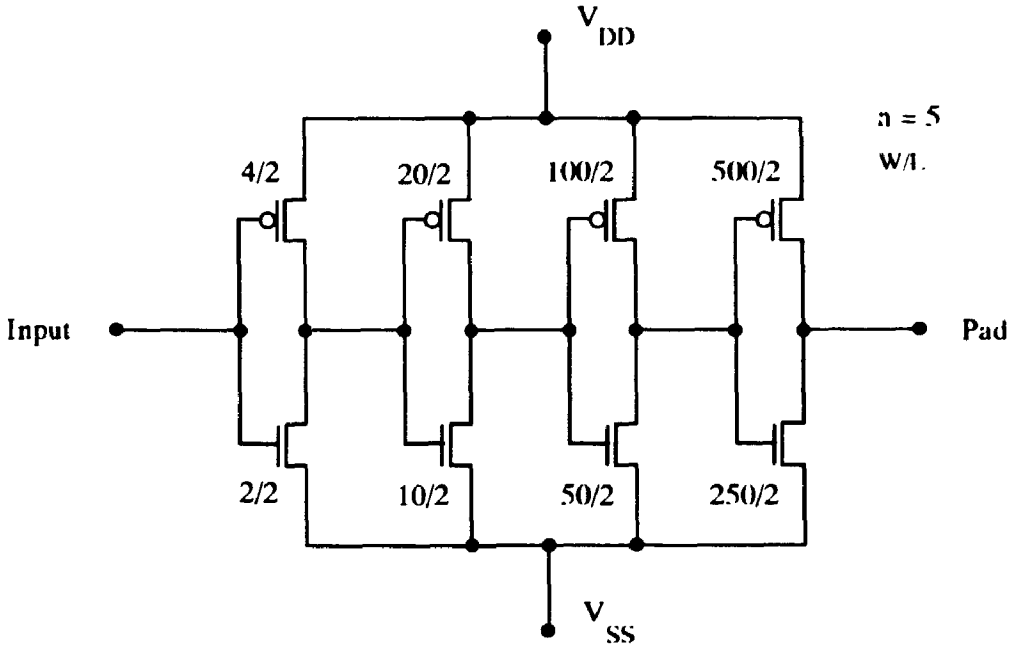


Figure 4.24 Schematic of Output Pad

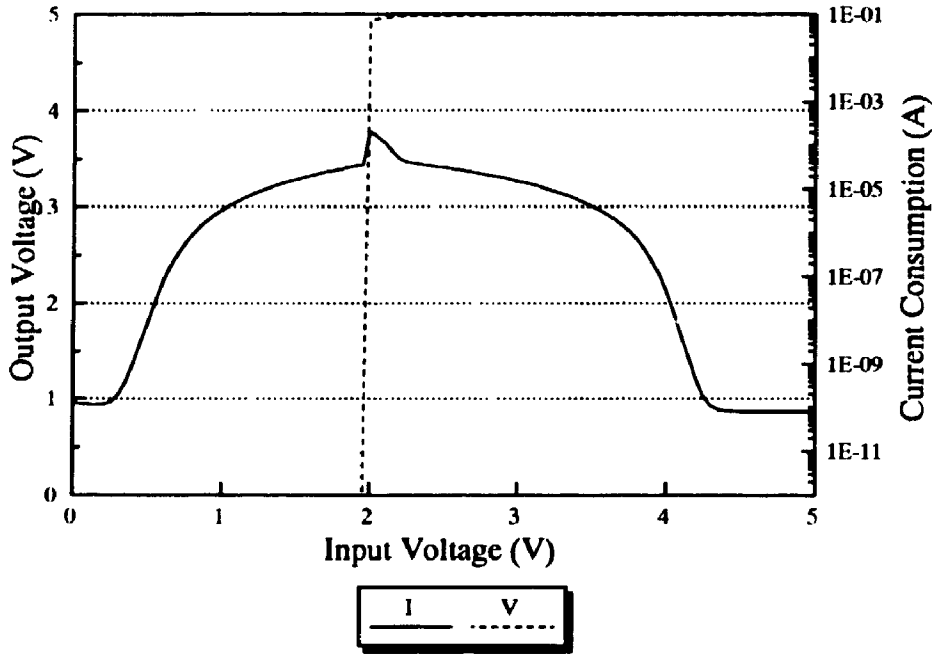


Figure 4.25 Typical I-V Characteristics of Output Pad

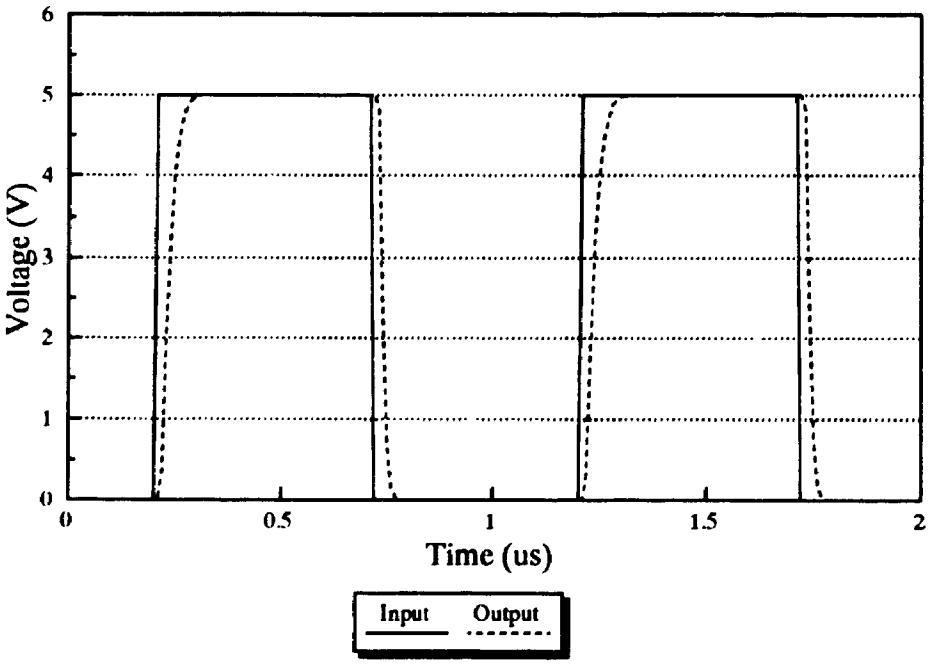


Figure 4.26 Typical Frequency Response of Output Pad

Table 4.3 Switching Characteristics of Output Pad

Output Pad	Transition Time (ns)		Propagation Delay (ns)	
	t_{Tr}	t_{Tf}	t_{Pr}	t_{Pf}
#1	20	20	10	10

** T_A=25°C; V_{dd}=5V; Input t_r,t_f=10ns, Load Impedance=50pF

4.4 Summary

A number of tests were performed on custom fabricated CCDs and protection networks to study their static and dynamic electrical characteristics during normal operation. Calculation methods for obtaining the maximum electric field strength, phase voltage, surface potential, transfer inefficiency and dark current build-up of CCDs were also discussed. Using these results as a starting point, further analyses were conducted to study latency effects in the devices under EOS/ESD conditions. The procedures and results of these experiments will be described in the next chapter.

Chapter 5

Device Failure Analysis

In order to gain a better understanding of the reliability issues involved in CMOS integrated circuits, a series of measurements were performed on both commercially available integrated circuits and a set of custom designed and fabricated devices. The tests investigated the effects of electrical stress, thermal shock, exposure to ultraviolet light, and thermal annealing.

Statistical analyses of the results demonstrate the presence of latent failures in CMOS integrated circuits due to ESD. The cumulative effect of repeated discharges can be partially alleviated using thermal annealing or exposure to light. A charge injection model is proposed to interpret the results.

5.1 Introduction

The purpose of a protection structure is to increase the EOS/ESD immunity of a device without interfering with the normal operation of the circuit. A typical protection structure of an integrated circuit is shown in Figure 5.1. The shunt elements are used to divert current . y from the internal circuit. During normal operation, the shunt elements are in a high impedance state - they switch to a low impedance state when overstress condition occurs. The series element, usually a resistor, is used to limit the current allowed to flow towards protected device during ESD.

Since the shunt elements are active devices, they require certain time to switch from a high impedance state to low impedance state. The susceptibility of the internal

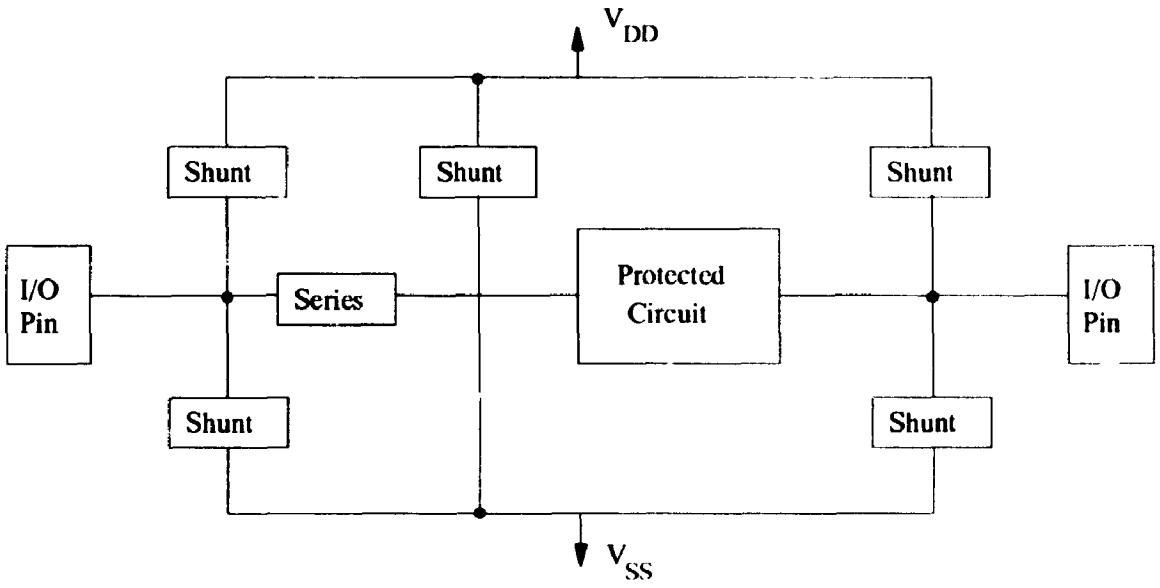


Figure 5.1 Typical Protection Structure of an Integrated Circuit

circuit depends on how quickly the shunt elements can be brought conduction. In addition, the efficiency and integrity of the shunt elements during and after ESD are also key factors affecting failures.

In reality, no integrated circuit can be entirely free of defects and imperfections; failure susceptible sites can originate at the micro defect level, such as interface defects or traps, and manifest their presence as macro defects, such as oxide shorts. In many cases, gate oxide shorts increase the quiescent power supply current, but may not affect the functionality of the device. These gate oxide shorts, created by either ESD/EOS or the fabrication process, that initially affect only the quiescent power supply current, can degrade with time and cause a permanent failure of the device. As devices are scaled down in size, physical effects such as charge trapping, hot carrier injection, the formation of interface states, and the oxide breakdown related to these types of time-dependent failures or latent failures become more significant.

The main objective of the experiments was to study the reliability of CMOS integrated circuits with emphasis on the protection circuits. The results of electrical measurements performed on integrated circuits and sub-components, before and after exposure to electrical stress, thermal shock, exposure to ultraviolet light, and thermal annealing, were used as the basis for the reliability studies. The main objective of the work was to use the experimental results for developing simple models that would clarify latency effects in semiconductor devices. It was found necessary to perform measurements at both the device and component levels to accurately isolate failure sites and analyze the nature of the faults.

5.2 Test Devices

Tests were performed on both commercially available and custom designed devices. Two different types of commercial CMOS devices; namely, 14069UB and 74HCU04, of the same manufacturer and date code, were used. They were chosen because of their structural simplicity; results obtained can contribute to the understanding of reliability issues in more complicated circuits.

5.2.1 CMOS B Series

The technology used in the B series is a 5 micron, single-polysilicon, single-metal, P-well, metal gate CMOS process. The schematic of the input protection circuit incorporated in the device is shown in Figure 5.2. The circuit consists of three diodes (D1, D2 and D3) formed by the implanted diffusion and well/substrate, and a parasitic well-to-substrate diode (D4). This ESD protection circuit limits the voltage appearing at the internal gate during the discharge by shunting the ESD current through

the breakdown of the diodes. The breakdown voltage is set at a level slightly higher than the normal operating voltage but lower than the breakdown level of the input gate. Typical electrical characteristics of this device are shown in Figure 5.4.

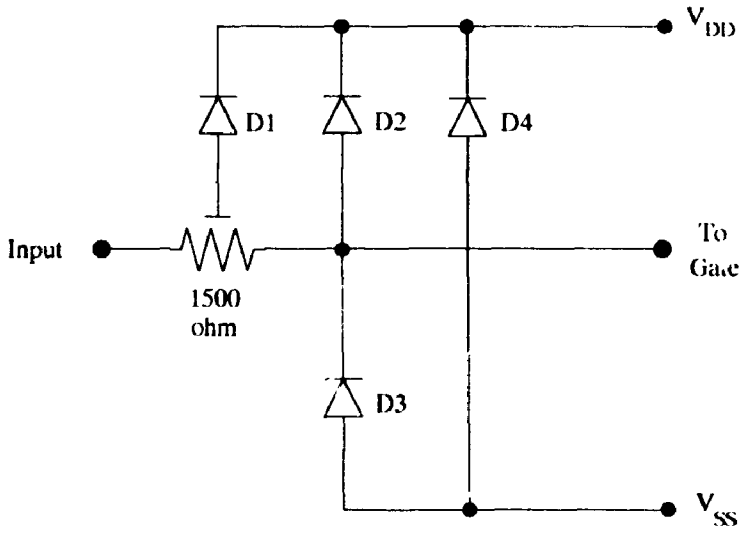


Figure 5.2 Input Protection Circuit of 14069UB

5.2.2 CMOS High-Speed Series

The technology used in the H series devices is a 3 micron, single-polysilicon, single-metal, P-well, polysilicon gate CMOS process. The circuit consists of two diffused diodes (D1 and D2) formed by the implanted diffusion and well/substrate, and a parasitic well-to-substrate diode (D3). The polysilicon resistor is designed to provide a current limiting function during a discharge. The equivalent circuit of this protection network is shown in Figure 5.3; its operation is similar to that used in the CMOS B series devices. Typical electrical characteristics of this device are shown in Figure 5.4.

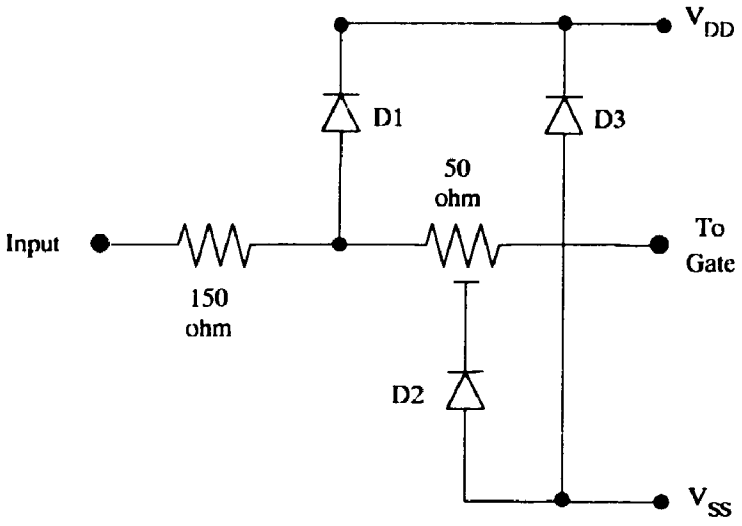


Figure 5.3 Input Protection Circuit of 74HCU04

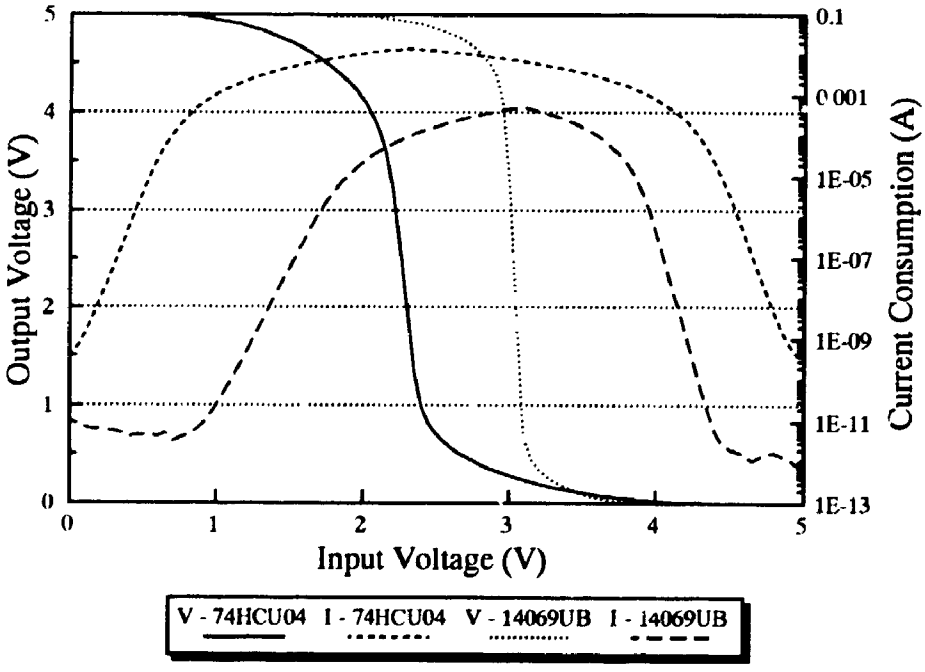


Figure 5.4 Typical Electrical Characteristics of Several Commercial Devices

5.2.3 Custom Fabricated CMOS Devices

The UWO test chips used in these experiments were fabricated using a 3-micron, single-polysilicon, double-metal, P-well, polysilicon gate CMOS process. In this project, a number of CCDs, protection circuits and MOS capacitors were analyzed and those suitable for the fabrication process were selected for implementing the design. The circuits were fabricated by the Northern Telecom Electronics silicon foundry in Ottawa. The detailed design procedures were discussed in Chapter 3; the following is a brief summary of the custom fabricated devices used in the investigation.

5.2.3.1 Charge-Coupled Devices (CCDs)

A CCD array is a microelectronic structure consisting of MOS capacitors in which charges are transferred from one capacitor to the next by an applied voltage pulse. As discussed in the previous chapters, any physical effects such as charge trapping, hot carrier injection, the formation of interface states, and oxide breakdown can seriously impair the operation of CCDs. Special MOS capacitors were designed and fabricated to study these effects in CCDs.

The cross-sectional views of the MOS capacitors used in these experiments are shown in Figure 5.5; both capacitors were enhancement (E)-type. Three different sizes, namely $30x30\mu m^2$, $60x60\mu m^2$ and $120x120\mu m^2$, were fabricated for both n and p-type capacitors. The corresponding capacitances for the n-type Si capacitors are 0.5pF, 2.5pF and 4.6pF respectively; for the p-type Si capacitors, the corresponding capacitances are 0.4pF, 2.0pF and 4.4pF respectively. These values were chosen

since they are typical of the capacitances found in commercial devices; a direct comparison of the results obtained for commercial and custom devices was thus possible. The C-V characteristics of a 120x120μm^2 MOS-C are shown in Figure 5.6.

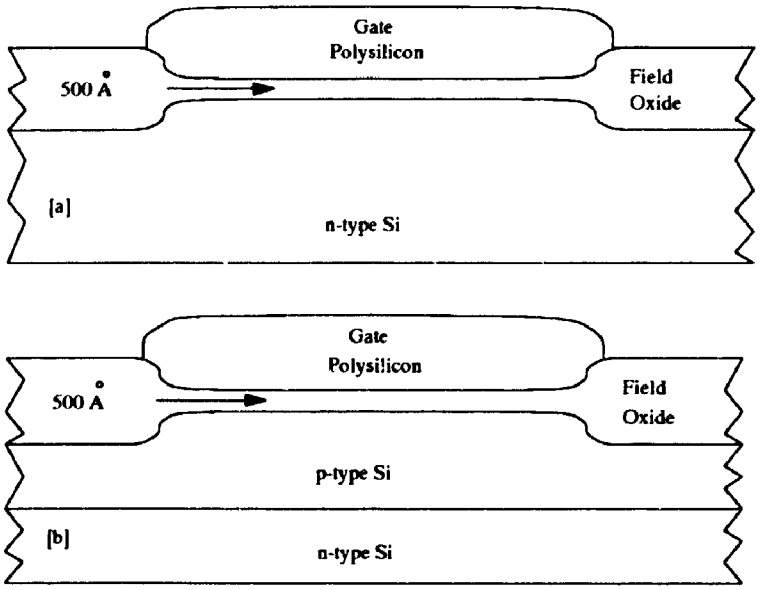


Figure 5.5 E-mode (a) n-Type and (b) p-Type Substrate MOS-C

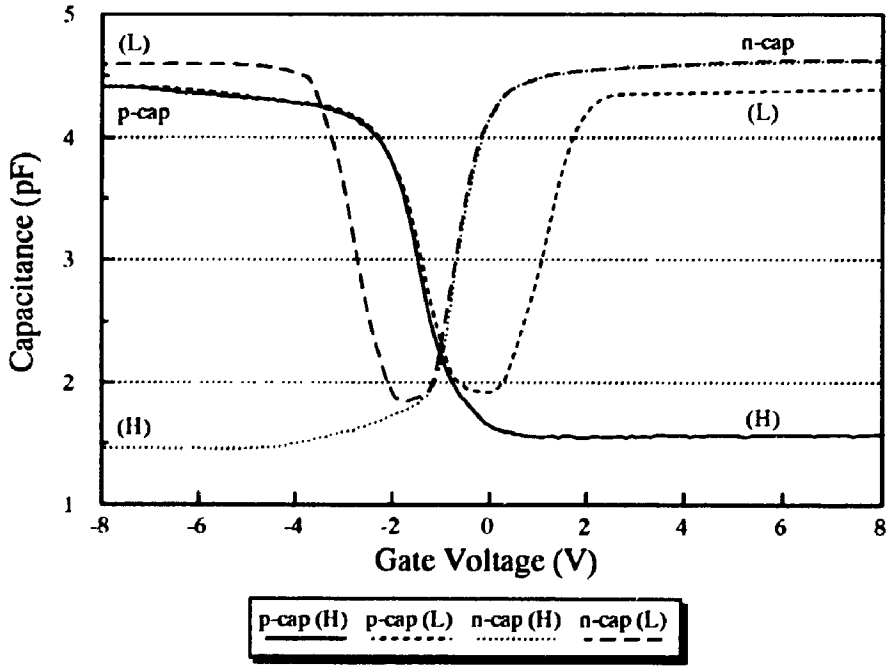


Figure 5.6 Typical C-V Characteristics of a 120x120μm^2 MOS-C

Experiments were performed to measure the gate oxide leakage current of both the n-type and p-type MOS-Cs. The purpose of these experiments was to investigate the leakage current at the onset of breakdown and the polarity effect on the breakdown threshold voltage for the MOS-C. The results are shown in Figure 5.7 and 5.8, respectively.

For n-type MOS-C, the breakdown voltages were approximately ± 55V. As shown in Figure 5.7, the current at the onset of breakdown was more gradual for negative voltage stress. This suggests that n-type MOS-C are more easily damaged by positive voltage stress than by negative during EOS/ESD.

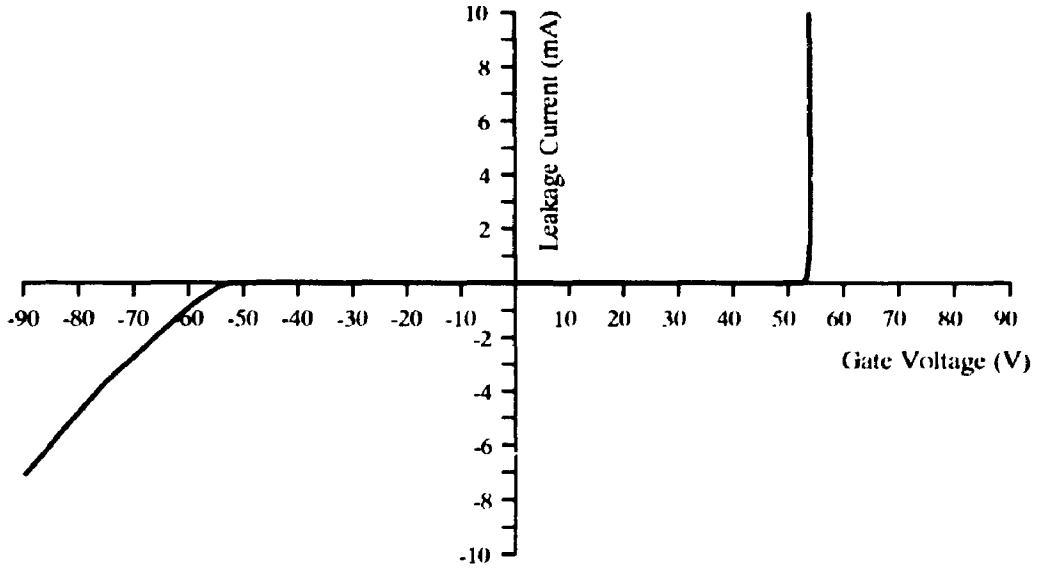


Figure 5.7 Typical Leakage Current for n-Type Si MOS-C

The results for the p-type MOS-C also demonstrated that the leakage current was more gradual with positive voltage stress. This indicates that p-type MOS-C are more easily damaged by negative voltage stress than by positive voltage stress. The breakdown voltages were approximately ± 55V.

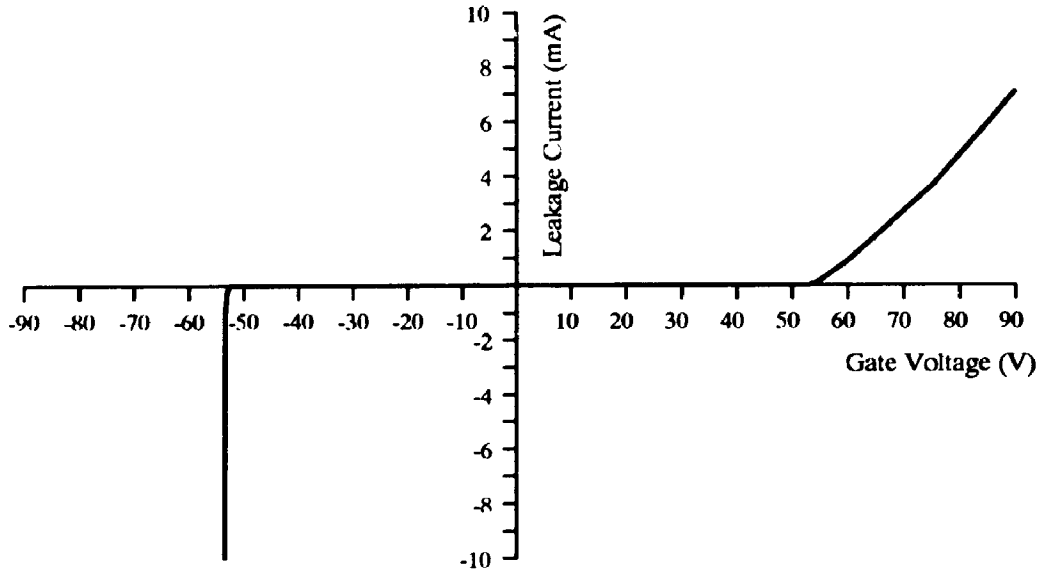


Figure 5.8 Typical Leakage Current for p-Type Si MOS-C

5.2.3.2 Protection Circuits

Two main inverter circuits, with protection networks, were designed, fabricated and packaged in ceramic packages. Circuits diagrams of the test circuits are shown in Figure 5.9 and 5.10. The circuits were designed in a modular fashion; the protection network and the transistor cell could be connected for global tests and disassembled for local tests on each module. This allowed measurements to be made on each diode/resistor and both the p-transistor and n-transistor. The gate areas for the nMOS and pMOS transistors used in the circuits were $6x6\mu m^2$ and $6x12\mu m^2$ respectively. The corresponding capacitances for these gate structures were approximately 0.002pF and 0.004pF; the breakdown voltages of the protection circuits 5.7V and -0.7V.

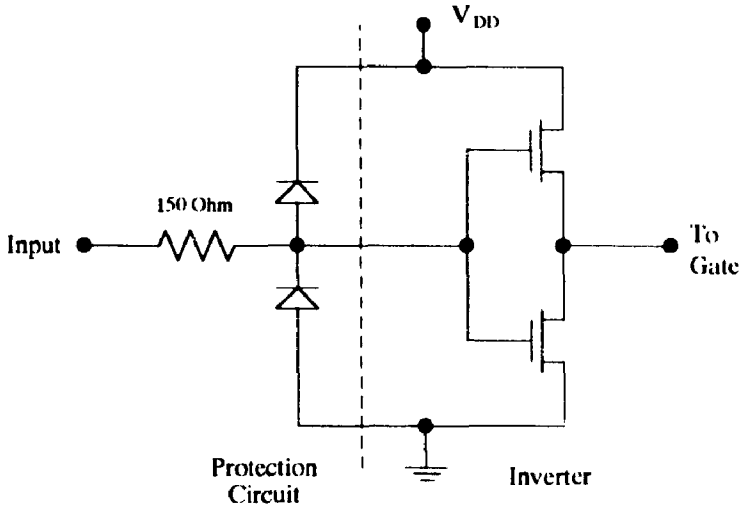


Figure 5.9 Equivalent Circuit of Custom Protection Circuit #1

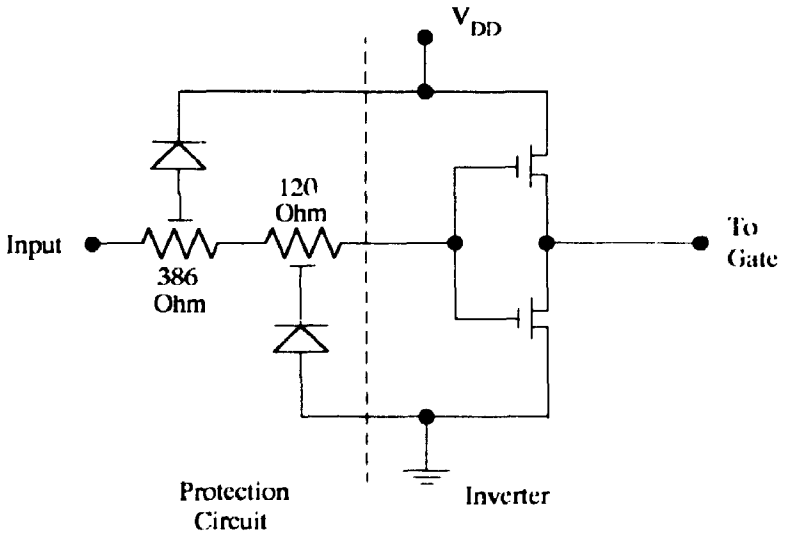


Figure 5.10 Equivalent Circuit of Custom Protection Circuit #2

The purpose of these tests chips was to examine their static and dynamic responses under various ESD conditions, and to allow a direct comparison with

commercial devices. The custom circuits were designed to allow local measurements to be made on individual components; the objective was to further analyze and explain the results of the measurements performed at the device level.

5.3 Failure Criterion

The failure criterion used throughout the testing of the commercial devices and the UWO test chips was defined as the condition where the quiescent current (I_{DDQ}) of the device exceeded the maximum current consumption specified by the manufacturer for a normal device. The current based measurement technique was chosen because of its efficiency in detecting non-stuck-at faults found in CMOS integrated circuits [69-70]. The nature of defects was determined by capacitance-voltage (C-V) measurements. The relationship between the trap location, density, energy and ESD voltage was studied using C-V techniques [76].

5.4 Experimental Setup and Procedure

The block diagram of the experimental setup used in the tests is shown in Figure 5.11. During the experiments, the pin-under-test was monitored for related damage by examining the I-V and C-V characteristics using a Hewlett-Packard 4145A Semiconductor Parameter Analyzer and a Hewlett-Packard 4280A C-V Analyzer, respectively. The temperature of the device-under-test was controlled between -55°C to 130°C using a Temptronic hot chuck. The HBM ESD stress was applied to the device using a KeyTek series 2000 ESD test system. The pin-under-test for the commercial devices was pin no. 1; the circuit input pin was stressed for the custom devices.

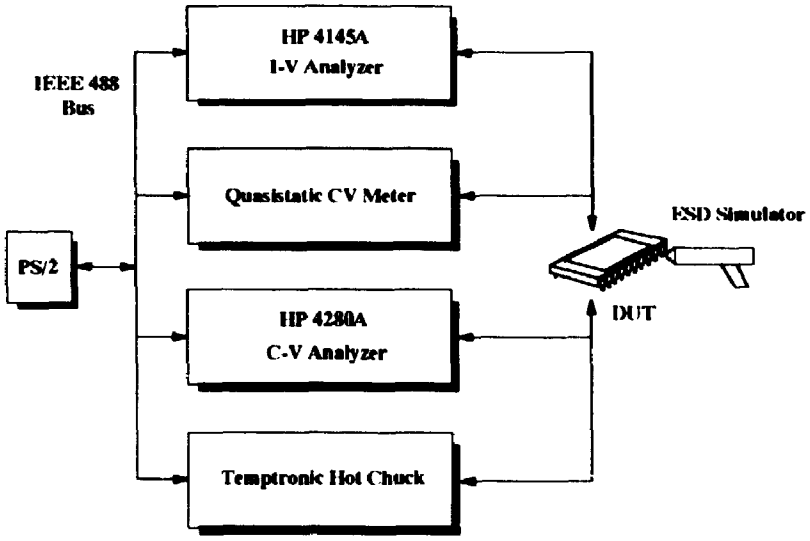


Figure 5.11 Block Diagram for the Experimental Setup

5.4.1 Electrical Stress Test

The schematic diagram of the test equipment used for all electrical stress tests is shown in Figure 5.12. The human-body current injection test method was used for both polarities of discharge. In this test procedure, the probe tip of the simulator is placed directly in contact with the pin of the device-under-test and the discharge energy is applied by closing the mercury relay. The current injection test method was chosen since it gives more repeatable results than the air discharge test method, in which the charged simulator tip is brought to the proximity of the device and an actual air discharge occurs. The current injection method was described in the second issue of IEC 802-2 [62]; it should be noted that the R-C values used in the simulator [R = 150 ohms, C = 150 pF] are different compared to the R-C network [R = 1500 ohms, C = 100 pF] used in conventional human body air discharge simulators [63].

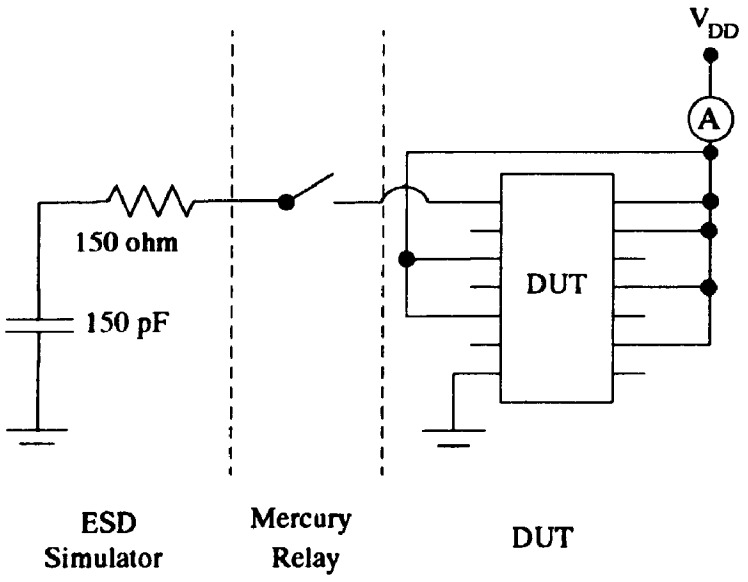


Figure 5.12 Test Circuit for Measuring the Electrical Characteristics of a Device

5.4.1.1 New Devices

Three types of tests, using both positive and negative current discharge, were performed on each new sample lot. The sample size for each test was 10.

5.4.1.1.1 Threshold Test

The purpose of this test was to determine the voltage level (V_1) at which a single pulse caused failure. The pin-under-test was subjected to a single pulse starting at 1kV and the test was repeated with new samples until failure occurred after a single pulse.

5.4.1.1.2 Step-Stress Test

The purpose of this test was to investigate whether the failure threshold voltage depended on the test voltage previously applied. The pin-under-test was step-stressed starting at 500 volts and the voltage was increased in equal increments of 100 volts until failure occurred.

5.4.1.1.3 Constant Amplitude Multiple Stress Test

This test was performed on each device type to determine the typical voltage level at which approximately ten pulses were required to produce a significant shift in the electrical characteristics.

5.4.1.2 Pre-stressed Devices

Tests were performed to investigate the latency effects on a preconditioned device. Sample lots, which had been subjected to a single stress of 0.5 and $0.75V_t$, were prepared for this experiment.

5.4.1.2.1 Threshold Test

The pin-under-test was subjected to a single pulse starting at 1 kV and the test was repeated with new samples until failure occurred for a single pulse.

5.4.1.2.2 Step-Stress Test

The pin-under-test was step-stressed starting at 500 volts and the voltage was increased in equal increments of 100 volts until failure occurred.

5.4.2 Thermal Shock Test

The purpose of this experiment was to investigate the effect of thermal shock and determine if a correlation exists between the characteristics of devices measured after thermal stress, and electrical stress due to ESD. The importance of this work was to determine if the results of an accelerated thermal shock test could be used to predict latent failures in integrated circuits. For the hot thermal shock test, the room temperature devices were placed four times into an oven heated to 250°C. Each thermal shock cycle consisted of a 15-minute heat exposure interval followed by a 5-minute rest period at room temperature. For the cold thermal shock test, the devices were placed in liquid nitrogen (-160°C) for 15 minutes and were cyclically shocked, 10 times. The interval between each shock was approximately 5 minutes.

5.4.3 Ultraviolet Light Test

The purpose of this test was to determine if the damage caused by electrical stress could be alleviated by ultraviolet light. The de-lidded devices were placed in a commercial EPROM eraser with short wavelength uv (254nm, 4.9eV) for one hour. The calculated intensity of the light source was 0.025 W cm^{-2} and the calculated absorption coefficient was $2x10^{6}$ cm^{-1}.

5.4.4 Thermal Annealing Test

The purpose of this test was to determine if the damage caused by electrical stress could be reversed by a thermal annealing process. The temperature of the device-under-test was slowly increased from room temperature (25°C) to 100°C and maintained for 10 minutes. The rate of increase, controlled by a Temptronic Hot

Chuck, was 2°C per minute.

5.5 Results

The experiments were performed on two groups of devices : commercial ones and custom made.

5.5.1 Commercial Devices

5.5.1.1 Electrical Stress Test

The experimental results of the tests are summarized in Table 5.1. The sample size for each test was 10. The values shown in Table 5.1 are the mean and the standard deviation [in brackets] of the failure voltage for each sample lot. During the experiments, power to the device-under-test had to be switched off after each stress to prevent latch-up.

Table 5.1 ESD Performance of Test Devices

Failure Voltage	14069UBCL		74HCU04	
Polarity	(+)kV	(-)kV	(+)kV	(-)kV
New				
1 Pulse (V_1)	2.02[0.08]	-3.67[0.09]	2.29[0.11]	-2.05[0.10]
Step Stress (V_4)	1.64[0.12]	-2.86[0.14]	1.97[0.11]	-1.68[0.14]
10 Pulses	1.59[0.07]	-2.84[0.10]	1.09[0.10]	-1.09[0.10]
Pre-Stressed				
0.5V_1				
1 Pulse (V_3)	2.20[0.14]	-3.73[0.10]	2.46[0.14]	-2.14[0.14]
Step Stress (V_4)	1.74[0.09]	-3.01[0.08]	2.12[0.12]	-1.77[0.07]
0.75V_1				
1 Pulse (V_5)	1.84[0.09]	-3.43[0.14]	2.06[0.11]	-1.80[0.17]
Step Stress (V_6)	1.56[0.06]	-2.59[0.16]	1.70[0.10]	-1.60[0.12]

5.5.1.1.1 New Devices

5.5.1.1.1.1 Threshold Test

The threshold voltages for the 14069UB were 2.02kV and -3.67kV while the failure voltages of the 74HCU04 were 2.29kV and -2.05kV. The difference in the amplitude of the failure voltage was believed to have been mainly due to the configuration of the protection circuits and partially due to the polarity of the test voltage.

5.5.1.1.1.2 Step-Stress Test

As shown in Table 5.1, the step stress failure voltages for the 14069UB and 74HUC04 were 1.64kV, -2.86kV and 1.97kV, -1.68kV, respectively.

5.5.1.1.1.3 Constant Amplitude Multiple Stress

The results are given in Table 5.1 for all the test devices. The failure voltages for the 14069UB were 1.59kV and -2.84kV for 10 pulses while the levels were 1.09kV and -1.09kV for the 74HCU04. Together with the results from the step-stress test, all the failure voltages were lower than those measured for a single pulse ESD; the results suggest that the repetitive application of relatively low voltage ESD pulses weakens the devices.

5.5.1.1.2 Pre-Stressed Devices

5.5.1.1.2.1 Threshold Test

The results of the tests in which an initial single high voltage pulse (0.5 and $0.75V_t$) preceded a second pulse are shown in Table 5.1. In general, if the preconditioning voltage is 0.5 of the single pulse threshold voltage, the device is hardened and the failure voltages for a single pulse increase. However, if the preconditioning voltage is higher, such as $0.75V_t$, the device will be weakened and the failure voltages decrease.

5.5.1.1.2.2 Step-Stress Test

The results were similar to those obtained in the threshold test. Preconditioning with a test voltage of $0.5V_t$ tended to harden the devices while, on average, a higher voltage ($0.75V_t$) decreased the failure voltage.

5.5.1.2 Thermal Shock Test

In the hot thermal shock test, both the voltage and current transfer characteristics increase after the first cycle. After subsequent exposure to thermal shock some devices fail. On the other hand, after the cold thermal shock test, only the current transfer characteristics increased.

5.5.1.3 Ultraviolet Light Test

Experiments have been performed to investigate the effect of ultraviolet light on normal devices. No significant shift in the electrical characteristics of the device-under-test was observed. Therefore, it was concluded that the device's interaction with ultraviolet light should not induce any degradation , such as charge trapping, to the device-under-test. For stressed devices, ultraviolet light exposure resulted in a decrease in the quiescent current; however, the current did not return to the previous (prestress) level.

5.5.1.4 Thermal Annealing Test

Experiments have been performed to investigate the effect of thermal annealing on normal devices. No shift in the electrical characteristics of the device-under-test was observed. Therefore, it was concluded that the thermal annealing process should not induce any degradation, such as an quiescent current increase in the device-under-test. Similar to the ultraviolet light annealing process, thermal annealing yielded a quiescent current decrease; again, the current did not return to the previous (prestress) level.

5.5.2 UWO Test Chips

Custom made devices exhibited similar increases in I_{DDQ} after electrical/thermal stress tests as the commercial ones. This was expected since the protection circuits employed in the commercial and the custom designed device's were similar. However, local measurements were conducted on the protection circuits and the transistor cells to explain the results obtained from the measurements made on the complete device.

5.5.2.1 Electrical Stress Test

5.5.2.1.1 Protection Circuits

After electrical stress, the circuit was disassembled and a set of tests was conducted on the protection network circuit and the transistor cell separately. Typical electrical characteristics, after a low level (<1kV) ESD, are shown in Figure 5.13. The circuit was disassembled and measurements were made on individual elements to identify the failure site. The I-V characteristics of the transistor cell inside the protection circuit were found to be normal while the leakage current of the protection diodes, shown in Figure 5.14, had increased. It can be concluded that, for low level ESD, the increased leakage current is due to the protection network circuit; the diodes were the site of damage.

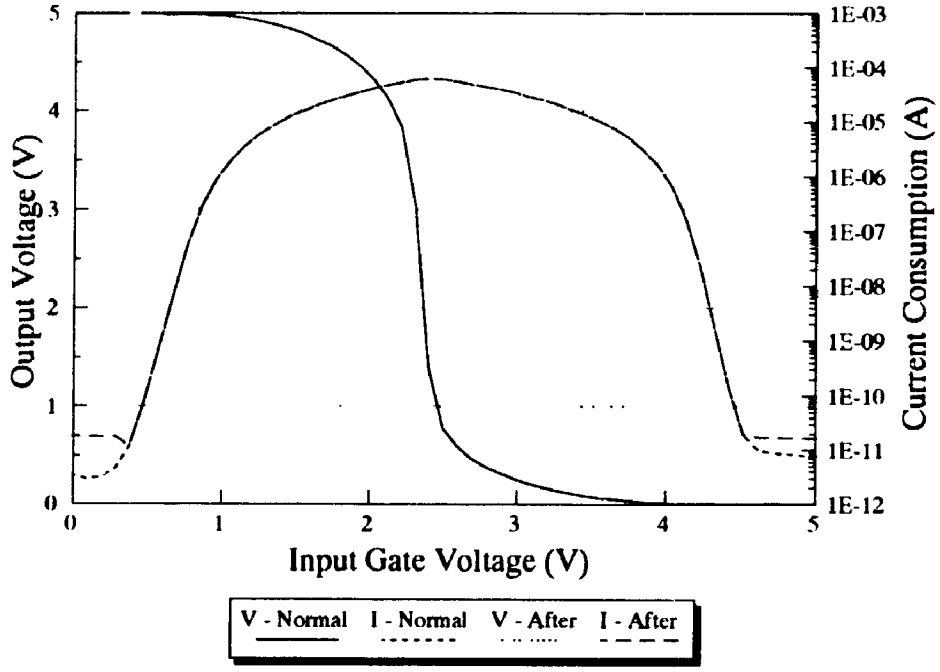


Figure 5.13 Typical I-V Characteristics of a Custom Device Before and After Low Level ESD

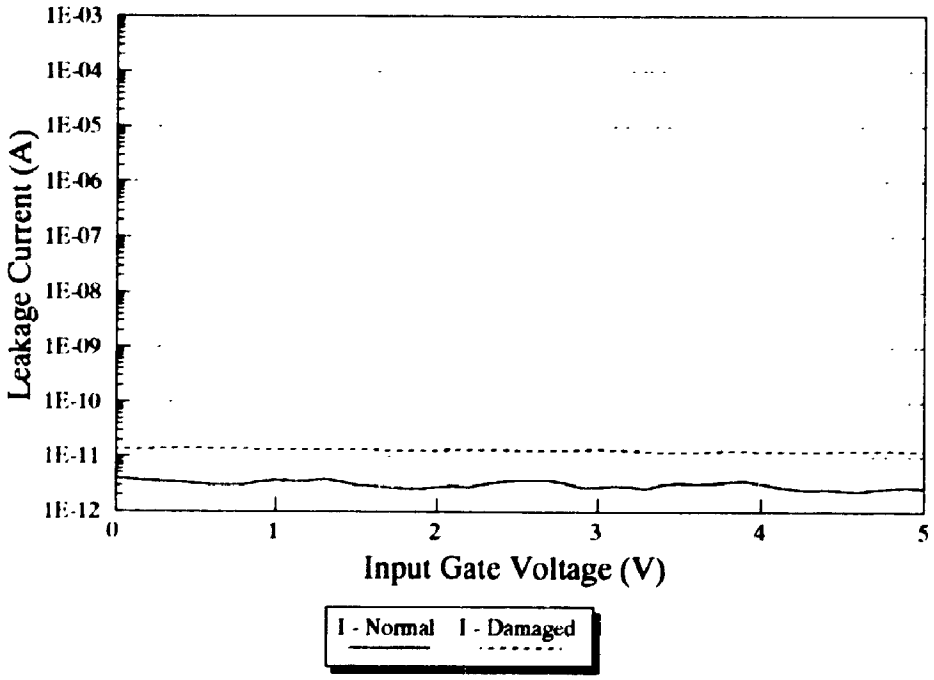


Figure 5.14 Comparison of Leakage Current in Protection Diode Before and After ESD

Similar experiments were performed on the protection circuits using a higher level (>1kV) ESD. Typical I-V characteristics are shown in Figure 5.15. Local measurements were conducted on the protection networks and the transistor cells; results are shown in Figure 5.16 and 5.17. It can be noted that, for high level (>1kV) ESD, the increased leakage current was caused by both the protection network circuit and the transistor cell; the leakage current through the protection network always predominated. Specific tests were performed on the p-channel and n-channel transistors. For low level ESD, only an increase in leakage current was observed; at higher levels of stress, both an increase in the leakage current and a shift in the threshold voltage were measured.

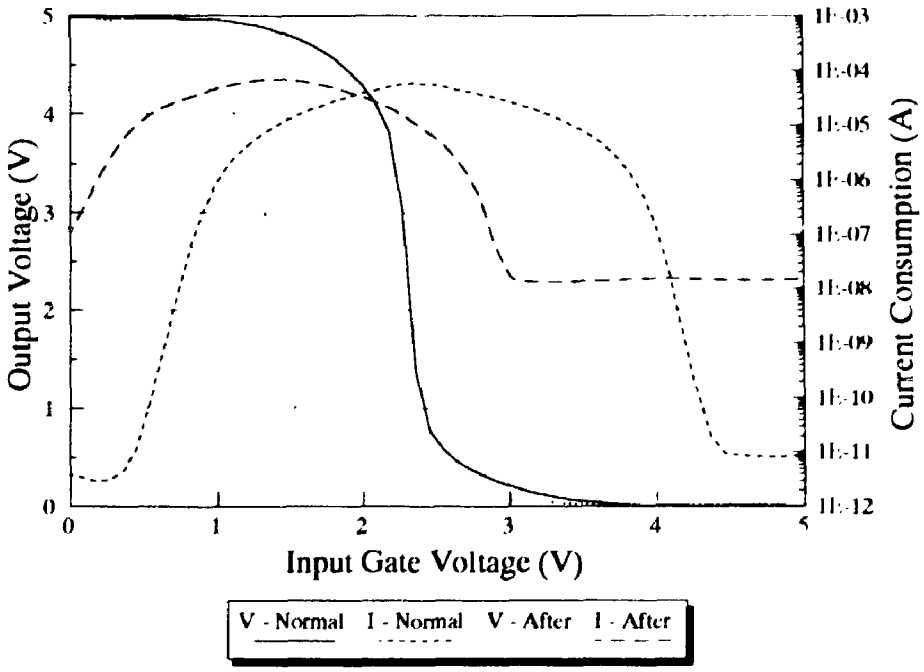


Figure 5.15 Typical I-V Characteristics of a Protected Circuit Before and After Higher Level ESD

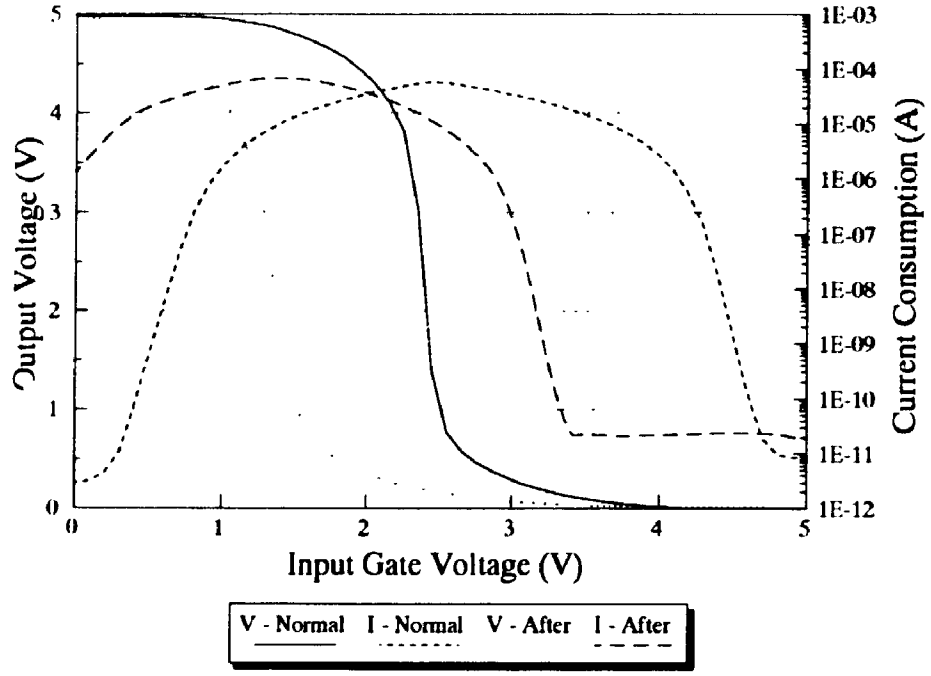


Figure 5.16 Typical I-V Characteristics of Transistor Cell Before and After ESD

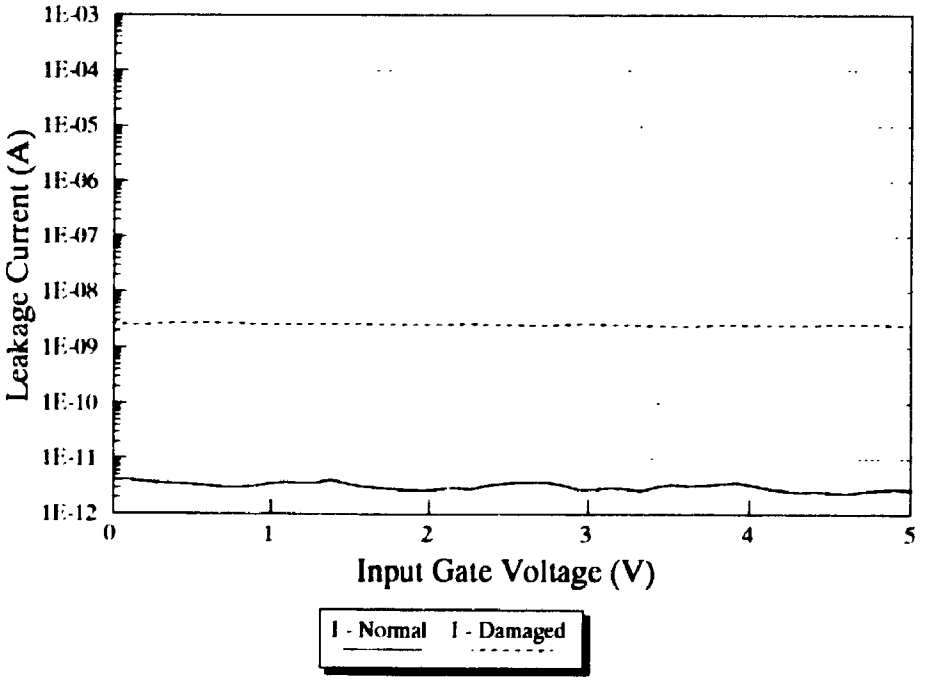


Figure 5.17 Comparison of Leakage Current in Protection Diode Before and After ESD

5.5.2.1.2 MOS-C/CCDs

Experiments were performed to study low level ESD effects on MOS-C and CCDs. Typical high and low frequency C-V curves for the n-type and p-type silicon charge transfer cells (MOS-C) in CCDs are shown in Figure 5.18 and 5.19, 5.20 and 5.21, respectively. For n-type substrate capacitors, a positive voltage stress resulted in a lateral shift in the positive direction, while a negative voltage stress produced no significant lateral shift. In both cases, there was a slight distortion in the C-V curves. This indicates that n-type capacitors are more easily damaged by positive voltage, compared to negative voltage stresses. It appeared that negative charges were injected and trapped in the gate oxide during the positive voltage stress, but a negligible amount of positive charge was injected into the gate oxide during the negative voltage stress.

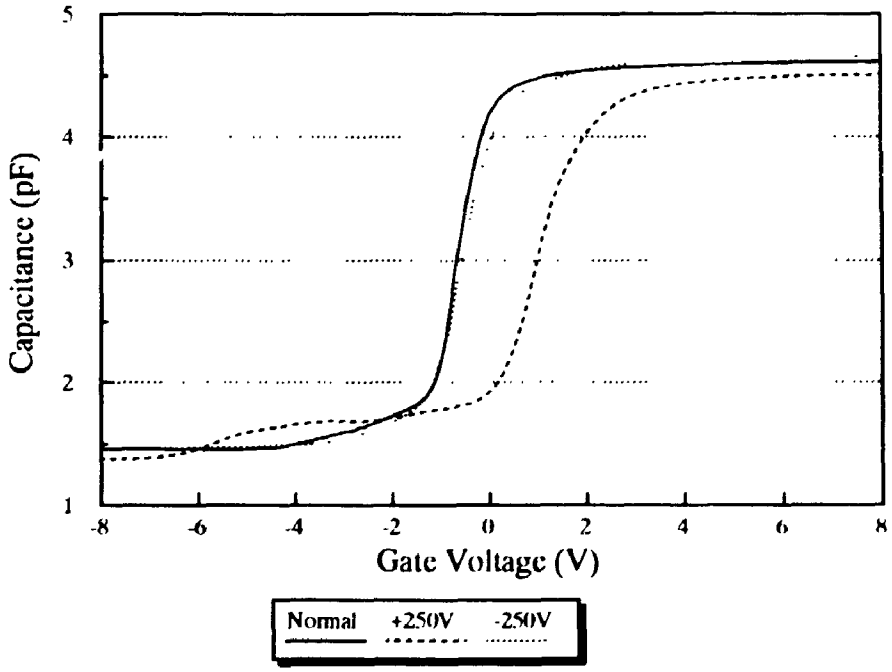


Figure 5.18 High Frequency C-V Curves of a n-Type MOS-C after ±250V ESD

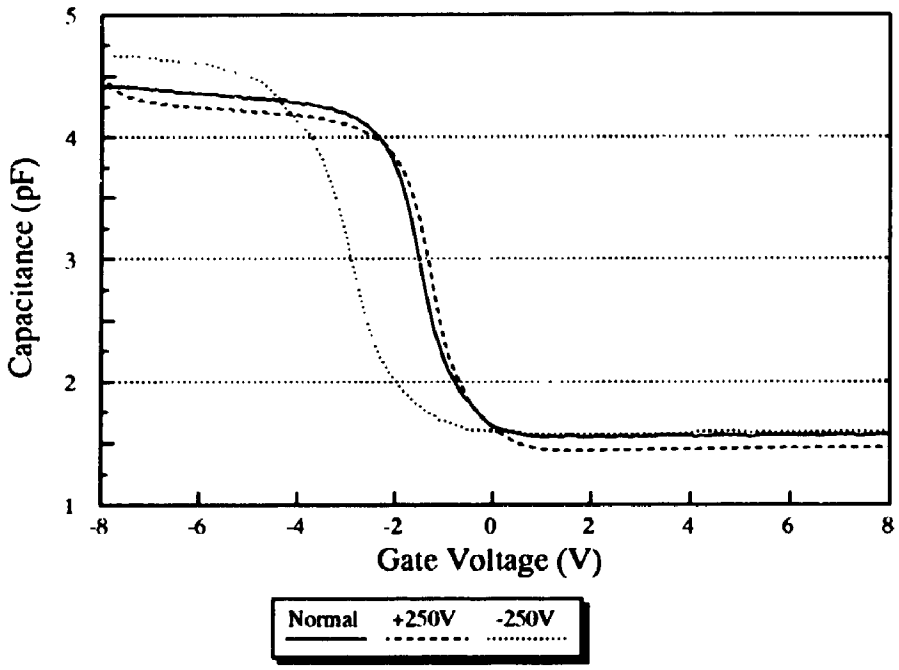


Figure 5.19 High Frequency C-V Curves of a p-Type MOS-C after ±250V ESD

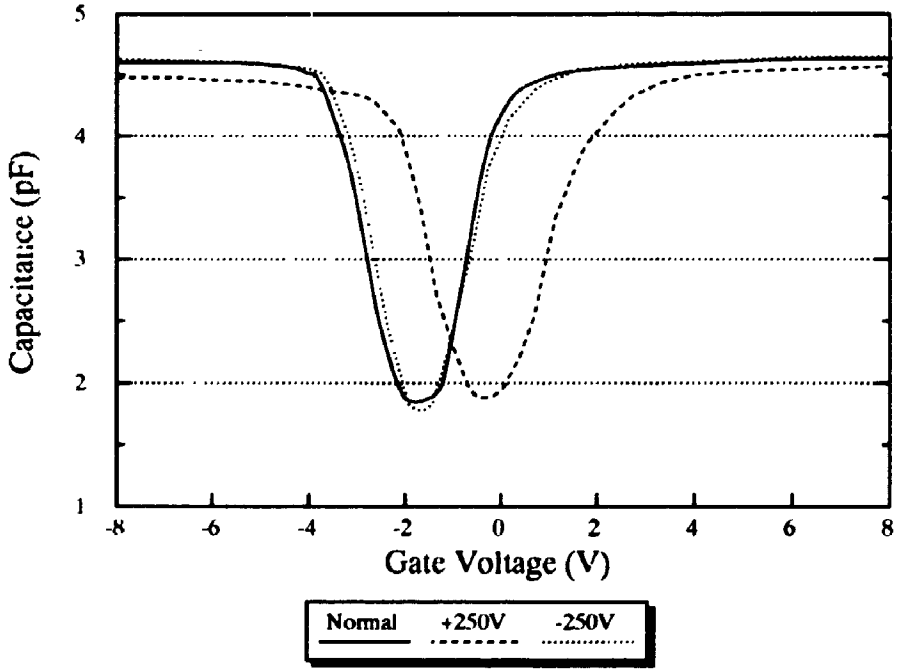


Figure 5.20 Low Frequency C-V Curves of a n-Type MOS-C after ±250V ESD

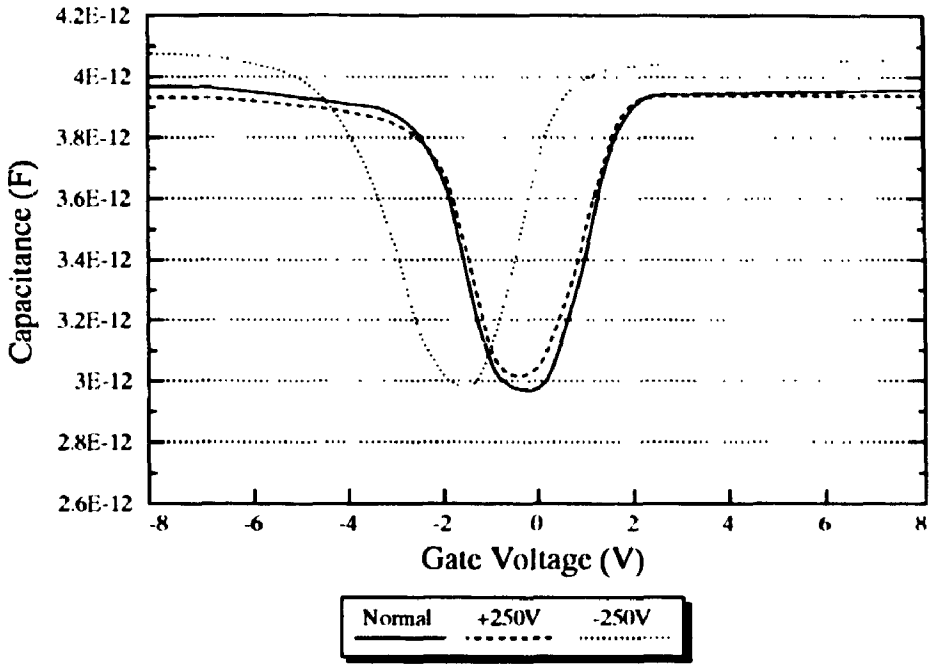


Figure 5.21 Low Frequency C-V Curves of a p-Type MOS-C after ±250V ESD

Using the data from the high and low C-V curves (Figures 4.18 to 4.21), the amount of oxide trapped charge, the interface trap capacitance and the interface trap density induced by the ESD can be calculated using the methods shown in Appendix B. The oxide trapped charges can be measured from the voltage parallel shift in the C-V curve. As charge is introduced into the oxide, the charge balance in that region will be upset. This effectively alters the capacitance for any gate bias, except for strong accumulation and strong inversion regions where the capacitance equals C_{ox} or becomes saturated. The amount of trapped charge can be calculated from the voltage shift in the C-V curve at flatband voltage, using equation (B.11) shown in Appendix B.

$$Q_{trap} = \Delta V_{FB} x C_{FB} \qquad \ldots(5.1)$$

where :

Q_{Trap} = oxide trapped charge

ΔV_{FB} = lateral shift in flatband voltage

C_{FB} = flatband capacitance

For the n-type MOS-C, the flatband capacitance and voltage obtained from the C-V curves were 3pF and -0.5V, respectively. The voltage shift at flatband voltage due to the positive ESD was 1.5V. Using equation (5.1), the amount of negative charge injected in the gate oxide by the positive ESD was 4.5×10^{-12}C. For negative ESD, the amount of charge injected in the gate oxide is negligible.

Similarly, the flatband capacitance and voltage for the p-type MOS-C were 3.5pF and -1.9V, respectively. The voltage shift at flatband voltage due to the negative ESD was -1.4V. The amount of positive charge injected in the gate oxide was 4.9×10^{-12}C. For positive ESD, the amount of charge injected in the gate oxide is negligible.

To calculate the interface trap density, one assumes that the interface traps usually do not respond to small, high frequency ac signals but responds to a slow dc bias; thus, these traps only affect the device capacitance at high frequency. Using the method shown in Appendix B, the interface capacitance can be calculated by subtracting the high frequency C-V curve from the low frequency C-V curve during depletion. The interface trap density can then be obtained by dividing interface capacitance by the gate area and electron charge.

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \quad \ldots(5.2)$$

$$D_{it} = \frac{C_{it}}{Aq} \quad \ldots(5.3)$$

where :

C_{it} = interface trap capacitance
C_{LF} = low frequency capacitance
C_{LF} = high frequency capacitance
C_{ox} = oxide capacitance
D_{it} = interface trap density
A = gate area
q = magnitude of electron charge

A computer program was developed to perform the CV analysis. The user manual and the options available in the program are discussed in Appendix B. An important piece of information obtained from CV analysis is the interface trap density versus trap energy curve. It shows the location and the energy of the interface traps in the bandgap region. As illustrated in Figure 5.22, interface traps are concentrated on the edges of conduction and valence bands. Moreover, the interface trap density was increased after ESD. Similar results were also obtained using p-type MOS-C samples.

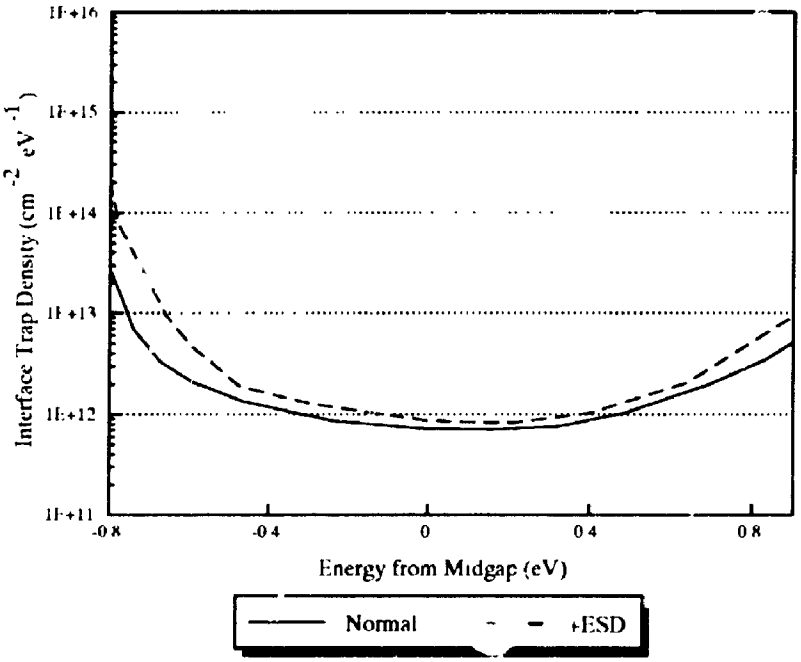


Figure 5.22 Interface Trap Density versus Trap Energy of a n-Type MOS-C Before and After +250V ESD

5.5.2.2 Thermal Shock Test

5.5.2.2.1 Protection Circuits

Tests which were performed on disassembled circuits after exposure to thermal stress showed that the increase in the leakage current was not distributed consistently in the two conducting paths. The changes were randomly distributed due to the protection network and the transistor cells. Voltage thresholds, in most cases, were not affected.

5.5.2.2.2 MOS-C/CCDs

The thermal shock test used in the experiments produced an increase in the leakage current through the MOS-C. Due to differing coefficients of thermal expansion of the materials used, the observed degradation is believed to be due to stress induced damage at interfaces.

5.5.2.3 Ultraviolet Light/Thermal Annealing Test

The purpose of this experiment was to investigate whether the damage is caused by trapped charges (temporary damage) or by the growth of conducting filaments between layers (permanent damage). If the damage were caused by trapped charges in the oxide, optical/thermal annealing processes should be able to detrap some of the charge and restore the normal electrical characteristics of the device. However, if the damage were permanent, such as caused by the formation of the conducting filaments between layers, optical/thermal annealing would not have a significant effect on the electrical characteristics of the device.

5.5.2.3.1 Protection Circuits

Characteristics of an electrically stressed (-1.5kV ESD) custom device, after optical/thermal annealing processes were investigated. After electrical stress, the circuit was disassembled and separate tests were conducted on the protection network circuit and the transistor cell. From the electrical stress test, one noticed that, for high level (>1kV) ESD, the increased leakage current was caused by both the protection network circuit and the transistor cell; the leakage current through the protection network always predominated. In addition, a shift in the threshold voltage

was observed in the transistor cell.

The results of the optical/thermal annealing process for the transistor cell and the protection network circuit are shown in Figure 5.23 and 5.24, respectively. As shown in Figure 5.23, the electrical characteristics of the transistor cell have returned to normal after the process. This means that the damage in the transistor cell is mainly caused by charge trapping in the gate oxide; recovery is possible if enough thermal energy is provided to excite the trapped charges and release them from the trapping sites. It is believed that the remaining shift in the characteristics is due to damage to the parasitic diodes associated with the edges of the gate electrodes, where an enhanced electric field exists.

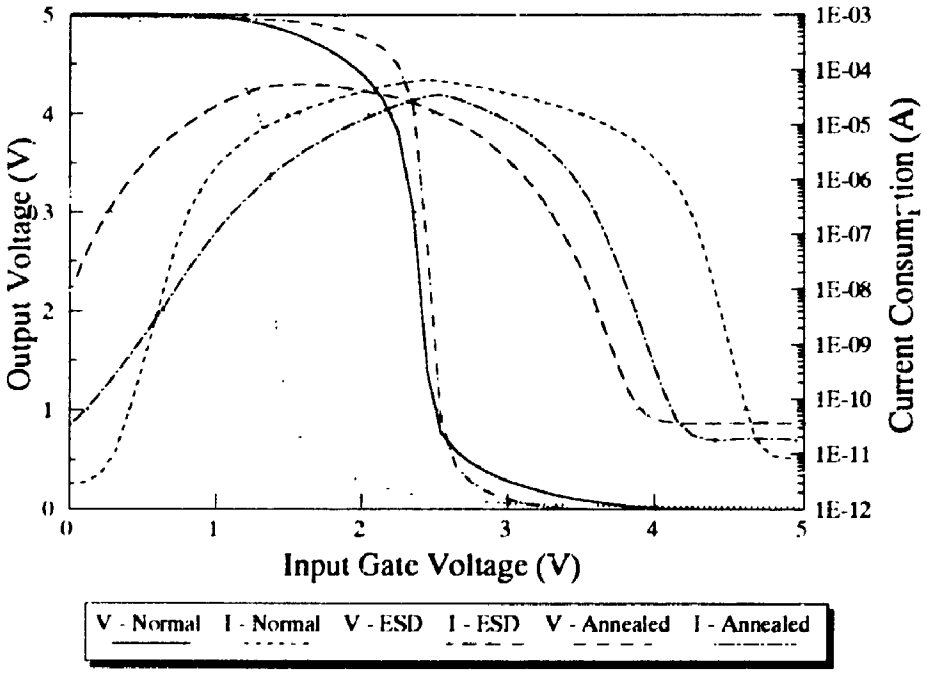


Figure 5.23 Typical I-V Characteristics of an Annealed Transistor Cell

The damage to the protection network circuit is probably caused by the growth of conducting filaments across the junction as the junction is turned on to shunt the high amplitude current during ESD. As shown in Figure 5.24, the damage is irreversible; the optical/thermal annealing processes do not have a significant effect.

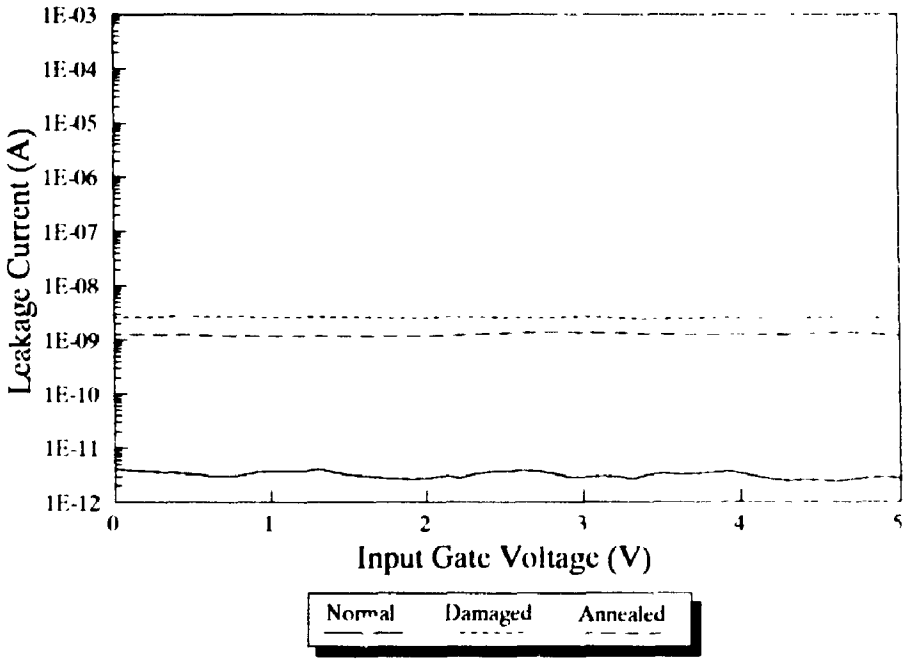


Figure 5.24 Typical I-V Characteristics of an Annealed Protection Network Circuit

5.5.2.3.2 MOS-C/CCDs

Similar results (Figure 5.25 and 5.26) were observed in the n-type MOS-C/CCDs. The damage during ESD in the MOS-C/CCDs cell is mainly caused by charge trapping in the gate oxide; partial recovery can be effected by providing enough optical/thermal energy to excite the trapped charges and release them from the trapping sites.

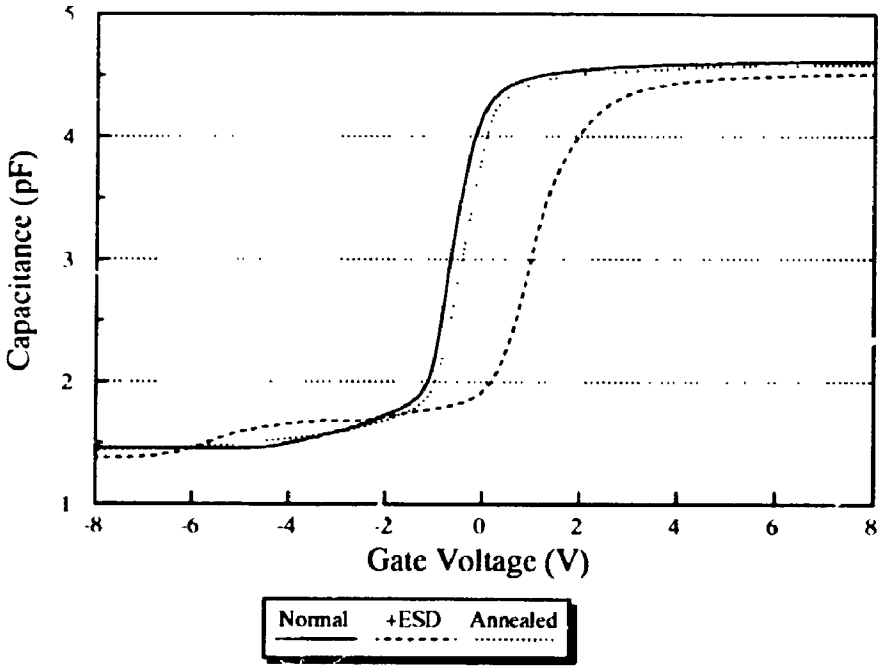


Figure 5.25 Typical High Frequency C-V Characteristics of a n-Type MOS-C After Annealing Process

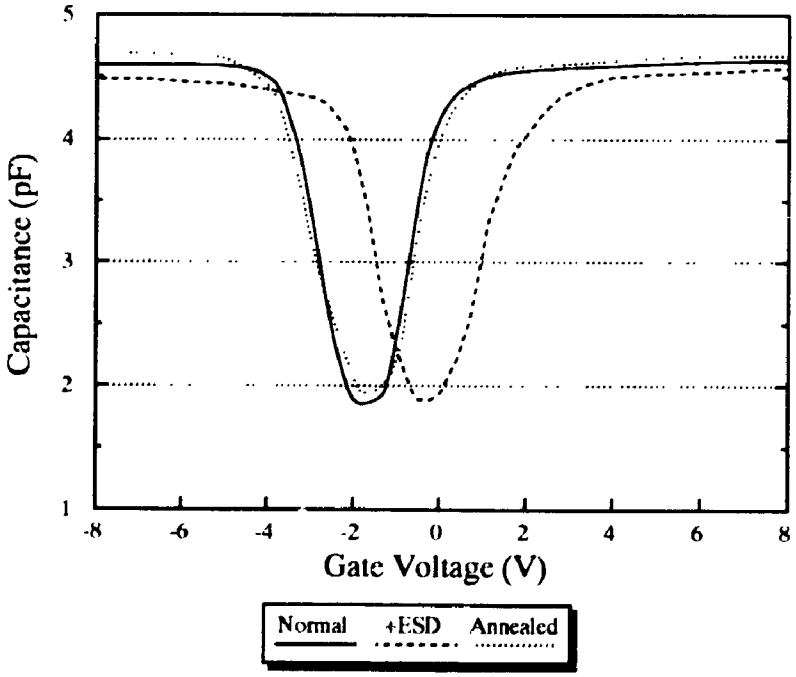


Figure 5.26 Typical Low Frequency C-V Characteristics of a n-Type MOS-C After Annealing Process

5.6 Charge Injection Model

Experimental work has shown that low level ESD causes damage in the reverse biased diodes in the input protection networks. High level ESD produces damage in both the protection diodes and the transistor cells. Measurements made on the individual transistors showed that there was a shift in the threshold voltages. A charge injection model is proposed to explain these results that serves as a basis for explaining device latent failure mode due to ESD.

The experiments have shown that the transistor cell, for increasing ESD stress, first showed an increase in leakage current, followed by a shift in the threshold voltage, as the leakage current increased further. A conceivable fault mechanism can be proposed that the initial increase in the leakage current is due to damage to the parasitic diodes associated with the edges of the gate electrode, where an enhanced electric field exists during the stress events. At higher stress levels, charge is injected through the gate and becomes trapped; a further increase in the leakage current and a shift in the threshold voltage results. The total leakage current is now caused by leakage through the parasitic diodes, and an effective reduction in channel length, due to the trapped charge.

Chapter 6

Conclusions and Recommendations

6.1 Summary and Conclusions

Integrated circuits cannot be entirely free of defects and imperfections. Failure susceptible sites can originate at the micro defect level as interface defects or traps, and lead to macro defects, such as oxide shorts. Often gate oxide shorts increase the quiescent power supply current, but may not affect the functionality of the device. These gate oxide shorts, created by either ESD/EOS or the fabrication processes, initially affect only the quiescent power current, but can degrade with time and cause a permanent failure in the device. The macro defects introduced by device manufacturing processes are easier to detect and can be eliminated by adjusting parameters during IC fabrication. Micro defects are more difficult to control, since the generation processes can depend on several parameters including time, temperature, and the stress voltage applied to the device. As devices are scaled down in size, physical effects such as charge trapping, hot carrier injection, the formation of interface states, and oxide breakdown related to these types of time-dependent failures or latent failures become more significant.

A series of tests, investigating the effects of electrical stress, thermal shock, exposure to ultraviolet light, and thermal annealing has been conducted on both commercially available and custom designed devices. Several different investigation techniques, namely I-V, C-V, thermal and optical methods, were used in this research to study the fundamental properties of latency effects in CMOS CCDs. It has been found

that the detection of latent failures at the device level is difficult to interpret, since the exact fault site is hard to locate. Although quiescent power supply current measurement is an acceptable global test method, custom designed integrated circuits comprised of independent modules were necessary to yield the fault site information.

In this study, a variety of charged coupled devices and protection network circuits were designed and fabricated using a 3-micron single polysilicon, double metal p-well Complementary Metal Oxide Semiconductor (CMOS) technology. This process is used by Northern Telecom Electronics (Ottawa, Ontario) and is available to Canadian university researchers through the Canadian Microelectronics Corporation (Kingston, Ontario). Measurements performed at the circuit level and at the individual components level confirmed the presence of latency effects. A charge injection model has been proposed which explains these results and which can be used for analyzing the latent failure mode due to ESD in other devices.

From the experiments performed on MOS transistors, it is clearly demonstrated that trapped charges are dependent on the polarity of the stress voltage. However, damage to protection diodes was independent of stress polarity and resulted in an increase in the leakage current. The increase in leakage can be modelled by the growth of conducting filaments between the diodes induced by the overcurrent conditions during ESD. When considering the protection circuit as a whole, a majority of the current would flow through the protection diodes during EOS/ESD. For low level (<1kV) EOS/ESD, the damage sites were confined to the protection diodes. Since the diodes require a finite amount of time to be brought in conduction, for medium to high level (>1kV) EOS/ESD, the stress would reach the MOS transistors. Therefore, the damage sites spread to the transistors. The increased leakage current was caused by

both the protection network circuit and the transistor cell, with the leakage current through the protection network being dominant. For higher levels of EOS/ESD, damage occurred in the contact cuts between two layers which vaporized when subjected to the high current density during ESD. In all cases, the quiescent current increased independently of applied stress polarity.

Measurements made on the individual transistors showed that there was a shift in the threshold voltages. The experiments showed that the transistor cell, during increasing ESD stress, first showed an increase in leakage current, followed by a shift in the threshold voltage as the leakage current increased further. It is proposed that the initial increase in the leakage current is due to damage to the parasitic diodes associated with the edges of the gate electrode, where an enhanced electric field exists. At higher stress levels, charge is injected through the gate and becomes trapped causing a further increase in the leakage current: a shift in the threshold voltage results. Carriers can be injected into the gate oxide either by emission or by tunnelling. In both cases, the carriers gain sufficient energy from the externally applied electric field to overcome the potential barrier at the Si-SiO_2 interface. The total leakage current is now caused by leakage through the parasitic diodes, and an effective reduction in channel length, due to the trapped charge.

Using the C-V techniques, the properties of trapped charge related to EOS/ESD voltage were studied. In general, experiments have shown that charge was located in deeper traps for higher EOS/ESD voltage stresses. Higher excitation energies, using thermal and optical methods, were required to release a portion of this charge. In addition, there was no direct evidence of a correlation between the thermal and electrical sensitivity of MOS devices. The thermal shock test used in these experiments

produces non-reversible damage to devices and cannot be used to predict latent failures. Due to dissimilar coefficients of thermal expansion of the materials used, the observed degradation was caused by stress induced damage at interfaces. In other words, the results of the thermal shock tests depend heavily on the quality of the wafer whereas, for electrical stress tests, the layout of the protection network circuits is a key factor affecting performance.

After examining the nature of failures in integrated circuit subjected to ESD, a generalized safety factor was developed for a typical integrated circuit, as shown in Figure 6.1. The safety factor definition is consistent with the purpose of the protection structure which is to increase the EOS/ESD immunity of the device without interfering with the normal operation of the circuit. The shunt elements are active devices used to divert current away from the inner devices to be protected. During normal operation, the shunt elements are in a high impedance state and switch to a low impedance state during overstress conditions. The series element, usually a resistor, is used to limit the current to the internal device structure during ESD.

The susceptibility of the internal circuit depends on how fast the shunt elements change conductivity. For direct ESD, the factor which indicates the susceptibility of the internal circuit depends on two parameters; (1) the rate of change of discharge current, i, and (2) the amplitude of discharge voltage, V. *i.e.*

$$\text{Safety Factor} = \frac{di}{dt} * \frac{dV}{dt}$$

$$= \frac{d^2E}{dt^2} \qquad \ldots(6.1)$$

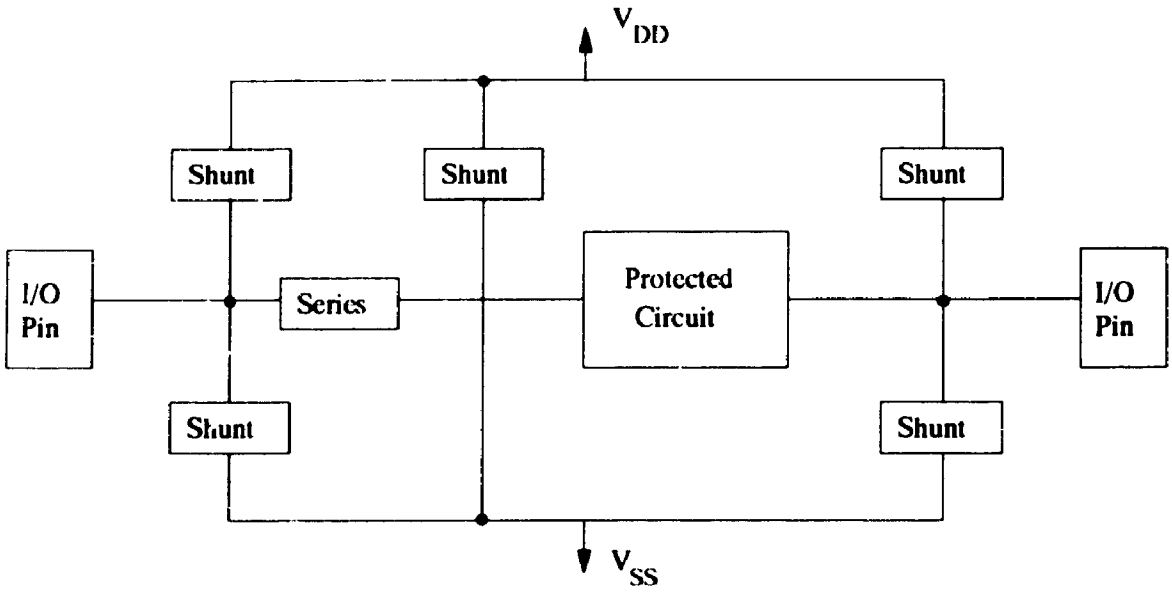


Figure 6.1 Typical Protection Structure of an Integrated Circuit

The susceptibility of the internal circuit under direct current injection depends on the rate of change of the ESD energy which is injected into the I/O pin rather than the amplitude of the discharge current or voltage. The safety factor of an integrated circuit depends on the shunt element speed and is usually determined by the design and fabrication processes. However, the rise time or rate of change of discharge current can be varied and depends on: (1) type of ESD discharge, *i.e.* Human Body Model, Charged Device Model, Machine Model, Field Induced Model, air or direct discharge etc. and, (2) input impedance of the integrated circuit. If a discharge energy deposition in terms of time is lower than the threshold value given by the protection circuit safety factor, the inner circuit will be protected. Otherwise, it will be damaged. Thus, for the same ESD voltage, damage to the internal circuit can occur while in other cases, no damage results.

The results reported in this thesis pertain to a series of measurements and analyses performed on simple integrated circuits. The work demonstrated the importance of modular test structures in failure analysis. It was found to be necessary to make measurements at the individual component level to explain the results of failure analyses performed at the global or device level. As the feature size of very large scale integrated circuits continues to decrease, and their density and complexity grows, there is a need to integrate test structures with the device circuitry in order to improve reliability.

An ideal test structure of the future would protect the circuit and upon command would provide information, not only on the present condition of the device, but also give an indication of the cumulative stress events to which the device has been already subjected. Such intelligent test structures would benefit semiconductor designers, since they could be used not only for failure analysis, but would become the basis of reconfigurable devices, which are essential in fault tolerant electronic systems.

Appendix A

Effect of Charge on MOS Structures

The physics of ideal and non-ideal MOS structures has been extensively studied. A review will be presented of the effect of various substrate dopant impurity distributions, and fixed charge, in the oxide, interface and substrate, on the threshold voltage of a basic p-type substrate MOS capacitor. The cross-sectional view of a p-type substrate MOS capacitor is shown in Figure 1. A similar analysis can be done for n-type substrate devices.

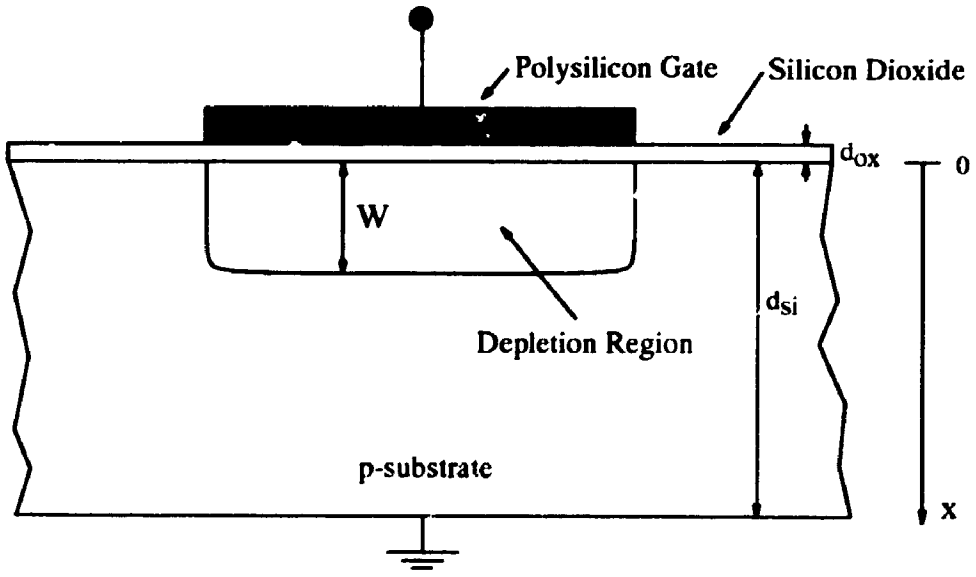


Figure A.1 A p-type MOS Capacitor

1.1 Ideal System

In an ideal MOS-C structure, one assumes that : (1) the oxide is a perfect insulator and no current flows through the oxide layer under all bias conditions; (2) there are no recombination-generation (R-G) centers located at the oxide-semiconductor interface

and inside the oxide; (3) the semiconductor is uniformly doped; (4) the gate electrode is sufficiently thick to be considered as an equipotential region under all bias conditions. In the following discussion, the MOS-C is assumed to be an ideal structure.

1.1.1 Uniform Charge Distribution

Consider the ideal p-type substrate MOS capacitor shown in Figure A.1, in which the charge is homogeneously distributed. The field in the capacitor can be determined by solving Laplace's and Poisson's Equations.

$$\nabla^2 V = 0 \qquad (oxide) \qquad \ldots(A.1)$$

$$\nabla^2 V = \frac{-\rho}{\varepsilon_{Si}} \qquad (silicon) \qquad \ldots(A.2)$$

When a negative voltage is applied to the gate, majority carriers (holes) are attracted to the oxide-semiconductor interface. The capacitor is in the charge accumulation mode; the electrical characteristics are similar to that of a parallel plate capacitor with the gate electrode forming one plate and the substrate forming the other. Using the Laplace's equation and the boundary conditions, V = 0 at silicon dioxide-silicon interface (x = 0) and V = V_o at gate-silicon dioxide (x = d_{ox}), the potential is given by :

$$V = \frac{V_o}{d_{ox}} x \qquad for \quad 0 < x < d_{ox} \qquad \ldots(A.3)$$

The electric field corresponding to this potential is :

$$E = -\nabla V = -\frac{V_o}{d_{ox}} \qquad for \quad 0 < x < d_{ox} \qquad \ldots(A.4)$$

The surface charge densities per unit area, ρ_s, on the two plates are given by :

$$\rho_s|_{x=0} = D|_{x=0} = \frac{\varepsilon_{ox} V_o}{d_{ox}} \qquad \ldots(A.5)$$

$$\rho_s|_{x=d_{ox}} = D|_{x=d_{ox}} = -\frac{\varepsilon_{ox} V_o}{d_{ox}} \qquad \ldots(A.6)$$

The surface charge density per unit gate area, ρ_s, is :

$$Q = |\rho_s| = \frac{\varepsilon_{ox} V_o}{d_{ox}} \qquad \ldots(A.7)$$

The oxide capacitance per unit gate area, C_{ox}, is :

$$C_{ox} = \frac{Q}{V_o} = \frac{\varepsilon_{ox}}{d_{ox}} \qquad \ldots(A.8)$$

Since there is no depletion layer formed, the total gate-to-substrate capacitance per unit area is C_{ox}.

When a positive voltage is applied to the gate, majority carriers (holes) are depleted from the region under the gate and the negatively charged acceptors attracted to the interface. The volume charge density per unit area in this region is dominated by the acceptors, N_A, and is given by:

$$\rho = -qN_A \quad C cm^{-3} \qquad \ldots(A.9)$$

This region is called the depletion region or space-charge region. The charge and potential distribution are determined by the solution of Poisson's equation.

$$\nabla^2 V = -\frac{\rho}{\varepsilon_{si}} = \frac{qN_A}{\varepsilon_{si}} \qquad \ldots(A.10)$$

For a depletion width of W, the following boundary conditions are applied.

$$V = 0, \quad \frac{\partial V}{\partial x} \rightarrow 0 \quad at \quad x = W \qquad \ldots(A.11)$$

Solving Poisson's equation, the potential is :

$$V = \frac{qN_A}{2\varepsilon_{si}}(x - W)^2 \qquad 0 \leq x \leq W \qquad \ldots(A.12)$$

The surface potential, φ_s, at x = 0, is :

$$\varphi_s = \frac{qN_A}{2\varepsilon_{si}} W^2 \qquad \ldots(A.13)$$

At the semiconductor surface, x = 0, the electric field, E_s, is :

$$E_s = -\nabla V|_{x=0} = -\frac{qN_A}{\varepsilon_{si}} W \qquad \ldots(A.14)$$

The normal component of the D-field discontinuity is given by the surface charge density. If no surface charge is present at the interface, the electric field in the oxide is :

$$E_{ox} = \frac{\partial V}{\partial x}\Big|_{ox} = \frac{\varepsilon_{si}}{\varepsilon_{ox}} \frac{\partial V}{\partial x}\Big|_{x=0} = \frac{qN_A}{\varepsilon_{ox}} W \qquad \ldots(A.15)$$

The gate voltage , V_G, applied across the p-type MOS capacitor is equal to the voltage across the oxide, ϕ_{ox}, and the surface potential , ϕ_s, at the semiconductor surface.

$$V_G = \phi_s + V_{ox} = \frac{qN_A}{2\varepsilon_{si}}W^2 + \frac{qN_A}{\varepsilon_{ox}}Wd_{ox} \qquad ...(A.16)$$

Thus, the small signal gate capacitance is :

$$C_g = \frac{\partial Q}{\partial V_g} = \left(\frac{\varepsilon_{si}}{W}+\frac{\varepsilon_{ox}}{d_{ox}}\right)^{-1} = \left(\frac{1}{C_D}+\frac{1}{C_{ox}}\right)^{-1} \qquad ...(A.17)$$

where C_D = depletion layer capacitance per unit area

$$= \frac{\varepsilon_{si}}{W}$$

C_{ox} = oxide capacitance per unit area

$$= \frac{\varepsilon_{ox}}{d_{ox}}$$

1.1.1.1 Threshold Voltage Calculation

The electron and hole concentrations in the semiconductor are related to the intrinsic carrier concentration of the semiconductor, n_i, Fermi level, E_F and intrinsic level, E_i. If we let the electrostatic potential, ϕ, be zero in the bulk of the semiconductor, i.e. E_i, the electron and hole concentrations are given by :

$$n = n_i e^{(E_i - E_F)/kT} = n_i e^{q(\phi - \phi_B)/kT} \qquad ...(A.18)$$

$$p = n_i e^{(E_F - E_i)/kT} = n_i e^{q(\phi_B - \phi)/kT} \qquad ...(A.19)$$

In the depletion mode, the concentration of electrons and holes in the depletion region are negligible. Therefore, the volume charge density in the depletion region is dominated by the acceptor density, N_A :

$$\rho = -qN_A \quad Ccm^{-3} \qquad \ldots(A.20)$$

When the gate voltage is increased further, the electron concentration becomes comparable to the acceptor density at the surface. When they are equal, the MOS system is said to be in "midgap". A further increase in surface potential will create a layer of electrons at the semiconductor surface; this layer is called the "inversion layer" and the system is in an "inversion mode". At inversion, the electron concentration at the surface is equal to the acceptor density in the substrate. The gate voltage is called the threshold voltage. The surface potential, ϕ_s, is equal to $2\phi_B$, where $q\phi_B$ is the energy difference between the actual and intrinsic Fermi levels of the bulk semiconductor.

$$N_A = n = n_i e^{q(\phi - \phi_B)/kT} \qquad (at \quad surface) \qquad \ldots(A.21)$$

$$N_A = p = n_i e^{q(\phi_B - \phi)/kT} \qquad (at \quad bulk) \qquad \ldots(A.22)$$

Solving equation (A.21),

$$\phi_B = \frac{KT}{q} \ln\left(\frac{N_A}{n_i}\right) \qquad \ldots(A.23)$$

Comparing equation (A.21) and (A.22), the onset of strong inversion occurs when :

$$(\varphi - \varphi_B)\big|_{surface} = (\varphi_B - \varphi)\big|_{bulk} \qquad \ldots(A.24)$$

Taking the potential at substrate as the reference:

$$\varphi_{surface} = 2\varphi_B \qquad \ldots(A.25)$$

At threshold voltage, the surface depletion width is maximum. From (A.12) :

$$\begin{aligned} W_{max} &= \left(\frac{2\varepsilon_{si}\varphi_s}{qN_A}\right)^{1/2} \\ &= \left(\frac{2\varepsilon_{si}(2\varphi_B)}{qN_A}\right)^{1/2} \\ &= \left(\frac{4\varepsilon_{si}KT\ln(N_A/n_i)}{q^2N_A}\right)^{1/2} \end{aligned} \qquad \ldots(A.26)$$

The threshold voltage is:

$$\begin{aligned} V_T &= V_G \\ &= V_{ox} + \varphi_{s.\,face} \\ &= \frac{qN_A}{\varepsilon_{ox}} W_{max} d_{ox} + 2\varphi_B \\ &= \frac{\sqrt{4\varepsilon_{si}qN_A\varphi_B}}{C_{ox}} + 2\varphi_B \\ &= \frac{Q_B}{C_{ox}} + 2\varphi_B \end{aligned} \qquad \ldots(A.27)$$

where $Q_B = \sqrt{4\varepsilon_{si}qN_A\varphi_B}$ is the charge in the depletion region per unit surface area.

Using equations (A.16) and (A.26), the relationship between the applied gate voltage and the surface potential in an inversion is derived as follows:

$$\begin{aligned} V_G &= \phi_s + V_{ox} \\ &= \phi_s - \frac{Q_{si}}{C_{ox}} \\ &= \phi_s - \frac{Q_N - qN_A W}{C_{ox}} \\ &= \phi_s - \frac{Q_N}{C_{ox}} + \frac{qN_A}{C_{ox}}\left(\frac{2\varepsilon_{si}\phi_s}{qN_A}\right)^{1/2} \end{aligned} \qquad \ldots(A.28)$$

where :

V_G = gate voltage

ϕ_s = surface potential

V_{ox} = voltage across gate oxide

Q_N = inversion charge

C_{ox} = oxide capacitance per unit area

q = magnitude of electron charge

N_A = acceptor doping concentration

W = depletion width

Re-arranging equation (A.28), ϕ_s is :

$$\phi_s = V_G + \frac{Q_N}{C_{ox}} - V_0\left\{\left(1 + \frac{2\left(V_G + \frac{Q_N}{C_{ox}}\right)}{V_0}\right)^{1/2} - 1\right\} \qquad \ldots(A.29)$$

where :

$V_0 = q\varepsilon_{si}N_A/C_{ox}^2$

The maximum electric field occurs at the interface and can be calculated from (A.15) and (A.26).

$$\begin{aligned} E_{si} &= \frac{qN_A}{\varepsilon_{si}} W \\ &= \left(\frac{2qN_A}{\varepsilon_{si}} \phi_s \right)^{1/2} \\ &= \left(\frac{2qN_A}{\varepsilon_{si}} (V_G - V_T) \right)^{1/2} \end{aligned} \qquad (A.30)$$

1.1.2 Linear Charge Distribution

If the charge density is linearly distributed in the substrate, the potential can be determined by solving Poiss 's Equation:

$$\nabla^2 V = -\frac{\rho_o}{\varepsilon_{si}} K \left(1 - \frac{x}{d_{si}} \right) \qquad \ldots(A.31)$$

Using the boundary conditions, $V = 0$, $\frac{\partial V}{\partial x} \rightarrow 0$ *at* $x = W$, the potential is

$$V = \frac{\rho_o K}{\varepsilon_{si}} \left(-\frac{x^2}{2} + \frac{x^3}{6d_{si}} + Wx - \frac{W^2}{2d_{si}} x - \frac{W^2}{2} + \frac{W^3}{3d_{si}} \right) \qquad \ldots(A.32)$$

At the interface (x=0), the potential is:

$$\phi_s = \frac{\rho_o K}{\varepsilon_{si}} \left(\frac{W^3}{3d_{si}} - \frac{W^2}{2} \right) \qquad \ldots(A.33)$$

and the electric field at the interface is:

$$E_{st} = \frac{-\rho_o K}{\varepsilon_{st}}\left(\frac{W^2}{d_{st}} - W\right) \qquad \ldots(A.34)$$

If no surface charge is present at the interface, the electric field in the oxide is:

$$E_{ox} = \frac{\rho_o K}{\varepsilon_{ox}}\left(\frac{W^2}{d_{st}} - W\right) \qquad \ldots(A.35)$$

and the voltage across the oxide is :

$$V_{ox} = -d_{ox}\frac{\rho_o K}{\varepsilon_{ox}}\left(\frac{W^2}{d_{st}} - W\right) \qquad \ldots(A.36)$$

The gate voltage applied across the p-type MOS capacitor is equal to the voltage across the oxide and the surface potential at the semiconductor surface:

$$V_g = V_{ox} + \phi_s \qquad \ldots(A.37)$$

At the threshold voltage, the surface depletion width is at a maximum and can be calculated from (A.33).

1.1.3 Exponential Charge Distribution

The following calculation assumes the charge density is exponentially distributed in the substrate.

The charge and potential distribution are determined by solution of Poisson's equation.

$$\nabla^2 V = -\frac{\rho}{\varepsilon_{st}} K e^{-\lambda x} \qquad \ldots(A.38)$$

Using the boundary conditions, $V = 0$, $\frac{\partial V}{\partial x} \rightarrow 0$ *at* $x = W$, the potential is

$$V_{si} = \frac{-\rho_o K}{\varepsilon_{si}\lambda}\left(\frac{e^{-\lambda x}}{\lambda^2} + \frac{e^{-\lambda W}}{\lambda}x - \frac{e^{-\lambda W}}{\lambda^2} - \frac{e^{-\lambda W}}{\lambda}W\right) \qquad \ldots(A.39)$$

At the interface, the potential is:

$$\phi_s = \frac{-\rho_o K}{\lambda\varepsilon_{si}}\left(\frac{1}{\lambda^2} - \frac{e^{-\lambda W}}{\lambda^2} - \frac{e^{-\lambda W}}{\lambda}W\right) \qquad \ldots(A.40)$$

At the semiconductor surface, the electric field is :

$$E_{si} = \frac{\rho_o K}{\varepsilon_{si}} W e^{-\lambda W} \qquad \ldots(A.41)$$

If no surface charge is present at the interface, the electric field in the oxide is:

$$E_{ox} = \frac{-\rho_o K}{\varepsilon_{ox}} W e^{-\lambda W} \qquad \ldots(A.42)$$

and the voltage across the oxide is :

$$V_{ox} = \frac{\rho_o K}{\varepsilon_{ox}} W e^{-\lambda W} d_{ox} \qquad \ldots(A.43)$$

The gate voltage applied across the p-type MOS capacitor is equal to the voltage across the oxide and the surface potential at the semiconductor surface:

$$V_g = V_{ox} + \phi_{surface} \qquad \ldots(A.44)$$

At the threshold voltage, the surface depletion width is at a maximum and can be calculated from (A.40).

1.2 Non-ideal System

In an ideal MOS system, there is no band bending at zero gate voltage; the flatband voltage, i.e. the voltage which has to be applied on the gate to achieve the flat band condition, is zero. As shown in Figure 1.9 for a real MOS system, the work function difference, the charges in the oxide, and the traps at the Si-SiO_2 interface can cause a non-zero flatband voltage. The flatband voltage for an non-ideal MOS system is equal to the work function difference and the voltage shift generated by the charges in the Si-SiO_2 system.

$$V_{FB} = \phi_{ms} - \frac{Q_{Si-SiO_2}}{C_{ox}} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot} + Q_{it}}{C_{ox}} \qquad \ldots(A.45)$$

where
- V_{FB} = flatband voltage
- ϕ_{ms} = work function difference
- Q_{Si-SiO_2} = charges in Si-SiO_2 system
- Q_f = fixed oxide charge
- Q_m = mobile ionic charge
- Q_{ot} = oxide trapped charge
- Q_{it} = interface trapped charge

Therefore, the threshold voltage for a non-ideal MOS system is:

$$V_T = V_{FB} + \frac{\sqrt{4\varepsilon_{si} q N_A \phi_B}}{C_{ox}} + 2\phi_B \qquad \ldots(A.46)$$

where V_T = threshold voltage

ε_{si} = permittivity of silicon

q = charge of electron

N_A = acceptor impurity density

ϕ_B = bulk potential

Appendix B

C-V Analysis Techniques

Although studies have shown that the quiescent current measurement method, which measures the power supply current during the circuit's quiescent state , is an effective method to detect non-stuck-at faults, it does not provide any information on the nature of defects. C-V measurements are usually used to provide this information during failure analysis. The relationship between the trap location, density, energy and ESD voltage can be studied using C-V techniques.

1.1 C-V Analysis

Typical C-V characteristics and the equivalent circuits of an n-type MOS-C responding to a small ac signal superimposed on a dc bias, are shown in Figures B.1 and B.2 respectively.

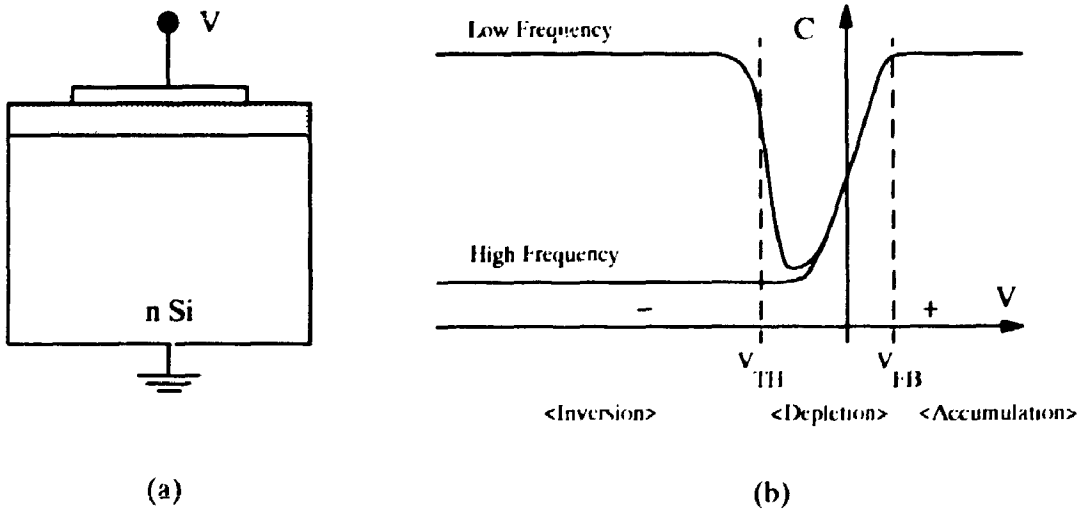


Figure B.1 Typical C-V Characteristics of n-type MOS-C

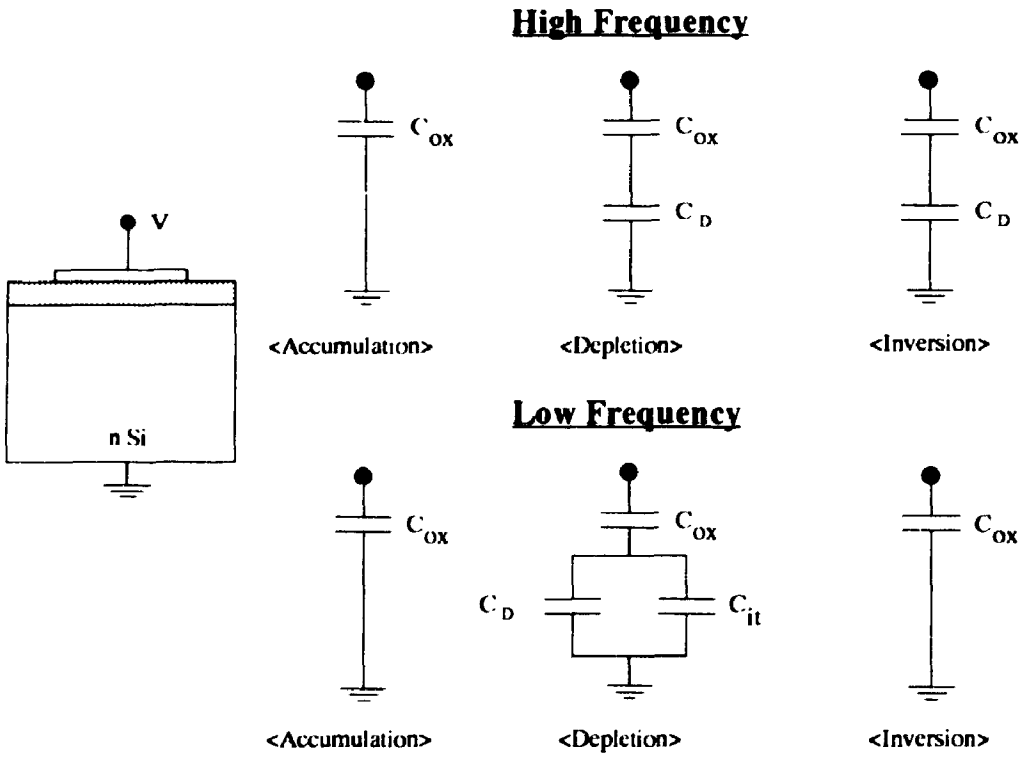


Figure B.2 Equivalent Circuits of n-type MOS-C

The quasistatic capacitance must be measured at a sufficiently low frequency (mHz) so that all traps completely respond to the input signal. To measure the high frequency capacitance, a small sinusoidal (10mV), high frequency (1MHz) signal is superimposed on a dc bias It is assumed that all traps completely respond to the low frequency signal while none respond to the sinusoidal high frequency signal. The following is a brief discussion of the measurement of high and quasistatic capacitances using different methods.

1.1.1 Low Frequency C-V Measurements

In low frequency C-V measurements, the steady state characteristics of a MOS capacitor are studied. The term "steady state" or "quasistatic" means that all

macroscopic parameters of the capacitor are either time independent or varying sinusoidally in time with time independent amplitudes. Usually in a steady state capacitance measurement, a small ac voltage is superimposed on the gate bias. The ac voltage must be within the small-signal range so that it produces a linear response of ac current. Because the test frequency required is less than 1Hz, accurate capacitance measurement techniques must be used. This difficulty can be overcome by using one of the following methods.

1.1.1.1 Ramp Method

In this method, a linear voltage ramp is applied to the MOS capacitor and the resulting displacement current is measured. The displacement current, I_G, flowing through the MOS capacitor, in response to a time varying voltage V, is related to the differential capacitance by :

$$\begin{aligned} I_G &= \frac{dQ}{dt} \\ &= \left(\frac{dQ}{dV}\right)\left(\frac{dV}{dt}\right) \\ &= C_x\left(\frac{dV}{dt}\right) \end{aligned} \qquad \ldots(B.1)$$

where :

I_G = displacement current
Q = charge in the capacitor-under-test
V = voltage across the capacitor-under-test
C_x = capacitance of the capacitor-under-test
t = time

If the slope of the linear voltage ramp, V, is "a",

$$C_x = \frac{I_G}{a} \qquad \ldots(B.2)$$

where :

C_x = capacitance of the capacitor-under-test

I_G = displacement current

a = slope of the linear voltage ramp

However, since the displacement currents are in the picoampere range, a direct measurement of the displacement current can only be done with a highly sensitive amperemeter and noise problems are usually encountered. The measured current is proportional to the ramp rate. Thus, the signal is smaller at slower ramp rates, which are often needed for devices with long minority carrier response times.

An indirect measurement method, using an amplifier, which can be used to measure the displacement current through the MOS capacitor in response to a linear voltage ramp is shown in Figure B.3.

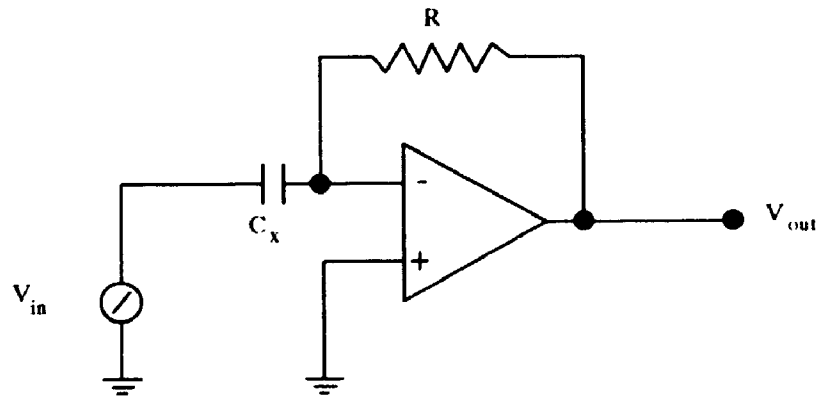


Figure B.3 Low Frequency Capacitance Measurement Using Ramp Method

The output of this amplifier is :

$$V_{out} = -RC_x \frac{dV_{in}}{dt} \qquad \ldots(B.3)$$

where :

V_{out} = output voltage
V_{in} = input ramp voltage
R = resistance
C_x = capacitance of the capacitor-under-test
t = time

If V(t) = ± at, then

$$V_{out} = \mp aRC_x \qquad \ldots(B.4)$$

where :

V_{out} = output voltage
a = slope of the input ramp voltage
R = resistance
C_x = capacitance of the capacitor-under-test

This circuit is basically a differentiator; it amplifies all transients or non-linearities in the ramp. In order to obtain a true low frequency C-V curve, the gate bias sweep rate must be slow enough for both interface traps and minority carriers to follow it over the entire gate bias range. Usually the sweep rate is 50mV/sec; this corresponds to a 0.16Hz sine wave with a maximum amplitude of 50mV.

1.1.1.2 Feedback Method

This technique measures displacement charge in response to a voltage step and makes use of a feedback charge amplifier [40]. The circuit, as shown in Figure B.4,

is an integrator; therefore it reduces the effect of spurious spikes. It offers a higher signal-to-noise ratio, the signal is independent of measurement time, and it is easily distinguished from error currents at the time of the measurement.

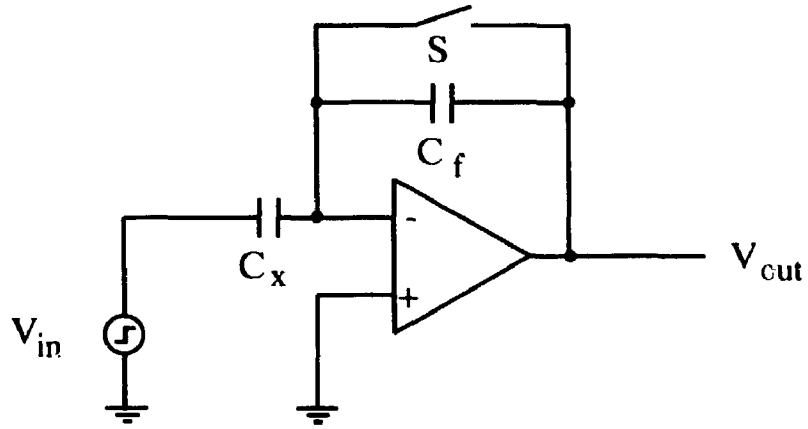


Figure B.4 Low Frequency Capacitance Measurement using Feedback Method

With reference to Figure B.4, the operation of the feedback charge method can be described as follows: when "S" is closed, the integrator acts as a voltage follower; when "S" is open, it integrates all charge deposited on the amplifier input. Since the circuit integrates the input current and any charge or current coupled to the input, Q/t is measured in the DUT at the time of the capacitance measurement, which is used to identify and correct stray-current errors and determine the equilibrium conditions. The input and output waveforms of the feedback low frequency capacitance meter is shown in Figure B.5

If the device-under-test (DUT) is an ideal capacitor with no leakage current, then the capacitance C_x can be calculated as:

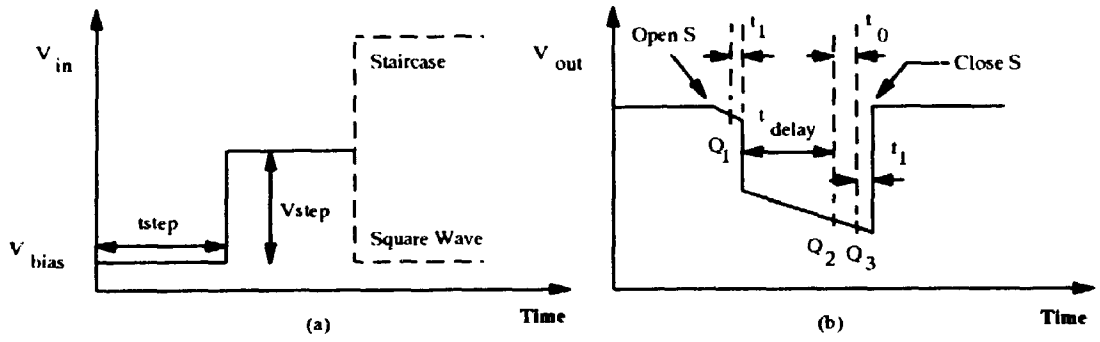


Figure B.5 (a) Input and (b) Output Waveforms of a Feedback Integrator

$$C_x = \frac{\Delta Q}{\Delta V_{in}} = \frac{Q_3 - Q_1}{\Delta V_{in}} = \frac{C_f \Delta V_{out}}{V_{step}} \qquad \ldots(B.5)$$

where :

C_x = unknown capacitance
Q = charges in capacitor
V_{in} = input voltage
V_{out} = output voltage
V_{step} = increment of input voltage

However, if the capacitor-under-test is a non-ideal capacitor with leakage current, then the leakage current can be estimated by :

$$\frac{Q}{t} = \frac{Q_2 - Q_3}{t_0} \qquad \ldots(B.6)$$

By plotting Q/t versus bias voltage, errors in the capacitance measurement caused by the leakage can be corrected as follows :

$$C_{x(corrected)} = C_x - \frac{\left(\frac{Q}{t}\right)(t_{delay} + t_0)}{V_{step}} \qquad \ldots(B.7)$$

and the corrected input voltage , V_i, is :

$$V_i = V_{bias} + \frac{1}{2}V_{step} \qquad \ldots(B.8)$$

1.1.2 High Frequency C-V Measurement

Interface charges do not respond to a small, high frequency ac signal. High frequency capacitance can be measured by superimposing a 1MHz small ac signal on the dc bias voltage. The amplitude of the ac signal must be well within the small signal range of the sample. A typical amplitude is 10 to 30 mV and the capacitance is measured by a phase sensitive detector.

1.1.3 Simultaneous High/Low Frequency Measurement

In most cases, it is more accurate to measure high and low frequency C-V curves simultaneously rather than sequentially. First, it ensures that there is no voltage shift between curves, which may be present when the two curves have to be aligned in the sequential method. A circuit diagram, which allows simultaneous CV measurement, is shown in Figure B.6. The bandpass filter routes the high frequency current to the high frequency CV meter and blocks the low frequency current. The band-reject filter routes the low frequency current to the low frequency meter and blocks the high

frequency current.

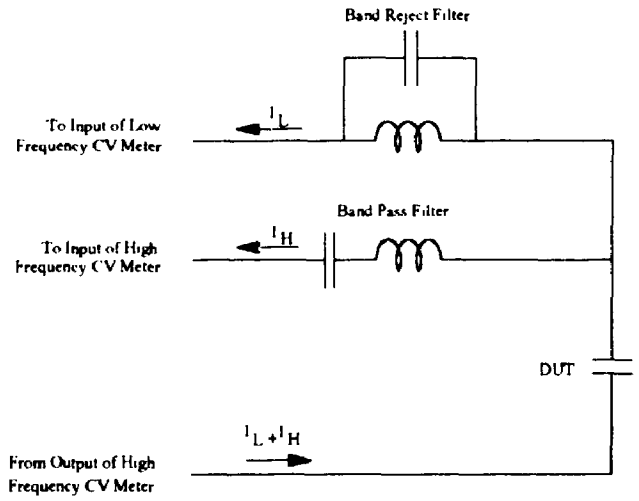


Figure B.6 Simultaneous High/Low Frequency Measurement

1.1.4 Interface Trap and Oxide Trapped Charge Calculations

Interface traps are defects which result from processing or device damage and are usually located at semiconductor interfaces. Depending on the applied voltage, these traps can be charged or discharged, and thus effectively create small device capacitances. These traps usually do not respond to small, high frequency ac signals but respon. 'o a slow dc bias; thus, these traps only affect the device capacitance at high frequency. As shown in Figure B.2, the interface capacitance (C_{it}) can be calculated by subtracting the high frequency CV curve from the low frequency CV curve during depletion. The interface trap density (D_{it}) can then be obtained by dividing C_{it} by the gate area and electron charge.

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \qquad \ldots(B.9)$$

$$D_{it} = \frac{C_{it}}{Aq} \qquad \ldots(B.10)$$

where :

C_{it} = interface trap capacitance
C_{LF} = low frequency capacitance
C_{LF} = high frequency capacitance
C_{ox} = oxide capacitance
D_{it} = interface trap density
A = gate area
q = magnitude of electron charge

The interface trap energy is derived from the band bending curve which is related to the potential at the semiconductor surface. The band bending curve is calculated from the low frequency CV curve, as shown in Figure B.7, by integrating the area between the C_{LF} and C_{ox} curves. By subtracting the bulk potential from the band bending curve, one can obtain the energy versus gate voltage curve.

Oxide trapped charges can be located at the metal-oxide interface, semiconductor-oxide interface or in the oxide. They are introduced by high energy fabrication processes, such as ion implantation or ESD/EOS. Hot electrons or holes excited by these processes are injected and trapped in the oxide. Oxide trapped charges are an important parameter in devices; they can alter the threshold voltage of a MOSFET and modify the semiconductor surface potential. The most common way to measure the oxide charge is from the voltage parallel shift in the CV curve. Figure B.8 illustrates the effect when trapped charge is present in the oxide. The voltage shift of the CV curve caused by the trapped charge can be explained as follows. As charge is introduced into the oxide, the charge balance in that region will be upset. For example, when electrons have been injected into the oxide in a n-type MOS-C, image charges

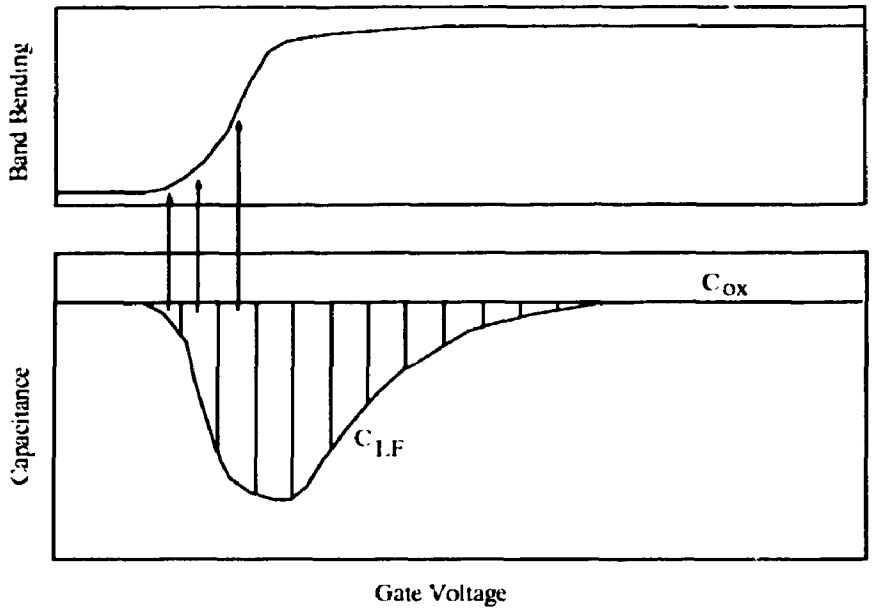


Figure B.7 Band Bending vs. Gate Voltage

are introduced in the gate and in the silicon. When a positive gate bias is applied to the structure, the image charge in the silicon will reduce the depletion layer while the image charge in the gate will decrease the negative gate charge. This effectively decreases (or shifts right) the capacitance for all gate biases except for strong accumulation and strong inversion regions where the capacitance equals C_{ox} or becomes saturated. The amount of trapped charge can be calculated from the voltage shift in the CV curve at flatband voltage, using equation B.11.

$$Q_{trap} = \Delta V_{FB} * C_{FB} \qquad \ldots(B.11)$$

where :

Q_{Trap} = oxide trapped charge

ΔV_{FB} = lateral shift in flatband voltage

C_{FB} = flatband capacitance

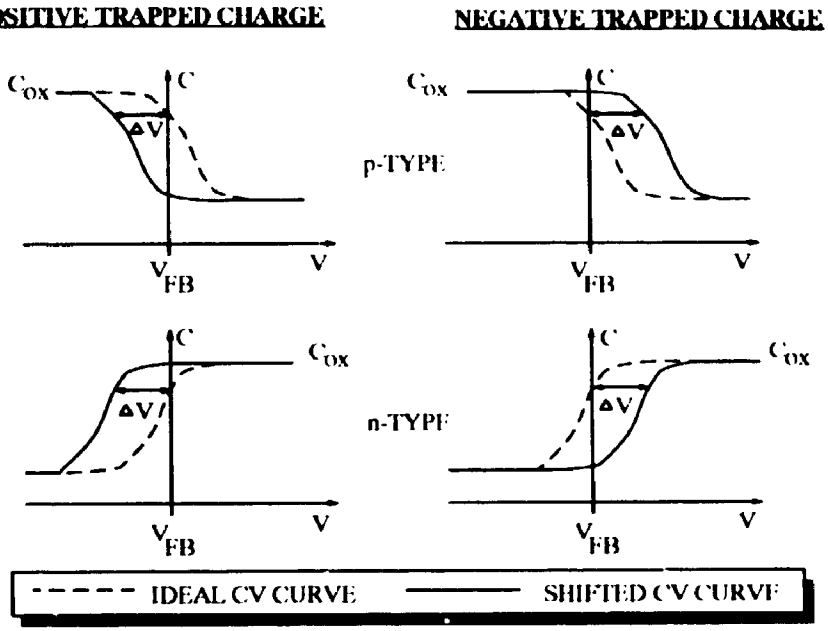


Figure B.8 Effect of Trapped Charges on High Frequency CV Curve

1.2 C-V Analysis Program

The following is a Turbo C program used to calculate the doping profile, interface trap density versus energy in the forbidden gap, band bending, effective oxide charge, semiconductor work function, and threshold and flatband voltages.

The options available in the program are as follows:

(1) Load CV data from file

(2) Print CV data

(3) Print Analysis Constants

(4) Draw Low Frequency C vs. Gate Voltage

(5) Draw High Frequency C Vs. Gate Voltage

(6) Draw High/Low Frequency C vs. Gate Voltage

(7) Draw Depletion Depth vs. Gate Voltage

(8) Draw Doping Profile vs. Depletion Depth

(9) Draw Interface Trap Density vs. Trap Energy

(10) Draw High Frequency $1/C^2$ vs. Gate Voltage

(11) Draw Band Bending vs. Gate Voltage

(12) Draw Low Frequency C vs. Band Bending

(13) Exit program

The format of input data file is:

First Line : No. of reading, gate oxide capacitance, thickness of oxide, gate area and doping concentration.

Remaining Lines : Low frequency capacitance, high frequency capacitance and gate voltage.

1.2.1 Listing of the Program

```
#include <stdio.h>
#include <math.h>
#include <graphics.h>
#include <stdlib.h>
#include <conio.h>
#include <ctype.h>

#define MAXPT    200                /* Max data points */

void menu(void);
void datain(void);
void CVdata(void);
void CVconst(void);
void maxmin(void);
void linegraph(int key);
void setup_scr(void);

const float q    = 1.60219e-19;      /* Charge of electron, C */
const float KT   = 4.046e-21;        /* Thermal energy at room temp, J */
const float Eox  = 3.4e-13;          /* Permittivity of SiO2, F/cm */
const float Es   = 1.04e-12;         /* Permittivity of Si, F/cm */
const float Eg   = 1.12;             /* Energy gap of silicon, eV */
const float ni   = 1.45e10;          /* Intrinsic carrier conc @ 300K, cm-3 */
const float Ng   = 1e20;             /* n+ poly gate donor doping, cm-3 */
```

```
FILE *fptr;
char *fname;
char autoscale;
float Vgs[MAXPT];
float Ch[MAXPT];
float Cq[MAXPT];
float dpt[MAXPT];
float N[MAXPT];
float Cit[MAXPT];
float Dit[MAXPT];
float BBend[MAXPT];
float TrapE[MAXPT];
float Csqu[MAXPT];
float Cox,area,Nx;
float Lb,CFb,VFb,VTh,PhiB,tox,WF,Qeff;
float x[MAXPT],y[MAXPT],z[MAXPT];
float xmax,xmin,ymax,ymin,xscale,yscale;
int cnt;
int bye,ok;
int xmax_scr,ymax_scr;

/* ------------------------------------------------------------------ */

void main(void)
  {

    bye=0;
    while (bye != 1)
      menu();
  }

/* ------------------------------------------------------------------ */

void menu(void)
  {
    int i,choice;
    char inbuf[130];

    printf("\n\n=================================================");
    printf("\n                  CV Analysis Program");
    printf("\n=================================================");
    printf("\n\n(1)  Load CV data from file");
    printf("\n(2)  Print CV data");
    printf("\n(3)  Print Analysis Constants");
    printf("\n(4)  Draw Low Frequency C vs. Gate Voltage");
    printf("\n(5)  Draw High Frequency C vs. Gate Voltage");
    printf("\n(6)  Draw High/Low Frequency C vs. Gate Voltage");
    printf("\n(7)  Draw Depletion Depth v . Gate Voltage");
    printf("\n(8)  Draw Doping Profile vs. Depletion Depth");
    printf("\n(9)  Draw Interface Trap Density vs. Trap Energy");
    printf("\n(10) Draw High Frequency 1/C^2 vs. Gate Voltage");
    printf("\n(11) Draw Band Bending vs. Gate Voltage");
    printf("\n(12) Draw High Frequency C vs. Band Bending");
    printf("\n(13) Draw Low Frequency C vs Band Bending");
    printf("\n(14) Exit Program");
    printf("\n\n=================================================");

    printf("\n\n\nEnter number to select from menu : ");
    gets(inbuf);
    sscanf(inbuf, "%d", &choice);

    switch (choice) {
      case 1:  datain(); break;
      case 2:  CVdata(); break;
      case 3:  CVconst(); break;
      case 4:  {  for (i=1; i<=cnt; i++)
               {
                 x[i]=Vgs[i];
                 y[i]=Cq[i]*1e12;
               }
```

```
        maxmin();
        if (autoscale == 'N')
          {
            printf("\n\nVgs (MAX),(MIN) = %5.2f %5.2f ",xmax,xmin);
            printf("\nEnter new values for Vgs (MAX),(MIN) : ");
            gets (inbuf);
            sscanf(inbuf,"%f,%f",&xmax,&xmin);
            printf("\n\nCq (MAX),(MIN) = %5.2e , %5.2e ",ymax,ymin);
            printf("\nEnter new values for Cq (MAX),(MIN) : ");
            gets (inbuf);
            sscanf(inbuf,"%f,%f",&ymax,&ymin);
          }
        linegraph(4); } break;
case 5:  {  for (i=1; i<=cnt; i++)
          {
            x[i]=Vgs[i];
            y[i]=Ch[i]*1e12;
          }
        maxmin();
        if (autoscale == 'N')
          {
            printf("\n\nVgs (MAX),(MIN) = %5.2f %5.2f ",xmax,xmin);
            printf("\nEnter new values for Vgs (MAX),(MIN) : ");
            gets (inbuf);
            sscanf(inbuf,"%f,%f",&xmax,&xmin);
            printf("\n\nCh (MAX),(MIN) = %5.2e , %5.2e ",ymax,ymin);
            printf("\nEnter new values for Ch (MAX),(MIN) : ");
            gets (inbuf);
            sscanf(inbuf,"%f,%f",&ymax,&ymin);
          }
        linegraph(5); } break;
case 6:  {  for (i=1; i<=cnt; i++)
          {
            x[i]=Vgs[i];
            y[i]=Ch[i]*1e12;
            z[i]=Cq[i]*1e12;
          }
        maxmin();
        if (autoscale == 'N')
          {
            printf("\n\nVgs (MAX),(MIN) = %5.2f %5.2f ",xmax,xmin);
            printf("\nEnter new values for Vgs (MAX),(MIN) : ");
            gets (inbuf);
            sscanf(inbuf,"%f,%f",&xmax,&xmin);
            printf("\n\nCq (MAX),(MIN) = %5.2e , %5.2e ",ymax,ymin);
            printf("\nEnter new values for Cq (MAX),(MIN) : ");
            gets (inbuf);
            sscanf(inbuf,"%f,%f",&ymax,&ymin);
          }
        linegraph(6); } break;
case 7:  {  for (i=1; i<=cnt; i++)
          {
            x[i]=Vgs[i];
            y[i]=dpt[i]*1e4;
          }
        maxmin();
        if (autoscale == 'N')
          {
            printf("\n\nVgs (MAX),(MIN) = %5.2f %5.2f ",xmax,xmin);
            printf("\nEnter new values for Vgs (MAX),(MIN) : ");
            gets (inbuf);
            sscanf(inbuf,"%f,%f",&xmax,&xmin);
            printf("\n\nDepth (MAX),(MIN) = %5.2e , %5.2e ",ymax,ymin);
            printf("\nEnter new values for Depth (MAX),(MIN) : ");
            gets (inbuf);
            sscanf(inbuf,"%f,%f",&ymax,&ymin);
          }
        linegraph(7); } break;
case 8:  {  for (i=1; i<=cnt; i++)
          {
```

```
                x[i]=dpt[i]*1e4;
                y[i]=fabs(N[i]);
              }
            maxmin();
            if (autoscale == 'N')
              {
                printf("\n\nDepth (MAX),(MIN) = %5.2e %5.2e ",xmax,xmin);
                printf("\nEnter new values for Depth (MAX),(MIN) : ");
                gets (inbuf);
                sscanf(inbuf,"%f,%f",&xmax,&xmin);
                printf("\n\nN (MAX),(MIN) = %5.2e , %5 2e ",ymax,ymin);
                printf("\nEnter new values for N (MAX),(MIN) : ");
                gets (inbuf);
                sscanf(inbuf,"%f,%f",&ymax,&ymin);
              }
                  ymin=log10(ymin);
            ymax=log10(ymax);
            for (i=1; i<=cnt; i++)
              y[i]=log10(y[i]);
            linegraph(8); } break;
      case 9:  {  for (i=1; i<=cnt; i++)
              {
                x[i]=TrapE[i];
                y[i]=fabs(Dit[i]);
              }
            maxmin();
            if (autoscale == 'N')
              {
                printf("\n\nTrap Energy (MAX),(MIN) = %5.2e %5.2e ",xmax,xmin);
                printf("\nEnter new values for Trap Energy (MAX),(MIN) : ");
                gets (inbuf);
                sscanf(inbuf,"%f,%f",&xmax,&xmin);
                     printf("\n\nTrap  Density  (MAX),(MIN)  =  %5.2e  ,  %5.2e
",ymax,ymin);
                printf("\nEnter new values for Trap Density (MAX),(MIN) : ");
                gets (inbuf);
                sscanf(inbuf,"%f,%f",&ymax,&ymin);
              }
            ymin=log10(ymin);
            ymax=log10(ymax);
            for (i=1; i<=cnt; i++)
              y[i]=log10(y[i]);
            linegraph(9); } break;
      case 10: {  for (i=1; i<=cnt; i++)
              {
                x[i]=Vgs[i];
                y[i]=Csqu[i]*1e-24;
              }
            maxmin();
            if (autoscale == 'N')
              {
                printf("\n\nVgs (MAX),(MIN) = %5.2f %5.2f ",xmax,xmin);
                printf("\nEnter new values for Vgs (MAX),(MIN) : ");
                gets (inbuf);
                sscanf(inbuf,"%f,%f",&xmax,&xmin);
                printf("\n\n1/Ch^2 (MAX),(MIN) = %5.2e , %5.2e ",ymax,ymin);
                printf("\nEnter new values for 1/Ch^2(MAX),(MIN) : ");
                gets (inbuf);
                sscanf(inbuf,"%f,%f",&ymax,&ymin);
              }

            linegraph(10); } break;
      case 11: {  for (i=1; i<=cnt; i++)
              {
                x[i]=Vgs[i];
                y[i]=BBend[i];
              }
            maxmin();
            if (autoscale == 'N')
              {
```

```
                printf("\n\nVgs (MAX),(MIN) = %5.2f %5.2f ",xmax,xmin);
                printf("\nEnter new values for Vgs (MAX),(MIN) : ");
                gets (inbuf);
                sscanf(inbuf,"%f,%f",&xmax,&xmin);
                     printf("\n\nBand Bending (MAX),(MIN) = %5.2e , %5.2e
",ymax,ymin);
                printf("\nEnter new values for Band Bending (MAX),(MIN) : ");
                gets (inbuf);
                sscanf(inbuf,"%f,%f",&ymax,&ymin);
              }

            linegraph(11); } break;
      case 12: {  for (i=1; i<=cnt; i++)
              {
                x[i]=BBend[i];
                y[i]=Ch[i]*1e12;
              }
            maxmin();
            if (autoscale == 'N')
              {
               printf("\n\nBand Bending (MAX),(MIN) = %5.2e %5.2e ",xmax,xmin);
                printf("\nEnter new values for Band Bending(MAX),(MIN) : ");
                gets (inbuf);
                sscanf(inbuf,"%f,%f",&xmax,&xmin);
                printf("\n\nCh (MAX),(MIN) = %5.2e , %5.2e ",ymax,ymin);
                printf("\nEnter new values for Ch (MAX),(MIN) : ");
                gets (inbuf);
                sscanf(inbuf,"%f,%f",&ymax,&ymin);
              }

            linegraph(12); } break;
      case 13: {  for (i=1; i<=cnt; i++)
              {
                x[i]=BBend[i];
                y[i]=Cq[i]*1e12;
              }
            maxmin();
            if (autoscale == 'N')
              {
               printf("\n\nBand Bending (MAX),(MIN) = %5.2e %5.2e ",xmax,xmin);
                printf("\nEnter new values for Band Bending (MAX),(MIN) : ");
                gets (inbuf);
                sscanf(inbuf,"%f,%f",&xmax,&xmin);
                printf("\n\nCq (MAX),(MIN) = %5.2e , %5.2e ",ymax,ymin);
                printf("\nEnter new values for Cq (MAX),(MIN) : ");
                gets (inbuf);
                sscanf(inbuf,"%f,%f",&ymax,&ymin);
              }

            linegraph(13); } break;
      case 14: bye=1; break;
      default: break;  }


  }

/* ------------------------------------------------------------------ */

void datain(void)
  {
    int i;
    int point;
    float inc;
    float v,c1,c2;
    float slope;
    float BBendFb;

    printf("\n\nEnter input data file name : ");
    gets(fname);
    fptr=fopen(fname,"r");
```

```
fscanf(fptr,"%d,%f,%f,%f,%f", &cnt, &Cox, &tox, &area, &Nx);

Cox=Cox*1e-12;
tox=tox*1e-7;

if (Nx < 0.0)
  WF=KT/q*log(ni/fabs(Nx))-KT/q*log(Ng/ni);
else
  WF=KT/q*log(Nx/ni)-KT/q*log(Ng/ni);

for (i=1; i<=cnt; i++)
  {
 fscanf(fptr, "%f,%f,%f", &c2, &c1, &v);
 Vgs[i]=v;
 Ch[i]=c1*1e-12;
 Cq[i]=c2*1e-12;
  }

fclose(fptr);

Vgs[0]=Vgs[1]-(Vgs[2]-Vgs[1]);
Ch[0]=Ch[1]-(Ch[2]-Ch[1]);
Cq[0]=Cq[1]-(Cq[2]-Cq[1]);
Vgs[cnt+1]=Vgs[cnt]+(Vgs[cnt]-Vgs[cnt-1]);
Ch[cnt+1]=Ch[cnt]+(Ch[cnt]-Ch[cnt-1]);
Cq[cnt+1]=Cq[cnt]+(Cq[cnt]-Cq[cnt-1]);

/* Debye Length */

Lb=sqrt(Es*KT/(q*q*fabs(Nx)));

/* Flatband Capacitance */

CFb=(Cox*area*Es/Lb)/(Cox+(area*Es)/Lb);

/* Flatband Voltage = Voltage at Flatband Capacitance */

for (i=1; i<=cnt; i++)
  {
 if ((CFb > Ch[i]) && (CFb < Ch[i-1]))
   point=i;
  }
slope=(Vgs[point]-Vgs[point-1])/(Ch[point]-Ch[point-1]);
VFb=Vgs[point]+(CFb-Ch[point])*slope;

Qeff = CFb*(WF-VFb)/area;

/* Bulk Potential */

if (Nx > 0.0)
  PhiB=KT/q*log(fabs(Nx)/ni);
else
  PhiB=KT/q*log(ni/fabs(Nx));

/* Threshold Voltage */

VTh=VFb+2*fabs(PhiB)+sqrt(4*Es*q*Nx*PhiB)/(Cox/area);

/* Depletion depth */

for (i=1; i<=cnt; i++)
  dpt[i]=area*Es*(1/Ch[i]-1/Cox);

/* Doping profile */
```

```
      for (i=1; i<=cnt; i++)
        {
       inc=(1/(Ch[i]*Ch[i])-1/(Ch[i+1]*Ch[i+1]))/(Vgs[i+1]-Vgs[i]);
       if ((inc != 0.0) && (Ch[i]/Cox != 1.0))
         N[i]=2.0*((1-Cq[i]/Cox)/(1-Ch[i]/Cox))/(area*area*q*Es*inc);
       else
         N[i]=0.0;
        }
      N[cnt]=0.0;

      /* Interface capacitance and density */

      for (i=1; i<=cnt; i++)
        {
       if ((Cq[i] != Cox) && (Ch[i] != Cox))
         {
           Cit[i]=1/(1/Cq[i]-1/Cox)-1/(1/Ch[i]-1/Cox);
           Dit[i]=Cit[i]/(area*q);
         }
       else
         {
           Cit[i]=0.0;
           Dit[i]=0.0;
         }
        }

      /* Band bending */

      for (i=0; i<=cnt; i++)
        BBend[i]=0.0;

      for (i=1; i<=cnt; i++)
        BBend[i]=BBend[i-1]+((1-Cq[i]/Cox)+(1-Cq[i+1]/Cox))*(Vgs[i+1]-Vgs[i])/2;

      /* Band banding at flatband voltage */

      for (i=1; i<=cnt; i++)
        {
        if ((VFb > Vgs[i]) && (VFb < Vgs[i-1]))
          point=i;
        }

      slope=(BBend[point]-BBend[point-1])/(Vgs[point]-Vgs[point-1]);
      BBendFb=BBend[point]+(VFb-Vgs[point])*slope;

      /* substract band bending at flatband voltage from BBend[MAXPT] */
      /* calculate trap energy                                        */

      for (i=1; i<=cnt; i++)
        {
       BBend[i]=BBend[i]-BBendFb;
       TrapE[i]=BBend[i]-fabs(PhiB);
        }

      /* Calculate square of high frequency capacitance */

      for (i=1; i<=cnt; i++)
        Csqu[i]=1/(Ch[i]*Ch[i]);

    }

/* ------------------------------------------------------------------ */

void CVdata(void)
  {
    int i;

    printf("\n\nEnter output data file : ");
    gets(fname);
    fptr=fopen(fname,"w");
```

```
    fputs("Rdg#     Vgs(V)       Ch(pF)       Cq(pF)",fptr);
    for (i=1; i<=cnt; i++)
      fprintf(fptr,"\n%3d\t%1.3f\t%1.4e\t%1.4e", i, Vgs[i], Ch[i], Cq[i]);

   fputs("\n\n\n\n\nRdg#    W(um)     N(cm^-3)     B_Bend(V)     Et(eV)     1/Ch^2
Dit(1/cm^2eV)",fptr);
    for (i=1; i<=cnt; i++)
      fprintf(fptr,"\n%3d  %1.4e  %1.4e  %1.4e  %1.4e  %1.4e  %1.4e",
           i, dpt[i]*1e4, N[i], BBend[i],TrapE[i], Csqu[i]*1e-24, Dit[i]);

    fclose(fptr);
  }

/* ------------------------------------------------------------------- */

void CVconst(void)
  {
    char type;

    if (Nx < 0.0)
      type='p';             /* p-type substrate */
    else
      type='n';             /* n-type substrate */

    printf("\n\nEnter output data file : ");
    gets(fname);
    fptr=fopen(fname,"w");

    fputs("                    *** Analysis Constants ***\n\n\n",fptr);
     fprintf(fptr,"\nCox(pF) : %1.4e                    tox(nm) : %1.4e", Cox,
tox*1e7);
    fprintf(fptr,"\nArea(cm^2) : %1.4e              Nbulk(cm^-3) : %1.4e", area,
Nx);
     fprintf(fptr,"\nCFb(pF) : %1.4e                  VFb(V) : %1.4e", CFb*1e12,
VFb);
     fprintf(fptr,"\nVTh(V) :  %1.4e                     PhiB(V) : %1.4e", VTh,
PhiB);
     fprintf(fptr,"\nLb(um) : %1.4e                   Dev. Type : %c", Lb*1e4,
type);
  }

/* ------------------------------------------------------------------- */

void maxmin(void)
  {
    int i,j;

    xmin=x[1];
    xmax=x[1];
    i=1;
    while (y[i] == 0.0)
      i=i+1;
    ymin=y[i];
    ymax=y[i];

    for(i=1; i<=cnt; i++)
      {
     if(xmin>x[i]) xmin=x[i];
     if(xmax<x[i]) xmax=x[i];
     if (y[i] != 0.0)
       {
         if(ymin>y[i]) ymin=y[i];
         if(ymax<y[i]) ymax=y[i];
       }
     else
       {
         j=i;
         while ((y[j] == 0.0) && (j < cnt))
           j=j+1;
         if (j >= cnt)
```

```
          {
          while (y[j] == 0.0)
            j=j-1;
          }
        y[i]=y[j];
       }
      }

    printf("\nUse auto scale ? (Y/N) ");
    autoscale=getche();
    getche();
    autoscale=_toupper(autoscale);
  }

/* ------------------------------------------------------------------------ */

void setup_scr()
   {
     int i;

     int graphdriver = DETECT, graphmode, error_code;
     initgraph(&graphdriver, &graphmode, "");
     error_code=graphresult();
     ok=0;
     if (error_code!=grOk)
      printf("No graphics hardware found !");
     else
      ok=1;
   }

/* ------------------------------------------------------------------------ */

void linegraph(int key)
  {
    int i;
    float xmark,ymark,xvalue,yvalue;
    char fprint[10];
    const int mark = 8;

    setup_scr();

    if (ok == 1)
      {
     /* axis */

     setgraphmode(getgraphmode());
     line(95,410,620,410);
     line(95,410,95,40);
     line(95,40,620,40);
     line(620,410,620,40);

     xscale=525/(xmax-xmin);
     yscale=360/(1.05*(ymax-ymin));

     settextjustify(CENTER_TEXT, CENTER_TEXT);
     settextstyle(0,0,1);

     for (i=0; i<=mark; i++)
       {
         xmark=95+xscale*(xmax-xmin)*i/mark;
         line(xmark,405,xmark,415);
         xvalue=xmin+i*(xmax-xmin)/mark;
         ymark=400-yscale*1.05*(ymax-ymin)*i/mark;
         line(90,ymark,100,ymark);
         yvalue=ymin+1.05*(ymax-ymin)*i/mark;
         if (fmod(i,2) == 0)
           {
          sprintf(fprint,"%1.2f",xvalue);
          outtextxy(xmark,425,fprint);
          sprintf(fprint,"%1.2e",yvalue);
```

```
          outtextxy(55,ymark,fprint);
           }
       }

     switch (key)
       {
         case 4: { outtextxy(350,20,"Low Frequency C vs. Gate Voltage");
                   outtextxy(350,450,"Vgs (V)"); } break;
         case 5: { outtextxy(350,20,"High Frequency C vs. Gate Voltage");
                   outtextxy(350,450,"Vgs (V)"); } break;
         case 6: { outtextxy(350,20,"High/Low Frequency C vs. Gate Voltage");
                   outtextxy(350,450,"Vgs (V)"); } break;
         case 7: { outtextxy(350,20,"Depletion Depth vs. Gate Voltage");
                   outtextxy(350,450,"Vgs (V)"); } break;
         case 8: { outtextxy(350,20,"Doping Profile vs. Depletion Depth");
                   outtextxy(350,450,"Depletion Depth (um)"); } break;
         case 9: { outtextxy(350,20,"Interface Trap Density vs. Trap Energy");
                   outtextxy(350,450,"Energy (eV)"); } break;
         case 10: { outtextxy(350,20,"High Frequency 1/C^2 vs. Gate Voltage");
                    outtextxy(350,450,"Vgs (V)"); } break;
         case 11: { outtextxy(350,20,"Band Bending vs. Gate Voltage");
                    outtextxy(350,450,"Vgs (V)"); } break;
         case 12: { outtextxy(350,20,"High Frequency C vs. Band Bending");
                    outtextxy(350,450,"Band Bending (V)"); } break;
         case 13: { outtextxy(350,20,"Low Frequency C vs. Band Bending");
                    outtextxy(350,450,"Band Bending (V)"); } break;
         default: break;
       }

     settextstyle(0,1,1);
     switch (key)
       {
         case 4: outtextxy(5,220,"Capacitance (pF)"); break;
         case 5: outtextxy(5,220,"Capacitance (pF)"); break;
         case 6: outtextxy(5,220,"Capacitance (pF)"); break;
         case 7: outtextxy(5,220,"Depletion Depth (um)"); break;
         case 8: outtextxy(5,220,"Doping Profile (cm^-3) [Log Scale]"); break;
           case 9: outtextxy(5,220,"Interface Trap Density (cm^-2eV^-1) [Log
Scale]"); break;
         case 10: outtextxy(5,220,"1/Ch^2 (1/pF^2)"); break;
         case 11: outtextxy(5,220,"Band Bending (V)"); break;
         case 12: outtextxy(5,220,"Capacitance (pF)"); break;
         case 13: outtextxy(5,220,"Capacitance (pF)"); break;
         default: break;
       }

     settextstyle(0,0,1);

     if ((key==4)||(key==5)||(key==6)||(key==7)||(key==8)||(key==9)||
         (key==10)||(key==11)||(key==12)||(key==13))
       {
         setviewport(95,40,620,410,1);
         setcolor(9);
         xmark=(x[1]-xmin)*xscale;
         ymark=360-(y[1]-ymin)*yscale;
         moveto(xmark,ymark);
         for (i=2; i<=cnt; i++)
           {
           xmark=(x[i]-xmin)*xscale;
           ymark=360-(y[i]-ymin)*yscale;
           lineto(xmark,ymark);
           }
         if (key==6)
           {
           setcolor(12);
           setlinestyle(3,0,1);
           xmark=(x[1]-xmin)*xscale;
           ymark=360-(z[1]-ymin)*yscale;
           moveto(xmark,ymark);
           for (i=2; i<=cnt; i++)
```

```
            {
              xmark=(x[i]-xmin)*xscale;
              ymark=360-(z[i]-ymin)*yscale;
              lineto(xmark,ymark);
            }
          setlinestyle(0,0,1);
           }
         setcolor(0);
       }

    setviewport(0,0,639,479,1);
    getch();
    restorecrtmode();
     }
  }

/* ------------------------------------------------------------------- */
```

Appendix C

CMOS Processing Technology

A 3-micron single polysilicon, double metal P-well Complementary Metal Oxide Silicon (CMOS) technology was chosen in this project. This process is used by Northern Telecom Electronics (Ottawa, Ontario) and is available to Canadian university researchers through the Canadian Microelectronics Corporation (Kingston, Ontario). Although the processing steps are more complex than comparable nMOS technology, the low static power consumption and the high noise immunity make this technology suitable in many VLSI circuit applicatiors.

The processing steps are illustrated using an inverter as an example circuit. The p-well CMOS starts with an n-type substrate. The first step is to define the p-wells in the substrate. Thick silicon dioxide on the p-well is etched away to allow p implantation (Figure C.1(a)). A similar step is used to define the n-well region in the substrate (Figure C.1(b)).

The next step is to define the device wells. First, a layer of silicon nitride is deposited on the thin silicon dioxide layer in which it will become the sources, drains, channel regions and diffusion interconnections. Second, a p-guard mask is used to put a p-implant into the p-well region. Finally, the silicon nitride is etched away and a thin layer of silicon dioxide is grown over the device well regions. The other areas are covered by a thick layer of silicon dioxide. These steps are shown in Figure C.1(c) to Figure C.1(e). Next, a photolithographic process is used to define the thin gate regions. Silicon dioxide is deposited on the device well areas (Figure C.1(f)).

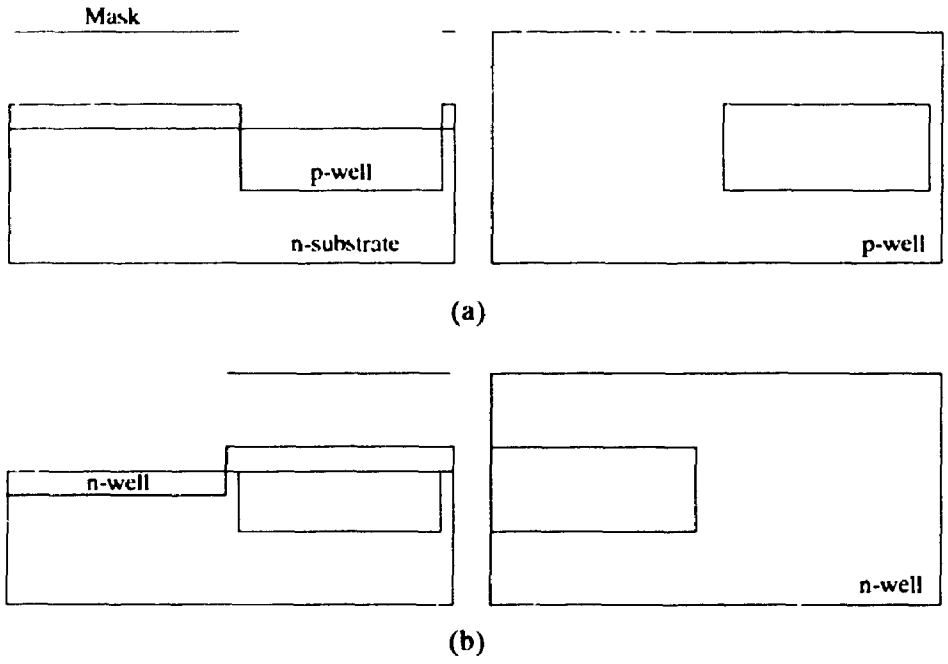


Figure C.1 CMOS Processing Steps : (a) p-well and (b) n-well masks

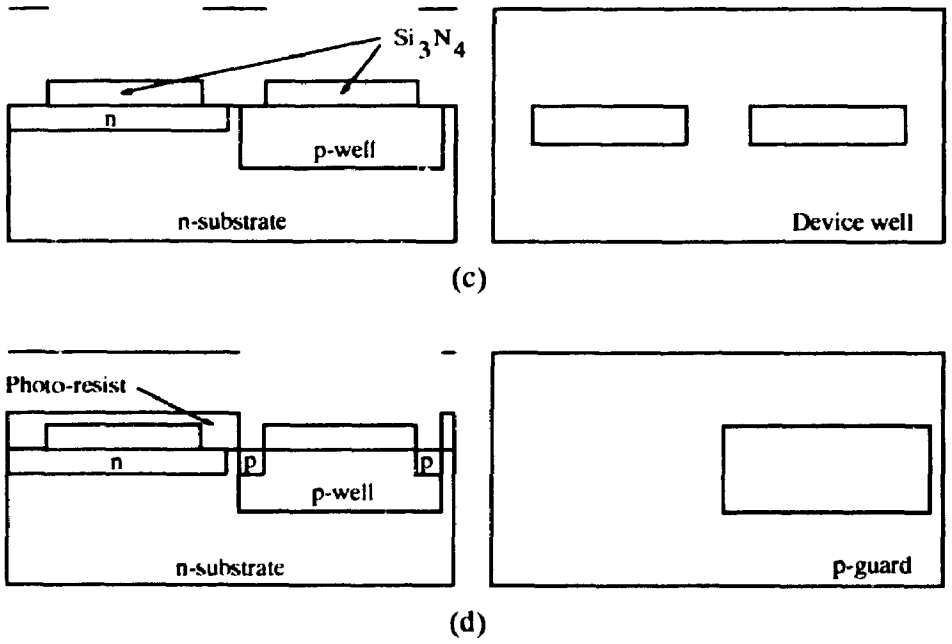


Figure C.1 CMOS Processing Steps : (c) Device well and (d) p masks

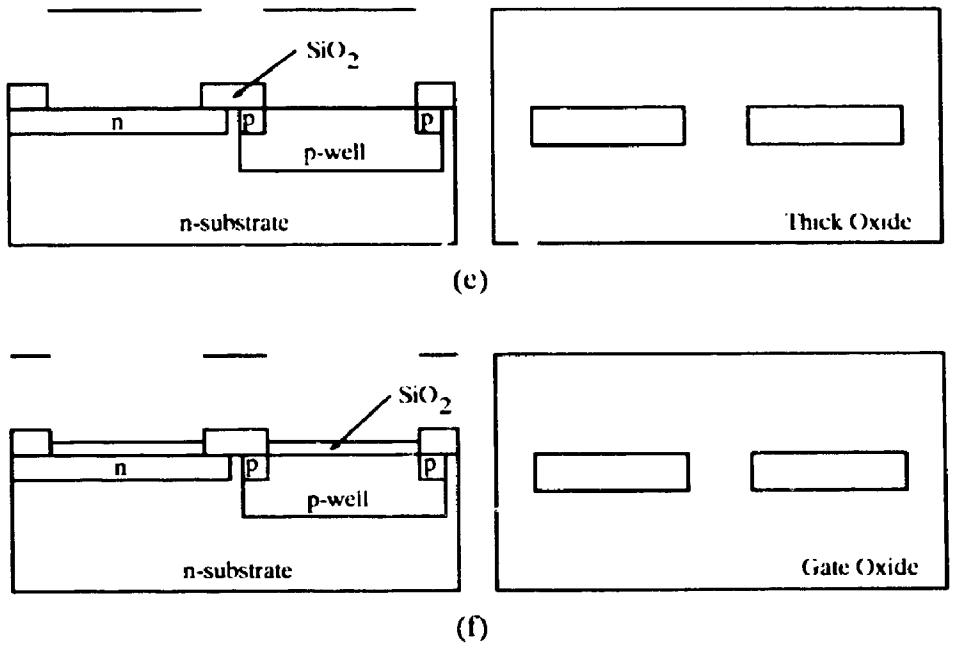
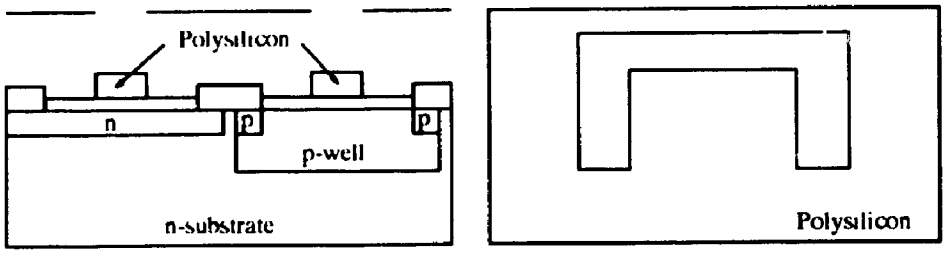


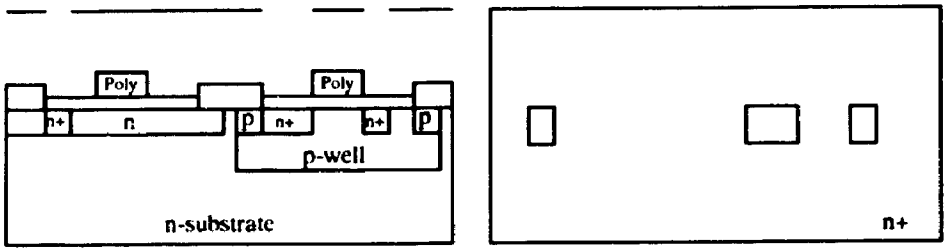
Figure C.1 CMOS Processing Steps : (e) Thick oxide and (f) thin oxide masks

A n+ mask is then used to define the n+ regions in the thin oxide. If the n+ implant is in the p-well, a n channel transistor is constructed. If the n+ implant is in the n-well, an ohmic contact is formed. Similarly, a p+ mask is used to define p+ doping in the thin oxide. A p channel transistor is formed if p+ implant is in the n-well while an ohmic contact is formed if the p+ implant is in the p-well. These are shown in Figures C.1(g) and Figure C.1(h) respectively.

Before aluminum is deposited to form the metallization lines, contact cuts are constructed by etching any silicon dioxide down to the diffusion or polysilicon regions. These allow the connections between diffusion or polysilicon regions to the metal lines (Figure C.1(i) and C.1(j)) to be made.

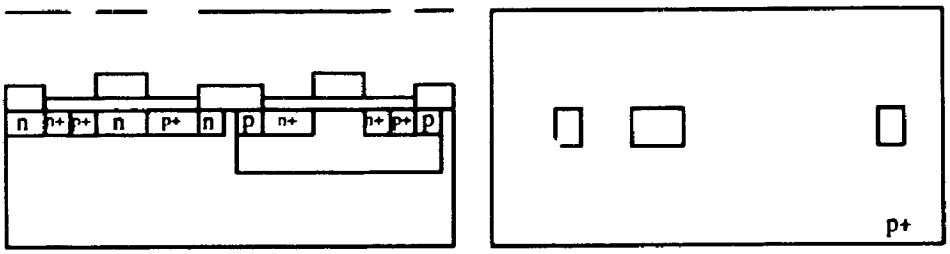


(g)

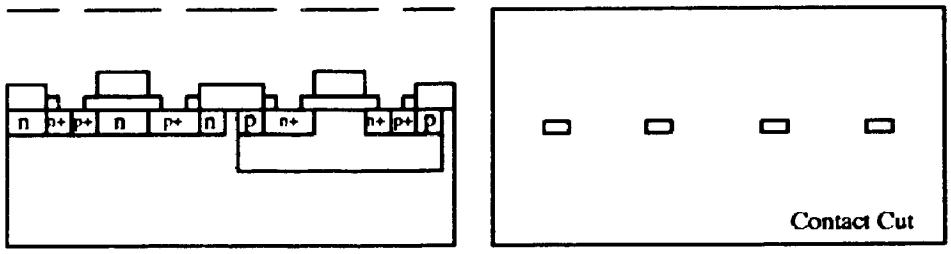


(h)

Figure C.1 CMOS Processing Steps : (g) Polysilicon and (h) n+ masks



(i)



(j)

Figure C.1 CMOS Processing Steps : (i) p+ and (j) contact cut masks

A second layer of silicon dioxide is then deposited over the entire surface and selected areas are etched out to form the vias. Another layer of aluminum is then applied to the surface to define the upper metallization lines (Figure C.1(k) and C.1(l)). In this particular technology, all bonding pads must be made with metal2.

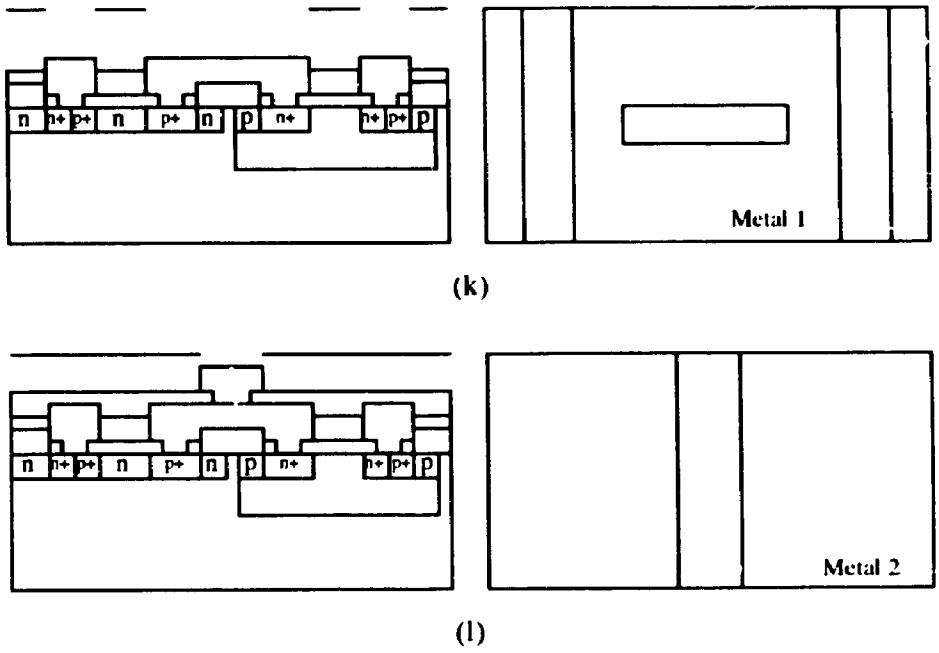
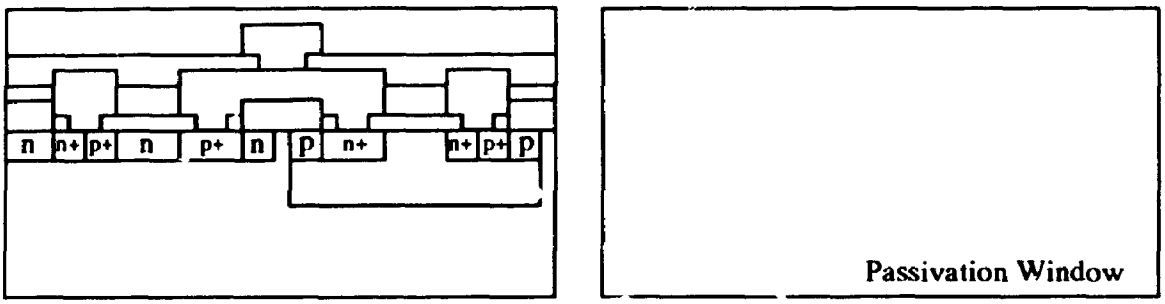


Figure C.1 CMOS Processing Steps : (k) Metal 1 and (l) metal 2 masks

Finally, a passivation layer, as shown in Figure C.1(m), is deposited over the entire wafer except the bonding pads area. This layer is used to protect the silicon surface against the ingress of contaminants.

The abbreviations and associated colours for the various CMOS layer used in this project are tabulated in Table C.1



(m)

Figure C.1 CMOS Processing Steps : (m) Passivation mask

Table C.1 CIF Layer Names and Colours

Layer	Meak Level	CIF Name	Colour
p-well	010	CPW	Brown
n-well (exclusion)	020	CNG	Green
Device well	030	CF	Blue
p-guard	040	CPG	Yellow
Capacitor p-doping	055	CCP	Brown
Polysilicon	060	CP	Orange
n+ doping (exclusion)	070	CNP	Red
p+ doping	080	CPP	Dotted-Blue
Contact	090	CC	Green
Metal 1	100	CM	Black
Via	110	CV	Yellow
Metal 2	120	CM2	Dotted Black
Passivation Window	130	CG	Blue

Due to the nature of semiconductor processing, layouts can never be exactly the same at the wafer level. In order to ensure that the device functions under all possible process variations, layout rules or design rules are used. Design rules specify certain geometric constraints on the layout network to the designer such that, even under the worst case misalignment and maximum edge movement of any feature, the patterns on the processed wafer will preserve the integrity of topological features of the designs. Design rules depend on the process design and equipment. The more conservative the rules are, the higher the probability the device will function. Alternately, the more aggressive the rules are, the more discretion is given to the designer to improve the circuit performance. Thus, designs rules are a compromise between yield, reliability and circuit performance. There are several approaches to define the design rules. The most popular are micron-based and lambda(λ)-based rules. In micron design rules, the minimum feature sizes and spacings for all the masks are specified in units of length (10^{-6} m). In lambda design rules, the minimum feature sizes and spacings for all the masks are based on a parameter lambda (λ). For example, the minimum spacing between two metal lines is 2λ and the minimum p-well width is 6λ.

In this project, micron-based design rules were used. The design rules for the Northern Telecom Electronics 3-micron CMOS process are specified using 5-micron scale for the minimum feature size. The designs will then be scaled down to 60% before fabrication. The following tables, Table C2 to C7, summarize the design rules used in this project.

Table C.2 Minimum Dimensions

Layer		Size
p-well	CPW	10
Device well	CF	5
Polysilicon	CP	5
n+ mask	CNP	5
p+ mask	CPP	5
Contact	CC	5
Metal 1	CM	5
Via	CV	5
Metal 2	CM2	5

Table C.3 Minimum Spacing

Layer		Spacing
n-well	CNG	5
Device well	CF	7
Polysilicon	CP	5
n+ mask	CNP	5
p+ mask	CPP	5
Contact	CC	5
Metal 1	CM	5
Via	CV	5
Metal 2	CM2	5

Table C.4 Enclosures

Layer		
Inner	Outer	Size
p-well	p-guard	5
p-guard	n-well	3
Device well	p-well	3
Gate	p-well	7
Contact	Metal 1	2
Contact	Device well	2
Contact	Polysilicon	2
Device well	p+ mask	4
Device well	n+ mask	4
p+ mask	n+ mask	0
Via	Metal 1	3
Via	Metal 2	3

Table C.5 Minimum Separations

Layer		Separation
p-well	p+ diff	14
p-well	n+ diff	9
p+ diff	n+ diff	8
Poly	Device well	4
Poly	p+/n+	5
p+/n+	Field	5
Contact	Gate	5
Via	Device well	5
Via	Poly	5
p-guard	p+ diff	9
p-guard	n+ diff	4

Table C.6 Overlaps

Layer		
Inner	Outer	Overlap
Poly	Device well	5
Contact	p+ mask	6
Contact	n+ mask	6

Table C.7 Pad Rules

Minimum size bonding pad glass opening	190
Metal 2 over glass enclosure	10
Minimum bonding pad to pad metal 2 spacing	125
Minimum bonding pad to unconnected circuitry separation	67
Recommendation minimum size probe pad glass opening	35
Recommendation centre to centre spacing of probe to be probed simultaneously	215
Minimum metal 2 width connection to bonding pad	100
Minimum metal 2 to bonding pad corner separation	34
Minimum metal 1 to glass opening separation	44

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