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Multichannel Radiofrequency Lock-in Detection For Coherent Processing Of Optical Signals

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MULTICHANNEL RADIO FREQUENCY LOCK-IN DETECTION FOR COHERENT PROCESSING OF OPTICAL SIGNALS

by

Gregory Wilson

Faculty of Engineering Science

Submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy

Faculty of Graduate Studies
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Abstract

The thesis deals with the extraction of weak radio frequency signals buried in noise by the technique of multichannel spectral analysis based on radio frequency lock-in detection. The technique and the developed instrument find extensive use in the fields of radio astronomy, remote sensing, and spectroscopy.

Radio frequency spectral resolution over a reception range of 0 - 512 MHz was achieved with a multichannel spectrum analyzer consisting of a radio-frequency pre-processor and a set of 64 parallel lock-in receivers. The reception range is divided uniformly into 64 evenly spaced channels of 8 MHz bandwidth. The pre-processor consists of wideband low noise amplifiers, wideband filters, RF mixing, and power splitting, providing preconditioning of the RF input signal for lock-in detection by the channel receivers. Each of the channel receivers are superheterodyne receivers and consist of a capacitively tapped strip transmission line filter, a thermally compensated square-law detector, and a synchronous detector. A software controlled electronic scanner sweeps the outputs of the receivers for data acquisition to take place. System control was facilitated through a user programmable microcomputer which performs data acquisition, data preprocessing, graphic display, and tape storage.

The technique for resolving weak radio frequency signals has been improved by the application of the concepts of parallel processing, modularity, and symmetry.

The concepts of parallel processing as applied to RF processing of weak signals were successfully employed in the multichannel spectrum analyzer. The resulting system is characterized by reduced hardware complexity, low-noise electronic circuitry, and improved reliability. The concepts of modularity and symmetry proved advantageous in reducing design and hardware development time.

The channel receiver is a novel design based on the principles of superheterodyne reception incorporating improved detection stages. A dual square-law detection scheme for thermal compensation significantly reduced the problem of thermal drift. The gated synchronous detector scheme eliminated contaminating noise that was asynchronous with the chopping signal and also chopper transition noise.

The minimum detectable power across all channels was measured to be -138 dBm $\pm$1 dB. In addition, across all channels, a noise figure of 3.05 $\pm$ 0.3 dB and a receiver noise temperature of 306 $\pm$ 43 K was measured. Through software control, the system can perform auto-calibration, address any combination of receivers, perform preprocessing of data for graphical display, and perform digital integration for extended periods of time.

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Glossary of Symbols and Abbreviations

Term	Description
ACIA	asynchronous communications interface adapter
ADC	analog-to-digital convertor (conversion)
AM	amplitude modulation
ASCII	American Standard Code for Information Interchange
B	bandwidth
B_i	input bandwidth
B_o	output bandwidth
B_{HF}	predetection bandwidth
BIFET	bipolar and FET technology
BPF	band-pass filter
BW	bandwidth
BWO	backward-wave oscillator
C	capacitor, Linvill stability factor
C_j	diode junction capacitance
CMOS	complementary MOS
CPU	central processing unit
dBm	logarithmic power units referenced to 1 mW
DAS	data acquisition system
DC	direct current
e_r	relative permittivity
EMI	electromagnetic interference
EPROM	electrically programmable ROM
f_c	centre frequency, cutoff frequency
f_T	unit gain-bandwidth product

F	noise figure
F_n	nth amplifier noise figure
F(S)	transfer function of PLL filter
FB	filter bank
FM	frequency modulation
G_n	nth amplifier gain
GPIB	general purpose instrument bus
H(S)	transfer function of PLL
HP	Hewlett-Packard
HPF	high-pass filter
I_n	diode RMS noise current
I_s	induced shield current, diode reverse saturation current
IEEE	Institute of Electrical and Electronic Engineers
IF	intermediate frequency
I/O	input/output
k	transformer coupling coefficient
K	Boltzmann's constant
K_d	phase detector gain
K_o	VCO gain factor
L	inductance
L_p	transformer primary inductance
L_s	transformer secondary inductance
LNA	low noise amplifier
LO	local oscillator
LPF	low-pass filter
m	modulation index

M	mutual inductance
MCSA	multichannel spectrum analyzer
MI	module interface
MOS	metal oxide semiconductor
MPU	microprocessor unit
n_g	generator noise power
n_i	diode noise power
n_r	receiver noise power
OHR	optical heterodyne receiver
OHS	optical heterodyne spectrometer
P_{min}	minimum detectable power
PA	port A of PIA
PB	port B of PIA
PCB	printed circuit board
PIA	peripheral interface adapter
PIN	p-intrinsic-n semiconductor
PLL	phase-locked loop
PS	power splitter
PTM	programmable timer module
PWM	pulse width modulation
q	electron charge
Q	quality factor
R_j	diode junction resistance
R_p	transformer primary resistance
R_s	shield resistance, transformer secondary resistance
RAM	random access memory

RC	resistor-capacitor
RF	radio frequency
RMS	root-mean-square
ROM	read-only memory
RTC	real-time-clock
SAW	surface acoustic wave
SETI	Search for Extra-Terrestrial Intelligence
SH	sample-and-hold
SNR	signal-to-noise ratio
SNR_i	input SNR
SNR_o	output SNR
STD	microcomputer bus type
STL	strip transmission line
SYN DET	synchronous detector
t_{LF}	postdetection integration time
T	absolute temperature (Kelvin)
T_a	antenna temperature
T_c	comparison load noise temperature
T_g	generator noise temperature
T_{min}	minimum detectable temperature
T_o	ambient temperature
T_r	receiver noise temperature
T_{sys}	system noise temperature
TSS	tangential sensitivity
TTL	transistor-transistor logic
μ_r	relative permeability
UHF	ultra high frequency

V_d	diode voltage
V_n	noise voltage
V_p	carrier amplitude
V_{pp}	voltage measured peak-to-peak
V_s	induced shield voltage
VCO	voltage controlled oscillator
VIA	versatile interface adapter
VSWR	voltage standing wave ratio
w_c	carrier frequency
w_n	natural frequency
w_s	modulation frequency
θ_i	PLL input phase
θ_o	PLL output phase
ζ	damping factor

Chapter 1

Reception of Spectrally Resolved Signals

1.1 Introduction

The radio frequency multichannel spectrum analyzer (MCSA) has many applications where signal reception is limited by noise. The more notable fields of application are spectroscopy, astronomy, and remote sensing.

The MCSA has an important role in the spectral resolution of optical signals in the field of high sensitivity laser spectroscopy. The laser is a coherent source that makes it ideal as an optical local oscillator for the heterodyning of optical signals. In its simplest form, an optical heterodyne receiver (OHR) consists of a laser local oscillator, a beamsplitter to mix the measured optical signal and local oscillator laser beams, and a fast photodetector. An optical heterodyne spectrometer (OHS) consists of an optical heterodyne receiver followed by radio frequency (RF) processing such as the multichannel spectrum analyzer (see figure 1.1).

Laser heterodyne spectroscopy is well suited for the study of absorption and emission lines because of its high resolution. This high resolution is limited by the uncertainty in laser frequency which, for a high quality stable gas laser, can be confined to a bandwidth of 10 kHz (Siegman, 1971). The first optical laser heterodyne

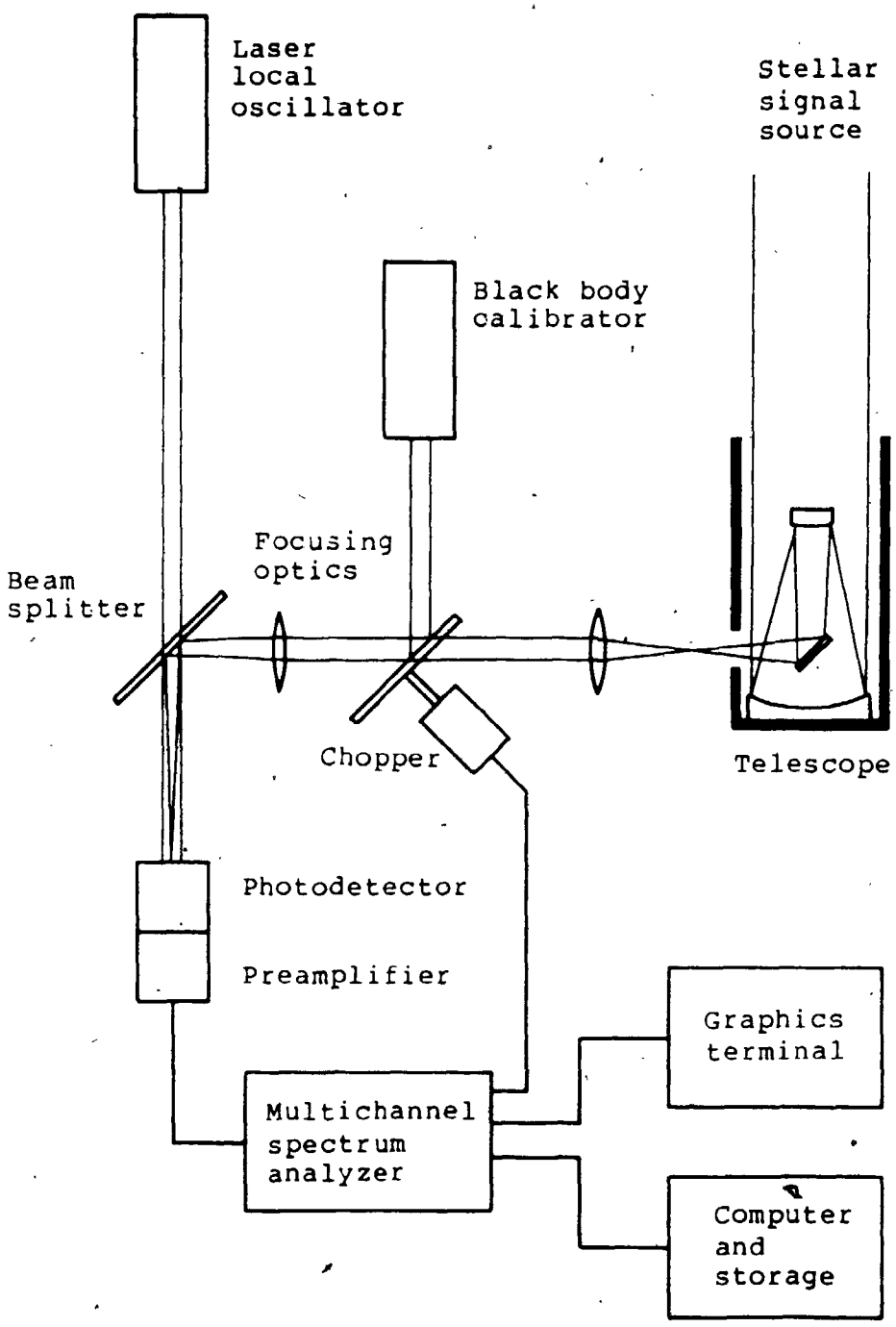


Figure 1.1 An optical heterodyne spectrometer.

detection experiments were performed by Nieuwenhuijzen (1970) on a number of bright stars and the planet Jupiter. The spectrometer consisted of a He-Ne laser, photodiode detector, wideband RF amplifier (200 MHz), and a lock-in amplifier.

Infrared heterodyne spectroscopy of carbon dioxide on Mars has been performed with a multichannel spectrometer at Kitt Peak National Observatory (Betz, 1975). The results proved the practicality and usefulness of infrared heterodyne techniques in astronomy. A spectral resolution of several orders of magnitude better than conventional methods was obtained.

The spectrometer employed a carbon dioxide laser as a local oscillator and a cooled (77 K) HgCdTe detector to produce an IF band from 0 to 1500 MHz. The IF band was spectrally resolved by a multichannel spectrum analyzer consisting of 40 x 5 MHz bandpass filters with a reception range of 50 - 250 MHz. Direct RF detection, synchronous detection, and multiplexing was performed on each of the channels.

The first tunable 8.5 μm infrared heterodyne spectrometer was constructed using tunable diode lasers (PbSe) for the study of black body emission from the Moon and Mars. The spectrometer had a reception range of 200 MHz covered by a bank of 8 x 25 MHz filters (Mumma, 1975). The RF signal from each channel was directly detected, synchronously detected, and then multiplexed for

data acquisition.

Infrared heterodyne spectroscopy is well suited to atmospheric studies because of its high detection sensitivity and high spectral resolution. The carbon dioxide laser heterodyne spectrometer at the Goddard Space Flight Centre and a tunable diode laser heterodyne spectrometer were utilized to make atmospheric absorption measurements based on solar observations of absorption lines of CO_2 and O_3 in the 10 μm band (Abbas, 1979).

The spectrometer consisted of 40 x 5 MHz, 23 x 50 MHz, and 1 x 1000 MHz bandpass filters. The outputs of the filters were processed by direct RF detection, synchronous detection, and multiplexing.

Infrared heterodyne spectroscopy of ammonia and ethylene in stars has been carried out with a multichannel analyzer consisting of 128 x 20 MHz filter banks (Betz, 1981). Initial observations were successful and present work is directed toward synthesizing laser local oscillator frequencies to higher accuracy.

A multichannel spectrum analyzer consisting of 2^{20} channels is presently being built by the NASA-Ames Research Centre for the SETI project (Search for Extra-Terrestrial Intelligence). Its high sensitivity is achieved through the use of large existing antennas, integrating for long periods of time, and using low temperature systems. High resolution is achieved by the examination of the channels with narrow bandwidths of 4 Hz

or less (Billingham et al, 1978).

An optical heterodyne receiver provides greater sensitivity than conventional direct detection schemes. The regions where these receivers are most useful are in the 3-5 μm and 8-14 μm regions where atmospheric windows exist.

In many cases, the output signal from a photodiode, produced by the detection of an optical signal, is very noisy. This noisy signal has a signal-to-noise ratio (SNR) much less than the capability of a direct detection scheme. The SNR can be greatly improved by periodically interrupting the optical signal, producing a modulated or chopped optical signal for coherent processing (Meade, 1983).

The high sensitivity processing of optical signals is made possible by the use of coherent detectors. These are phase-sensitive detectors that measure difference voltages by using a synchronous reference voltage derived from the input modulator or chopper. Phase-sensitive detection provides amplitude as well as phase information in the presence of noise and interference. Phase-sensitive detectors that are phase-locked to the modulation or chopper frequency with no phase offset are synchronous detectors (Meade, 1983).

The preservation of amplitude and phase information makes heterodyne detection systems suitable for interferometry. Long baseline interferometers have been

used to study fringe signals from the planet Mercury in the 10 μm region (Johnson, 1974).

Coherent processing systems operating on the phase-sensitive detector principle are known as lock-in detection systems and the equipment is known as lock-in amplifiers (Meade, 1983).

Previously mentioned heterodyne spectrometers are limited in their RF processing capabilities by the characteristic behaviour of each of the RF bandpass filters. Since all filters are different, the process of alignment and balancing, with respect to other filters, places a practical limit to the number of filters in the multichannel spectrum analyzers.

The electronic techniques of superheterodyne receiving were not employed in these spectrometers. This is an important technique that is widely used in common radio receivers. Superheterodyne reception is the process of multiplying two frequencies together (RF signal and RF local oscillator) and making use of the resulting difference frequency as the intermediate frequency (IF) band.

The benefits of superheterodyne reception are that most of the amplification and filtering takes place in the IF band rather than in the RF band. Amplification at a fixed narrow frequency band is much easier to accomplish than at a variable, wider frequency band. In addition, the local oscillator may be changed to receive a different

RF band without altering the superheterodyne receiver. IF filtering for a given bandpass response is easier to obtain and keep consistent across many receivers.

This thesis describes a multichannel lock-in detection system developed for the coherent processing of optical signals. A radio frequency multichannel spectrum analyzer has been designed, built and tested for detection of weak signals buried in predominantly white noise. Sixty-four channel filters and receivers covering a range of 0 - 512 MHz are employed to extract the signal from noise. The signal is alternately switched or chopped with a noise reference and synchronously detected by the receivers.

The system consists of four parts: a radio frequency (RF) section, a detector section, a digital electronic section, and a microcomputer section.

The RF section consists of wideband low noise amplifiers, high-pass filters and low-pass filters in the front-end module. Following this, there are filter banks containing a total of 64 channel filters of equal bandwidth (8 MHz) uniformly spaced across the reception range of 0 - 512 MHz. Each of the 64 channels has a superheterodyne receiver incorporating square-law detection for optimum sensitivity.

The detector section consists of 64 synchronous detection or coherent detection circuits following the

superheterodyne receivers. These maximize the sensitivity of the multichannel spectrum analyzer (MCSA) by significantly reducing all noise, including system noise, that is asynchronous with the chopped input signal.

The digital electronics supplies all the necessary control signals for synchronous detection, analog-to-digital conversion, and data collection.

The microcomputer with its operating system provides user and external computer interfacing with the analyzer. In addition, some data processing and manipulation is possible, such as extended integration times and graphic displays of system spectral response. The data, once collected by the microcomputer, is transferred to a minicomputer for further analysis and storage.

The radio frequency multichannel spectrum analyzer (MCSA) was designed and built with state-of-the-art technology. Very low noise, wideband, gallium arsenide (GaAs) preamplifiers were used as the first stage of amplification on the front-end module of the MCSA for improved noise figure characteristics. Wideband, linear, double-balanced mixers were employed in the front-end module and throughout the system to minimize intermodulation distortion. Tapped strip transmission line structures were used as high quality (Q) channel filters and power splitters. The concepts of lock-in detection were applied to detection at radio frequencies. Two stages of detection, square-law detection and

synchronous detection, were employed for optimum sensitivity. A dual square-law detection scheme was used to maximize the sensitivity of the RF superheterodyne receivers. Each receiver output is synchronously detected to improve the signal-to-noise ratio. It also includes Dicke chopper edge cancellation to eliminate spurious responses due to edge effects.

The data acquisition system containing a high speed, 12-bit analog-to-digital converter can perform a system sweep and conversion of all the receiver outputs (128 for both signal and reference outputs) in 3.1 ms. As with all of the system, the scanning is under control of a microcomputer which also handles data transfer to a graphics terminal and to a minicomputer. The entire system was designed to be controlled by a microcomputer. In this way, the system can be easily reconfigured and optimized for a given application by changing the controlling software.

The multichannel spectrum analyzer is essentially a multichannel lock-in amplifier system. Sixty-four channels divide the reception range uniformly and perform coherent detection in each channel. The channel receivers are lock-in amplifiers that coherently or synchronously detect the chopped RF input signal.

The multichannel spectrum analyzer differs markedly from other spectrum receiver designs. The MCSA uses multiple channels of a fixed bandwidth and at a fixed

frequency spaced uniformly across the frequency range of interest. Most other spectrum receiver designs employ a single channel that is swept through the desired frequency range.

The MCSA system is essentially a parallel processing system in the time domain, since each of the multiple channels is continuously receiving signals. The swept spectrum receiver systems are essentially serial processing systems since an event that occurs on the input will only be recorded when it is synchronous in time with the sweeping channel.

This thesis is organized into eight chapters which are briefly described below.

Chapter two describes the multichannel spectrum analyzer and its environment. A comparison is made with more common swept spectrum analyzers. The lock-in amplifier technique and design are discussed.

Chapter three gives an overview of the entire MCSA, emphasizing the functional operation of the system. Theory supporting design decisions and characteristics of the system is presented.

Chapter four provides details of the structure of the multichannel spectrum analyzer. Each electronic component of the analyzer is described in detail with supporting diagrams and schematics.

Chapter five describes the tests and calibrations performed on the system. Tests and calibrations are shown for individual components and sections of the system. A complete system test and calibration are described and evaluated.

Chapter six describes an optical heterodyne experiment for validation and calibration of the multichannel spectrum analyzer.

Chapter seven discusses the foregoing tests, and results. In addition, recommendations regarding the project are made.

Chapter eight briefly summarizes the project and presents the conclusions.

Chapter 2

The Multichannel Spectrum Analyzer System.

2.1 The Multichannel Spectrum Analyzer

The following is a brief functional description of the multichannel spectrum analyzer (MCSA), followed by a more detailed functional description of the system with reference to figure 2.1. The application of the concepts of modularity, symmetry, and parallelism to the MCSA are described.

The multichannel spectrum analyzer system was developed for the acquisition of signals buried in noise. To optimize the recovery of the signal, synchronous detection is employed. To accommodate this detection scheme, the RF input is switched or chopped alternately with a reference source (ie. noise source). This scheme was derived from a receiver originally developed by Dicke (1946).

The RF input reception range of 0 - 512 MHz is covered by 64 channel filters and receivers. Each channel filter consists of a transmission line filter with a bandwidth of 8 MHz. These channel filters are uniformly spaced across the 512 MHz reception range. Sixty-four channel receivers are connected to the 64 channel filters and use square-law detection to recover the signal.

LNA - low noise amplifier

f_{exLO} - external local oscillator frequency

PS - power splitter

LPF - low-pass filter

HPF - high-pass filter

OSC - oscillator

FB - filter bank

IFA - intermediate frequency amplifier

DET - detetor

DA - differential amplifier

SYN DET - synchronous detector

MI - module interface

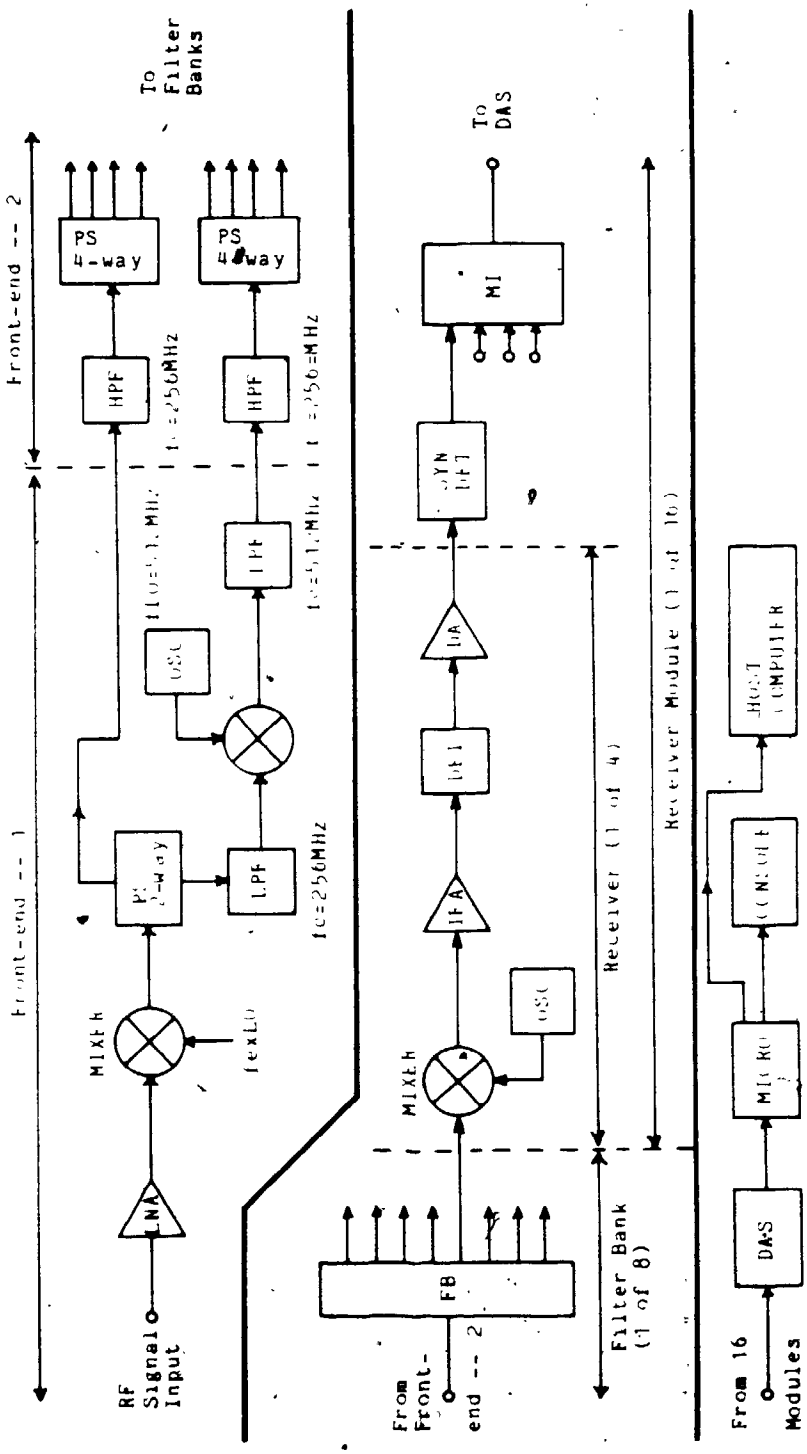
DAS - data acquisition system

f_C - centre frequency

RF - radio frequency

f_{LO} - local oscillator frequency

Legend for figure 2.1


To Filter Banks
To DAS
Front-end -- 2
Front-end -- 1
PS 4-way
HPF
LPF
MIXER
LNA
RF Signal Input
fc=256MHz
MI
DAS
FB
From Front-end -- 2
Filter Bank (1 of 8)
Receiver (1 of 4)
Receiver Module (1 of 16)
From 16 Modules

The output of each channel receiver is synchronously detected to remove any noise that is asynchronous with the chopped RF input. The output of each synchronous detector is integrated for 6 s by an analog integrator and collected by the data acquisition system. A microcomputer performs some preprocessing on the digitized data and either displays it on the console terminal or sends it to the host computer for further analysis. Details of the operation of the analyzer are shown in figure 2.1.

The multichannel spectrum analyzer (MCSA) can be divided into seven parts: first section of the front-end module, second section of the front-end module, filter banks, receiver modules, data acquisition system, microcomputer, and host computer. This partitioning is based mainly on the physical construction of the MCSA, but is also a convenient logical partitioning of the system.

The first section of the front-end module receives the RF input signal using a low-noise amplifier (LNA). The output of the LNA may be frequency shifted by a mixer and external oscillator to a convenient frequency band in the 512 MHz reception range. The signal power is split (PS) two ways with one output going to one side of the second section of the front-end module and the other output going on for further processing. The upper half of the signal spectrum (LPF, f_c = 256 MHz) is suppressed and the lower half passed. The lower half of the original spectrum is frequency shifted to the upper half by mixing

(512 MHz) and directed to the second side of the second section of the front-end module.

Section two of the front-end module consists of two identical sets of circuitry; one for the upper half and one for the lower half of the signal spectrum. Here, the signal is high-pass filtered (HPF, f_c = 256 MHz) and power split (PS) four ways. There is a total of eight outputs for each of the eight filter banks (FB).

The filter banks (FB) consist of eight channel filters. These filters are tapped transmission line structures and isolate the required frequency band for the receivers. There is a total of 64 outputs from all of the filter banks.

Four outputs from four different filter banks go to a receiver module. The receiver module consists of four receivers, four synchronous detectors, a local oscillator, and a module interface. Each receiver in a module and between modules is identical. They have an intermediate frequency (IF) of 64 MHz with a bandwidth of 8 MHz and square-law detection. The synchronous detector (SYN DET) switches in phase with the chopped RF input and recovers the signal from the multiplexed signal and reference waveform. The module interface (MI) links the receiver module with the data acquisition system and with the system controller of the microcomputer. There is a total of 16 receiver modules in the MCSA system.

The data acquisition system (DAS) collects and digitizes the 64 detected signals from all of the modules. This is done under direct control of the microcomputer.

The microcomputer (MICRO) controls the entire MCSA system by providing control signals for the synchronous detector and controlling the data acquisition system. It also performs some preprocessing for graphic displays at the console terminal. In addition, it also handles data transfer to a host computer (PDP-11/23, PDP-10).

The host computer is required for further data analysis and storage; it also facilitates software development for the microcomputer.

In the development of the MCSA, the principles of multiplicity and symmetry were employed. The channel filters are organized into filter banks, and receivers into multiples of an identical receiver module. This multiplicity allows subsystem symmetry to be employed, better alignment of modules, and negligible pick-up of spurious signals.

This multiplicity of design has a number of benefits. Subsystem design and implementation are much less time consuming and tedious, since the circuits are simply reproductions. Design problems and their solutions, encountered during development, are similar throughout all of the subsystems.

The 8 filter banks are all basically of the same construction with only minor differences to accommodate

the different resonant frequencies. All 64 receivers are identical, having the same intermediate frequency (IF), IF bandwidth, and detection scheme. The receivers only differ in the local oscillator frequency and the RF input frequency. All 64 synchronous detectors are identical. All module interfaces are identical except for wire-wrapped pins that uniquely define an address for the a receiver module and receiver.

Parallel processing as it is employed in the MCSA has a number of advantages. Continuous reception at all frequencies in the reception range of 0 - 512 MHz is a significant improvement over that of a swept spectrum analyzer since an event occurring at any time will be received and recorded. This is an important characteristic as many phenomena of scientific interest are transient in behaviour.

Parallel processing systems may, in general, involve more circuitry than a serial processing system, but there is a trade off between numerous, redundant, simple circuits and a few highly complex individual circuits. Redundancy is an important factor in improving system reliability. Failure of a channel or even a group of channels will not necessarily bring the entire system to a halt. More elaborate parallel systems may have provision to replace a failed subsystem, with one on standby, resulting in no noticeable degradation of performance. This is particularly important in aircraft, or military

systems where a system failure can be catastrophic (Hobb, 1970).

In general, parallel systems are more expensive than serial ones due mainly to the quantity of circuitry in a parallel system. In addition, some data acquisition system is usually required to record and collect the data generated continuously by all the channels.

Parallel processing systems are typically used in areas of phased array radar, sonar processing, radar processing, pattern recognition, and computer hardware and software.

The highly parallel MCSA for the SETI project, under development at the NASA-Ames Research Centre, is a system for very high spectral resolution of astronomical radio signals. A typical application of this system would be the spectral search of the 'water-hole' spectrum (1.420 - 1.667 GHz) which is bounded by the hydrogen and hydroxyl lines. The effectiveness of such a MCSA is given by the time-bandwidth product of the system, which is the ratio of the reception range to the channel bandwidth ('frequency bin'). This is simply equal to the number of bins or channels that the system is capable of analyzing simultaneously (Machol, 1979).

The resolution capability is the ability to distinguish between two signals that are close together. The sampling theorem as applied to the frequency domain requires uniform sampling by the channels at greater than

twice the frequency interval of interest (Stremler, 1979). Consequently, for the presented MCSA which has 64 channels of 8 MHz each, the spectral resolution is 16 MHz which implies a minimum separation of 16 MHz to resolve two closely placed signals. Resolution can be improved by increasing the number of samples or channels in the frequency interval. Sampling, in practice, must be greater than the theoretical minimum of twice the interval (Nyquist rate). Filters are not perfectly rectangular but have sloping transition bands which produce distortion known as aliasing (Ziemer, 1976).

Since the noise power in a channel is directly proportional to bandwidth (n = KTB), it is desirable to reduce the channel width as much as possible. However, for a filter bandwidth, B, it takes at least 1/B seconds for the filter to settle. In addition, increasing analog integration time over 10 seconds produces marginal improvement in SNR due to the problem of 1/f noise (Leger, 1976). However, digital integration is immune to this problem and can perform integration on a channel for extended periods of time.

The upper limit on the reception bandwidth is set by the computational speed of the computer and its memory size. The lower limit on the width of the bin is set by the stability of the system's components such as: local oscillators, amplifiers, power supplies, and filters.

2.2 Swept Spectrum Analyzers

A swept spectrum analyzer is basically a superheterodyne receiver where the local oscillator is swept across the frequency band of interest. The local oscillator and RF input signal are applied to a mixer and the output intermediate frequency (IF) is bandpass filtered and detected. The swept spectrum analyzer is a common laboratory instrument. In the following, its operation is described and compared to the MCSA.

Spectrum analyzers of this type are capable of very wide frequency sweeps (spectrum range), limited mostly by the the sweeping capability of the local oscillator (Adam, 1969). Using multiple frequency conversion techniques improves the total reception bandwidth, but not the spectrum width. The spectrum width can be increased by increasing the sweep range of the local oscillator. A device that has this property is the backward-wave oscillator (BWO).

A BWO differs from conventional microwave oscillators in that the output frequency of oscillation is not determined by resonant circuits, but by a frequency-selective feedback and amplification process. This device is capable of voltage-tuned bandwidths of up to 5:1. A typical BWO has a range of 2 - 4 GHz. Thus, the spectrum width for a spectrum analyzer employing this device would be 2 GHz.

Serious problems with the swept spectrum analyzer are stability in the BWO and linearity in the mixer. Phase-locked loop techniques have been employed to stabilize the sweeping system for the BWO with the result that inherent FM can be reduced to less than ±1 KHz (Adam, 1969). The linearity of mixers with respect to bandwidth and dynamics is difficult to improve. Optimal linearity can be achieved by using small bandwidths and ensuring the input RF signal is small compared to the local oscillator for minimal intermodulation distortion.

Resolution is an important characteristic of a spectrum analyzer. It is affected by the width and shape of the IF passband and by the frequency sweep rate of the local oscillator. If two frequencies are spaced closer than the passband of the IF passband filter, then only a single response will occur. If the local oscillator is swept too fast past a signal, the detector will not have time to respond completely. Resolution is also affected by linearity of the swept local oscillator. Any inherent FM in the local oscillator will be displayed since the detector cannot differentiate between the input signal and the undesired FM signal from the local oscillator.

Simplicity of the MCSA makes it more advantageous than the swept spectrum analyzer. Local oscillators are stationary and phase-locked to a single reference. This eliminates the need for complicated circuitry required to control the linearity of sweep, maintain constant

amplitude, and control FM noise.

The mixers in the MCSA are used only in the relatively narrow frequency range of the channel filters and with a stationary oscillator. Consequently, the mixer has a linear response across that range. In addition, virtually all intermodulation products are produced well away from the IF band and are heavily suppressed by the IF bandpass filter.

The resolution of the MCSA cannot be directly compared to that of a swept system since the MCSA is optimized for detection of signals buried in noise. Signals that are spaced closer than the channel bandwidth of 8 MHz will not be resolved separately. However, the detector bandwidth, after synchronous detection and integration, is the inverse of the integration time of 6 seconds or 0.17 Hz. A typical swept system has a minimum detection bandwidth of 1 kHz.

2.3 Lock-in Amplification

As mentioned in the Introduction, lock-in amplifiers are used in phase-sensitive detection systems for the measurement of amplitude and phase of periodic signals buried in noise and interference. The typical lock-in amplifier consists of a phase-sensitive detector, preamplifiers, post-detection amplifiers, and extensive reference processing (Meade, 1983). A functional description of lock-in amplification follows with emphasis placed on its application to the design of the MCSA.

Lock-in amplification is used in two main areas of experimental activity. The first area of use is in signal acquisition or recovery of modulated signals from noise. The second area of use is in precision measurement of signals where noise is not a problem. The first case is of direct interest for this thesis.

Conventional lock-in amplifiers have been optimized for use in the range of 1 kHz to 1 MHz. This is due to a large majority of applications requiring such a frequency range and electronics is readily available for this range. The techniques of lock-in amplification can be applied to any frequency, but compromises are necessary to accommodate technical problems. At radio frequencies, there are problems with amplifiers, since operational amplifiers with their characteristic high gains, high input impedance, and low output impedance, do not function

much beyond a few megahertz. In general, at high frequencies, all components of an electronic system start to deviate significantly from the ideal, thus making the required compensations more complicated.

The phase-sensitive detector, which is at the heart of the lock-in amplifier, was originally developed by Dicke (1946). This detector was developed for a receiver system known as the Dicke receiver (see section 3.5 for details). The basic lock-in amplifier consisting of a preamplifier, adjustable filter, variable gain amplifier, mixer, reference channel, and adjustable low-pass filter, is shown in figure 2.2 (Meade, 1983).

The preamplifier on the input of the lock-in amplifier is a low- noise amplifier. The first stage of amplification must have good noise characteristics rather than gain, so that noise produced in this amplifier does not bury the signal further into noise.

The adjustable filter in the signal channel limits the noise bandwidth to the vicinity of the signal frequency. This is important mainly to keep the front stage amplifiers out of saturation. This is possible in wideband situations where random noise pulses may add up and drive the amplifier into saturation, resulting in distortion and intermodulation.

In the detector section, it is essential to have an ideal multiplier. It must have a linear performance under all applied levels of signal and noise. Departure from

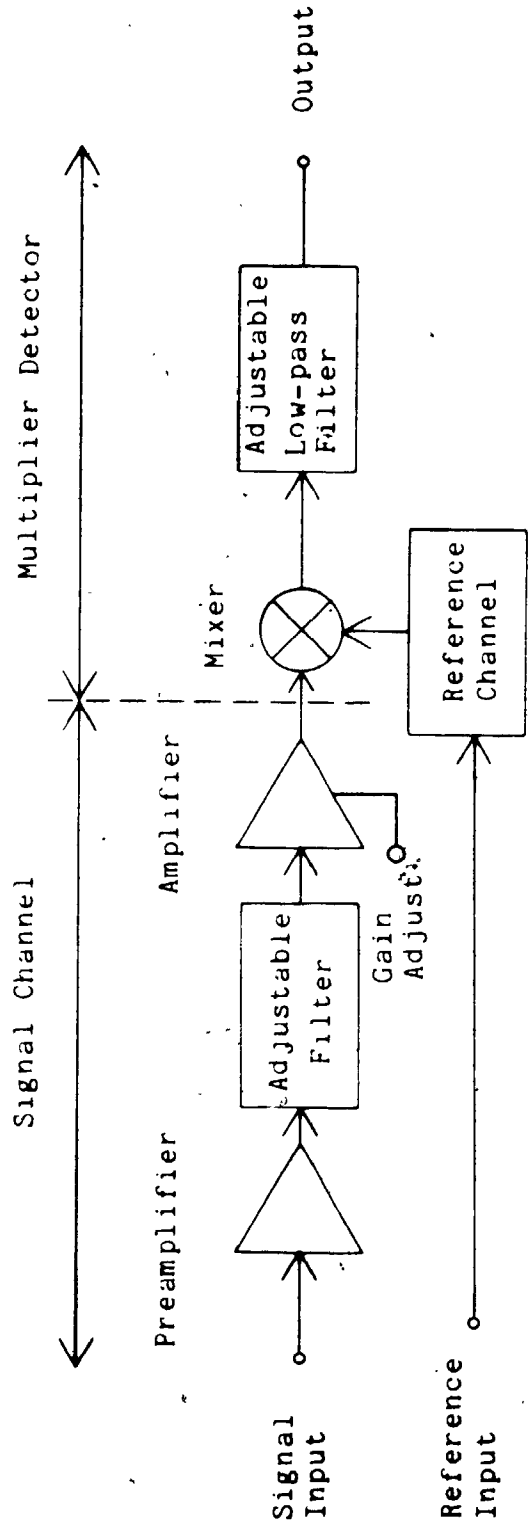


Figure 2.2 Block diagram of a lock-in amplifier.

linearity will give rise to distortion. The switching multiplier or phase-sensitive detector provides the widest linear dynamic range for signal-recovery systems (Meade, 1983). In this case, the multiplier is driven by a square-wave switching waveform that is synchronized to the applied reference waveform.

The switching waveform is derived from the reference channel and is triggered by the positive-going edge of the reference channel. A calibrated phase control can phase shift the switching waveform with respect to the reference, independent of frequency.

The adjustable low-pass filter usually has a relatively long time constant or narrow bandwidth to reduce high frequency noise. However, there must be a compromise on the bandwidth since, as it decreases, there will be greater tracking error of the output to follow a changing signal. Most low-pass filters are simple one-stage or two-stage RC filters.

Commercial lock-in amplifiers are often specified by the word 'capability'. Systems that are described as 'capable' are those that can withstand very low levels of input SNR (ie., -20 dB) while maintaining a linear response to a synchronous signal (Meade, 1983). SNR improvement in a lock-in amplifier is limited only by the minimum bandwidth of the output filter of the synchronous detector. This improvement is only realized provided that the desired signal is fixed in amplitude and phase for the

duration of the experiment and the settling time of the output filter.

The improvement factor supplied by synchronous detection is B_i/B_o where B_i is the input bandwidth and B_o is the output bandwidth. The output signal-to-noise ratio (SNR_o) is given by:

$$SNR_o = \frac{B_i}{B_o} SNR_i \qquad 2.1$$

The multichannel spectrum analyzer is essentially a multichannel lock-in system with each channel designed as a simple lock-in amplifier. The front-end, wideband, low-noise amplifiers on the MCSA are equivalent to the preamplifiers of the basic lock-in amplifier (see figure 2.1). The front-end filters and filter banks of the MCSA are equivalent to the signal channel filter of the lock-in amplifier. The synchronous detector of the MCSA is equivalent to the multiplier detector section of the lock-in amplifier. The MCSA has, in addition, a number of mixers and local oscillators, but these only provide frequency translation and do not affect the lock-in amplifier.

The MCSA, as mentioned in the previous section, has a minimum output bandwidth of 0.17 Hz. For an input signal buried in white noise within the reception bandwidth of 512 MHz, the improvement factor by equation 2.1 is 94.8 dB. For a band limited input signal of 8 MHz, the

improvement factor is 76.7 dB.

Chapter 3

Overview of the Multichannel Spectrum Analyzer

3.1 Noise, Shielding, and Ground Considerations

To realize the full potential of parallel processing in spectrum analysis, the problems of electromagnetic interference (EMI) must be considered. At frequencies above a few megahertz, electromagnetic interference (EMI) becomes a significant problem. At a few hundred megahertz, EMI problems are severe and require the same attention as the circuits being developed.

Figure 3.1 shows a simple block diagram of a heterodyne radio receiver with all the possible problems associated with improper shielding and grounding (Ott, 1976). The interface generated within a system can be divided into four parts: electric field coupling, magnetic field coupling, conductive coupling, and common impedance coupling. The wiring between various stages of a system are conductors of noise and some stages are sources of noise. The ground currents flowing from various stages flow through common impedances and produce a noise voltage on the ground bus.

Noise can be broadly defined as any undesired electrical signal present in a circuit. Nonlinearities that produce unwanted signals in a circuit are not noise but distortion products resulting from imperfectly built

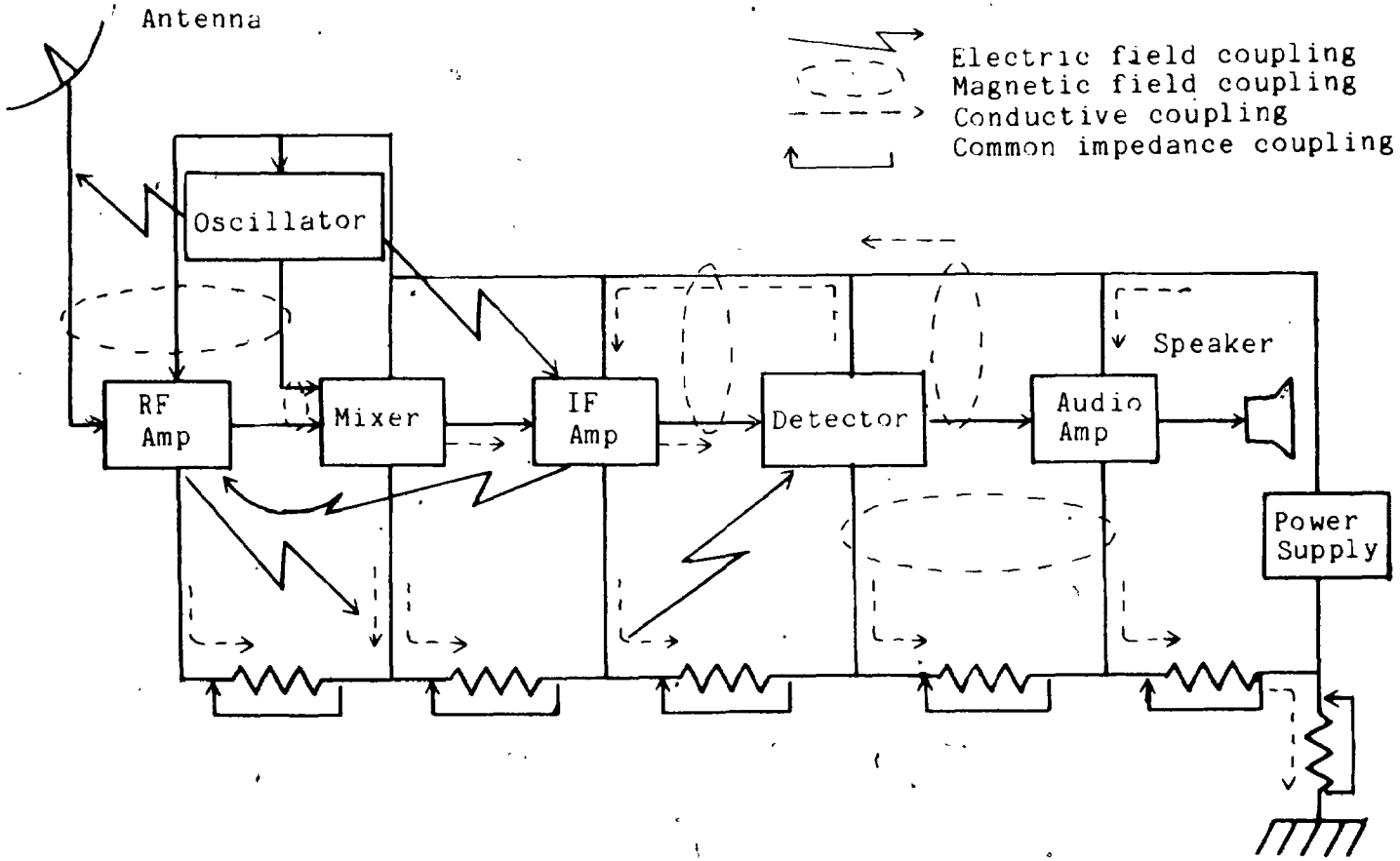


Figure 3.1 Electromagnetic interference in a common heterodyne radio receiver (Ott, 1976).

circuits. There are basically three categories of noise: intrinsic noise due to the nature of physical systems (ie.; thermal noise, shot noise); man-made noise due to motors, switches, etc.; and natural disturbances such as lightning and the signals generated by sun spots.

Electric field coupling of noise between two circuits is analogous to capacitive coupling between the circuits under consideration. Likewise, if a time varying magnetic field couples two conductors from two circuits, then this can be represented by a mutual inductance between the two.

Conductive coupling of noise into a circuit is a serious problem and can best be realized by considering the power leads of a circuit that may run through a noisy environment, pick up the noise, and conduct it into the circuit.

Noise coupling through common impedance occurs when currents from two different sources flow through a common impedance. The typical situation is when two circuits have a common ground and the two ground currents flow through the common ground impedance. The result is that one circuit sees the ground potential modulated by the ground current of the second circuit as it flows through the common ground impedance (Ott, 1979).

Noise can result from the galvanic action between dissimilar metals. Water vapour or moisture between the two metals produces a chemical wet cell. The galvanic action causes positive ions from one metal (anode) to be

transferred to the other metal (cathode) which leads to corrosion of the anode. The rate of corrosion depends on the ambient moisture content and the relative separation of the metals in the galvanic series. For example, a poor combination of metals is copper and aluminum with the result that aluminum is corroded away from the copper. Plating the copper with lead-tin solder reduces this corrosion considerably since the solder is closer to aluminum in the galvanic series (Ott, 1979).

Noise due to electrolytic action occurs when any two metals with an electrolyte (moisture) have a direct current flowing through them.

An effective way to reduce the problems of capacitive coupling is through the use of shielding to break the capacitive link between two circuits. This can best be illustrated by considering capacitive coupling between two conductors, one of which is shielded (ie., coaxial cable).

Figure 3.2 shows the equivalent circuit for a conductor capacitively coupled to a coaxial cable. The equivalent circuit accounts for extension of the centre conductor beyond the shield and termination in a finite resistance to ground. The noise voltage coupled to the centre conductor with a grounded shield is given by:

$$V_n = \frac{SRC_{12}V_1}{1+SR(C_{12}+C_{2g}+C_{2s})} \qquad 3.1$$

Minimizing C_{12} by reducing the extension beyond the shield

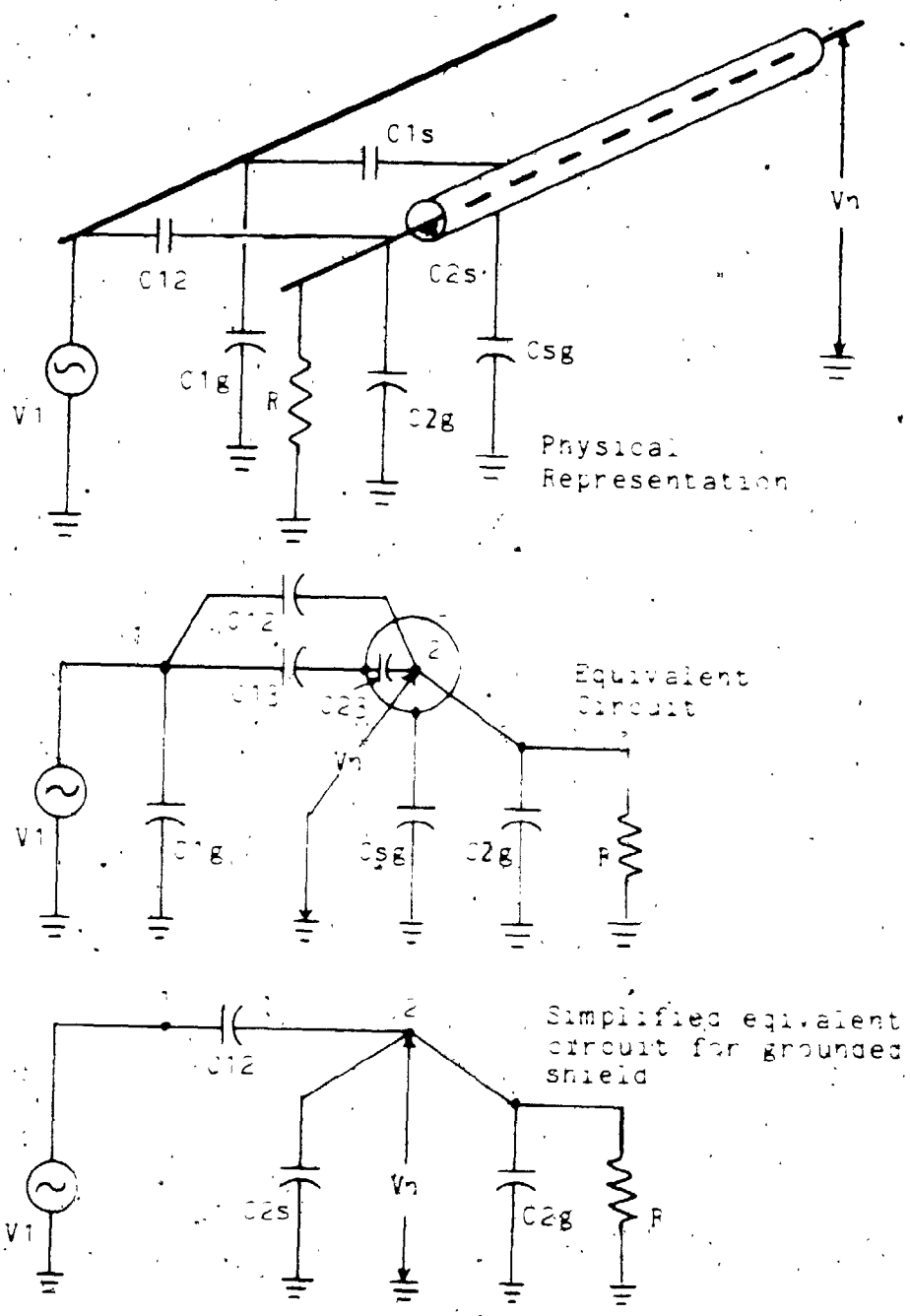


Figure 3.2 Capacitive coupling between a conductor and a shielded conductor.

and providing a good RF ground on the shield will minimize the capacitively coupled noise voltage. Multiple ground points on the shield should not be spaced further than 1/20th of a wavelength of the highest significant frequency (Ott, 1976).

Generally, some of the impedances in figure 3.2 are much smaller than others.

$$R << \frac{1}{S(C_{12}+C_{2g}+C_{2s})} \qquad 3.2a$$

then from equation 3.1

$$V_n = SRC_{12}V_1 \qquad 3.2b$$

This is the noise voltage due to the capacitance (C_{12}) between the external conductor and the exposed centre conductor of the coaxial cable. If the coaxial cable is braided, then C_{12} will also include capacitive coupling through the holes in the shield.

The problems associated with magnetic field coupling can be understood by considering a similar circuit to that considered for the capacitive coupling case. Figure 3.3 illustrates the magnetic coupling case between a conductor and a shielded coaxial cable. The basic equations for inductive coupling into a closed loop are:

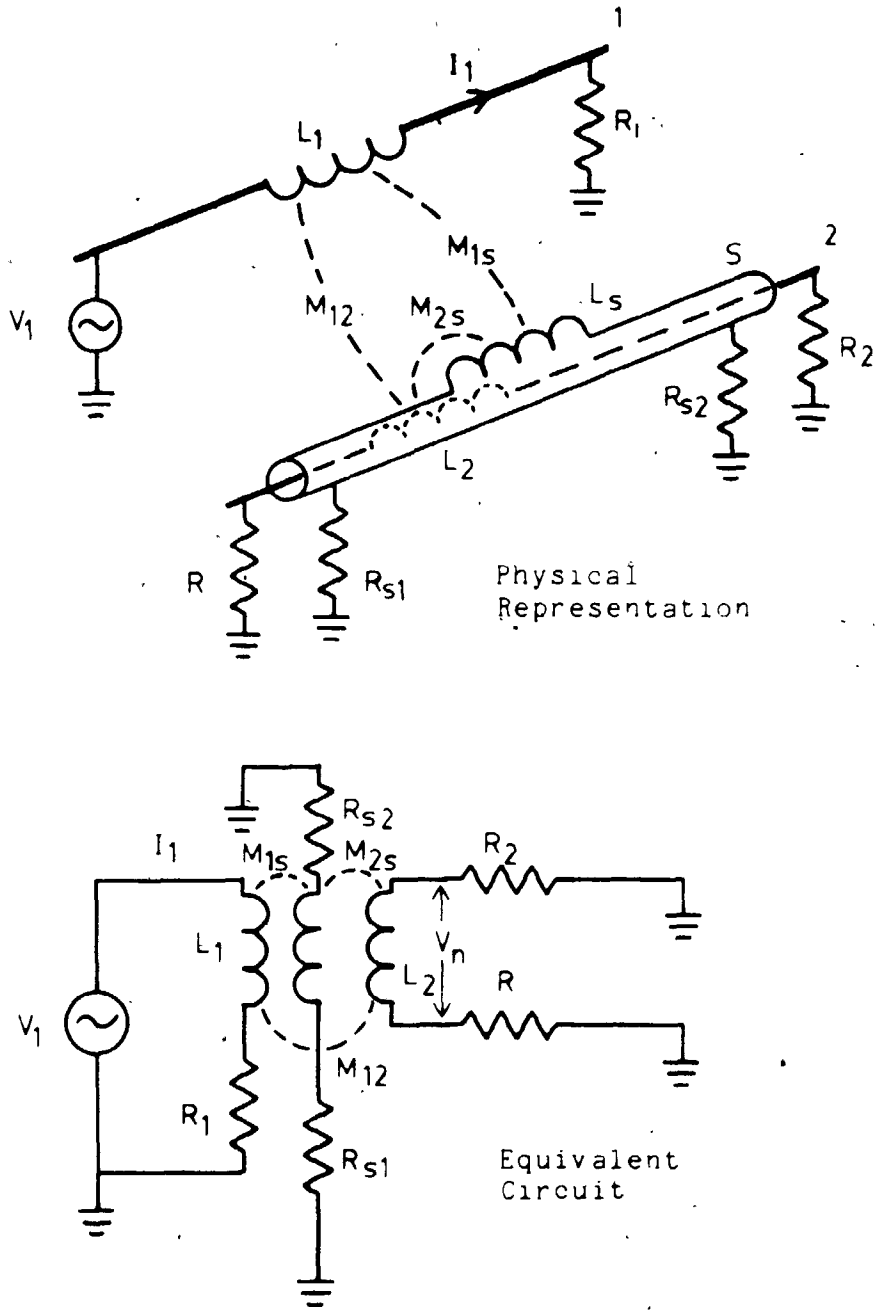


Figure 3.3 Magnetic coupling between a conductor and a shielded conductor.

$$V_n = \frac{-d}{dt}\int_A \bar{B}\cdot\bar{A}\, dA \qquad 3.3a$$

$$V_s = SBACos\theta = SMI_s \qquad 3.3b$$

where B = magnetic flux density

A = area of closed loop

V_n = induced noise voltage

V_s = induced shield noise

M = mutual inductance

I_s = induced shield current

R_s = shield resistance

Consider now the case of magnetic coupling between the shield and the inner conductor. If one assumes that the shield is a a very thin tubular conductor, then for a uniform axial current flowing in it, all of the magnetic field is external to the tube and none is internal. (Ott, 1976). Since the magnetic flux produced by the shield also links the inner conductor, the inductance of the shield equals the mutual inductance between the shield and the inner conductor (Ott, 1976).

The voltage, V_n, induced in the centre conductor by a shield current of I_s is given by:

$$V_n = SMI_s \qquad 3.4a$$

$$V_s = I_s(SL_s+R_s) \qquad 3.4b$$

$$\therefore V_n = \frac{SMV_s}{SL_s+R_s} \qquad 3.4c$$

$$\because M = L_s$$

$$\therefore V_n = \frac{SV_s}{S+R_s/L_s} \qquad 3.4d$$

The last equation implies a cutoff frequency of $f_c=R_s/(2\pi L_s)$ which is in the audio frequency band for most coaxial cables (eg., for RG-58C, f_c = 2 kHz).

The external magnetic field can be eliminated if there is a shield current equal and opposite to that flowing in the centre conductor. The fields produced by the centre conductor and the shield will cancel. Therefore, in order to successfully reduce radiation of magnetic fields from a conductor, the shield should be grounded at both ends. It should be noted that magnetic shielding at high frequencies above cutoff is not due to the magnetic shielding properties of the shield but is due to the return current on the shield generating a field that cancels the centre conductor's field (Ott, 1976).

At frequencies below cutoff, a ground plane will provide a better return path than the shield because it will have lower effective inductance than the mutual inductance between the shield and centre conductor. Below cutoff, the shield is one of the circuits conductors where any noise current in it will produce an IR drop and hence a noise voltage. For maximum noise protection at low

frequencies, the shield should not be one of the signal conductors. One end of the circuit must be isolated from ground to eliminate a ground plane return path.

Double-shielded or triaxial cables can eliminate the noise problem altogether since the noise current flows on the outer shield and the return signal current flows on the inner shield. The two currents, therefore, do not flow through a common impedance. Triaxial cables are expensive. However, ordinary coaxial cables behave like triaxial cables at frequencies above 1 MHz due to a phenomena known as skin effect. In this situation noise current flows on the outside surface of the shield and the signal current flows on the inside surface.

The proper use of grounding is one of the primary ways of reducing noise in any electronics system. The two basic objectives involved in the design of good grounding systems are: elimination of common ground impedances which will generate noise voltages if currents from other circuits pass through it; and elimination of ground loops which are susceptible to magnetic fields. Most electronic systems require three types of grounds: one for equipment enclosures (eg., chassis, racks), one for noisy high power circuits (eg., motors), and one for the signal grounds of low-level circuits.

Shields for amplifiers should always be connected to the common point of the amplifier even if it is at a different potential than ground. If it is connected to

another convenient ground then capacitive coupling (between: shield-input, shield-output, shield-common) could setup feedback conditions for oscillation. When the shield is connected to the amplifier's common point, one capacitive coupling is shorted and the feedback eliminated. Shielded cables for differential amplifiers at low frequencies should be grounded at one end only. Grounding should be at the common point of the source or the common point of the amplifier, never both.

At high frequencies where cables are more than 1/20th of a wavelength, capacitive coupling tends to complete ground loops at several points, thus making it impossible to isolate the unterminated end. For long cables, grounding may be required at least every 1/10th of a wavelength.

The shielding effectiveness of metallic sheets consists of absorption loss, reflection loss, and a correction factor to account for multiple reflections (Manassewitsch, 1976). In practice, a solid shield enclosing a circuit can provide more than 90 dB of shielding effectiveness (Ott, 1976). However, this shielding is often degraded by leakage through seams, joints, and holes.

Leakage from a seam or hole depends on the maximum linear dimension of the opening, the wave impedance, and the frequency of the source. For best shielding, the noise induced currents in the shield should be allowed to

flow undisturbed in the manner in which they were induced by the incident field. These currents will generate additional fields that will tend to cancel the original field. Thus a series of small circular holes will be much better at shielding than a large hole of the same area in the shield.

Seams may be required in some cases (eg., lids for boxes) and here, effective shielding can be maintained with the use of EMI gaskets. The gaskets ensure uniformity of current flow around the box. Lids with flanges reduce EMI as well by increasing the surface area around the lid's perimeter for better electrical contact and for capacitive coupling to the walls of the box.

Passive components located in the low-level electronic portions of a circuit can be major contributors of noise. Components such as: resistors, capacitors, diodes, and transformers have different noise characteristics and must be treated differently.

Resistors, theoretically, produce a noise power equal to KTB. However, this ignores the effect of 1/f noise or excess noise which is dependant on the construction of the resistor. Generally, the more uneven the DC current flows through the resistor, the more excess noise is generated (Motchenbacher, 1973). Composition carbon resistors usually generate the greatest noise, whereas tin oxide, metal film, and wire-wound are all lower noise devices. All resistors used in the construction of the MCSA were

low-noise carbon film resistors (Philips, CR carbon film).

In general, capacitor noise is not a problem in circuit design. A real capacitor does have loss which is a shunt leakage resistor. Tantalum electrolytic capacitors work well in low noise applications but are prone to noise generation if they are reverse biassed by a transient (Motchenbacher, 1973).

The problems associated with electromagnetic interference during the development of the multichannel spectrum analyzer were severe. Conscientious application of the above noise, shielding, and grounding considerations has resulted in a relatively noise free system.

3.2 Front-end Module

The radio frequency front-end module is the first stage of RF processing that the signal from the photodetector passes through. The front-end module consists of amplifiers, mixers, power splitters, and filters. This is shown in the block diagram of figure 3.4. The following functional description of the front-end module emphasizes the reasoning behind certain design schemes in the light of theoretical considerations and practicality.

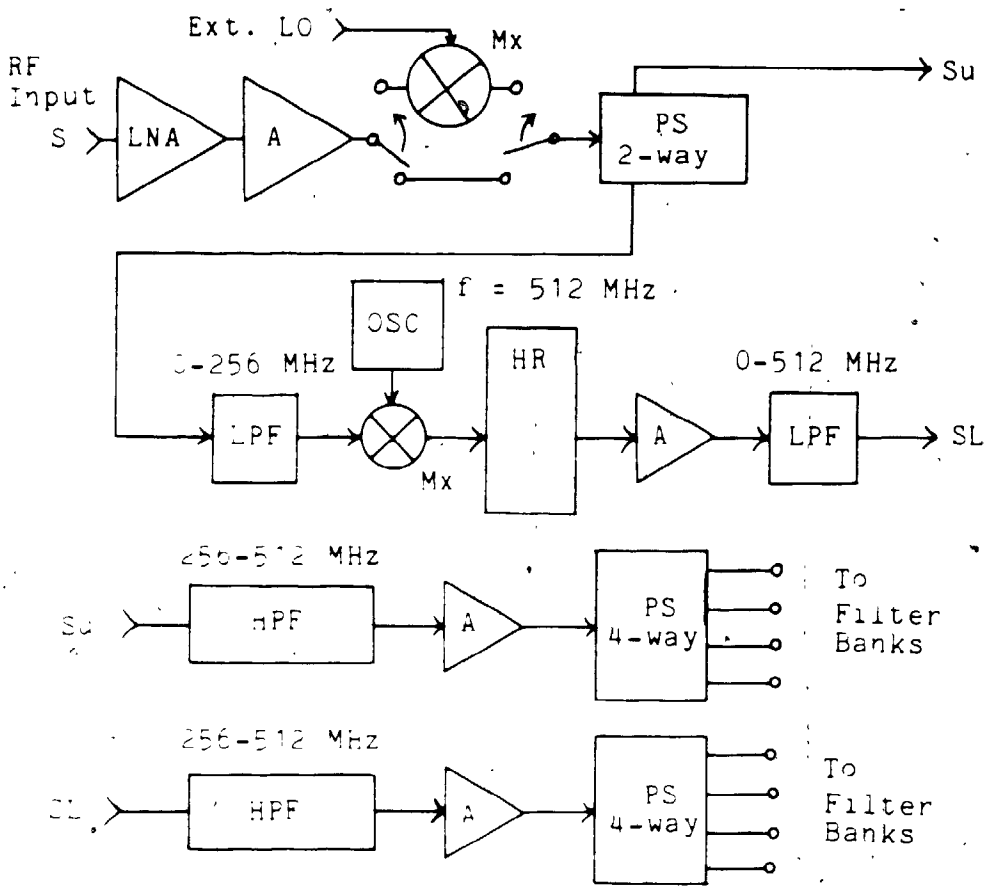
The system noise response is largely determined by the noise behaviour of the first amplifier. Friis formula for the effective noise figure of a cascade of amplifiers is given by:

$$F = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1G_2} + \ldots \qquad 3.5$$

where F_n = nth amplifier noise figure

G_n = nth amplifier gain

Consequently, low-noise, high performance preamplifiers are very important as the first component of an RF system. These amplifiers are normally purchased along with a detailed test report on their characteristics, since they are difficult to build. High quality, wideband (500 MHz), low-noise amplifiers typically have maximum noise figures



S - RF signal input (0 - 512 MHz)
Su - upper half of S (256 - 512 MHz)
Sl - lower half of S (0 - 256 MHz)
LPF - low-pass filter
HPF - high-pass filter
HR - helical resonator
A - amplifier
LNA - low noise amplifier.
OSC - local oscillator (512 MHz)
PS - power splitter
MX - mixer
Ext LO - external LO

Figure 3.4 Front-end of the MCSA.

of 2.8 - 4.0 dB (eg., Avantek: AMM-502).

Following the first low-noise amplifier, other lower quality and more economical amplifiers may be used without adversely affecting the noise performance of the system. Lower quality amplifiers typically have maximum noise figures of 6.0 - 8.0 dB and greater variability of VSWRs of the input and output.

After the input stage of amplification, there is a stage available for external mixing to shift the input RF signal into the 0 - 512 MHz reception range of the multichannel spectrum analyzer (MCSA). This may require changing the input amplifiers and mixers to microwave devices.

The next stage is a 2-way wideband power splitter where half of the signal is passed through a high-pass filter (f_c = 256 MHz) to become the upper half of the signal spectrum; the other half of the signal passes through a low-pass filter (f_c = 256 MHz) to become the lower half of the signal spectrum. Splitting the RF signal spectrum into two parts facilitates the RF processing required later in the MCSA.

The lower half of the signal spectrum is then shifted up to the same band that the upper half of the signal spectrum occupies by mixing it with 512 MHz from the front-end local oscillator. Since both halves of the signal spectrum occupy the same one octave band, RF design and implementation problems are alleviated. In the 256 -

512 MHz band, UHF and microwave electronic techniques such as tapped capacitive filters and strip transmission lines can be employed. In addition, many of the circuits required for the 64 channels become similar, requiring only minor modifications to capacitors and inductors.

The mixer (SRA-1) provides a minimum of 40 dB isolation between the LO and IF ports, but the feed-through of the local oscillator was found to be excessive. The local oscillator frequency is adjacent to the upper channels and if large enough may saturate them. The local oscillator residue on the IF output of the mixer is suppressed by an additional 30 dB by a helical resonator.

Practical helical resonators can be constructed with unloaded quality factor (Q) greater than 1000 for the VHF and UHF bands. They are similar to quarter wavelength transmission lines except their centre conductor is wound in a helix (MacAlpine, 1959). A helical resonator consists of a coil within a usually cylindrical shield with one end in good electrical contact with the shield. A trimmer capacitor may be connected between the open circuit end and the shield to adjust the effective electrical length of the helical resonator. Alternately it may be placed in shunt with the resonator to add to the effective distributed capacitance.

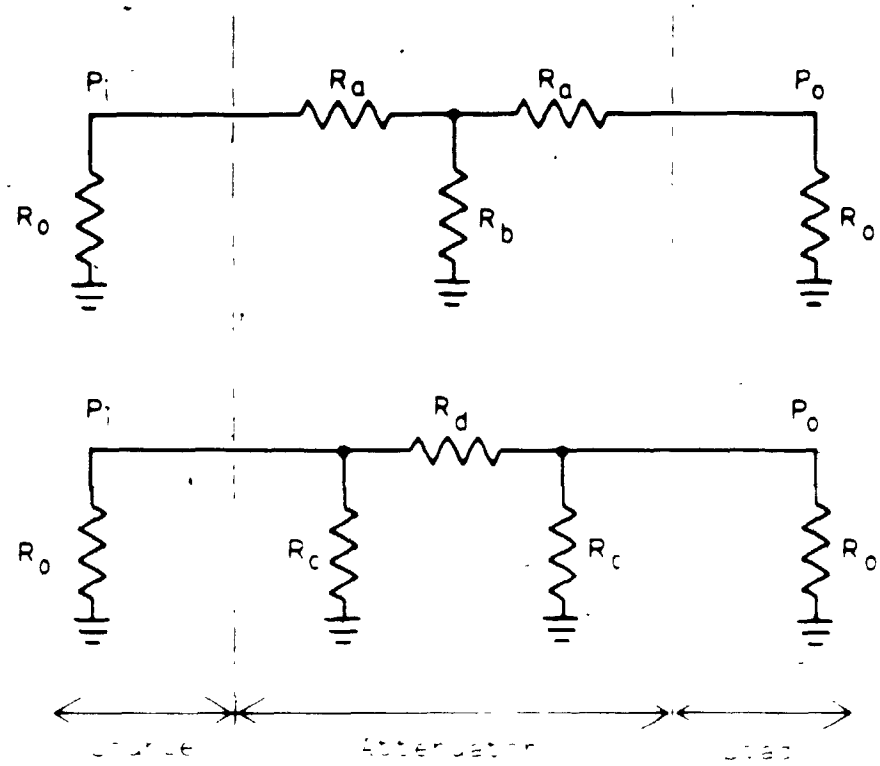
Most of the helical resonator design is based on empirical equations since the rigorous theory becomes

cumbersome in practical situations. Graphical solutions display a number of practical parameters that may be optimized (MacAlpine, 1959). Appendix D describes the design of the helical resonator used in the MCSA and also describes a transmission line approximation to the resonator.

The output of the helical resonator passes through a 3 dB attenuator before amplification. The purpose of the attenuator is to provide a wideband resistive impedance load for the helical resonator and to absorb reflections from the input of the amplifier that could ruin the high-Q response of the helical resonator. General attenuator design is shown in figure 3.5 for the characteristic impedance of R_o.

After passing through the attenuator, the signal is amplified by a wideband amplifier module. The output of the amplifier is low-pass filtered (512 MHz) to remove the band of frequencies that are the sum of the front-end local oscillator and the input signal. The low-pass filter also removes harmonics of the local oscillator of which the strongest will be at 1.024 GHz and 1.536 GHz. The receivers are not tuned to these frequencies but intermodulation distortion may produce spurious responses which could be detected by the receivers.

The output of the low-pass filter is terminated by another 3 dB attenuator providing isolation for the next stage, a high-pass filter (f_c = 256 MHz). The combination



$$K = \sqrt{\frac{P_i}{P_o}} \qquad R_a = \left(\frac{K - 1}{K + 1}\right) R_o, \qquad R_b = \left(\frac{2K}{K^2 - 1}\right) R_o$$

$$R_c = \left(\frac{K + 1}{K - 1}\right) R_o, \qquad R_d = \left(\frac{K^2 - 1}{2K}\right) R_o$$

R_o - characteristic impedance
P_i - input power
P_o - output power.

Figure 3.5 'T' and 'π' Attenuator design.

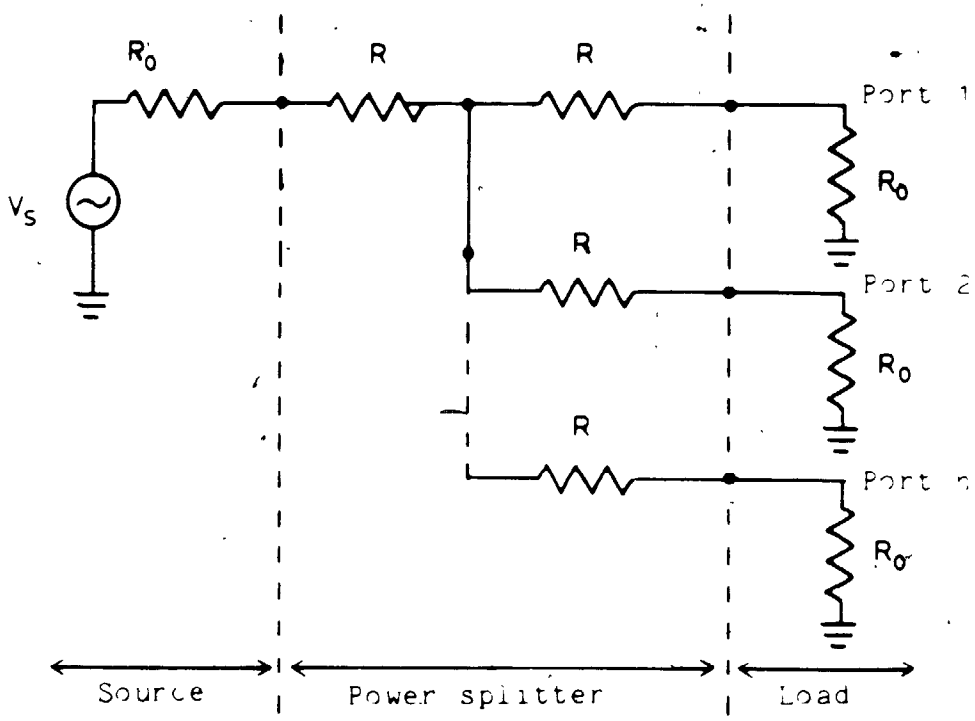
of a low-pass and a high-pass filter produces a band-pass response of 256 - 512 MHz. Two separate filters were designed rather than one band-pass filter to facilitate testing and calibration. With separate filters, the upper and lower cutoff frequencies can be adjusted independently.

The discussion so far has been concerned with the processing of the lower half of the signal spectrum. From now on the discussion will apply to both halves of the signal spectrum.

The signal passes through a high-pass filter (f_c = 256 MHz) to eliminate spurious responses that may be detected by the receivers. High quality filters generally have a sharp transition band, high attenuation in the stopband, and minimum ripple in the passband. Practical filters must compromise on these requirements. Standard tables are available that aid in the selection of a filter for a given practical situation (Christen, 1966). The high-pass filter is a 13th-order Chebyshev filter that gives a very sharp transition band, high attenuation in the stopband, and very low ripple in the passband. The Chebyshev filter is superior to the Butterworth at cutoff and in the stopband, and is in fact the optimum all-pole filter (Johnson, 1976). Data tables for high order filters are not readily available; however, the expressions for generating the tables are known (Newcomb, 1970).

The output of the high-pass filter is terminated by a wideband amplifier module which provides a nominal 50 ohms load for the filter. The amplifier boosts the signal by 10.5 dB to compensate for the 12 dB loss of the 4-way power splitter, which follows.

The 4-way resistive power splitter preserves the characteristic impedance (50 ohms) which is used in the RF electronics for the MCSA. Commercial 4-way power splitters are available (Mini-Circuits: ZFSC-4-1) with low insertion loss (0.6 dB over 6 dB split). However, they generate a greater VSWR problem than the resistive splitter. The filter banks, through which the signal passes next, are very sensitive to source impedance. They behave predictably only when loaded by 50 ohms. The general resistive power splitter design for 'n' ports is shown in figure 3.6.



$$R = \left[\frac{N-1}{N+1}\right] Ro \qquad P_{loss} = 20 \text{ Log } (n)$$

Figure 3.6 Resistive power splitter design.

3.3 Filter Bank Realization

The filter banks provide the 64 channel filters for the multichannel spectrum analyzer (MCSA). The filter banks are enclosed in eight shielded boxes or modules, each containing eight channel filters. Each of the channel filters is based on a resonant transmission line structure. The signal is tapped from a distributor transmission line by a small capacitor. These channel filters have been thoroughly explored previously (Wilson, 1981) and will be presented only briefly here.

Shielding is very important for the filter banks since eight channel filters are enclosed in the same shielding box. The nature of resonant transmission lines is such that at some points in the line there are either high currents flowing or high voltages. Accompanying these are large electric and magnetic fields.

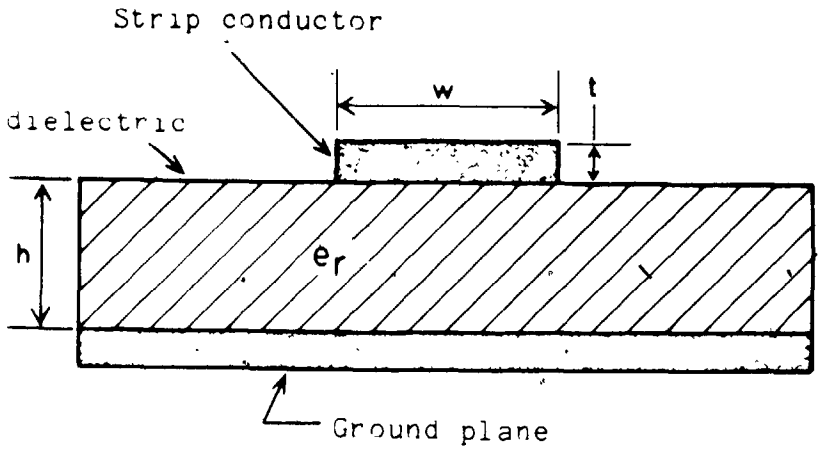
The transmission lines are printed as strips on a double-sided printed circuit board (PCB) with the opposite side being a ground plane. Consequently, electric fields tend to be well confined to the PCB and do not produce appreciable interference with adjacent channels. The electric fields reside mainly in the PCB dielectric (epoxy-fibreglass, G-10), since it has a relative permittivity, e_r, of about 4.7. The magnetic field poses a greater problem since the dielectric of the PCB has a relative permeability, μ_r, of about 1.0. The magnetic

field is much less confined than the electric field with the result that parasitic coupling to other structures is more likely.

A very accurate approximation (Blood, 1980) to the characteristic impedance of a strip transmission line (STL) is shown in figure 3.7 along with a cross-sectional view of the STL. Commonly used STLs have 50 and 100 ohm characteristic impedances which correspond to strip widths of 2.54 and 0.51 mm (0.1 and 0.02 in.) respectively for 1.59 mm (1/16 in.) double-side PCB.

The frequency assignments for the channel filter centre frequencies are derived from the reception bandwidth of 512 MHz by dividing it by number of channels (64) to give a channel bandwidth of 8 MHz. Therefore, the the upper and lower boundaries of the channel is an integral multiple of 8 MHz and the centre frequency, f_c, is given by:

$$f_c = 8n + 4, \quad \{n = 0, 1, 2, \ldots, 63\} \qquad 3.6$$



Characteristic impedance, Zo, approximation:

$$Zo = \frac{87}{\sqrt{e_r + 1.41}} \ln \left[\frac{5.98\ h}{0.8w + t} \right]$$

Figure 3.7 Strip transmission line cross-section and characteristic impedance, Zo.

3.4 Channel Receiver Operation

The channel receiver is functionally described in the following with emphasis placed on theoretical and practical considerations. The channel receiver design is the same for all 64 channels since there are no circuits dependent on the RF frequency of the signal or the local oscillator. This symmetry facilitates assembly of the receiver by eliminating the need for reproducing a new layout mask and negative for each receiver. Testing, tuning, and calibration are simplified since the receivers have similar characteristics and problems. A functional block diagram of the receiver is shown in figure 3.8.

The channel receiver accepts two sources of RF energy, one is the local oscillator and the other is the desired signal which has been chopper modulated. The chopped signal consists of RF energy from the signal source and RF energy from the reference source.

The local oscillator frequency is chosen such that the products of mixing, the sum and difference of the signal and local oscillator, yield one product centred at the IF centre frequency of 64 MHz. Table 3.1 lists the channels along with their appropriate local oscillator frequencies.

Sixteen local oscillators are sufficient for mixing the 64 channels to the IF band since the lower half of the total signal spectrum (0 - 256 MHz) is frequency shifted

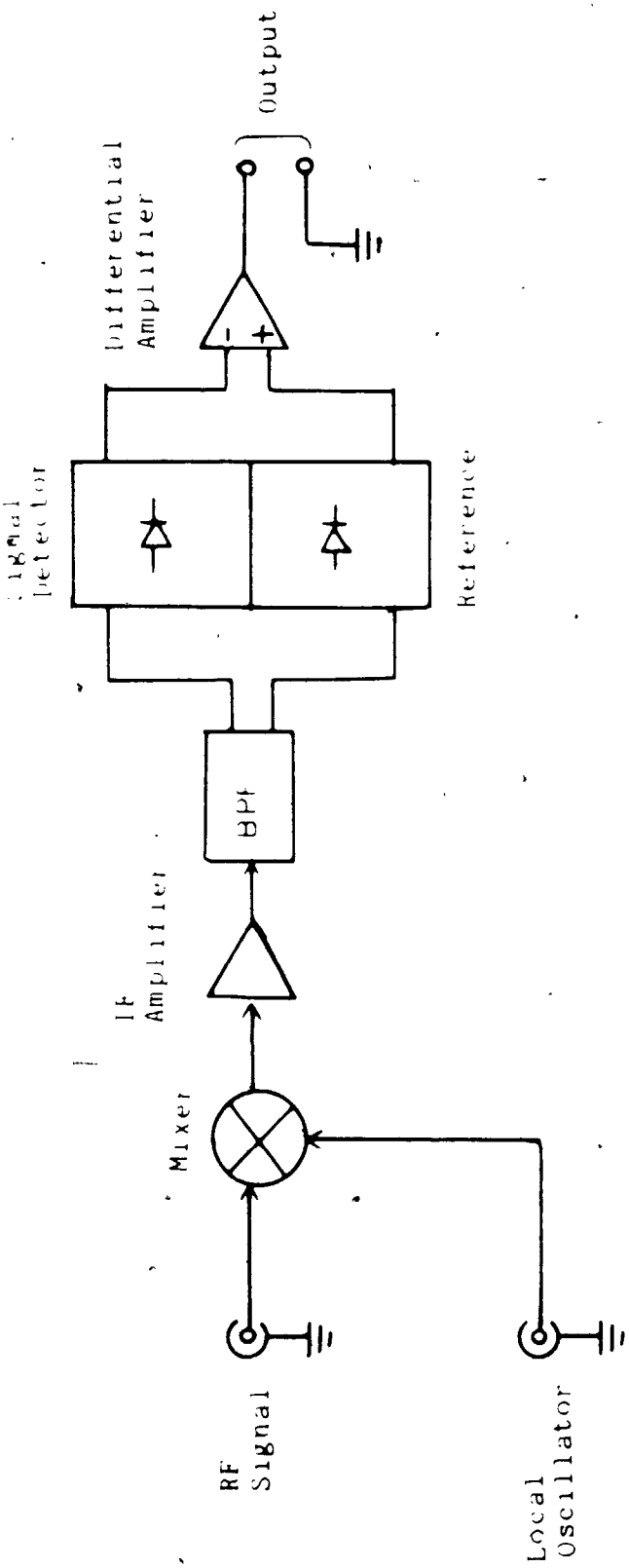


Figure 3.8 Receiver functional block diagram.

Table 3.1 Channel numbers tabulated with channel addresses, centre frequencies, and local oscillators.

Channel Number (hex)	Channel Address (hex)	Centre Frequency (MHz)	Local Oscillator (MHz)
00	3D	4	444
01	39	12	436
02	35	20	428
03	31	28	420
04	2D	36	412
05	29	44	404
06	25	52	396
07	21	60	388
08	1D	68	380
09	19	76	372
0A	15	84	364
0B	11	92	356
0C	0D	100	348
0D	09	108	340
0E	05	116	332
0F	01	124	324
10	3F	132	444
11	3B	140	436
12	37	148	428
13	33	156	420
14	2F	164	412
15	2B	172	404
16	27	180	396
17	23	188	388
18	1F	196	380
19	1B	204	372
1A	17	212	364
1B	13	220	356
1C	0F	228	348
1D	0B	236	340
1E	07	244	332
1F	03	252	324

Table 3.1 continued

Channel Number (hex)	Channel Address (hex)	Centre Frequency (MHz)	Local Oscillator (MHz)
20	02	260	324
21	06	268	332
22	0A	276	340
23	0E	284	348
24	12	292	356
25	16	300	364
26	1A	308	372
27	1E	316	380
28	22	324	388
29	26	332	396
2A	2A	340	404
2B	2E	348	412
2C	32	356	420
2D	36	364	428
2E	3A	372	436
2F	3E	380	444
30	00	388	324
31	04	396	332
32	08	404	340
33	0C	412	348
34	10	420	356
35	14	428	364
36	18	436	372
37	1C	444	380
38	20	452	388
39	24	460	396
3A	28	468	404
3B	2C	476	412
3C	30	484	420
3D	34	492	428
3E	38	500	436
3F	3C	508	444

to the upper half of the spectrum (256 - 512 MHz) by mixing it with the front-end local oscillator (512 MHz). This effectively produces two signals in the same channel frequency band. Four channels can be selected such that mixing with a single common local oscillator will produce either a sum or difference IF frequency centred at 64 MHz.

The ideal mixer has a number of qualities: square-law response, wide linear dynamic range, conversion gain, low noise figure, and high isolation between all ports. All practical mixers have certain limitations and as a result third-order intermodulation and cross-modulation distortion are present (Kraus, 1980). The double-balanced mixers used in the receiver are commercial devices (Mini-Circuits, SBL-1) and have, internally, well balanced input and output transformers, and accurately matched diode rings. A high degree of isolation (50 dB at 5 MHz, 35 dB at 500 MHz) is achieved by the internal centre tapped transformers when the LO drive is large enough to switch the diodes cleanly on and off. The two-tone, third-order intermodulation products are typically 50 to 60 dB less than the IF output (Mini-Circuits, 1979).

In general receiver designs, the IF amplifier supplies the major portion of the gain between the antenna and the detector. In the channel receiver design most of the gain is in the wideband RF amplifiers in the front-end module. It would be uneconomical to use high quality RF

amplifiers for a single channel receiver, but for the MCSA it is cost effective. Some IF amplification is required in the channel receiver to raise the desired signal above the 1/f noise level of the detector stage (DeMaw, 1982).

Since a flat amplitude response is desired in the passband, the channel receiver design is similar to an AM receiver design, as opposed to an FM receiver where a linear phase shift is desired (Kraus, 1980). The IF amplifier provides high gain to the signals in the passband and rejects other spurious responses from the mixer as well as feed-through of the local oscillator and RF signal. In general, the network at the mixer IF port should pass the IF band and reject all other frequencies (Kraus, 1980). However, this would result in reflection of higher order harmonics back to the mixer for remixing, and may generate spurious responses in the IF band or in the RF or LO ports. Wideband termination of the IF port with 50 ohms and careful shielding is the only viable alternative, and was the strategy chosen in the channel receiver design.

The interstage IF filter is a bandpass filter centred at 64 MHz with a bandwidth of 8 MHz. The filter is a single-tuned transformer with high attenuation in the stopband and good passband characteristics. This type of filter is extensively used in RF electronic designs because it provides impedance matching to the next stage, and DC isolation. In this application, the transformer

impedance matches the output of the IF amplifier to the detector diodes.

A pair of matched Schottky hot-carrier diodes (MBD102) were used in the square-law detection portion of the channel receiver. One diode is the RF detector while the other is a thermal reference for cancelling the effects of thermal offset drift. The diode detection circuitry was designed to detect low-level signals in the range -60 to -30 dBm (Watson, 1969). A good quality mixer or detector diode behaves basically like a nonlinear resistor or varistor.

The V-I characteristic of a Schottky hot-carrier detector diode is given by (Watson, 1969):

$$I = I(V_d) = I_s\left(e^{qV_d/nKT} - 1\right) \qquad 3.7$$

where I_s = diode saturation current

q = electron charge (1.6×10^{-19}C)

T = absolute temperature

K = Boltzmann's constant (1.38×10^{-23}J/K)

n = constant (~1)

V_d = diode voltage

When $V_d = V_o + \Delta V$ then the above equation can be represented by the following Taylor expansion:

$$I = I(V_o + \Delta V) = I(V_o) + \frac{dI}{dV}\Delta V + \frac{1}{2}\frac{d^2I}{dV^2}(\Delta V)^2 + \ldots \quad 3.8$$

For an amplitude modulated wave, the applied voltage is:

$$\frac{v}{V_p} = (1+m\sin(w_s t))\sin(w_c t) \quad 3.9a$$

$$\frac{v}{V_p} = \sin(w_c t) + \frac{m}{2}\cos(w_c - w_s)t - \cos(w_c + w_s)t \quad 3.9b$$

where v = modulated input voltage

V_p = carrier amplitude

m = modulation index

w_s = modulation frequency

w_c = carrier frequency

Equation 3.9b shows that the input signal contains the angular frequencies w_c, $w_c - w_s$, $w_c + w_s$ which are the same for the second term on the right side of equation 3.8. The third term on the right side produces the useful terms for a detector diode and the components are shown in table 3.2. The expression shows that the output current at the modulation frequency increases with forward bias current since d^2I/dV^2 increases (Watson, 1969).

A real diode will deviate from the above idealized analysis due to the effect of parasitic inductance and capacitance. Figure 3.9 shows the equivalent circuit for a Schottky diode. For optimum performance as a detector a

Table 3.2 Third term components of Taylor expansion of diode equation.

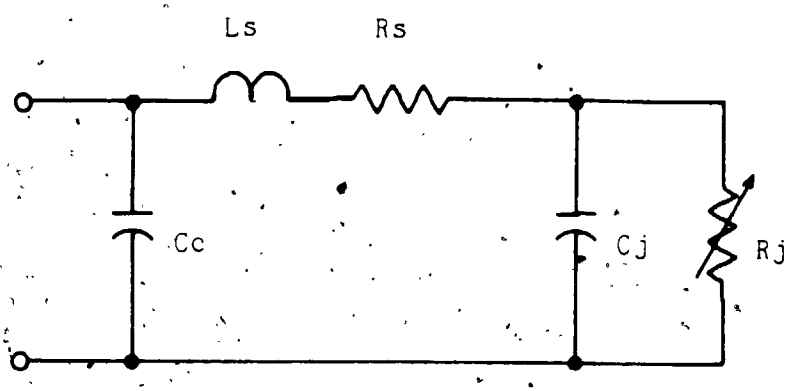
Third term: $\frac{1}{2} \frac{d^2I}{dV^2} (\Delta V)^2$

from equation 3.8

frequency component	relative amplitude
dc	$1 + m^2/2$
w_s	$2m$
$2w_s$	$m^2/2$
$2(w - w_s)$	$m^2/4$
$2w - w_s$	m
$2w$	$(1 + m^2)/2$
$2w + w_s$	m
$2(w + w_s)$	$m^2/4$

note: - 'm' is modulation index
- absolute amplitudes are obtained by multiplying the above terms by the following factor:

$$\left(\frac{V_p^2}{4}\right)\left(\frac{d^2I}{dv^2}\right)$$



Ls - internal series inductance
Rs - series resistance
Cc - case capacitance
Cj - junction capacitance
Rj - junction resistance

Figure 3.9 Equivalent circuit for Schottky diode.

matching network is required to impedance match the output of the preceding stage to the junction resistance, R_j, of the diode. The diode cutoff frequency is given by $f_c = 1/(2\pi R_s C_j)$. The junction resistance is given by:

$$R_j = \frac{dV}{dI} = \frac{nKT}{qI} \qquad 3.10$$

The available noise power from a diode is as follows (Uhlir, 1963):

$$n_i = \left(T_w + \frac{f_n I_d}{f}\right) KTB \qquad 3.11$$

where $T_w KTB$ = shot noise term

f_n = flicker noise corner frequency

I_d = diode current

B = bandwidth

The above diode noise equation has a frequency independent part which is shot or thermal noise, and has a frequency dependent part which is flicker (1/f) noise. The shot noise term can alternately be expressed by (Van der Ziel, 1976):

$$I_n^2 = 2qIB \qquad 3.12$$

The sensitivity of a low-level detector is determined by the diode's noise characteristics, parasitic loss, impedance mismatch loss, amplifier noise properties, and

detection bandwidth (Watson, 1969). Current sensitivity is given by (Cowley,1966):

$$B = \frac{\Delta i}{P} = \frac{q}{2nKT} \frac{1}{\left(1+\frac{R_s}{R_j}\right)\left(1+\left(\frac{f}{f_o}\right)^2\right)} \qquad 3.13a$$

$$f_o = \frac{1}{2\pi C_j R_j} \sqrt{\frac{R_s+R_j}{R_s}} \qquad 3.13b$$

where B = current sensitivity

Δi = change in short-circuit DC current

P = available input power

Since C_j, R_j, and R_s are dependent on DC bias, there is a limit to the maximum value for B as a function of bias and is generally in the range 1 - 15 μA/uW.

The highest values of B are obtained for the DC bias in the range of 10 - 100 μA. The optimum bias depends on a number of considerations: increasing the forward bias reduces the impedance and results in increased bandwidth; and flicker noise increases with bias current as equation 3.11 shows. The optimum bias for a detector diode is usually determined experimentally. The Schottky diode, MBD102, was used in the channel receiver design of the MCSA (C_c = 0.18 pF, L_s = 3 nH, C_j = 0.88 pF, I_s = 0.02 μA). It was found to have optimum detection sensitivity at a forward bias current of 20 μA.

Detector sensitivity is commonly expressed as tangential sensitivity (TSS) which is a subjective term but an adequate measure for sensitivity. It can be directly measured from an oscilloscope trace since it is the point at which the peak output of the signal-plus-noise equals twice the value of peak noise alone. This corresponds to an SNR of 2.5 (see first trace in figure 5.23). Since a low-level detector is a square-law detector, the output power is proportional to the square of the input power and TSS is proportional to the square root of the amplifier bandwidth. For RF frequencies below 15 GHz, a typical TSS is -60 dBm for a bandwidth of 100 KHz.

The output of the detector stage of the receiver goes into a differential amplifier. Virtually ideal differential amplifiers are now available and are known as instrumentation amplifiers. They have extremely high input impedances ($>10^{12}$ ohms), low bias currents of 3 pA, and high common-mode rejection ratio (110 dB minimum). Typical devices are: LF152, LF352, and LH0036.

3.5 Synchronous Detector Operation

The theoretical basis of synchronous detection is described along with the functional implementation of this technique.

The synchronous detector as developed for the multichannel spectrum analyzer, was based on the original design first developed by Dicke (Dicke, 1946). The detector then was known as the switched or Dicke receiver. The receiver was developed for astronomical experiments where a highly sensitive radio frequency receiver was required. Figure 3.10 shows the functional layout of the Dicke receiver.

The input of the Dicke receiver is continuously switched between the signal source (antenna) and the comparison or reference noise source. At the time when the receiver was developed, there were considerable problems with power supply regulation, amplifier gain stability, and filter stability. Today, these problems have ceased to be the predominant obstacle. However, contamination of the signal in the RF amplification section due to poor shielding and thermal instability of the detector are still a problem today. The Dicke receiver is the basis from which most present day lock-in amplifiers are designed.

The essential idea behind the Dicke receiver is to multiplex a calibration signal, in this case a thermal

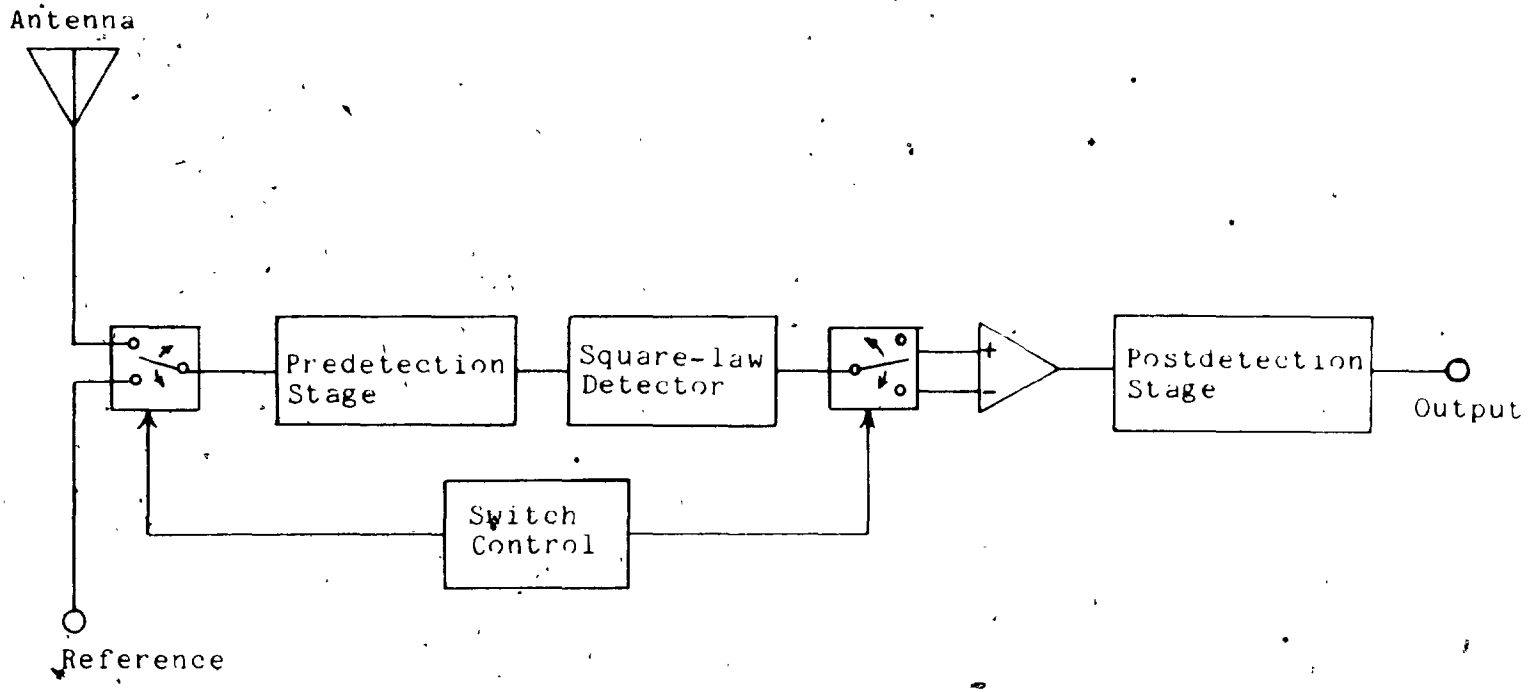


Figure 3.10 Dicke receiver.

noise source, with the desired signal, process the two together, and then demultiplex them at the output.

The RF section of the Dicke receiver (figure 3.10) consists of amplification and mixing, to produce an IF band containing the desired signal, and the reference. Square-law detection has been shown to be the best detection scheme for an optimum sensitive receiver (Kelly, 1963) and this has been used in the next stage of processing. Such a detector has the added advantage that its output voltage is directly proportional to its input power. The output of the detector is bandpass filtered and video amplified and then demultiplexed to regenerate the desired signal component and the reference component. The integrator in the post-detection stage is essentially a low-pass filter that integrates the difference between the signal and the reference over a long period of time.

The sensitivity or minimum detectable signal, Tmin, of a receiver is defined to be that condition where the signal-to-noise ratio (SNR) is unity or when $T_c = T_a$. The sensitivity of a Dicke receiver based on square-wave modulation and demodulation with no post-detection bandpass filtering and DC video amplification is given by (Kraus, 1966):

$$\Delta T_{min} = \frac{2T_{sys}}{\sqrt{B_{HF}/t_{LF}}} \qquad 3.14$$

where ΔT_{min} = minimum detectable signal temperature

T_{sys} = system noise temperature

B_{HF} = predetection bandwidth

t_{LF} = postdetection integration time

For a total power receiver, the expression for sensitivity would be the same as equation 3.14 but without the factor of 2 on the right side. Since the Dicke receiver is a switched receiver (0.5 duty cycle), it is only connected to the signal half the time.

The postdetection integration can be increased up to the limit given by the time signal profile (Kraus, 1966). However, 1/f noise increases with the integration time, making extended analog integration (> 10 s) impractical (Leger, 1976).

Problems associated with the DC thermal offset drift of the detectors can be eliminated by AC coupling and narrow bandpass filtering at the output of the square-law detector. There is some loss of sensitivity but this is often countered with improved thermal stability. The above modifications would introduce a factor of $\pi\sqrt{2}/4$ on the right side of equation 3.14. Demodulation in this case may be performed with a sinusoid. If sinusoidal modulation rather than square-wave modulation is used on the input signal then an additional factor of $\pi/4$ is required on the right side of equation 3.14 (Kraus, 1966).

Generally, the AC coupled version of the Dicke receiver is the preferred design for previously mentioned

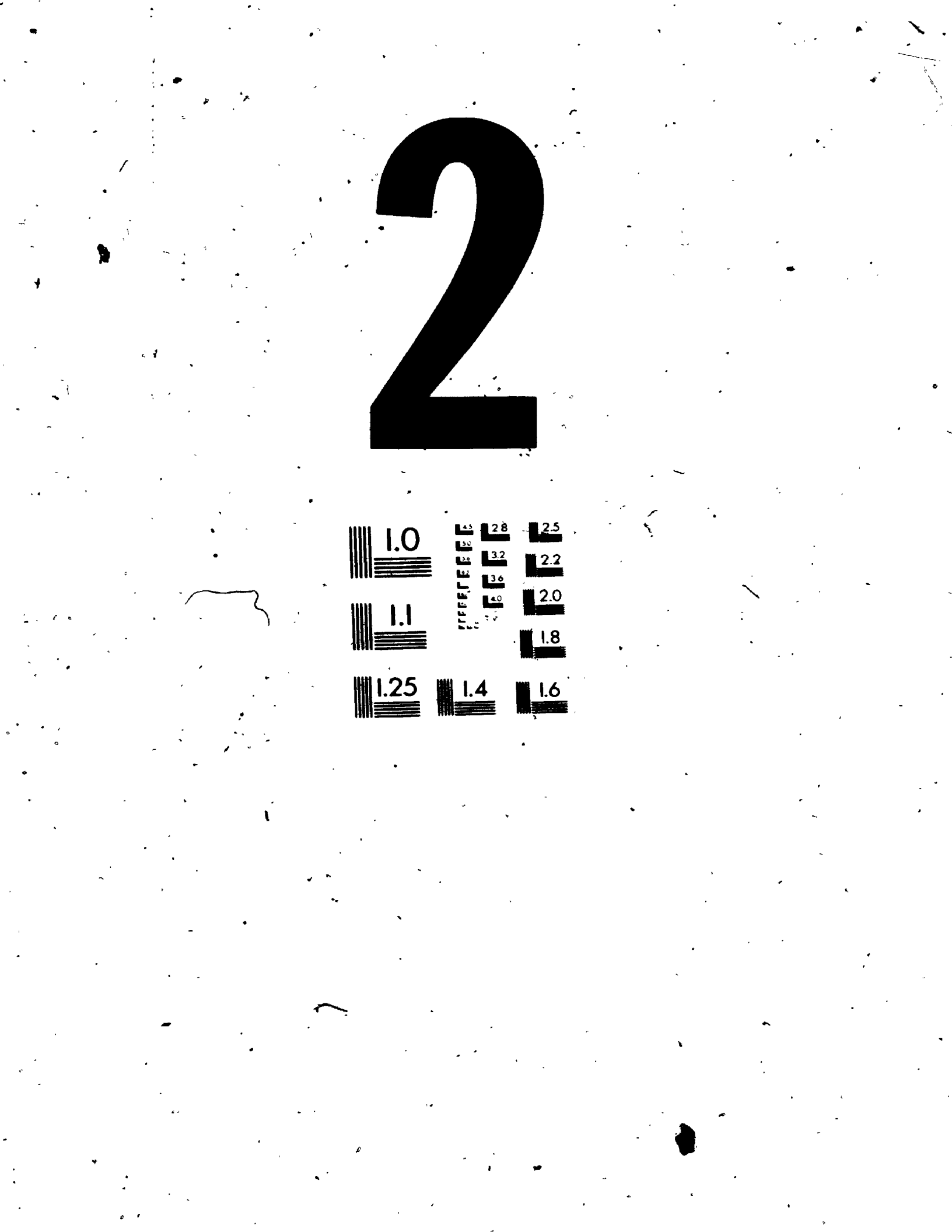
reasons. However, the synchronous detector in the MCSA uses the DC coupled scheme for a number of reasons. The DC coupling preserves the universality of the receiver system. All digital switching signals and control lines are under microcomputer control and ultimately under the user's control through software. Hence, the configuration of the MCSA can be altered from a synchronous detection arrangement to a total power detection arrangement by the use of controlling software. In addition, DC thermal offset drift can be accounted for, and eliminated by calculation once the signal has been detected and digitized.

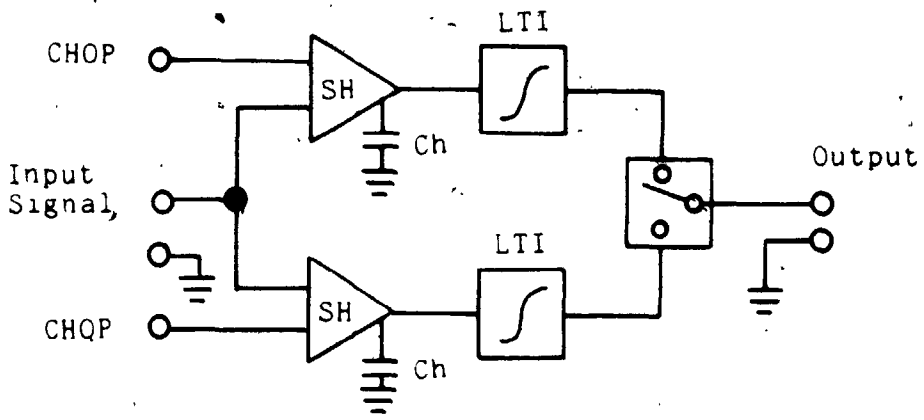
There are a number of variations of the Dicke receiver with most of them being more complicated schemes for balancing the signal and the comparison noise source. A method proposed by Orhang and Waltman (1962) incorporates gain-modulation for balancing. A null-balancing Dicke receiver was proposed by Machin, Ryle, and Vonberg (1952) where the output of a noise generator, which is used as a comparison load, is controlled by a feedback loop from the integrator output. The control voltage on the noise generator then contains a measure of the imbalance in the system.

These balancing schemes have not been implemented in hardware in the synchronous detector of the MCSA. However, any desired modifications can be implemented through software. Once the output of the synchronous

detector has been digitized by an anolog-to-digital converter, statistical processing can be applied to the data that would be difficult or impossible to implement in hardware.

The synchronous detector used in the MCSA consists of two sample-and-hold (SH) units with long-time integrators on the outputs (see figure 3.11). The two SHs alternately sample the multiplexed signal synchronously with the chopper control signal. The characteristics of the SH can be a serious problem in sensitive receivers. One important component is the hold capacitor which can be a significant source of error in an accurate SH circuit. Dielectric absorption is a problem with most capacitors. For example, a mylar capacitor may 'sag back' up to 0.2% after a quick sample. Some capacitors that have low hysteresis are polystyrene, polyproplene, and Teflon. Mica and polycarbonate have moderate hysteresis loss. Ceramic capacitors are not recommended since they have very poor hysteresis response and are susceptible to microphonic pickup. Digital feed-through can be a very serious problem if the capacitor is not shielded from the relatively large digital control signals in close proximity. Shielding consists usually of grounded guard traces printed on the PCB around the capacitor pins (National, 1980).


2
1.0
1.1
1.25
1.4
1.6
2.8
3.2
3.6
4.0
2.5
2.2
2.0
1.8



SH - sample-and-hold
LTI - long-time integrator
Ch - hold capacitor

Figure 3.11 Synchronous detector block diagram.

3.6 Local Oscillator and Frequency Multiplier Operation

The local oscillator for each of the 16 modules is synthesized and frequency multiplied from a single crystal oscillator. The crystal oscillator (32 MHz) is the primary reference frequency which is divided down to produce the main reference frequency of 250 kHz. All other oscillators are phase-locked to the main reference and are an integral multiple of the frequency. A block diagram of local oscillator synthesis is shown in figure 3.12.

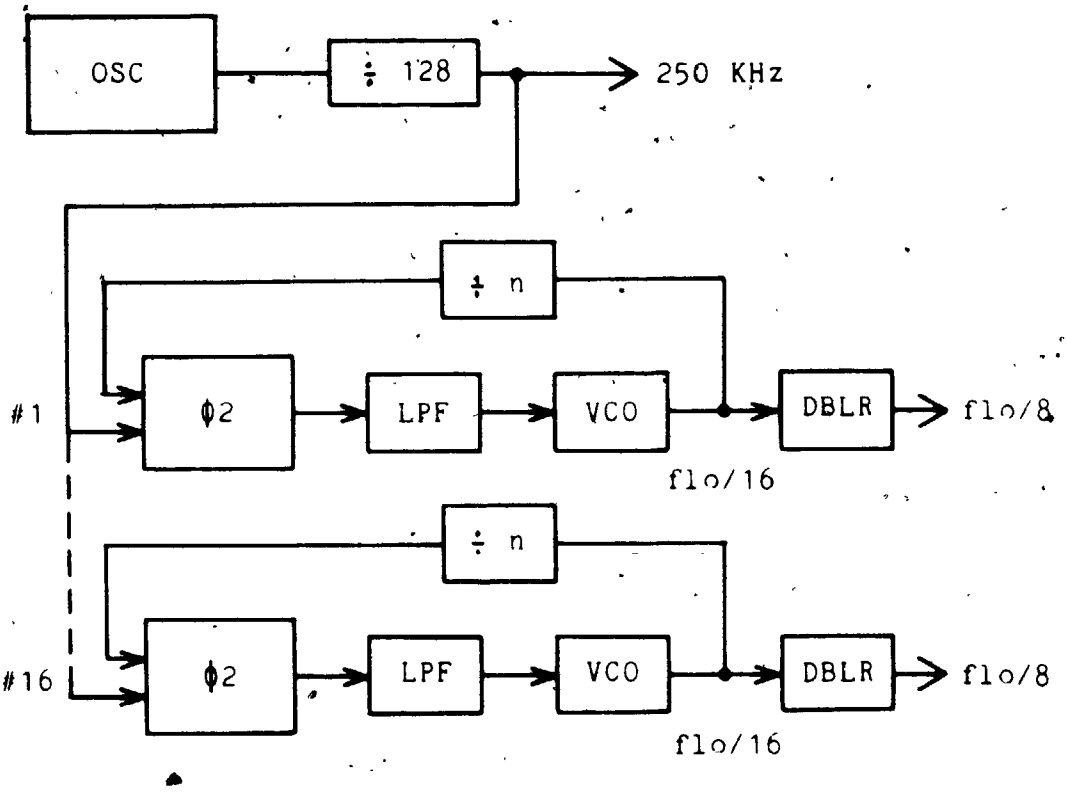
The advantage of phase-locked systems for generating local oscillator frequencies is that the frequency can be changed, should different frequency assignments be desired.

The basic block diagram of a phase-locked loop used in frequency synthesis is shown in figure 4.12a. The closed loop transfer function, H(s) is given by (Gardner, 1979):

$$H(S) = \frac{\theta_o(S)}{\theta_i(S)} = \frac{K_o K_d F(S)}{S + K_o K_d F(S)} \qquad 3.15$$

where K_o = VCO gain factor, [V/rad]

K_d = phase detector gain, [rad/s.V]



flo/8 = { 55.5, 54.5, 53.5, ..., 40.5 MHz }

OSC - oscillator
φ2 - phase II of phase-locked loop (MC14046)
LPF - low-pass filter
VCO - voltage controlled oscillator
DBLR - frequency
flo - receiver local oscillator frequency

Figure 3.12 Local oscillator synthesis block diagram.

The transfer function of the loop filter is:

$$F(S) = \frac{St_2+1}{St_1+1} \qquad 3.16$$

where $t_1 = (R_1+R_2)C$

$t_2 = R_2C$

The closed loop transfer function with a passive loop filter now becomes:

$$H(S) = \frac{S(2\ w_n - w_n^2/K_oK_d)+w_n^2}{S^2+2\zeta w_n S+w_n^2} \qquad 3.17a$$

where

$$w_n = \sqrt{\frac{K_oK_d}{t_1}} \qquad 3.17b$$

$$\zeta = \frac{1}{2}\sqrt{\frac{K_oK_d}{t_1}}\left(t_2+\frac{1}{K_oK_d}\right) \qquad 3.17c$$

It can be shown (Gardner, 1979) that for quick lock-on the maximum difference between the VCO frequency and the reference frequency is $2\zeta w_n$.

The frequency multiplier, consists of four transistors, the first three are driving each other hard in order to produce harmonics. In each transistor the output is tuned to the second harmonic of the input to maximize its transfer to the next stage. The net effect by the frequency multiplier is multiplication by eight of the synthesized local oscillator. The fourth transistor

is used as a buffer amplifier that drives the four mixers in the receivers. Figure 3.13 shows a block diagram of the frequency multiplier.

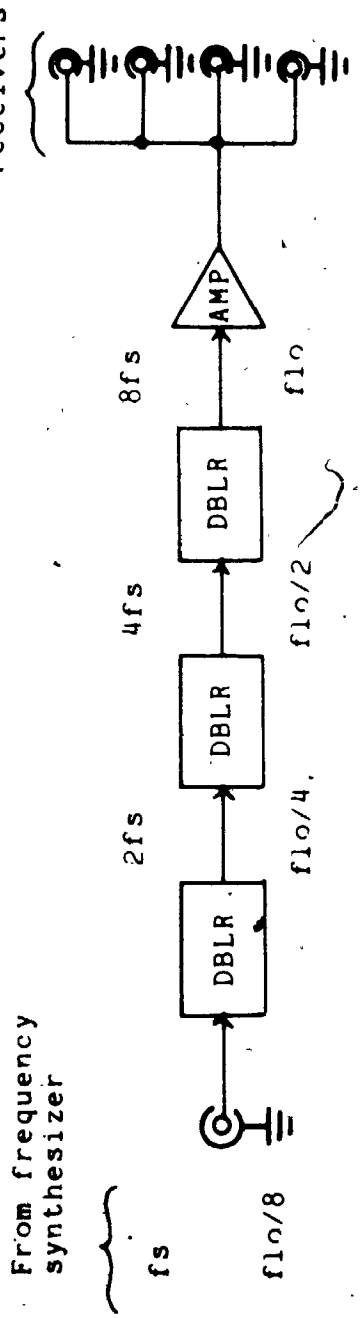


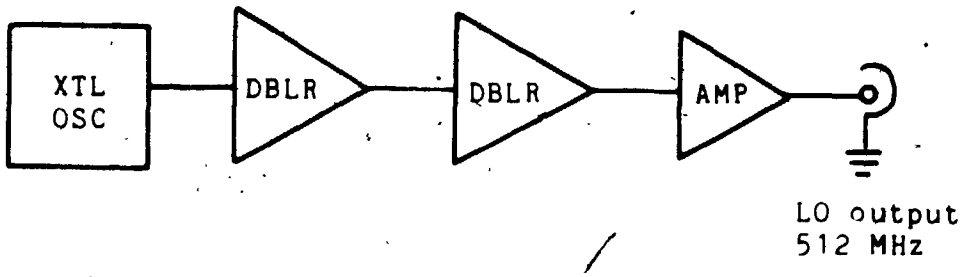
Figure 3.13 Frequency multiplier block diagram.

3.7 Front-end Local Oscillator Operation

The front-end local oscillator is used in the front-end module to shift the lower half of the signal spectrum (0 - 256 MHz) to the upper half of the signal spectrum. A block diagram of the front-end local oscillator is shown in figure 3.14. The oscillator consists of a crystal oscillator (128 MHz) to generate the primary frequency, two frequency doubling stages, and a buffer amplifier to produce the final local oscillator frequency of 512 MHz required for the front-end mixer. Shielding must be carefully considered in the circuit design because the circuit, by its nature, generates a large number of harmonics that may contaminate the input RF signal. In addition the oscillator must be well shielded from the synchronous detector control signals to prevent any modulation that would be synchronous with the operation of the detector.

The crystal oscillator is based on the Colpitts oscillator which is a design often used at high frequencies. The Colpitts oscillator configuration takes full advantage of the internal capacitances that are inherent in all transistors (RCA Corp.).

The transistor multiplier stages were designed using a combination of lumped components (inductors, capacitors) and distributed components (transmission lines). The high frequency electronics (512 MHz) on the circuit board makes



XTL OSC - crystal oscillator
DBLR - frequency doubler
AMP - amplifier
LO - local oscillator

Figure 3.14 Front-end local oscillator block diagram.

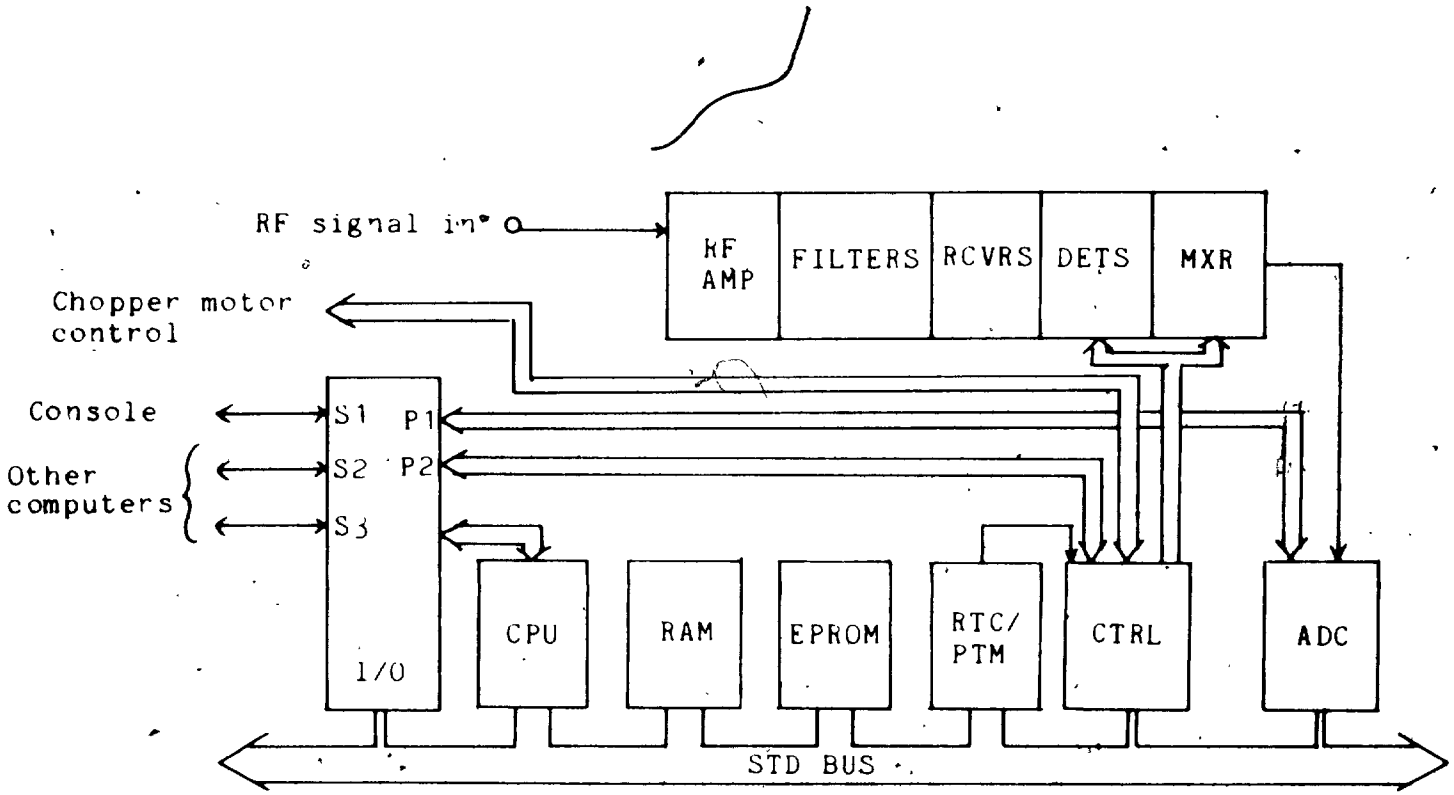
use of strip transmission lines instead of inductors, since inductors become too small and impractical.

3.8 Overview of the Microcomputer System

A microcomputer system was developed as a control system for the multichannel spectrum analyzer. Figure 3.15 illustrates the interfacing between the microcomputer and the RF portion of the multichannel spectrum analyzer (MCSA).

All microcomputer boards plug into an STD bus but not all make full use of it. The central processing unit (CPU) board, random access memory (RAM) board, real-time clock and programmable timer module (RTC/PTM) board, and erasable programmable read-only memory (EPROM) board are the only ones to make full use of the bus while the other boards (controller board, analog-to-digital converter (ADC) board) only draw power from the bus.

The input/output (I/O) board provides communication between the microcomputer, the rest of the analyzer, and other external devices by the use of serial ports (S1, S2, S3) and parallel ports (P1, P2). The primary source of I/O is by the console port (S1) where commands can be issued for software control of the entire system and where results can be graphically displayed. The other serial ports (S2 ,S3) are used to link the microcomputer to other computers (PDP-11/23, PDP-10) for the transfer of data and software. The parallel ports (P1, P2) control the RF portion of the MCSA by issuing commands to the ADC board (via P1) and to the controller board (via P2).



S - serial port
P - parallel port
CPU - central processing unit
RAM - random access memory
EPROM - erasable programmable read-only memory

ADC - analog-to-digital convertor
RF AMP - radio frequency amplifier
RCVRS - receivers
DETS - detectors
MXR - multiplexer
CTRL - controller
RTC/PTM - real-time clock and programmable timer module

Figure 3.15 Block diagram of microcomputer with RF portion of MCSA.

The CPU board contains the microprocessor (MC6809) plus 16K of on-board CMOS memory. The operating system for the microcomputer system is resident on the CPU board with some additional application software on the EPROM board.

The RAM board consists of 128K of mapped memory for temporary mass storage of data from the ADC board. Permanent storage is handled by sending the data to one of the computers down a high speed serial line (S2, or S3).

The RTC/PTM board contains a real-time clock (RTC) and programmable timer modules (PTM). This board provides various system timing and clock pulse signals required by the MCSA.

The EPROM board contains up to 64K of application software for the microcomputer system. It may be accessed through the STD bus and loaded into RAM on the CPU board.

The controller board generates control signals for running the MCSA. It also accepts control signals from the chopper motor itself and from the chopper clock source. This board is under control of the CPU board by way of the parallel port P2.

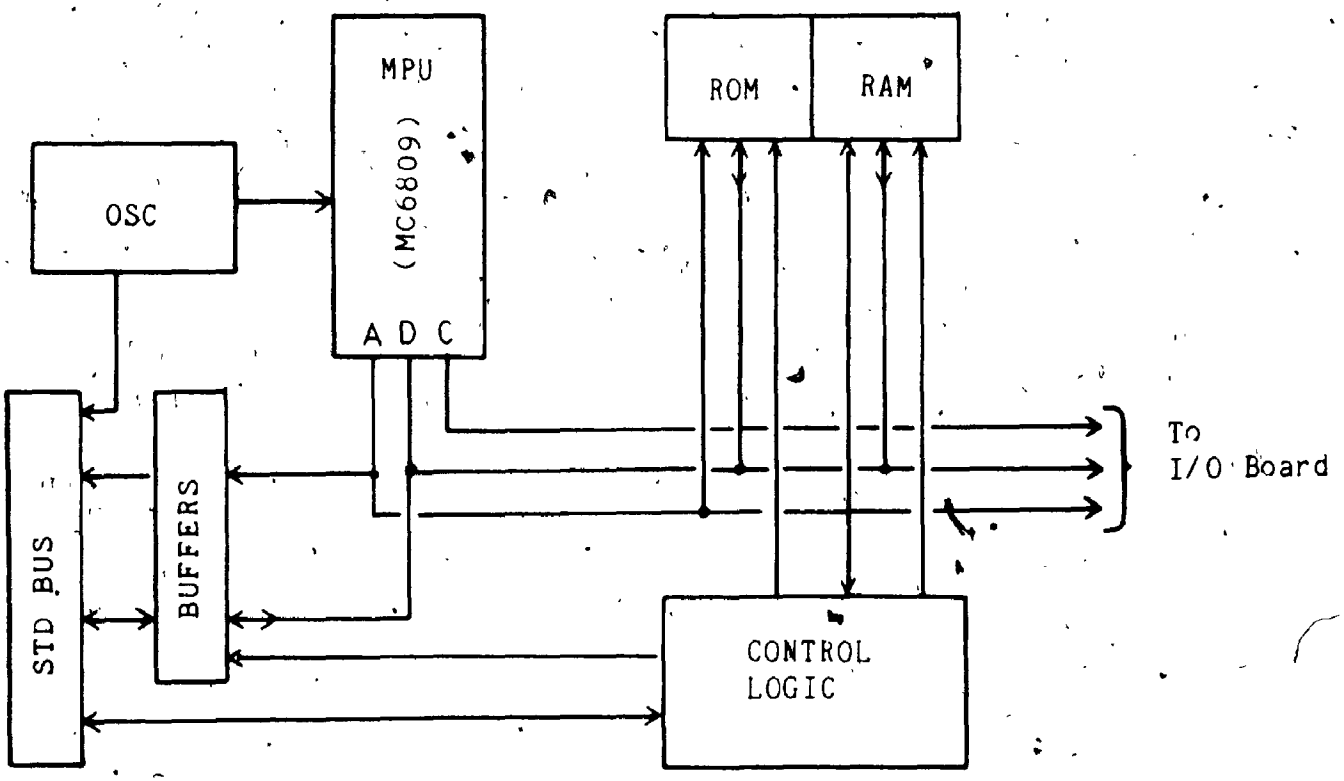
The ADC board performs an analog-to-digital conversion on the detected signal from the synchronous detector. The ADC is controlled by parallel port P2 of the I/O board.

3.9 Overview of the Central Processing Unit Board

The basic functions of the central processing unit (CPU) board are shown in the block diagram of figure 3.16. The CPU board can be accessed in two ways. One way is through the STD bus and the other is through a secondary bus connected to the I/O board. The address, data, and control lines on the secondary bus are unbuffered since nothing else shares the bus. The address, data, and control lines for the STD bus are buffered since it is a shared bus.

The control logic box in the figure represents all the hardware logic required for selecting memory chips, sending control signals on the STD bus, and controlling bus access.

The CPU board was designed to be adaptable to a multiprocessor microcomputer environment. Such a system would be able to distribute some of the processing required in handling the data generated by the MCSA. In particular, graphic processing is time consuming and could be performed by a slave CPU board rather than the master CPU board.



OSC - oscillator
MPU - microprocessor unit
ROM - read-only memory
RAM - random access memory

A - address
D - data
C - control

Figure 3.16 Block diagram of CPU board.

3.10 Overview of the Input/Ouput Board

The block diagram showing the functions of the input/output (I/O) board is shown in figure 3.17. The I/O board is under complete control of the CPU board, and in fact can be thought of as an extension of the CPU board.

The three serial ports (ACIA) all run from the same baudrate generator with a few wire-wrap selectable baudrates (300, 600, 1200, 9600). Interrupts generated by the serial ports and the parallel ports are encoded according to priority. The two parallel ports (PIA) are the primary receivers and transmitters of data and commands for the MCSA. The parallel ports can generate four interrupts and are encoded by the priority encoder. Priority of interrupt may be altered by changing wire-wrap connections on the I/O board.

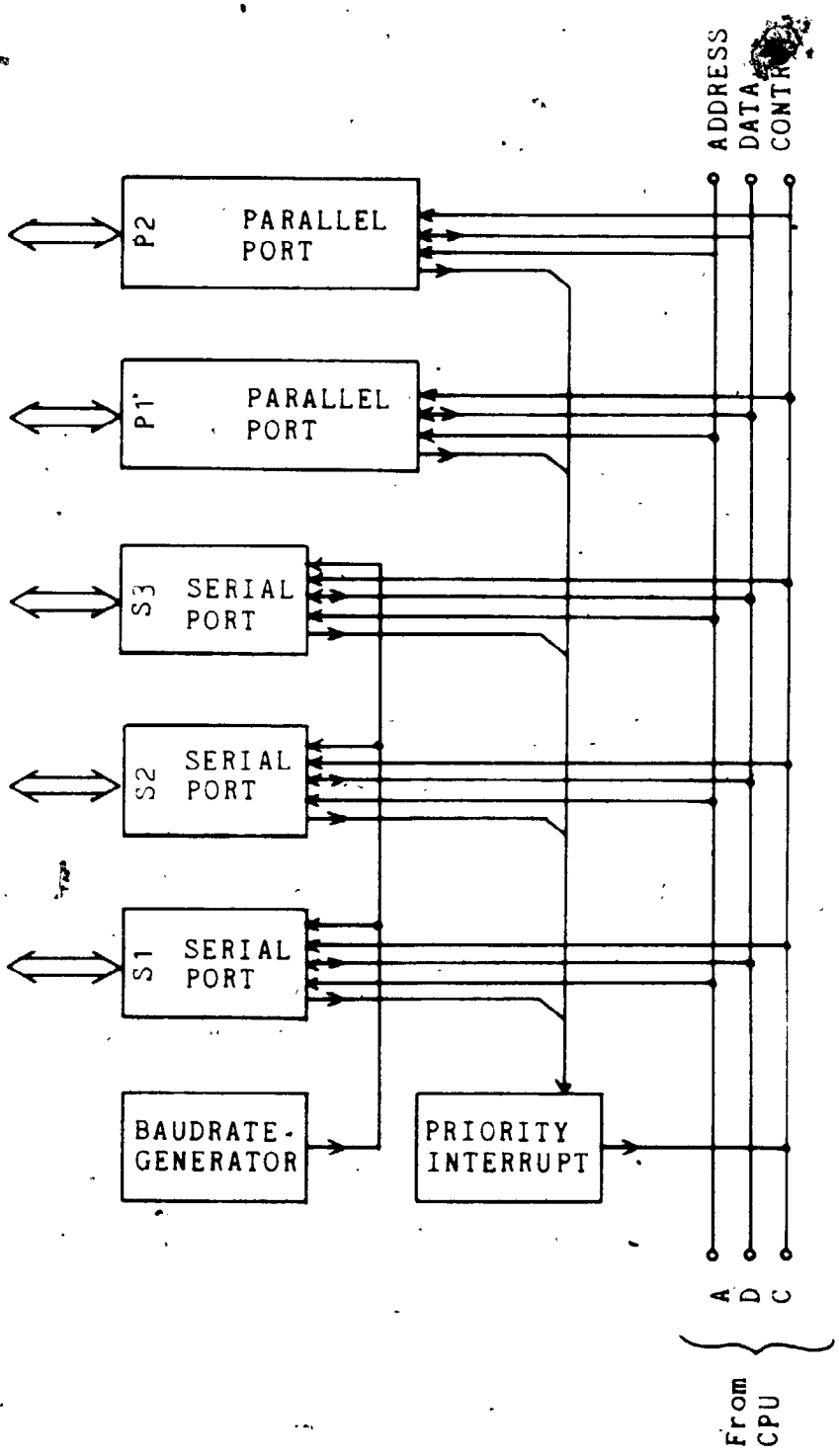


Figure 3.17 Block diagram of I/O board.

3.11 Overview of the Random Access Memory Board

The functional components of the random-access memory (RAM) board are shown in figure 3.18. The board contains 128K of mapped memory for temporary mass storage of data from the MCSA.

The technique of memory mapping is very useful from a software standpoint. For instance, programs operating on data tables need not recompute offsets for indexed addressing when working on different sets of tables. Changing the memory map automatically redirects the access to a different physical location but the same logical location.

The control logic box is required to alter the memory mapping registers, to issue read/write commands to the dynamic RAM, and to control the data buffer. The operating state of the RAM board is determined by the setting of latches in the control logic box. The latches can enable or disable the board and switch the two 64K banks of RAM. The refresh logic box contains the neccessary hardware logic for generating the refresh control signals for transparent refresh of the dynamic RAM. Thus, no wait states are required of the CPU in order for a dynamic refresh cycle to take place.

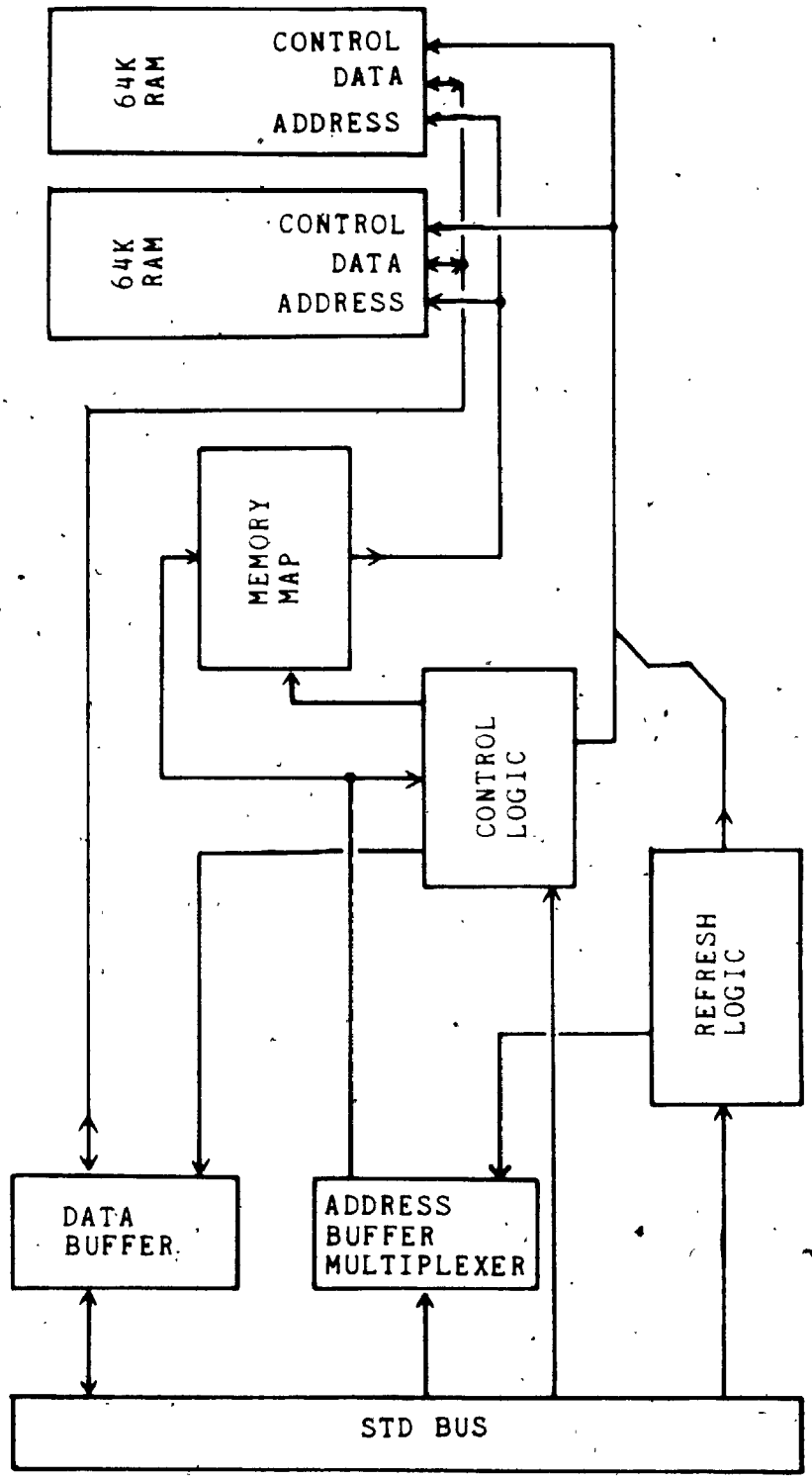


Figure 3.18 Block diagram of RAM board.

3.12 Overview of the Erasable Programmable Read-only Memory Board

The erasable programmable read-only memory (EPROM) board contains application programs stored in read-only memory and has a total capacity of 64K bytes. The memory is arranged into two banks of 32K each, of which only one bank is accessible at any one time.

The stored software is accessed through the STD bus by first communicating with the EPROM board control logic. The EPROM board will be enabled and placed on the STD bus in much the same fashion as the RAM board is. A latch register controls the enabling and disabling of the board, and the switching between the 32K banks of EPROM (see figure 3.19). The decoder/control logic is active when the EPROMs are being accessed and generate the appropriate chip-enable signals when the EPROMs are selected and deselected.

The clock regenerator circuitry is required for some of the decoding logic and for generating valid-address and valid-data signals.

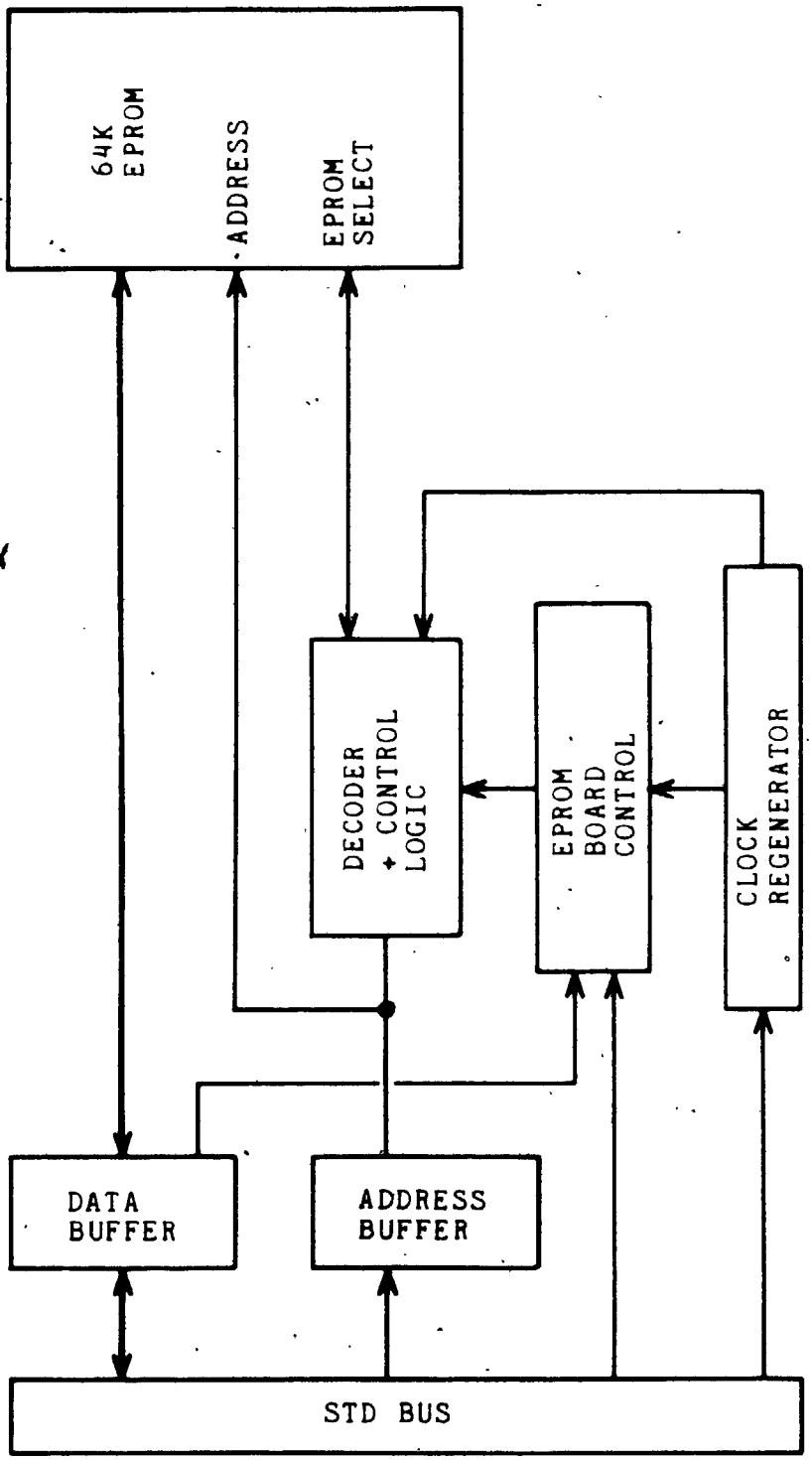


Figure 3.19 Block diagram of the EPROM board.

3.13 Overview of the Controller Board

The block diagram of the controller board is shown in figure 3.20. It consists of four registers, two phase-locked loops (PLL), and inhibit control logic.

One of the four registers controls the other three registers. The first and third registers control the buffer for control signals and the input clock selector. The second register holds the address of the receiver to be accessed by the ADC board.

The two PLLs generate the chopper signals and the receiver control signals. The first PLL locks to the clock frequency required to drive the chopper. It has a very long time constant, so it primarily serves to smooth out sudden phase changes in the clock frequency. The second PLL is used to synthesize a high frequency from which the inhibit control signal is derived. An inhibit signal is required by the synchronous detector to remove noise at the edge of the chopper control signal transition.

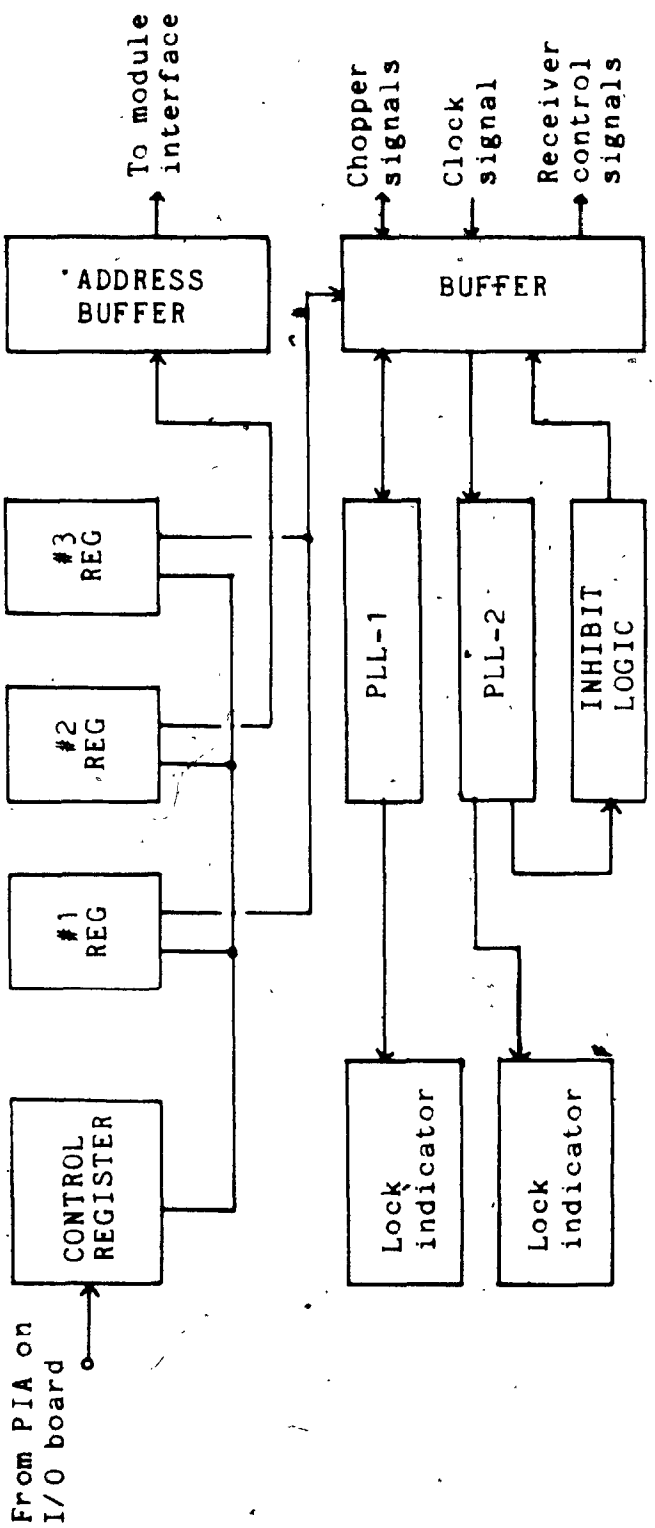


Figure 3.20 Block diagram of controller board.

3.14 Overview of the Analog-to-digital Converter Board

The analog-to-digital conversion (ADC) board is shown in figure 3.21. It consists of a 12-bit ADC chip, multichannel selection, amplification, auto-calibration, dual sample-and-holds (SH), and start/complete logic.

The 12-bit ADC chip has a typical conversion time of 100 uS but with the addition of speed-up circuitry, the chip can run at a conversion time of 24 uS. At the higher conversion rate, the conversion process will be complete just before the microcomputer is ready to accept the data. At the slower rate the microcomputer would have to wait some time for completion of the conversion process. A complete system sweep of the 64 receiver signal and reference channels takes 3.1 ms at the high conversion rate as opposed to 12.8 ms at the slower rate.

The data and control data transfer between the ADC board and the CPU board takes place through a parallel port (PIA). The control lines permit software control of channel selection (1-of-8), auto-calibration, and initiation of the ADC sequence.

The dual SH unit permits acquisition of the input signals by one SH while the other one holds its voltage for the ADC until it has completed the conversion process.

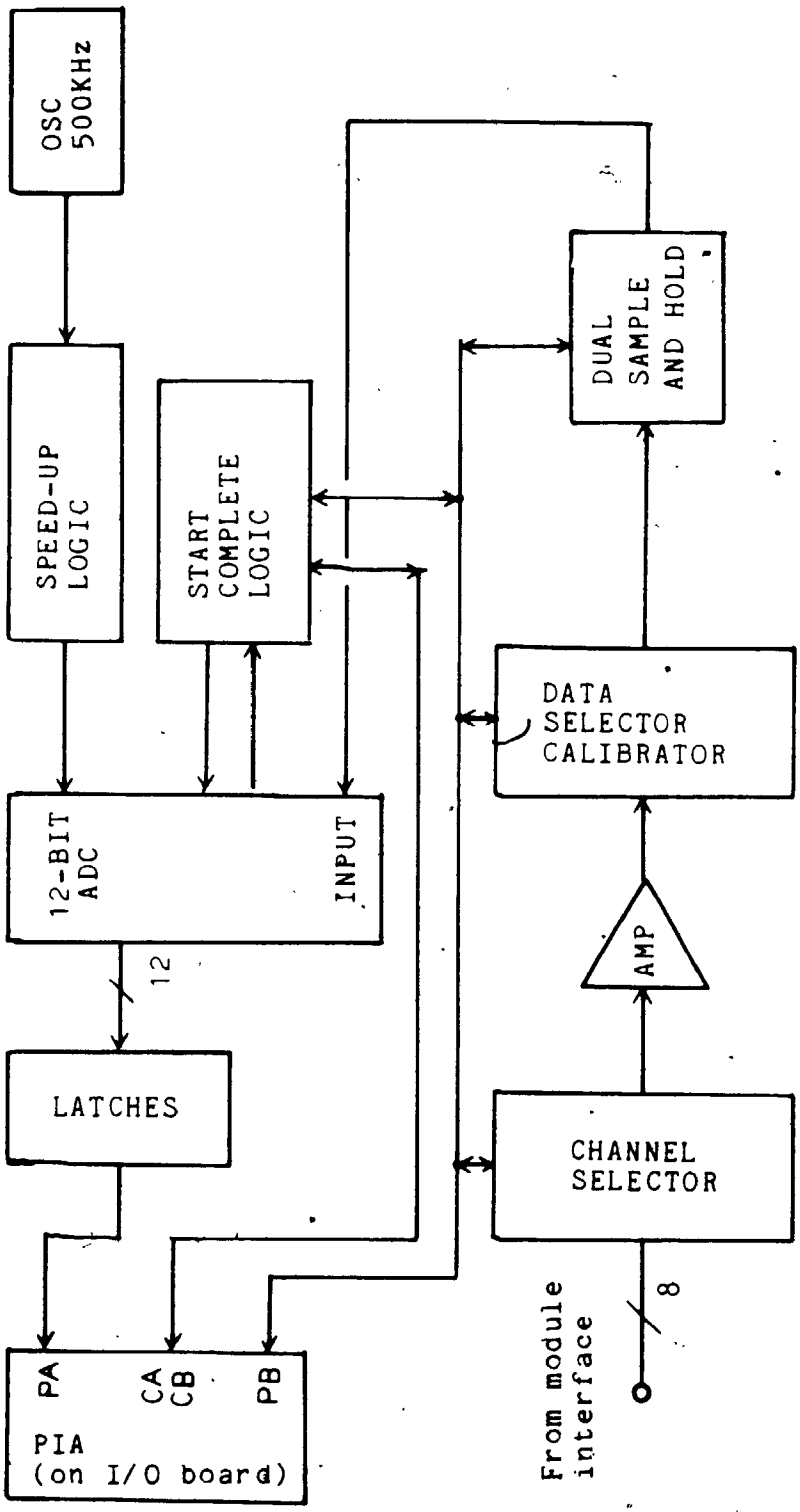


Figure 3.21 Block diagram of ADC board.

3.15 Overview of Real-time Clock and Programmable Timer Module Board

The RTC/PTM board contains a real-time clock (RTC) and two programmable-timer modules (PTM) (see figure 3.22).

The RTC/PTM board is accessed in the same way as the RAM board; the board control logic is first accessed and an enable bit is written to the enable latch to activate the board.

When the board control logic is deselected and the enable bit has been set, the RTC/PTM board will be on the STD bus and the RTC and PTMs can be programmed and treated the same as memory locations.

The RTC is a real-time clock that provides time of day to the second, and the date. It can also provide periodic interrupt and 50 bytes of CMOS RAM. The RTC is important for event timing during an experiment.

The PTM is a programmable timer with three internal 16-bit counters that can be controlled by software to generate clock signals, and interrupts. It also has three asynchronous clock and gate/trigger inputs. The PTM is primarily used in the MCSA for generating the chopper drive clock signal. The two PTMs together are capable of simulating all the neccessary control signals for the receiver modules. They proved valuable during the development stages of the MCSA system.

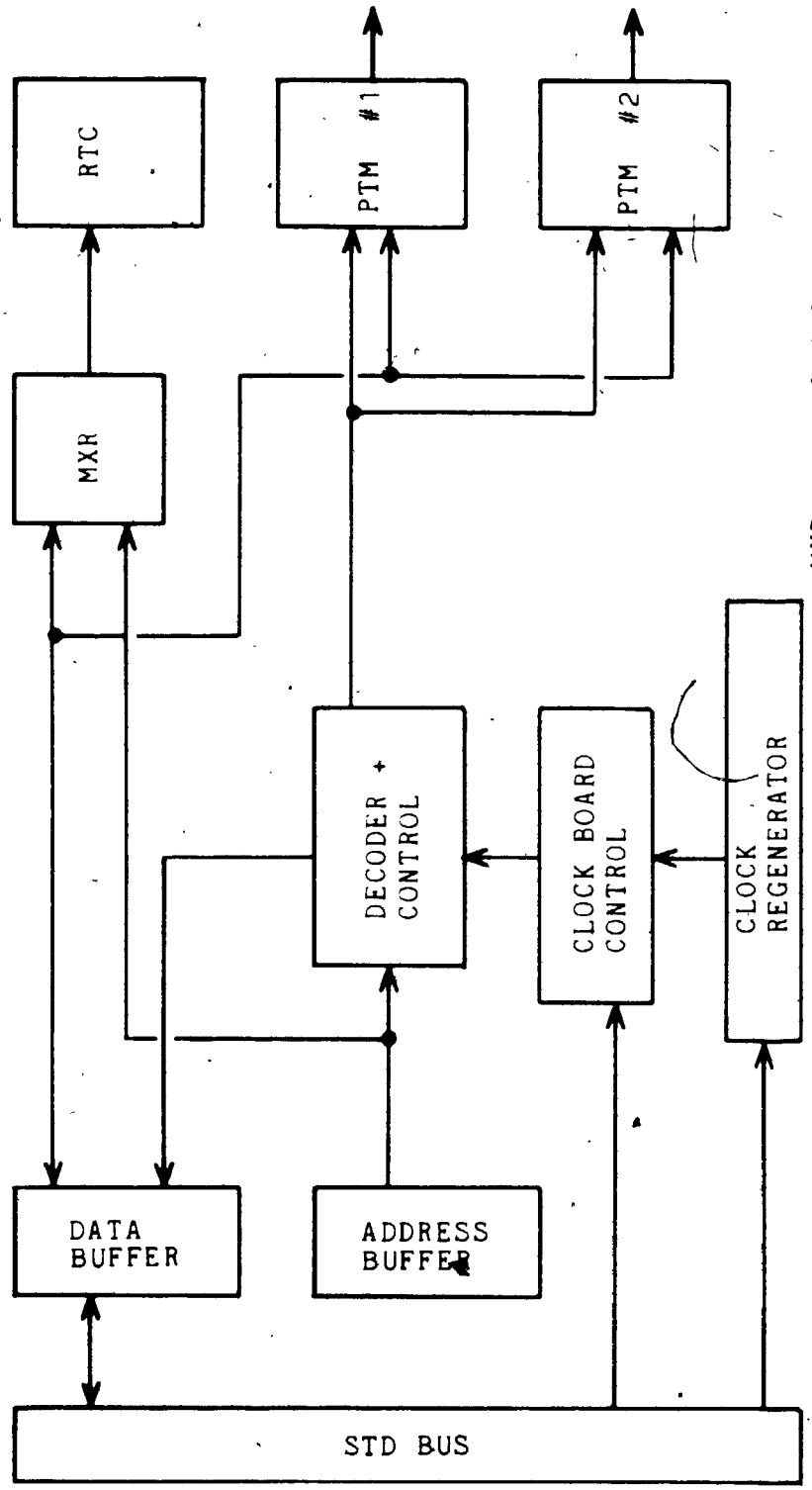


Figure 3.22 Block diagram of RTC/PTM board.

3.16 Software Considerations

There is a wide variety of software presently available for microcomputer systems. The criteria for designing the microcomputer system for the multichannel spectrum analyzer (MCSA) was to design essentially a small intelligent programmable control system with a small yet powerful operating system. In addition, due to the nature of research and development, an operating system had to be flexible to match a given environment. This required not only having the source code to the operating system, but having an operating system which could be modified for custom applications. The FORTH operating system, developed originally for radio astronomy applications, met most of these requirements. The particular implementation of FORTH for the 6809 microprocessor (MPU) is fig-FORTH version 1.0 which is public domain software (Forth).

The FORTH software system was defined by Moore in the late 1960s in order to improve his productivity as an applications programmer (Moore, 1980) FORTH was designed to supply the user with a full set of software tools which allow the use of a single language in software problems (Harris, 1981).

The FORTH operating system normally contains an interpreter, compiler, assembler, editor, and utilities. Most of these programs are written in the FORTH language and hence the operating system is known as a metasystem.

Any part of the FORTH software system can be readily modified. However, a standard for the FORTH language (FORTH-79) was defined which has managed to keep some uniformity in different implementations (Forth).

The underlying principle to FORTH is simplicity. The design of FORTH is such that it forces the programmer to adopt structured programming techniques, to decompose complex models into simpler systems, and encourage bottom-up implementation of software modules. The design and analysis of a software system is still the traditional top-down approach but it is in the implementation of the software that FORTH differs from the more usual practice.

In keeping with simplicity, FORTH contains routines that are quite small with most having only 6 or 7 lines of code. This includes the compiler (1 line), the interpreter (7 lines), and the loader (4 lines). A typical complete FORTH operating system for a microcomputer which can be written entirely in FORTH itself can reside in less than 8K bytes of memory (Brodie, 1981).

Since FORTH is simpler than other operating systems, it executes more quickly and requires less memory. High-level FORTH routines execute faster than other equivalent high-level routines, with speeds approaching 50 - 90% of machine language. Compiled code is compact with typical FORTH applications requiring about half the memory that an assembly-language program would require.

Productivity in program development, when FORTH is used, is roughly ten times better than when assembly-language is used and twice better than when high-level language is used (Brodie, 1981).

The first scientific use of FORTH occurred when it was written for a Honeywell H316 at the NRAO (National Radio Astronomy Observatory) in 1971. Its primary task at that time was data-acquisition for a radio telescope (Moore, 1980). Since that time, FORTH has played an important role in a great number of astronomical applications.

Unlike most other software systems, FORTH makes use of a stack in passing parameters between subroutines, and its programming notation is the reverse Polish notation (RPN) made popular by HP calculators.

Details of the implementation of FORTH in the microcomputer for the MCSA can be found in section 4.16. Software programs used by the system are listed in appendix F.

Chapter 4

Implementation of the Multichannel Spectrum Analyzer

4.1 Shielding and Grounding

The multichannel spectrum analyzer (MCSA) consists of radio frequency electronics, low frequency analog electronics, digital electronics, and power electronics. Each of these functional blocks requires different design procedures to minimize the effects of electromagnetic interference (EMI) that originate from them or influence them. The following describes the noise reduction techniques implemented in the MCSA to minimize the effects of EMI.

Diecast aluminum boxes were used for shielding RF electronics in the MCSA. These boxes have flanged lids, to minimize leakage from the seams. As the lids made good electrical contact with the perimeter of the boxes, use of conductive gaskets was not found to be necessary. All coaxial cables passing through the shielded box were carefully decoupled by bringing a small section of the exposed shielding braid of the cable into electrical contact with the hole in the aluminum box. Aluminum foil was packed in the hole for firm support of the cable and for good electrical conductivity between the shielding box and cable. Proper connectors (BNC, miniature BNC) were used for the most critical applications and for the best

results.

The shielding boxes were mounted in groups on one side of aluminum shielding plates to form modules. The plates support the boxes and give some degree of shielding between modules by providing a very low conductive path to ground for stray internal or external signals.

The power is distributed to each module by a separate set of power lines from a power regulator rather than adjacently linking ('daisy chaining') the modules together. This eliminates common impedance ground paths or supply voltage paths between modules. The power on each module is regulated once again to the various voltages required. This typically provides 75 dB ripple rejection of signals on the module power line. All power lines distributed to the modules' regulators are twisted pairs or triples of wire heavily loaded with capacitance (3.3 μF tantalum capacitor).

The power lines on the module were linked to adjacent boxes since the boxes are in close proximity and the power lines are heavy gauge wire. The power lines on entering the box are only RF shorted to each other with a small capacitor (4.7 nF ceramic capacitor) and not to the wall of the shielding box. If the power supply lines were capacitively shorted to the wall, then any induced RF currents flowing in the wall may flow out of the box along the power line. The power supply lines immediately pass through a ferrite RF choke (Ferroxcube: °VK200 19/4B) which

provides up to 800 ohms series impedance to RF currents generated internally or externally.

All of the RF circuit boards are mounted in the boxes with a single screw bolted to the bottom of the box and the circuit board bolted on the screw between two nuts. The RF circuit boards have ground planes on the component side and, around the perimeter of these boards, brass shim stock tabs have been soldered. The brass tabs are flexible and long enough to make good electrical contact with the aluminum box walls when the board is push fitted and mounted in the box. It is possible to have noise generated between the brass and aluminum due to galvanic action but, since the environment is very dry, galvanic action and corrosion have not been noticed. In the most sensitive RF electronic boxes, all of the brass tabs have been tinned with solder to reduce galvanic action. Gaps between the RF circuit boards and the box walls have been filled with compressed aluminum foil to exclude any magnetic fields that may tend to circulate about the board.

Signal lines that exit from the RF boxes are either coaxial cables or a twisted pair of lines which are grounded at one end only (usually the source) and terminate at a high impedance differential amplifier.

The digital electronics on the module together with the RF electronics are contained in shielding diecast aluminum boxes. This reduces pickup and modulation of the

low-level RF signals by the high-level digital signals. The power supply lines for the digital electronics are driven by a different set of regulators from those used for the RF circuitry. The common connection point is at the entrance of the module supply lines.

Control and return signal lines for the digital circuitry on the module are assembled in ribbon cables with alternate lines being a signal ground. The alternating signal grounds provide excellent shielding from electric fields between adjacent lines, but only minimal shielding from magnetic fields. Since all of the digital electronic circuits were designed with CMOS integrated circuits, there are very low currents flowing in the control lines resulting in very low magnetic fields. Very little interference was noticed from the control lines on the signal lines.

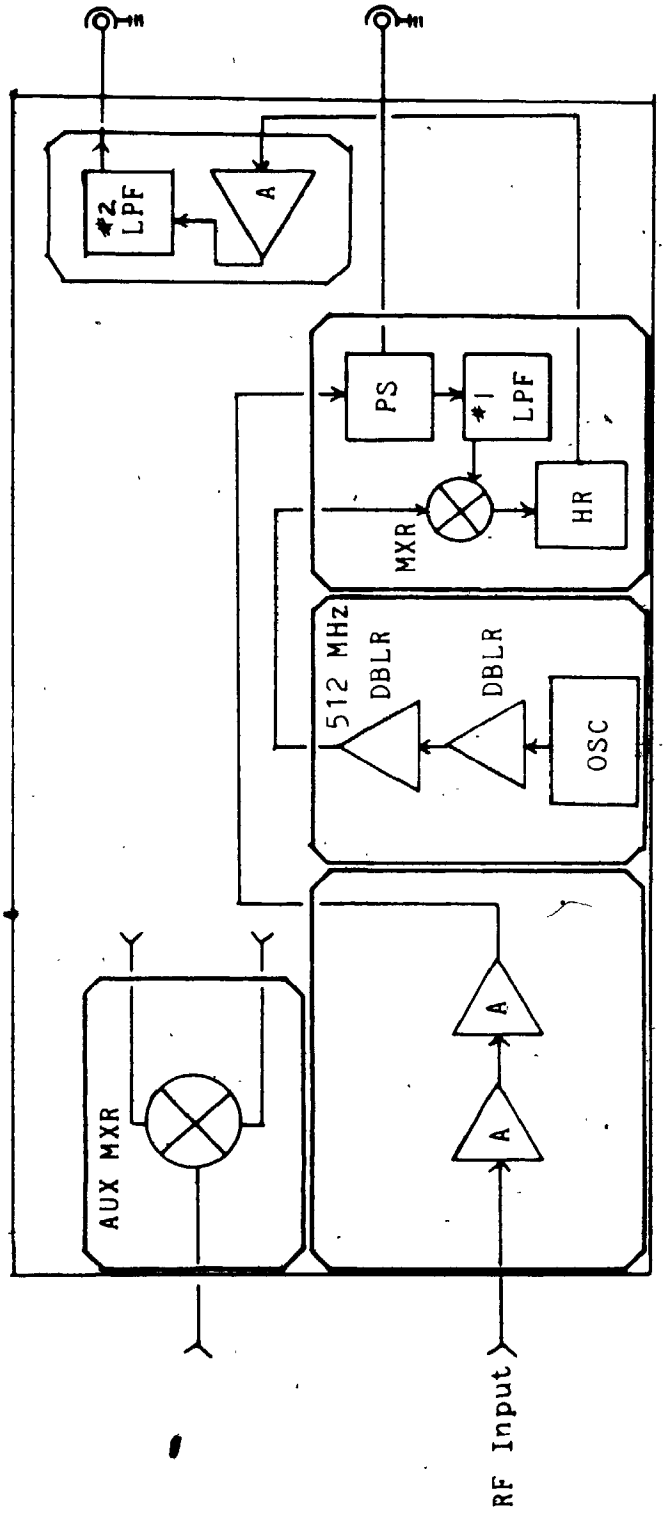
4.2 Front-end Module

The radio frequency front-end module of the multichannel spectrum analyzer is the first stage of RF processing for the input signal. It consists of wideband amplifiers, mixers, power splitters, and wideband filters. The following describes in detail the implementation of the front-end RF electronics.

The front-end module consists of two sections, each being a module in itself. The first section of the front-end module that the input signal meets is a wideband low-noise amplifier. This amplifier was supplied by Avantek Inc. (see Appendix C under 'Amplifier - AMM502B' for specifications) and is designed for the range of 5 - 500 MHz. Following this, there is another similar amplifier (from Tron-Tech Inc.) that is optional and can be placed in cascade with the previous amplifier for additional gain. This amplifier has a better noise figure but less gain and lower compression point (see Appendix C under 'Amplifier - W1GA' for specifications). The noise performance of a system is much better when blocks of RF gain are switched in line to obtain a desired amplification rather than large amplification reduced by switchable attenuators. Switchable attenuators are much more convenient since they are simply attenuator pads inserted in line with the input coaxial cable. However, inserting attenuators before the first stage of

amplification degrades the noise figure of the input signal drastically. This is clearly shown by Friis' formula for noise figure, equation 3.5, where high attenuation is like an inverse gain amplifier. Both of the wideband amplifiers are supplied in shielded boxes with BNC connectors. For additional shielding, the two amplifiers were mounted inside a large diecast aluminum container along with regulators for the power supply lines.

The output of the front-end RF amplifiers is connected to a 2-way power splitter (Mini-Circuits: PSC2-1W). This device has good broadband properties and is shielded from EMI (see Appendix C under 'Power splitter - PSC2-1W' for specifications). The power splitter was mounted on a printed circuit board along with a low-pass filter, mixer, and helical resonator. The circuit board was enclosed in a diecast aluminum box for shielding and was located away from the shielded box containing the front-end amplifiers. The hardware layout of the front-end module is shown in figure 4.1 and should be compared with the front-end block diagram in figure 3.4. The diecast shielding boxes for the front-end module were arranged in a roughly linear fashion and mounted on an aluminum shielding plate. This arrangement minimizes RF paths and reduces pickup problems if there is leakage from one box to the next.



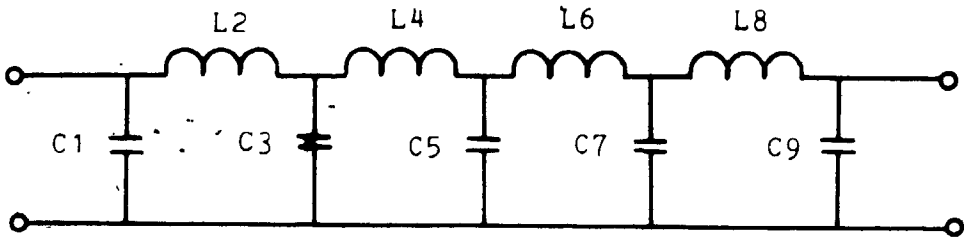
A - amplifier
DBLR - frequency doubler
OSC - oscillator
MXR - mixer
HR - helical resonator
PS - power splitter
LPF - low-pass filter
AUX - auxiliary mixer

Figure 4.1 Hardware layout of first section of front-end module.

The two outputs of the power splitter (in first section of front-end module) are processed by two identical sets of circuitry in the second section of the front-end module after one of the outputs has had some additional RF processing. This processing is required by the lower half of the signal spectrum and consists of low-pass filtering, frequency translation, and further filtering.

The lower half of the signal spectrum is low-pass filtered (f_c = 256 MHz). The filter is a 9th-order Chebyshev low-pass filter designed for a passband ripple of 0.28 dB and its schematic is shown in figure 4.2. All capacitors are 10 pF trimmers (Philips 808 film dielectric) in parallel with fixed-value ceramic capacitors. This combination brings the variable capacitance within range of the required capacitance. The 44. nH inductors were made with 2 turns of AWG #28 wire with an approximate diameter of 4.76 mm (3/16 in.). Adjusting the inductance is a matter of spreading or compressing the coils for less or greater inductance. A nominal 50 ohm resistor is required to terminate this filter since its design was based on a 50 ohm source and load impedance.

The next stage is a double-balanced mixer which has a VSWR dependent on frequency. Thus, the mixer cannot provide a good 50 ohm resistive termination to the low-pass filter over a wideband.



Chebychev low-pass filter

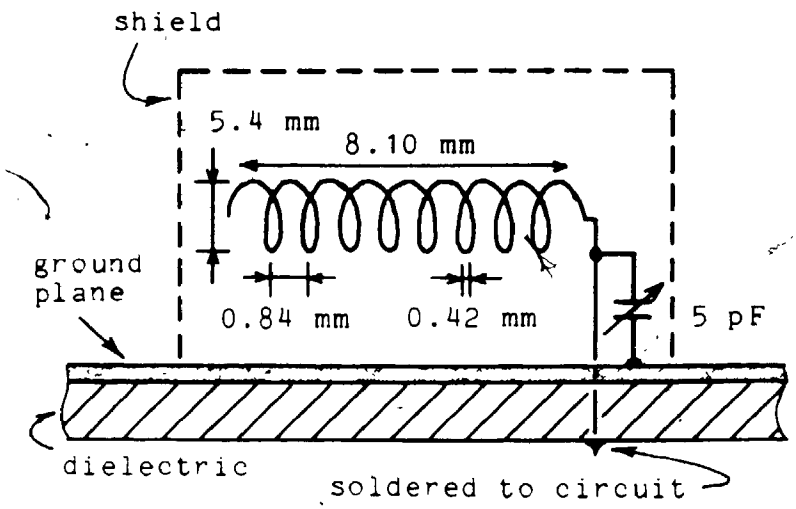
9th order, 0.28 dB ripple, fc = 256 MHz

C1 = 18.6pF	L2 = 42.0nH
C3 = 30.2pF	L4 = 46.0nH
C5 = 30.8pF	L6 = 46.0nH
C7 = 30.2pF	L8 = 42.0nH
C9 = 18.6pF	

Figure 4.2 Low-pass filter schematic (fc = 256 MHz).

The mixer is a commercially available double-balanced device (see Appendix C under 'Mixer - SRA-1W' for specifications). It yields good mixing characteristics provided that the local oscillator is large enough (7 dBm) to switch the internal diodes to enable good chopping action.

The output of the mixer passes through a helical resonator which is a narrow band-reject filter that reduces the feed-through of the local oscillator by an additional 30 dB over the isolation provided by the mixer. The detailed structure of the helical resonator is shown in figure 4.3. It consists of a coil mounted on a printed circuit board (PCB) inside a square cavity. The coil behaves like a coiled centre conductor of a transmission line with one end open-circuited and the other end connected to the circuit. The copper ground plane on the PCB forms one wall of the cavity with the other walls made from brass shim stock. All the seams of the cavity were sealed with solder to prevent leakage and to obtain the maximum Q for the cavity. High Q resonant cavities with helical centre conductors are prone to mechanical vibration which would result in amplitude modulation of the rejected signal. Mechanical vibrations were damped in the helical resonator by a piece of sponge rubber inserted down the axis of the coiled conductor. The resonant frequency of the helical resonator can be adjusted by a 5 pF trimmer capacitor (Philips 808 film dielectric) which



Refer to Appendix D.

Figure 4.3a Helical resonator structure.

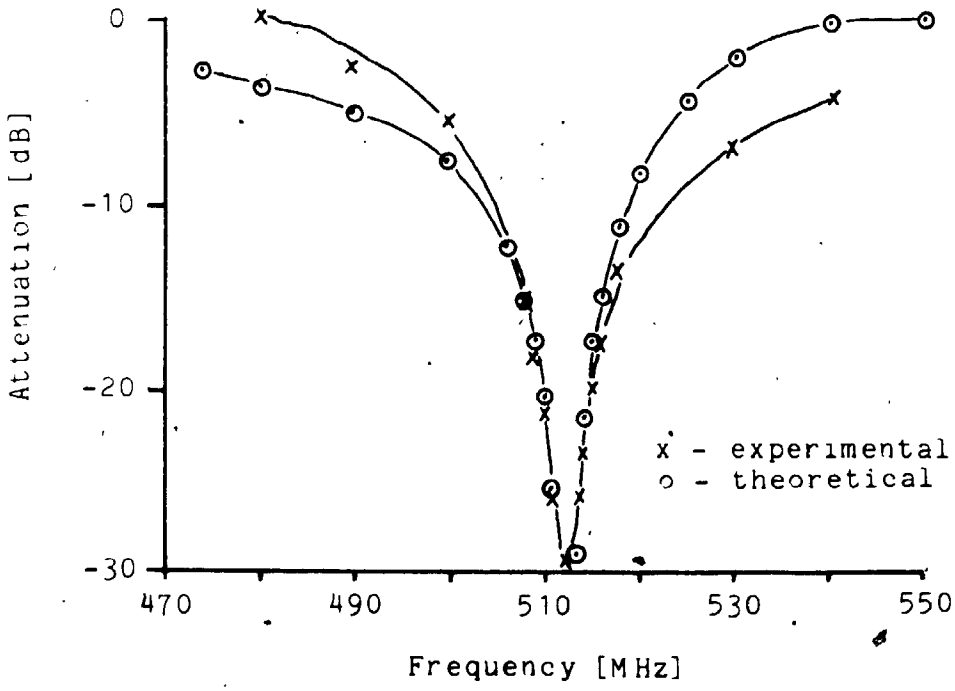


Figure 4.3b Frequency response of the helical resonator.

was placed in parallel with the resonator to ground. The helical resonator was developed using the paper published by MacAlpine (1959) which contains both graphs and design equations. The design details are presented in Appendix D.

The output of the helical resonator leaves the shielded box via BNC connectors and coaxial cable and enters another shielded box containing an attenuator, amplifier, and low-pass filter (see figure 4.4).

The attenuator, designed for 3 dB loss, is in a 'T' configuration and from figure 3.5 the calculated values for the resistors are: R_a = 8.6 ohms, and R_b = 141 ohms (actual values used were: R_a = 8.2 ohms, R_b = 150 ohms).

The signal from the attenuator is capacitively coupled to a wideband amplifier module (see Appendix C under 'Amplifier - MWA110' for specifications). This device was biased for a collector current of 20 mA which, from the data sheets, implies a collector resistor 440 ohms. This was made up of a .47 ohm resistor, a ferrite bead (Ferroxcube, VK200 19/4B), and a 390 ohm resistor. The junction between the 47 ohm resistor and the ferrite bead was capacitively decoupled (10 nF) to ground, to filter out any supply line noise. At a current of 20 mA, the amplifier has a gain of 16 dB and a 1 dB compression point of 5 dBm.

The amplifier was designed to be a buffer to drive a 9th-order Chebyshev low-pass filter. The filter was

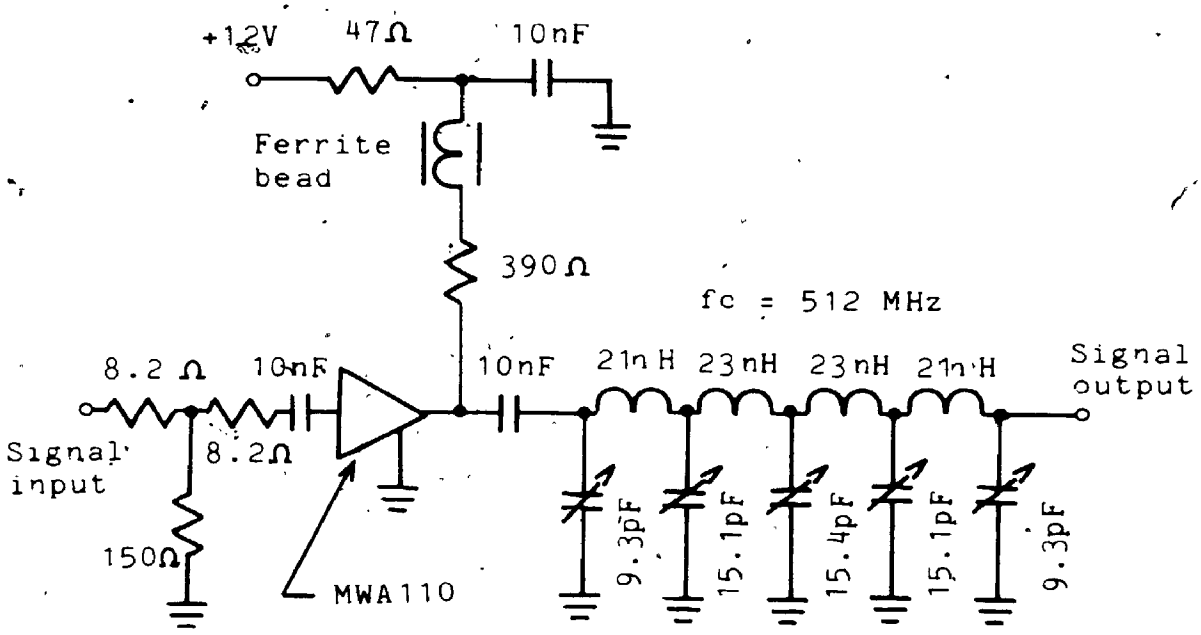


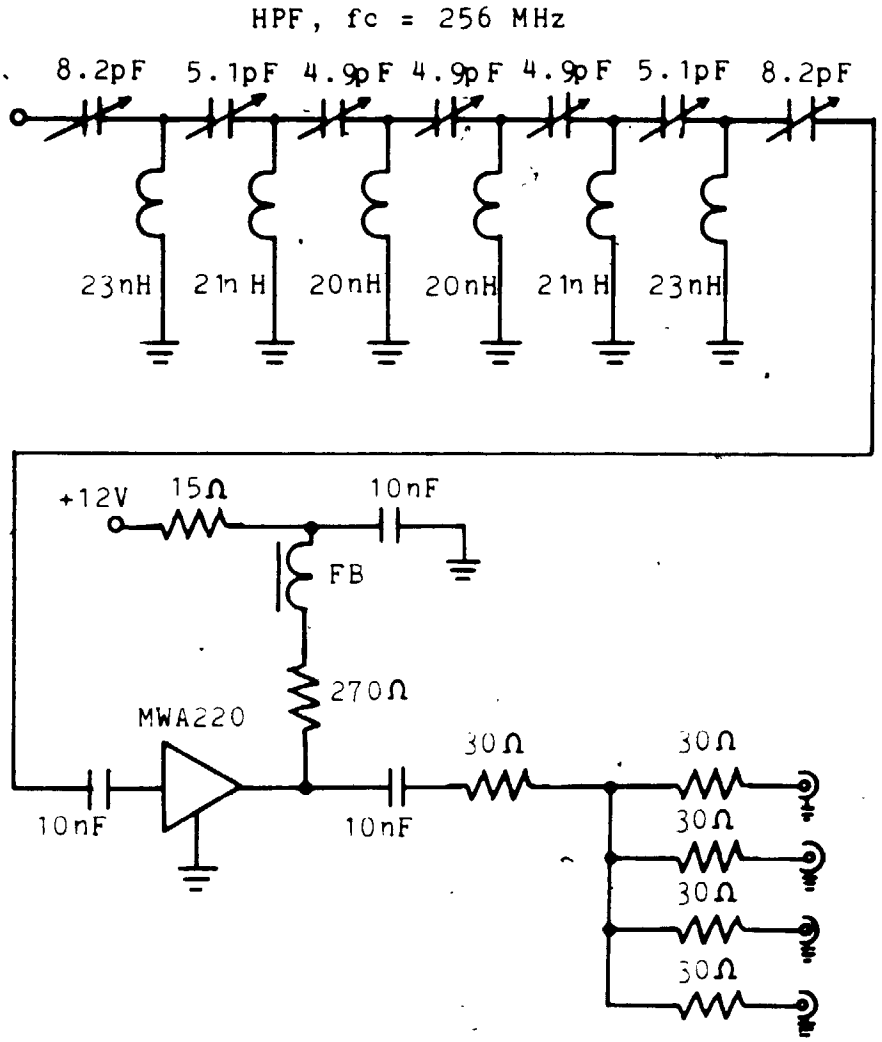
Figure 4.4 Buffer amplifier and low-pass filter for the lower half of the signal spectrum.

designed for a cutoff frequency of 512 MHz and a passband ripple of 0.28 dB. The capacitors used in the filter are 10 pF trimmers (Philips 808 film dielectric) with 4.7 pF fixed value ceramic capacitors in parallel. The inductors are 1.5 turns of wire (AWG #24), with a diameter of 3.2 mm (1/8 in.).

The next stage of RF processing was designed to be the same for both the upper and lower halves of the signal spectrum. This stage resides on the second section of the front-end module and contains a high-pass filter, amplifier, and 4-way power splitter (see figure 4.5). The high-pass filter is a 13th-order Chebyshev with a cutoff frequency of 256 MHz, a 0.28 dB passband ripple, and a very sharp transition band. The capacitors used in the filter were 10 pF trimmers. The inductors were 1.5 turns of wire with a diameter of 12.2 mm (1/4 in.).

The output of the high-pass filter is capacitively coupled to a wideband amplifier module (see Appendix C under 'Amplifier - MWA220' for specifications). The amplifier, a wideband hybrid, was biassed with a collector current of 30 mA and is shown in figure 4.5.

The amplifier drives a resistive 4-way power splitter. The design of the power splitter is shown in figure 3.6. For the case of a 4-way split, 30 ohm resistors are required for a match to 50 ohms on all ports. The outputs of the two 4-way power splitters are connected to the inputs of the eight filter banks.



FB - ferrite bead (Ferroxcube VK200 19/4B)

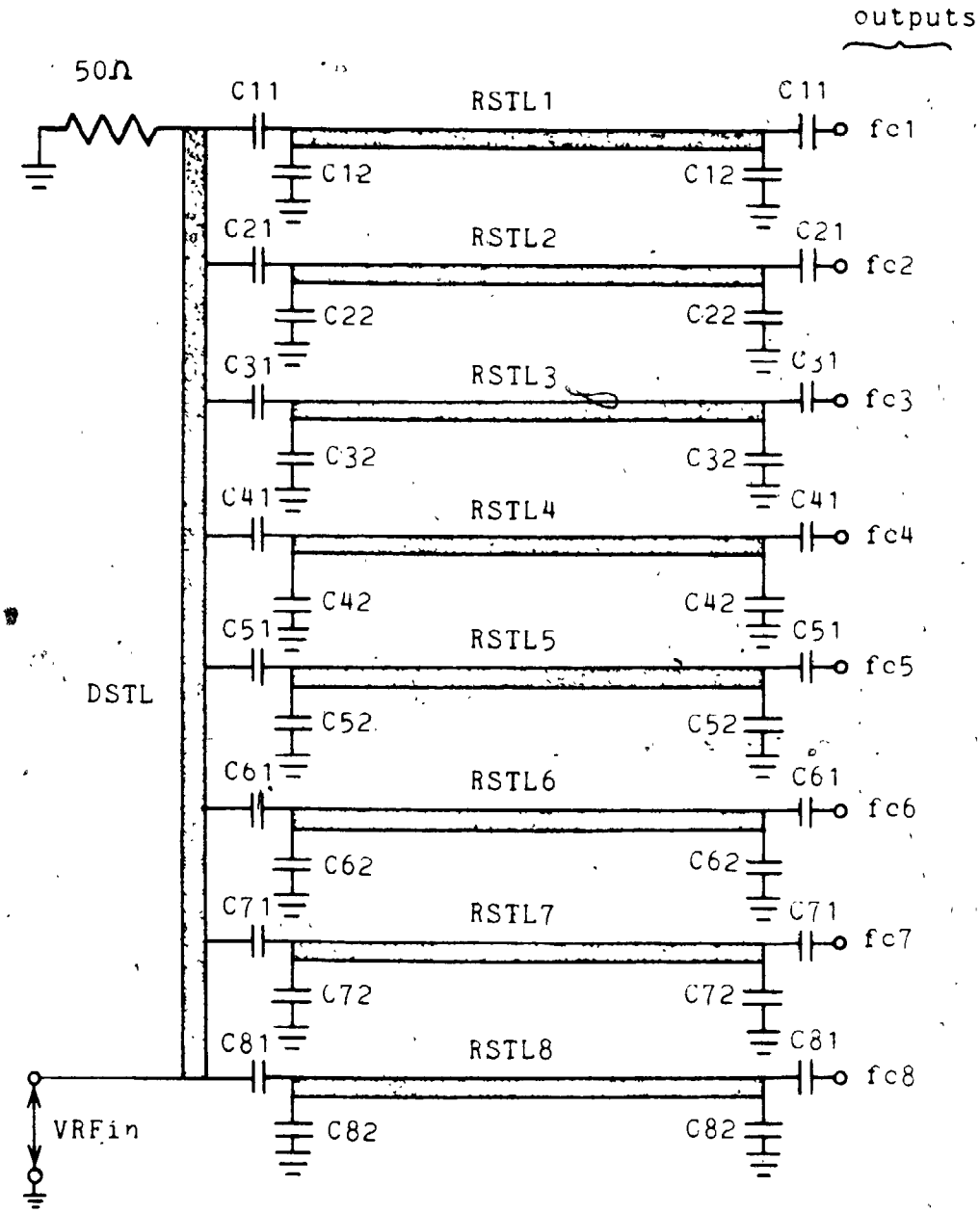
Figure 4.5 Schematic of second section of front-end.

4.3 Filter Banks and Channel Filters

The filter banks follow the front-end module of the MCSA and contain the 64 channel filters. The input to the filter banks comes from the 4-way power splitters of the second section of the front-end module. The general configuration of the filter bank is shown in figure 4.6 with table 4.1 listing the component values for the eight filter banks. The following is a detailed description of the filter banks.

Each of the eight filter banks contain eight transmission line channel filters. The filter bank was constructed on a double-sided copper clad printed circuit board (epoxy-fiberglass laminate, G-10). The transmission line strips were printed on one side of the board with the reverse side being copper clad to provide a ground plane. The filter bank board was enclosed in a shielded box that was machined from 4.76 mm (3/16 in.) utility grade aluminum sheeting. Around the perimeter of the board, brass shim stock tabs were soldered for good electrical contact with the walls of the box. Access holes were provided in the side panels to allow for external adjustment of the trimmer capacitors on the transmission line filter.

Referring to figure 4.6, the RF signal enters the filter bank and propagates along the distributor strip transmission line (STL) which is terminated in its



Refer to table 4.1 for component values.

STL - strip transmission line
DSTL - distributor STL
RSTL - resonant STL

Figure 4.6 Filter bank structure.

Table 4.1 Filter bank components.

Centre Frequency (MHz)	STL length (mm)	Tapping Capacitor (pF)	Shunt Capacitor (pF)
260	178	1.77	3.80
268	173	1.70	3.70
276	168	1.62	3.60
284	164	1.55	3.50
292	159	1.47	3.40
300	154	1.40	3.30
308	150	1.36	3.24
316	147	1.32	3.18
324	143	1.28	3.12
332	140	1.24	3.06
340	136	1.20	3.00
348	133	1.16	2.94
356	130	1.12	2.88
364	128	1.08	2.82
372	125	1.04	2.76
380	122	1.00	2.70
388	120	0.97	2.66
396	117	0.94	2.62
404	115	0.91	2.58
412	112	0.88	2.54
420	110	0.85	2.50
428	108	0.83	2.46
436	106	0.81	2.42
444	105	0.78	2.38
452	103	0.76	2.34
460	101	0.74	2.30
468	99	0.72	2.28
476	98	0.70	2.26
484	96	0.69	2.24
492	95	0.67	2.22
500	93	0.65	2.20
508	91	0.63	2.18

characteristic impedance of 50 ohms. The distributor STL was designed for a characteristic impedance of 50 ohms which is the case when the strip width is 2.54 mm (0.1 in.) (see figure 3.7). Along the length of the distributor STL, there are capacitive taps (Philips 010 foil dielectric series 010EA) to a half wavelength resonant STL. The tapping capacitors have small variable values (5 pF) and do not couple all of the signal power available into the resonant STL. This effective insertion loss is desirable since interaction between adjacent channels is minimized (Wilson, 1981). The resonant section of the channel filter is fundamentally a 'π' matching filter with the usual series inductor replaced with a half wavelength STL. The resonant STL was printed on the filter bank board as a 0.51 mm (0.02 in.) wide strip to provide a characteristic impedance of 100 ohms. The length of the strip varies according to the required centre resonant frequency (see table 4.1). Two trimmer capacitors (5 pF) were placed in shunt at the ends of the resonant STL to effectively adjust the electrical length of the STL. The output tapping capacitor couples out the signal into a 50 ohm STL which carries the signal to one of the eight miniature BNCs on the output of the filter bank.

The filtered signals on the output of the filter bank are carried by coaxial cables (RG-174) to receivers located inside the receiver modules for detection.

4.4 Channel Receiver

The radio frequency channel receiver follows the the filter banks and receives the signal from one of the eight channel filters of the filter bank. The channel receivers were assembled into groups of four receivers with a common local oscillator frequency. The four receivers along with four synchronous detectors, a frequency multiplier, and a module interface were mounted on an aluminum shielding plate to become one of sixteen receiver modules for the multichannel spectrum analyzer (see figure 4.7). The following is a detailed description of the implementation of the channel receiver.

Figure 4.8 is a schematic diagram of the RF receiver used in each of the 64 channels of the MCSA. All of the receivers are identical in design and construction since they all share a common 8 MHz wide IF band centred at 64 MHz. However, each receiver has a different RF and local oscillator input required to translate the signal frequency into the IF band.

Each receiver was assembled on a 5. x 10. cm double-sided epoxy-glass (G-10) printed circuit board and housed in a diecast aluminum alloy box (Hammond Series 1590B, 11. x 6. x 2.5 cm). These boxes have an interlocking flanged lid with self-tapping screws, no sharp corners and provide adequate shielding for frequencies under 1 GHz. The receiver is the most

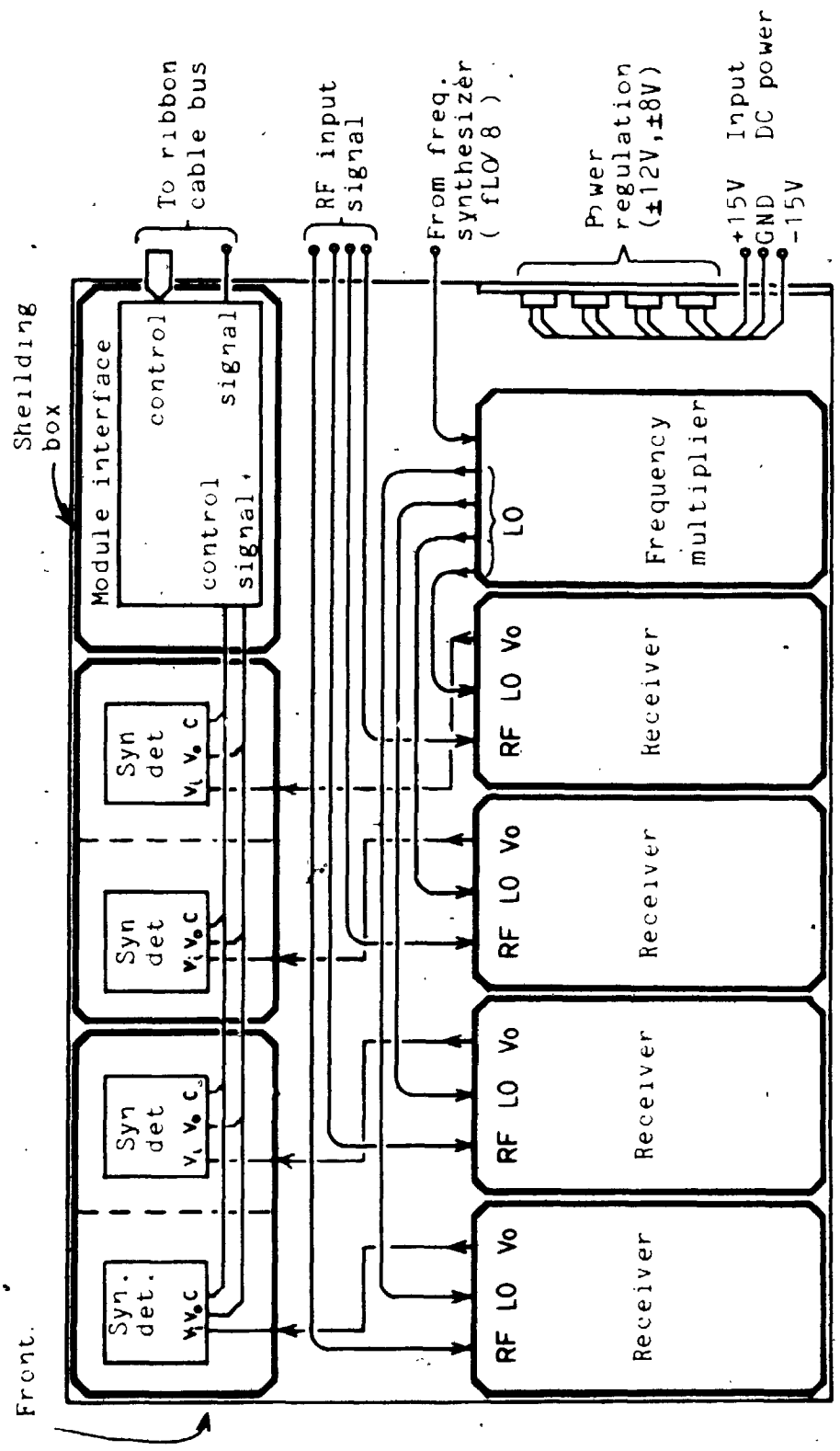


Figure 4.7 Hardware layout of the receiver module.

sensitive part of the system and therefore, a great deal of care was taken to provide for the most effective shielding possible.

All conductors entering the receiver boxes were properly decoupled to eliminate any contaminating external signals from entering the receiver box and also to prevent RF leakage from the box. The appropriate way to pass a shielded cable (RG-174 coaxial cable) through a shielding wall is by the use of industry approved connectors such as BNCs or smaller SMAs. Due primarily to space limitations and hardware cost, an alternate means was adopted. The same effectiveness in shielding was achieved by passing the coaxial cable, with some of its shielding braid exposed, through the shielding wall and compressing aluminum foil into the hole. This technique brought the exposed braid of the coaxial cable into RF contact with the box and prevented any RF signals, that might have been induced on the outside of the braid, from entering the receiver box.

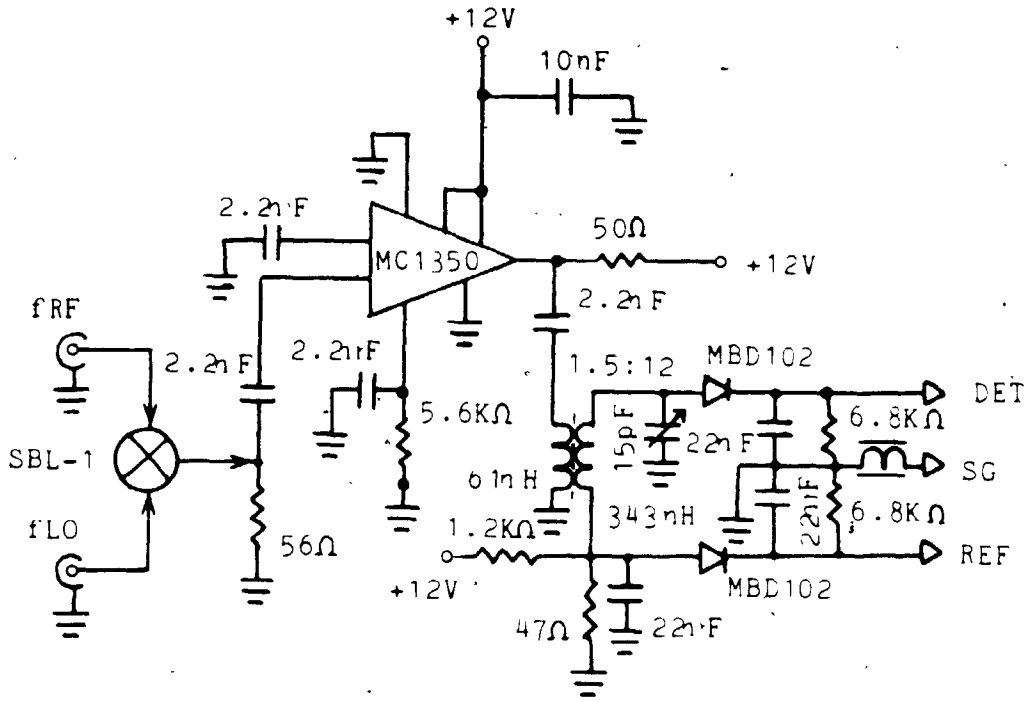
The receiver printed circuit board has a copper plane on the component side (top side). Small flexible brass shim stock tabs were used to bring the ground plane into RF contact with the interior of the receiver box. This was particularily important at the frequencies approaching 500 MHz since the combination of the box with a copper plane of the size required to construct the receiver boards makes a convenient and highly undesirable resonant

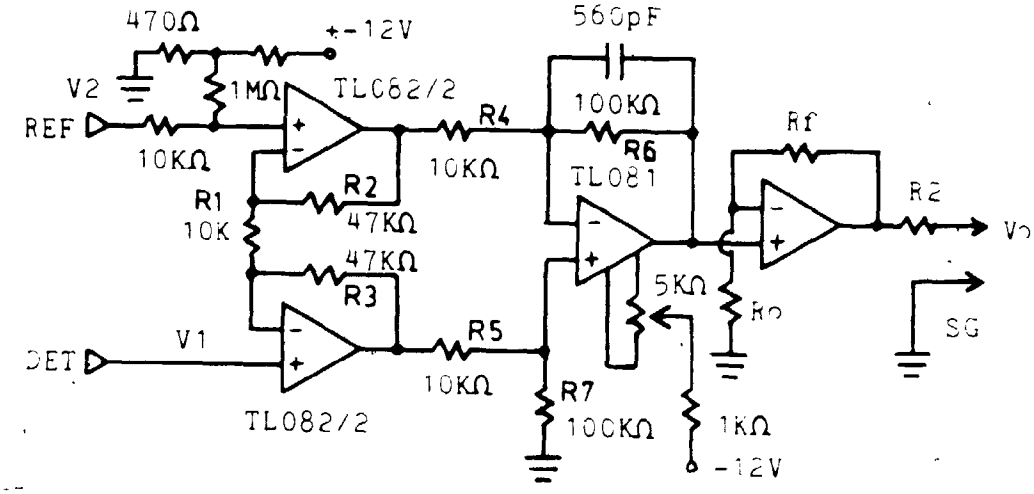
cavity. In some cases, despite the brass tabs, resonances occurred and could only be eliminated by packing aluminum foil in the spaces around the perimeter of the receiver board.

The receiver (see figure 4.8) contains an RF double-balanced mixer, an IF amplifier, an IF bandpass filter, a pair of matched Schottky diodes, an instrumentation amplifier, and a variable gain amplifier.

The double-balanced mixer is a commercial device (see Appendix C 'Mixer SBL-1' for specifications) with reliable, predictable behaviour over the frequency range of 0 to 512 MHz and good economy.

The intermediate frequency (IF) amplifier follows the mixer and is an integrated circuit (MC1350) specifically designed for automatic gain controlled IF amplification in radio and TV designs. Under matched conditions, this amplifier can provide up to 45 dB of gain at the required IF centre frequency of 64 MHz. However, in the receiver design for the MCSA, both the input and the output of the amplifier were heavily loaded with 56 ohm resistors. The IF amplifier was arranged in a single-ended configuration with minimum gain reduction. This arrangement greatly simplified the layout, reduced any inherent instability, provided a nominal 50 ohm resistive output impedance to the IF transformer, and achieved 16 dB of gain. The IF amplifier also serves as a buffer that isolates detector diode from any possible feed-through of the RF signal or





$$Vo = \left(1+\frac{Rf}{Ro}\right)\frac{R6}{R1R+}\left(R1+R2+R3\right)\left(Vdet-Vref\right) = 104\left(1+\frac{Rf}{Ro}\right)$$

where $R6/R4 = R7/R5$

Figure 4.8 Schematic of channel receiver.

the local oscillator.

Following the IF amplifier, there is an IF bandpass filter centred at 64 MHz with a bandwidth of 8 MHz (at 3 dB). The design of the filter was based on a single tuned transformer which provides both the bandpass response and the impedance matching to the detector diode. The input impedance of the Schottky hot-carrier detector diode (MBD102), when forward biassed for square-law detection (20 μA), has been found to be 2600 ohms (Wilson, 1981). The transformer coil former (Cambion) is constructed of a polypropylene material with a ferrite core (carbonyl TH) optimized for the 2.0 - 40 MHz frequency range. Operating the ferrite core at 64 MHz and beyond produced no noticeable degradation in the response of the filter.

The design of the single-tuned transformer is described in literature (Kraus, 1980). Starting from the required values for the impedance, frequency and bandwidth; the inductance, capacitance and coupling factor were calculated (R_p = 50 , R_s = 2600 , f_c = 64 MHz, B = 8 MHz; L_p = 61 nH, L_s = 343 nH, C = 15.7 pF, K = 0.39). The secondary of the transformer (detector side) was tuned with a 10 pF trimmer capacitor in parallel with a fixed 10 pF capacitor (see figure 5.18). The secondary of the transformer was made part of the DC bias circuit for the two Schottky hot-carrier detector diodes (MBD102).

The detector diodes were matched at a forward bias current of 20 μA for optimum square-law performance. One of the diodes was used as a small signal detector while the other diode was used as a thermal reference. Since the two diodes are matched and at the same temperature, thermal drift of one diode will be cancelled by the other when the diode voltages are differentially amplified (Turner, 1974). The RC networks on the outputs of the detector diodes have a bandwidth of 1 KHz. The bandwidth is wide enough to pass the detected square-wave from the chopped signal. Polycarbonate, metallized film capacitors (22 nF) were used since they maintain good characteristics over a wide temperature range and are not subject to vibration noise (microphonics) which is typical of ceramic capacitors.

The differential instrumentation amplifier following the dual detectors was assembled out of BIFET operational amplifiers (MC34001, MC34002) and matched resistors. BIFET op-amps are wideband, have fast slew rates, low input bias currents, low input offset currents, high input impedance and are economical. The analysis of the instrumentation amplifier is straightforward with the voltage transfer function shown in figure 4.8 (Stout, 1976). All the similar resistors were matched so that all the gains associated with the reference and the detector voltage would be the same. The nominal voltage gain of the amplifier is 104. Coarse offset adjustment can be

accomplished by changing resistors in the reference voltage arm circuit. Fine offset adjustment can be accomplished from outside of the shielded box by accessing a 5 K potentiometer at the opposite end of the receiver to the RF inputs. The access holes for the four receivers can be reached from the bottom side of the receiver module.

A variable gain amplifier follows the instrumentation amplifier and is used to balance the gain of a receiver against other receivers. The maximum output voltage swing of the receiver is 0 - 12 V. The output of the receiver is carried by twisted wire pair to next stage of processing, the synchronous detector.

4.5 Synchronous Detector

The schematic for the synchronous detector is shown in figure 4.9. The construction and design of all the synchronous detectors are the same. Two detector circuits were housed in the same diecast aluminum shielding box. The following is a detailed description of the implementation of the synchronous detector.

Shielding the detector circuits was necessary because the associated digital electronics can be a strong source of EMI. Digital signals, in general, are characterized by large voltage square-wave signals with fast transitions and large current surges. This can produce EMI that can be induced in the relatively low-level RF signal lines. In addition, contamination of the local oscillator by the digital signals would appear as modulation in phase with detection process of the synchronous detector.

The synchronous detection process rejects all contaminating signals that are asynchronous with the detector; however, it preserves synchronous signals. Synchronous contaminating signals, such as the control signals, will produce an incorrect detector output. Consequently, all digital control lines were shielded and confined within shielding boxes. In addition, all ribbon cables carrying control lines had ground lines placed between all signal and control lines. Current surges were minimized by the exclusive use of CMOS digital and MOS

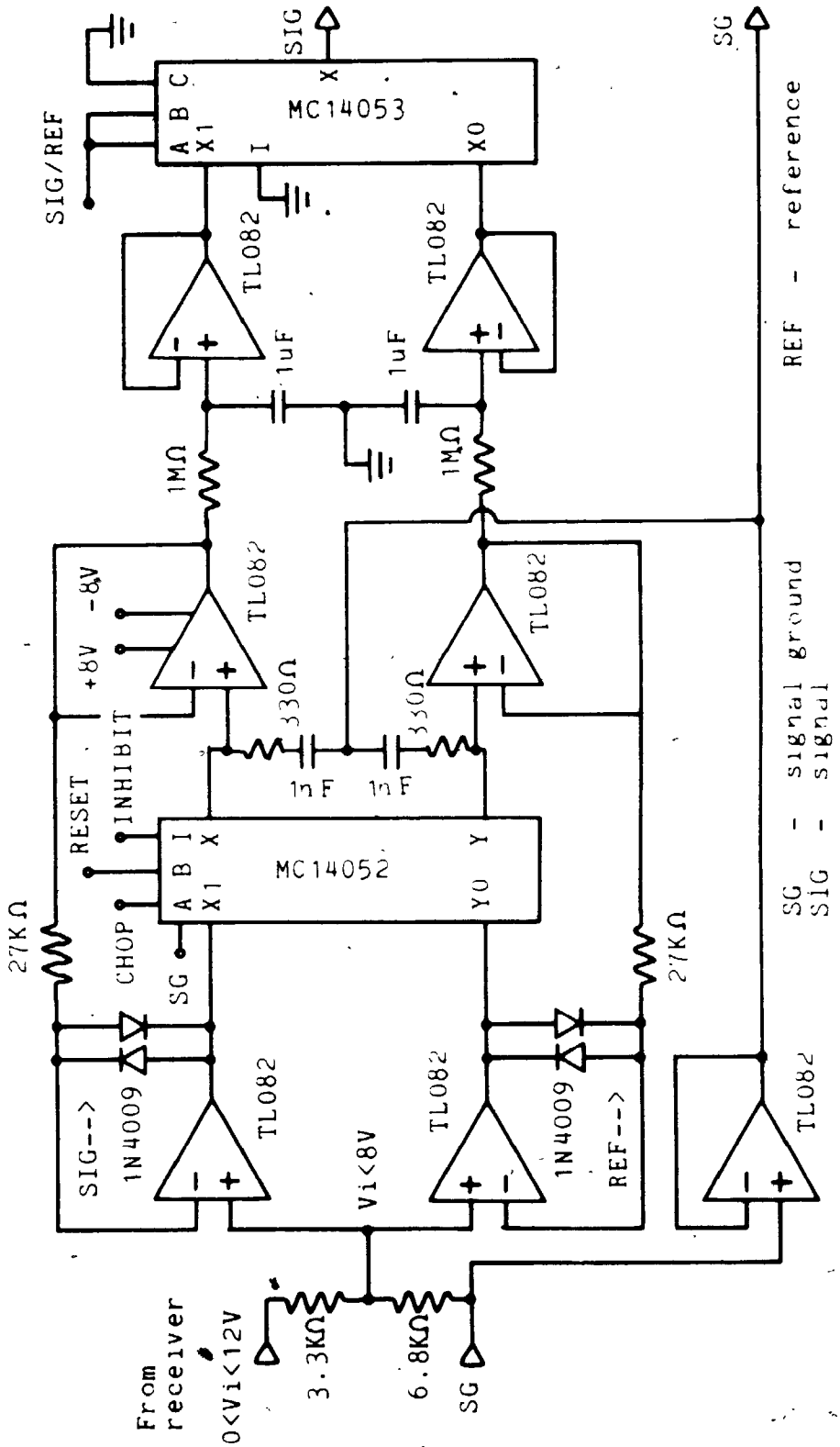


Figure 4.9 Synchronous detector schematic.

linear integrated circuits.

The input signal to the synchronous detector passes through a resistor voltage divider network to reduce the maximum voltage swing by 33% (0 - 8 V). The input signal is required to work within the supply voltage range (± 8 V) of the detector. The supply voltage range permits safe operation of a mixture of integrated circuit families (CMOS digital, MOS linear).

The two lines from the receiver, signal and signal ground, enter the synchronous detector as a twisted wire pair. The signal ground is buffered by a voltage follower to provide a voltage reference for the synchronous detection process. The ground reference is isolated from the digital control ground to eliminate problems associated with common ground paths. The ground reference is used until the processed signal reaches the analog-to-digital convertor in the data acquisition system.

The receiver signal is connected to on the inputs of two sample-and-hold (SH) circuits. One SH synchronously samples the input signal for the RF portion and the other SH synchronously samples for the reference portion.

The SH circuits were constructed from two BIFET voltage followers separated by a CMOS switch and a hold capacitor. The input voltage follower buffers the input signal and charges the hold capacitor when the CMOS switch is closed. Clamping diodes are required on the output of

the voltage follower to prevent voltage swings, which would reduce response time, when the CMOS switch is opened and closed. The CMOS switch (MC14052) is operated by a number of control lines. The CHOP control line is the synchronizing control signal and is phase-locked to the control signal for the optical chopper. The RESET control line resets the synchronous detector by discharging the hold capacitor to ground. The INHIBIT control line electronically gates the CMOS switch off during the passage of a transition in the chopped input signal. The detector is inhibited at the transition to prevent the associated edge effects of the chopper blade. The edge effects will be manifested as large transient spikes at the leading and trailing edge of the chopped signal.

Following the CMOS switch a hold capacitor (1 μF) acquires and preserves the sample voltage. The resistor (330 ohms) on the hold capacitor controls excessive current surges and in combination with the hold capacitor, has a time constant 2 μS. Thus, the sample-and-hold can respond very rapidly to signal changes.

After the hold capacitor, there is a second voltage follower which buffers the hold voltage on the capacitor. The voltage follower drives a large time constant integrator where all of the analog integration takes place. It is made up of a 1 MΩ resistor and a 1 μF capacitor with a time constant of 6.3 seconds. Further analog integration is unnecessary since digital

integration can be done more simply by application software after the signal has been digitized. The large time constant integrator is buffered by a voltage follower whose output enters a CMOS switch (MC14053) that operates as a data selector.

The sampled and integrated voltages corresponding to the RF signal and reference signal pass through the data selector (MC14053), one at a time, as determined by a SIG/REF control line.

The outputs of the four synchronous detectors on one receiver module enter the receiver module interface which controls access to the module by the data acquisition system. The receiver module interface is shown in figure 4.10. The 4-bit comparator (MC14585) compares the logic level on the four module address lines (A2 - A5) against the module address. Provided that each receiver module has a unique address, only one module will be enabled when a receiver is addressed. The two least significant address lines (A0 - A1) select one of four receivers of the enabled module. Address line A6 is equivalent to the control line SIG/REF and selects either the signal output or reference output of the synchronous detector.

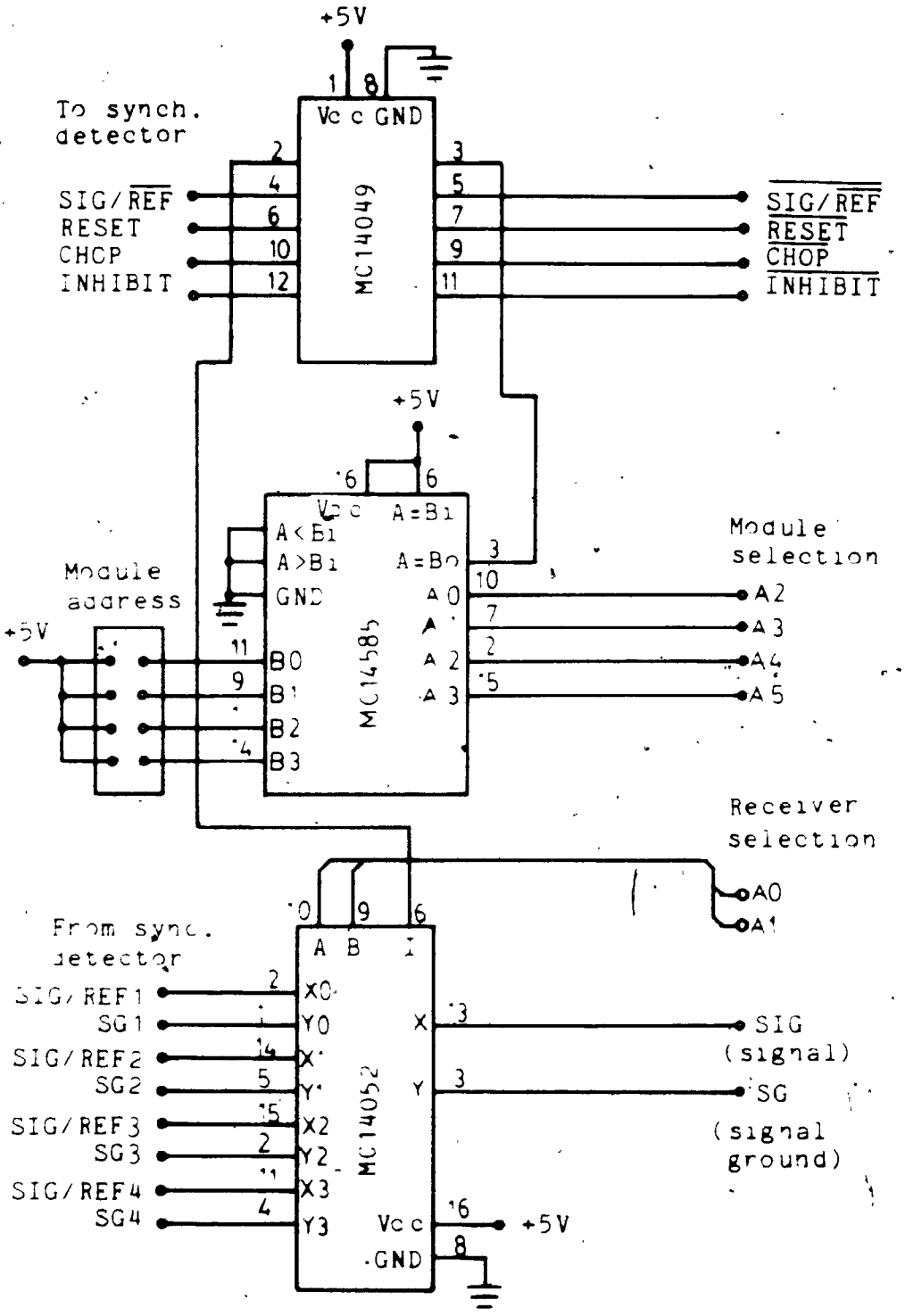


Figure 4.10 Receiver module interface.

4.6 Local Oscillator and Frequency Multiplier

Sixteen local oscillators (LO) are required for the sixteen receiver modules making up the RF portion of the multichannel spectrum analyzer. All of the LO frequencies are synthesized from a common reference frequency of 250 KHz. This comparatively low frequency is required so that digital signals are well within the working range of TTL digital devices (counters and inverters) and of CMOS devices (phase-locked loop or PLL).

The local oscillator frequencies for the receiver are synthesized in two sections. The first section, discussed here, synthesizes a frequency with PLLs and then doubles it. The next section, which is on the receiver module, takes the synthesized frequency and multiplies it by eight to generate the final local oscillator frequency required by the receivers (Manassewitsch, 1976). The schematic for the local oscillator synthesis design is shown in figure 4.11.

The reference frequency of 250 KHz is derived from a high frequency crystal oscillator running at a frequency of 32 MHz. The oscillator configuration shown in figure 4.11 is known as a Colpitts oscillator with the crystal operating in series resonance. This oscillator design is commonly used at high frequencies because it is essentially a common-base configuration, if one replaces the crystal with a bypass capacitor. The transistor,

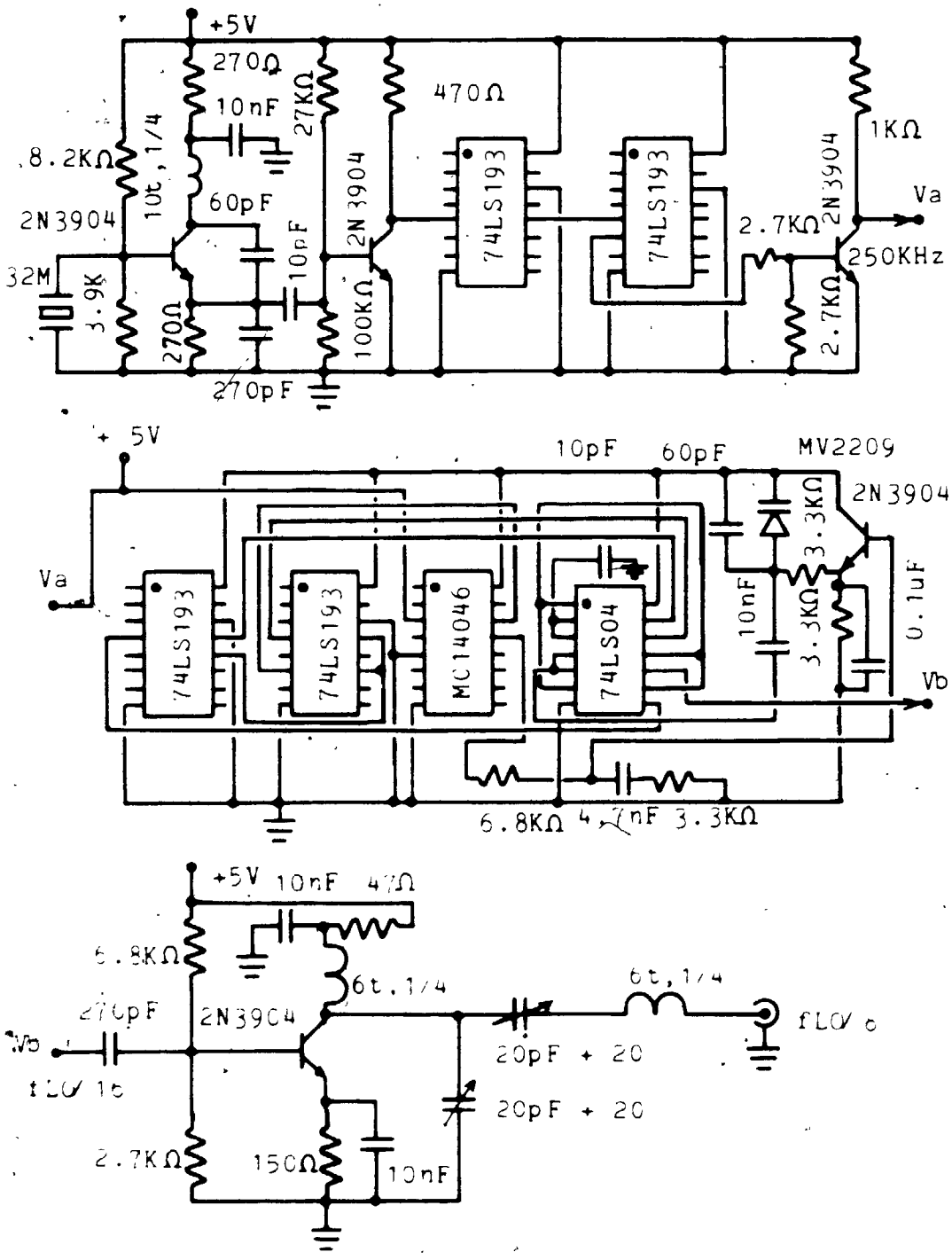


Figure 4.11 Frequency synthesizer schematic.

2N3904, provides sufficient output power and voltage swing (2 V_{pp}) from the emitter and is capable of driving low impedances of the order of 300 ohms.

The output of the oscillator is coupled through a 10 pF capacitor to filter out some harmonics and also to buffer the oscillator from the next stage. The next stage is overdriven, switching into saturation and cutoff, and produces a good symmetrical square-wave at 32 MHz to trigger the TTL counters (74LS193). The two counters are presettable binary synchronous counters that were set to divide by 128 in order to generate the 250 KHz reference signal. The output of these counters passes through a buffer amplifier that squares-up the reference signal to ensure proper triggering of the CMOS PLLs (MC14046).

The phase-locked loop (figure 4.12) consists of the phase detector II from the MC14046, a low-pass filter on the phase detector output, an emitter follower on the low-pass filter output, a varactor diode, and a TTL voltage controlled oscillator (VCO). Only phase detector II circuitry of the MC14046 CMOS chip is used since this detector will not lock onto harmonics of the VCO frequency (Blanchard, 1976). The loop filter is a second order passive low-pass filter with an emitter follower on the output to act as a buffer. Since phase detector II is nonlinear in its response to phase changes, there is no structured design procedure for determining the loop filter components. However, if one designs for the linear

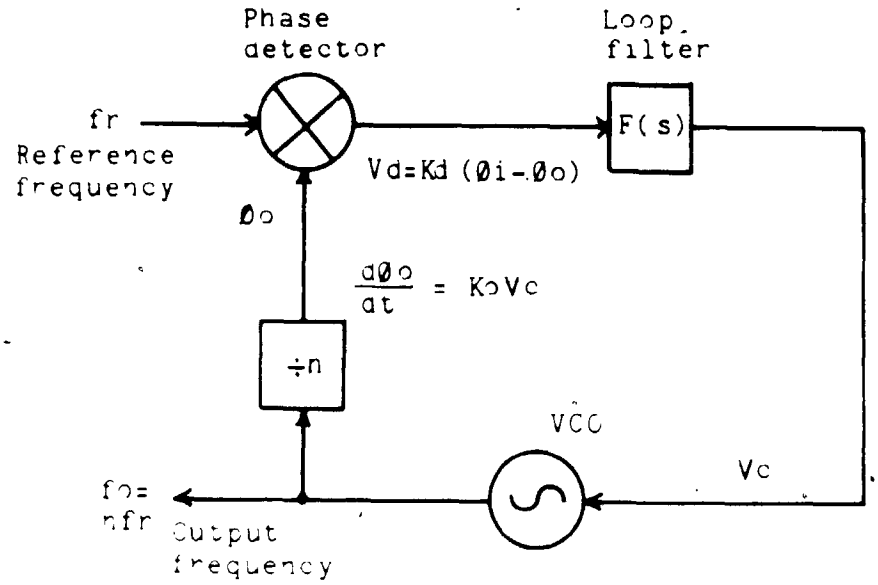


Figure 4.12a Theoretical frequency synthesizer

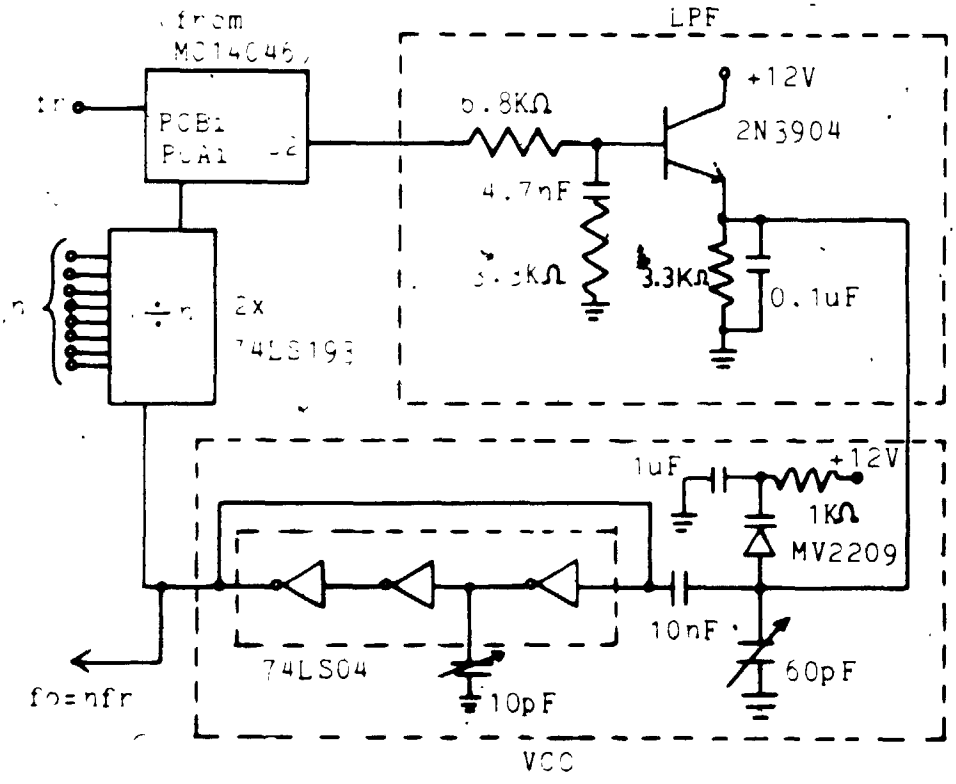


Figure 4.12b Frequency synthesizer implementation

phase detector I and determines the loop filter's components, one will find these values work equally as well with detector II without any problems with harmonic lock-up (Best, 1984).

The voltage controlled oscillator (VCO) consists of a three inverter ring from a TTL quad inverter (74LS04) (see figure 4.12b). A varactor diode (MV2209) in parallel with a 60 pF trimmer capacitor provide the electronic variable capacitance needed to adjust the VCO frequency. The output of the VCO is divided by a programmable counter (74LS193) whose output goes to the phase detector where it is compared with the reference frequency. When the PLL has locked up, the VCO frequency is some multiple of the reference frequency in the range of 20.25 MHz to 27.75 MHz in 0.25 MHz steps. Appendix A details the calculation of the loop filter's components.

The output of the synthesized frequency is taken from the VCO and is doubled by a frequency multiplier built as an overdriven transistor amplifier. Since the input signal is quite large (4 V_{pp}), there is no need for matching the signal to the base of the transistor (2N3904). The output matching network selects the second harmonic and rejects all other harmonics generated by the nonlinear operation of the transistor. The magnitude of other harmonics can be reduced by adjusting the value of coupling capacitance on the input to the frequency doubler.

The frequency multiplier in the receiver module is the next section in generating the final local oscillator frequency required by the receivers. Since all of the generated frequencies were large signals over 320 MHz, careful consideration was given to shielding. There must be no leakage from the frequency multiplier box since the local oscillators are strong enough to saturate the square-law detector of the receiver if it gets past the IF stage. The shielding practices used for the receiver were adopted for the frequency multiplier. All power lines were heavily decoupled with capacitors and ferrite beads, and separate regulators and power lines were used. Brass tabs were used on the printed circuit board around its perimeter to bring it in good electrical contact with the diecast aluminum box. Aluminum foil was utilized to fill spaces between the PCB and the box wall to eliminate circulating RF fields that might have set up parasitic resonances.

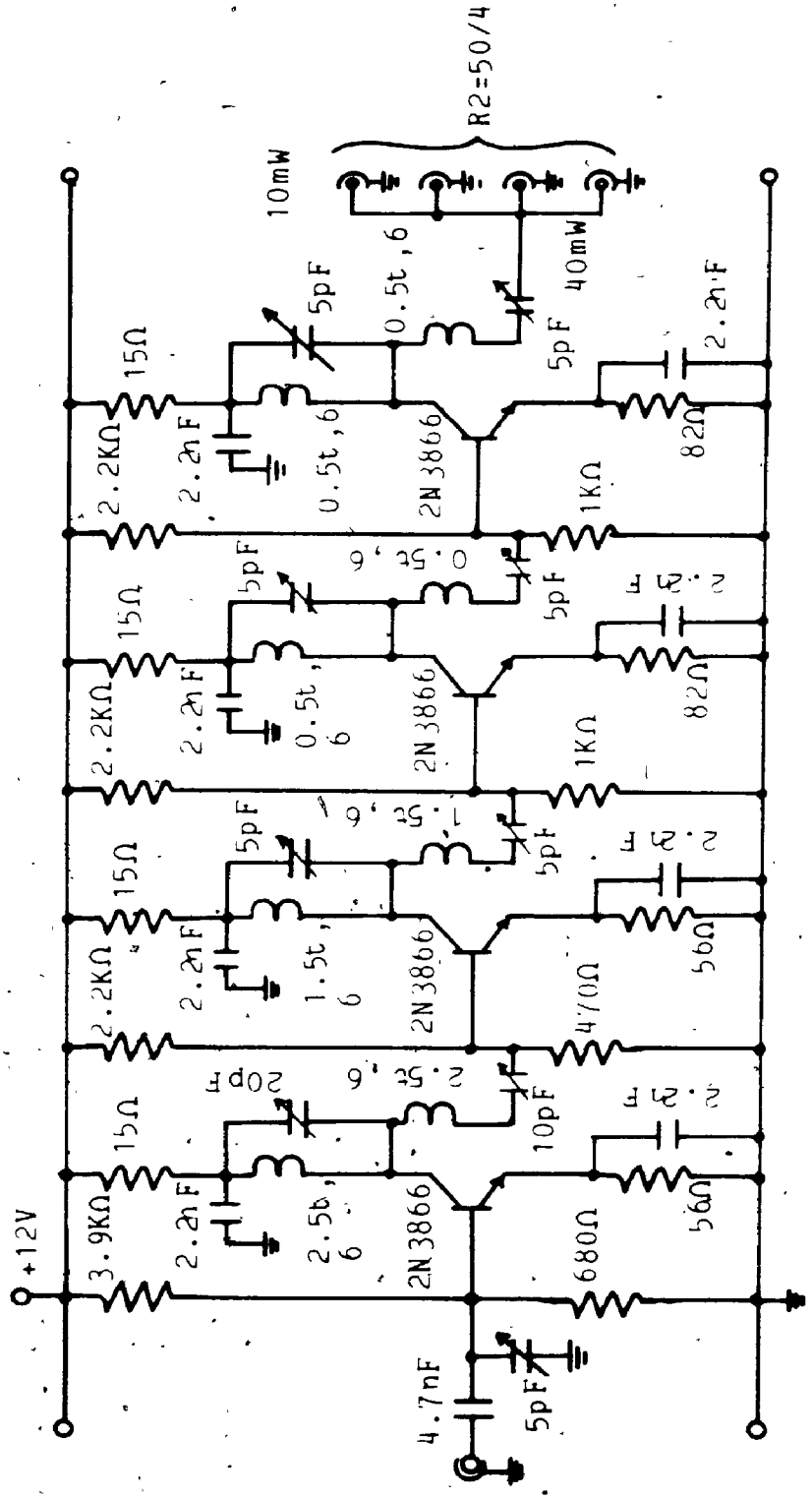
The RF frequency multiplier consists of four RF medium power transistors (2N3866) with a unity gain-bandwidth product (f_T) of 1 GHz at a current of 40 mA. The first three transistors are frequency doublers to obtain the required multiplication by eight. The last stage is a buffer amplifier that is capable of driving four mixers of the receivers in parallel, which is an effective load impedance of 12.5 ohms. Each mixer requires at least 7 dBm local oscillator power to ensure

good switching action for its internal diodes. Thus, the output amplifier must provide at least 13 dBm (20 mW) of power into 12.5 ohms.

The schematic for the frequency multiplier is shown in figure 4.13. Since sixteen of the circuits must be made, identical circuit layouts were adopted for all of them with facility to adjust some of the reactive components from the top side of the circuit without requiring removal of the printed circuit board. Each transistor stage is a common emitter stage with the interstage matching networks being a combination of a parallel and a series resonant circuit.

The transistors are driving each other with a large signal in order to generate harmonics from the nonlinear response of a transistor to large signals (DeMaw, 1982). Analysis of the large signal behaviour of transistors at radio frequencies is difficult and of limited value due to a high dependence on input signal levels. However, small signal Y-parameter analysis may be used to generate starting values for matching networks that can be easily adjusted for best performance.

Y-parameter analysis gives expressions for stability (Linvill stability factor C), transducer gain, and optimum load and source admittances. These expressions are given in Appendix B (Hejhall, 1978). The optimum load and source admittances for the 2N3866 at several frequencies are shown on a Smith Chart in figure 4.14.



note: inductor specification
ie., 0.5t,6 = 0.5 turns,
6mm diameter

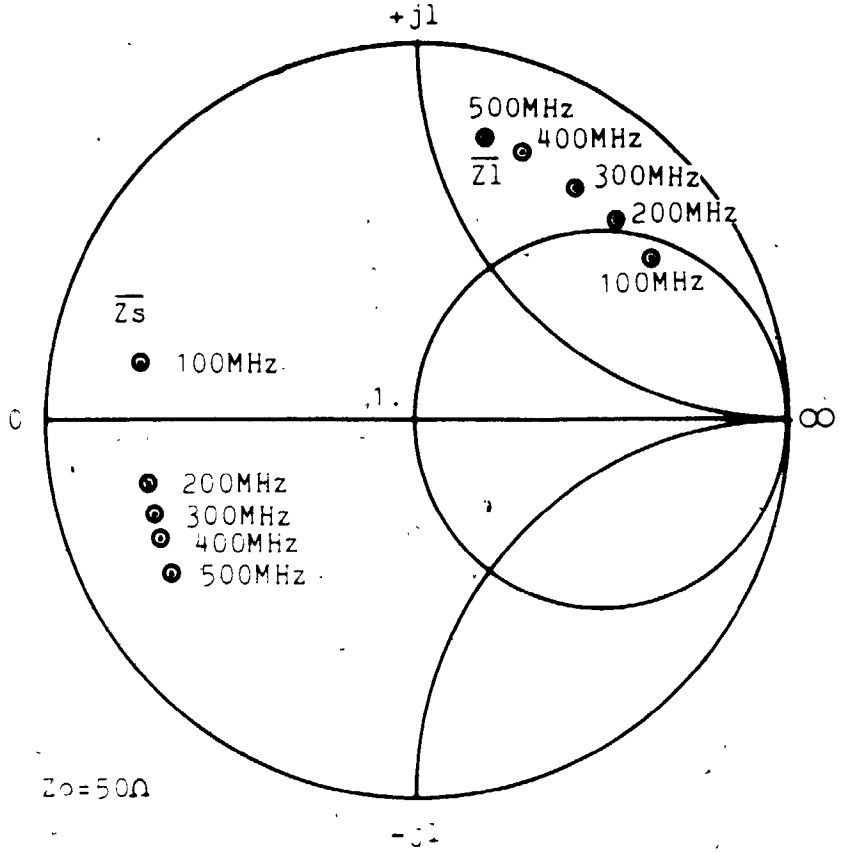
Figure 4.15 Frequency multiplier schematic

The matching networks required between the transistor stages must conjugately match the input and output for maximum power transfer, and must provide narrow bandwidth at the desired frequency to minimize the transfer of undesired harmonics to the next stage.

Most of the impedance matching was performed graphically on a Smith Chart. Figure 4.15 shows graphically an impedance matching solution on a combined impedance-admittance chart for one of the frequency multiplier transistors (2N3866) at 101 MHz. The quality factor, Q, of the circuit is largely determined by the parallel tuned circuit on the output (collector) of the transistor. For a parallel tuned circuit, the Q is given by:

$$Q = RwC = \frac{R}{wL} \qquad 4.1$$

The larger the Q of a circuit, the narrower the bandwidth will be and hence, the cleaner the output will be from a transistor generating harmonics. In practice, with radio frequency electronics, high Q's are difficult to obtain as the Q of the reactive components themselves become significant. The circuits for the frequency multiplier were designed with this in mind by incorporating variable components that would overlap the lines of constant resistance and conductance as shown in figure 4.15.



100MHz : $\overline{Zs}$ = 0.14-j0.04, $\overline{Zl}$ = 1.71+j2.56

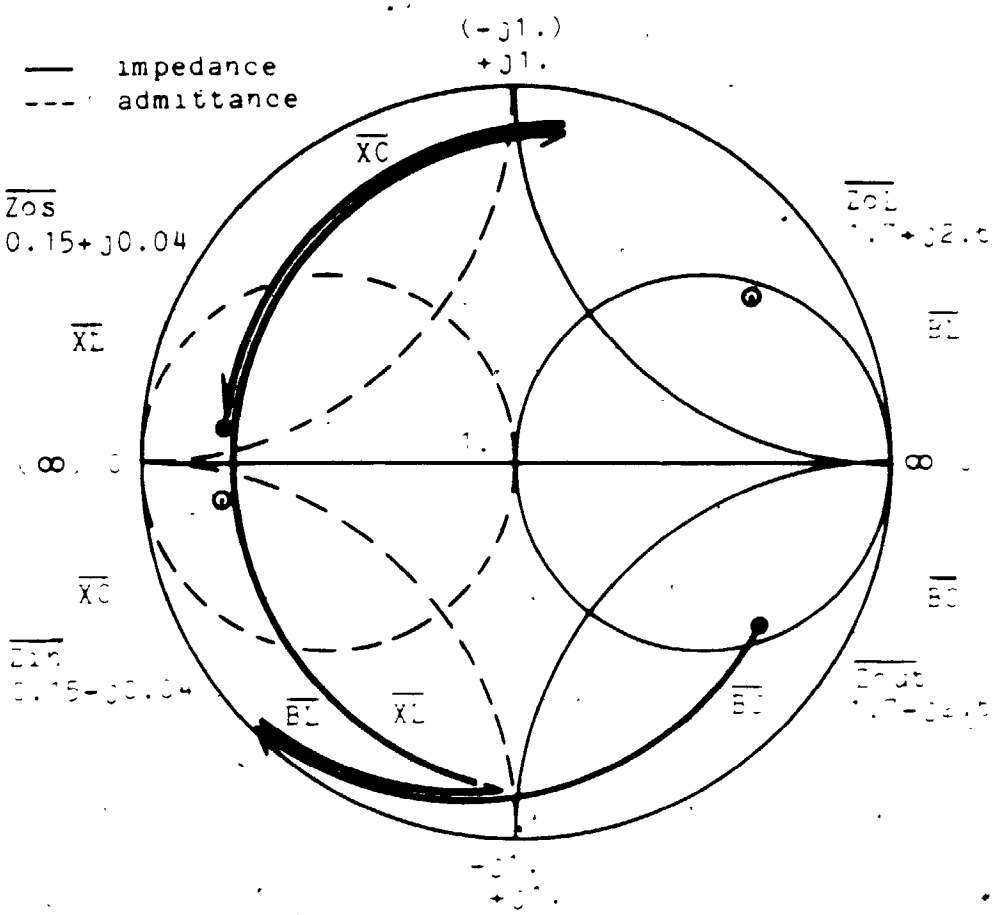
200MHz : $\overline{Zs}$ = 0.16-j0.06, $\overline{Zl}$ = 1.22+j1.93

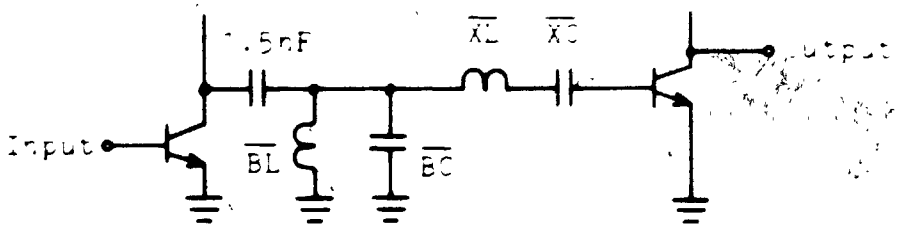
300MHz : $\overline{Zs}$ = 0.17-j0.12, $\overline{Zl}$ = 0.73+j1.58

400MHz : $\overline{Zs}$ = 0.18-j0.18, $\overline{Zl}$ = 0.59+j1.30

500MHz : $\overline{Zs}$ = 0.15-j0.25, $\overline{Zl}$ = 0.43+j1.17

Figure 4.14 Optimum load and source impedances for 2N3866.





101MHz	BL = 0.9	L = 88nH
	BC = 2.0	C = 64pF
	XL = 2.0	L = 159nH
	XC = 1.0	C = 32pF

Figure 4.15 Impedance matching of a 2N3866 on a combined impedance/admittance Smith-chart.

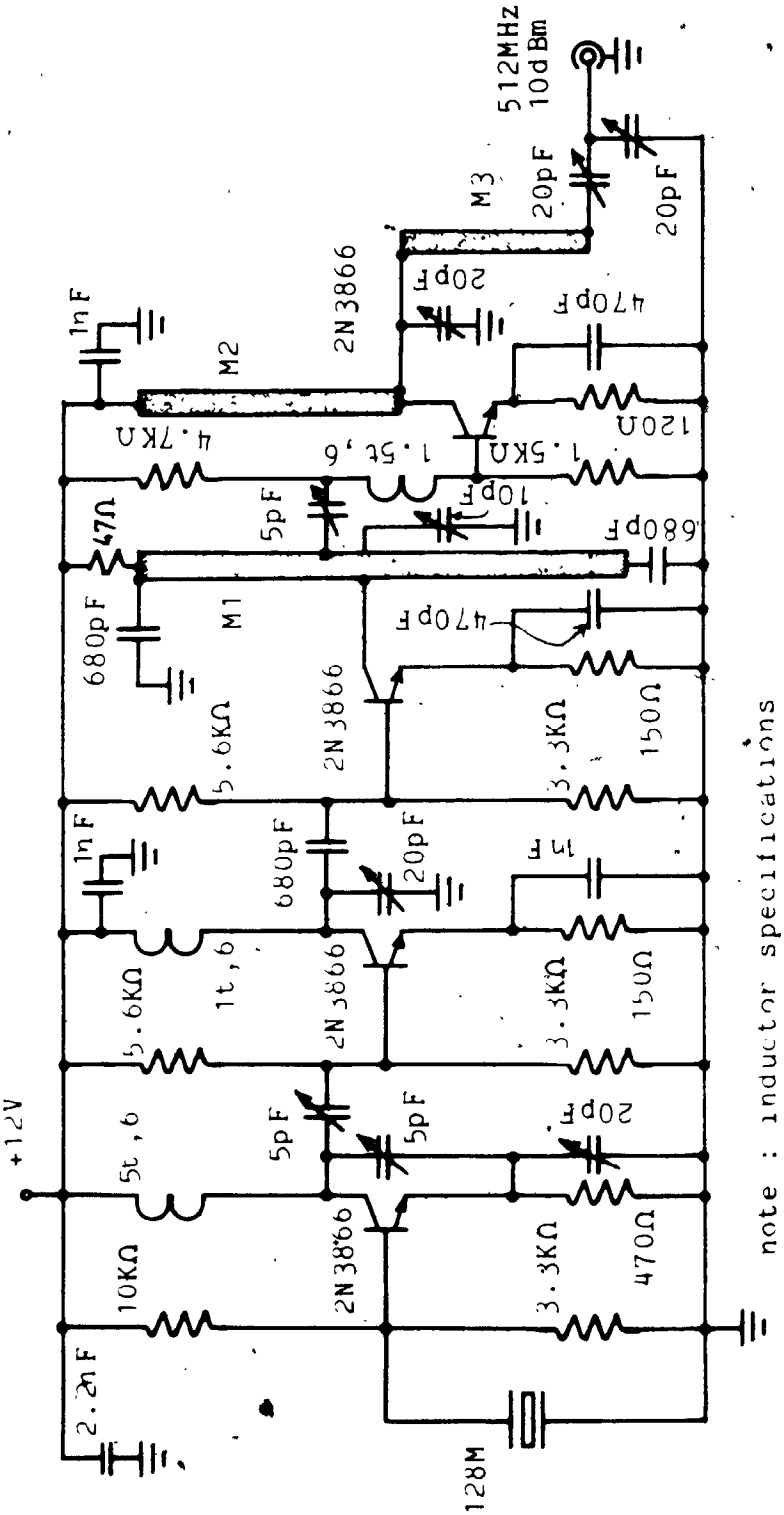
4.7 Front-end Local Oscillator

The local oscillator in the front-end of the multichannel spectrum analyzer shifts the lower half of the input spectrum from 0 - 256 MHz up to 256 - 512 MHz. The following describes in detail the implementation of the front-end local oscillator.

Great care was taken in designing a well shielded box, since as pointed out earlier, the local oscillator is a source of large signals not only at the oscillation frequency but also at all harmonics of it. Brass shim stock tabs were used on the circuit board perimeter to bring it in good electrical contact with the shielded box.

The schematic diagram for the local oscillator is shown in figure 4.16. The circuit consists of a crystal oscillator (128 MHz) and a quadrupler to multiply the frequency up to 512 MHz. The crystal oscillator was designed in the Colpitts configuration with the crystal operating in series resonance.

The oscillator transistor (2N3866) was biassed for 5 mA collector current and with 2.3 V drop across the emitter resistor. The collector current was designed to be at a higher level than the more typical 1 - 2 mA to ensure sufficient gain at high frequencies. The emitter resistor voltage drop was designed higher than usual to ensure good thermal compensation of the transistor. Transistors that are thermally compensated by negative



note : inductor specifications
ie., 5t,6 = 5 turns; 6mm diameter

note : M1 = 50 strip transmission line, 2.5x40mm
M2 = 50 strip transmission line, 2.5x28mm
M3 = 50 strip transmission line, 2.5x51mm

Figure 4.16 Front-end local oscillator schematic.

feedback from the emitter typically have 2 - 3 V across the emitter resistor.

The quadrupler circuitry follows the oscillator and the first stage is a frequency doubler. The signal from the oscillator is coupled into the doubler by a 5 pF trimmer capacitor. Optimum matching is not required here since the oscillator has sufficient signal power (3 V_{pp}). The small coupling capacitance tends to isolate the oscillator from the doubler which is generating a large number of harmonics. The output of the doubler is a high Q parallel tuned circuit for selecting the second harmonic and rejecting other frequencies. The doubler was designed for a high collector current of 25 mA with 3.75 V across the emitter resistor.

The next stage is a second frequency doubler biassed at the same level as the first one. A strip transmission line (STL) was used as the resonant circuit on the output of this transistor. The STL was designed for a characteristic impedance of 50 ohms and was printed as a strip (2.5 x 51 mm) on double-sided printed circuit board. The STL was capacitively shorted to ground at both ends. It has an input tap 20 mm from the lower end of the strip and an output tap 25 mm from the lower end.

The STL is tuned at the input tap with a 10 pF trimmer capacitor to ground. The STL behaves as inductor rather than a transmission line since it is much less than a quarter of wavelength (about 80 mm at 512 MHz on a

printed circuit board) (Wilson, 1981). The STL solves the problems that coils have at frequencies around 512 MHz. At these frequencies coils become unrealistically small, consisting only of half turns of wire above a ground plane. The coils tend to inductively couple with other components which often leads to unexpected resonances and parasitic oscillations The STL solves these problems by keeping the electromagnetic fields well confined to the printed circuit board.

The output tap on the STL is closer to the shorted end than the input tap because this is a lower output impedance point required to drive the buffer amplifier. The input coupling is a series tuned circuit resonant at 512 MHz. The buffer amplifier is biassed for 18 mA in the collector and 2.2 V across the emitter resistor. The output stage of the buffer was designed with two STLs which behave like inductors. The first STL is in parallel resonance with a collector 20 pF trimmer capacitor and the second STL is in series resonance with a 20 pF trimmer capacitor.

The output of the frequency multiplier was designed to drive a mixer (SRA-1) in the first section of the front-end module of the MCSA at a power level of 7 dBm. The output can be adjusted by detuning the output matching networks slightly. Larger adjustments in output power can be accomplished by changing the emitter resistor in the buffer amplifier. Generally, output power will increase

as the collector current increases since the gain of the transistor is slightly dependent on collector current.

4.8 Microcomputer System

A microcomputer system was developed for the control of the multichannel spectrum analyzer. It was designed to perform the functions of system control, data acquisition, data collation, data processing, and data transfer. The details of the implementation of the system are briefly described in the following.

The microcomputer system consists of a CPU board, an input/output (I/O) board, a random-access-memory (RAM) board, a read-only-memory (EPROM) board, a controller board, an analog-to-digital conversion (ADC) board, and a timer (RTC/PTM) board. All of these boards use a standard bus known as the STD bus.

The STD bus was developed in 1978 by Mostek Corp. and Pro-Log Corp. to be a compact, modular, general-purpose bus structure for microcomputer systems. The STD bus is economical and can support any 8-bit microprocessor presently available. The bus is compact with each card measuring 11.4 x 16.5 cm (4.5 x 6.5 in.).

The concept of the STD bus is based on a simplified bus connection scheme. The backplane bus handles communications between boards only and is independent of the type of board or CPU in use. Other system interconnections that are required, take place on a second set of connectors on the boards themselves.

The adoption of the STD bus as a formal industry standard is presently under cosideration by the IEEE and has the designation IEEE P691.

The STD bus consists of four sections: power supply lines, 8 bi-directional data lines, 16 address lines, and 26 control lines. The control lines include control of memory, I/O, the bus itself, auxilliary power supply, interrupts, and CPU control.

Appendix E contains diagrams and tables for the microcomputer system. Table E.1 shows the pin designation for the STD bus.

4.9 Central Processing Unit Board

The microcomputer system is controlled by a central processing unit (CPU) board which uses Motorola's MC6809 microprocessor.

The layout and schematics for the CPU board are shown in figures E.2, E.3a, E.3b, and E.3c. The CPU board can be configured for 8K of EPROM (NMC2732) and 8K of CMOS RAM (HM6116lP-4) for a total of 16K of on-board memory. The CPU board may be accessed two ways; one is through the STD bus and the other is through the VIA port (SY6522, versatile interface adapter). For general purpose applications the VIA socket may be bypassed with wire jumpers allowing access directly to the microcomputer bus. Bus control is handled by both hardware and software. Software can change bits in bus registers which will control the action of the bus hardware logic when the appropriate signals on the bus occur.

The configuration of the CPU board may be altered by changing the wire-wrap connections on the jumper blocks (see the above figures). Three levels of interrupts are possible by the use of jumper block J1. A second jumper block (J2) allows the on-board memory to be switched between 2716, 2732, and 6116 memories. The schematic shows a typical setup for two 2732 EPROMs and four 6116 RAMs (note: 2732 EPROMs are only allowed in the two sockets closest to the MPU). The third jumper block (J3)

is used to designate the CPU's name or number. This is useful in some software applications where the operating system needs to know what hardware resources are available and how the system is configured. Jumper block J4, allows relocation of 2K blocks of memory without physically changing EPROMs. This is particularily useful in software development.

Bus control is performed by two registers at the same address location (address $FFDX, where X is any 4-bit number). One register is a read-only register and the other is a write-only register. The read-only register (74LS374) contains information on the bus status and the CPU's name. The write-only register (74LS174) enables or disables the bus and sends bus control signals (see figure E.4)

The CPU board implemented for the MCSA handles all I/O by the VIA socket. The VIA connector is linked by ribbon cable to an I/O board which resides on the STD backplane. Bypass connections are required for the VIA socket and are shown in figure E.4.

4.10 Input/Output Board

The input/output (I/O) board contains three serial ports, two parallel ports, and priority interrupt encoding.

The I/O board was designed to conform to the STD bus standard but only in physical dimensions and power supply connections. The hardware logic requires 0 and +5 V, and the serial line drivers require ±12 V. Communication between the I/O board and the CPU board takes place by a 26-pin connector on the I/O board and the bypassed VIA port on the CPU board. The schematic for the I/O board is shown in figure E.5a and E.5b.

The I/O board is accessed by addressing any location in the range $FFC0 - $FFCF (note: the prefix symbol, $, indicates that a hexidecimal number follows). The parallel ports (PIA: MC6821) occupy addresses $FFC0 - $FFC3 and $FFC4 - $FFC7. The serial ports (ACIA: MC6850) occupy addresses: $FFC8 - $FFC9, $FFCA - $FFCB, and $FFCC - $FFCD. The interrupt encoder (MC14532) occupies address $FFCF. Address location $FFCE is unused (see figure 4.17).

Serial communication uses the RS-232C standard of which only five lines are implemented: TXD, RXD, RTS, CTS, and DCD. The serial device is an asynchronous communications interface adapter (ACIA: MC6850) which was designed to interface with the MC6800 family of hardware.

The rate of serial communication is set by a baud rate generator (MC14411) which supplies a few frequencies that can be selected by jumper block J7 (see figure E.4b).

Parallel communication takes place by the use of peripheral interface adapters (PIA: MC6821). These devices provide a universal means of interfacing peripheral equipment to the microcomputer system. They have been used extensively throughout the development of the MCSA.

The priority interrupt encoder (MC14532) is very useful for vectored interrupt handling of I/O devices. Interrupt lines from each of the I/O devices (7 lines) are encoded to produce a 3-bit number. This number can be read and used as an offset in various types of addressing modes. The interrupting device is known immediately without the need for time-consuming polling of I/O devices. In the event that a multiple interrupt occurs simultaneously, the interrupt device with the highest priority will be serviced first. The priority is set by wire-wrap connections on jumper block J8 (see figure E.4b).

4.11 Random Access Memory Board

The random-access-memory (RAM) board contains 128K of memory mapped dynamic RAM (MCM6664). The RAM is accessed through the STD bus.

The memory mapping on the RAM board enables swapping of 2K blocks of memory. In this way, the RAM locations that are masked by the CPU memory ($C000 - $FFFF) can be mapped into an accessable region. There is no danger of a 'crash' on the data bus when the CPU memory is accessed and the RAM board is enabled because the data bus line drivers for the STD bus are disabled (see figure E.7a).

Up to sixteen memory boards may be used at any one time provided that each has a unique name or number wire-wrapped on the J1 jumper block. The name is a 4-bit number unique to the board and is used to match a portion of the address required to setup the memory mapping. The memory mapping hardware is located at address $7FN0 - $7FN3 where N is the 4-bit number.

The memory mapping hardware is accessed when the MEMEX control line on the STD bus is asserted by the CPU through its bus register. The lower four bits of a data byte (lower nibble) are written into the mapping register (74LS170) when the locations $7FN0 - $7FN3 are addressed. The RAM board is enabled when a bit (D0) is written to the address $7FN8, and is placed on the STD bus when MEMEX is released from the asserted condition.

4.12 Erasable Programmable Read-only Memory Board

The EPROM board contains 64K of read-only-memory that is accessable by the STD bus and can be used in conjunction with the CPU memory. The memory consists of two banks of 32K each (see figure E.8).

The EPROM board is accessed through the STD bus by setting an enable bit in much the same fashion that is done for the RAM board. The MEMEX control line is asserted which allows access to the enable latch. An enable bit, D0, is written to the enable latch at address $7FNX which will put the EPROM board on the STD bus when MEMEX is released. Only the first 12 bits of the address, $7FNX, are used with the 4-bit number, N, being the unique number of the board. One of the two banks of 32K will be selected when a 1 or 0 is written into b1 of the register at $7FNX.

4.13 Controller Board

The controller board contains the neccessary hardware logic to generate the receiver address, chopper clock signals, synchronous detector control signals, and other clock signals. The board is controlled by one of the parallel ports on the I/O board. The board layout is shown in figures E.10a, E.10b.

The controller board receives commands from a PIA (MC6821) which is configured for write-only operation. The hardware is setup so that registers on the controller board are controlled by the 3 least significant bits of the PA port of the PIA. Data bytes are transferred by port PB of the PIA.

The controller board contains three 8-bit registers (74LS374). The first one controls external access to the board by tri-stating the bi-directional buffers (74LS244), and can also tri-state the other two registers. The second register buffers the addresses for the receivers. The third register selects the type of clock (PTM or external) for generating the synchronous detector control signals.

There are two phase-locked loop (PLL) circuits on the controller board. One PLL locks to the clock frequency selected by register #3 and sends its VCO output to the chopper drive output pin. The sole purpose of this PLL is to smooth out sudden phase transitions in the clock

frequency when a different frequency is selected (eg., reprogram PTM). Phase transitions are smoothed out by a large time constant loop filter (30 seconds).

The second phase-locked loop generates the INHIBIT control signal required by the synchronous detectors. The PLL synthesizes a frequency that is 256 times the chopper frequency which is then passed through 2 programmable counters (MC14526) to effectively time the on and off periods of the INHIBIT control signal. When the 2 PLLs have locked, 2 LEDs will light up indicating the locked condition. Figures E.11a and E.11b show a complete schematic of the controller board.

4.14 Analog-to-Digital Conversion Board

The analog-to-digital conversion (ADC) board consists of a 12-bit CMOS ADC (ADC1210), an eight channel multiplexer, auto-calibration, dual sample-and-holds, a buffer amplifier, and hardware logic for parallel port access.

The ADC board consists of two sections; one is digital electronics, and the other is analog electronics. All of the digital electronics is associated with logic control of the ADC board and switching control of the analog signal paths (see figures E.13a, E.13b).

The ADC board is controlled by a PIA (MC6821) parallel port on the I/O board. The PIA has two bi-directional ports (PA and PB) for parallel communication. Port PA was setup for read-only operations and reads the 2 bytes of digitized signal on receiving a rising edge of CC. (conversion complete signal).

Port PB was setup for write-only operations, and controls: the input data selector for one-of-eight input signals, the reference data selector for on-board ADC calibration, sample-and-hold multiplexing, and triggering SC (start conversion process of the ADC). The schematic of the ADC board is shown in figures E.13a and E.13b.

The ADC integrated circuit (ADC1210) was designed for single power supply operation (10.0 Vdc) with input signal acceptance range of $\pm$ 5Vdc. Negative voltages are

permissible since internal resistors on the input pins of the ADC effectively shift the voltage to within an acceptable range. Circuitry, external to the ADC chip, enables it to run at fast conversion times of 24 μS, as opposed to the more typical time of 100 μS. The digital output of the ADC is buffered by open drain non-inverting buffers (MM74C906) for logic level shifting to +5 Vdc. The outputs of the buffers are latched (74LS373) and then clocked into the PA port of the PIA when a rising edge from CC (conversion complete) is received.

Two sample-and-hold (SH) devices (LF398H) on the ADC board are alternately switched to the input of the ADC chip. As one SH is sampling the input signal and charging its hold capacitor, the other SH is holding its sampled voltage for the ADC while it is performing the conversion process. Both sampling and digitization take the same time (24 μS) so there is no waiting time in the entire process. Port PB provides eight bits for control of the ADC board. The 3 least significant bits (PB0, PB1, PB2) instruct the input data selector (MC14051) to select one of the eight input signals. Bit PB4 initiates the analog-to-digital conversion process. Bit PB5 synchronizes the switching of the SHs with the start of a series of conversions so that the same SH is consistently used for a particular input signal. The bits PB7, PB8 control the calibration selector (MC14052) by selecting 0 Vdc, +2.666 Vdc, -2.666 Vdc, or the analog input signal.

4.15 Real-time Clock and Programmable Timer Module Board

The RTC/PTM board contains a real-time-clock chip (RTC: MC146818) and two programmable timer modules (PTM: MC6840). The purpose of this board is to provide real time information during the course of an experiment, and to provide a clock signal for the chopper drive. During the development of the MCSA, the PTMs proved to be very useful in synthesizing various clock signals required as control signals (see figures E.14a,b for board layout).

The RTC/PTM board is accessed through the STD bus and is similar to the RAM board in the way it is enabled (see figures E.15a and E.15b for schematic). Board control logic is accessed by asserting the MEMEX control line on the STD bus. The board is enabled by writing a bit (D0) to the enable latch at address $7FNX and releasing MEMEX.

Address decoding is not taken all the way to a unique location but only as far as to clearly separate the RTC and the PTM. The RTC is selected in the address space $7FXX and occupies $40 locations. The PTM-1 and PTM-2 are selected at addresses $7E0X and $7E1X respectively.

The STD bus control signals, CLOCK and CNTL, are used to regenerate the quadrature clock, Q. The clock is required by the hardware for the correct determination of valid-address and valid-data. The CNTL signal is used to multiplex the lower address lines with the data lines for the RTC.

4.16 Software Implementation

The multichannel spectrum analyzer is completely controlled by software and has relatively few external controls for system control. Of the many types of operating systems presently available for microcomputers, the FORTH operating system was adopted for use with the 6809 based microcomputer.

The bulk of FORTH resides in the top 8K of EPROM ($E000 - $FFFF) of the CPU board. The RAM locations $D000 - $DFFF are required by FORTH as well. The operating system is started by hardware reset (front panel RESET, or STD bus PBRESET).

The particular implementation of FORTH for the MC6809 microprocessor is derived from fig-FORTH (release 1, version 1.0, June 1980) which is public domain software made available by the Forth Interest Group (FORTH). The software has been modified to conserve space and to make room for application software. All routines associated with disk operations have been removed since there are no disk capabilities with the present system. The start of FORTH has been repositioned to $E000 and the dynamic portion starts at $D000. This enables FORTH to be run from only the CPU board (see figure 4.17 for a memory map).

Some system routines in FORTH were altered to improve the execution time of the operating system. This was done

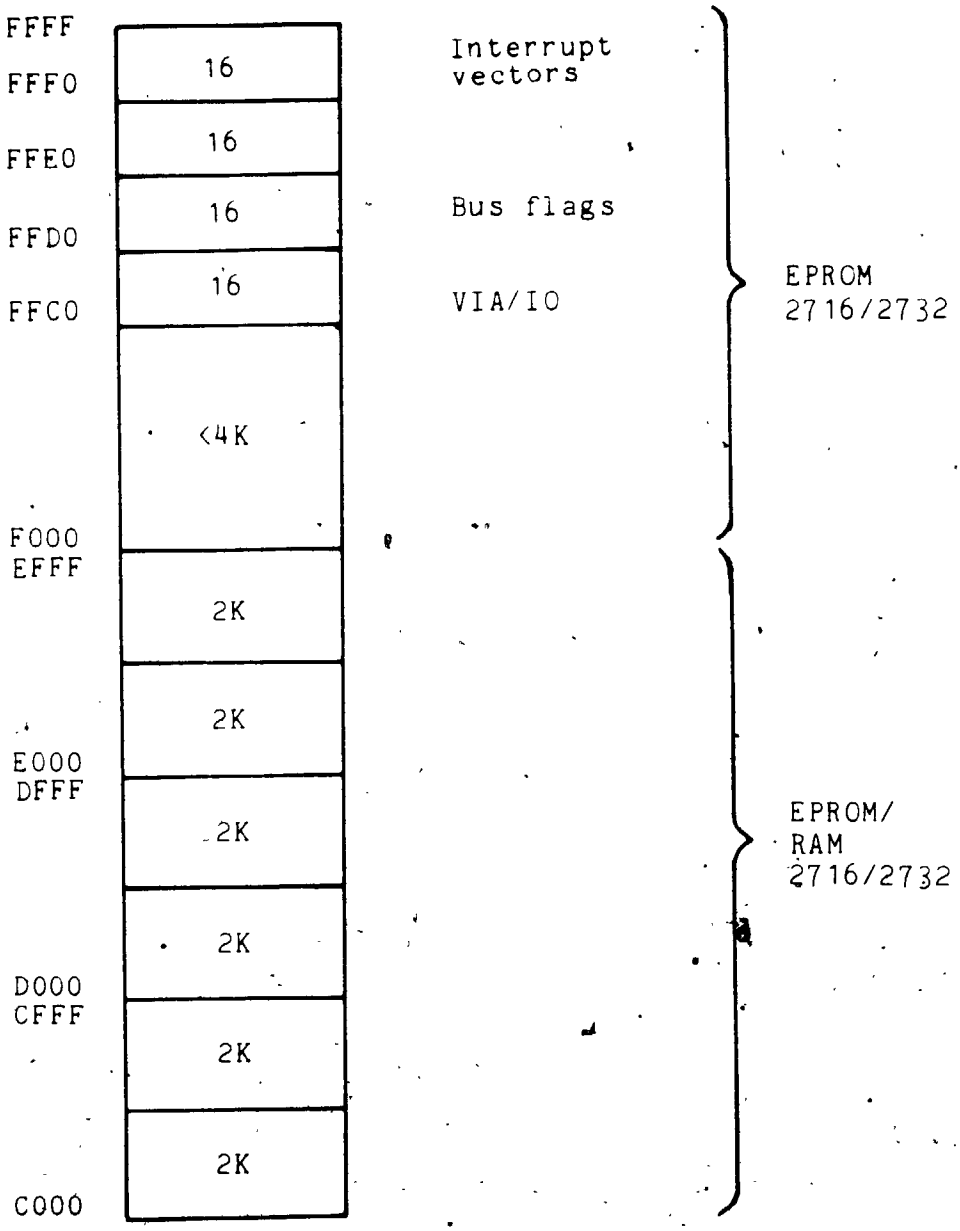


Figure 4.17 CPU board memory map.

at the expense of slightly increased memory requirements.

In order to run the MCSA, a large number of routines were written of which some could be directly appended to FORTH while others had to be stored off the CPU board and on the EPROM board. The routines appended to FORTH are an integral part of it and can be immediately executed. The other routines on the EPROM board are not precompiled. They are stored as ASCII text since they are often modified during the course of system development. These routines may be linked to the FORTH dictionary by issuing a LOAD command with the starting address (any address except $0000).

A large number of routines have been written to run the MCSA either directly or to provide support for application routines. The routines can be roughly divided into seven groups: 1) low FORTH routines, 2) high FORTH routines, 3) board/device commands, 4) low application routines, 5) high application routines, 6) low graphic routines, 7) high graphic routines. These groups are by no means definitive but serve only to aid in the description of the diverse routines developed for the microcomputer system. The low FORTH routines are those that are only concerned with FORTH itself. Most of these routines are quite short and simple, and usually serve only as macros for other routines. The high FORTH routines perform a task whose result is of prime importance. Most FORTH commands are high FORTH routines

and are compiled from other high FORTH, low FORTH, and primitive FORTH routines. Board/device commands are routines that access a board or device in order to perform a simple function such as enabling or disabling a board or read/write to a register. Low application routines perform tasks that make use of one or more boards/devices. For example, the routine ADC0 accesses the ADC board, initiates an analog-to-digital conversion, reads the 12-bit number, and returns with it on the stack. High application routines go many steps further than low application routines by bringing together a number of the low application routines to produce results like graphic displays and data tables. Low graphic routines are mainly macros that relieve the tedium of typing graphic commands directly into graphic programs. High graphic routines are a collection of FORTH routines and low graphic routines for production of useful graphic displays.

Appendix F lists all of the FORTH routines developed for the MCSA. They are grouped according to the seven previously defined groups and are also listed according to how they appear in the FORTH operating system and in the EPROM board. Appendix F also contains all of the source listings of the FORTH routines.

Chapter 5

System Tests and Calibrations

5.1 Front-end Module Tests and Calibration

Test and calibration procedures were carried out on both sections of the front-end module to verify design objectives for this portion of the multichannel spectrum analyzer (MCSA). The procedures were performed on individual parts, on combinations of parts, and on sections of the front-end module. The results of the test and calibration procedures provide a reference should retesting and recalibration become neccessary.

The sequence of tests and calibrations on the parts of the front-end module follow the RF signal path as it passes through the hardware (See figures 2.1, 3.4). The first set of tests was performed on the system starting with the front-end wideband amplifiers up to the 4-way power splitters.

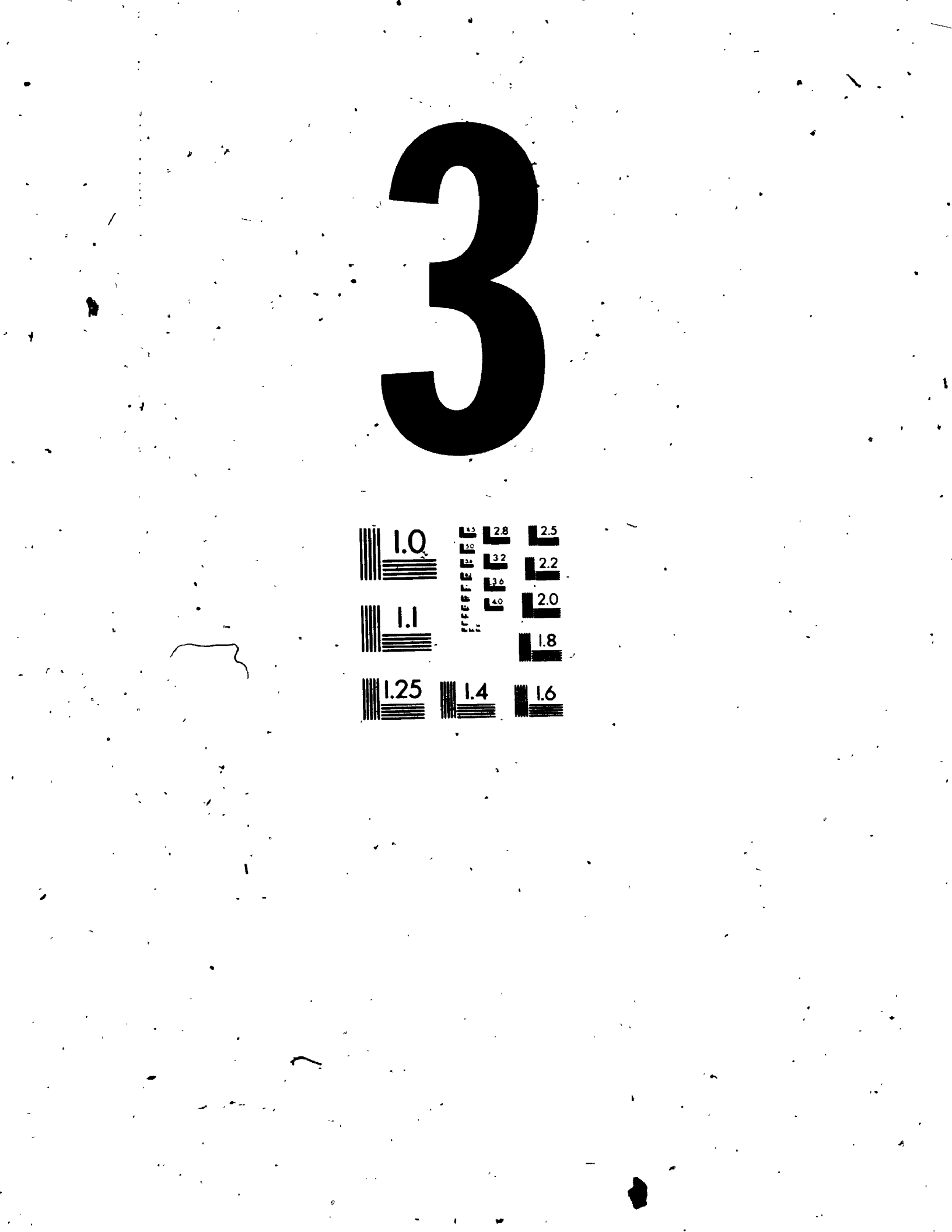
The first stage of the front-end module is an RF amplification stage. The two RF amplifiers (AMM502B, W1GA) were tested and were found to have amplification of 27 dB and 20 dB, and noise figures of 2.7 dB and 1.8 dB respectively (See Appendix C for specifications).

The 2-way power splitter following the RF amplifiers module (PSC2-1W) used in the front-end module was tested on a separate printed circuit board mounted in a small

diecast aluminum box for shielding. The voltage-standing-wave-ratio (VSWR) was relatively low (1.2:1) for this device. However, it was found that deviation from a 50 ohm termination on any ports noticeably influenced the other ports. It was found important to have a 50 ohm termination for the wideband filters as their response depends highly on it. Resistive attenuation on the input and output ports of a filter was found to be useful in dampening reflections at these ports.

One of the outputs of the 2-way power splitter goes to the second section of the front-end module for high-pass filtering, the other output continues in the first section for further processing.

The next stage of processing in the first section is a low-pass filter (9th-order Chebyshev, f_c = 256 MHz) which is shown in figure 4.2. The experimental and theoretical responses of the low-pass filter are plotted in figure 5.1. The response test and calibration were done with the filter isolated from the circuit, and with the aid of a network analyzer (HP - 8410A, HP - 8412A) and a sweep oscillator (HP - 8690B, HP - 8699B). The experimental response shows little deviation from the theoretical response in the pass-band and only minor deviation in the transition and stop band. The frequency response plots are shown with a linear frequency scale rather than the more common logarithmic scale. Since the


3
1.0
1.1
1.25
1.4
1.6
2.8
3.2
3.6
4.0
2.5
2.2
2.0
1.8

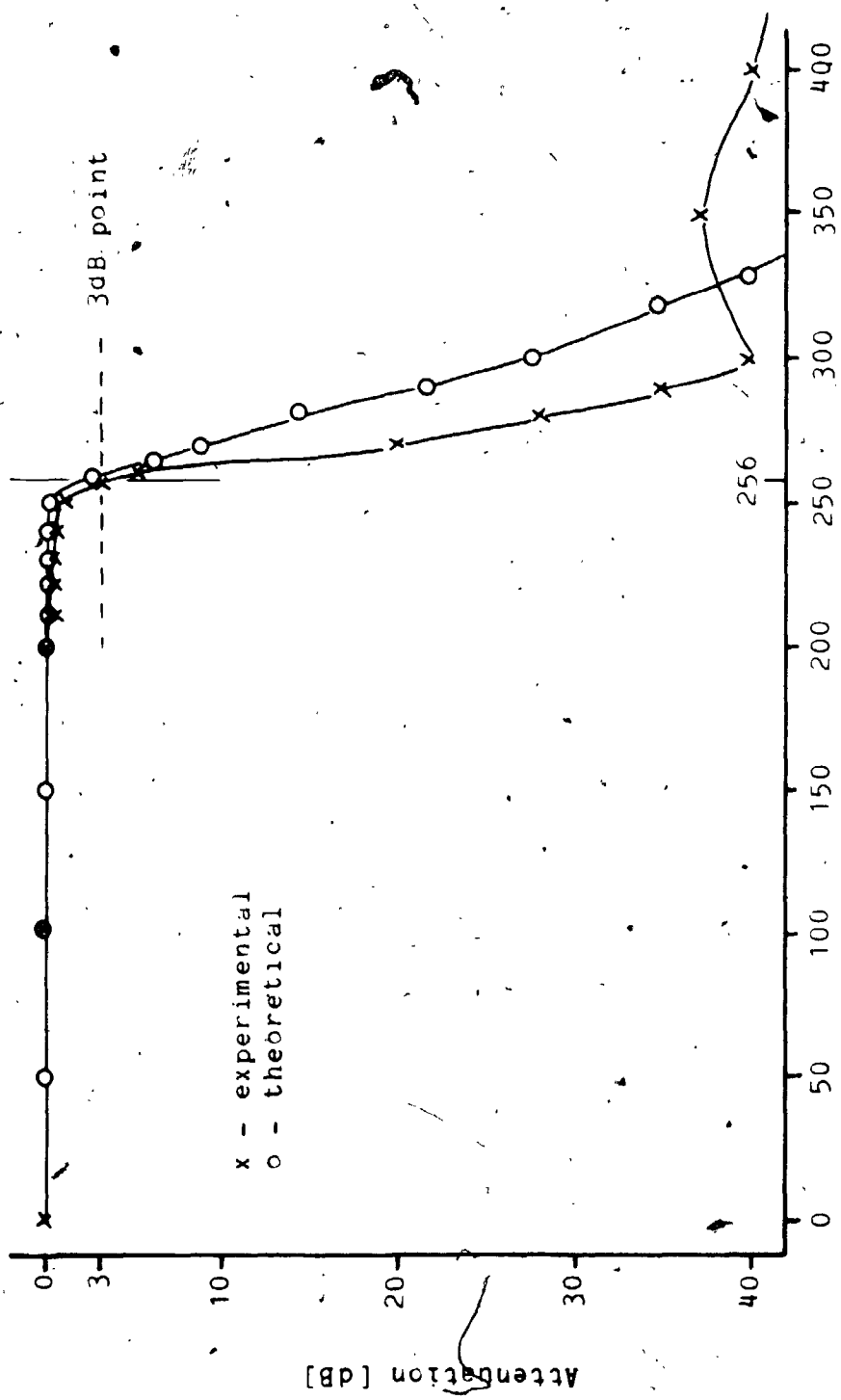


Figure 5.1 Low-pass filter response (fc = 256MHz).

reception range of 0 - 512 MHz is divided into 64 channels of equal bandwidth, it was logical to use a linear scale in the plots.

The low-pass filter is of the Chebyshev type which, as the theoretical response illustrates, is characterized by equiripple in the passband, sharp roll-off in the transition band, and no ripple in the stopband. The experimental response is typical of an elliptic filter (Cauer filter) where there is equiripple in both the passband and stopband (Daniels, 1974). The idealized Chebyshev response was unattainable at these high frequencies for the following reasons. Firstly, the lumped components (inductors and capacitors) do not behave ideally over the 512 MHz bandwidth; capacitors suffer from dielectric losses and inductors have losses due to the skin effect. Secondly, the RF energy on the input of a filter may propagate across the space between the input and the output. This is especially a problem in the stopband frequency range where the input RF energy is reflected back to the source which may not absorb it. Conditions for launching the reflected signal into the shielding box cavity may become favourable. Thirdly, lumped components begin to exhibit transmission line properties which can lead to undesirable enhancement in the stopband.

The most important aspects of the low-pass filter response are: good rejection in the stopband (greater

than 36 dB), a sharp transition occurs at 256 MHz, and the passband is equiripple (less than 0.28 dB).

The front-end mixer (SRA-1W) follows the low-pass filter and was found to produce good mixing results provided that the local oscillator signal is at 7dBm input level. However, considerable problems were encountered when connecting circuits such as the preceding low-pass filter. The RF port of the mixer could not provide the 50 ohm resistive termination required by the following wideband filter. Its VSWR was found to be within the specified maximum of 2:1 but was still found to drastically affect the filter response. The addition of a 50 ohm resistor in parallel with the RF port of the mixer improved the response to an acceptable level. The resistor adds loss to the circuit but also absorbs spurious signals appearing at the RF port.

The helical resonator following the mixer worked well in rejecting the front-end local oscillator. The response and calibration test was done in circuit with the mixer removed. The experimental and theoretical response curves are plotted in figure 4.3b. The theoretical response was based on a transmission line approximation to the helical resonator (see Appendix D). The experimental response follows the theoretical response in the reject band quite well, providing up to 30 db rejection of the front-end local oscillator at 512 MHz. The presence of the resonator did affect the response of the two closest

channels. At 508 MHz and 500 MHz, the centre frequencies of the two adjacent channels, the attenuation had dropped to 14 dB and 5 dB respectively. Compensation for the loss can be accomplished by increased IF gain in the respective channel receivers. The effective characteristic impedance of the experimental response was found to be very close to the 500 ohm designed value. An attempt was made to tune the resonator at the free end but the Q of the available trimmer was too low. The result was a broadening in the rejection bandwidth. The trimmer in this position also proved to be extremely sensitive to adjustment and hence, could not be relied on for a stable adjustment.

The characteristic impedance and propagation velocity in a transmission line are related to the distributed inductance and capacitance per unit length by the following expressions (Jordon, 1950):

$$Z_0 = \sqrt{\frac{L}{C}} \qquad 5.1$$

$$v = \sqrt{\frac{1}{LC}} \qquad 5.2$$

Using the transmission line approximation to the helical resonator, the above equations may be applied. The shunt capacitor of the helical resonator is effectively in parallel with the distributed capacitance and hence tends to reduce the effective characteristic impedance and

reduce the propagation velocity. In order to obtain the highest Q possible, minimal trimmer capacitance was used and the coil was snipped to bring it very close but above the desired resonant frequency.

The output of the helical resonator passes through an attenuator designed for 3 dB loss which in actuality gives 3.1 dB loss. Following the attenuator, there is a wideband amplifier module (MWA110) which provides 16 dB of gain across the 256 - 512 MHz band.

The wideband amplifier drives a low-pass filter, which is the last stage in the first section of the front-end module. The filter was designed as a 9th-order Chebyshev filter. The theoretical and experimental frequency response are plotted in figure 5.2. The experimental response shows less than 1 dB ripple in the passband of 0 - 512 MHz and a sharp transition of 32 dB in 10 MHz. The stopband settles down to greater than 27 dB attenuation. As with the previously discussed filters, the experimental response is characteristic of an elliptic filter of which the Chebyshev filter is a special case (Daniels, 1974).

The second section of the front-end consists of two identical halves with each half containing a high-pass filter, an amplifier, and a 4-way power splitter.

The two high-pass filters are 13th-order Chebyshev filters, with each having a cutoff frequency of 256 MHz. The frequency response of these two filters are plotted in

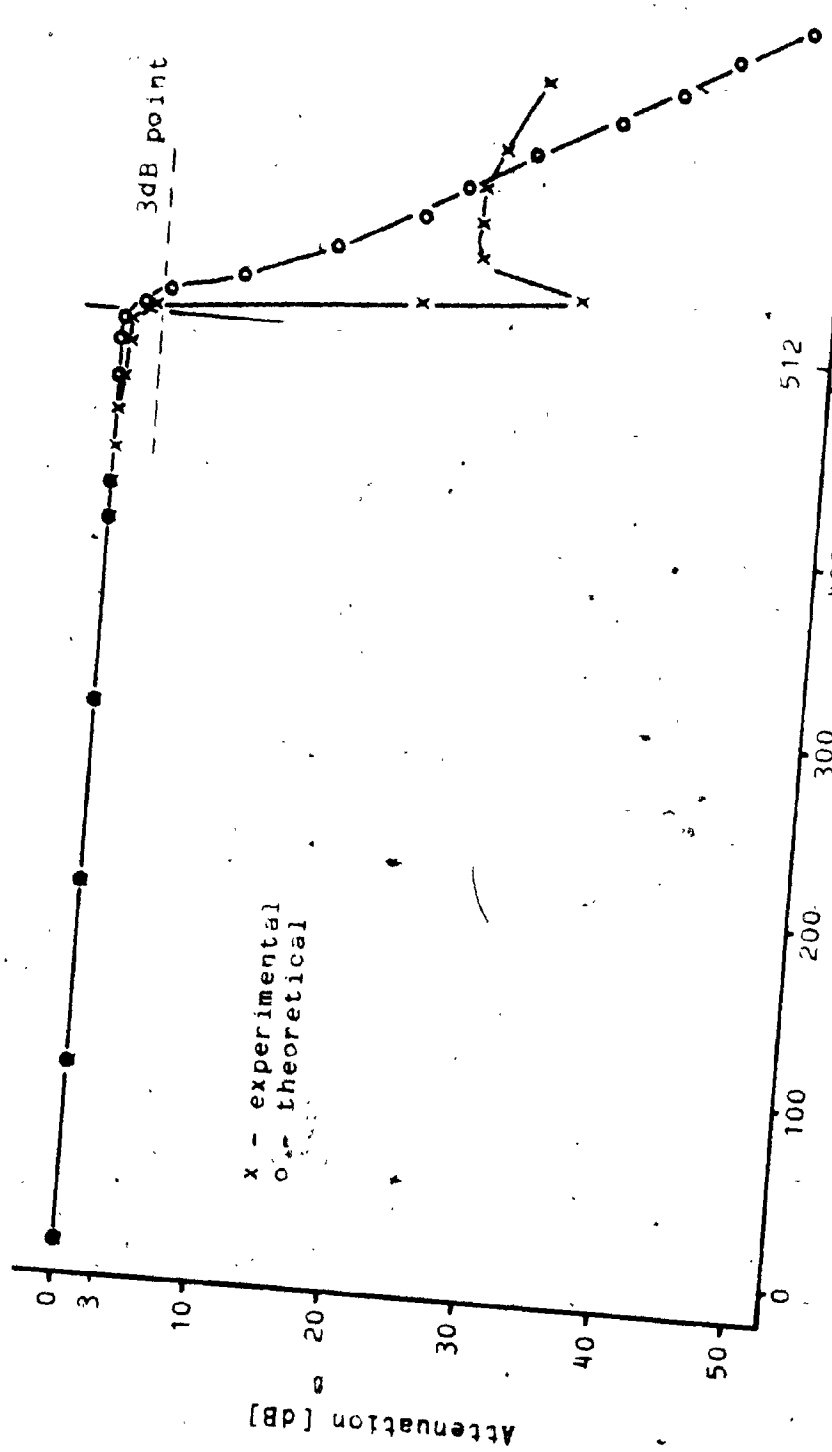


Figure 5.2 Low-pass filter response (f_c = 512MHz).

figure 5.3 (lower half of signal spectrum) and figure 5.4 (upper half of signal spectrum). Both filter experimental responses show very good passband properties with less than 1 dB ripple which compares favourably with the designed ripple of 0.28 dB. The transition band for the two filters is virtually the same with a transition of 45 dB in 40 MHz. The stopband for both filters is very low with the response for the upper half of the signal spectrum settling down to 45 dB attenuation, and for the other filter the response settles down to 50 dB attenuation. These two filters depart from the similarity to an elliptic filter that was noticed in previous filters. The passbands for the filters are sufficiently low that the previously mentioned mechanisms for passband ripple do not operate. In the stopband, propagation of the RF energy from the input to the output around the filter is considerably less favourable than in previous filters and is evident by the very high attenuation and minimum ripple.

The frequency response of the combined low-pass filter (from the first section of the front-end module) and high-pass filter (from the second section of the front-end module) for the lower half of the signal spectrum is plotted in figure 5.5. The experimental frequency response of the combined filters has good attenuation (>50 dB) in the lower stopband and low ripple in the passband (<1 dB). However, there is some

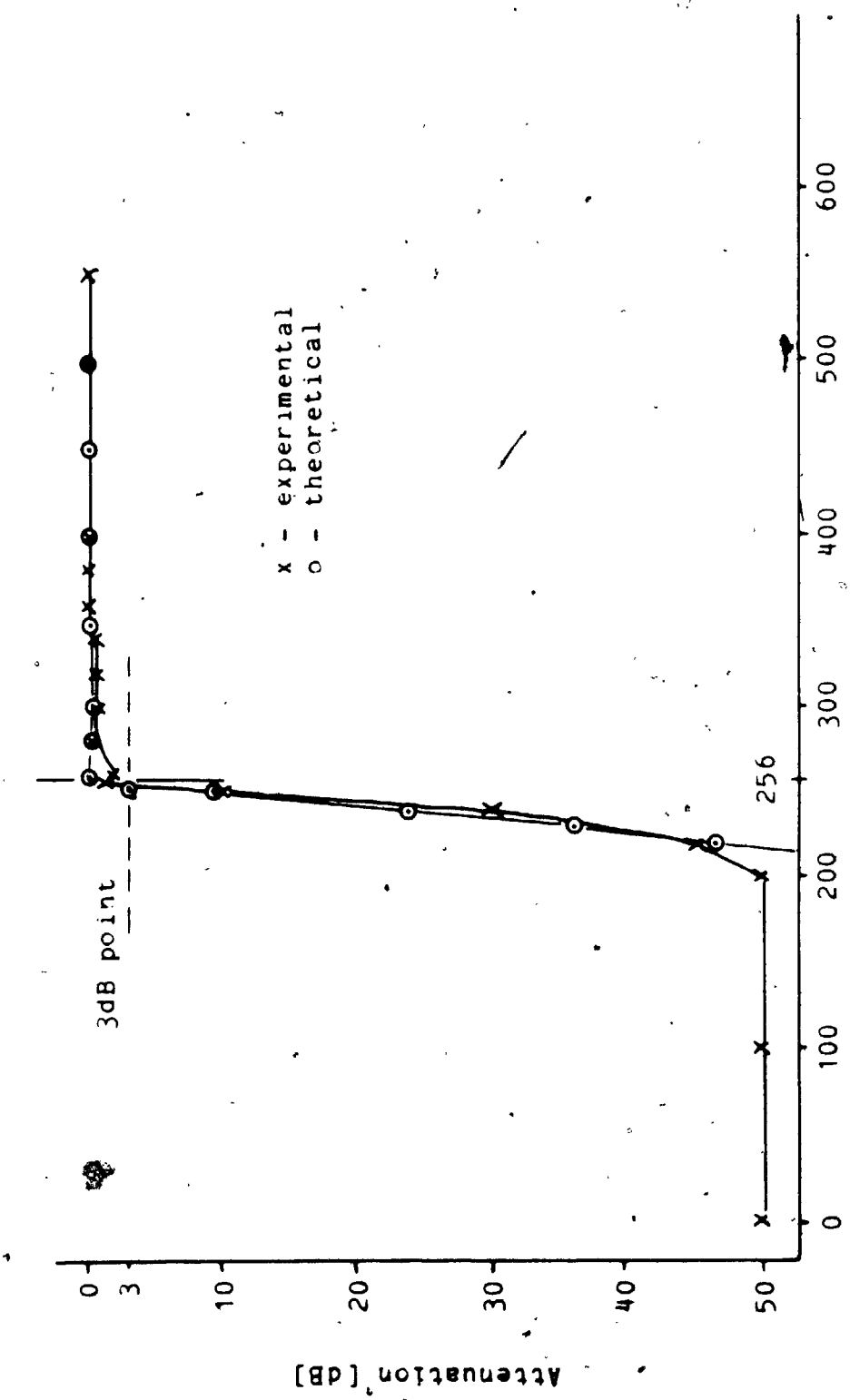


Figure 5.3 High-pass filter response for lower half of signal spectrum (fc = 256MHz).

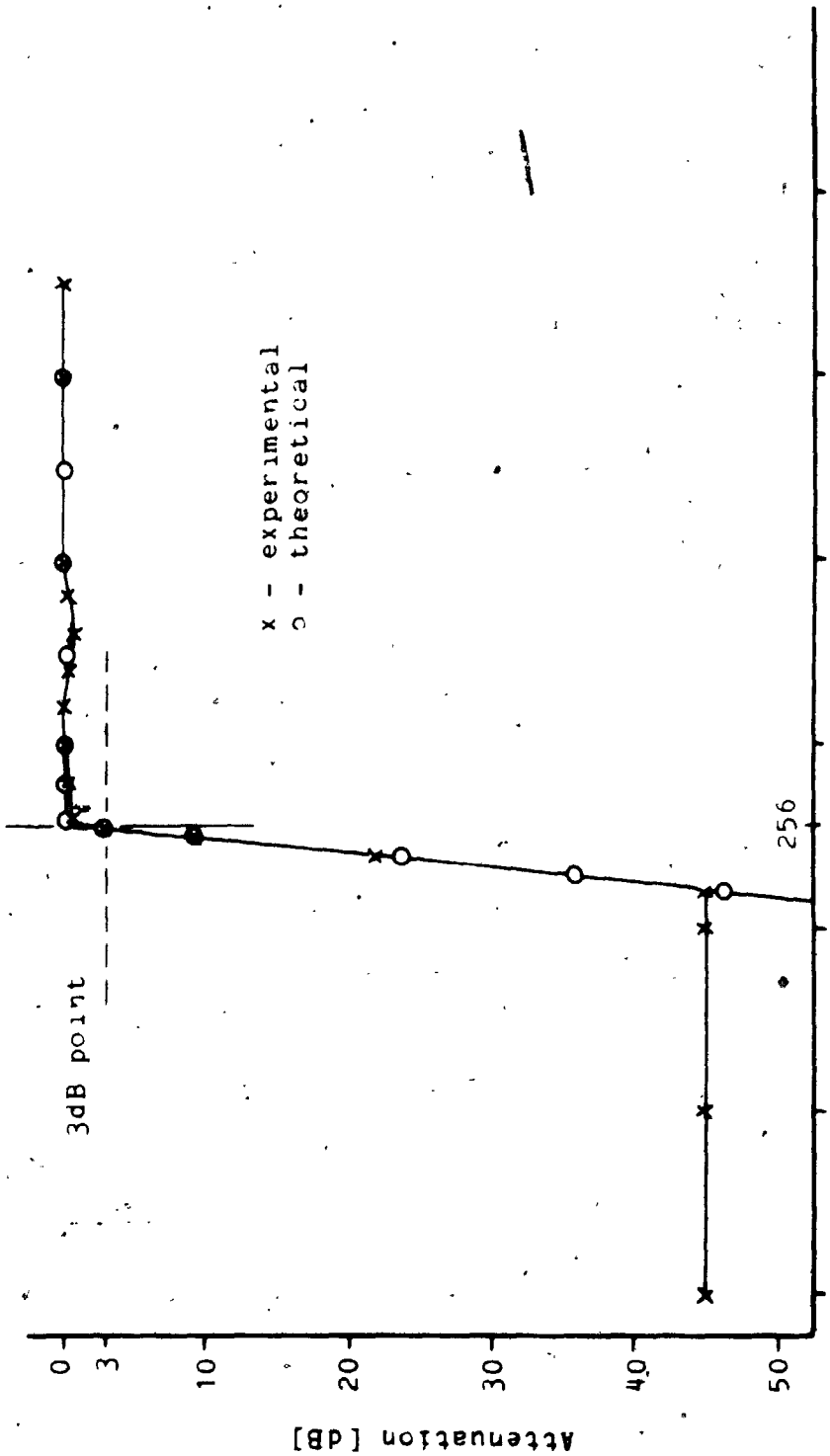


Figure 5.4 High-pass filter response for upper half of signal spectrum (fc = 256MHz).

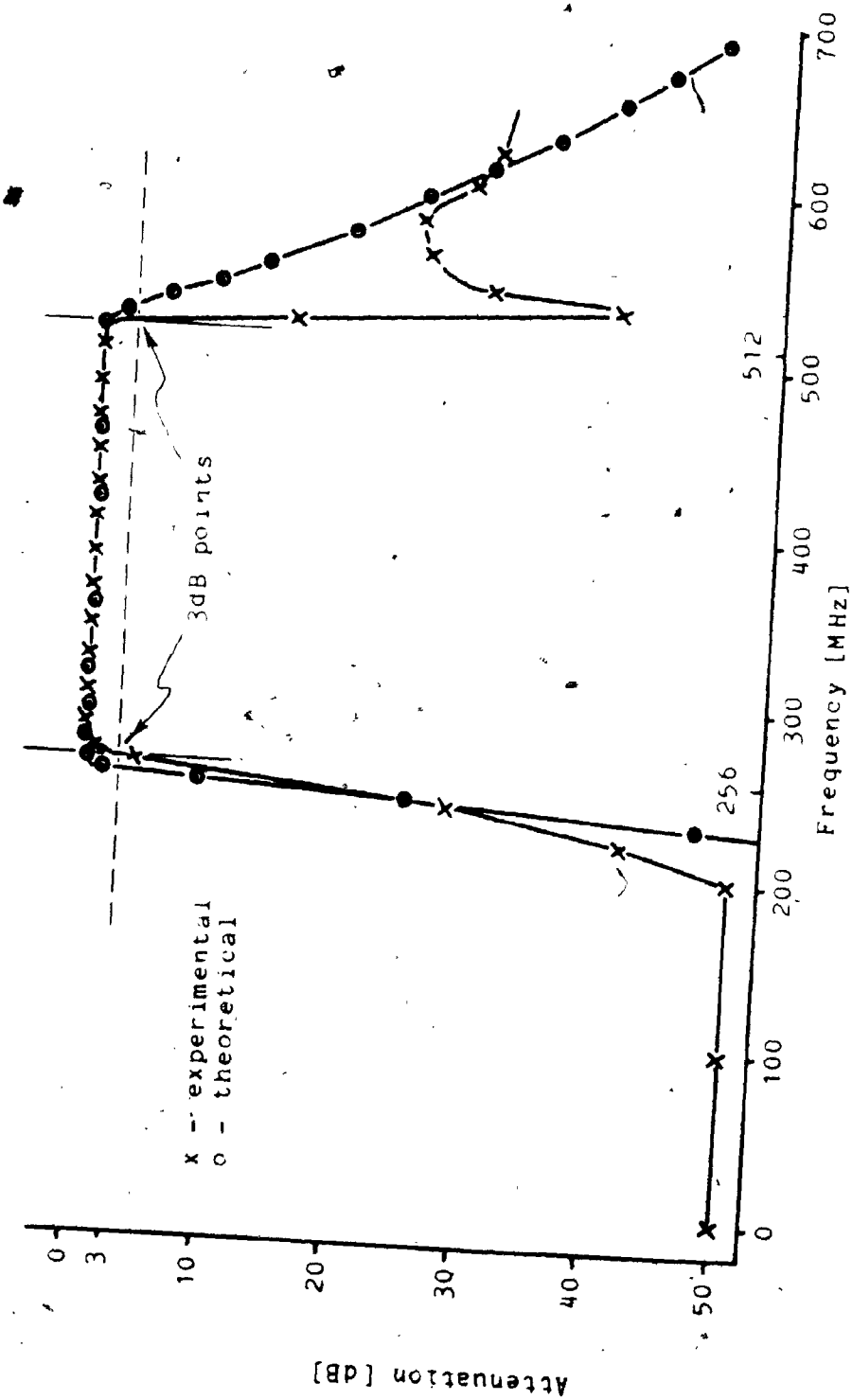


Figure 5.5 Frequency response of combined low-pass and high-pass filter (fcl =512MHz, fch =256MHz).

degradation in response for the upper and lower transition bands and in the upper stopband compared to that of previous results. The lower transition band (256 MHz) has a response roll-off of 45 dB in 60 MHz. This is still acceptable, since there are no channels operating below 256 MHz. If spurious frequencies appear in the transition band, they may not be sufficiently attenuated to prevent detection by adjacent channels. They can be dealt with on an individual basis if they become a problem. The upper transistion band has a sharp roll-off response of 40 dB in 20 MHz and the upper stopband settles to an attenuation of 30 dB. The experimental transition response is characteristic of the response for a transmission line filter or a helical resonator. This implies that at 500 MHz and above the discrete components used in the filter are behaving less like lumped components and more like distributed components.

The output of the high-pass filter of the second section of the front-end module is amplified by a wideband module (MWA220). Both amplifiers provided 10.5 dB of gain across the 256 - 512 MHz frequency range and drive the 4-way resistive power splitter.

The power splitters present a 50 ohm resistive termination to each of the filter banks but at the expense of 12 dB attenuation in total or 6 dB loss over that of a lossless 4-way split.

A complete front-end frequency sweep was performed with both sections of the front-end module connected and with the front-end local oscillator in operation. The input RF power level was set at -40 dBm to prevent overload of any of the wideband amplifiers which would result in distortion. The RF signal source was a Wavetek Signal Generator (model 3000) and the detector was a Tektronix Oscilloscope (model 7104) with a high frequency plug-in vertical amplifier module (model 7A29, BW = 1 GHz). The output signal was taken from one of the ports of the 4-way power splitter while the other ports were terminated in 50 ohms. Since there are two halves to the signal spectrum, two frequency sweeps were performed. The Wavetek Signal Generator has a parallel port on the rear panel for program control of the output frequency. The parallel port of the microcomputer was linked to the port and stepped the signal generator through the reception range of 0 - 512 MHz in 8 MHz steps.

The front-end frequency response corresponding to the lower half of the signal spectrum is plotted in figure 5.6. The experimental response of output power versus frequency has a passband gain greater than 12 dB and relative attenuation of more than 26 dB in the stopband. The maximum ripple in the passband is 12 dB. The transition band has a sharp roll-off of 12 dB per 10 MHz.

The ripple in the passband is undesirable but is manageable. The ripple in the passband can be linearized

by adjusting the gain in the receivers. In general, this should be avoided because the IF gain of a simple receiver is optimized for a narrow range of amplification and stability. Signals that appear in the peaks of the sweep response will be relatively large compared to those channels detecting signals in the troughs of the sweep response. The result would be a higher level of interference despite the isolation between channels.

The desired response is one with a flat passband, sharp transition, and high attenuation in the stopband. The last two of these have been met adequately. The ideal flat passband response is difficult to obtain in practice, since it depends on a large number of parameters that are not mutually independent but are coupled. Hence, adjustment of one of the components (inductor or capacitor) may alter the response in a number of locations.

The response in figure 5.6 can be directly attributed to mismatching between various subsections such as power splitters, mixers, filters, and amplifiers. The filters were especially sensitive to source and load impedances, as mentioned previously. The response could be improved by retuning the filters but the problem of coupled parameters limits the retuning to small adjustments. The problem of mismatching was alleviated a little by the use of attenuators which have a broadband dampening effect and tend to isolate one stage from another.

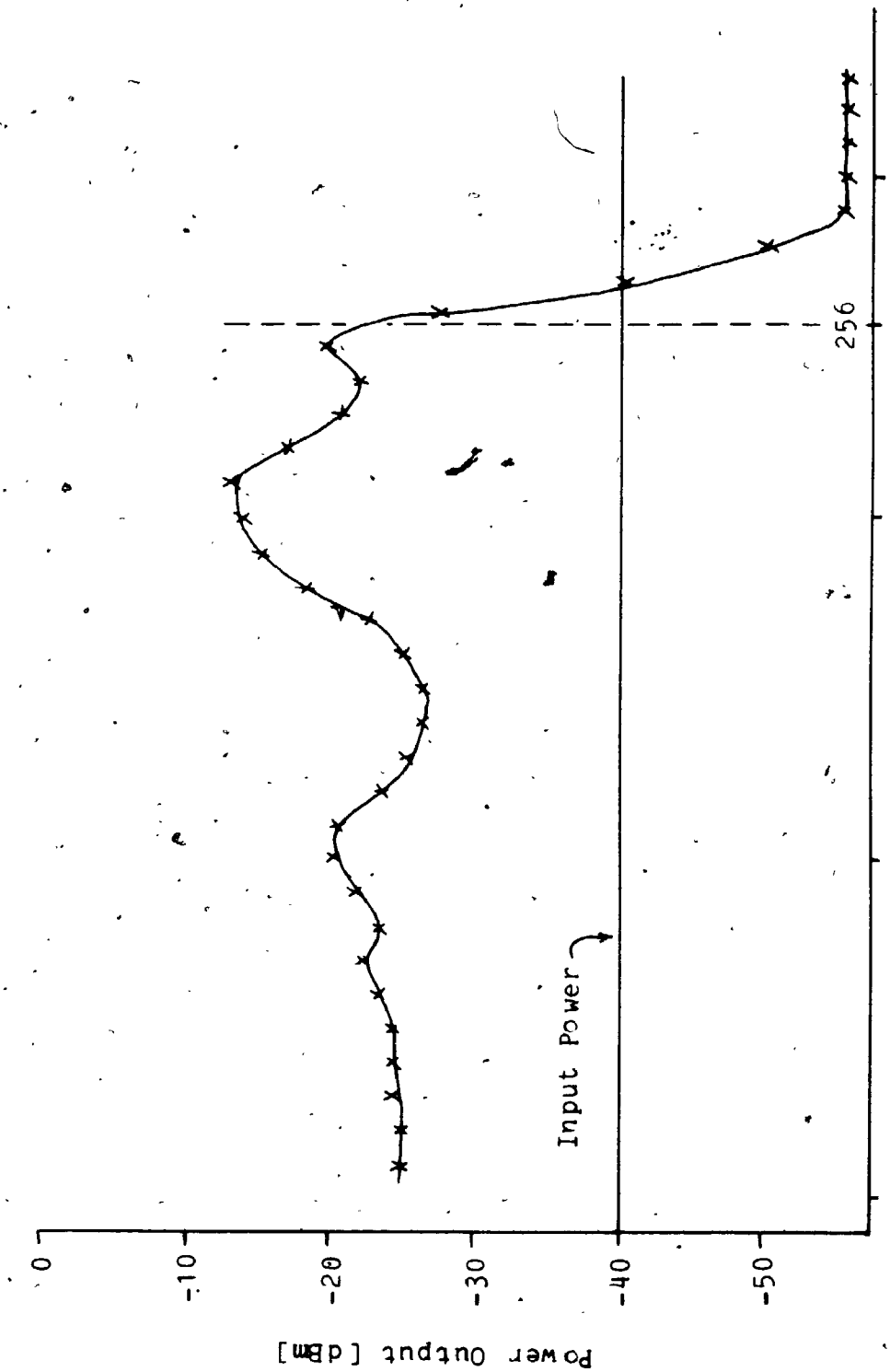


Figure 5.6 Front-end frequency sweep for lower half of signal spectrum.

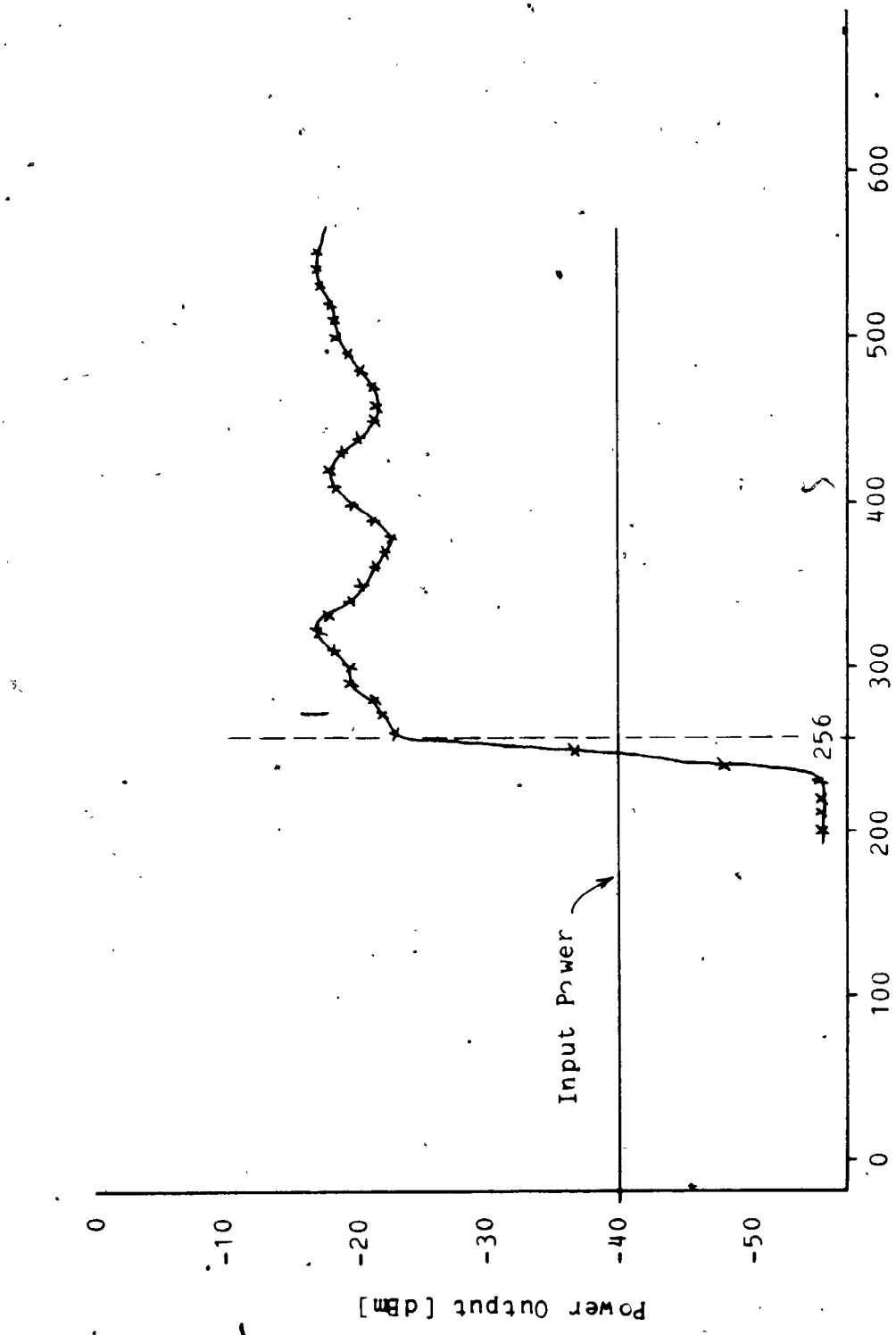


Figure 5.7 Front-end frequency sweep for upper half of signal spectrum.

The front-end sweep corresponding to the upper half of the signal spectrum is shown in figure 5.7. The experimental response shows output power versus frequency with the gain in the passband greater than 16 dB and the relative attenuation in the stopband greater than 30 dB. The maximum ripple in the passband is 5 dB which is undesirable, but manageable and is much less ripple than in the response for the lower half of the signal spectrum (see figures 5.6 and 5.7). The transition band is very sharp with a roll-off of 12 dB per 10 MHz. This half of the signal spectrum has considerably less RF processing to go through than the previous one and hence, less distortion of the response due to mismatching.

5.2 Filter Bank and Channel Filter Tests and Results

The frequency response of each bank of filters for the eight channels is shown in figures 5.8 through to 5.15. The filter banks operated satisfactorily.

The filter response of each channel was optimized on a network analyzer (HP 8410A) with a phase magnitude display (HP 8412A) and a sweep oscillator (HP 8690B, HP 8699B). This test apparatus is capable of sweeping from 100 MHz to 2 GHz and displaying the magnitude and phase response of a two-port network.

Each channel filter was tuned for the desired centre frequency, bandwidth, and insertion loss. It was desirable to have the channel filter tuned with the peak response corresponding to the centre, and with the 8 MHz bandwidth delimited by the same,relative attenuation. The half power points (or 3 dB) points) in a filter response are often used to delimit a filter's bandwidth, but in the case of the channel, this would lead to excessive channel overlap or channel aliassing. The channel filters were tuned at the 6 dB power points which would provide 12 dB isolation between two signals at the centre frequency of two adjacent channels.

It was important to keep the insertion loss of each channel filter the same, relative to one another and across filter banks. In this way, the frequency response is kept as flat as possible. An insertion loss of 10 dB

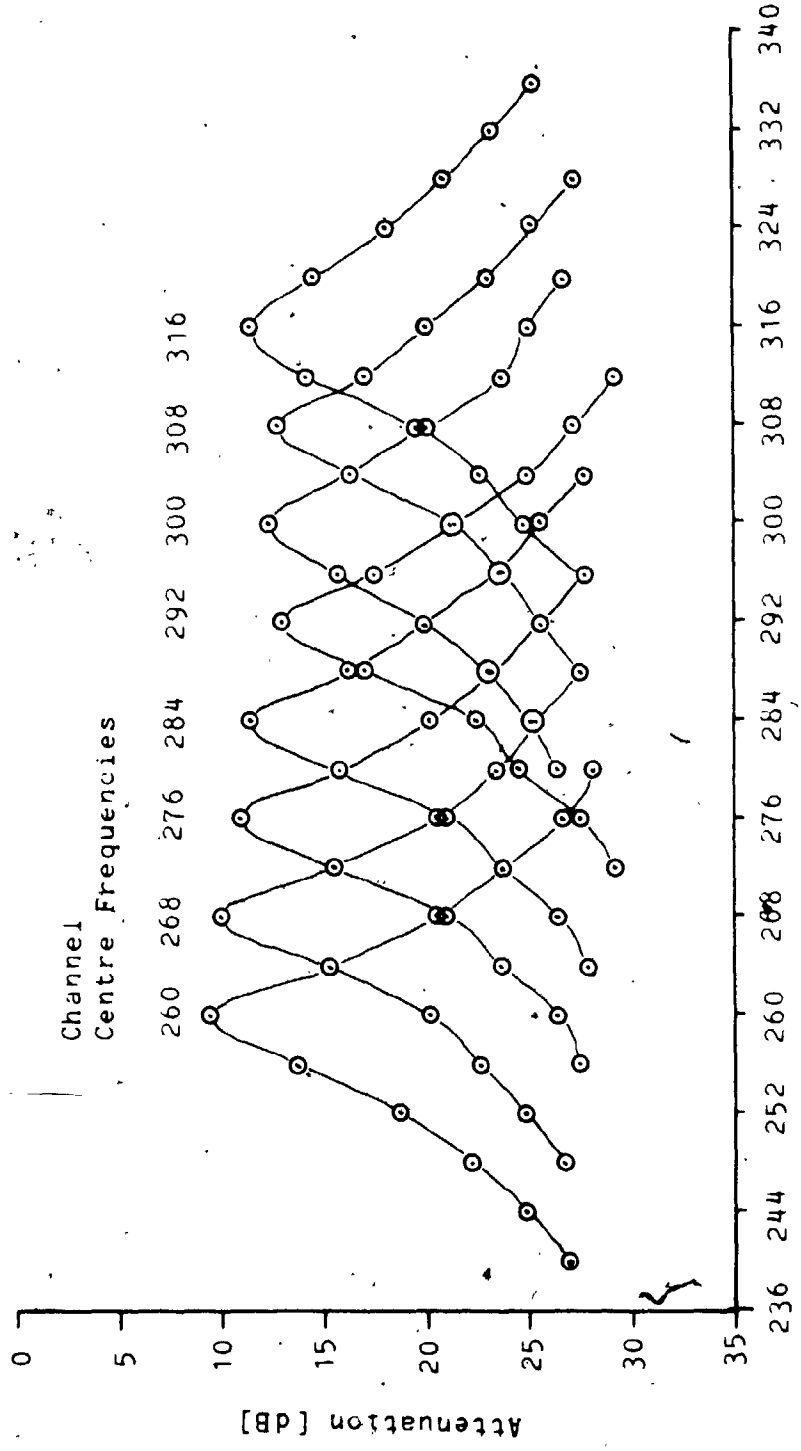


Figure 5.8 Filter bank response (260 - 316 MHz) for lower half of signal spectrum.

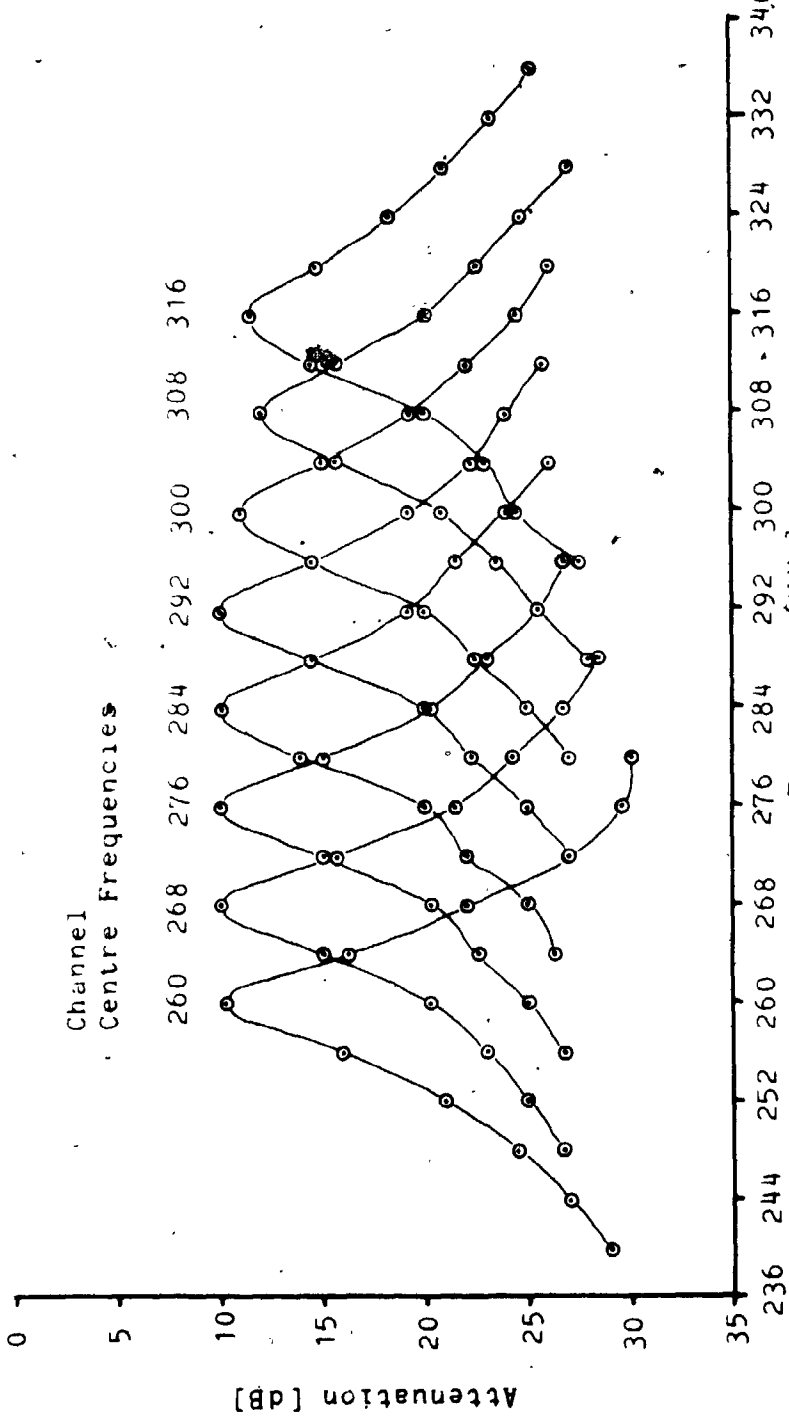


Figure 5.9 Filter bank response (260 - 316 MHz) for upper half of signal spectrum.

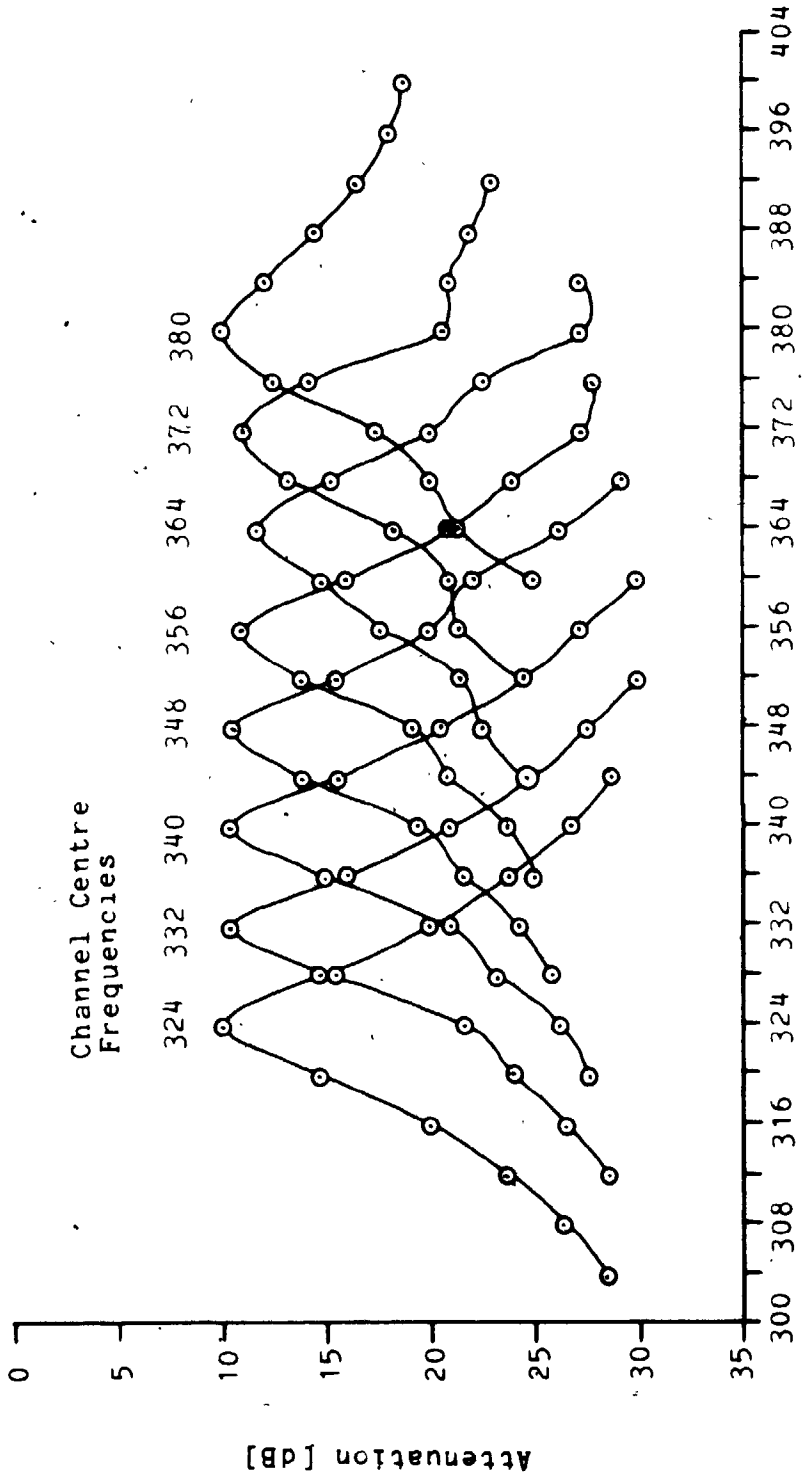


Figure 5.10 Filter bank response (324 - 380 MHz) for lower half of signal spectrum.

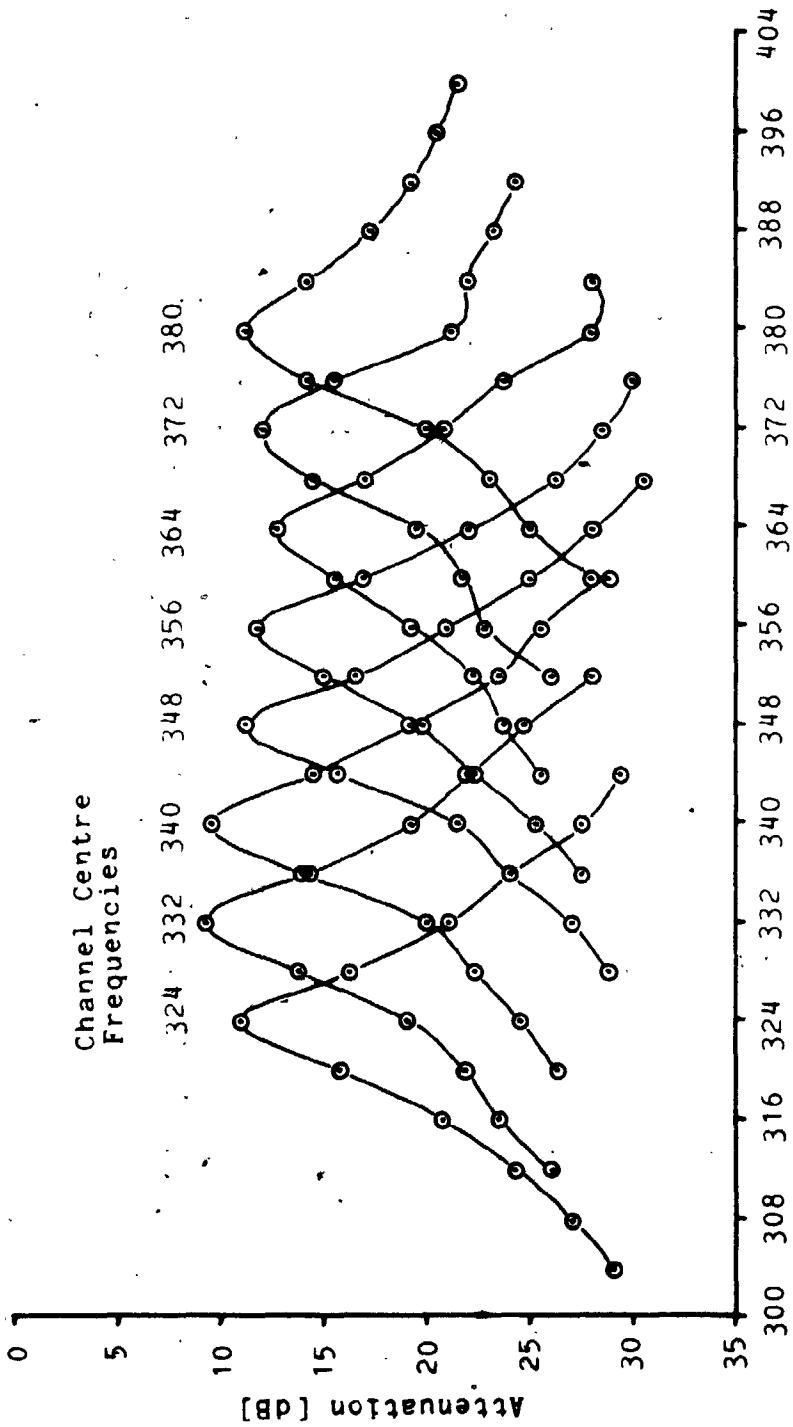


Figure 5.11 Filter bank response (324 - 380 MHz) for upper half of signal spectrum.

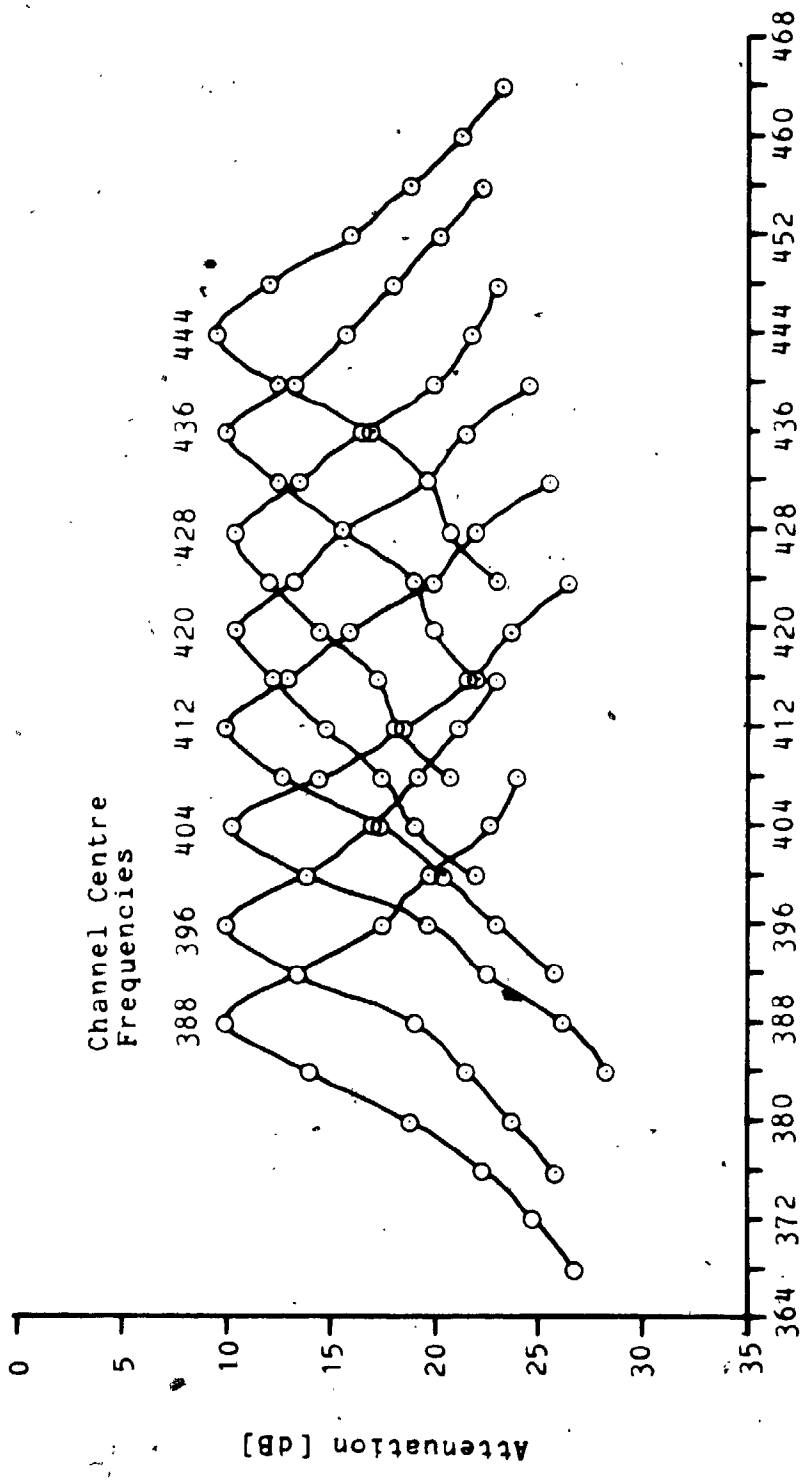


Figure 5.12 Filter bank response (388 - 444 MHz) for lower half of signal spectrum.

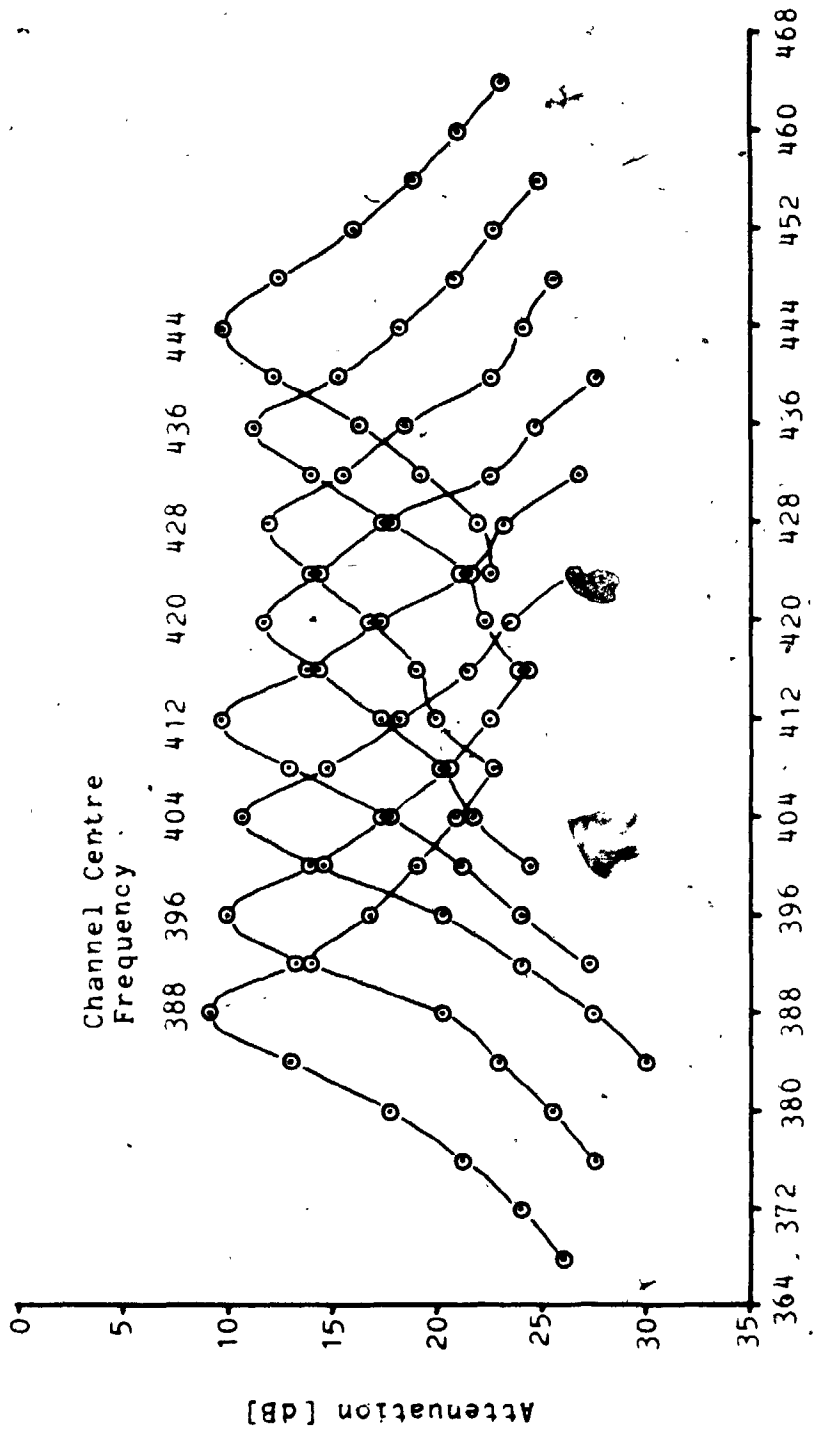


Figure 5.13 Filter bank response (388 - 444 MHz) for upper half of signal spectrum.

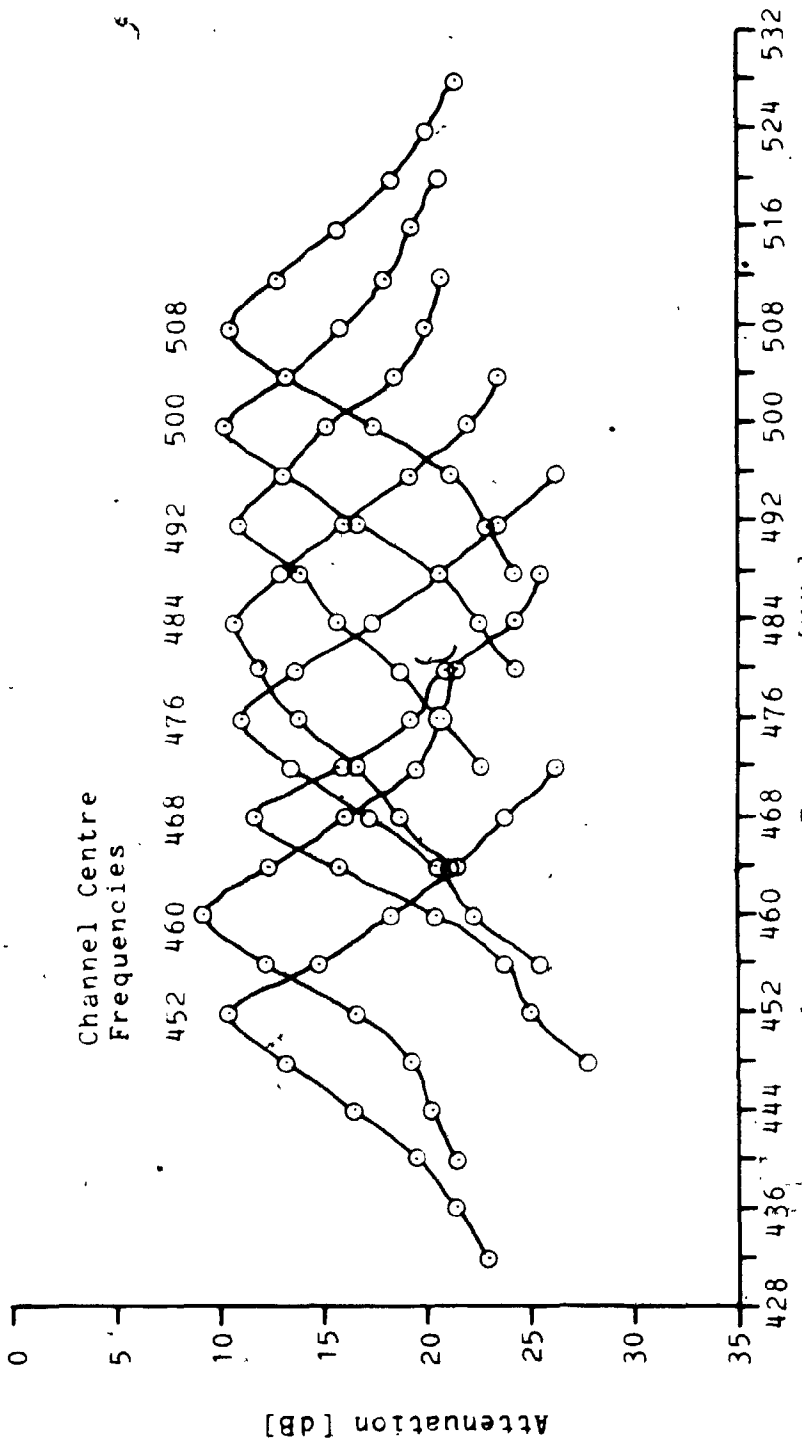


Figure 5.14 Filter bank response (452 - 508 MHz) for lower half of signal spectrum.

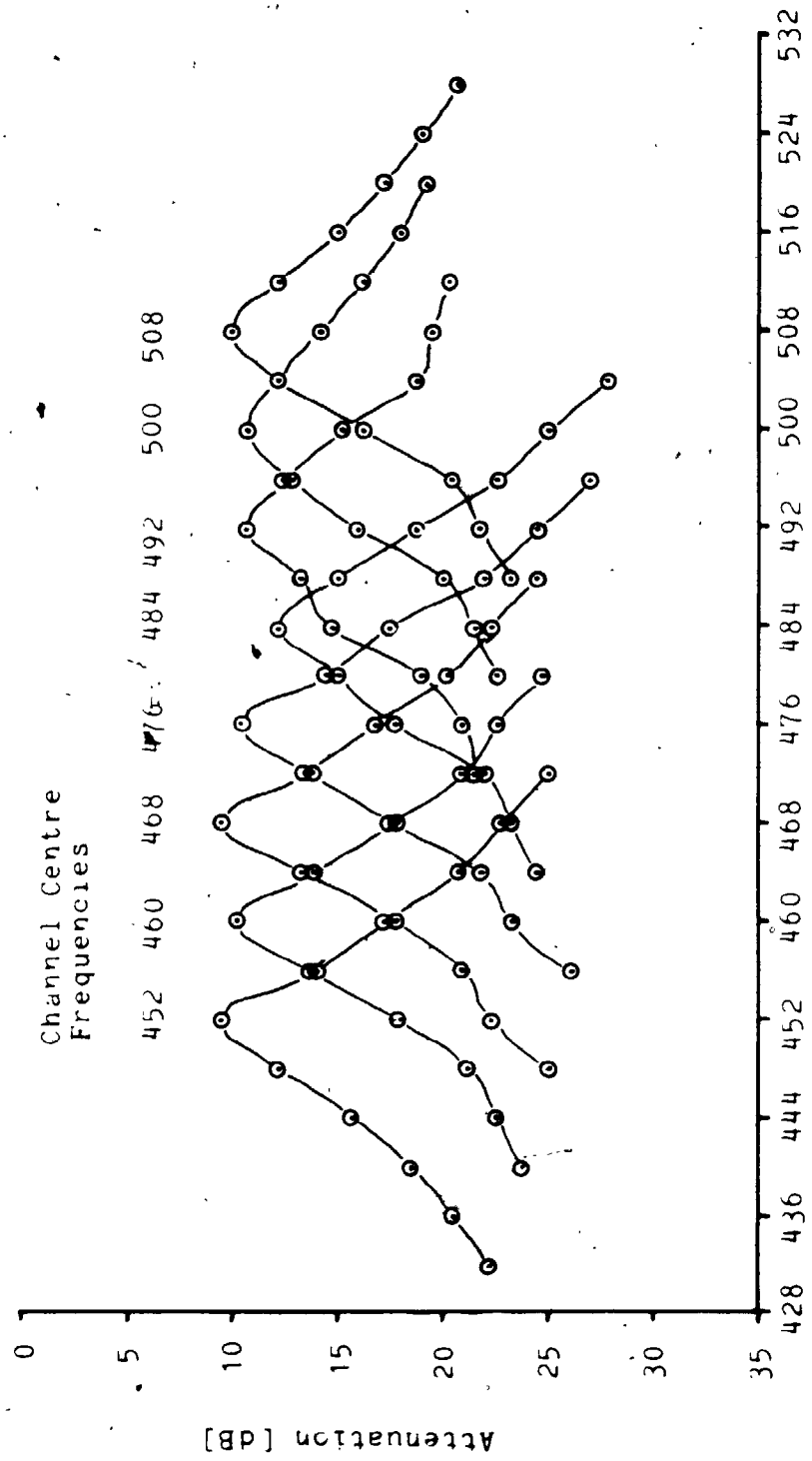


Figure 5.15 Filter bank response (452 - 508 MHz) for upper half of signal spectrum.

was finally adopted as being a compromise between minimum loss and undistorted channel filter response. At low levels of insertion loss, ripples will appear in the response due to impedance interaction of adjacent channels (Wilson, 1981).

A frequency sweep from the input of the front-end module to the output of the channel filters was performed with an input level of -20 dBm. The response for the lower half of the signal spectrum is shown in figure 5.16. The response is reasonably flat at an output level of -23 dBm $\pm$ 4.5 dB and has less ripple than the front-end frequency sweep shown in figure 5.6. The results were better than expected; it would seem that the mismatching of the front-end with the filter bank altered the frequency response in a favourable manner without adjusting the channel filters. It is also possible to do some RF compensation for the ripple in frequency response by adjusting the insertion loss of the channel filters. However, since the ripple is still manageable, the filter banks were not adjusted.

The response for the upper half of the signal spectrum is shown in figure 5.17. The response is quite flat from 256 - 512 MHz at a level of -20 dBm $\pm$ 4 dB. The ripple of this response is nearly the same as that of the previous response and it would appear, in this case, that the front-end output is well matched to the filter banks as there is little change in the ripple when compared to

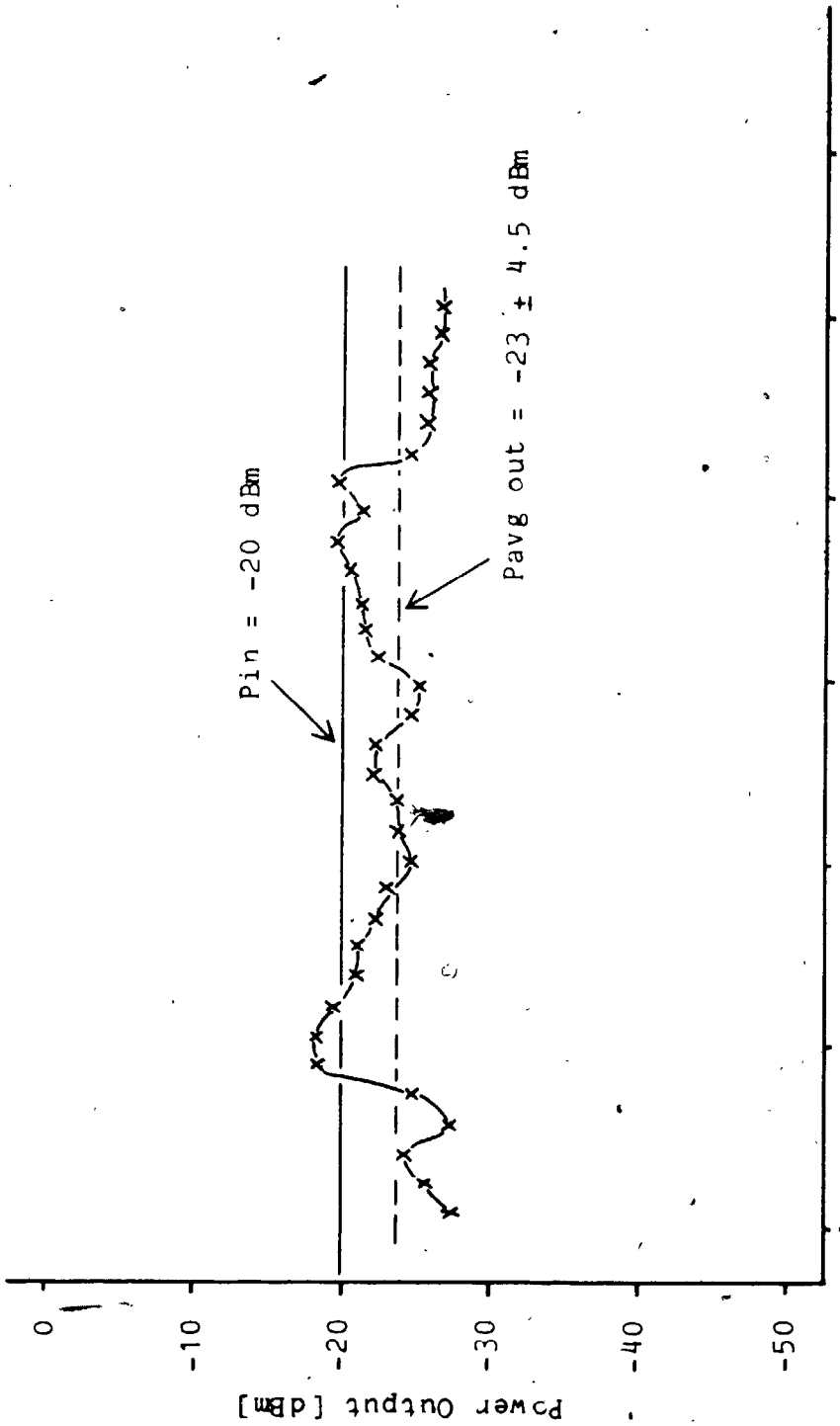


Figure 5.16 Frequency sweep of lower half of signal spectrum (input: front-end, output: filter bank).

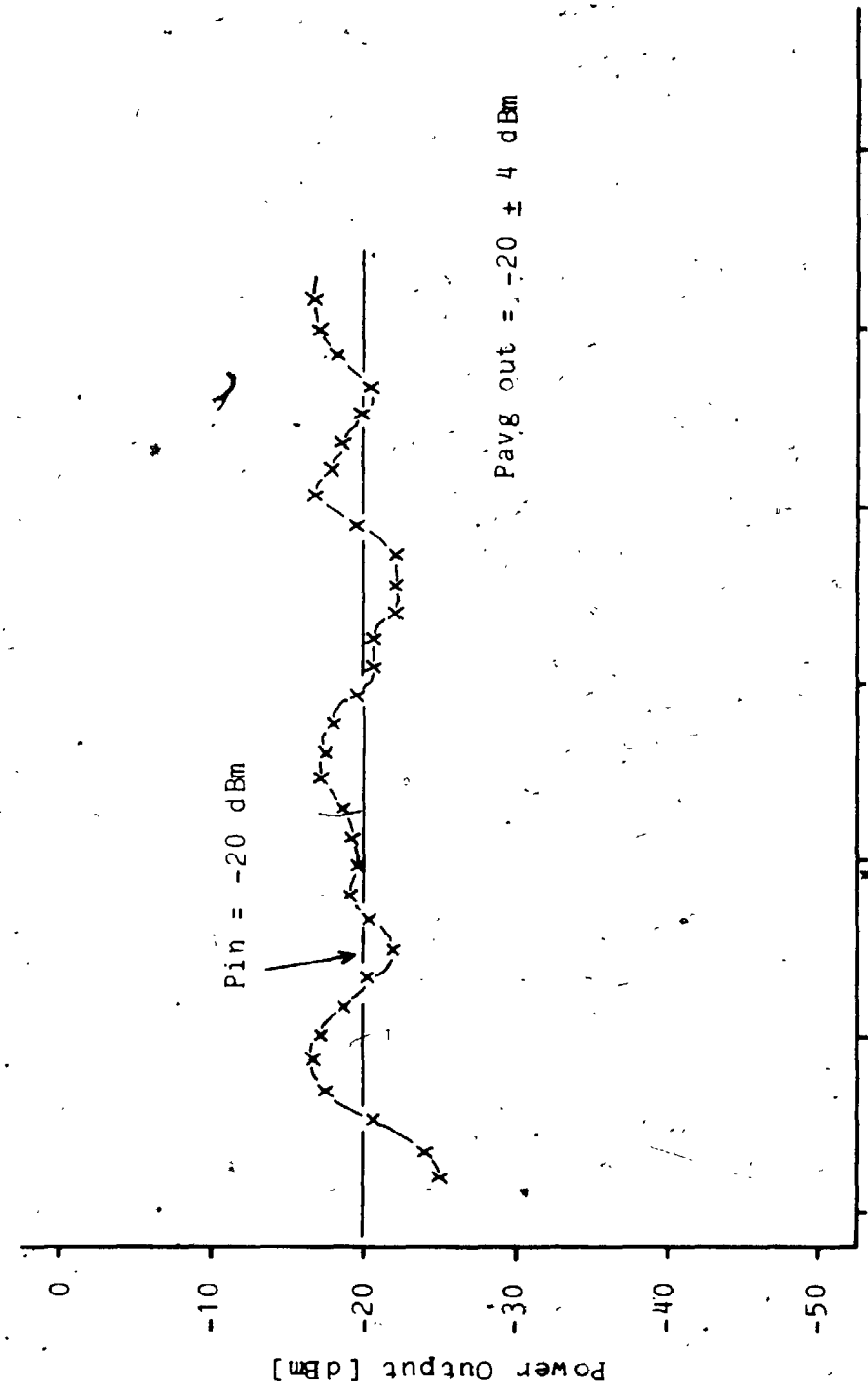


Figure 5.17 Frequency sweep of upper half of signal spectrum (input: front-end, output: filter bank).

the front-end response in figure 5.7. Adjusting the insertion loss of the channels to compensate for the ripple was considered unnecessary since the ripple is still acceptable.

5.3 Channel Receiver Tests and Results

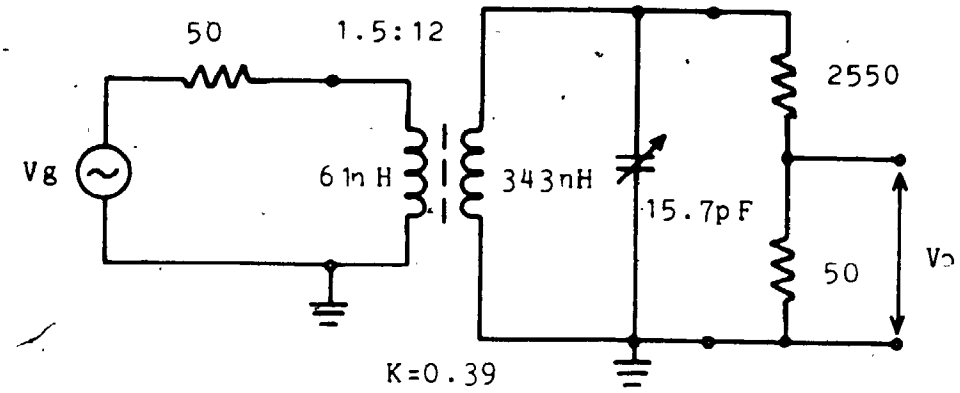
Considerable care was taken in the design of the receiver housing and associated input and output lines to eliminate the effects of external and internal contaminating signals. The largest signal in proximity to the receiver is the local oscillator and it is very important to keep this strong signal away from the small-signal detector diode. The coaxial cable (RG-174) used, provides 60 dB isolation between the inside conductor and the outside braid and 120 dB isolation between the centre conductor of two adjacent coaxial cables. The majority of the RF amplification takes place in the front-end module which furnishes sufficient gain to produce a difference of 40 - 50 dB between the signal and the local oscillator in the receiver module.

Searching for RF leakage was facilitated by the construction of a small RF probe which was simply a small coil soldered to the open end of a coaxial cable. The probe was connected to the 50 ohm vertical amplifier of the 7104 oscilloscope and the coil end of the probe was passed over all likely points of RF leakage. Any leakage would be inductively coupled into the probe and displayed on the oscilloscope.

The double-balanced mixer (SBL-1) of the receiver worked well, but did require resistive 50 ohm loads on the RF, LO, and IF ports. The resistor on the IF port

dissipates some of the signal, but it is required to dampen the input capacitance of the IF amplifier and to absorb the other product produced by mixing. Damping resistors of 50 - 100 ohms on the other two ports were tried, but were found to be largely unnecessary.

Preliminary tests of the IF transformer were performed under ideal conditions with an HP sweep generator driving the 50 ohm primary and a 2600 ohm resistor divider load on the secondary. The resistor divider load consists of a 2550 ohm resistance in series with a 50 ohm resistor to ground. The output voltage was taken across the 50 ohm resistor which matches the input impedance of the vertical amplifier of the 7104 oscilloscope. After accounting for voltage reduction in the resistor divider output, the response of the transformer under these ideal conditions is plotted in figure 5.18. The transformer core was adjusted for critical coupling and the capacitance was adjusted for the centre frequency. The parameters namely bandwidth, centre frequency, and coupling are not independent in this design and cannot be selected without affecting the others. Consequently, a satisfactory compromise must be met, otherwise the coil windings must be changed to obtain a new set of parameters. Figure 5.18 shows a good response for the transformer with the 3 dB points at the required 60 and 68 MHz.



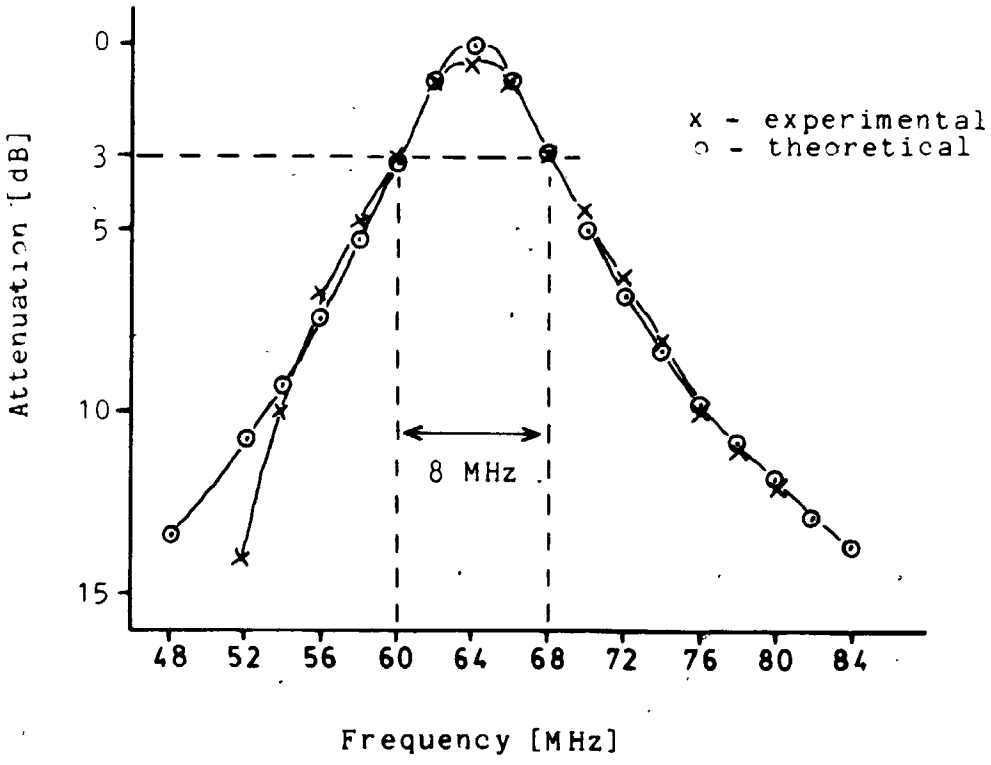


Figure 5.18 Ideal transformer response.

The pair of Schottky detector diodes (MBD102) were matched by measuring the diode voltage to within $\pm$ 0.25% under the conditions of constant room temperature (25°C) and 20 μA bias. The diode equation (3.7) shows that matching in this case pairs diodes with common saturation currents, I_s. The actual operating temperature (36°C) is higher than room temperature. It was assumed that the matched diodes would remain matched at the slightly elevated temperature. The reactive components of the diode detector cannot be easily calculated, but can be determined experimentally. It has been shown that the diode (MBD102) has effectively a series inductance of 3 nH and a parallel capacitance of 0.8 pF and a dynamic impedance of 2600 ohms (Wilson, 1981). The series inductance had minimal effect at 64 MHz, but the capacitance did have an effect and was compensated by the trimmer capacitor on the secondary of the transformer.

The instrumentation amplifier worked well once the coarse offset control had been set. There is external access to a potentiometer for fine offset control when balancing of the system after it has thermally stabilized.

The variable gain amplifier was adjusted with the right combination of resistors when the local oscillator circuitry had been completed and final adjustments made.

The receiver response tests and calibrations for all 64 channels proved to be long and laborious. Fortunately, the care and patience applied during assembly led to

consistently good results through all channel receivers. The most important requirement of the receivers is that the bandpass response be well defined and similar for all receivers. Figures 5.19 through 5.22 are all normalized plots of the receiver responses and, hence, do not reflect the difference in gain between channels (note: the responses are grouped according to receiver sequential numbers corresponding to channel numbers, and not channel addresses). The gain of a receiver is dependent on the amplitude of the local oscillator, conversion gain of the mixer, matching efficiency of the transformer, and sensitivity of the detector diode. The figures demonstrate that each receiver has a good bandpass response centred at 64 MHz with a 3 dB bandwidth of 8 MHz.

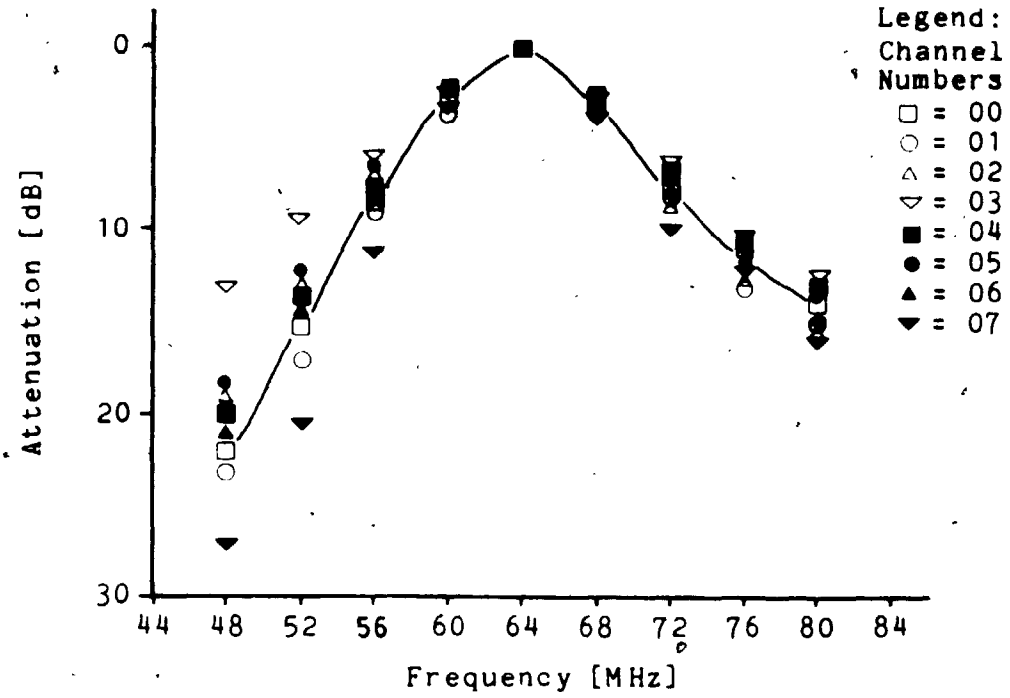


Figure 5.19a Receiver responses.

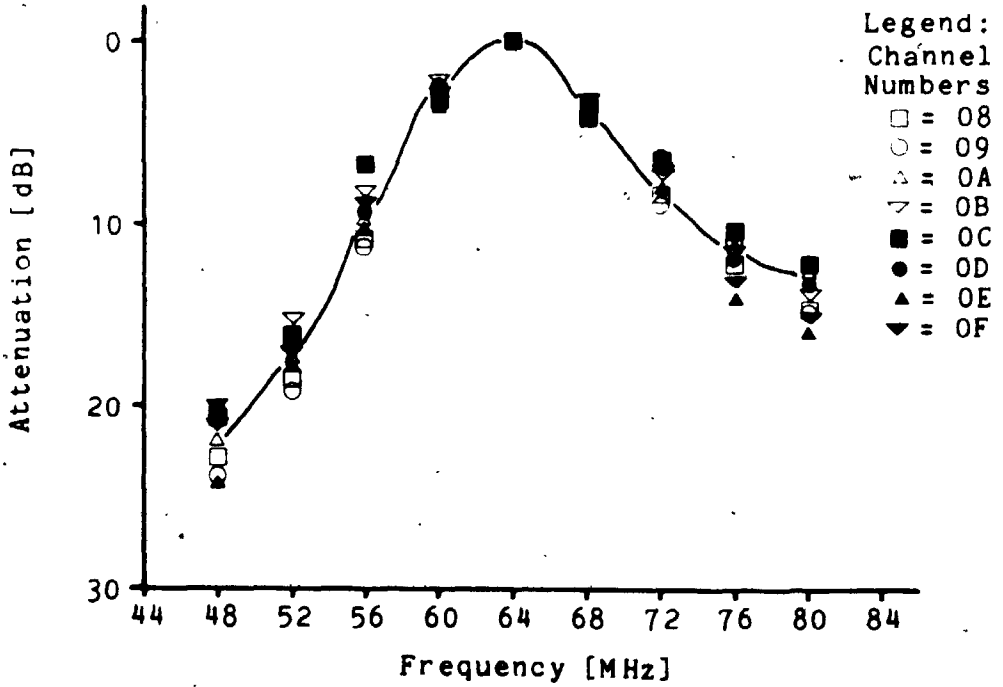


Figure 5.19b Receiver responses.

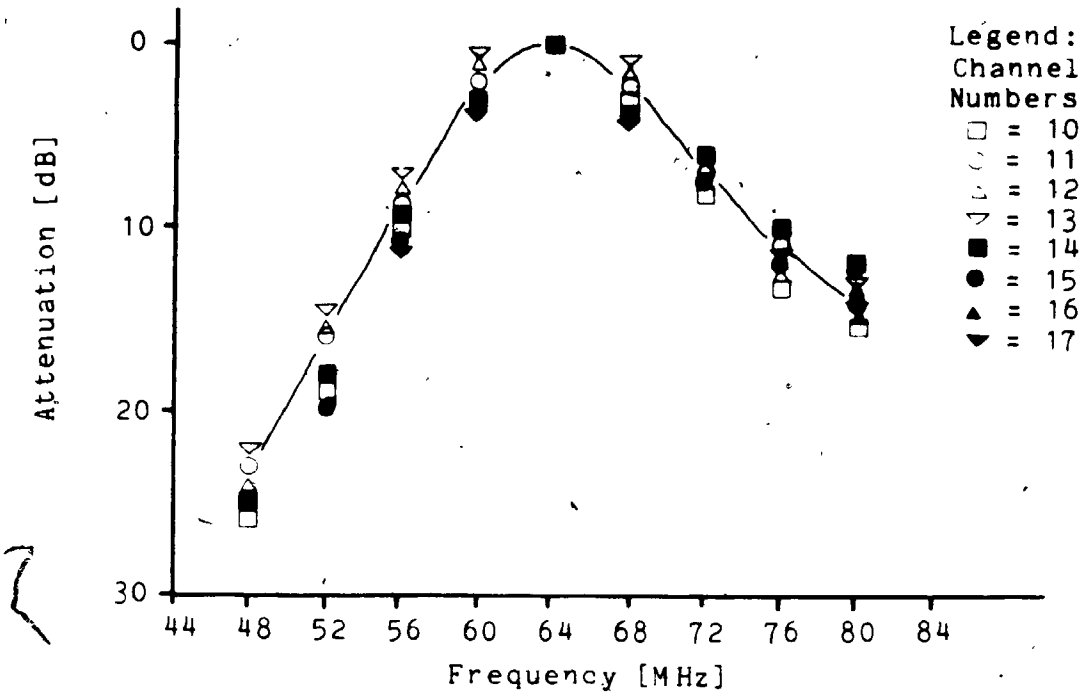


Figure 5.20a Receiver responses.

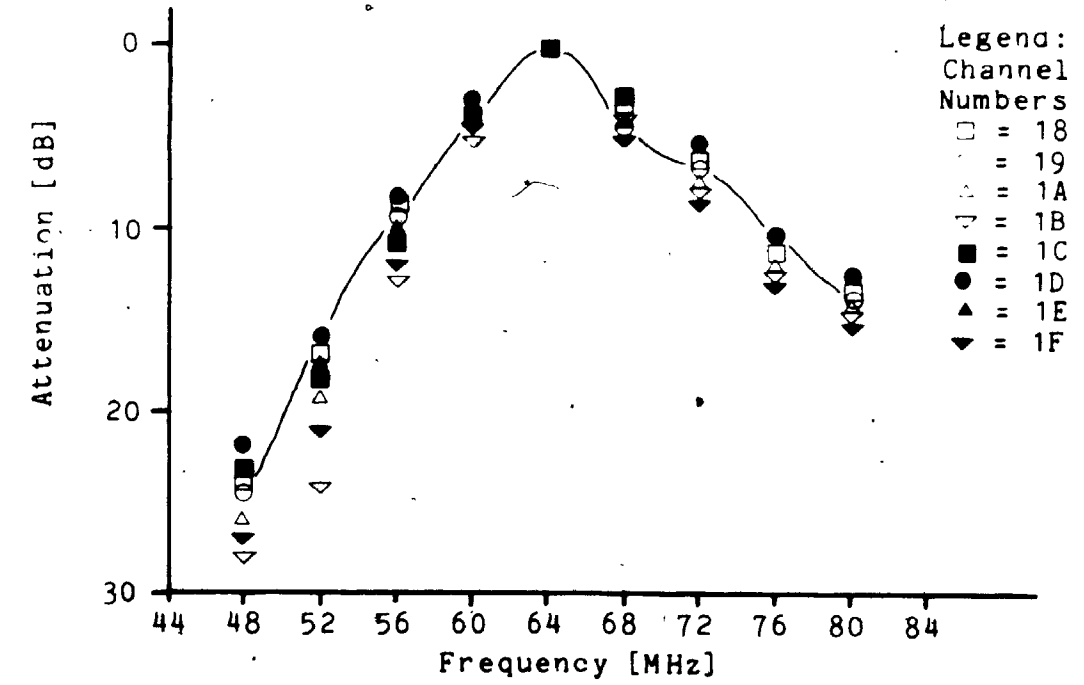


Figure 5.20b Receiver responses.

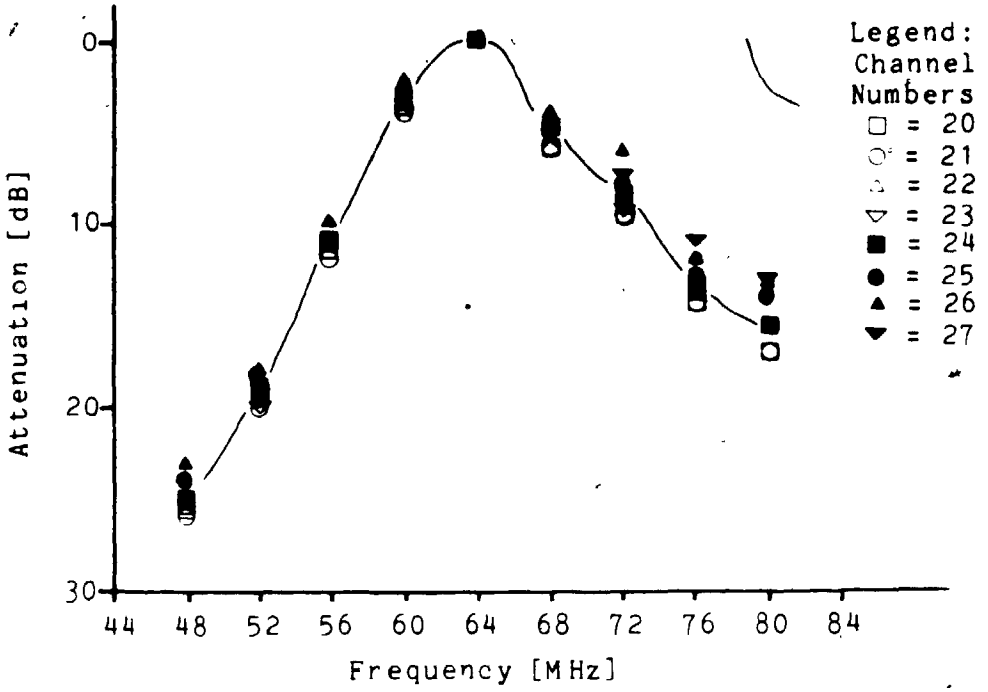


Figure 5.21a Receiver responses.

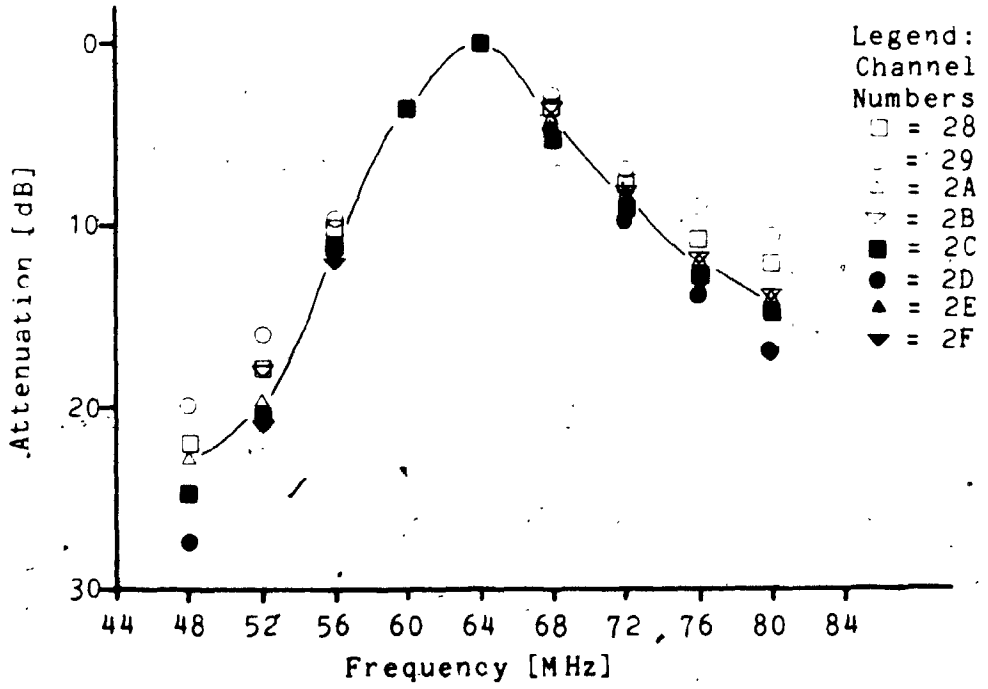


Figure 5.21b Receiver responses.

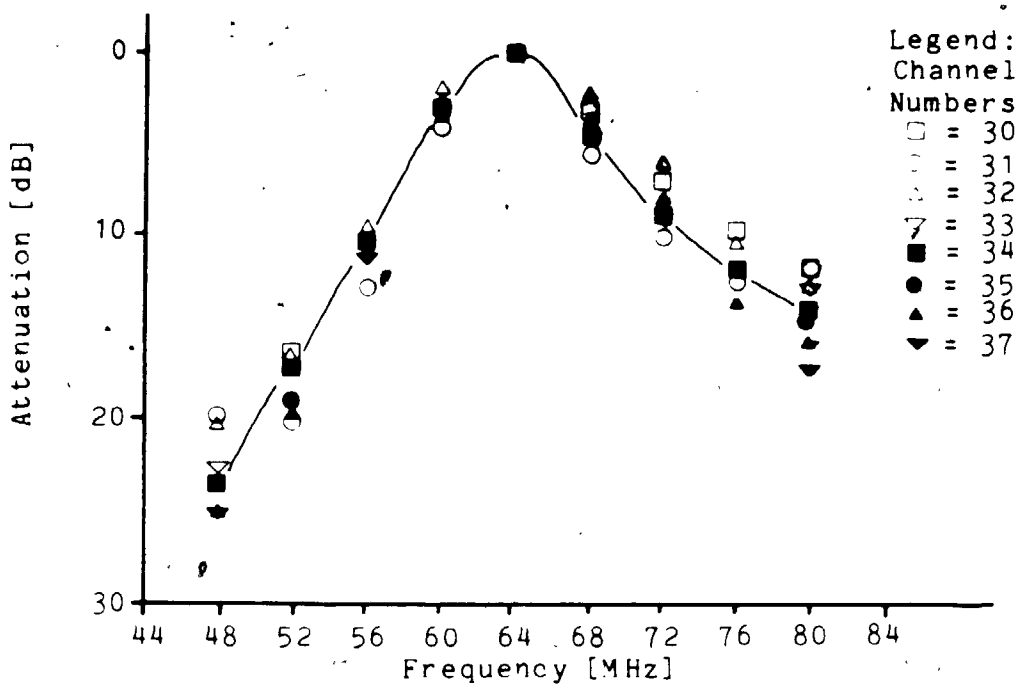


Figure 5.22a Receiver responses.

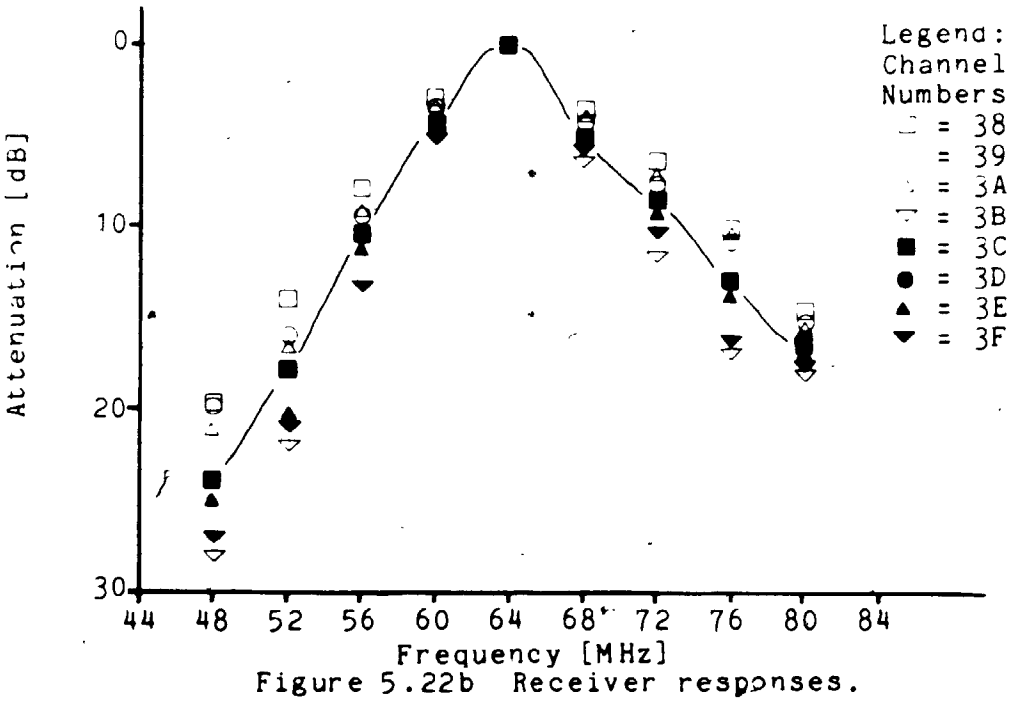


Figure 5.22b Receiver responses.

5.4 Synchronous detector, Tests and Results

Attention given to the concepts of shielding and grounding resulted in relatively noise-free signals from the receivers. Preliminary circuits were tested having a common signal ground with the digital circuitry. The common ground proved to be source of much noise even with CMOS digital circuits. Isolating the two grounds greatly reduced noise contamination of the receiver signals. There was very little noise associated with cross-talk of digital signals on the detected signals. This is the direct result of providing each digital control line and signal line with a ground return line. In doing this the effects of EMI were virtually eliminated.

Figure 5.23 shows the timing diagram for the synchronous detector. All the synchronous detectors are operating in phase. They all receive the same CHOP control signal and INHIBIT control signal. Consequently, the edges of the CHOP control signal are inhibited for all synchronous detector simultaneously, thus eliminating the problem of cross-talk between two synchronous detectors. An entire system sweep by the data acquisition system can be done in 3.1 ms which includes both signal and reference outputs of each of the 64 synchronous detectors. At this rate the system can easily perform a sweep between the edge transitions of a CHOP control signal with a frequency of 100 Hz. Likewise, a sweep can be easily performed

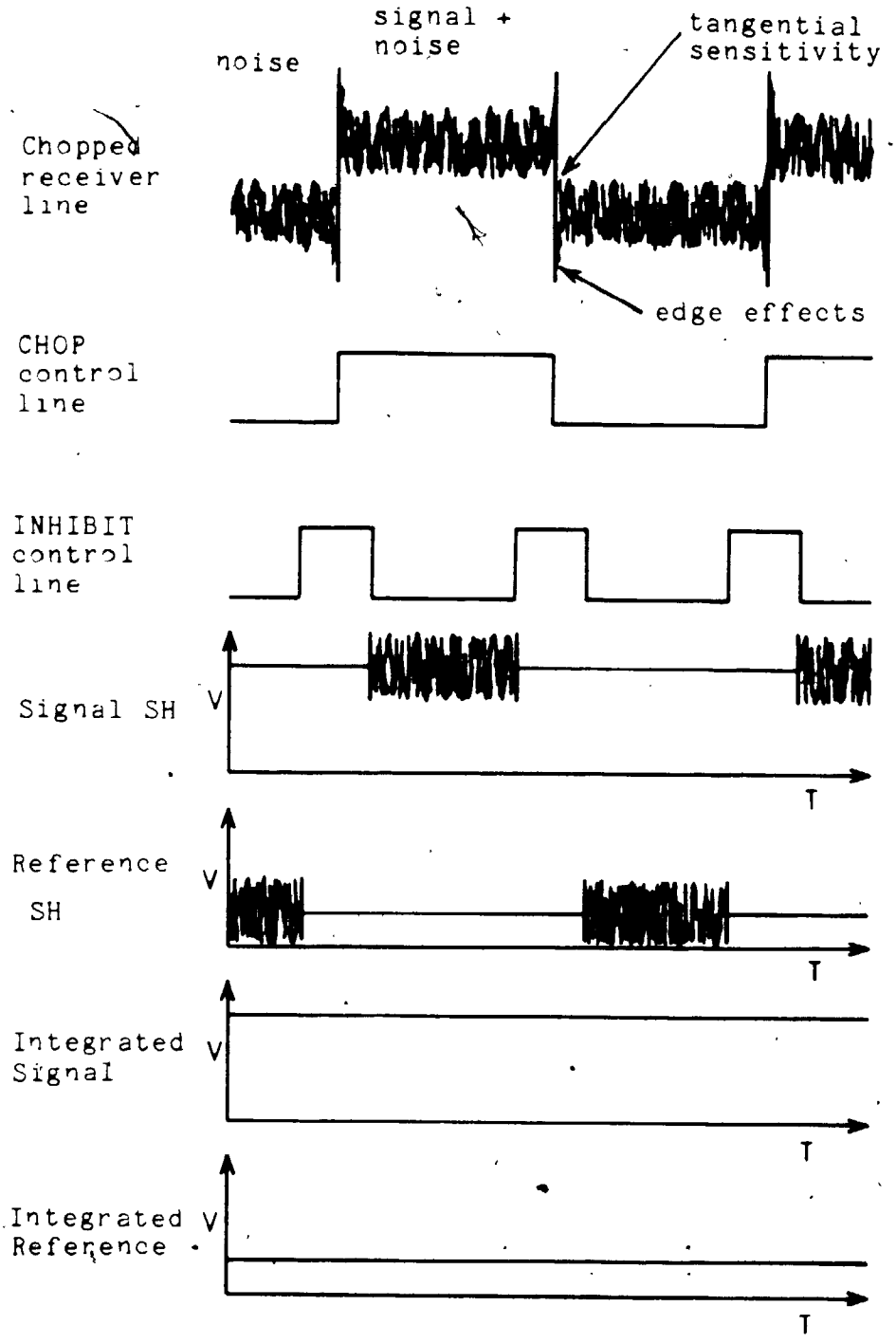


Figure 5.23 Synchronous detector timing diagram.

between the zero crossing points of the 60 Hz AC power lines. The zero crossing points are significant source of noise for some very sensitive equipment because rectifying diodes in power supplies switch on and off at this point, producing EMI at multiples of 120 Hz.

Referring to figure 5.23, the first trace is the output signal of the receiver at the level of tangential sensitivity (TSS) or the SNR is 2.5. The edge effects shown in this trace vary, depending on the type of chopper modulation in use. One type of chopper is the mechanical chopper used in optical applications. It consists of a stepping motor with a blade mounted on the rotor shaft. The blade periodically interrupts the optical beam. Edge effects produced by this type of chopper occur just as the blade cuts the beam and appears as overshoot and undershoot at the leading edge of the trace. All optical choppers exhibit phase noise and jitter to some extent on the leading and trailing edge of the chopped beam. Another type of chopper is an electronic circuit used in the processing of RF signals. The RF chopper uses PIN diodes (MPN3401) in a bridge configuration (see Appendix G). The detected output of this type of chopper is characterized by overshoot on the leading edge of the waveform and undershoot on the trailing edge. There is virtually no phase noise or jitter on the edges of the this chopper provided that the trigger signal is symmetric. The RF chopper was used extensively for

testing and calibrating the synchronous detector and the entire multichannel spectrum analyzer system.

The INHIBIT trace in figure 5.23 shows when the synchronous detector is gated off (when INHIBIT is high) to eliminate any edge effects in the chopped signal from the receiver. The width of the INHIBIT pulse can be adjusted to maximize passage of the signal or reference and to ensure removal of the edge effects.

The next two traces in the figure show the outputs of the sample-and-holds without the edge effects. This is the waveform just before the long-time constant (6.28/s) integrator. The last two traces are typical outputs of the integrator for the signal and the reference.

5.5 Local Oscillator and Frequency Multiplier

The schematic of the frequency synthesis portion of the local oscillator is shown in figure 4.11. The crystal oscillator (32 MHz) produced a voltage swing of 2 V_{pp} for the following buffer stage which triggers the first counter. The output of the buffer produced a symmetrical square-wave which is required by the TTL counter (74LS193) to ensure triggering of the counter without skipping a pulse. The counters are guaranteed to work up to 40 MHz provided that a symmetric square-wave is used. The first pair of counters divide the primary frequency by 128 to generate the main reference frequency of 250 kHz.

The voltage controlled oscillator (VCO), which is a three TTL inverter ring, had an unloaded oscillation frequency of 32 MHz. Loading the output of one of the inverters with a 60 pF trimmer capacitor allowed frequency adjustment over a range of 24 - 32 MHz. In the phase-locked loop (PLL), the VCO was controlled by a varactor diode (MV2209) which had a capacitance range of 30 - 70 pF.

Each of the 16 PLLs were adjusted by breaking the loop at the point where the error voltage line is connected to the varactor diode. The reverse voltage across the varactor was clamped at 1.5 Vdc, which was 3.5 Vdc when referenced to ground. This reverse voltage allows maximum variance in capacitance of the varactor.

The trimmer capacitor in parallel with the varactor was adjusted until the desired frequency of oscillation was obtained. The loop was closed and the PLL would then lock to the main reference frequency (250 KHz).

The 16 frequency multipliers on the receiver modules worked satisfactorily after some minor initial problems. They all produced sufficient local oscillator power at 7 dBm into each receiver. The output power was adjusted by detuning the stages in the multiplier or by changing the emitter resistor in the buffer amplifier stage. Detuning was done carefully so that the harmonic content of the output was not increased significantly. All of the frequency multipliers were tuned such that the total harmonic content was at least 20 dB less than the fundamental. The double-balanced mixer that the local oscillator drives suppresses the local oscillator and its harmonics by up to 40 dB between the LO-IF and LO-RF ports.

Leakage of RF signals from the frequency multiplier was a severe problem. Leakage from the seams of the lid was reduced by milling the edges of the box flat and milling the lip of the lid flat. This ensured continuous electrical contact around the lid. Power lines passing through the box wall were heavily capacitively decoupled to each other and passed through a ferrite bead.

Parasitic oscillation was encountered in some of the frequency multipliers. The layout of the printed circuit

board was such that inductive coupling between input and output matching networks was minimized. Provision had been made for brass shields if required and were used in all of the frequency multipliers. The parasitic oscillations were usually eliminated by simply rotating the inductors with respect to one another.

5.6 Front-end Local Oscillator Tests and Results

The front-end local oscillator provided an output power of 10 dBm into 50 ohms at 512.002 MHz. The output waveform was a clean sinusoid with harmonics suppressed by more than 15 dB.

Difficulties were encountered in obtaining the desired output. Parasitic oscillation at nonharmonic frequencies presented a persistent problem. At 1.2 GHz, internal capacitance and short lead lengths (series inductance) were such that the conditions for oscillation at this frequency were satisfied. Detuning the interstage matching networks merely shifted the parasitic oscillation frequency. Increasing the value of the emitter resistor reduced the collector current and solved the problem. The reduction in collector current reduces the gain of the transistor at high frequencies which is then incapable of supporting the parasitic oscillation. In addition, the spaces between the printed circuit board and the walls of the aluminum box were packed with aluminum foil, and more brass shim stock tabs were used around the board's perimeter to ensure good electrical conductivity.

The crystal oscillator produced a large output voltage (3 V_{pp}) for the next frequency doubler stage. The crystal oscillator was relatively insensitive to thermal drift. The output would settle down to 3 V_{pp} and 512.002 MHz within 5 minutes of operation. The oscillator

was also relatively insensitive to the tuning of the matching networks in the following doubler stages. This is due primarily to the small coupling capacitor which tends to isolate the oscillator from the other stages.

The strip transmission lines printed on the circuit board eliminated problems with stray inductive coupling due to very small coils in close proximity. This coupling was the source of some very high parasitic oscillations (1.2 GHz).

5.7 Microcomputer System Tests and Results

The entire microcomputer system has been working for nearly 3 years without any significant failure.

The first portion of the microcomputer system that was operational was the CPU board and the IO board. A primitive operating system was written in assembler code and programmed into an EPROM. The primitive operating system permitted memory modification on the CPU board and communication to a host computer through the microcomputer. The FORTH operating system was acquired and the assembler code was transferred into a file on the host computer. A cross-assembler, written for the MC6809 microprocessor, was utilized to assemble the FORTH operating system and generate an object file containing the s-record formatted object code. The s-record file was down-loaded into the microcomputer and programmed into two 4K EPROMS (D2732D). The EPROMS were installed in the CPU board and the FORTH operating was brought up.

Other components in the microcomputer system worked as described in Chapter 4. Problems that were encountered during the development of the system proved to be simple yet time consuming.

Problems associated with the microcomputer system have virtually all been traced back to connectors. Poor quality connectors would fail as a result of corrosion of contacts, failure to make contact due to mechanical

damage, and through continual use.

5.8 System Tests and Results

The multichannel spectrum analyzer (MCSA) was tested as a complete system with a simulated RF input signal. The tests consisted of dynamic responses, offset responses, thermal drift responses, adjacent channel interaction, and noise performance.

Most of the tests required an RF input signal that was chopper modulated for proper operation of the synchronous detectors. A calibrated programmable RF signal generator (Wavetek: model 3000) was utilized as the RF source. The RF signal from the generator was modulated by an electronic RF chopper (see Appendix G) to simulate the chopped RF signal from a photodetector.

During the systems operation in the reception range of 0 - 512 MHz a number of problems were revealed. Most of these were difficult to isolate but not difficult to solve. The problems can be listed as receivers failing to answer when addressed, several receivers answering to a single address, imbalance in receiver gain and offset, and software failures.

All of the tests, except the thermal drift tests, were performed when the system had thermally stabilized. The system is mounted in an open cabinet (no front or back doors). Consequently, no attempt was made to control the temperature of the system by heating elements or cooling fans. The MCSA was found to thermally stabilize within 90

minutes from cold start. Calibration frequency sweeps of the system before and after an experiment were necessary to compensate for additional thermal drift.

The first system test performed was an offset response test of the system. This test was performed with no input RF signal. The RF input on the front-end module was terminated in 50 ohms. All 64 channels were swept by the programmable RF signal generator and an analog-to-digital conversion (ADC) was performed on both the signal and reference side of the channel. Each receiver has an offset control accessible from the bottom of the receiver module. The offset for each receiver was adjusted for minimum ADC response (nominal output value of 4). They were not adjusted for zero response because the ADC does not indicate negative values. If the offset drifted below zero, offset compensation by software would produce errors.

Dynamic response tests were performed on the system for gain balance of the receivers across the channels of the system. The first test consisted of a sweep of the reception range (0 - 512 MHz) at the maximum input RF power level before any of the receivers saturated or compressed the signal. The power from the signal generator was set at 10 uW (-20 dBm) which passes through the RF chopper (8 dB attenuation) and through an attenuator pad (20 dB) before entering the RF input connector on the front-end module. The RF signal entering

the MCSA was 15.8 nW (-48 dBm). The purpose of this test was to adjust the gain of each receiver in order to produce a response with the smallest ripple possible across the reception range.

A maximum ripple of 2 dB in the response was finally obtained by adjusting the variable gain amplifiers in each receiver. The response is plotted in figure 24.

The ripple of 2 dB across the reception range can be compensated for by software. A calibration frequency sweep of the reception range at a fixed input RF power level can be performed before and after the experiment for verification. In addition, a calibration sweep for offset and thermal drift compensation can be performed.

A series of dynamic response tests were performed to establish the linearity of the channels with respect to received RF power. These tests were performed at a number of fixed input power levels and the results for a group of channels are plotted in figures 5.25a, 5.25b, 5.26a, and 5.26b. The responses shown were done without software gain compensation, but were done with offset compensation. The selected channels (channel numbers $20 to $2F) are a single channel from each of the 16 receiver modules.

Ideally, the responses in the above figures should be a linear function of the ADC value with input power. The square-law detectors in the receivers should produce an output voltage that is directly proportional to the input power level. The operation of the synchronous detector

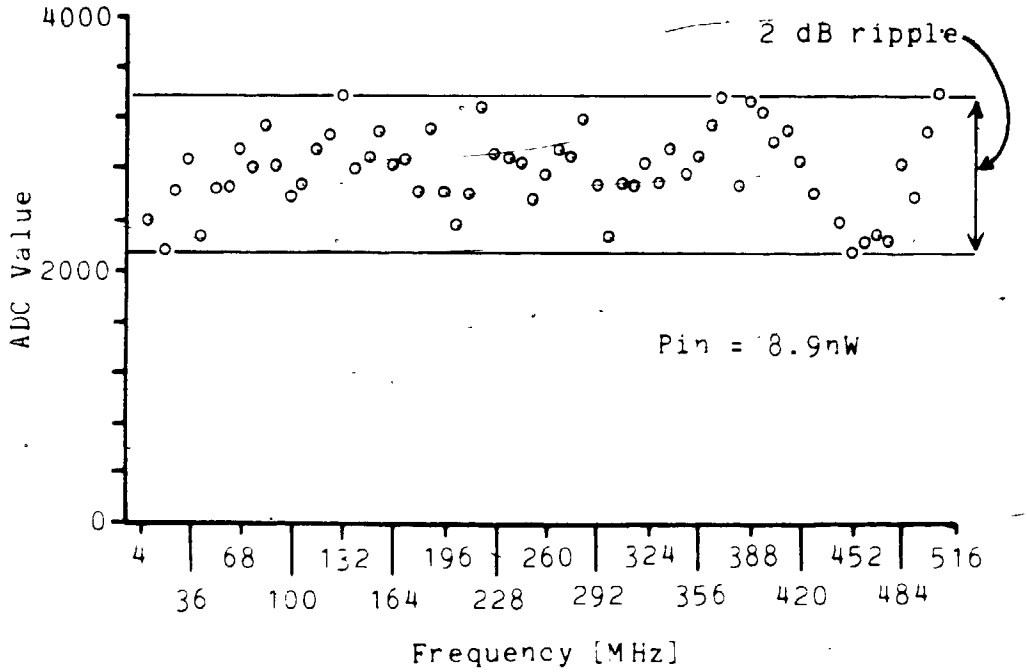


Figure 5.24 Linear response to frequency sweep.

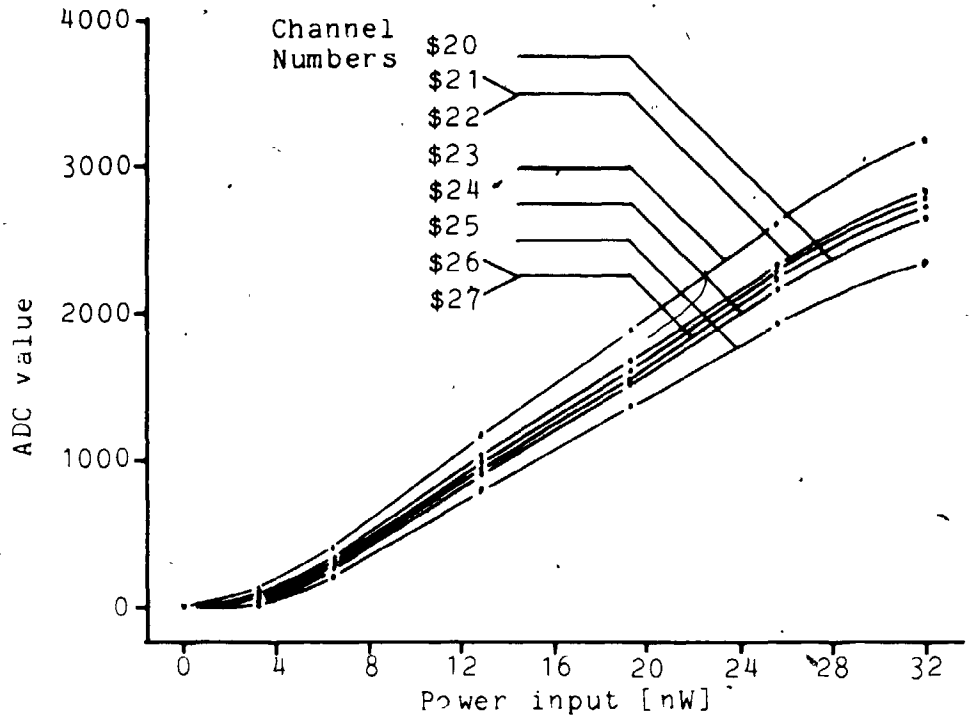


Figure 5.25a Dynamic response of selected signal channels ($20 - $27).

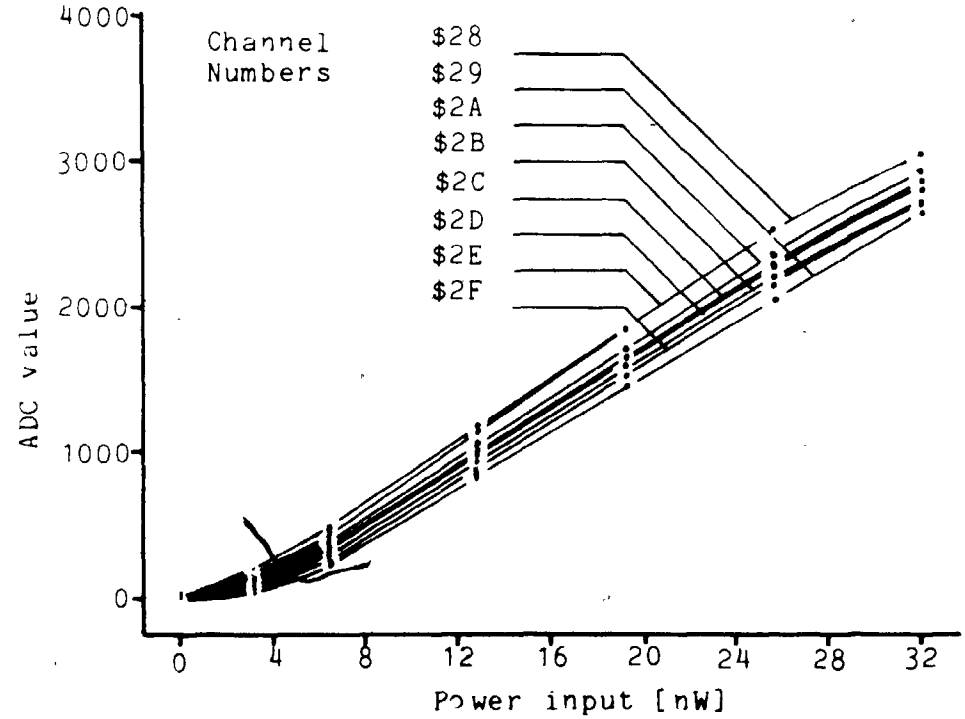


Figure 5.25b Dynamic response of selected signal channels ($28 - $2F).

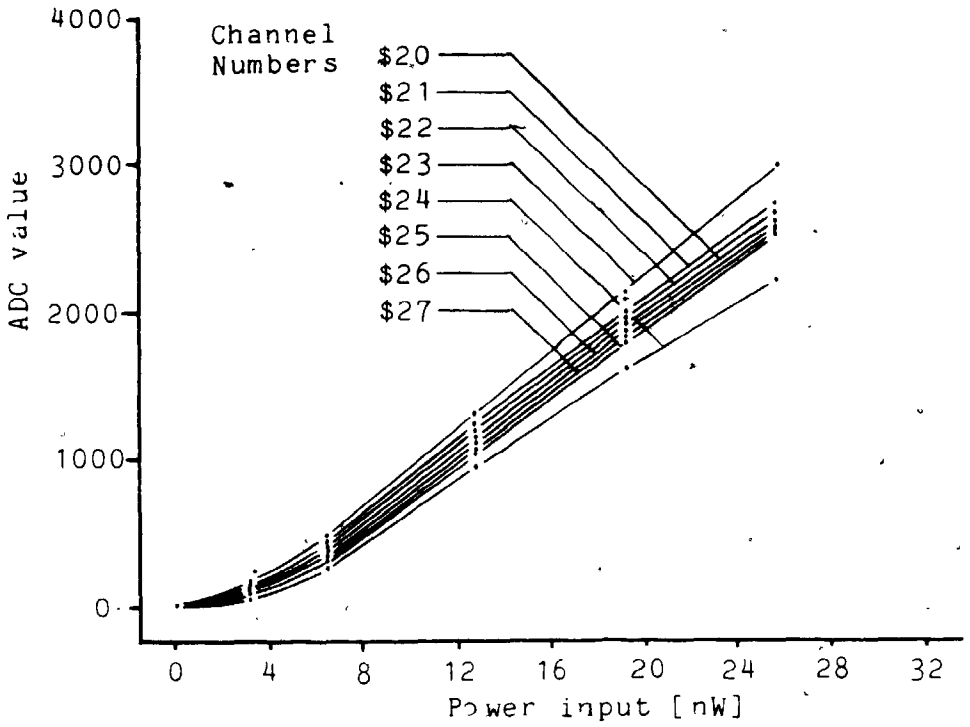


Figure 5.26a Dynamic response of selected reference channels ($20 - $27).

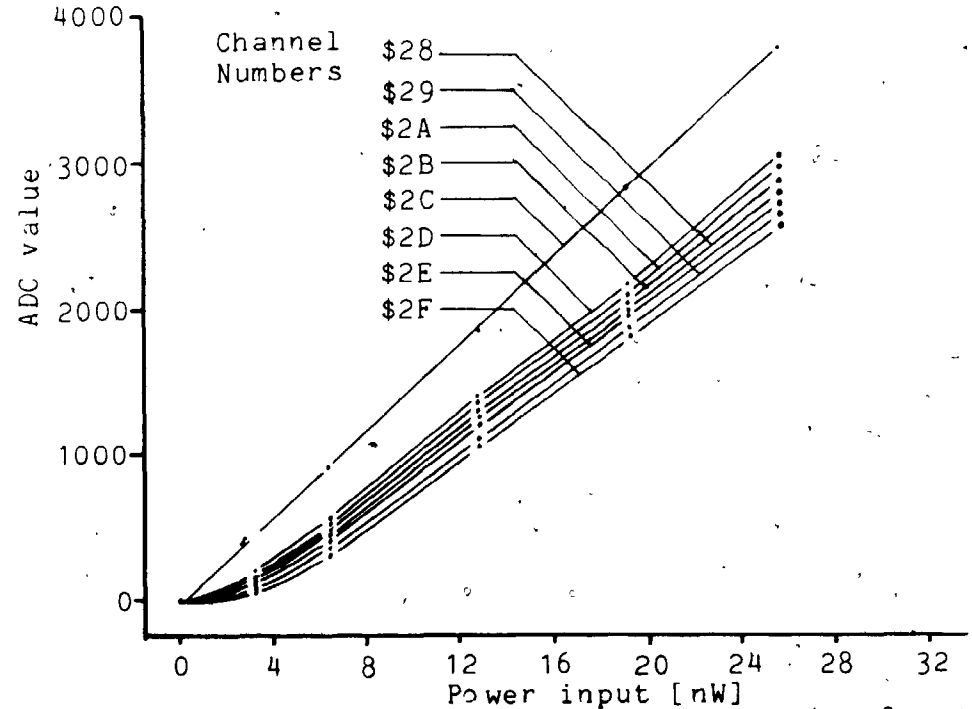


Figure 5.26b Dynamic response of selected reference channels ($28 - $2F).

should not affect this condition provided that the detector signal is within the linear range of its amplifiers and the signal is present long enough for the long-time integrators to settle.

The responses in figures 5.25a and 5.25b were performed on the signal side of each channel. All of the responses have a linear characteristic between 6 nW and 26 nW. Below and above this range, all responses exhibit a slight deviation from linearity. The deviation at the high power end is due partly to the non-ideal square-law response of the detector diodes and to nonlinearity of data selector circuits and amplifiers. The low power deviation is due to hysteresis in the hold capacitors of the sample-and-holds.

The dynamic response of the reference side of the receivers is demonstrated in figures 5.26a and 5.26b. All of the responses have a linear characteristic between 6 nW and 26 nW and show the same deviation from linearity as did the previous figures. The gain on the reference side of the channels is slightly higher than the signal side, because the impedance of the RF chopper (when it is switched on) is slightly different between the reference port and the signal port.

A thermal drift test was performed on all of the channels of the MCSA. A typical set of responses is shown in figure 5.27a. All of the responses shown were done at a constant input power level of 19 nW (-47 dBm) to ensure

a response in the linear range indicated by the dynamic response tests. Software compensation was done for the offset, but not for the gain.

The thermal gain drift response shows that all responses settle to a final value within 90 minutes from cold start. The cold start temperature was the same as the room ambient temperature (20°C) and final operating temperature, 90 minutes after cold start was 36°C measured in the centre receiver module. The final drift response values were typically 50% of their cold start values. All responses had similarily shaped thermal response curves and reached thermal equilibrium together.

The thermal gain drift is due to gain variations throughout the system and not to offset drift. The gain of all the RF amplifiers change slightly due to changes in temperature (typically 1% for a 10°C change). Gain variation can be caused by variation in the output of the local oscillators. All of the local oscillators are phase-locked, but are not amplitude compensated. The IF output of each mixer in the receiver is a product of the RF signal and the local oscillator and consequently, is proportional to the magnitude of these.

The main cause of gain variation are the square-law detectors which are subject to thermal drift both in gain and offset. Thermal offset drift was compensated by hardware through the use of a matched reference detector diode placed beside the detector diode.

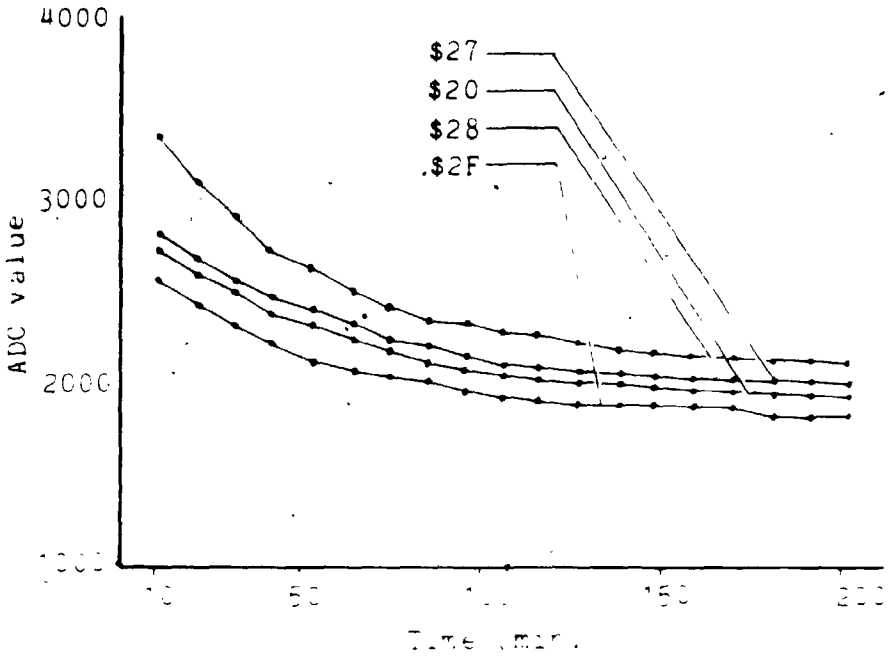


Figure 5.27a Thermal gain drift response.

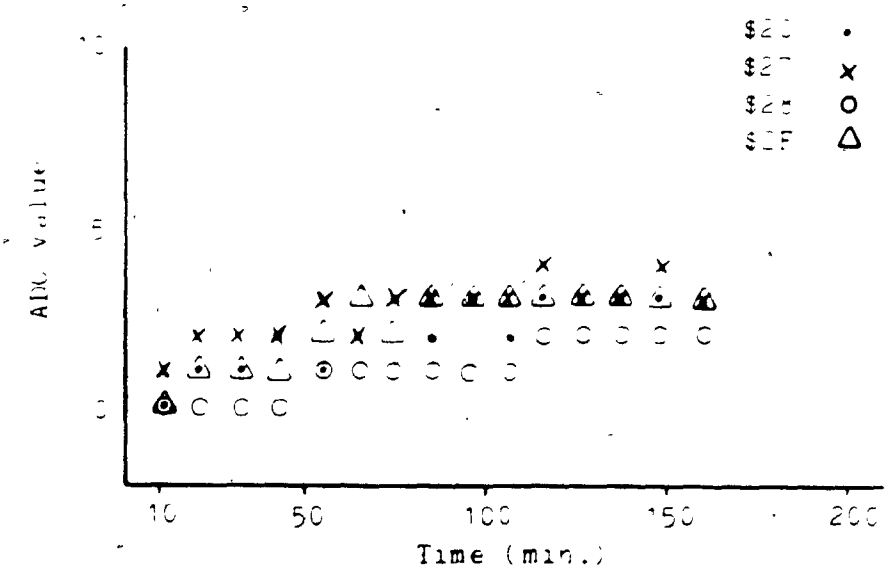


Figure 5.27b Thermal offset drift response.

Gain variation due to thermal effects of the square-law diode can be explained by considering the diode equation (eqn. 3.7) and its Taylor series expansion (eqn. 3.8). The coefficient for the ΔV^2 can be shown to be:

$$\frac{d^2I}{dV^2} = I_s\left(\frac{q}{nKT}\right)^2 e^{qV_d/(nKT)} \qquad 5.3$$

The ratio of the coefficient at two temperatures (T_1, T_2) can be shown to be:

$$C = \frac{d^2I_2/dV_2^2}{d^2I_1/dV_1^2} = \left(\frac{T_1}{T_2}\right)^2 e^{(1/T_2-1/T_1)qV_d/(nK)} \qquad 5.4$$

For $T_1 = 293^{O}K$, $T_2 = 309^{O}K$, and $V_d = 0.30$ V, the ratio of the coefficients, C, becomes 0.492. This accounts for virtually all the thermal drift noted experimentally.

Figure 5.27b shows the thermal drift of the offset value for each receiver. The responses settle within 90 minutes to a low nominal value of 2. Fluctuations in the offset responses are due partly to the ADC conversion error when an analog signal is close to a transition point from one value to the next of the ADC. The result is an ambiguity of 1/2 of the least significant bit (LSB) in the ADC digital output. The offset thermal drift is, theoretically, a function of temperature given by the diode equation. The ratio of the function at two different temperatures (T_1, T_2) is the same as equation 5.4 but without the T_1/T_2 factor. For the same conditions

for T_1, T_2, and V_d, mentioned above, the offset should drift to 0.54 of its original value. Figure 5.27b shows that the compensation effect of the second thermal reference diode worked well in cancelling the offset thermal drift.

The long term effects of output drift are plotted in figure 5.28 for a few representative channels. The long term response test was performed by sweeping the frequency reception range of the MCSA with a 19 nW (-47 dBm) RF signal every 10.5 minutes for 3 hours. The programmable RF signal generator was used as the signal source. Over the period of 200 minutes commencing 6 hours after cold start, the output value drifts down by 1.3% in the worst case. The maximum ripple on the curves is 8 units or 0.5%. The output of the signal generator was level controlled and did not contribute to the drift.

Short term drift is plotted in figure 5.29. The data was sampled every 2 seconds for 120 seconds. The data is a repesentative portion of a larger set of data that was taken over a period of 20 minutes. The data fluctuates about a mean value by one or two bits. The fluctuation is partly due to conversion error of the ADC and partly due to thermal noise.

The effects of adjacent channel interaction are shown in figures 5.30a, 5.30b, 5.30c, and 5.30d. The test was performed at an input RF signal level of 19 nW (-47 dBm) using software compensation for both offset and gain. The

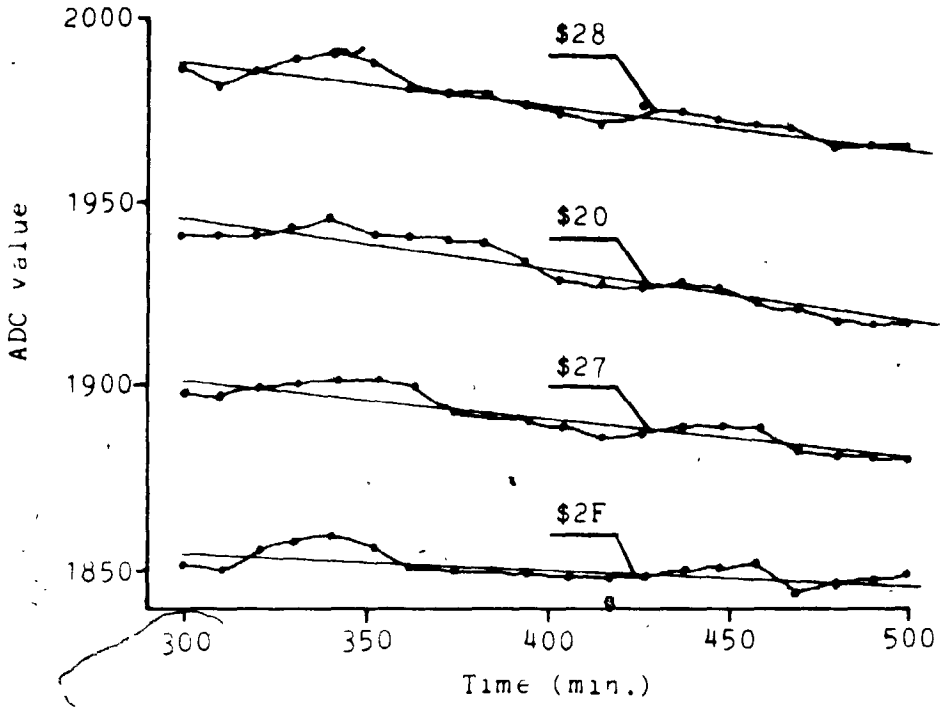


Figure 5.28 Long term thermal drift response.

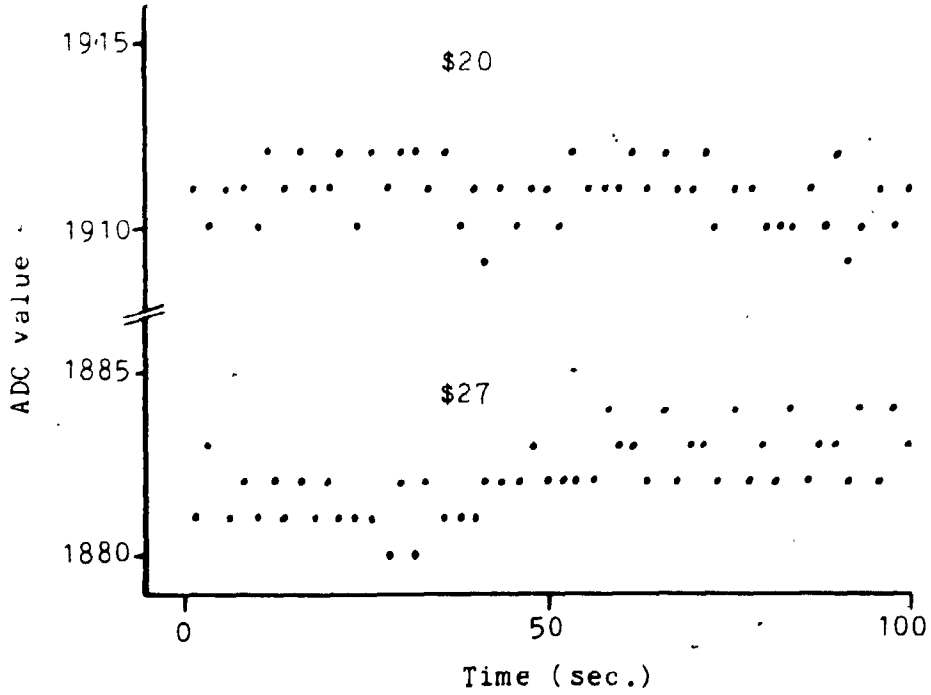


Figure 5.29 Short term thermal drift response.

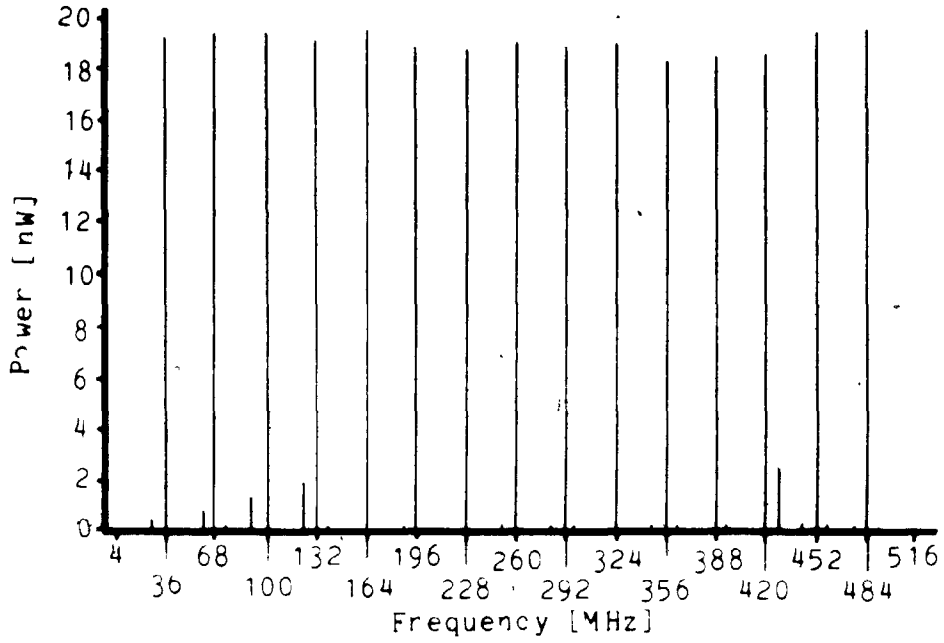


Figure 5.30a Adjacent channel interaction.

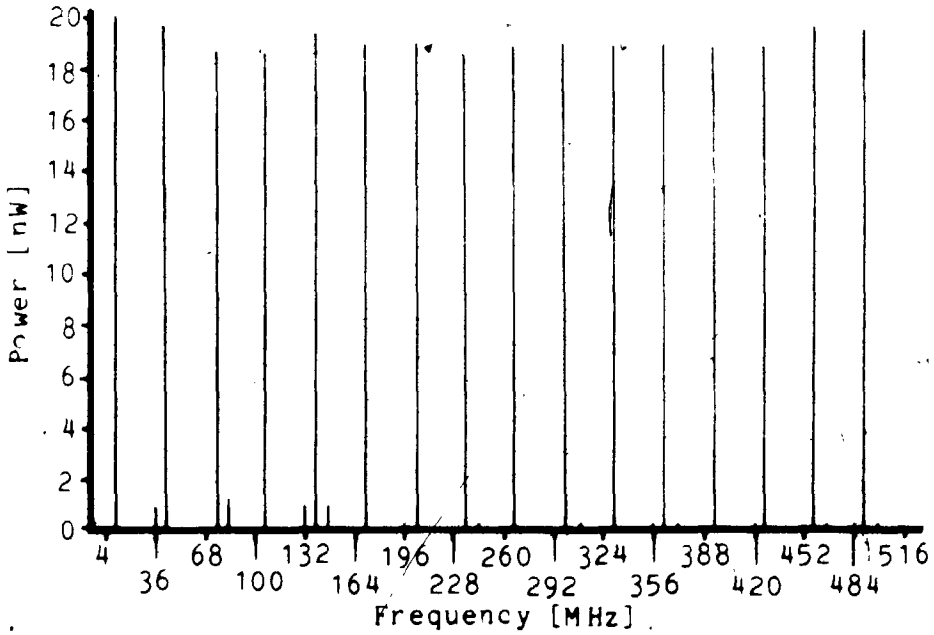


Figure 5.30b Adjacent channel interaction.

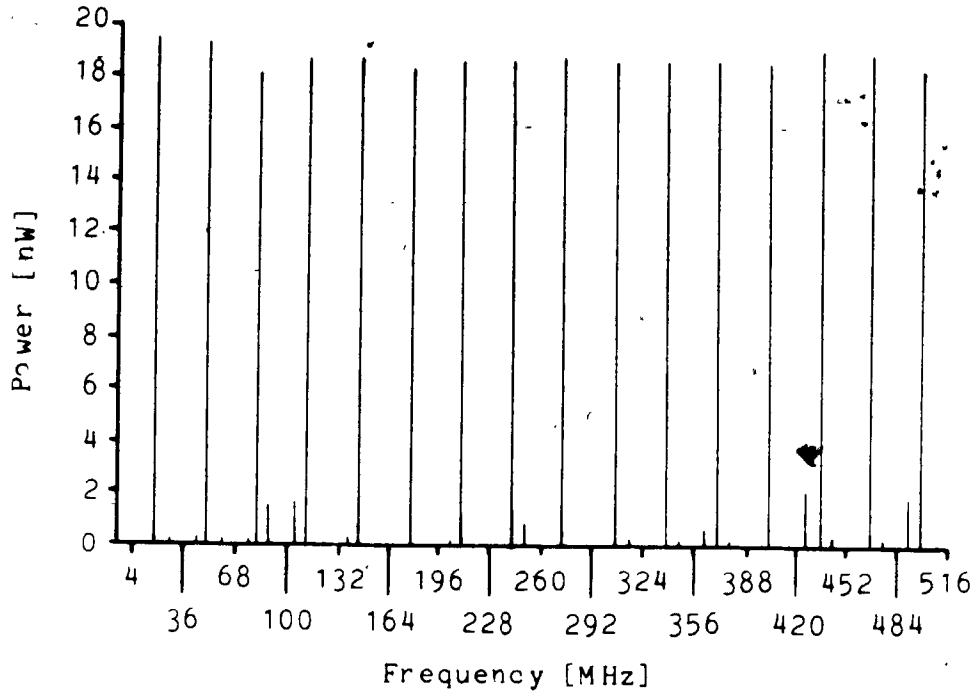


Figure 5.30c Adjacent channel interaction.

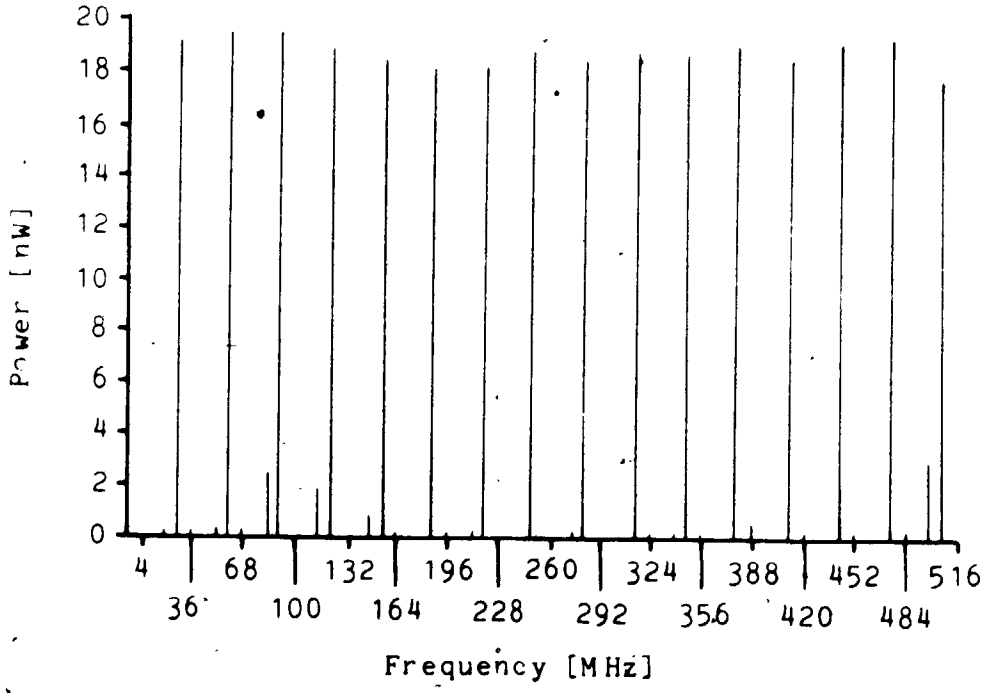


Figure 5.30d Adjacent channel interaction.

resulting response is flat with a maximum ripple of ±0.13 dB. Interaction between adjacent channels is limited to the very next channel only. The minimum isolation between channels was found to be 8.2 dB for the pair of channels at 500 MHz and 508 MHz. Typically the isolation is greater than 10 dB between adjacent channels with many having greater than 20 dB isolation.

The standard procedure for measuring noise figure of a system requires the use of a calibrated noise source and a means for measuring noise power. The first step is to terminate the input of the instrument by a matched resistive load and measure the output noise power ($n_r = KT_rB$). Next, the noise generator is connected to the input and the output noise power ($n_g = KT_gB$) is measured. It is convenient to have an adjustable noise generator so that the output power (n_g) can be set to twice n_r. In this case, the noise figure can be found from (Kraus, 1966):

$$F = 1 + \frac{T_r}{T_o} = \frac{T_g}{T_o} - 1 \qquad 5.5$$

$$T_r = T_g - 2T_o$$

where T_r = receiver noise temperature

T_g = noise generator temperature

T_o = ambient temperature

For the MCSA, the detection limit is determined by a one bit fluctuation in the output of the ADC. The MCSA exhibited virtually no background system noise when configured without auxiliary RF amplification. The auxiliary amplification stage (50 dB) was added to the front-end module between the low noise front-end amplifiers and the 2-way power splitter. The amplifier stage has a noise figure of 6.3 dB but since it follows the front-end amplifier, it has a minimal effect on the total noise figure of the front-end amplifiers. The additional gain raised the noise floor of the system sufficiently across the reception range to produce an adequate ADC value for noise measurements. The ADC values are directly proportional to RF power in the channel since the receivers incorporate square-law detectors.

Noise was injected into the front-end input by a calibrated noise generator (Mega-Node). The generator derives noise from a specially designed vacuum tube diode. It also has a calibrated meter from which the noise figure can be read directly.

The noise figure of the MCSA was found to be 3.05 ± 0.3 dB across all 64 channels. This corresponds to a receiver noise temperature of 306 ± 40 K. In general, a good quality receiver has a noise figure of a few dB. The noise figure of a receiver is determined mainly by the noise figure of the first amplifier. The front-end amplifier used has a noise figure of 2.7 dB. The 0.35 dB

difference can be accounted for by considering loss in the front-end cables and noise due to the auxiliary amplification stage.

The sensitivity of the system can be calculated from equation 3.14 which is an expression for the minimum detectable signal temperature, ΔTmin, of the MCSA. The equivalent predetection bandwidth, B_{HF}, is 1.5 times the IF bandwidth or 12 MHz. The integration time, t_{LF}, is 2 times the RC time constant (6.3 s) of the long-time integration or 12.6 s. The system noise temperature was found to be 306 K. The above values when substituted into equation 3.14 give a theoretical minimum detectable signal temperature of 0.050 K. This implies a minimum detectable signal power ($Pmin = K\Delta TminB_{HF}$) of 8.28×10^{-18} W (-141 dBm).

The minimum detectable signal power of each channel of the MCSA was measured. The auxiliary amplifier stage that was used in the noise figure measurements was also used here.

The minimum detectable signal power (Pmin) is that input power level required to produce a signal-to-noise ratio (SNR) of unity. Since it has been shown that the output of the square-law detectors of the receivers is directly proportional to input power, the conversion values of the ADC are directly proportional to power. An SNR of unity occurs when the peak value of signal-plus-noise exceeds the peak value of noise alone by

the RMS deviation value (or standard deviation) of the noise.

A calibrated RF signal generator was used as a test signal source and was modulated by the electronic RF chopper. The test signal was synchronously detected and its input level was adjusted for the conditions of unity SNR. The test procedure was facilitated by a test program written in FORTH that automatically calculated the mean and standard deviation of the ADC values.

After accounting for losses in the RF chopper and attenuators on the output of the signal generator, the minimum detectable signal power (Pmin) was found to be -138 dBm. This signal power was found to be uniform (less than $\pm$1 dB) across all of the channels.

The minimum detectable signal power was found to be sensitive to the chopper frequency. At low chopper frequencies (less than 5 Hz), Pmin would degrade to about -124 dBm. At high frequencies (50 Hz or more), Pmin would reach -138 dBm. This is the result of low frequency noise from the chopper control signals. Despite careful consideration of the problems of both high and low frequency noise and interference (see chapter 3), some influence of these spurious signals was observable at the detection limit of the system.

In general, the spectrum of the MCSA at high amplification levels was noise-free. However, interference and noise were detectable in those channels

that correspond to radio communications bands. In particular, problems were encountered in the citizen's band (CB, 26.965 - 27.405 MHz), FM band (88 - 108 MHz), and local TV band (CFPL channel 10, 192 - 198 MHz). This environmental noise was typically 10 dB greater than the system backgroud noise. Improved shielding of the front-end amplifiers may reduce the problem, but would not solve the problem of pick-up by cables connecting the experimental apparatus with the MCSA.

Chapter 6

An Optical Heterodyne Spectrometer

6.1 Introduction

Two optical heterodyne experiments were performed for verification of the capabilities of the multichannel spectrum analyzer (MCSA). The MCSA can spectrally resolve the RF difference frequencies arising from the interference of optical signals. Similarily, the MCSA can spectrally resolve a stellar optical source with a resolution from 10^6 to 10^8 of the optical part of the spectrum.

The MCSA was used in the detection of the intermodal beat frequencies of a single He-Ne laser operating at 632.8 nm. The MCSA was also used in the coherent detection of RF signals resulting from the heterodyning of two He-Ne lasers.

The first optical laser heterodyne detection experiments were performed by Nieuwenhuijzen (1970) on a number of bright stars and the planet Jupiter. The instrumentation consisted of the 200-cm telescope at the Ondrejov Observatory, combining optics, a PIN photodiode (HPA 4204), RF amplifier, RF detector, lock-in amplifier, and a He-Ne laser (632.8 nm).

The laser, being a monochromatic and spatially coherent source, is ideal as an optical local

oscillator for the heterodyning of optical signals.

The linewidth and lineshape of the atomic transition determines the linewidth and shape of the laser line. Both stimulated and spontaneous emission processes occur during laser action, with the spontaneous emission contributing to narrow band gaussian noise. This noise is the limiting noise source in a laser (Siegman, 1971).

Figure 6.1a shows the structure of a He-Ne laser tube (Spectra Physics: model 155) and figure 6.1b shows the mechanism of operation of the laser.

Figure 6.1b shows how some energy levels of He and Ne match. Excited He atoms have relatively long life times and some may transfer energy to Ne atoms by collision. The pumping action takes place between electrons and He, and between He and Ne.

Under strong pumping action, a population inversion may be generated and the Ne atoms may produce laser action on several different transitions (632.8 nm, 1.15 μm, and 3.39 μm). The laser frequency lies within the characteristic resonant frequency band of the medium. This band corresponds to the gain curve of the laser.

The He-Ne laser used in the optical heterodyne experiment is specified to have an output power of 0.5 mW, a wavelength of 632.8 nm, a longitudinal mode separation of 550 MHz, and a TEM_{oo} spatial mode when operating.

The optical signals were detected by a junction photodetector. For fast response times a PIN photodiode

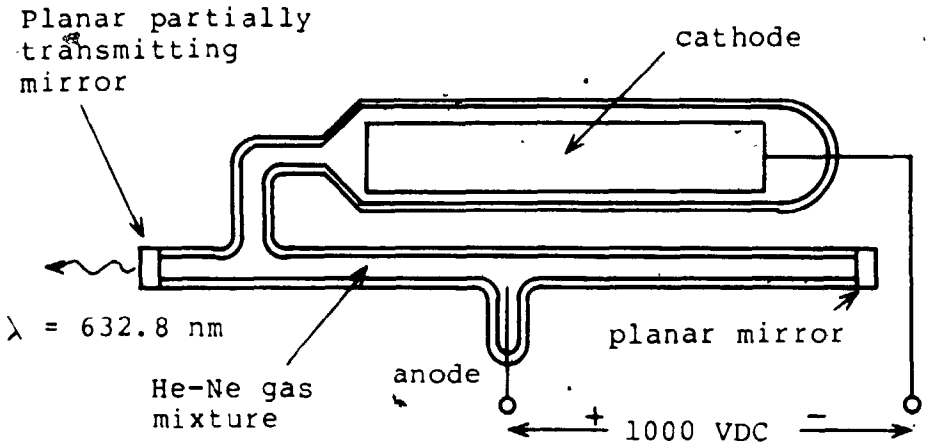


Figure 6.1a He-Ne laser tube.

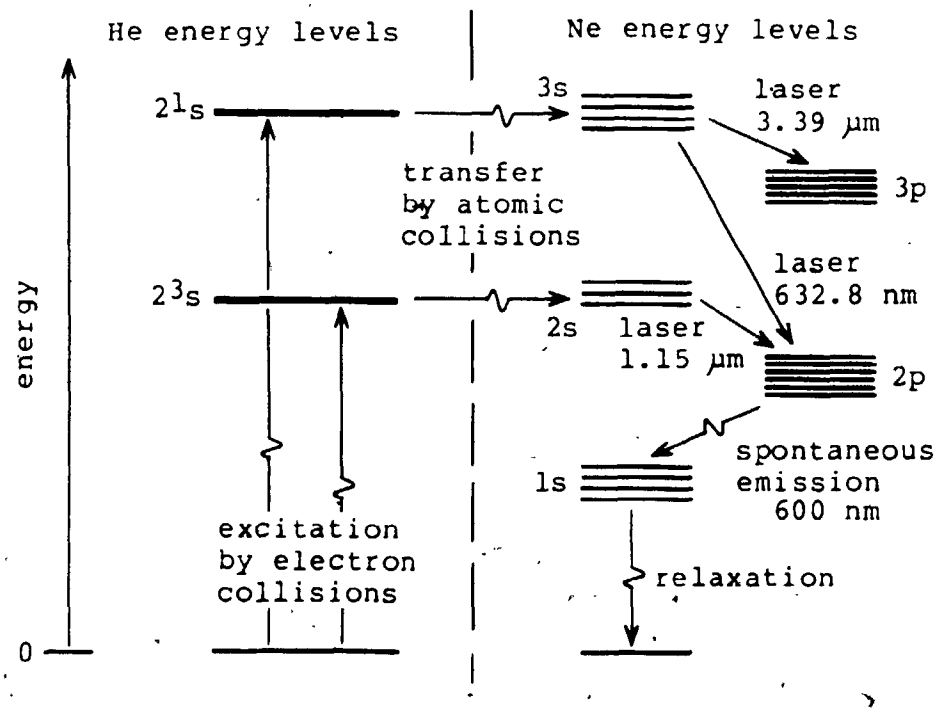


Figure 6.1b He-Ne laser operation.

was used (Philips: BPX65).

A typical PIN photodiode is constructed from three layers of p-type, intrinsic, and n-type silicon semiconductor. The depletion region formed by the intrinsic (undoped) layer provides a larger depletion depth which results in much smaller capacitance. The reduced capacitance improves the response time greatly over p-n photodiodes (Budde, 1983). Typical response times when loaded with 50 ohms is 0.5 - 1.0 ns.

The PIN photodiode is a planar silicon device with a wavelength response of 200 - 1100 nm and a peak response near 850 nm. The peak responsivity is 0.55 A/W at 850 nm (0.40 A/W at 632.8 nm, with a quantum yield of 0.8 electrons/photon (Budde, 1983). The noise equivalent power (NEP) is 3.3×10^{-14} W/$\sqrt{Hz}$ and detectivity (D* is 3.03×10^{12} cm$\sqrt{Hz}$/W for a reverse bias of 20 V. The dark current or leakage current of a reverse biassed photodiode limits the detection of small signals. A guard ring around the radiant sensitive area shunts the surface leakage current around the load resistor (Budde, 1983).

The photodiode will produce an RF current at the difference frequency of two optical sources only when their polarizations are not perpendicular (Nieuwenhuizen, 1970). The He-Ne laser used in the optical experiments is randomly polarized.

6.2 Method

The detection of optical signals at a wavelength of 632.8 nm was accomplished by a PIN photodiode (BPX65) with 27 dB of wideband preamplification to provide a spectral response up to 700 MHz (1.4 ns). Details of the detector/preamplifier design are shown in figure 6.2.

The photodiode was reverse biassed with 8.3 V to reduce the capacitance of the junction to about 8 pF from its zero bias value of 15 pF. With a nominal 50 ohm load resistor, the 3 dB spectral response point occurs at 423 MHz.

Preamplification of the detected signal is performed by a pair of wideband hybrid modules (MWA110) that are designed for 50 ohm characteristic impedance systems. The collectors of the modules were biassed for 9 mA to provide 13.5 dB of gain in each stage. A shielded, 9 V battery, power supply was used to provide an uncontaminated source of power. The noise figure of the preamplification stage is determined by the first amplifier and is nominally 4 dB.

Since the detector/preamplifier is the most sensitive part of the optical heterodyne system, it was mounted in two small diecast aluminum shielding boxes to exclude contaminating external RF signals.

The first optical heterodyne experiment performed was the detection of the intermodal beat frequency of a single

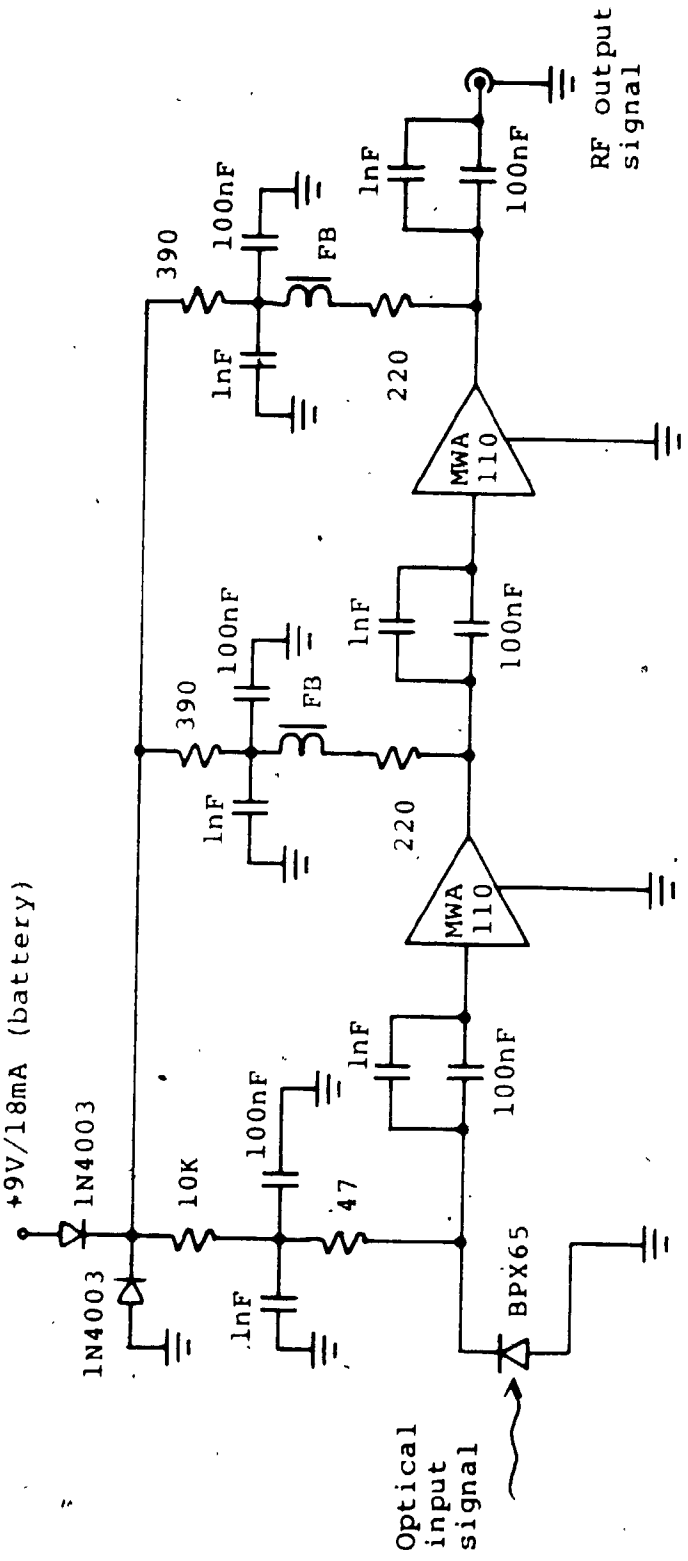


Figure 6.2 Optical detector and preamplifier design.

He-Ne laser (Spectra Physics, model 155). The setup, shown in figure 6.3, was operated with only the local oscillator (LO) laser functioning.

The LO laser beam is reflected 90° by a planar mirror, passes through a coated glass beam splitter (Amersil Inc., Suprasil fused silica), and illuminates the photodiode of the detector/preamplifier to produce an RF signal. The detected RF output passes through auxiliary wideband amplification (35 dB) and is then frequency shifted by a wideband mixer (Mini-Circuits: model SBL-1X, f_{LO} = 194 MHz) into the reception range of the MCSA. The output of the mixer passes through a chain of attenuator pads for amplitude control and then onto the MCSA for spectral processing.

The second optical experiment performed was the heterodyning of two He-Ne lasers (Spectra Physics, model 155) and the detection of the beat frequencies between the two lasers. The setup is shown in figure 6.3 but without the mixer.

The LO laser beam is reflected 90° by a planar mirror, passes through a glass beam splitter, passes through an adjustable aperature, and then illuminates the sensitive area of the photodiode. The signal laser beam is partially reflected 90° by the glass beam splitter where it is combined with the LO laser. The internal reflection of the beam splitter produces an off axis image of the signal laser parallel to the main reflection and is

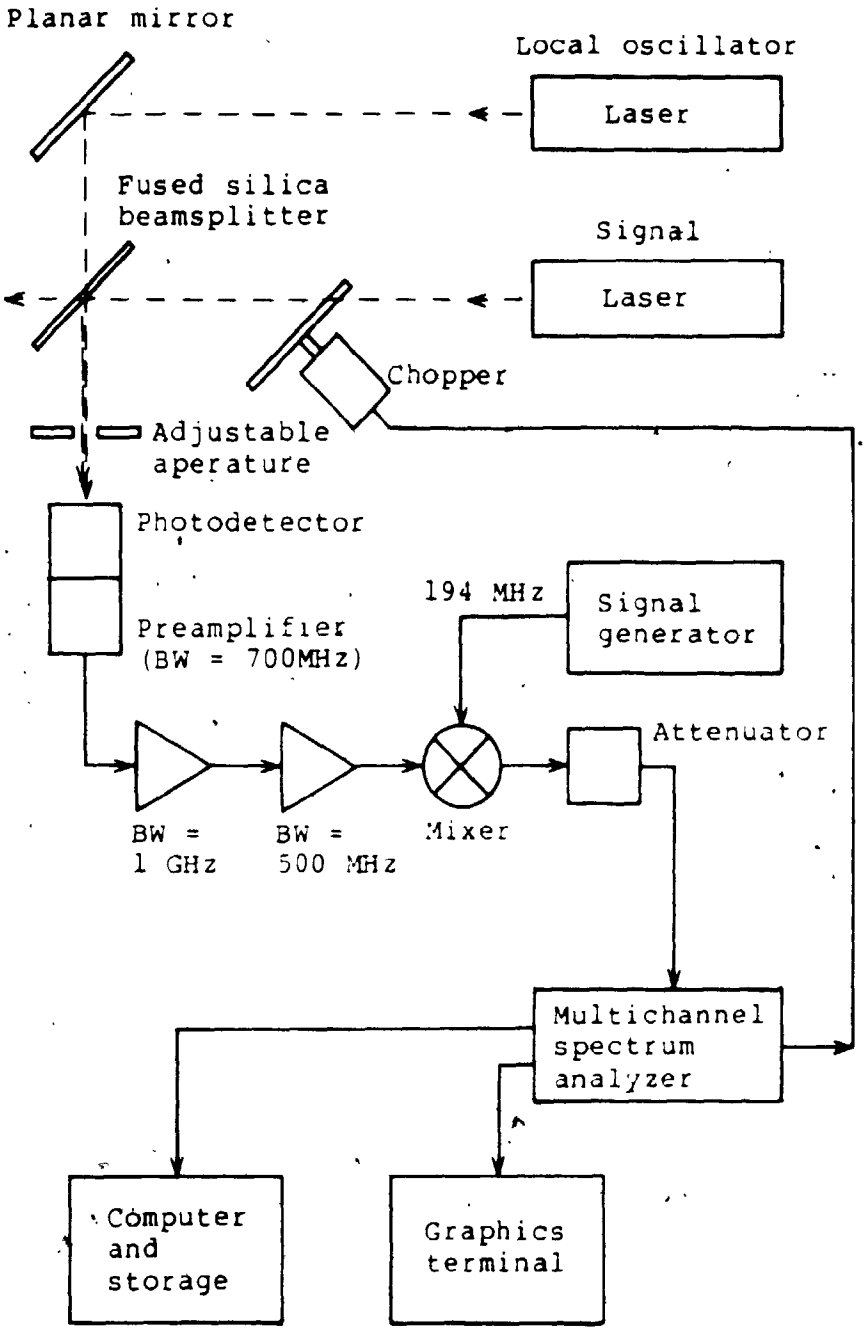


Figure 6.3 Optical heterodyning of He-Ne lasers.

stopped by the adjustable aperature.

Careful alignment of the optical equipment ensured that the signal and LO laser beam were travelling parallel paths after the beam splitter. This also ensures that the wavefronts of the two lasers are aligned and that any interference patterns are much larger than the sensitive area of the photodiode.

The detected RF signals are preamplified at the detector stage and then amplified again (35 dB) by the auxiliary amplifiers. The amplified signals pass through a chain of attenuator pads for amplitude control before entering the MCSA for spectral processing.

6.3 Results and Discussion

The output powers of the two He-Ne lasers were measured with a power meter (Scientech, model 36-0001, 36-2001) and both were found to be 0.6 mW. The LO laser, after passing through the optics, illuminated the photodiode with 0.35 mW of power. The coated beam splitter (aluminum coating, 50% transmissivity) reflected 0.25 mW of power. The uncoated flat glass window on the case of the photodiode has a transmissivity of 96% (fused silica at 632.8 nm) and reduces the illumination power to 0.336 mW.

The responsivity of 0.4 A/W for the photodiode implies an expected induced DC current of 134 μA for incident power of 0.336 mW. The measured average DC current was found to be 109 μA. The difference is 23% and can be attributed to misalignment of the LO laser on the detector surface.

Low frequency noise was present in the induced current. A noise current of 0.35 μA was directly attributable to 60 Hz power line contamination of the laser signal. Noise current spikes of 2 - 10 μA that appeared every few seconds, were the result of microphonic pickup from the chopper drive.

The optical homodyne experiment demonstrated that more than one axial mode frequency is present in the He-Ne laser by the detection of an intermodal beat frequency at

550 MHz. A calibrated signal was sent down the detector in place of the photodiode. In this way the intermodal beat signal power was found to be 0.5 nW (-63 dBm) which corresponds to 6.3 uA sourced by the photodiode into an equivalent resistance of 25 ohms (50 ohm load resistor in parallel with 50 ohm input impedance of amplifier).

The amplitude of the intermodal beat frequency fluctuated considerably due to minor temperature variations over a period of 30 minutes and is shown in figure 6.4a.

Despite thermal stabilization of the lasers, the separation of the mirrors drift slowly about a mean separation. The result is that the magnitude of the axial modes will fluctuate depending on their position in the gain curve. The product of these modes, which is the detected intermodal beat frequency, will also fluctuate.

The length of the laser tube or resonant cavity is equivalent to $c/2\pi f$ or 27.3 cm for the beat frequency of 550 MHz. The thermal coefficient of expansion of the glass laser tube is $1x10^{-6}K^{-1}$ which, for a tube length of 27.3 cm, is a variation of 273 nm/^{o}C. This represents a change of 0.43 /^{o}C or a change in laser frequency of 475 MHz/^{o}C.

The optical heterodyning of two He-Ne lasers produced a response at the difference frequency between the modes of the lasers. The two laser sources are randomly polarized but become partially polarized at the beam

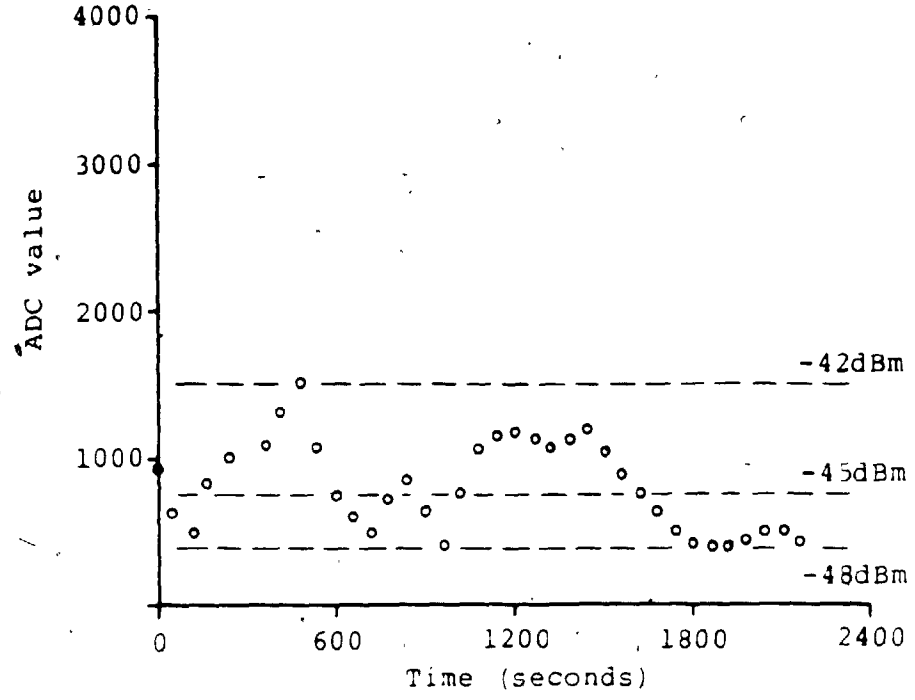


Figure 6.4a Response of the intermodal beat frequency.

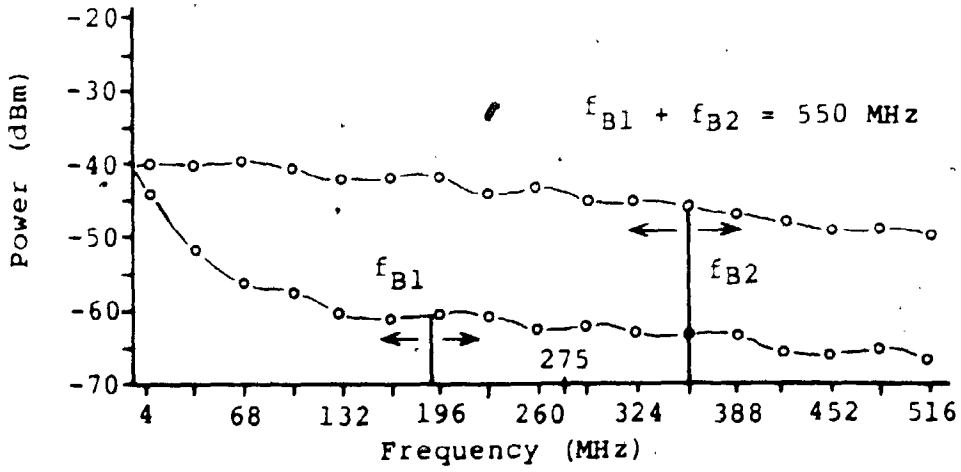


Figure 6.4b Heterodyne beat frequencies.

splitter. The LO laser becomes partially horizontally polarized with respect to the plane of incidence and the signal laser becomes partially vertically polarized to the same plane of incidence. Only the parallel components of polarization contribute to optical mixing and produce an RF difference frequency at the photodiode.

The spectral response displayed only a single large beat frequency (f_{B1}) most of the time. A smaller second beat frequency (f_{B2}) appeared as the main beat frequency drifted above 244 MHz. The second beat frequency is equivalent to 550 MHz - f_{B1}. The sum of the two beat frequencies equal the axial mode separation frequency of 550 MHz (see figure 6.4b).

The maximum signal power of the main beat frequency was 1.78×10^{-13} W (-97.5 dBm) which corresponds to 0.119 μA sourced by the photodiode. The signal power of the second beat frequency was much smaller (>6 dB) than the main beat frequency.

The beat frequencies would stablize in amplitude and frequency after the two lasers had been operating for a couple of hours and had thermally stabilized. There was no fluctuation in the amplitude of the beat frequency that corresponded to that of the intermodal beat frequency shown in figure 6.4a. Rapid fluctuations would be averaged by the analog integrator (6 s). However, the beat frequency would drift slowly and randomly in frequency with time (0.1 MHz/s) due to minor variations in

temperature.

The relatively large single beat frequency with a small secondary beat frequency implies that the lasers are running with at least two modes. The relative size implies that a single mode is favoured and that modes higher than two are probably not present. The linewidth or gain curve of a He-Ne laser is doppler broadened and is typically 1500 MHz (Siegman, 1971). Depending on where the threshold for laser action passes through the gain curve, two axial modes could fit in the gain curve. The above heterodyne results agree with this.

The foregoing heterodyne experiments demonstrated the application of the MCSA in the coherent detection of weak RF signals resulting from the heterodyning of optical signals.

Chapter 7

Discussion of the Multichannel Spectrum Analyzer

7.1 Discussion of System Concepts

A radio frequency multichannel system incoporating the techniques of lock-in detection for the aquisition and coherent processing of optical signals has been designed and built. The reception range of 0 - 512 MHz was divided into 64 channels of equal bandwidth (8 MHz) and spread uniformly across the entire reception range. Microcomputer control is an integral part of the system.

The concepts of modularity and symmetry were applied in the development of the MCSA. The system consists of 64 identical receivers, 64 identical synchronous detectors, 16 identical module interfaces, 16 similar synthesized local oscillators, and 64 similar transmission line filters.

There were a number of advantages to the modularity principle. From a technical standpoint, design and implementation of hardware was much less time consuming and tedious. Errors during assembly were fewer because most procedures were duplicates. Design time and development time was required for only a minimum of circuits developed to ensure operation under the full range of conditions. Implementation time was greatly reduced since all circuits had similar characteristics and

problems. Long term reliability of operation and performance was better since circuit failures often had a similar root cause.

The MCSA system is essentially a parallel processing system. It differs markedly from the more conventional swept spectrum instruments in many respects. Each receiver channel of the MCSA is fixed or is stationary in frequency. Consequently, there was no FM noise from the local oscillator, there were no problems associated with the linearity of the receiver mixers, and the design and implementation of RF electronics was not complicated. Reduced complexity lead to an improvement in the reliability of the system. It should be emphasized that failure of one of the multiple channels would not necessarily bring the entire system down. During the development stages of the system a number of receivers had failed, but work could continue until a number of problems had accumulated and it became convenient to remedy all the problems.

The disadvantages to a parallel processing system are cost and labour required in construction. These two points are the main obstacles that impede the progress toward higher degrees of parallelism for the MCSA. These problems can be eliminated by employing a higher degree of integration in the system. Such integration represents the next step in the evolution of parallel analyzers toward the techniques of integrated circuit design.

Using custom integrated circuits to replace most of the MCSA circuitry would make it possible to design a highly parallel system consisting of a thousand or more receiver channels.

An integrated MCSA system has been built at NASA-Ames Research Centre for the SETI project (Search for Extra-Terrestial Intelligence). The device is capable of analyzing 74,000 channels or frequency bands. The device is only a prototype, the intention is to develop a system employing 2^{20} channels. The system uses 4-bit digitization on a reception range of 0 - 10 MHz with digital filtering to produce 128 (2^7) intermediate channels. Each of the intermediate channels is connected to a microprocessor based FFT computer which generates 8192 (2^{13}) channels (Seeger, 1979; Billingham et al, 1978).

Present day integrated circuit technology makes it difficult to mix digital, RF and low frequency signal processing circuits on the same integrated chip. Thus, separate chips might be required for the RF processing, synchronous detection, signal multiplexing, and data acquisition.

For highly parallel systems, the concepts of integration are important also from a reliability standpoint. Since greater functionality can be designed into a highly integrated circuits making them more versatile, the total number of chips employed can be

lower.

Some components, such as RF filters, cannot be readily transferred to an integrated circuit. However, the concept of symmetrical design was successfully applied in the implementation of strip transmission line filters for the receiver channels. Other technologies, such as surface acoustic wave devices (SAW filters) are capable of RF filtering but are presently prohibitively expensive in a highly parallel application (Matthews, 1977) and seem to be confined to limited frequency bands.

Alternately, RF processing could be accomplished by wideband active power splitting without filters. This would be effective only if buffer amplifiers were used that provided sufficient isolation between channels, preventing local oscillator signals from propagating backward down an RF signal line and into another channel receiver.

If a filter is not used before the receiver mixer, the IF band would be the superposition of two RF bands that are the sum difference frequencies of the IF and local oscillator. The frequency spectrum would appear as a double image separated by twice intermediate frequency. Once detected and digitized, the superimposed bands could be separated by software.

In general, the concepts and techniques of lock-in detection were successfully employed at radio frequencies. Lock-in systems are conventionally used at low frequencies

(< 1 MHz) but have been shown to work well at frequencies far above 1 MHz. Although lock-in detection systems have been developed and optimized for low frequency applications, they can be adapted to RF processing, and used for the MCSA, provided that accommodation has been made for the nonideal behaviour of RF components. The microcomputer system could facilitate such application by performing preprocessing on the digitized data in order to compensate for some of the RF deficiencies.

The MCSA provides a bandwidth improvement factor of 94.8 dB over the reception bandwidth of 512 MHz, and this is directly reflected in the output SNR (see equation 2.1). Across all 64 channels, the MCSA has a noise figure of 3.05 $\pm$0.3 dB, a receiver noise temperature of 306 $\pm$40 K, and a minimum detectable signal of -138 dBm.

7.2 Discussion of the RF Subsystems

Throughout the development stage of the RF electronics for the MCSA, problems were encountered with electromagnetic interference, shielding, and grounding. Only after much work was a full appreciation and understanding of the problem reached.

Each field of electronics (RF, audio, and digital) is influenced differently by EMI, and each requires a different approach to their suppression. Effective EMI reduction techniques must be used not only within a particular field of electronics but its influence in the other fields must be also considered. For example; a coaxial cable carrying an RF signal is very effective in containing it within the cable but a nearby low frequency chopper signal can be induced in both the cable shield and centre conductor.

Careful consideration of the problems of EMI during the development of the MCSA produced a system that is relatively free of noise and contamination. None of the 64 channels exhibited spurious responses due to interfering channels, local oscillators, or harmonics. In addition, there were no major problems with external sources of noise such as radio or television signals.

The front-end module of the MCSA contains the RF amplifiers, mixers, filters, and splitters. The module performed all necessary functions satisfactorily. The

module is presently cramped for space and should be expanded by placing the RF amplifiers on a separate module. This would improve shielding, convenience and provide space for modifications and adjustments especially when it is required to switch amplifiers in and out of line. In addition, provision could be made to power the first couple of amplifiers from battery that is shielded and free of contaminating signals.

The low-pass and high-pass filters in the front-end modules all had satisfactory responses. All of the filters were based on the Chebyshev type but produced responses typical of an elliptic (Cauer) filter (The Chebyshev filter is a special case of the elliptic filter). The deviation from the ideal behaviour was the result of nonideal capacitors and inductors behaving like transmission line sections at high frequencies, and the propagation of RF energy between the input and output of the filter when reflections in the filter occur. Despite these problems, it was advantageous to make use them in an optimized response for the passband, transition band, and stopband.

The front-end mixer (SRA-1W) was a source of a number of problems that could be solved to some degree by selecting a more perfect mixer. The design of the MCSA is such that it relies on the linearity of the front-end mixer. The output ports of the mixer have a maximum specified VSWR of 2:1. The uncertainty in the

VSWR greatly affected the wideband response of the filters because they rely on 50 ohm resistive terminations that are independent of frequency.

The residual front-end local oscillator signal that appears on the IF port was suppressed by 30 dB. This is insufficient to prevent detection by adjacent channels. The residual oscillator signal was further suppressed by 30 dB with a helical resonator. The resonator is characterized by a very narrow rejection band. Alternately, the signal may be actively suppressed by feeding forward some of the oscillator and subtracting it from the IF output; the idea being to cancel the residual signal.

Front-end frequency response sweeps of the MCSA, with the output taken from the 4-way power splitter, are plotted in figures 5.6 and 5.7. The plot demonstrates the integrity of the front-end of the system. The large ripple (±6 dB maximum) in the plots can be directly attributed to mismatching between the stages of amplification, filtering, and mixing. Ideally, the passband response should be flat with a sharp transition band, and high relative attenuation in the stopband.

Since in both plots, the frequency separation between peaks of the ripple is much wider than an individual channel bandwidth, the ripple only influences the effective gains of the channels with respect to one another. Compensation for the ripple could be

accomplished by adjusting the IF gain or the postdetection gain in the receiver.

The strip transmission line channel filters were used to divide the RF signal into individual channels. The combination of the filter banks with the front-end improved the overall frequency response of the front-end by producing a maximum passband ripple of ± 4.5 dB (see figures 5.16 and 5.17). In general, mismatching between stages tends to degrade the response. However, in this case, the relative ripple in the peak responses of the channel filters with respect to other channels had a compensating effect on the ripple of the system frequency sweeps.

The local oscillator and frequency synthesizer are sensitive components of the MCSA since noise in the local oscillator (AM and FM) would be detected by the receiver's square-law detector. Most of the noise is asynchronous with the chopper and cancelled by synchronous detection. However, noise that is synchronous with the chopper control signal would be a very serious problem if it contaminated the local oscillator. The synchronous detector being unable to differentiate between the noise and the RF signal, would produce an inaccurate output. Noise reduction techniques were applied throughout the design of the local oscillators to minimize the possibility of contamination. Noise from the oscillators was not detectable by the MCSA.

The local oscillator signals for the receivers were synthesized by phase-locking at a low frequency and then frequency multiplied up to the required oscillator frequency. Alternately, the required frequency could be synthesized directly without multiplication. The latter method, although more difficult, is the preferred approach since it eliminates noise due to harmonics and sub-harmonics (Manassewitsch, 1976). Output level control of the oscillator was not used in the MCSA but should be considered if thermal gain compensation is adopted for the square-law detectors.

7.3 Discussion of the Detection Subsystem

The detection subsystem of the MCSA is the most sensitive part of the system. It consists of two sections: square-law detection in the receiver for detection of the RF signal, and synchronous detection for coherent demodulation of the chopper modulated RF and reference signal.

The RF receiver was designed on the basic heterodyne principle with a square-law detector that was compensated for thermal offset drift. Offset compensation was accomplished by a thermal reference diode that was matched to the signal detector diode (see figure 5.27b). Control of thermal gain drift was not employed since compensation for gain drift can be handled by software and calibration sweeps of the system.

An improvement on the channel receiver would be to employ thermally stabilized square-law detectors. A simple method would be to heat the diodes with a resistor. Temperature could be controlled by controlling the resistor's current. Temperature could be sensed by measuring the voltage across the thermal reference diode.

In highly parallel systems, it would become increasingly difficult to adjust each receiver for offset, IF gain, IF bandwidth, postdetection gain, and postdetection integration. At the risk of making the receiver more complicated, these adjustments could be

performed electronically under software control. This would permit rapid, periodic updating of the system for optimum performance.

The synchronous detector met the requirements with very little problem associated with synchronous noise. A few improvements in the synchronous detection circuitry would be directed toward higher quality devices and components rather than circuit modification. The two sample-and-holds were implemented with BIFET operational amplifiers and could be replaced with a single device (LF398). It would be convenient to have the difference signal (RF minus reference signal) available along with the other signals. Electronic control of the long-time integrator would also be convenient.

7.4 Discussion of the Data Acquisition System and Microcomputer System

The data acquisition system input is connected to the output on each of the receiver modules. The interface controls access to the synchronous detector's analog outputs and provides the control signals for proper operation. The selected analog signal is placed on the ribbon cable bus which connects all receiver modules and leads to the ADC board for digitization.

The analog signal when placed on the bus is driven by a voltage follower but is still susceptible to noise on route to the ADC. The analog signal could be encoded for better noise immunity by the use of pulse width modulation (PWM). The amplitude of the signal would be encoded as the width of a pulse of a carrier frequency. The noise improvement of PWM is the result of increasing the transmission bandwidth by encoding and then reducing the bandwidth, along with the noise, on decoding. The ADC would have to perform conversions at a slower rate to provide adequate time for the decoding to take place. The decoding could be done by an integrator that would filter out the carrier and its harmonics.

The data acquisition system was designed with a 12-bit ADC which has a dynamic range of 4096:1 (36.1 dB). A 16-bt ADC would perform conversions at a much slower rate but would have a dynamic range of 65536:1 (48.2 dB).

A larger dynamic range could be obtained by preceeding the ADC with a logarithmic amplifier.

The microcomputer system was used as an intelligent control system for the MCSA. Virtually all the functions of the MCSA are under software control. The microcomputer performs the control functions quickly and in addition is capable of some preprocessing to obtain extended integration times and graphic displays. The intention was to perform further data analysis and storage on a larger computer (PDP-11/23) where more elaborate software packages are available.

Presently, powerful personal computers (IBM) are available that can largely replace the microcomputer system. All commands to the MCSA pass through two parallel ports which can be readily adapted to a different microcomputer system. However, in keeping with the original concept of an intelligent controller, the present microcomputer performs the tasks of data acquisition, collation, system calibration, and graphical display quite adequately.

The FORTH operating system currently running the MCSA proved to be an adequate software tool. Development of both hardware and software proceeded rapidly together. FORTH would be an excellent choice as a controlling operating system if the microcomputer system is updated.

Chapter 8

Conclusions

8.1 Conclusions

A multichannel lock-in detection system has been developed for the coherent processing of optical signals. The multichannel spectrum analyzer (MCSA) has an important role in an optical heterodyne spectrometer as it spectrally resolves the resulting intermediate frequency (IF) band containing the signals of interest.

The novel design of the MCSA incorporates the principles of lock-in detection and superheterodyne reception in each of its 64 receivers, to extract weak radio frequency (RF) signals from noise.

A common system organization consists of scientific instrumentation connected to an external computer with user control required for both machines. The analyzer improves on this by fully integrating the two. All access and control of the MCSA occurs through the user programmable microcomputer. The microcomputer performs the tasks of data manipulation, some data processing, extended integration times, and graphic display of spectral responses.

The FORTH operating system was used throughout the development of the MCSA. It proved to be invaluable as a software tool in both the hardware and software

development stages of the MCSA.

The concepts of modularity and symmetry, common in other engineering designs, were successfully translated and applied in the development of the MCSA. Modularity was particularly beneficial during the development stages by reducing significantly the time required for many modifications. Circuit symmetry greatly alleviated start-up difficulties, since problems were similar in all the circuits.

The concepts of parallel processing, which are well developed in computer designs, were successfully employed in the RF processing electronics and detection electronics. Despite cost and construction labour, the system has proved to be reliable with only minor failures.

The ideas of lock-in detection, which are often used at audio frequencies, coupled with superheterodyne reception, were successfully applied in a novel receiver design. The technique of lock-in detection greatly reduced the systems sensitivity to noise. Particularily troublesome were external noise transmissions from CB radio, FM radio, and TV stations. The technique of superheterodyne detection greatly improved the sensitivity of the system by incorporating IF band (64 MHz) amplification, IF filtering, square-law detection and low frequency amplification.

The MCSA was developed for maximum sensitivity. Consequently, it is very sensitive to noise and

contamination coming from both internal and external sources. It was found that the problems of electromagnetic interference (EMI) required just as much attention as did the development of the MCSA's subsystems.

The noise performance of the MCSA is largely determined by the first few front-end amplifiers of the front-end module. The noise performance can be improved by placing the front-end amplifiers in a separate module with provision for battery power supply.

Noise generated as a result of distortion was much more difficult to eliminate. Harmonics from the frequency multipliers of the local oscillator were particularly troublesome. The techniques of phase-locked frequency synthesis applied to RF frequencies would significantly reduce the distortion but at the expense of increased circuit complexity.

The strip transmission line filters in the filter banks proved to be effective in dividing and bandpass filtering the RF signal into individual channels. Taking advantage of the distributed parameter behaviour of components resulted in reliable, trouble-free operation despite the high radio frequencies involved.

The most sensitive part of the MCSA is the channel receiver. The novel design was based on the principles of superheterodyne reception with improved square-law detection by employing dual detectors to compensate for thermal offset drift. Compensation for the thermal gain

drift was accomplished through software rather than hardware. A further improvement receiver would be the design of compensation circuitry for thermal gain drift.

The data acquisition system with its 12-bit ADC proved to be satisfactory. The high speed ADC scans the entire system quickly with very little CPU idle time. Dynamic range improvement could be achieved by preceding the ADC with a logarithmic amplifier.

The multichannel spectrum analyzer was successfully used in an optical heterodyne experiment. The experiment consisted of two parts: homodyne detection for the spectral reception of the intermodal beat frequencies of a He-Ne laser, and heterodyne detection for spectrally resolving the RF signals arising from the interference of two optical lasers.

The MCSA combines the power of RF parallel processing (64 x 8 MHz channels) over a wide reception bandwidth of (512 MHz), with the noise reducing techniques of lock-in detection and superheterodyne detection, to produce a system capable of supporting some of the most sensitive experiments now being performed in optical heterodyne spectroscopy. In addition, the generality and versatility of the system is orchestrated by the microcomputer and its software.

The MCSA has a bandwidth improvement factor, which is directly reflected in the output SNR, of 94.8 dB over the reception range of 512 MHz. The noise figure of the

analyzer is 3.05 $\pm$ 0.3 dB with the receiver's noise temperatures 306 $\pm$ 40 K. The minimum detectable signal power is -138 dBm.

Appendix A

A.1 Phase-Locked Loop Calculations

The following calculations derive the loop filter components neccessary for frequency synthesis of the 16 local oscillators. The calculations are based on equations 3.15 - 3.17c and diagram 4.12b.

Intial conditions:

V_{DD} = 5 V,

f_r = 250 KHz, main reference frequency

f_L = 20 MHz, low VCO frequency

f_H = 30 MHz, high VCO frequency

V_v = 5 V, varactor voltage range

n = 100, counter preset value

$\Delta w_L = 2\pi f_r/10$, lock range

Derivation of t_1, t_2:

$K_d = V_{dd}/\pi = 1.59$ V/rad

$K_o = 2\pi(f_H - f_L)/(nV_v) = 1.26 \times 10^5$ rad/s.V

$\Delta w_L = 2\zeta w_n = 2\pi f_r/10 = 1.57 \times 10^3$ rad

let $\zeta = 1.0$

$\therefore w_n = \Delta w_L/2\zeta = 7.85 \times 10^4$ rad/s

rearranging equations 3.17b and 3.17c we get:

$t_2 = \zeta/2w_n - 1/K_oK_d = 1.37 \times 10^{-6}$ s

$t_1 = K_oK_d/w_n^2 = 3.25 \times 10^{-5}$ s

$\therefore R_1C = t_1 - t_2 = 3.11 \times 10^{-5}$ s

let $R_1 = 6.8\ K\Omega$

$\therefore C = 4.6 \times 10^{-9}\ F$

$\therefore R_2 = t_2/C = 300\Omega$

Appendix B

B.1 Y-Parameter Amplifier Analysis

Only a pertinent part of the analysis is presented here (Hejhall, 1978).

An important factor in the design of a transistor amplifier is its potential stability. This can be determined from the Linvill stability factor (C):

$$C = \frac{|Y_{12}Y_{21}|}{2g_{11}g_{22}-Re(Y_{12}Y_{21})} \qquad B.1$$

When C is greater than unity, the transistor is potentially unstable. When C is less than unity, the transistor is unconditionally stable.

If the transistor proves to be potentially unstable, the analysis must proceed using the Stern stability factor K. The design procedure for this case is lengthy and is well presented in the work by Hejhall (1978).

The analysis of a transistor that proves to be unconditionally stable is much simpler than the unstable case. The transistor amplifiers used in the MCSA were found to be stable and the design precedure for them is presented here.

Transducer gain, G_T, is defined as the output power delivered to a load by the transistor, divided by the maximum input power available from the source:

$$G_T = \frac{4Re(Y_S)Re(Y_L)|Y_{21}|^2}{|(Y_{11}+Y_S)(Y_{22}+Y_L)-Y_{12}Y_{21}|^2} \qquad B.2$$

The source and load admittances, Y_S and Y_L, required to achieve the maximum transducer gain for an unconditionally stable transistor may be calculated from:

$$G_S = \frac{1}{2Re(Y_{22})} R_y^2 - |Y_{12}Y_{21}|^2 \qquad B.3a$$

$$B_S = -Im(Y_{11}) + \frac{Im(Y_{12}Y_{21})}{Re(Y_{22})} \qquad B.3b$$

$$G_L = \frac{1}{2Re(Y_{22})} R_y^2 - |Y_{12}Y_{21}|^2 \qquad B.3c$$

$$B_L = -Im(Y_{22}) + \frac{Im(Y_{12}Y_{21})}{Re(Y_{11})} \qquad B.3d$$

where $R_y = 2Re(Y_{11})Re(Y_{22}) - Re(Y_{12}Y_{21})$

The foregoing design equations were used in the analysis of 2N3866 radio frequency transistor. The small signal parameters for this device are available in the Motorola Transistor Data Manual (Motorola, 1978). Table B-1 shows these Y-parameters for various frequencies and the corresponding calculated results.

Table B.1 RF transistor (2N3866) characteristics

I_C = 80 mA

Y-Par.	Frequency (MHz)			
	50	100	200	400
Y_{11}	30+j12	35+j12	50+j5	55-j15
Y_{12}	-0.1-j0.5	-0.1-j1.2	-0.4-j2.6	-1.7-j4.5
Y_{21}	360-j620	70-j360	-40-j200	-75-j70
Y_{22}	0.8+j3.0	1.0+j4.7	2.1+j9.2	5.5+j17
C	0.93	0.87	0.75	0.62
Y_{Sopt}	91.8-j85.8	127-j36	112+j39	56+j56
Y_{Lopt}	2.45-j4.97	3.6-j5.4	4.7-j7.4	5.6-j13
G_T	950	176	35	7.45

Appendix C

C.1 Device Specifications

Amplifier - AMM502B

description: RF, wideband, low-noise

manufacturer: Avantek Inc.

model: AMM502B

range: 5 - 500 MHz

gain: 27 $\pm$1 dB

noise figure: 2.7 dB maximum

VSWR: 2:1 input max., 2:1 output max.

compression: 1 dB at 20 dBm minimum

Amplifier - W1GA

description: RF, wideband, low-noise

manufacturer: Tron-Tek Inc.

model: W1GA

range: 5 - 1000 MHz

gain: 20 $\pm$0.5 dB

noise figure: 1.8 dB maximum

VSWR: 2:1 input max., 2:1 output max.

compression: 1 dB at -3 dBm

Power splitter - PSC2-1W

description: RF, wideband

manufacturer: Mini-Circuits Laboratory

model: PSC2-1W

range: 1 - 650 MHz

impedance: 50 Ω, all ports

isolation: 25 dB typical

insertion loss: 0.7 dB typical

VSWR: 1.2:1 maximum

Mixer - SRA-1W

description: double-balanced, wideband

manufacturer: Mini-Circuits

model: SRA-1W

range: 1 - 500 MHz

impedance: 50 Ω

isolation: LO-RF: 45 dB, LO-IF: 40 dB

conversion loss: 6.5 dB

VSWR: LO: 3:1, IF: 1.5:1, RF: 1.5:1

Mixer - SBL-1

description: double-balanced, wideband

manufacturer: Mini-Circuits

model: SBL-1

range: 1 - 500 MHz

impedance: 50 Ω

isolation: LO-RF: 45 dB, LO-IF: 40 dB

conversion loss: 6.5 dB

VSWR: LO: 3:1, IF: 1.5:1, RF: 1.5:1

Amplifier - MWA110

description: RF, wideband, hybrid module

manufacturer: Motorola

part number: MWA110

range: 1 - 700 MHz

gain: 14 ±1 dB

noise figure: 4.0 dB

VSWR: 2:1 for less than 550 MHz

compression: 1 dB at -3 dBm

Amplifier - MWA220

description: RF, wideband, hybrid module

manufacturer: Motorola

part number: MWA220

range: 1 - 800 MHz

gain: 10 ±1 dB

noise figure: 6.5 dB

VSWR: 1.7:1 for less than 700 MHz

compression: 1 dB at +12 dBm

Appendix D

D.1 Helical Resonator Design and Approximation

An excellent discussion of helical resonators can be found in the paper by MacAlpine (1959) and in the 'Radio Amateur's Handbook' (DeMaw, 1980).

The general structure of the helical resonator is shown in figure D.1. The design equations presented have been modified to account for metric units of measure.

A helical resonator was employed on the output of the front-end mixer to reject any feed-through of the local oscillator by an additional 30 dB. Using the design equations of figure D.1, the follow results were obtained:

given: $Z_o = 500\Omega$, $f_o = 512$ MHz

then; $D = 9.82$ mm

$d = 5.40$ mm

$B = 13.02$ mm

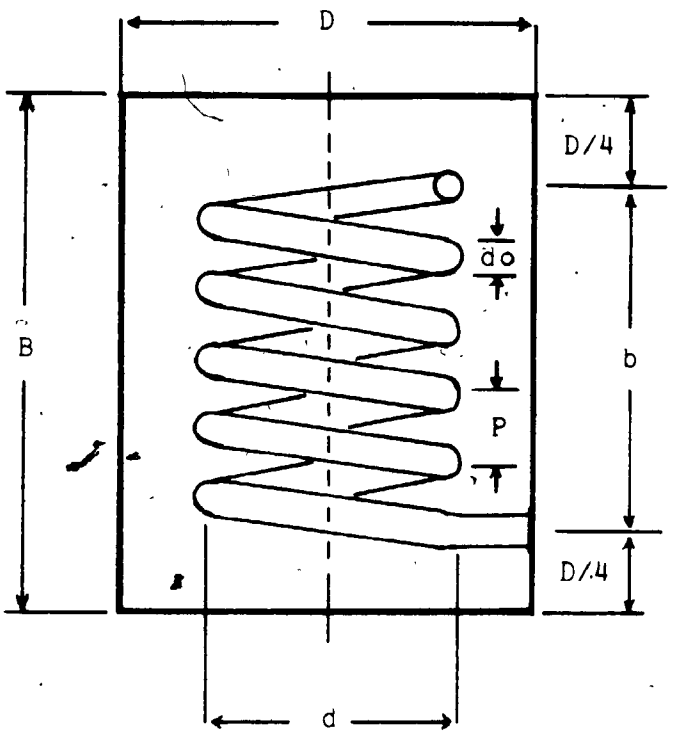
$b = 8.10$ mm

$N = 9.64$ turns

$P = 0.842$ mm/turn

$d_o = P/2 = 0.421$ mm

The helical resonator may be approximated by an open circuit transmission line. The equivalent circuit and appproximation equations are shown in figure D.2.



if shield is square, then D = 1.2 x width.
best results with:

$$d = 0.55\ D, \qquad b = 0.825\ D$$

$$0.4 < do < 0.6\ P, \qquad B = 1.325\ D$$

if D [m] and fo [MHz] then:

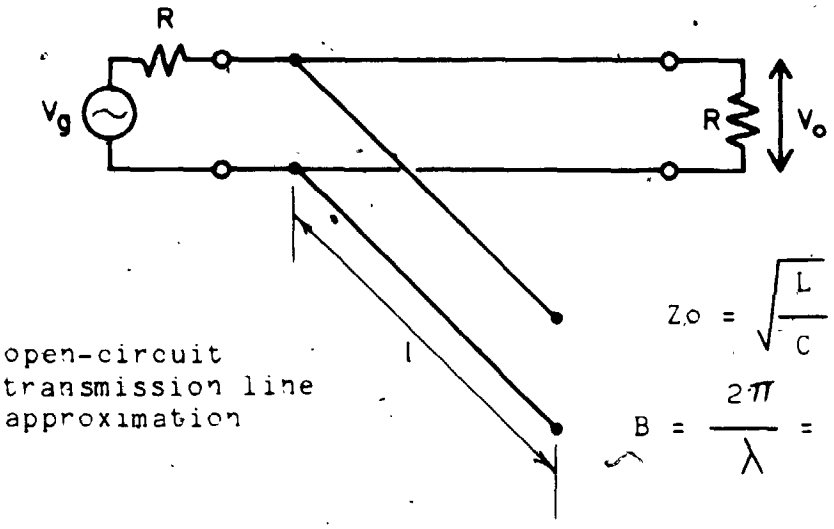
$$Qn = 1.968\ D\ fo^{*},$$

$$N = 48.5 / (fo\ D)$$

$$Zo = 2515 / (fo\ D),$$

$$P = 17.03\ fo\ D \quad [mm/turn]$$

Figure D.1 Helical resonator structure and design.



for a transmission line:

$$Zin = Zo\left(\frac{Zl\ \mathrm{Cos}(Bl) + j\ Zo\ \mathrm{Sin}(Bl)}{Zo\ \mathrm{Cos}(Bl) + j\ Zo\ \mathrm{Sin}(Bl)}\right)$$

$\therefore$ for an open circuit transmission line:

$$Zin = -j\ Zo\ \mathrm{Cot}(Bl)$$

$\therefore$ the response of the above circuit is:

$$G = -10\ \log\left[1 + \left(\frac{R}{2Zo}\right)^2 . \mathrm{Tan}^2(Bl)\right]$$

Refer to figure 4.3b for theoretical and experimental responses.

Figure D.2 Equivalent circuit and approximation for a helical resonator.

Appendix E

E.1 Microcomputer Schematics

The following figures are a complete, detailed set of schematics for the microcomputer system used with the multichannel spectrum analyzer.

Table E.1 Pin designations of the STD bus

Component side

Pin	Mnemonic	Flow +in,-out	Description
1	+5V	+	+5Vdc
3	GND	+	ground
5	-5V	+	-5Vdc
7	D3	+/-	data bus
9	D2	+/-	data bus
11	D1	+/-	data bus
13	D0	+/-	data bus
15	A7	-	address bus
17	A6	-	address bus
19	A5	-	address bus
21	A4	-	address bus
23	A3	-	address bus
25	A2	-	address bus
27	A1	-	address bus
29	A0	-	address bus
31	-WR	-	write to memory or I/O
33	-IORQ	-	I/O address select
35	-IOEXP	+/-	I/O expansion
37	-REFRESH	-	refresh timing
39	-STATUS1	-	CPU status
41	-BUSAK	-	bus acknowledge
43	-INTAK	-	interrupt ack.
45	-WAITRQ	+	wait request
47	-SYSRST	-	system reset
49	-CLOCK	-	clock from CPU
51	PCO	-	priority chain out
53	AUX GND	+	aux. ground
55	AUX +V	+	aux. postive

Table E.1 continued

Circuit side

Pin	Mnemonic	Flow +in,-out	Description
2	+5V	+	+5Vdc
4	GND	+	ground
6	-5V	+	-5Vdc
8	D7	+/-	data bus
10	D6	+/-	data bus
12	D5	+/-	data bus
14	D4	+/-	data bus
16	A15	-	address bus
18	A14	-	address bus
20	A13	-	address bus
22	A12	-	address bus
24	A11	-	address bus
26	A10	-	address bus
28	A9	-	address bus
30	A8	-	address bus
32	-RD	-	read to memory or I/O
34	-MEMRQ	-	memory address select
36	-MEMEX	-	memory expansion
38	-MCSYNC	-	machine cycle sync
40	-STATUS0	-	CPU status
42	-BUSRQ	+	bus request
44	-INTRQ	+	interrupt req.
46	-NMIRQ	+	non-maskable int
48	-PBRST	+	push button reset
50	-CNTRL	+	aux. timing
52	PCI	+	priority chain in
54	AUX GND	+	aux. ground
56	AUX -V	+	aux. negative

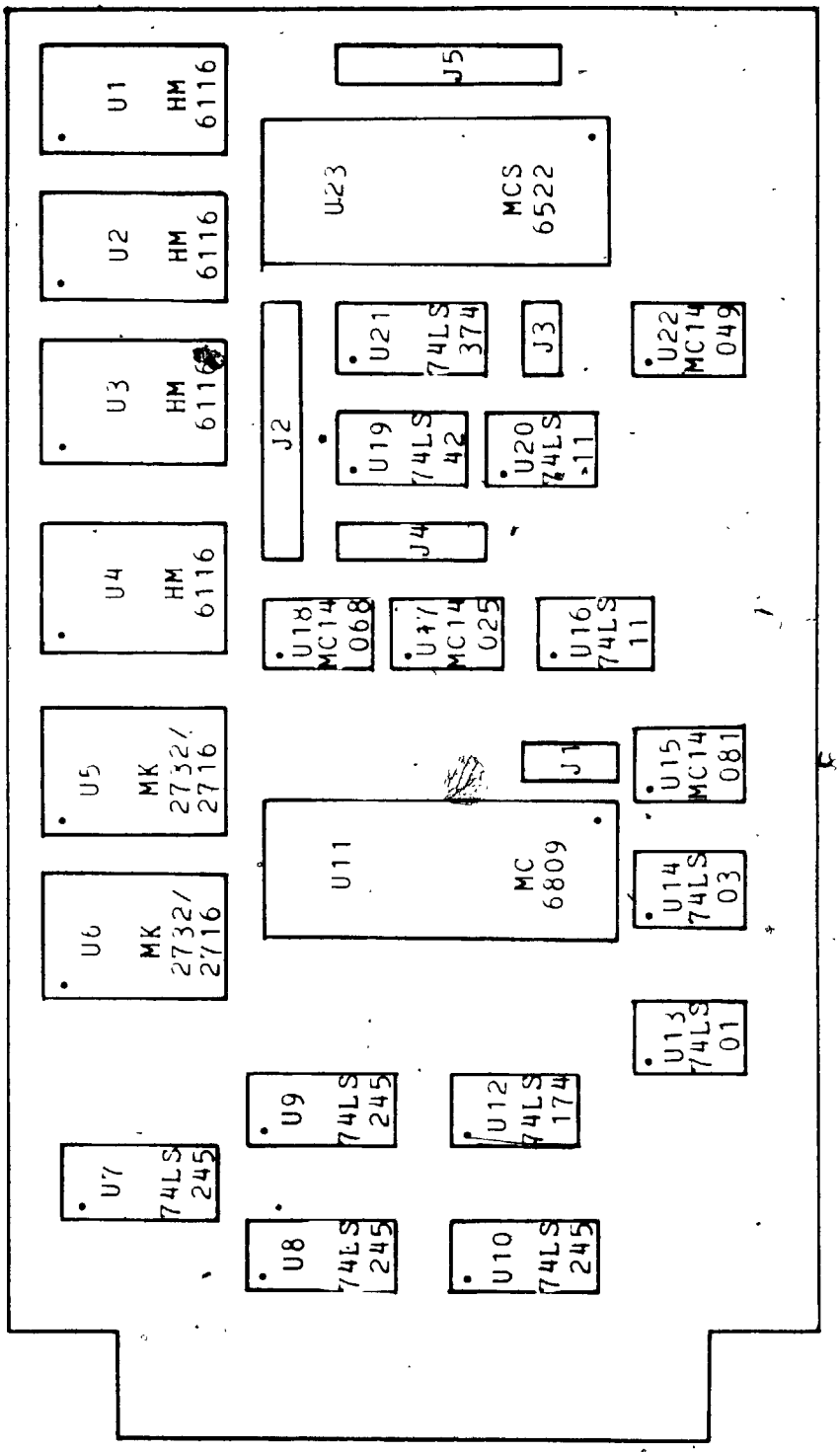


Figure E.1a CPU board layout.

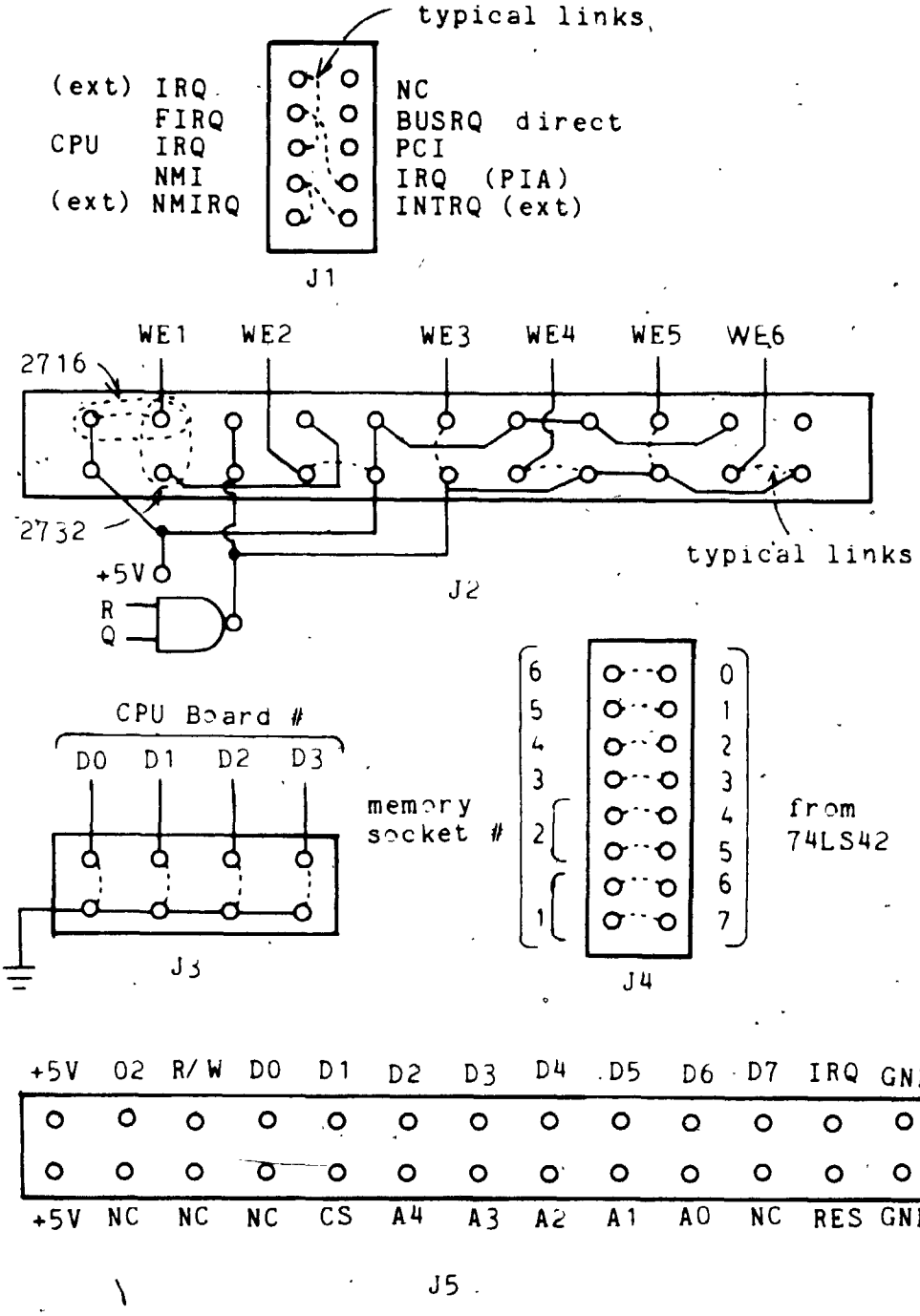


Figure E.1b CPU board layout.

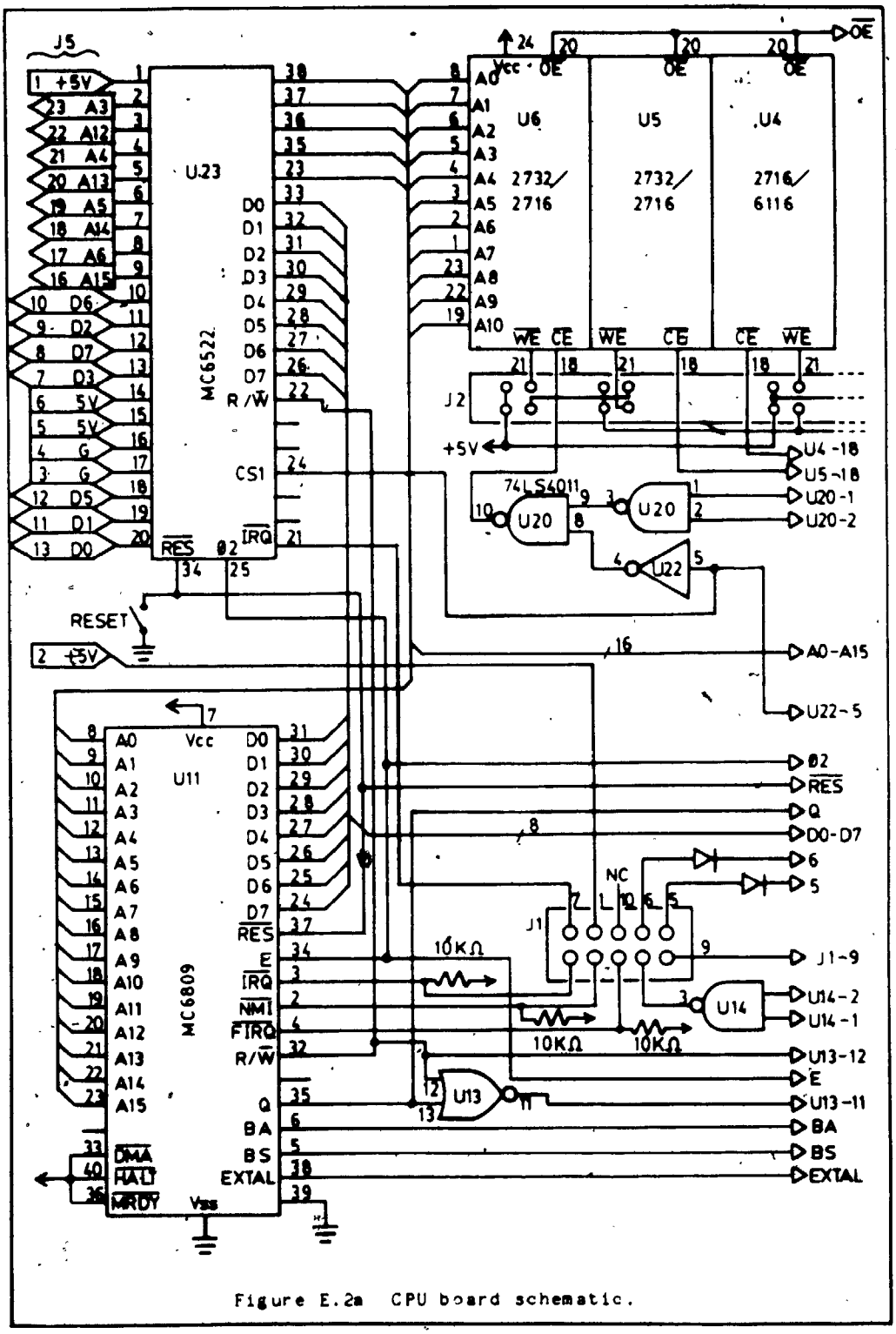


Figure E.2a CPU board schematic.

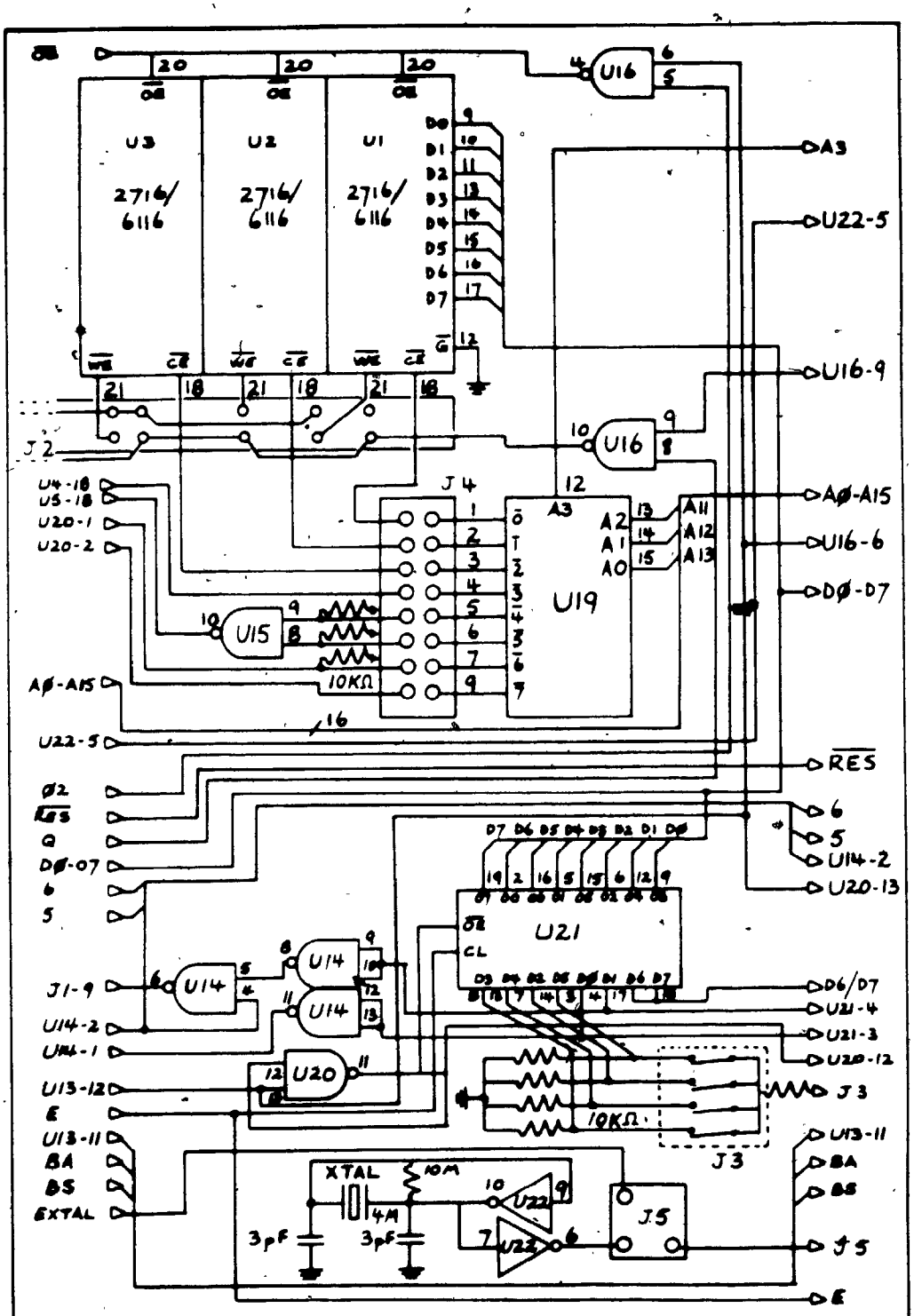


Figure E.2b CPU board schematic.

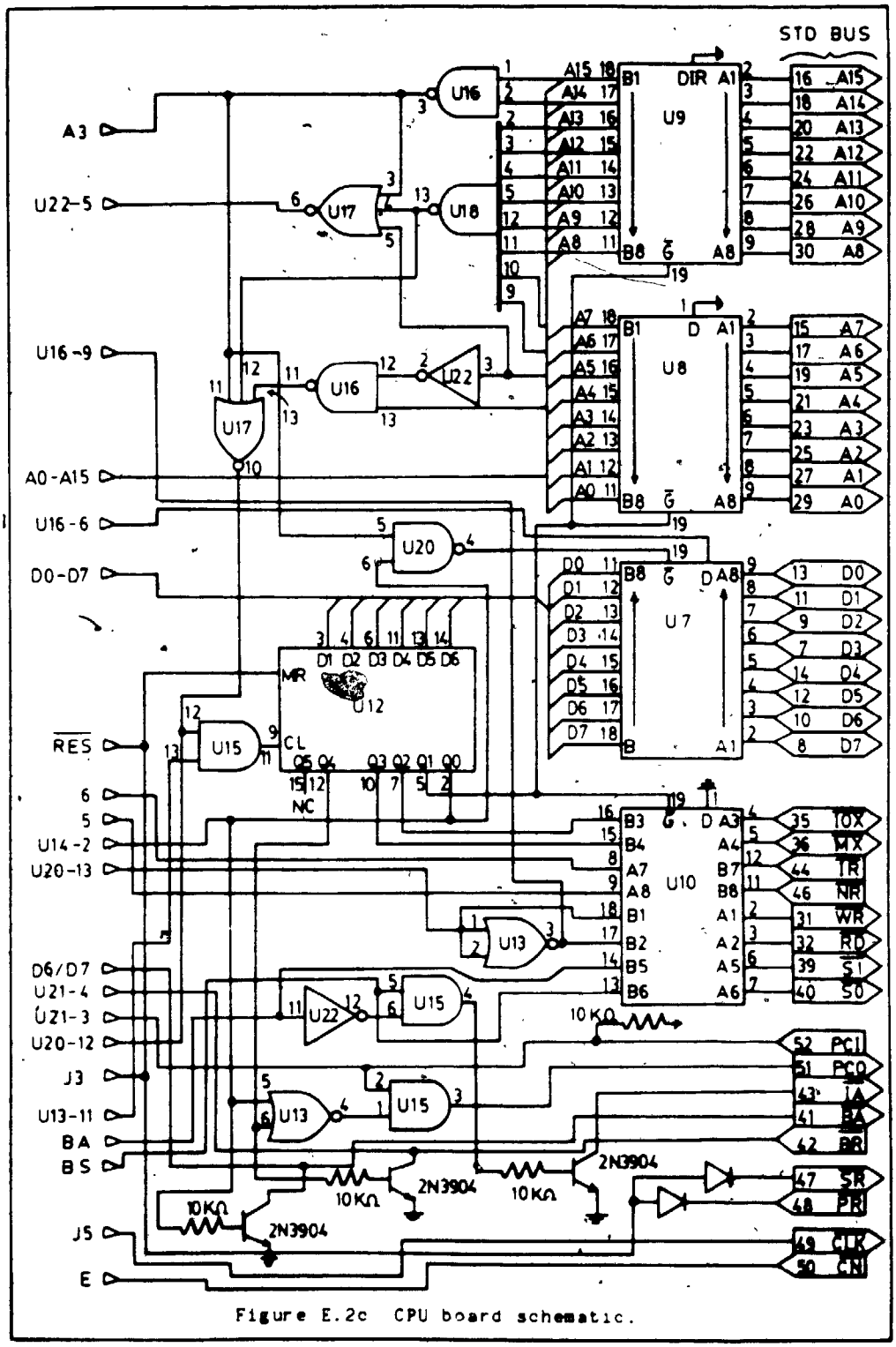
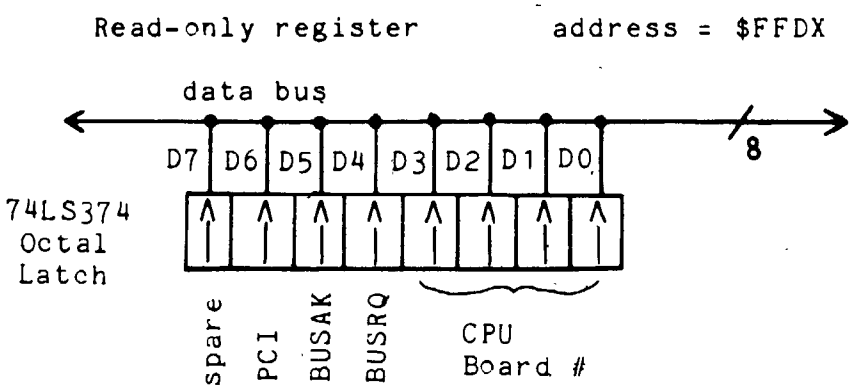
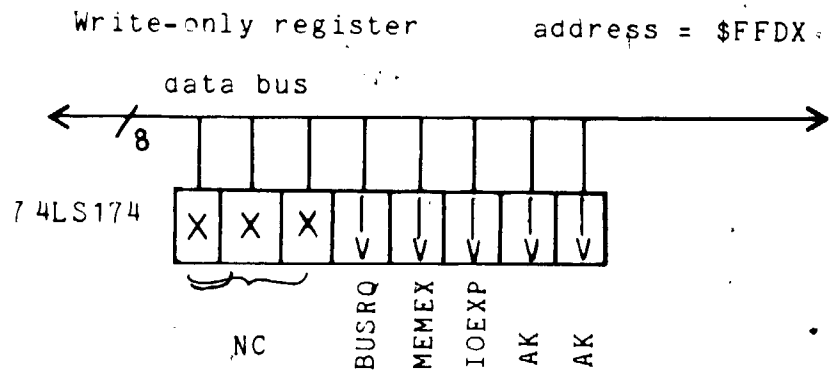
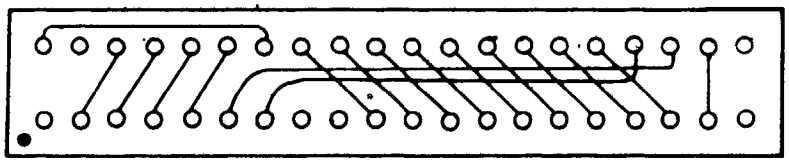


Figure E.2c CPU board schematic.







VIA (SY6522) socket jumpered for IO board

Figure E.3 CPU board bus flags and VIA jumpers.

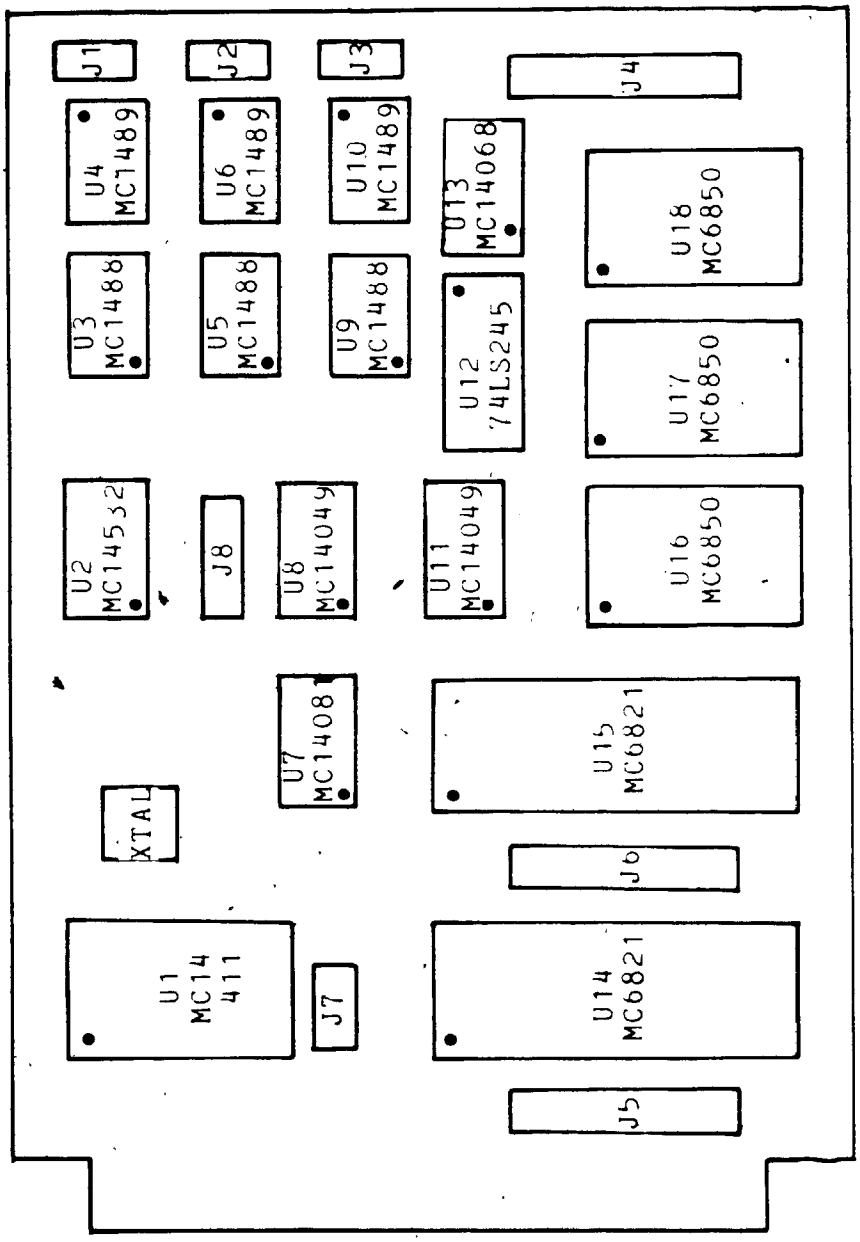
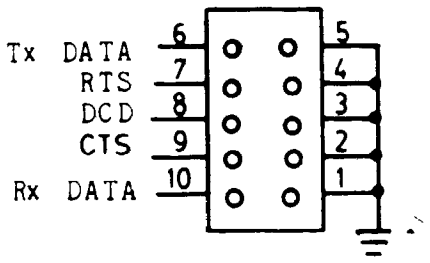
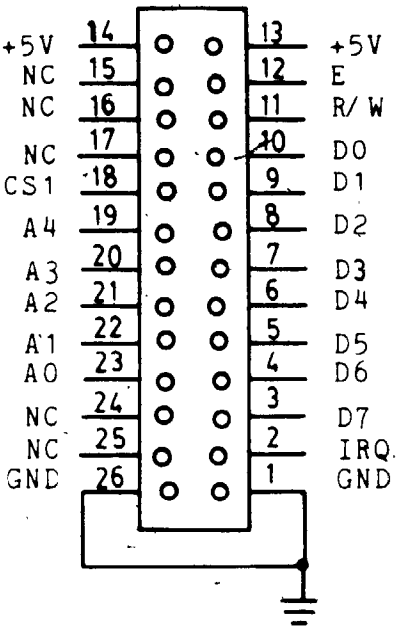


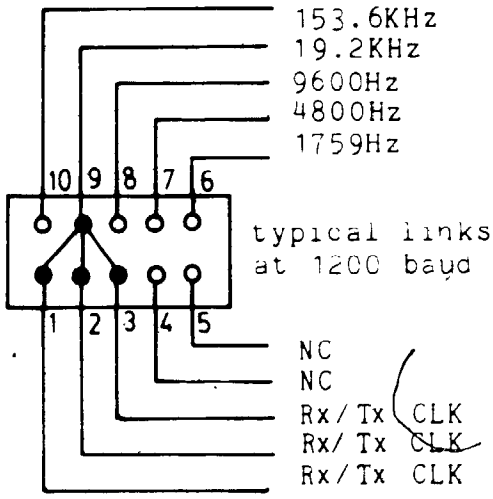
Figure E.4: I/O board layout.



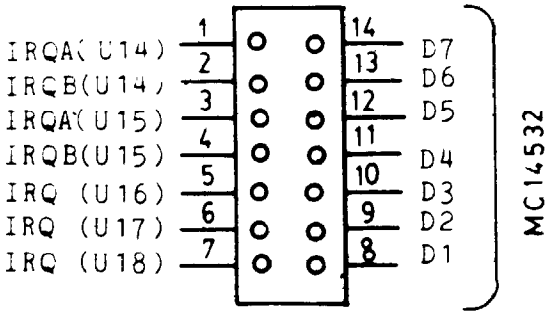
J1/J2/J3 pinout



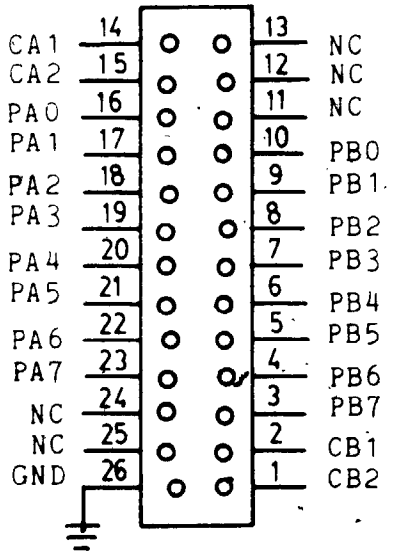
J4 pinout



J7 pinout



J8 pinout



J5/J6 pinout

Figure E.4b I/O board layout.

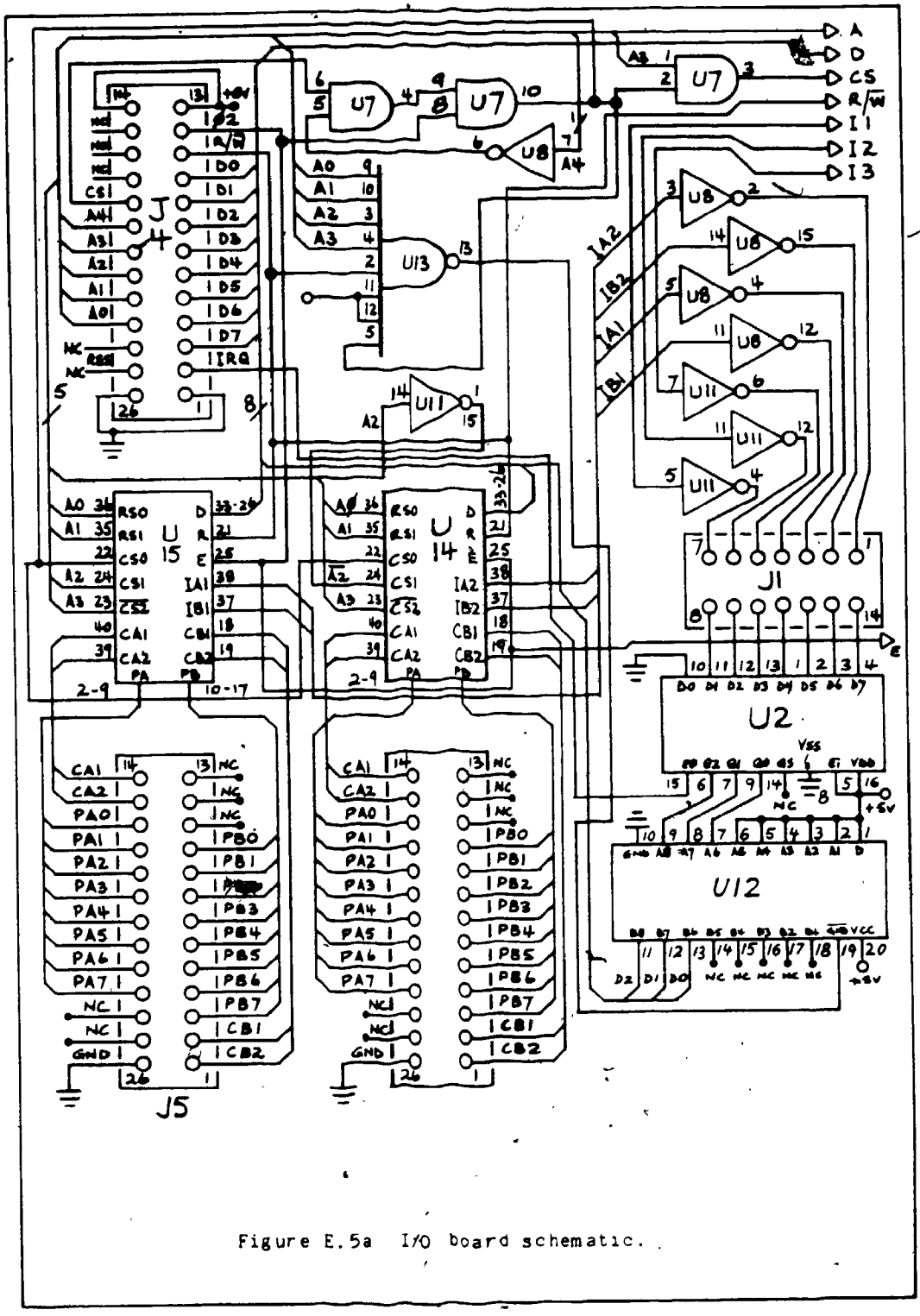


Figure E.5a I/O board schematic.

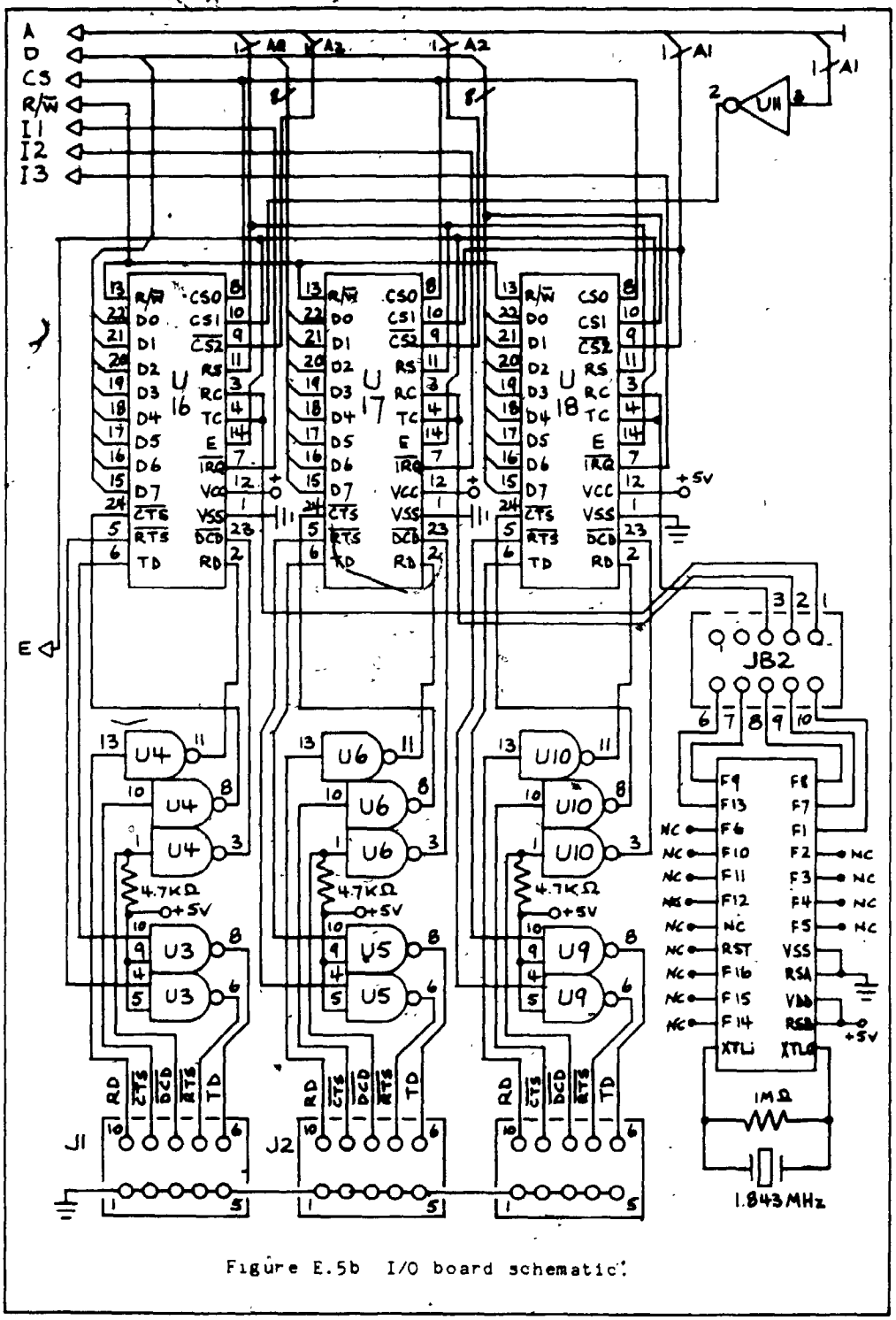
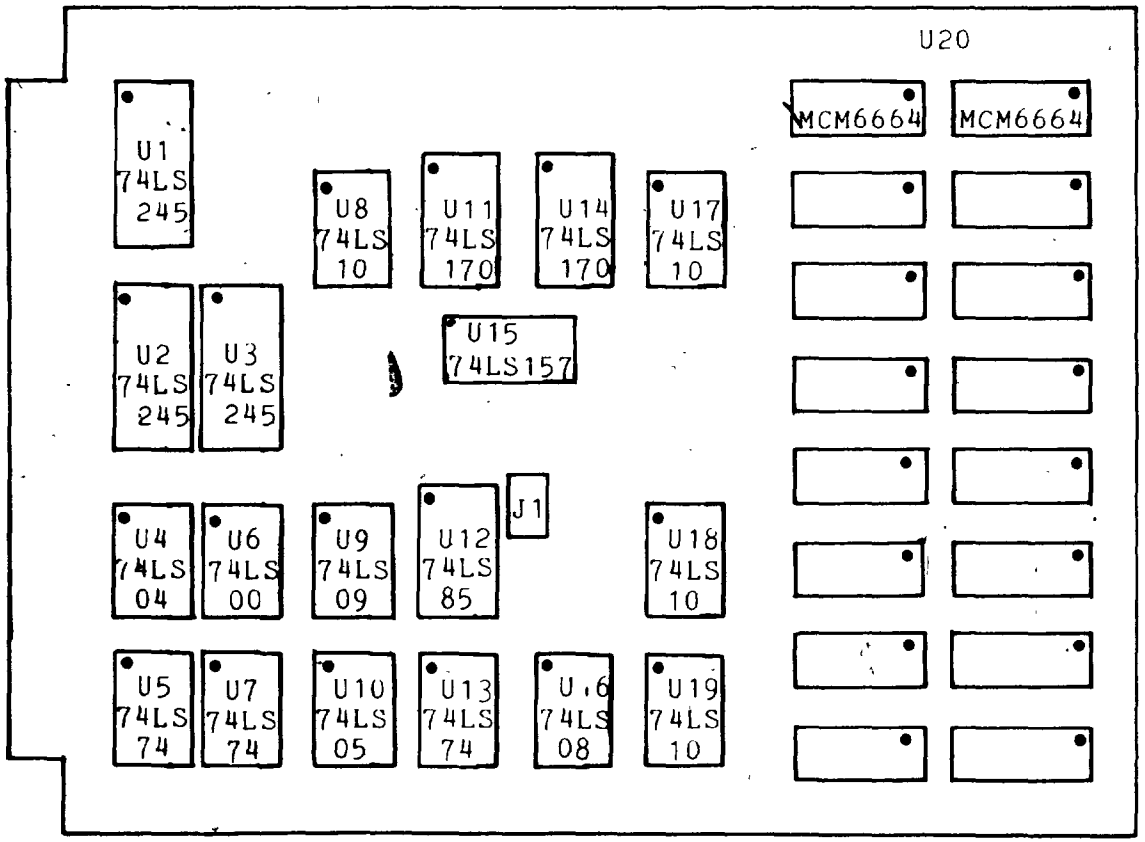
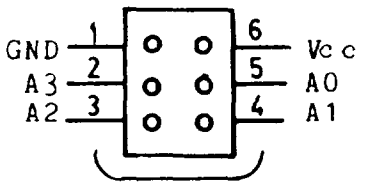


Figure E.5b I/O board schematic





all from U12

J1 pinout (board name).

Figure E.6 RAM board layout.

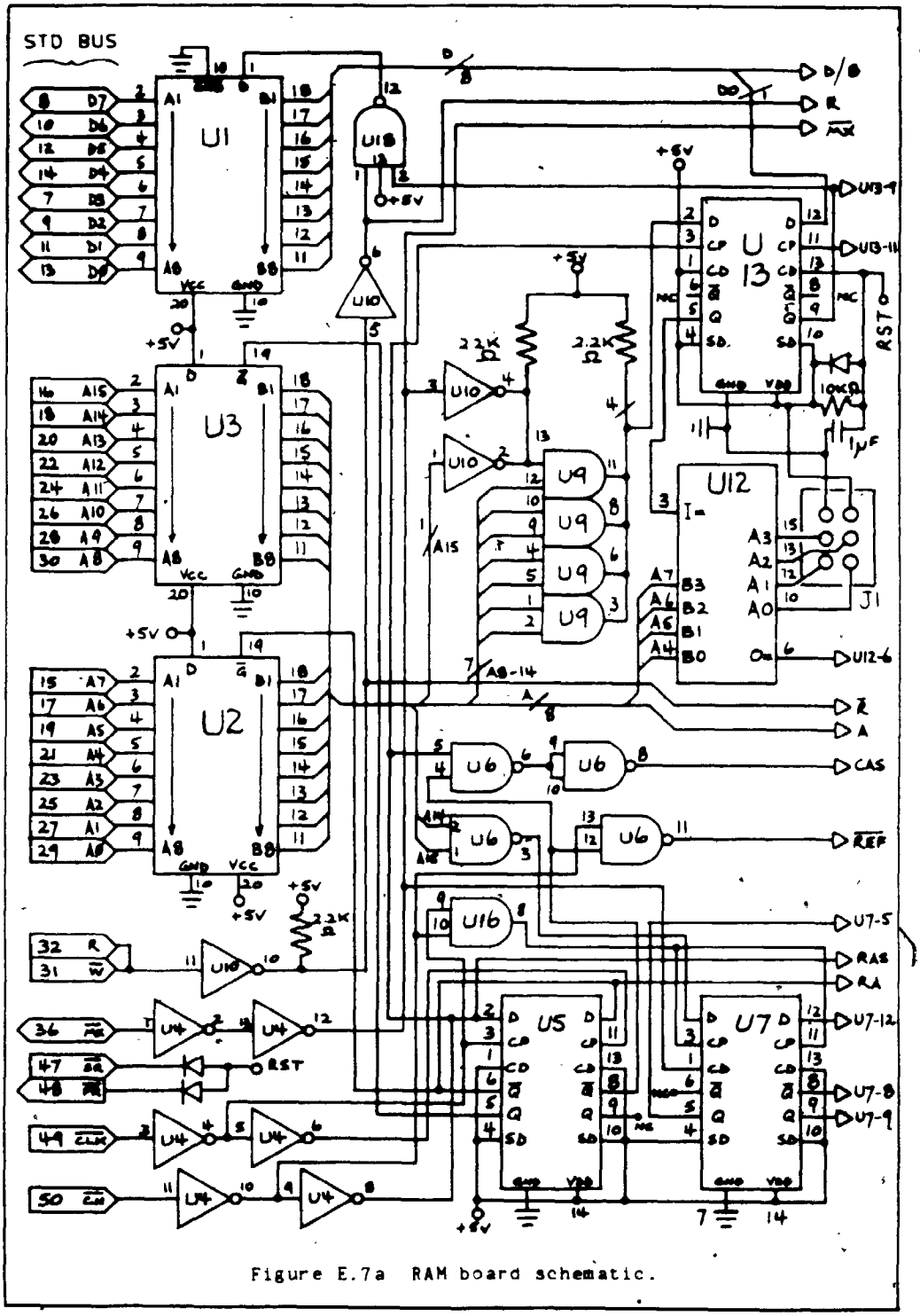


Figure E.7a RAM board schematic.

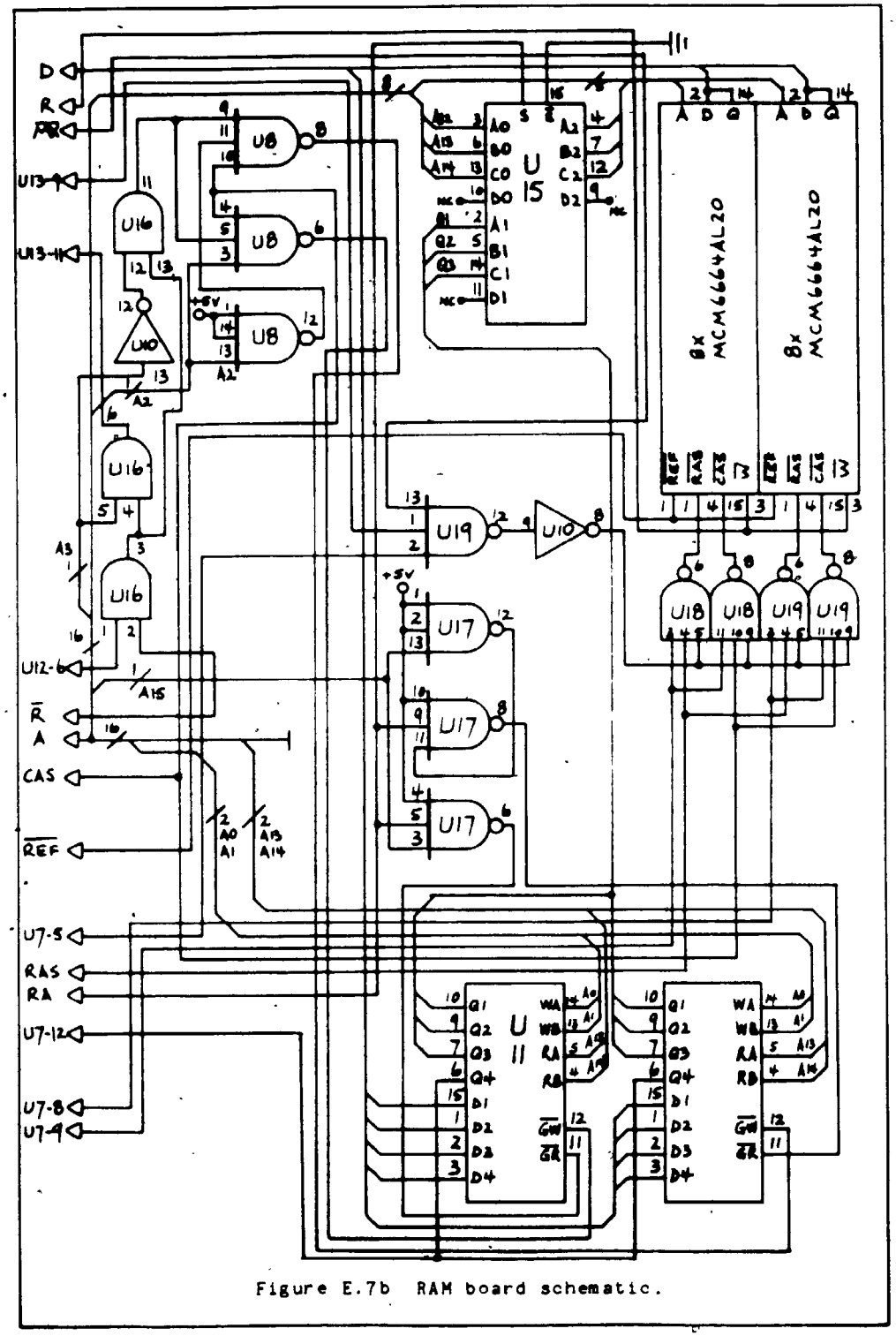
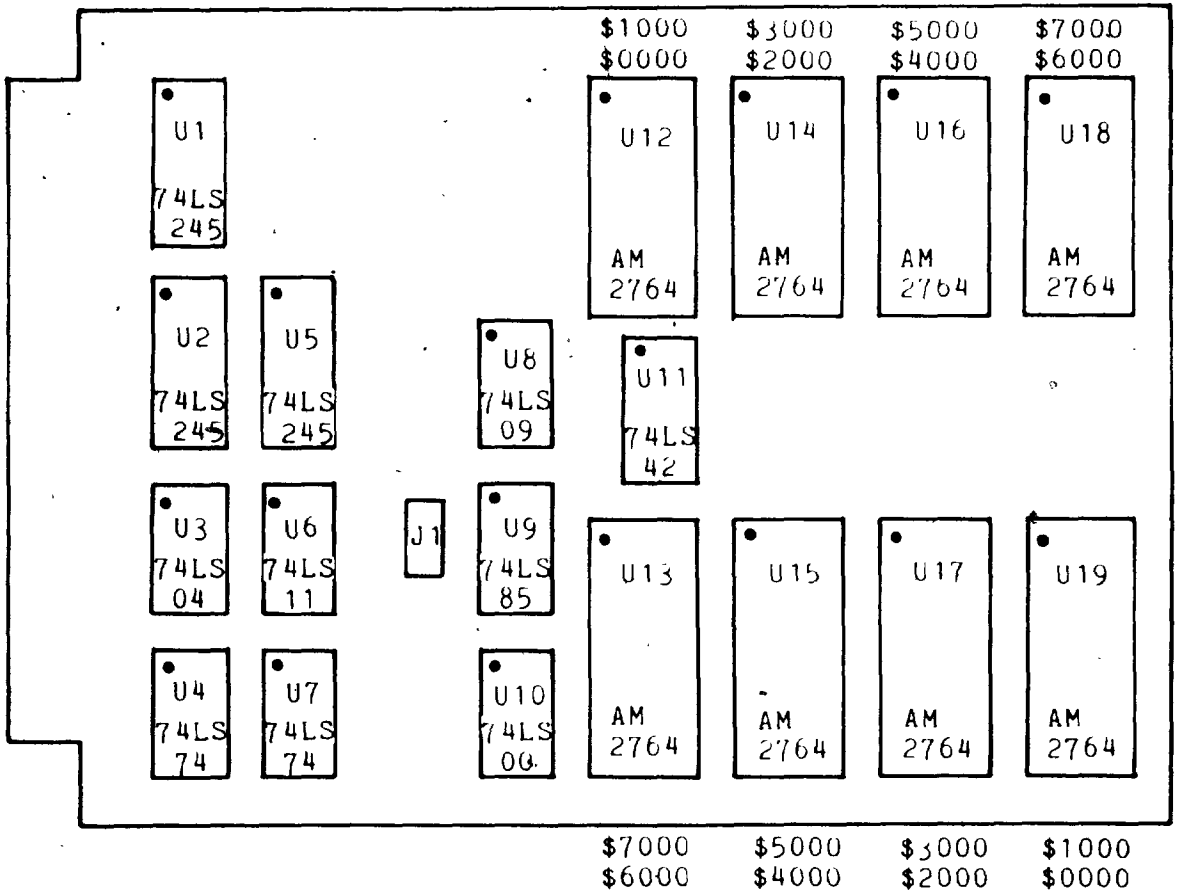
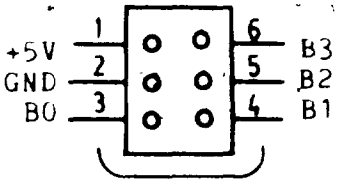


Figure E.7b RAM board schematic.





from
74LS85

J1 pinout

Figure E.8 EPROM board layout.

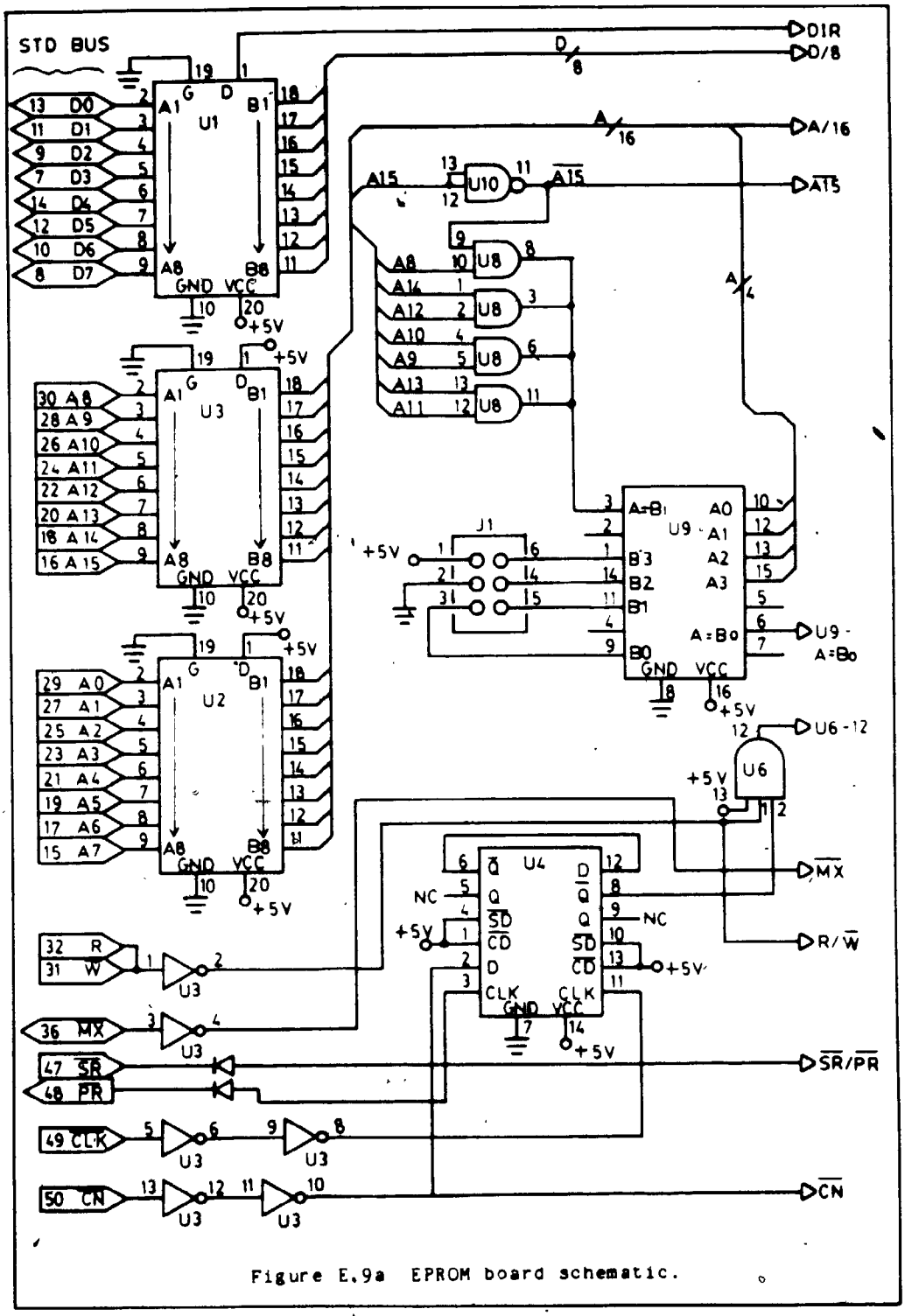


Figure E.9a EPROM board schematic.

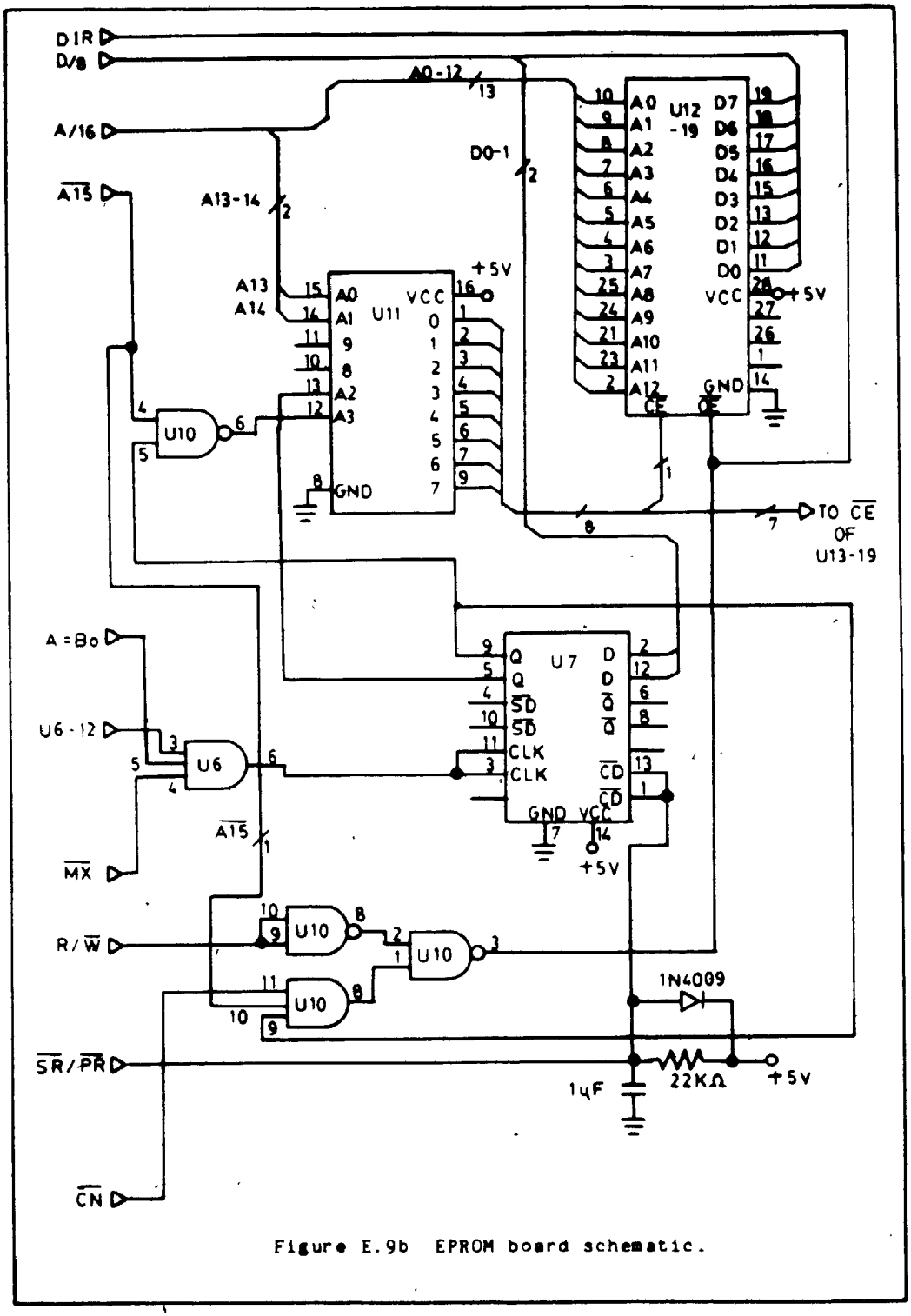


Figure E.9b EPROM board schematic.

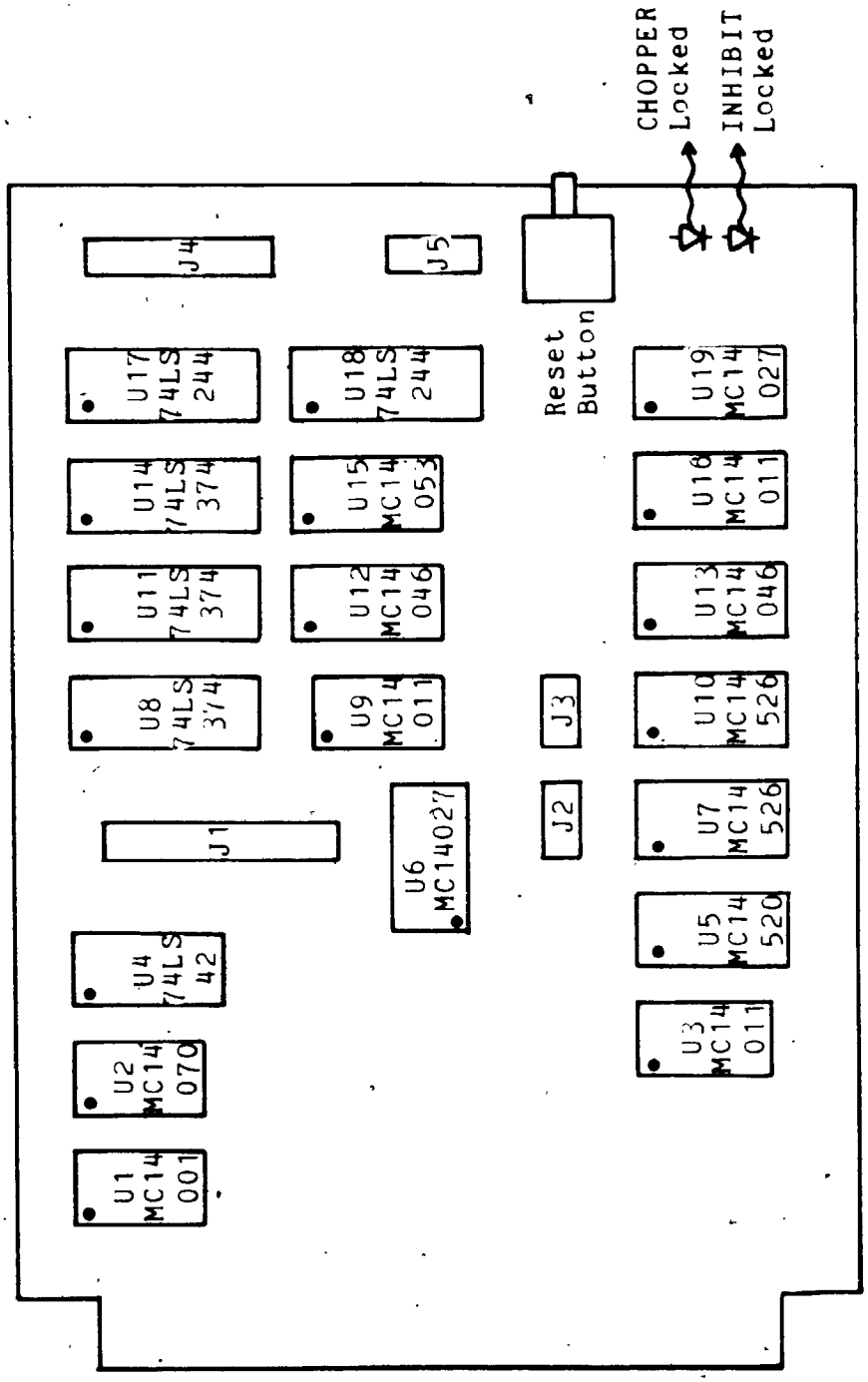


Figure E.10a Controller board layout.

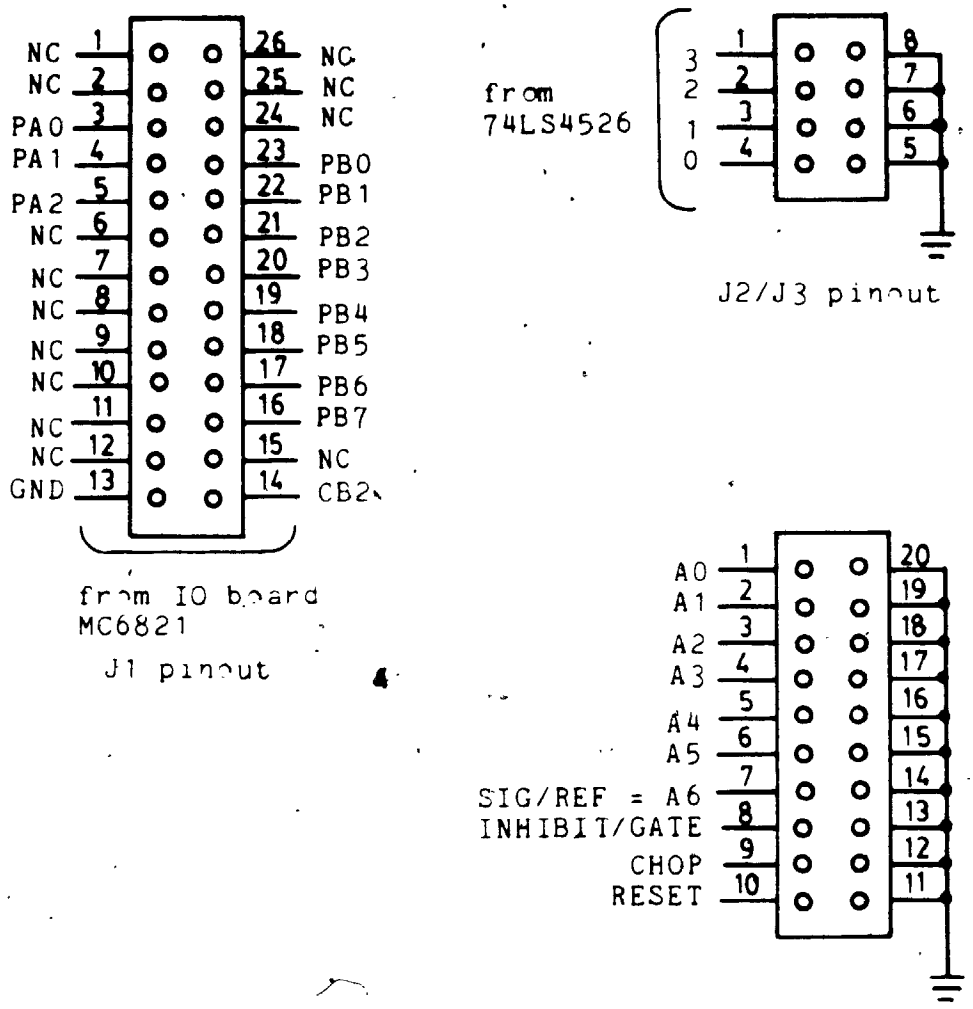


Figure E.10b Controller board layout.

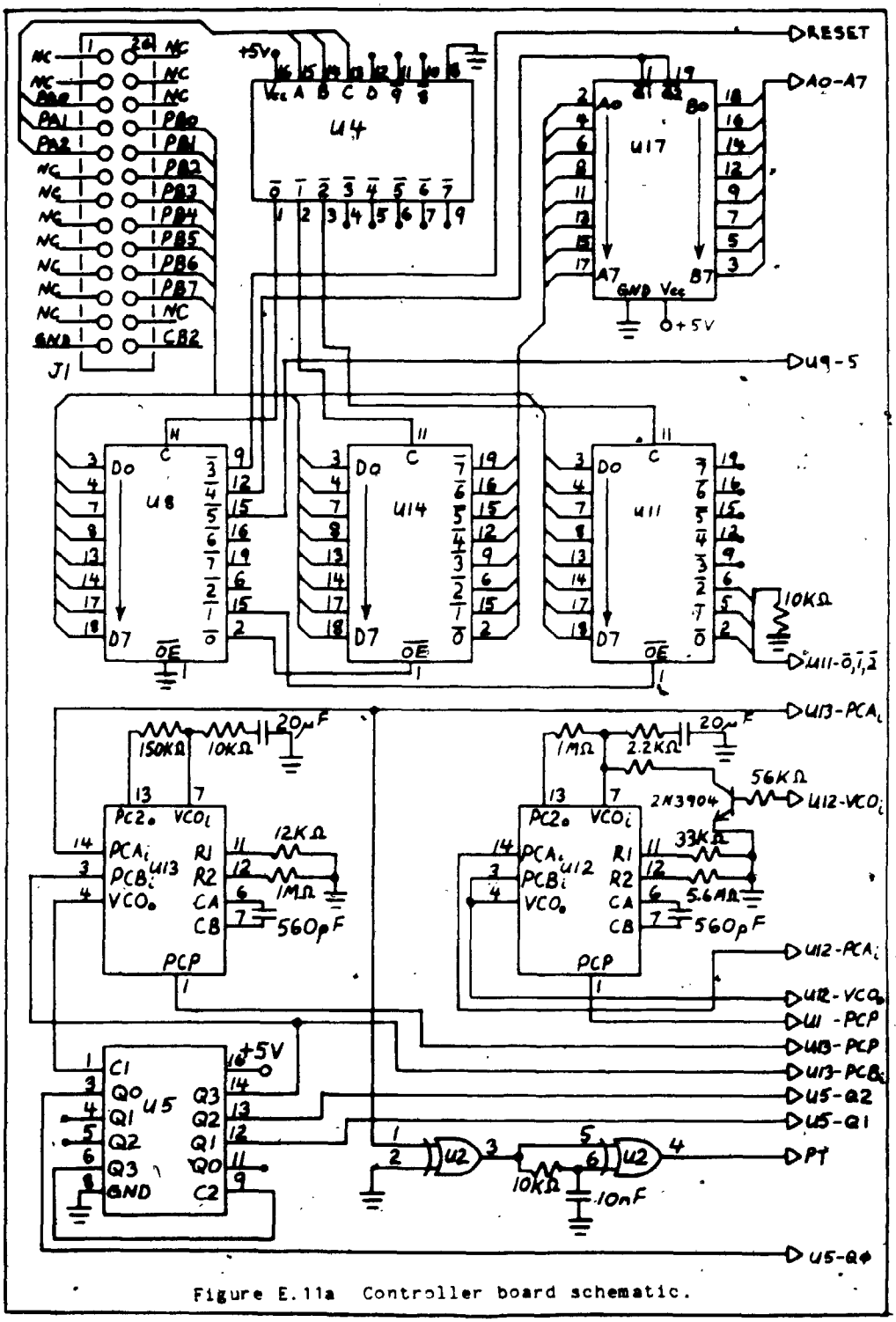


Figure E.11a Controller board schematic.

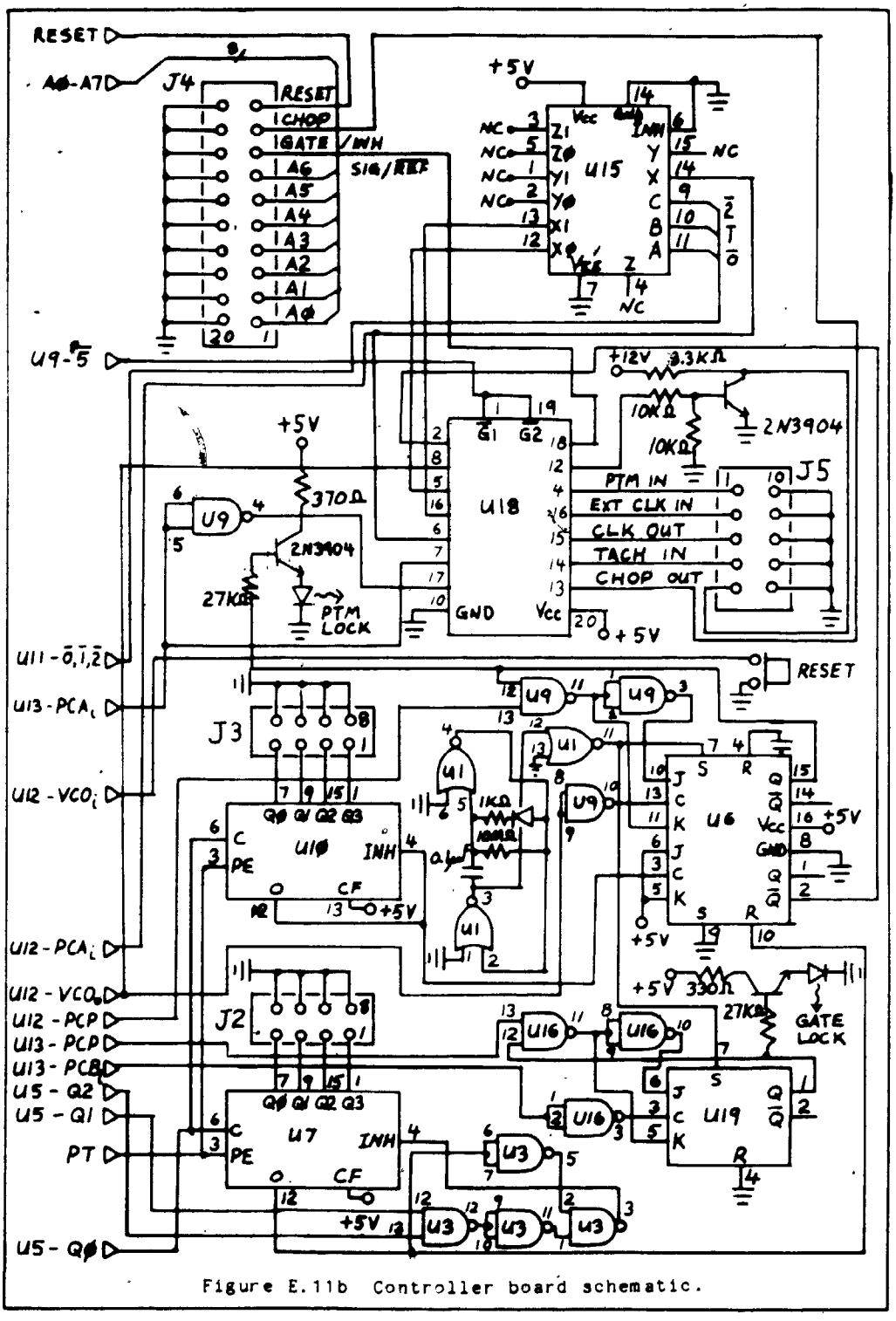


Figure E.11b Controller board schematic.

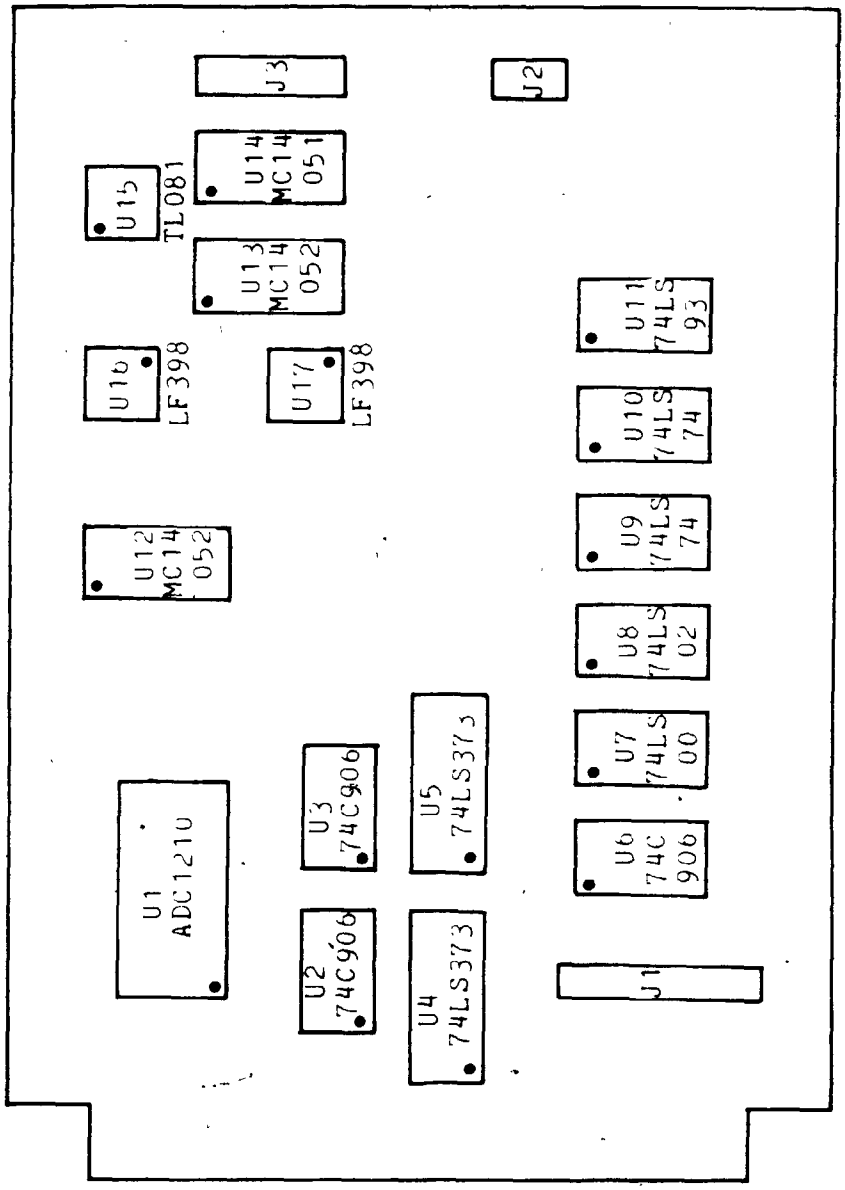
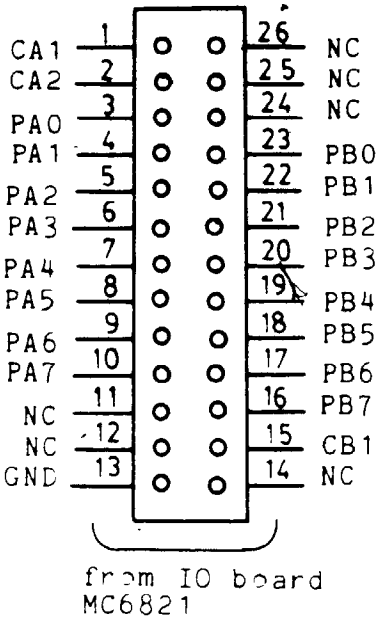
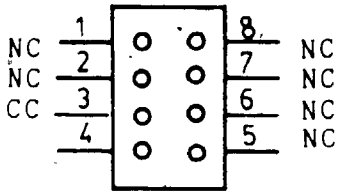


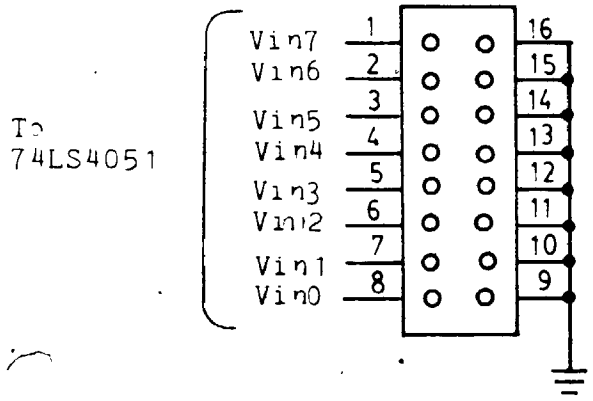
Figure E.12a. ADC board layout.



J1 pinout

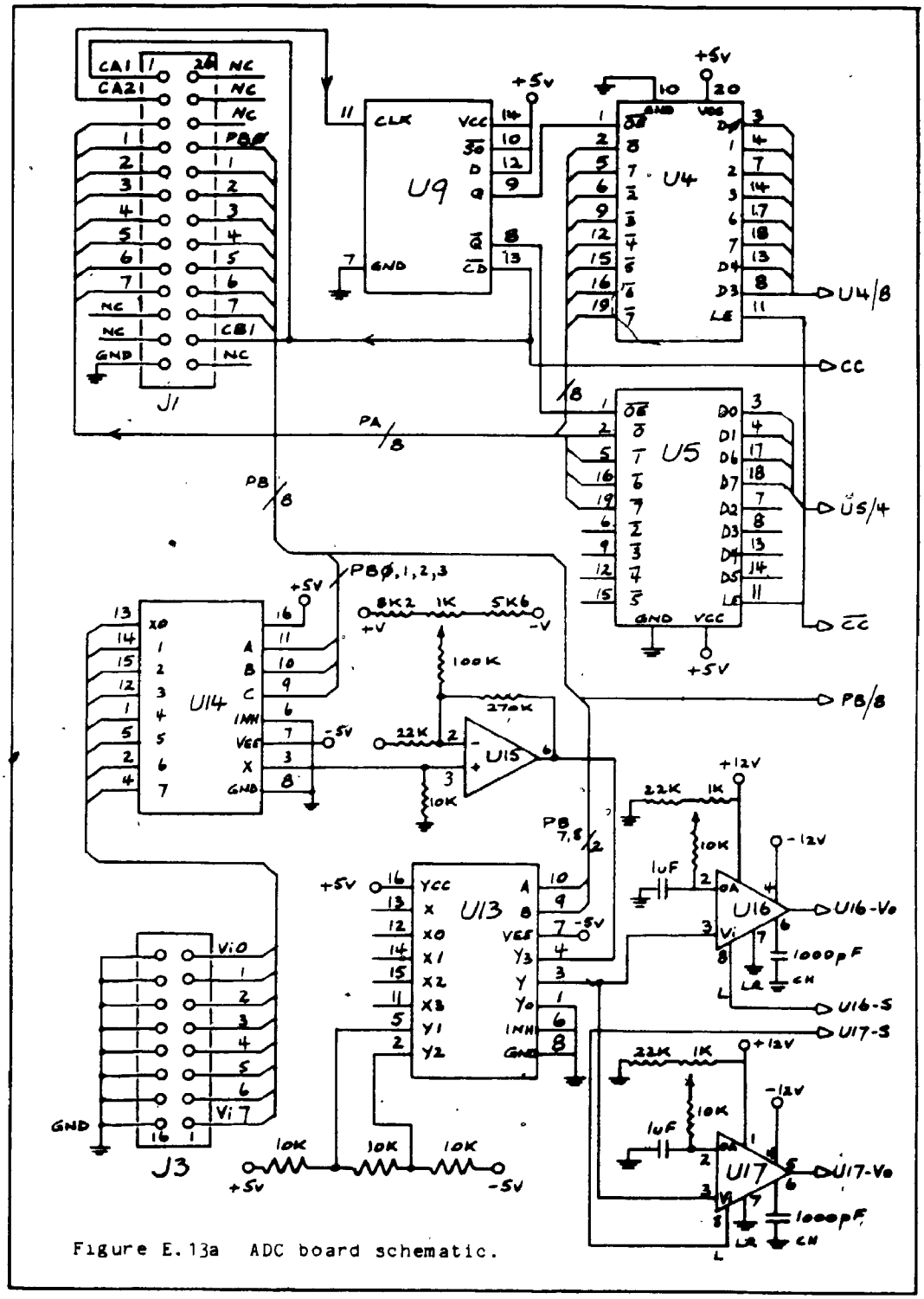


J2 pinout



J3 pinout

Figure E.12b ADC board layout.


CA1
CA2
NC
PB
CB1
GND
J1
U9
CLK
VCC
GND
U4
U4/B
CC
PA/8
PB/8
U5
U5/4
PB0,1,2,3
+5V
-5V
8K2
1K
5K6
+V
-V
100K
270K
22K
10K
U14
U15
PB/8
PB 7,8/2
U13
+12V
-12V
1uF
U16
U16-Vo
U16-S
1000pF
U17-S
U17
U17-Vo
Vi:0
Vi 7
J3
Figure E.13a ADC board schematic.

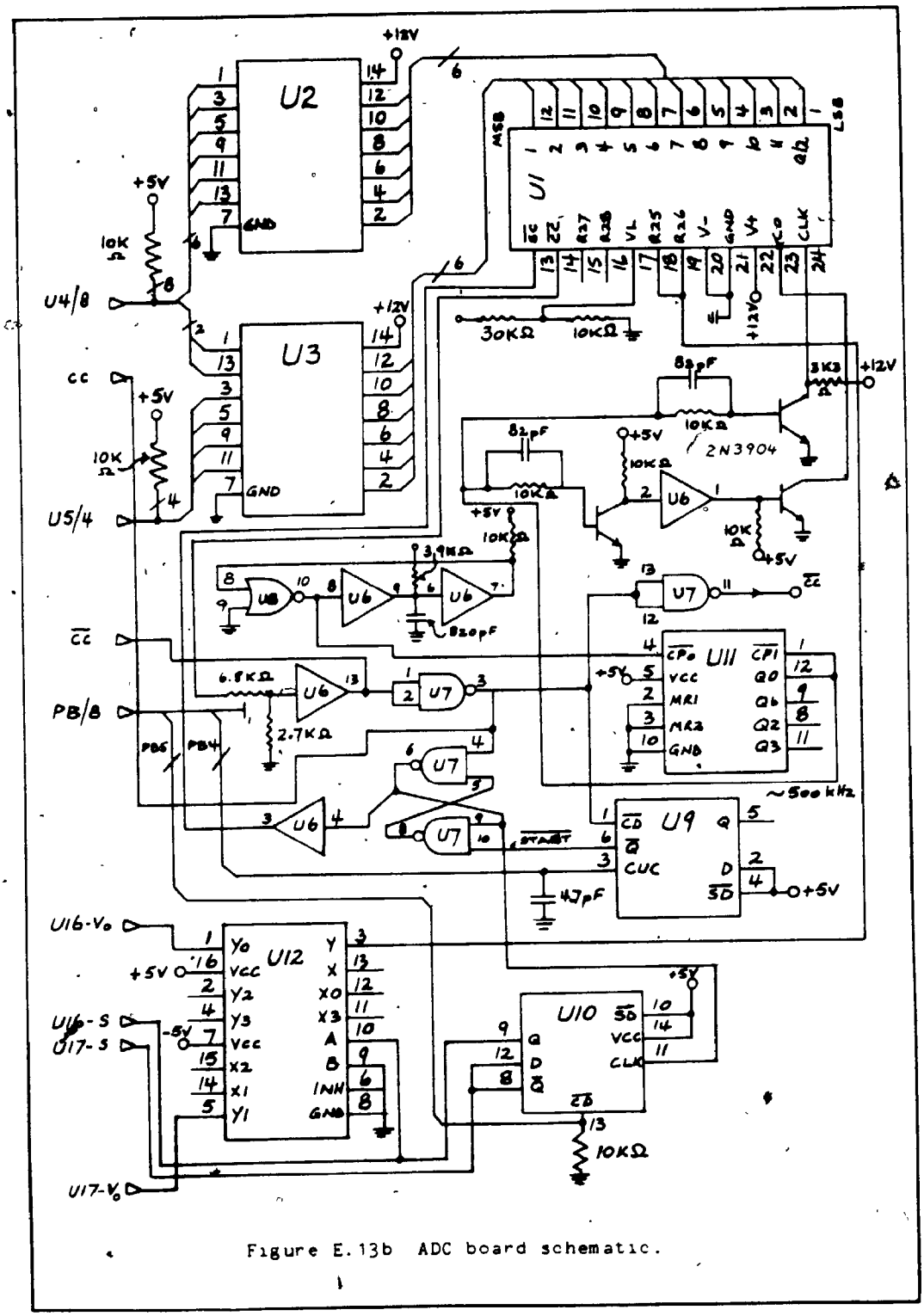


Figure E.13b ADC board schematic.

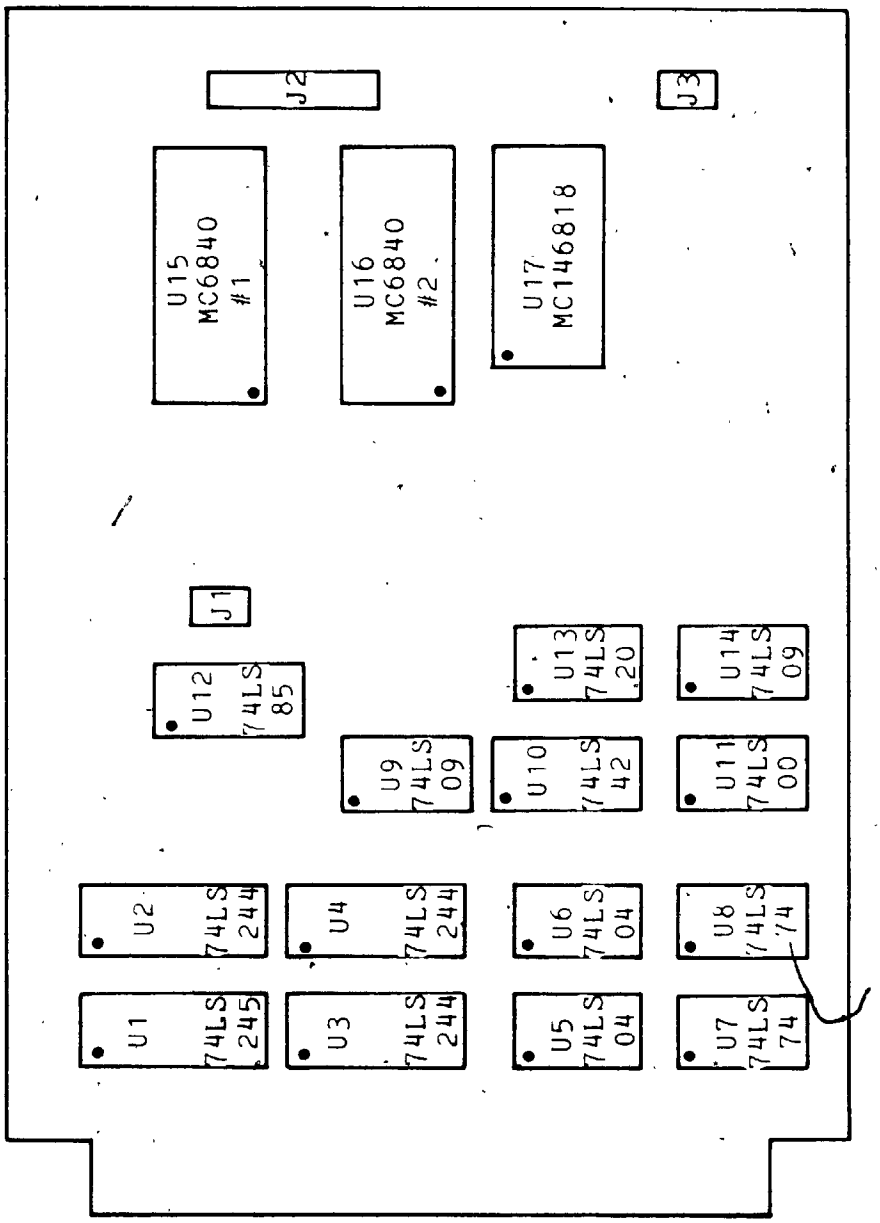


Figure E.14: RTC/PTM board layout.

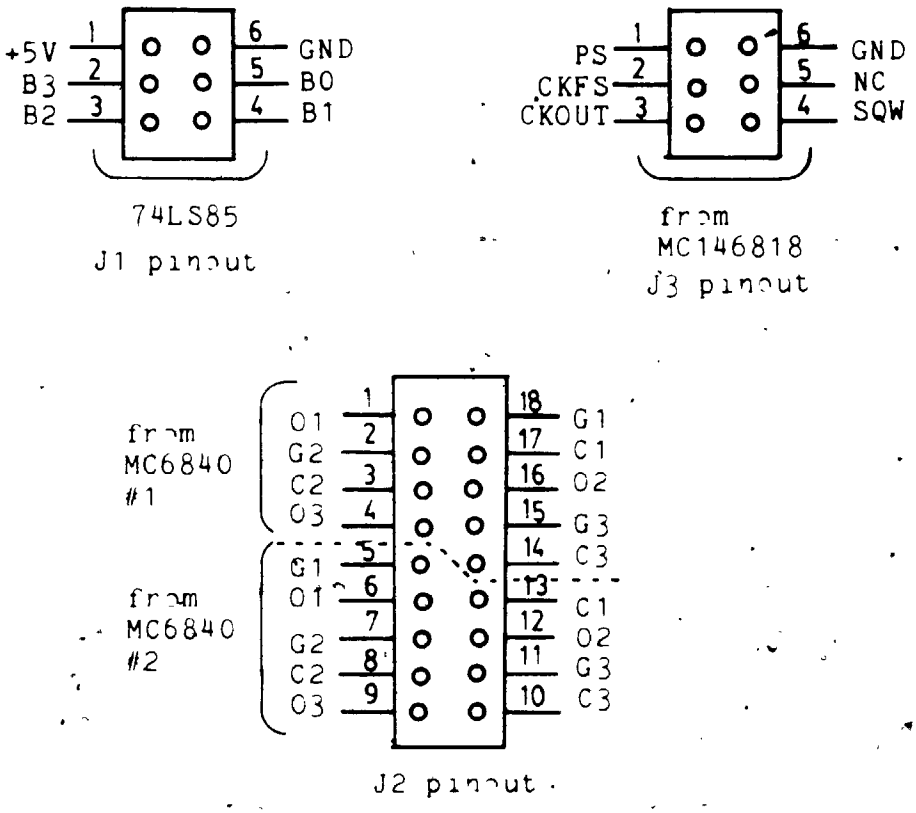


Figure E.14b RTC/PTM board layout.

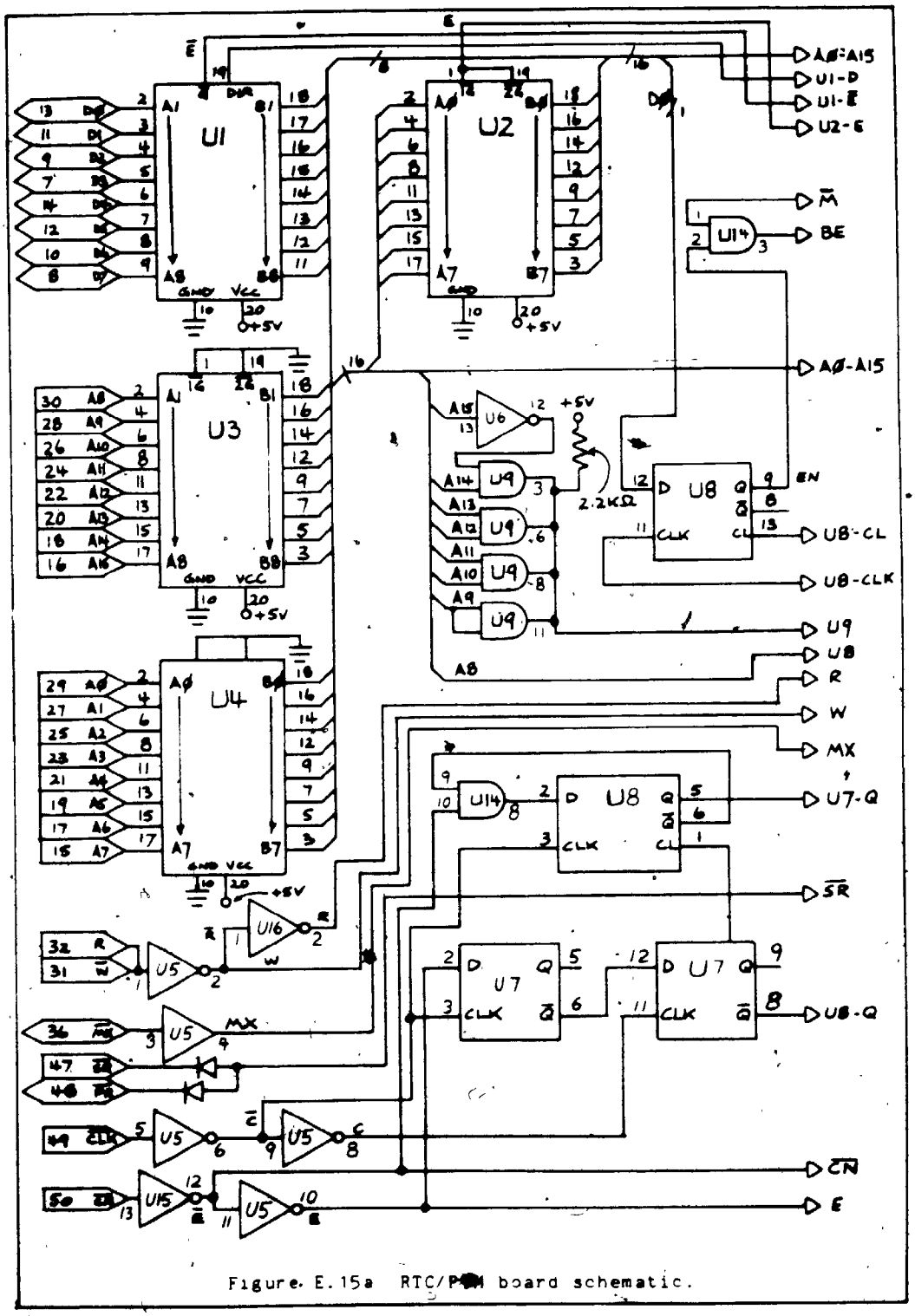


Figure E.15a RTC/PSM board schematic.

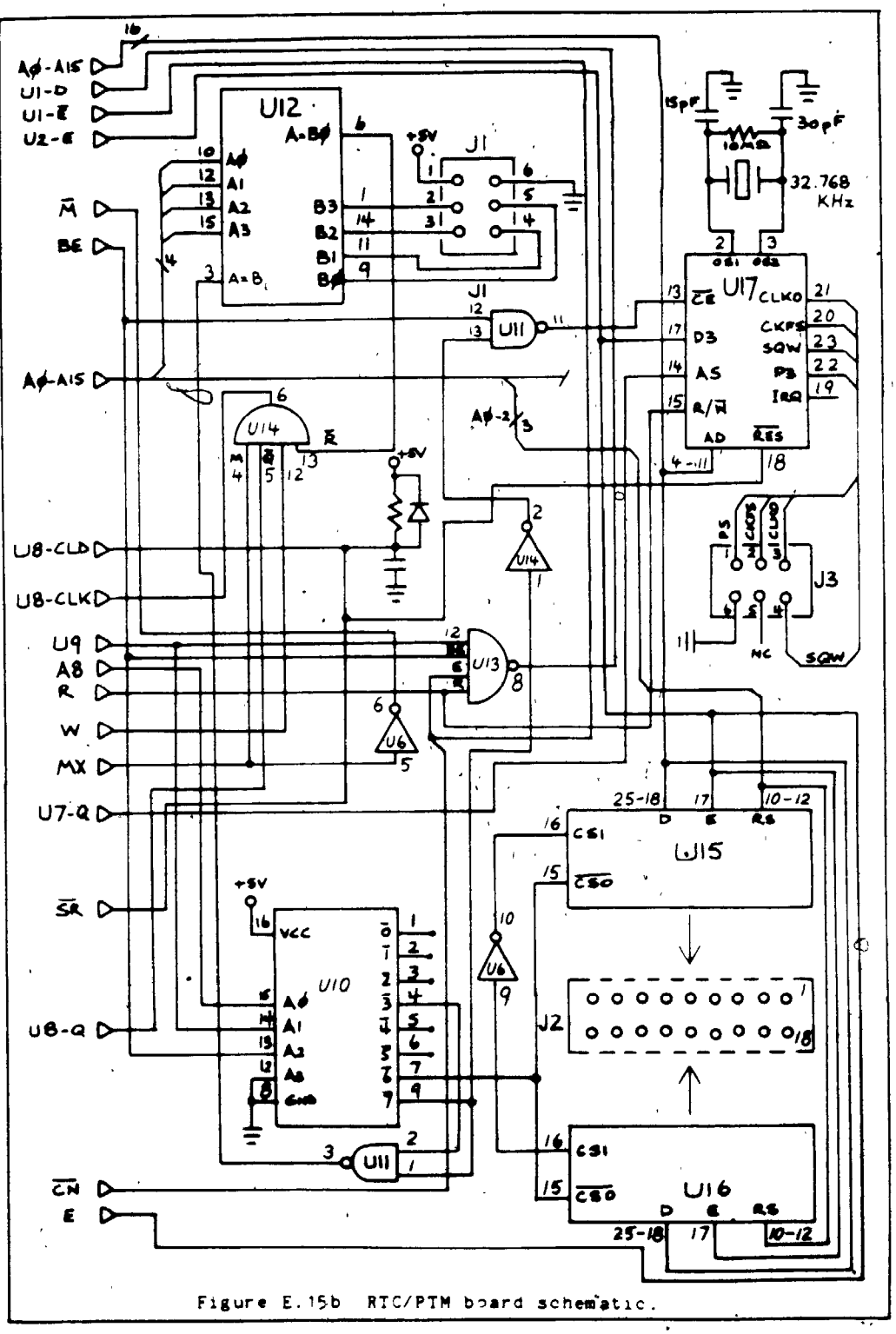


Figure E.15b RTC/PTM board schematic.

Appendix F

F.1 Software Routines for the MCSA

Table F.1 lists the FORTH routines required by the microcomputer to run the multichannel spectrum analyzer. The table groups the routines according to their types as was outlined in section 4.10.

Table F.2 lists the same routines but arranged according to the way they appear in the FORTH dictionary and also the way they appear stored on the EPROM board.

Following the tables are the source listings for those routines that have been written in FORTH.

Table F.1 List of FORTH routines according to type.

1) Low FORTH routines:

QRCV	QXMT	SRCRD	GETW
PUTW	SWAP-	=IF	TS@
TS!	TSC@	TSC!	DAT!
DAT@	DATC!	DATC@	

2) High FORTH routines:

VTS	DL4TH	VT	VTSR
VTDL	CMPR	START	LOG2
CNCA	CACN	OUTPUT	LINEAR
LOG	TIDY	ED	CAT

3) Board/device commands:

MBMMP	MBE	EBE	CBE
DBUS	RPIA2	SPIA2	WCR
WSW	WAR	RST	SPIA1

4) Low applications routines:

$DATE	DATE	EPGM	TM
ADC0	%ISPEC0	%ISPEC1	%PSPEC0

5) High applications routines:

FADC0	-USPEC	ISPEC	PSPEC

6) Graphics primitive

-ON	-OFF	-ES	-CLR
-[]	-V	-P	-[]R
-VR	-PR		

7) Graphics routines:

-AXIS	-VLIN

Table F.2 List of FORTH routines in dictionary.

1) Precompiled FORTH routines (on CPU board).

MBMMP	MBE	EBE	CBE
DBUS	SDATE	DATE	VTS
DL4TH	QRCV	QXMT	SRCRD
GETW	PUTW	EPGM	CMPR
SWAP-	=IF	RPIA2	SPIA2
WCR	WSW	WAR	RST
TM	SPIA1	ADC0	START

2) Uncompiled FORTH routines (on EPROM board)

TS@	TS!	TSC@	TSC!
DAT!	DAT@	DATC!	DATC@
LOG2	%LOGF	CNCA	CACN
-ON	-OFF	-ES,	-CLR
-[]	-V	-P	-[]R
-VR	-PR	-AXIS	-VLIN
FADC0	OUTPUT	-USPEC	SPEC
%ISPEC0	%ISPEC1	ISPEC	%PSPEC0
PSPEC	LINEAR	LOG	TIDY
ED	CAT		

```
(       FORTH Routines for the
        Multichannel Spectrum Analyzer
)
: MBMMP ( Usage: r7 r6 r5 r4 r3 r2 r1 r0 MBMMP )
  15 FFD0 C!     ( enable bus, clear MEMEX to access board
        control )
  7FF8 7FF0 DO I C! LOOP ( loop through and initialize
        memory map to the values: r0 to r7 )
  1 7FF8 C! ( enable memory board )
  1D FFD0 C! ; ( set MEMEX for normal operation )

: MBE   ( Usage:  MBE )
  DBUS  ( disable all boards and disable bus )
  7 6 5 4 3 2 1 0 MBMMP ; ( set mapping registers to
        physical location )

: EBE   ( Usage: 0/1 EBE )
  DBUS ( disable all boards and disable bus )
  15 FFD0 C! ( enable bus, clear MEMEX )
  2 * 1+ 7F00 C! ( select EPROM section )
  1D FFDO C! ; ( clear MEMEX for normal operation )

: CBE   ( Usage:  CBE )
  DBUS  ( disable all boards, disable bus )
  15 FFD0 C! ( enable bus, clear MEMEX )
  1 7F10 C!      ( enable RTC/PTM board )
  1D FFD0 C! ;  ( set MEMEX for normal operation )

: DBUS  ( Usage:  DBUS )
  15 FFD0 C! ( enable bus, clear MEMEX )
  8000 7F00 DO 0 I C! 8 +LOOP ;

: SDATE ( Usage:  yy mm dd hh mm ss SDATE )
  80 7F0B C!     ( set SET-bit only in reg. B )
  20 7F0A C!     ( set DVn for 32KHz, reset rest of reg A )
  7F00 C!        ( set seconds )
  7F02 C!        ( set minutes )
  7F04 C!        ( set hours )
  1 7F06 C!      ( set day to Sunday )
  7F07 C!        ( set day of month )
  7F08 C!        ( set month )
  7F09 C!        ( set year )
  0 7F0B C! ;    ( start normal operation )

: DATE  ( Usage: DATE )
  7F09 C@ . 7F08 C@ . 7F07 C@ .
  SPACE 7F04 C@ . 7F02 C@ 7F00 C@ . ;

: SPIA1 ( sets PIA-1 for adc-board )
  28 FFC1 C! 0 FFC0 C! 2C FFC1 C!
  32 FFC3 C! FF FFC2 C! 36 FFC3 C! ;
```

```
: SPIA2 ( sets PIA-2 for controller-board )
  0 FFC5 C! FF FFC4 C! 4 FFC5 C!
  0 FFC7 C! FF FFC6 C! 2C FFC7 C! ;

: WPRA
  FFC4 C! ;

: WPRB
  FFC6 C! ;

: WCR ( write to cntrl-reg on controller-brd )
  0 WPRA FFC6 C! ;

: WSW ( write to switch-rer on controller-brd )
  1 WPRA FFC6 C! ;

: WAR ( write to address-reg on controller-brd )
  2 WPRA FFC6 C! ;

: RST ( reset controller-board )
  83 7E11 C! 3 7E10 C! 600 7E14 ! 2 7E10 C! ;

: TM ( Usage: chopper-speed TM )

  7E14 ! ;

: ADC0 ( Usage: ADC0 adc-value )
  E0 FFC2 C! F0 FFC2 C! F8 FFC2 C!
  BEGIN FFC1 C@ 7F > UNTIL
  BEGIN FFC3 C@ 7F > UNTIL
  FFC2 C@ DROP FFC0 C@ 100 * FFC0 C@ + 0FFF AND ;

: START ( start-up everything )
  DBUS CBE RST SPIA2 1 WSW CC WCR FF WAR 400 TM SPIA1 ;

SP@ VARIABLE TS0 (  top-of-stack for local variables  )

: SWAP- SWAP - ;

: =IF COMPILE OVER COMPILE = [COMPILE] IF ;

: TS@ TS0 SWAP- @ ;

: TS! TS0 SWAP- ! ;

: TSC@ TS0 SWAP- C@ ;

: TSC! TS0 SWAP- C! ;

0 VARIABLE DAT (  general purpose data reg )
  20 ALLOT
```

```
: DAT! DAT + ! ;

: DAT@ DAT + @ ;

: DATC! DAT + C! ;

: DATC@ DAT + C@ ;

0 VARIABLE LOGT
  2680 , 5269 , 759D , 95C0 ,
  B350 , CEAE , E829 , FFFF ,

: LOG2
  -DUP IF ABS ELSE 1 ENDIF 10 0
  DO DUP 3FFF > IF I LEAVE ELSE 2 * ENDIF LOOP
  0E SWAP- SWAP 4000 - DUP >R 800 / 2 * DUP DUP
  2+ LOGT + @ SWAP LOGT + @ - OVER 400 * R> SWAP- 800 */
  SWAP LOGT + @ + SWAP ;

: %LOGF
  LOG2 C0 U/ SWAP DROP ;

: CNCA (  chan-  CNCA chan-addr  )
  DUP 10 <
  IF 10 SWAP- 4 * 3 -
  ELSE DUP 20 <
    IF 20 SWAP- 4 * 1 -
    ELSE DUP 30 <
      IF 20 - 4 * 2+
      ELSE 30 - 4 *
      ENDIF
    ENDIF
  ENDIF ;

: CACN (  chan-addr CACN chan-  )
  4 /MOD SWAP 0
  =IF DROP 30 +
  ELSE 1
    =IF DROP 0F SWAP-
    ELSE 2
      =IF DROP 20 +
      ELSE DROP 1F SWAP-
      ENDIF
    ENDIF
  ENDIF ;

: -ON 1B EMIT ." Pp" ;

: -OFF 1B EMIT ." " ;

: -ES ." S(E)" ;
```

```
: -CLR -ON -ES -OFF ;

: -[] ( y-coord. x-coord -[] )
  5B EMIT . 2C EMIT . 5D EMIT ;

: -V ( y-coord x-coord -V )
  56 EMIT -[] ;

: -P ( y-coord x-coord -P )
  50 EMIT -[] ;

: -[]R ( dy dx -[]R )
  5B EMIT DUP 0< IF ELSE 2B EMIT ENDIF .
  2C EMIT DUP 0< IF ELSE 2B EMIT ENDIF . 5D EMIT ;

: -VR ( dy dx -VR )
  56 EMIT -[]R ;

: -PR ( dy dx -PR )
  50 EMIT -[]R ;

: -AXIS
  [ DECIMAL ] DECIMAL
  -ES 0 100 -P 400 100 -V 400 760 -V
  0 90 -P 11 0
  DO 0 10 -VR 40 -10 -PR
  LOOP 410 70 -P 17 0
  DO -10 40 -PR 10 0 -VR
  LOOP 17 0
  DO 420 I 40 * 105 + -P ." T'" I 32 * 4 + . ." '"
  LOOP 450 285 -P ." T(S2,H2)'FREQUENCY [MHz]'"
  300 20 -P ." T(D90)(S2,H2)(D90)'AMPLITUDE'"
  ." T(D0)(S1)(D0)' '" 0 0 -P [ HEX ] HEX ;

: -VLIN ( table-addr n-data -VLIN )
  [ DECIMAL ] DECIMAL 4 * OVER + SWAP 0 ROT ROT
  DO I @ I 2+ @ ABS 25 256 */ 400 SWAP- SWAP 4 - 10 8 */
  110 + 0 OVER -P ." V(W(E))[+0,+400]" -V ?TERMINAL
  IF DROP 1 ENDIF 4 +LOOP [ HEX ] HEX ;

' NOOP CFA 0A DAT!

: FADC0 ( control- FADC0 )
  DUP 2
  IF 40 * >R 40 0
    DO 3F I - CNCA J + WAR ADC0 0A DAT@ EXECUTE
      1FC I 8 * -
    LOOP R> DROP
  ELSE 2
  =IF DROP 40 0
    DO 3F I - CNCA DUP WAR ADC0 SWAP 40 +
      WAR ADC0 - 0A DAT@ EXECUTE 1FC I 8 * -
    LOOP
```

```
  ELSE DROP
  ENDIF ENDIF ;

: PORT ( port-  PORT )
  2 * FFC6 + DUP D018 ! D01A ! ;

: OUTPUT ( tab-addr  -of-words OUTPUT )
  DECIMAL 0D EMIT 0A EMIT 8 /MOD >R SWAP R> 0
  DO 8 0
    DO ?TERMINAL DROP DUP @ 5 .R 2+
    LOOP 0D 0A EMIT EMIT
  LOOP SWAP DUP
  IF 0
    DO ?TERMINAL DROP DUP @ 5 .R 2+
    LOOP
  ELSE DROP
  ENDIF DROP HEX ;

: -USPEC
  2 0 DATC! ( port 2 )
  2 1 DATC! ( sig-ref data )
  43 2 DATC! ( 'C' for continuous sweep and display )
  CR ." 2 or 3 (2)? " KEY 33 =
  IF 33 0 DATC! ENDIF
  -ON -AXIS
  BEGIN
    1 DATC@ FADC0 4 DAT@ EXECUTE SP@ 40 -VLIN
    IF FFC9 C@ 2 DATC!
    ENDIF 1 2 DATC@
    43 ( 'C' - cont. sweep )
    =IF SWAP DROP 0 SWAP
    ENDIF
    53 ( 'S' - single sweep )
    =IF DROP DROP 0 KEY
    ENDIF
    44 ( 'D' dump data )
    =IF DROP DROP 0 53
      0 DATC@ PORT SP@ 4 + 80 OUTPUT 1 PORT
    ENDIF
    52 ( 'R' - sweep ref )
    =IF 1 1 DATC! SWAP DROP 0 SWAP
    ENDIF
    47 ( 'G' - sweep sig )
    =IF 0 1 DATC! SWAP DROP 0 SWAP
    ENDIF
    46 ( 'F' - sweep sig-ref )
    =IF 2 1 DATC! SWAP DROP 0 SWAP
    ENDIF
    8 DAT@ EXECUTE
    0D ( <cr> - exit )
    =IF DROP DROP 1 1
    ENDIF 2 DATC! >R
    SP! R>
```

```
  UNTIL -OFF ;

: SPEC
  ' NOOP CFA DUP 4 DAT! 8 DAT! -USPEC ;

: %ISPEC0 (  Averaging routine )
  6 DAT@ @ FFFF =
  IF SP@ 6 DAT@ 100 CMOVE
  ELSE 100 2
    DO I 6 DAT@ + DUP @ 3 DATC@ DUP 1 - SWAP */
      SP@ 4 + I + DUP @ 3 DATC@ /
      ROT + DUP ROT ! SWAP ! 4
    +LOOP
  ENDIF ;

: %ISPEC1
  49 =IF DROP DROP 0 53 FFFF 6 DAT@ ! ENDIF ;

: ISPEC (  interval ISPEC  )
  3 DATC! CF00 6 DAT! FFFF 6 DAT@ ! ' %ISPEC0 CFA
  4 DAT! ' %ISPEC1 CFA 8 DAT! -USPEC ;

: %PSPEC0 (  Peak routine  )
  6 DAT@ @ FFFF =
  IF SP@ 6 DAT@ 100 CMOVE
  ELSE 100 2
    DO I 6 DAT@ + DUP @
      SP@ 4 + I + DUP @
      ROT MAX DUP ROT ! SWAP ! 4
    +LOOP
  ENDIF ;

: PSPEC
  CF00 6 DAT! FFFF 6 DAT@ ! ' %PSPEC0 CFA 4 DAT!
  ' %ISPEC1 CFA 8 DAT! -USPEC ;

: LINEAR
  ' NOOP CFA 0A DAT! ;

: LOG
  ' %LOGF CFA 0A DAT! ;

: PFRQ ( frq port-  PFRQ )
  SWAP DUP 209 > IF DROP 208 0D 2 DATC!
  -OFF 7 EMIT -ON ENDIF SWAP PORT U.
  ." FRQ" D EMIT 1 PORT ;

: TD ( 0.1 second intervals of time delay )
  0 DO 589 0 DO LOOP LOOP ;

: %CSPEC0
  %PSPEC0 0C DAT@ DUP 3 PFRQ 0E DATC@ + 0C DAT! 28 TD ;
```

```
: %CSPEC1
  49 =IF DROP DROP 0 53 FFFF 6 DAT@ ! 4 C DAT! ENDIF ;

: CSPEC ( start-freq. freq.-step CSPEC )
  0E DATC! 0C DAT! CF00 6 DAT! FFFF 6 DAT@ ! ' %CSPEC0
  CFA 4 DAT! ' %CSPEC1 CFA 8 DAT! -USPEC ;
```

Appendix G

G.1 Electronic RF Chopper

An electronic RF chopper modulator was designed and built to facilitate the testing of the multichannel spectrum analyzer. It consists of four RF ports and one input chopper signal port. The chopper operates by alternately switching the input RF signal from one output port to another port. If one of the output ports is terminated in 50Ω , then the RF signal at the other port will appear switched or chopped off and on.

The RF chopper was designed in a diode bridge configuration as shown in figure G.1. A total of 12 PIN diodes (MPN3401) were used in four 'T' sections between ports. When a 'T' section is turned off, the two series diodes are reversed biassed for high impedance and the shunt diode is forward biassed to short circuit any RF signal that gets through. When a 'T' section is turned on, the two series diodes are forward biassed for low impedance to allow passage of the RF signal and the shunt diode is reverse biassed for a high impedance. The transistor circuitry provides the switching signals neccessary to drive the diode bridge. The FET input provides a high input impedance to chopper signal with a threshold of 1.5 V.

The RF chopper has 8 dB loss when switched on, and 30 dB isolation when switched off, for a signal at 500 MHz.

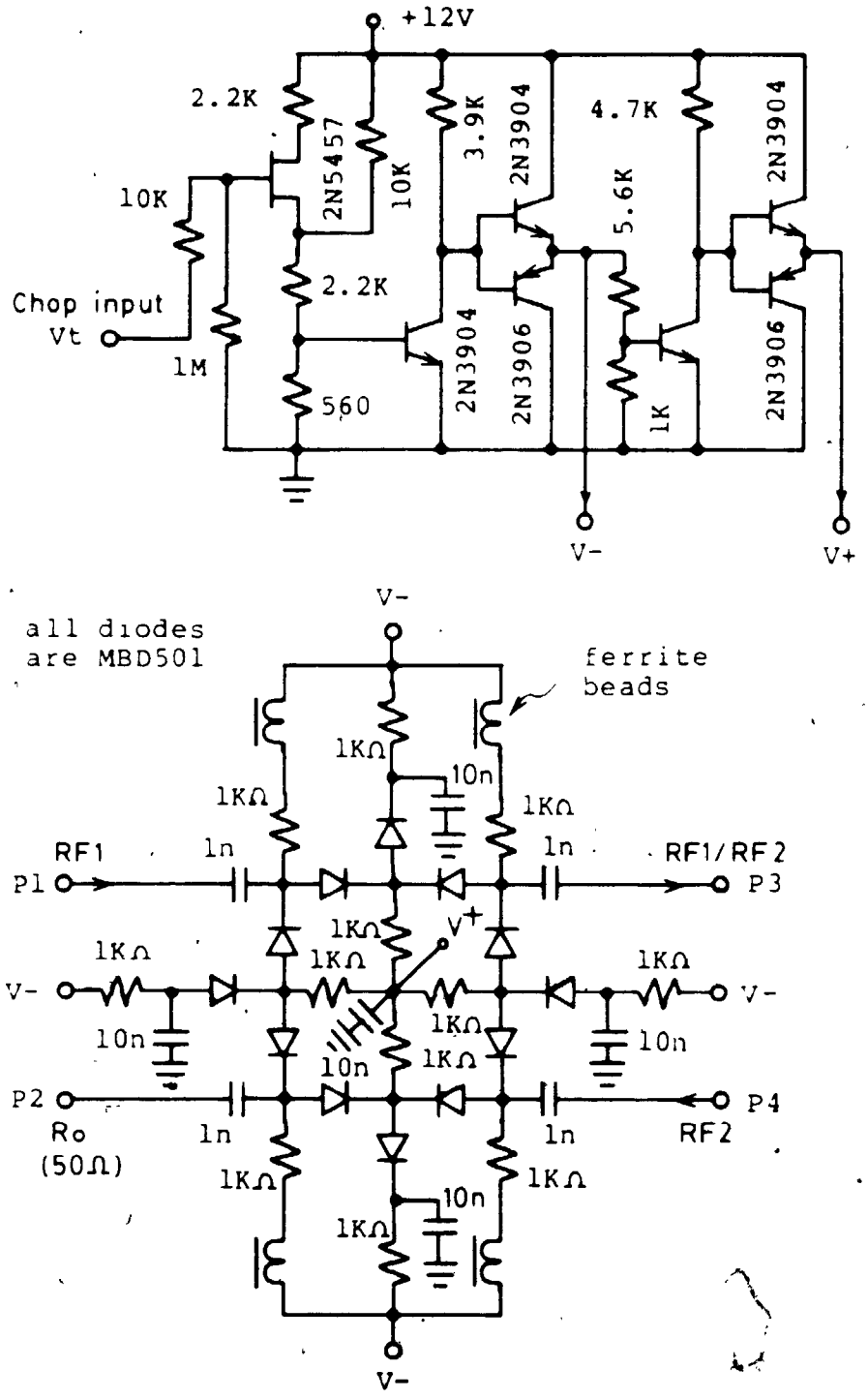


Figure G.1 Electronic RF chopper.

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