1-30-2014 12:00 AM

An Accurate Offline Phasor Estimation Technique For Fault Location In Series Compensated Lines

Rubeena Rubeena
The University of Western Ontario

Supervisor
Dr. Mohammad R. Dadash Zadeh
The University of Western Ontario

Graduate Program in Electrical and Computer Engineering
A thesis submitted in partial fulfillment of the requirements for the degree in Master of Science

AN ACCURATE OFFLINE PHASOR ESTIMATION TECHNIQUE FOR FAULT LOCATION IN SERIES COMPENSATED LINES

(Thesis format: Monograph)

by

Rubeena

Graduate Program in Electrical and Computer Engineering

A thesis submitted in partial fulfillment
of the requirements for the degree of
Masters in Engineering Sciences

The School of Graduate and Postdoctoral Studies
The University of Western Ontario
London, Ontario, Canada

Abstract

With the increasing demand of electric power supply, the necessity to transmit more power has become the need of the hour. The excess power can be transferred by building new infrastructure (costly and time taking) or by using series compensation (relatively cheaper and faster alternative). Series compensation is a technique in which line inductance is compensated by placing a capacitor in series with the line. This helps in increasing the transmission capacity of the existing line. Series compensated lines face several challenges when it comes to protection and fault location. Current and voltage signals used by the protection and fault location algorithms, contain considerable sub-synchronous frequency components (SSFCs) which do not damp sufficiently within a typical fault clearing time of the line protection system. Presence of such SSFCs affects the accuracy of the available phasor estimation techniques which in turn impacts the accuracy of phasor-based fault location algorithms. In the presented research work (refer publication 1) a new offline Prony-DFT (Discrete Fourier Transform) based phasor estimation technique is introduced, which almost eliminates these SSFCs in addition to removal of noise, harmonics and decaying DC and results in more accurate phasor estimation for fault location in series compensated transmission lines. The idea is to estimate the transient signal using Prony analysis. The transient signal thus obtained is subtracted from the original fault current/voltage signal to obtain the fundamental signal. Conventional one-cycle DFT algorithm is then used to perform phasor estimation. The performance of the proposed technique is evaluated using an assumed theoretical signal and PSCAD/EMTDC simulation and results are compared with the available accepted techniques, namely, Direct-Prony analysis and the 4-cycle Discrete Fourier transform algorithm.

Keywords: Phasor Estimation, Series Compensation, Sub-synchronous Frequency Components, Prony.

Acknowledgement

I would first like to thank Almighty God for blessing me with lovely people around without whom I would never be able to pursue and complete this research work.

I would like to express my sincere thanks and gratitude to my supervisor Dr. Mohammad Reza Dadash Zadeh for his valuable guidance throughout the course of this research. His continuous motivation and extended support has helped me in successfully completing the course and research work. He has been a great teacher, guide, mentor, well-wisher and above all a nice human being.

I would like to thank Tirath for helping me out in fault location studies. I would also like to thank ECE faculty members Dr. Rajiv Varma and Dr. Vijay Parsa for a great classroom learning experience. As a TA, I would like to extend my sincere thanks to Dr. Dilrobaei Mehdi and Dr. Adamiak for being nice and considering throughout my TA duties.

I would now like to thank one of the most important person in my life my husband Ahmad Ovais for his love, motivation and much needed emotional support which kept me going and of-course not to forget his tireless efforts in commuting between Toronto-London. Thanking them (my parents) would not be sufficient as they are the reason for my existence. I can only ask Almighty to make me an obedient child of theirs. I am also thankful to my sisters, my brothers, Ammi and Abba for their selfless love and affection.

A special mention and thanks to Mr. Atif Hamid and Sabiha Hamid for their unconditional love, help and support during my and my husbands stay in Canada and making us feel at home though miles away from home.

Last but not the least, I would like to thank ECE grad co-ordinators Melissa and Chris, for all the administrative help.

I gratefully acknowledge the financial support provided by Western University to pursue this research work.

Dedication

I dedicate this work to my beloved daughter ’ALIA’.

Contents

List of Figures

List of Tables

List of Appendices

List of Abbreviations, Symbols, and Nomenclature

CCVT: Capacitor Coupled Voltage Transformer

CT: Current Transformer

DDOCs: Decaying DC Offset Components

DFT: Discrete Fourier Transform

DTFT: Discrete Time Fourier Transform

FACTS: Flexible AC Transmission System

FSC: Fixed Series Capacitor

HV: High Voltage

MOV: Metal Oxide Varistor

RSD: Relative Standard Distribution

SC: Series Compensation

SCPU: Series Capacitor Protection Unit

SSFCs: Sub-synchronous Frequency Components

SSR: Sub-synchronous Resonance

SSSC: Static Synchronous Series Capacitor

TCSC: Thyristor Controlled Series Capacitor

THD: Total Harmonic Distortion

TSSC: Thyristor Switched Series Capacitor

Chapter 1

Introduction

1.1 Power System Protection

Power system is a complex network with three major components, i.e., generation, transmission and distribution. After generating the power, it is transferred to the end users through a complex network of transmission and distribution lines. The electric power is transmitted at a very high voltage to save losses. The level of voltage reduces as we go down to the consumer level. Electric power is available to the end user at a specified voltage and frequency, which is typically 110 V and 60 Hz in North America. The steady-state performance of the power system is achieved through careful planning, design, installation and operation of very complex networks of generators, transformers, and transmission and distribution lines. Due to the huge size of power system and proper protection mechanisms in place, the power system appears to be in a steady-state to an end user. However, in reality, it is subjected to constant disturbances of various kinds. These disturbances can be caused due to frequent changes in load conditions or by faults in the system. The faults can occur either by operator's mistake, failure of equipment (insulation failure, flashover or physical damage) or by a natural cause (like lightning and thunder storms). These faults can be short circuit (conductor to conductor) or open circuit (broken conductor) in nature. Since faults cannot be prevented and can happen any time, it is

important and critical to have a proper protection system in place.

The main role of protection system is detection of abnormal power system condition and initiation of corrective action in minimum possible time so as to isolate the faulted part and bring back the power system to steady-state. Conventional power system protection consists of three major components: 1) Transducers 2) Protection Relays and 3) Circuit interrupters (Circuit breaker). Protection relay is the brain of the protection system. The main function of a protection relay is to detect the fault and isolate the faulted section by tripping corresponding circuit breakers and restore the isolated components if the fault is cleared. But they cannot prevent the damage already happened because they detect the fault only after it takes place. Therefore, the purpose of protection is to prevent any further damage to the equipment, reduce stress on other equipments, remove the faulted part from the system as soon as possible in order to maintain the system's stability and integrity and most importantly, minimize any danger to the human. Thus, speed is an important aspect of protective relaying and is important to minimize the impact of a fault on the power system or its equipments. Other important aspects are sensitivity, selectivity and reliability [1].

Selectivity is the capability to discriminate between the faults inside the protection zone and those outside it. This requirement is important to ensure that the minimum area is isolated in the event of any fault condition. Sensitivity is the capability to discriminate between the fault and normal conditions, although the difference between the two is small. This ensures the correct operation of the protection system during faults and other power system scenarios which can bring fault and normal conditions closer to each other. Reliability is the degree of certainty that a protection system will work correctly. This requirement depends on two factors: dependability and security. Dependability is the ability of a relay to operate correctly when it is required. It is important because a less dependable system means it might not operate when required. Security is the ability of a relay to never operate incorrectly [5].

For accurate fault diagnosis and decision making, protection relays depend on current and voltage signals measured by the instrument transformers. These days industrial practice is to

use numerical relays. A numerical relay can be visualized as a black box with input, processor and output blocks. First, the current and voltage signals are fed to the relay. Then these signals are converted into digital samples for further processing in digital signal processors and microprocessor units where protection algorithms are implemented. Finally, once the processing is over and decision is made by the relay, the output module sends the decision to corresponding circuit breakers.

Most of the protection algorithms use voltage and current phasors to implement various protection functions. Therefore, it is important to accurately determine the voltage and current phasors. Any error in phasor determination may affect the decision made by the protection relays. Fault location is another important area in relaying after detection and isolation of the fault. The accuracy of fault location is important in order to pinpoint the fault, do the maintenance and restore the system back to normal condition as soon as possible. Accurate fault location thus saves the time and efforts of the maintenance crew [6]. Timely repair will help in restoring the power to the end users and preventing revenue loss for the utilities. Unlike the generators and transformers which are housed in an enclosure and reside in a substation, transmission lines are subjected to tough weather conditions as they run through all kinds of terrain to transfer power. Hence, most of the faults in the power system occur on transmission lines. In today's practice, fault location in transmission line is an important research area in power system protection.

1.2 HV Transmisison Network and Series Capacitor Compensation

Transmission system is an interconnected network of high voltage conductors. Once the power is generated, it gets transmitted to end users over transmission lines. But with the ever increasing power consumption, the stress on the existing infrastructure to transmit more power is growing. Since there is a limit on the amount of power that can be transferred over an existing

line (governed by the line impedance and stability limit of the transmission line), one cannot transfer more than the maximum amount of power on an existing line as this might push the network into unstable region in addition to increase in the line losses. Increase in losses can cause overheating which may result in sagging of conductor more than a specified limit thereby causing severe transmission line faults as the sagged conductor can touch a part of tree or vegetation or other lines. Therefore, in order to transfer more power, utilities need to build new sets of lines to enhance the transmission capacity. But, constructing a new line is not an easy option. It is expensive and requires a lot of time, resources and land. Often projects get stuck as the utilities do not get permission from different authorities, or right of way is not available. Another option to transfer more power which is relatively cheaper, less cumbersome and less time consuming is to enhance the transmission capacity of existing transmission lines.

One way to enhance the maximum power transfer capacity is to compensate for the line inductance. For compensating the line inductance, a capacitor is placed in series with the transmission line. These lines are called series capacitor compensated transmission lines. Series compensation not only helps in increasing power transfer capability [7]-[8] but it also helps in reduction of losses, improving transient stability, voltage drop and better load division among parallel transmission lines [9]. Furthermore, the cost of series compensation is low and the lead time is relatively short as well [10]. The percentage of the line inductance which is compensated by the capacitor is called the degree of compensation. The compensation level generally ranges from 25% to 75% of transmission line inductance [11]. Different devices are available for series compensation for example, thyristor controlled series capacitor (TCSC), static synchronous series capacitor (SSSC), thyristor switched series capacitor (TSSC) and fixed series capacitor (FSC) [3]. Except fixed series capacitor, all the other devices are flexible AC transmission system (FACTS) based. The main advantage of using FACTS based devices is their fast and dynamic control. For example, TCSC provides the ability to the user to vary the compensation level according to the requirement [12]. Also, there are several other advantages associated with these devices one of which is the enhanced level of protection of series capac-

itor through faster bypass. Selection of device depends upon the requirement of the utilities and the budget available as all these advantages have a cost associated with them, i.e., cost of FACTS devices.

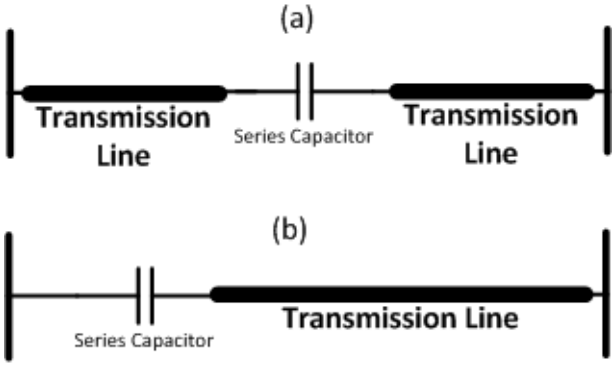

Figure 1.1: (a): Mid-Line Compensation (b): Line-End Compensation

If the system does not require a dynamic control, the conventional fixed series capacitors can serve the purpose. FSCs are the most cost effective option for compensating the line inductance. As shown in Figure 1.1, the series capacitors can either be installed in the middle of the line with full compensation or in most of the cases, the full compensation is done at one end of the transmission line. The placement of a series capacitor unit is governed by installation limitation and system requirements. Both the locations have their own merits and demerits as discussed below:

1. **Mid-Line compensation**: The main advantage is the optimized voltage control and higher effectiveness. However, it is expensive as the utilities have to build a dedicated substation in the middle of the transmission line. Moreover maintenance of the site is not easy. Any data with respect to series capacitor protection unit is not available locally if high speed communication is not available.

2. **Line-End compensation**: This presents a cost effective solution as the utilities do not have to build a dedicated substation, and maintenance of the site is much easier. Any information regarding series capacitor protection unit can easily be accessed from the

control room located at the ends.

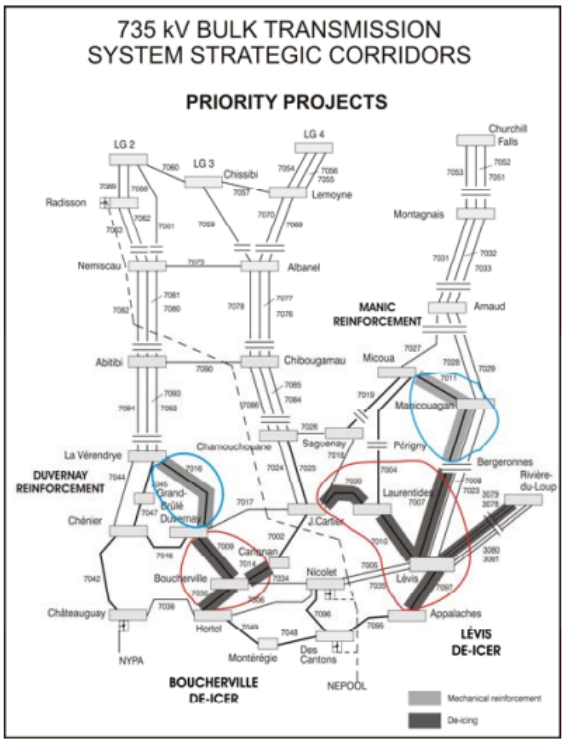

Figure 1.2: HydroQuebec's Network of Series Compensated Lines [13]

As an example of a system with series compensated transmission lines, Figure 1.2 represents the Hydro Quebec's network. It consists of 11422 km of 735 kV lines of which about 8000 km are series compensated. This network shows different type of compensation discussed previously, i.e., the mid line and end line compensation [13].

1.2.1 Fault on a Series Compensated Line and Fault Location

In the event of any fault on a transmission line or on any equipment, a chain of events takes place. First, the protective relays at both line ends detect the fault and then they send trip signals to their dedicated circuit breakers for isolating the faulted line. If the fault is temporary, the line protection system makes an attempt to reclose the circuit breaker and bring the isolated line back to the network. But if the fault is permanent, operators need to physically check the

extent of damage and clear the fault manually. Power to the affected customers, if possible, is transferred through the other paths till the line is restored. Power outage time can be reduced if the relay is able to locate the fault with more precision. Once the fault is pinpointed and if it is a permanent fault, maintenance crew will be sent to clear the fault and bring the isolated section back in service. However, for finding the exact location of the fault, it is important to have an accurate fault location algorithm.

Process of fault location in the series compensated transmission lines is not as straight forward as in the uncompensated lines [14]. Presence of the series capacitor unit and its over-voltage protection devices in the fault loop makes the task challenging Figure 3.1. Series capacitor is protected by a non-linear resistor called metal oxide varistor (MOV) which is placed in parallel with the capacitor [16]. Resistance offered by MOV is a function of the line current [17]. Therefore, in the event of any fault, MOV offers an impedance which depends on the fault current and is varying. Hence, estimation of voltage drop across MOV becomes challenging. Therefore, most of the fault location algorithms presented so far assumes the location of the MOV in the middle of the line (being the worst case scenario).

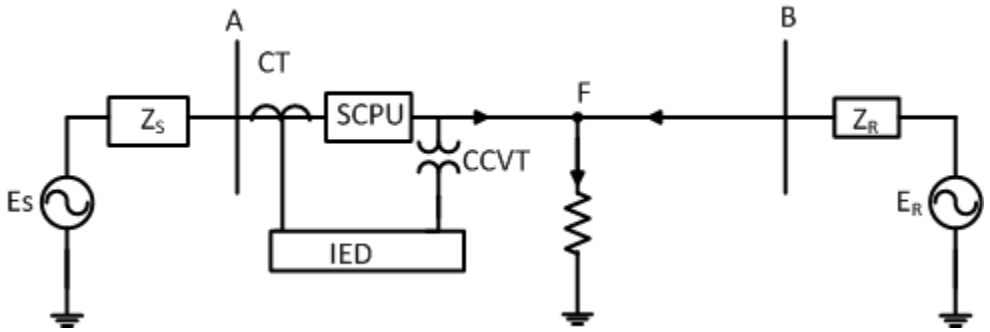

Figure 1.3: Location of CCVT on line side or right hand side of SCPU

As discussed earlier, the series capacitor can be placed either in the middle or at the line end. If the series capacitor is located at the line end, there is a possibility that the potential transformer is located on the line side of the SCPU (Series capacitor protection unit) (Figure 1.3). In such a case, voltage drop across MOV is not required (as the voltage is available

at a point after SCPU) and fault location algorithm for uncompensated transmission lines can be used to locate the fault at point F. However, in actual practice the potential transformers can also be located on the bus side of SCPU (Figure 1.4). If the potential transformer is on the bus side of the SCPU or if the SCPU is located in the middle of the line, then the fault location algorithm for uncompensated lines can not be used. This is so because that would now require the knowledge of voltage drop across MOV which is a challenging task because of its inter-dependence to the fault current. Since the focus of the research is to develop an accurate phasor estimation technique for series compensated lines, location of CCVT is considered to be on line side of the SCPU. This has enabled the author to use the fault location algorithm for uncompensated lines which are relatively more established and have less sources of error.

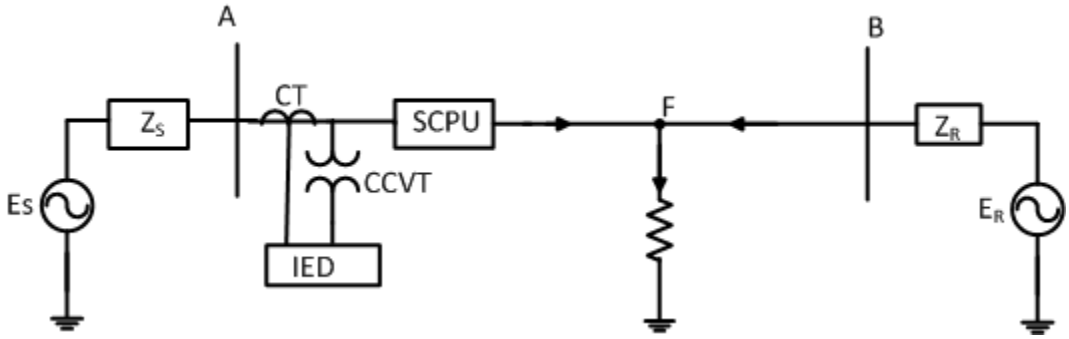

Figure 1.4: Location of CCVT on bus side or left hand side of SCPU

Apart from MOV, there is a spark-gap and a bypass breaker which provide protection for the MOV. The way these components operate, defines the properties and components of the fault current [16]. One of the main difference in the components of the fault currents of series compensated and uncompensated lines is the presence of sub-synchronous frequency components in both voltage and current signals [14]. When fault happens on a series compensated line, the capacitor and line inductor exchange energy. This phenomenon gives rise to the frequency components lower than the fundamental frequency known as sub-synchronous frequency components (SSFCs). Unlike CT and CCVT transients, these SSFCs last for longer duration, sometimes for more than 4-5 cycles. It will be shown in the later part of the research

that the presence of SSFCs adversely affects the performance of conventional DFT-based phasor estimation techniques and thereby fault location accuracy.

As discussed in the previous section, fault location in series compensated lines is not easy. Therefore, researchers have proposed dedicated fault location algorithms for series compensated lines. Fault location algorithms found in literature can be broadly categorized as: 1) instantaneous-time-based and 2) phasor-based. Instantaneous-time-based techniques such as the ones proposed in [15] [16] and [21], utilize instantaneous values of measured voltage and current signals to determine the fault location. These techniques are not affected by the presence of sub-synchronous frequency components. However, the error introduced by voltage and current transformers or any unseen error can significantly reduce the accuracy of the fault location. Further, in these techniques, line zero sequence parameters have been used as part of the fault location algorithm. Since line zero sequence parameters cannot be estimated accurately (because of its dependence on soil resistivity), fault location algorithm based on instantaneous values becomes very susceptible to error.

In case of phasor-based fault location algorithms, only two techniques have been proposed in the literature. In the first technique proposed in [23], an equivalent model of the series capacitor and MOV is considered to be known and the voltage drop across the series capacitor is compensated. In this case, the same philosophy of fault location used for uncompensated line is applicable. However, accuracy of the equivalent series capacitor and MOV model directly affects the accuracy of the fault location. This is disadvantageous as most of the time the accurate model is not available. Although, line zero sequence parameters are not required as part of the fault location algorithm.

In the second technique proposed in [24] and [25], series capacitor and MOV parameters are not utilized as part of the fault location algorithm. In this method, current measurements at both line ends and voltage measurements at the line section without series capacitor are used to determine the fault location. Even though phasors are used in this method, it is not possible to avoid using zero sequence parameters. Therefore, for the sake of simplicity and to reduce

the sources of error from the fault location algorithm so as to accurately analyze the proposed phasor estimation technique, author has assumed location of voltage measurement transducers at the line sides.

1.3 Issues and Proposed Solution

As discussed previously, accuracy of phasor-based algorithms depend upon the accuracy of measured phasors. Presence of DDOCs and SSFCs in the fault current signal is bound to affect the phasor-based protection techniques. Discrete Fourier transform (DFT) is one of the most commonly used algorithm in numerical protective relays to estimate the phasors of the voltage and current signals based on which relays make necessary decisions. Pre-filtering of current signal prior to phasor estimation is mostly employed in practice to reduce the adverse effect of the presence of DDOCs in the current signal. The filter used for this purpose, known as Mimic-filter, is a high-pass or band-pass filter which can effectively attenuate DDOCs [31]. A phasor estimation based on Cosine algorithm is proposed in [32]. This method is as effective as the use of mimic filter and results in transient response time of 1+1/4 cycles. Other techniques are also proposed in literature which estimate the DDOC and removes it to obtain an accurate phasor value [33]-[34]. Paper referred in [35] represents a real-time technique which compensates for decaying DC. This technique uses the fact that integrating the signal over a power system cycle eliminates the power frequency components and its harmonics and leaves behind the DC content of the signal. Authors have derived the relationship to estimate the phasor component due to decaying DC and computed it on real time basis. The signal phasor's real and imaginary part are then added to the respective real and imaginary part of decaying DC which has a negative effect on the signal. Since the signal is averaged, this method is very effective even if noise and harmonics are present.

However, all of these techniques are most effective when line is uncompensated and SSFCs are not present in the current signal. To deal with SSFCs present in the fault currents of a

series compensated transmission line, a reiterative technique is proposed in [36] to damp the DDOCs and SSFCs present in the fault current. This technique employs use of a short-window DFT-based mimic filter to damp the DDOCs and SSFCs. At each iteration, the damped signal is reconstructed and if the damping is not sufficient, the reconstructed signal is fed back to the same process for further damping until a sufficient amount of damping is achieved. The accuracy of the algorithm is dependent upon the window length selected, signal to noise ratio, and number of iterations performed. Therefore, a compromise has to be made between filter response time and accuracy. This method is proposed for online phasor estimation applications, since it is fast but at the same time it is less accurate. This makes it suitable for high speed protection but not for fault location.

A Fourier filter algorithm is proposed in [37] to estimate fundamental frequency component of current signal in series compensated transmission. The proposed algorithm is based on the hypothesis that the fault-induced transient responses for series compensated transmission lines consist of either three DDOCs or one DDOC and one SSFC depending upon the fault resistance. However, this may not be always a correct assumption for all fault types and system configurations. This technique is also proposed for online phasor estimation which is fast but less accurate. The proposed algorithm is very sensitive to noise and will show significant error in case there is very small noise or distortion in the measured signals.

As proposed in [36] and [37], with a short data window, it is possible to damp SSFCs and DDOCs for online applications but it is not possible to effectively eliminate them for precise fault location. In addition, both techniques are very sensitive to measurement noises. In order to achieve a higher accuracy, effective removal of the transient components from the fault current signal is essential. Hence, the use of longer data window which includes the entire fault data from the fault inception to the breaker interruption and intensive computation is proposed in this research so as to fully identify the characteristics of the transient components of fault current signal and then compensate them to accurately estimate the fault current and voltage phasors. The proposed technique is therefore suitable for offline fault location methods. Based

on the literature review performed by the author, no prior study has been done to completely remove the SSFCs or multiple SSFCs and perform accurate offline phasor estimation.

From the literature study, it has been concluded that it is impossible to completely remove these SSFCs from the fundamental signal unless their characteristics are known, i.e., magnitude, angle, decaying constant and frequency of oscillations. To remove these SSFCs from the fault current so as to have steady-state phasors, a new technique which is termed as Prony-DFT is proposed. The technique first uses an averaging filter to remove the fundamental and its integer harmonics from the fault current/voltage signals. The averaged signal thus obtained contains the parameters of the transient signal only. The parameters of the averaged transient signal are then obtained using Prony analysis. Prony [38] is used to identify the different mode and corresponding parameters present in the averaged signal. Using these parameters, the averaged signal is reconstructed and is compared with the original averaged signal. Using the parameters of the best fitted averaged signal, the original transient signal is reconstructed using the mathematical relationship derived in Section 3.4.1. The transient signal thus obtained is subtracted from the original fault current/voltage signal to obtain the fundamental signal. The fundamental signal thus obtained is used for performing the phasor estimation using conventional one-cycle DFT algorithm. However, the proposed technique is only applicable for offline applications as it requires 3-4 cycles of fault current data.

1.4 Research Objectives

The main objective of this research work is to develop an accurate and effective offline phasor estimation algorithm for fault location in series compensated line, which effectively removes the sub-synchronous frequency components arising due to the interaction between the line inductance and the series capacitor during faults. This research work is carried out in four stages:

1. Study of series compensated transmission lines and behavior of capacitor's overvoltage

protection unit.

2. Development of the offline phasor estimation algorithm.

3. Performance evaluation of the proposed technique using a theoretical signal.

4. Performance evaluation of the proposed technique using PSCAD simulations and fault location.

1.5 Contributions

This research study has resulted in the following key contributions:

1. A new offline phasor estimation technique is proposed which can accurately estimate voltage and current phasors of series compensated lines. The proposed algorithm is not sensitive to the presence of noise and harmonics.

2. Techniques proposed earlier in the literature have been tested only for an assumed theoretical signal. In this study, the combination of PSCAD simulation and fault location in MATLAB is proposed to further evaluate the performance of the proposed technique. Since the phasor values for simulated PSCAD signal are unknown, fault location is used as a mean to determine the accuracy of the proposed method. This method is more effective as it also considers the non-linearity of the MOV and its resultant dynamic impedance.

1.6 Thesis Outline

This thesis is organized in five chapters: In Chapter 1, an introduction to the research is presented along with the importance of the research to the area of power system protection. In Chapter 2, fundamentals of phasor estimation and its significance in power system relaying application are discussed. Phasor estimation based on DFT is presented. In the later part of the

chapter, the impact of SSFCs and other transient components on the accuracy of DFT-based phasor estimation technique is discussed.

In Chapter 3, series capacitor's overvoltage protection unit and its various components are discussed in detail. Problem of sub-synchronous frequency components associated with series compensated lines and lines adjacent to them has also been defined in this chapter. The later part of the chapter also discusses the proposed Prony-DFT based technique for accurate phasor estimation of fault current signal consisting of SSFCs and DDOCs. This chapter also includes the theory behind prony analysis and the analytical analysis required for the proposed technique. Further, the test results of the proposed technique on a theoretical signal are presented to establish the accuracy of the proposed technique.

In Chapter 4, the error comparison of the proposed method for various fault scenarios simulated in PSCAD on a 500 kV series compensated transmission lines is presented with respect to 4-cycles Mimic-DFT algorithm. Finally, in Chapter 5, summary of the complete research work is presented. Contributions and conclusion of the research work are presented. This chapter also discusses scope for future research work.

1.7 Summary

An introduction to the research and its importance to the area of power system relaying was presented in this chapter. Then the issues associated with the phasor estimation in series compensated lines and proposed solution were discussed. Key contributions of the research work were highlighted. The research objectives and a detailed outline of the organization of the thesis were also provided in this chapter.

Chapter 2

Phasor Estimation

2.1 Introduction

This chapter introduces the available tools and techniques which are used by the industry for calculating the accurate phasors for protection purpose. Current and voltage phasors of the fundamental frequency are required, for protection and fault location algorithms. These phasors reside inside the numerical relays. Accuracy of phasors is important as incorrect phasor measurement may impact the accuracy of protection and phasor-based fault location algorithms.

In the healthy condition, the line current and voltage signals in the power system are purely sinusoidal with fundamental frequency component. Therefore, conventional 1-cycle DFT discussed in Section 2.3.1 can be used for calculating the phasors as it also suppresses noise and harmonics substantially. But, in the event of any fault on the power system, the fault current and voltage signals gets corrupted with additional transient components. The fault current gets contaminated by DDOCs, harmonics and noise. The fault current also has an additional component, known as sub-synchronous frequency components (SSFCs) in case of series compensated lines. Similarly, the potential transformer used for voltage measurement suffers from CCVT transients discussed in Section 2.4.3 of this chapter. Thus, the fault signals may have multiple frequencies present apart from the frequency of interest and use of conventional DFT

will result in erroneous phasors. Phasor error will not only impact the protection algorithm but also the fault location algorithms. Presence of decaying DC is not as harmful as SSFCs for phasor estimation and fault location algorithms. As compared to SSFCs, decaying DC component does not last longer and conventional phasor estimation techniques can be used. The uncompensated lines (SSFCs are not present) use the last cycle of fault data to estimate the fault location. But when it comes to series compensated lines, the SSFCs do not damp quickly and last longer than the fault clearing time. As discussed in Chapter 1, presence of SSFCs impact the accuracy of phasor estimation and hence the fault location. The next section defines the phasor and windowing process.

2.2 Phasor

The process of extraction of signal parameter (amplitude and phase angle) with respect to power system frequency is referred to as phasor estimation [2]. Any sinusoidal signal $x(t)$ can be represented by its phasor form $X{=}A\angle\theta$. A Phasor form contains the information about the signal amplitude(A) and phase angle(θ). For example, consider the following signal:

$$x(t) = A\cos(\omega t + \theta) \tag{2.1}$$

Equation 2.1 can be rewritten as

$$x(t) = A.\Re(e^{j(\omega t+\theta)}) \tag{2.2}$$

$$X = Ae^{j\theta} = A\angle\theta \tag{2.3}$$

The phasor for the signal in (2.1) can be represented by (2.3) provided that the signal amplitude (A), phase angle (θ) and angular frequency(ω) are time invariant. For example, in case of a series RL circuit supplied by a sinusoidal source, the differential equation can be expressed in time domain as

$$v(t) = Ri(t) + L\frac{di(t)}{dt} = V_m\cos(\omega t) \tag{2.4}$$

If we are only interested in steady-state response of the system, the differential equation can be converted into an algebraic equation by applying phasor definition to (2.4). In this case, circuit variables can be calculated simply based on other variables.

$$V = RI + j\omega LI \text{ or } I = \frac{V}{R + j\omega L} \text{ or } Z = R + j\omega L = \frac{V}{I} \tag{2.5}$$

where V is the voltage phasor equals to $V_m\angle\theta_v$; I is the current phasor equals to $I_m\angle\theta_i$ and Z is the circuit impedance.

Different techniques are available for estimating the phasors. Before discussing them it is very important to understand the concept of 'window' described in the next section.

2.2.1 Windowing

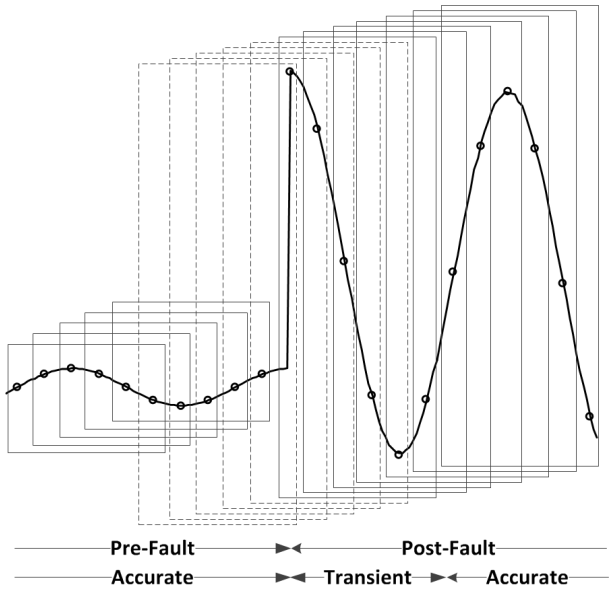

Figure 2.1: Representation of Data Samples in a Window

As discussed in the previous section, power system's measured voltage and current waveforms can be distorted by harmonics and noise; therefore, estimating accurate phasors for a pure power system frequency signal requires extracting of the phasor of fundamental frequency

phasor component by either removing or suppressing the unwanted frequencies present in the signal. For defining the phasor, it has been assumed that the signal is time invariant. However, in practical power system it is not possible to have constant signal parameters. Therefore, the phasor estimation is done only for a short span of time which is often termed as phasor estimation for a window (refer Figure 2.1).This short span is generally a power system cycle which is equal to 16.67 ms for a 60 Hz system. It is assumed that during this period, the signal parameters, i.e., magnitude (A), phase (θ) and angular frequency (ω) are constant. The data window is constantly updated with new samples, thereby discarding the previous samples. Thus, phasor estimation is carried out with every new sample in order to estimate accurate phasor. However, the accuracy of phasors depend upon the accuracy of samples. In the event of any disturbance or fault, these samples undergo a transition stage which includes samples from both pre-fault and post-fault instances as shown in Figure 2.1 by the windows with dashed lines. Therefore, in the event of any fault, there is always a transition time equal to the size of phasor estimation window, when the estimated phasor value is not accurate.

2.3 Phasor Estimation Techniques

As stated earlier, the power system signals, i.e., voltages and currents are often corrupted with noise, harmonics, decaying DC during a disturbance or fault on the system. In order to estimate the accurate fundamental phasor, it is necessary to get rid of these extra components contaminating the fundamental signal and extract only the fundamental frequency component. There are different methods for estimating the phasors, e.g., Discrete Fourier transform (DFT), Cosine-based, Mimic-DFT. The next section focuses on 1-cycle and 4-cycle DFT. Cosine-based and Mimic-DFT are discussed in Section 2.5.

2.3.1 Discrete Fourier Transform (DFT) Algorithm

DFT is the most commonly and widely used technique when it comes to protection relay environment. Extraction of a particular frequency component is done using Fourier transform. However, in relay environment, sampled data at discrete time step is available for processing; therefore, the Fourier-transform calculation is also done in discrete environment and is termed as Discrete Fourier Transform or DFT. Before defining DFT, let us first understand Discrete-Time Fourier Transform (DTFT).

$$X(j\omega) = \sum_{n=-\infty}^{n=+\infty} (x[n])e^{-j\omega n} \tag{2.6}$$

where ω is $2\pi f/f_s$.

Equation (2.6) shows the mathematical representation of Fourier transform for a sampled data signal. Generally a window of sampled data as discussed in the beginning of the chapter is taken to perform Fourier analysis. Therefore, a truncated version of the above is used for practical purposes. The truncated DTFT is given by (2.7).

$$X_N(j\omega) = \sum_{n=0}^{N-1} (x[n])e^{-j\omega n} \tag{2.7}$$

This truncation is equivalent to multiplying by a rectangular window of data length 'N' which results in broadening of spectral peaks and spectral leakage, i.e., presence of side lobes.

Let us now define a full-cyle (1-cycle) DFT where the window length is selected as $N = f_s/f_n$ and the frequency of interest is f_n. In power system protection, DFT is essentially the same as DTFT, evaluated at N equally spaced frequencies between 0 and 2π.

$$X = \frac{2}{N} \sum_{n=0}^{N-1} x[n]e^{-j2\pi \frac{f_n}{f_s} n} \tag{2.8}$$

Knowing $N = f_s/f_n$

$$X = \frac{2}{N} \sum_{n=0}^{N-1} x[n]e^{-j2\pi \frac{f_n}{Nf_n} n} \tag{2.9}$$

$$X = \frac{2}{N}\sum_{n=0}^{N-1} x[n]e^{-j2\pi\frac{n}{N}} \tag{2.10}$$

For a pure sinusoidal signal such as $x(t) = A\cos(2\pi f_n t + \theta)$,

$$x[n] = x(\frac{n}{f_s}) = A\cos(2\pi\frac{n}{N} + \theta) \tag{2.11}$$

Equating x[n] into (2.10) we get (2.12)

$$X = \frac{2}{N}\sum_{n=0}^{N-1} A\cos(2\pi\frac{n}{N} + \theta)e^{-j2\pi\frac{n}{N}} \tag{2.12}$$

Using Euler's identity (2.12) can be rewritten as (2.13).

$$X = \frac{1}{N}\sum_{n=0}^{N-1} A\left(e^{j(2\pi\frac{n}{N}+\theta)} + e^{-j(2\pi\frac{n}{N}+\theta)}\right)e^{-j2\pi\frac{n}{N}} \tag{2.13}$$

Simplifying (2.13) results into (2.14), which can further be simplified into (2.15).

$$X = \frac{1}{N}\sum_{n=0}^{N-1} A\left(e^{j\theta} + e^{-j(4\pi\frac{n}{N}+\theta)}\right) \tag{2.14}$$

$$X = Ae^{j\theta} + \frac{Ae^{-j\theta}}{N}\sum_{n=0}^{N-1} e^{-j4\pi\frac{n}{N}} \tag{2.15}$$

Assuming $r = e^{-j4\pi\frac{1}{N}}$ of a Geometric progression (G.P.) series, the sum of a finite G.P. is given by (2.16).

$$\sum_{n=0}^{N-1} r^n = 1 + r + r^2 + \cdots + r^{N-1} = \frac{1-r^N}{1-r} \tag{2.16}$$

Simplifying, (2.15) using (2.16) we get

$$\sum_{n=0}^{N-1} e^{-j4\pi\frac{n}{N}} = \frac{1-e^{-j4\pi\frac{N}{N}}}{1-e^{-j4\pi\frac{1}{N}}} = 0 \tag{2.17}$$

Therefore,

$$X(f_n) = Ae^{j\theta} = A\angle\theta \tag{2.18}$$

Equation (2.18) represents phasor for any sinusoidal signal with the fundamental frequency of f_n. For estimating the phasor of fundamental frequency f_n, equation (2.12) can be written as

$$X(f_n) = \frac{2}{N}\sum_{n=0}^{N-1} A\cos(2\pi\frac{n}{N} + \theta)e^{-j2\pi\frac{n}{N}} \tag{2.19}$$

Using (2.11) and equating into (2.19), we get (2.20)

$$X(f_n) = \frac{2}{N}\sum_{n=0}^{N-1} x[n]e^{-j2\pi\frac{n}{N}} = \underbrace{\frac{2}{N}\sum_{n=0}^{N-1} x[n]\cos 2\pi\frac{n}{N}}_{X_r\text{:Real Filter}} + j\underbrace{\frac{2}{N}\sum_{n=0}^{N-1} -x[n]\sin 2\pi\frac{n}{N}}_{X_i\text{:Imaginary Filter}} \tag{2.20}$$

$$X_r = \text{Real Filter} = \frac{2}{N}\cos(\frac{2\pi}{N}n) \tag{2.21}$$

$$X_i = \text{Imaginary Filter} = -\frac{2}{N}\sin(\frac{2\pi}{N}n) \tag{2.22}$$

where $n = 0, ..., N-1$. Phasor's amplitude and angle can be computed by (2.23) and (2.24), respectively.

$$A = \sqrt{(X_r)^2 + (X_i)^2} \tag{2.23}$$

$$\angle\theta = \arg(X_r + jX_i) \tag{2.24}$$

Figure 2.2 shows the real and imaginary filters represented by (2.21) and (2.22).

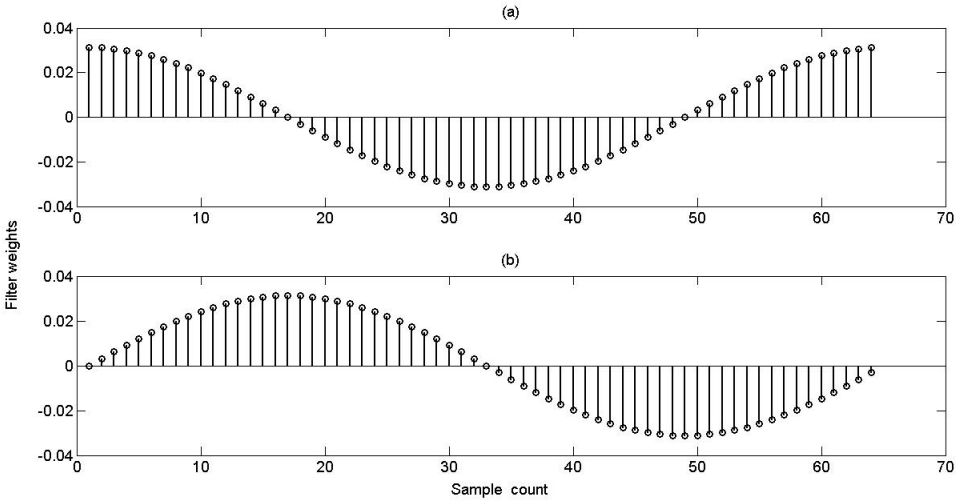

Figure 2.2: (a): Real DFT Filter (b): Imaginary DFT Filter

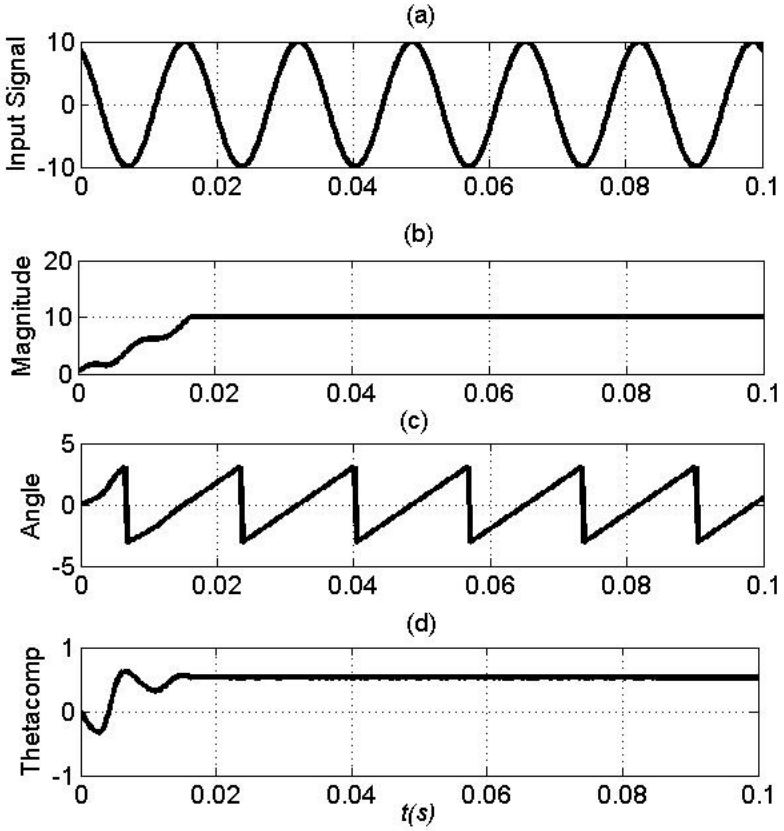

Figure 2.3: (a): Input signal (b): magnitude (c): rotating angle (d): compensated angle

$$x(t) = 10 * cos(2\pi * 60 * t + \pi/6) \tag{2.25}$$

Equation (2.25) represents a pure sinusoidal 60 Hz signal. Figure 2.3 (a) shows the input signal. When input signal is passed through DFT filters, it returns the magnitude and angle as represented by Figure 2.3 (b) and (c). It can be observed from time response that DFT has a transient time of 1-cycle. Also, it gives a constant phasor magnitude output for a pure 60 Hz signal once the transient time is over. It can also be observed from the angle that it is constantly varying. As the window of samples are updated upon acquisition of a new sample, the inherent phase shift $2\pi/N$ occurs. Because of this phenomenon, the phasor obtained using this method is called rotatory phasor. It is possible to compensate this angle to obtain a consistent angle. Figure 2.3 (d) shows the compensated angle. However, in most of the relaying application, there is no need for such compensation as all the estimated phasors rotate with the same pace and our interest is only the angle difference rather than the absolute angle.

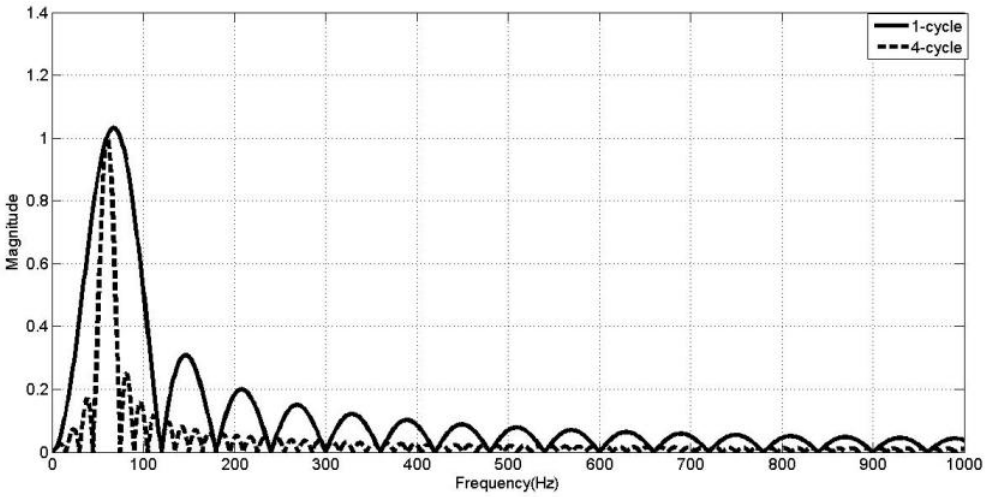

Figure 2.4: Frequency Response of 1-Cycle and 4-Cycles DFT's Real Filters

In Figure 2.4 and Figure 2.5, frequency response of 1-cycle and 4-cycles DFTs' real and imaginary filters is shown. It can be observed from the real and imaginary filter's frequency response (magnitude) of 1-cycle DFT that it removes DC and integer harmonics, suppresses

noise, non-integer harmonics and sub-synchronous frequency components. These features of 1-cycle DFT are compared with 4-cycles DFT in the next section.

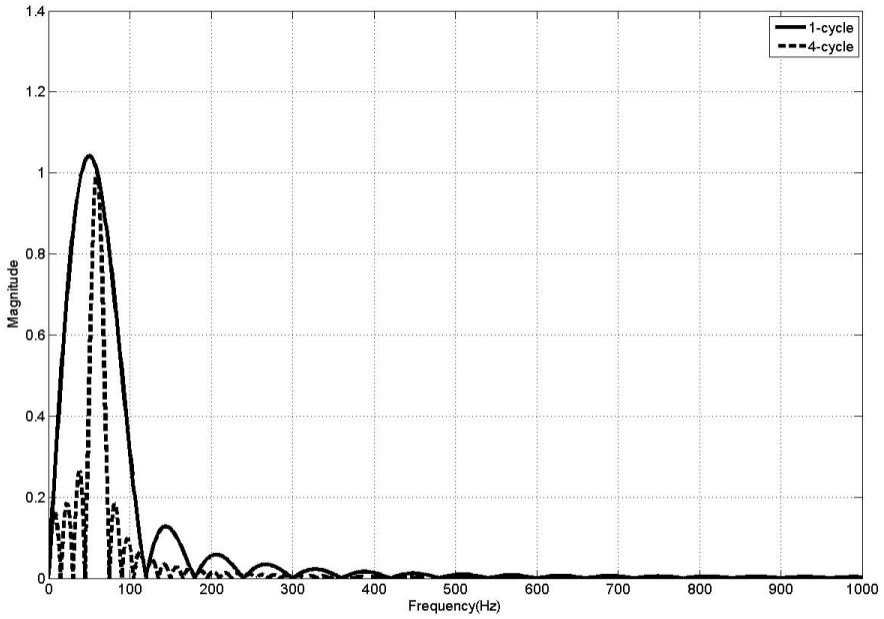

Figure 2.5: Frequency Response of 1-Cycle and 4-Cycles DFT's Imaginary Filters

2.3.2 4-Cycles Based Discrete Fourier Transform (DFT) Algorithm

Theoretically 4-cycle DFT is same as 1-cycle DFT. The only difference is that for 4-cycles DFT the window size is $N = 4\frac{f_s}{f_n}$, which is four times to that of the 1-cycle DFT. The reason for discussing the 4-cycle DFT is that it gives the best performance out of all the available techniques and it is fair to compare the result of the proposed method with it. Figure 2.4 and Figure 2.5 represents the frequency response of real and imaginary filters of a 4-cycles based DFT. It can be observed from the response that as compared to 1-cycle DFT it does a good job in suppressing the lower frequency components, removing DC and significantly attenuating the high frequency components. However, it does not fully remove them.

From Figure 2.6, which shows the transient response time for a pure 60 Hz signal, it may

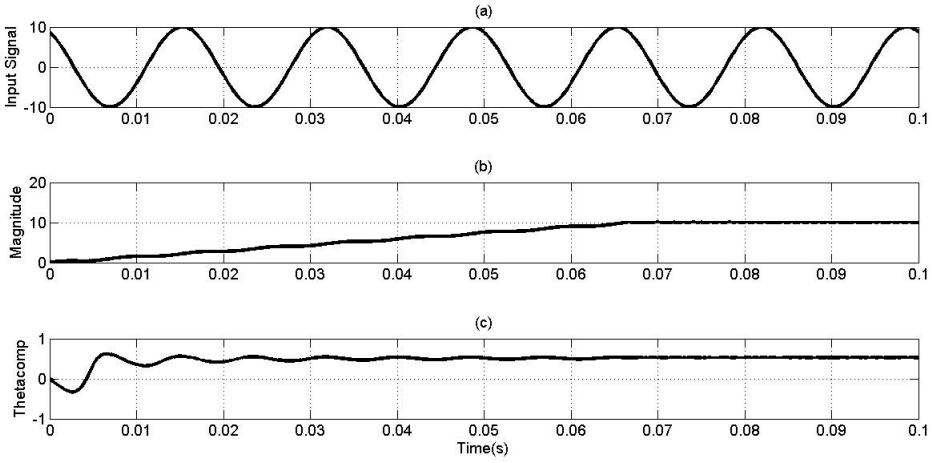

Figure 2.6: Transient response of 4-cycles DFT for a pure 60 Hz signal

be noted that the transient response time is 4 cycles for a 4-cycles DFT-based algorithm.

To sum up, 4-cycles DFT has superior performance compared to the conventional 1-cycle DFT algorithm. As observed from the frequency response, 4-cycles DFT considerably attenuates the noise and harmonics and lower frequency components compared to 1-cycle DFT. However, the disadvantages attached with 4-cycles DFT is its slower time response compared to 1-cycle DFT.

Other unwanted components in the fault current apart from noise and harmonics are decaying DC offset components (DDOCs) and sub-synchronous frequency components (SSFCs). CCVT (Capacitive coupled voltage transformer) transients also poses challenge for estimating the voltage phasors. These unwanted signal components, their impacts on 1-cycle and 4-cycle based DFT algorithms and their mitigation strategies are discussed in the next section.

2.4 Transients Components of Fault Signals

2.4.1 Decaying DC

Whenever a fault happens on a power system, fault current during transient condition may comprise of harmonics, noise and an exponentially decaying DC component often referred as DC offset. A decaying DC offset is a non-periodic signal and has a relatively wide range of frequency spectrum with larger distribution at lower frequencies. If phasor estimation is carried out without removing or attenuating the DC offset or the unwanted low frequency components, it will give erroneous result as evident from the frequency response of the DFT filters (see Figure 2.4). The magnitude error due to the DFT-based phasor estimation can be very high and can reach up to 15.1% as reported in [31]. Although DC offset decays very fast, i.e., within few cycles, for high speed relaying applications, knowledge of accurate phasors with smallest possible time delay is essential for fast decision making by the relays. Therefore, modern numerical relays also employ algorithms for removal of decaying DC offset for correct phasor estimation. Next section discusses few of the commercially available techniques for DC removal application. Input signal given by (2.25) is now contaminated with 100% decaying DC

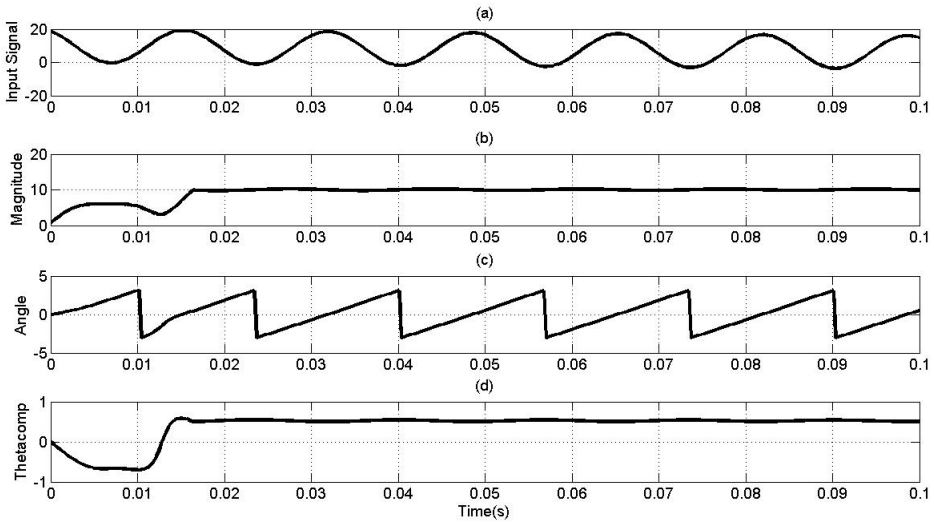

Figure 2.7: (a): Input signal with 100% decaying DC (b): magnitude phasor estimated by DFT

component with a time constant of 0.2 s, representing the worst possible case (refer Figure 2.7 (a)). It can be observed from its time response as shown in Figure 2.7 (b) that instead of getting constant phasor magnitude, the output of 1-cycle DFT is oscillatory in nature.

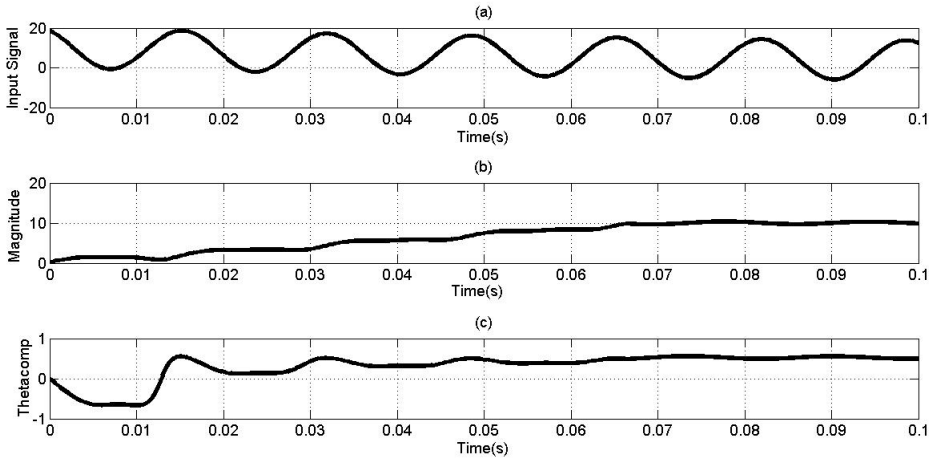

Figure 2.8: (a): Input signal with 100% decaying DC, (b): estimated magnitude by 4-cycles DFT (c): estimated compensated angle by 4-cycles DFT

Figure 2.8 (a) shows an input signal with a 100% decaying DC component and 0.1 sec time constant. Figure 2.8 (b) and (c) shows the estimated magnitude and angle phasors using 4-cycle DFT algorithm. It can be observed that even with a decay constant of 0.1 s, the output is oscillatory.

2.4.2 Sub-synchronous Frequency Components (SSFCs)

The natural frequency at which the electrical network exchanges energy with the mechanical system (turbine-generator) is known as sub-synchronous resonance condition (SSR). Series combination of line inductance L and capacitance C results in sub-synchronous frequencies in the series compensated lines given by (2.26)

$$f_o = f_n \sqrt{\frac{X_c}{X_L + X_s}} \tag{2.26}$$

where f_o is the sub-synchronous frequency component; X_c is the reactance of the series capacitor; X_s is the inductive reactance of the source; X_L is the inductive reactance of the line.

As discussed in Chapter 1, the capacitor can be located either in the middle or at the end of the line. If the series capacitor is located at the end of the line, the fault can either be located very close to the capacitor or away from the capacitor. In case of a close-in fault the fault current is very high such that the spark-gap flashes immediately (within 1 ms) and capacitor and MOV gets bypassed. In such a case there will not be any SSFCs in the fault current because capacitor is out from the fault loop. However, if the fault is located away from the series capacitor either in the middle or at the end of the line. MOV conducts to protect the capacitor from over-voltage. In this situation the fault current will contain SSFCs. The sub-synchronous frequency present in the fault signal can be estimated using (2.27).

$$f_o = f_n \sqrt{\frac{X_{ceq}}{X_{LF} + X_s}} \tag{2.27}$$

where X_{ceq} is the equivalent capacitive reactance offered by the series capacitor during MOV conduction; X_{LF} is the inductive reactance of the line to the fault point. X_c is replaced by X_{ceq} in (2.26). It is done so because when MOV conducts, the series capacitor is not in the path of the fault current for full time. Fault current partially conducts through MOV and partially through capacitor. Therefore effective capacitive reactance is different from the rated reactance of the capacitor. Also X_{ceq} will always be less than X_c.

From (2.27), it can be observed that f_o depend upon the source impedance ratio (SIR=$\frac{X_s}{X_{LF}}$) and location of the fault point. However, it can be estimated that for most of the distant faults there is high possibility that ratio of X_{ceq} and $(X_{LF} + X_s)$ is less than 1 and the system will see the sub-synchronous frequencies, the range of which will be typically (40-55) Hz.

However, if the series capacitor is in the middle, chances of flashing of spark-gap are less until the fault lasts for a longer duration. In this scenario, the fault current will contain the SSFCs.

Figure 2.9 (a) shows a 60 Hz signal (Amplitude:10 A) with a 50% 40 Hz sub-synchronous

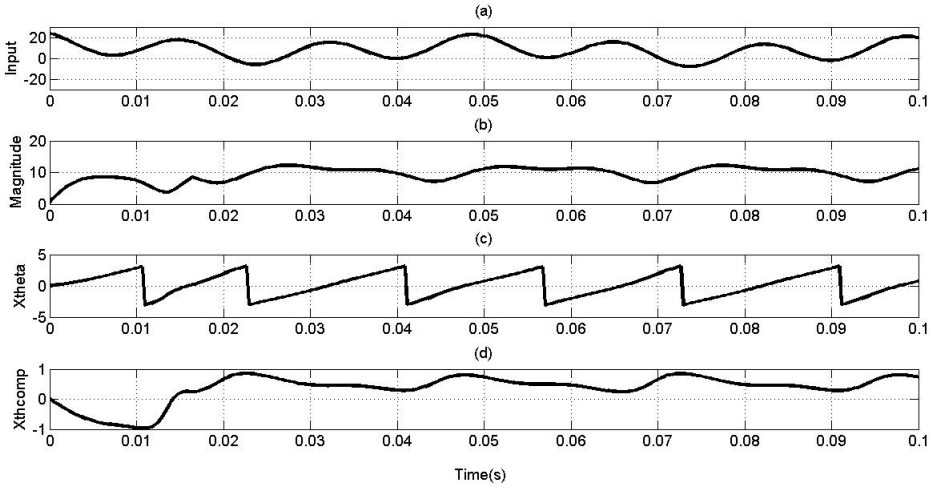

Figure 2.9: (a): 60 Hz input signal with a 40 Hz sub-synchronous component (b): magnitude phasor (c): uncompensated rotatory phasor (d): compensated angle phasor

frequency component. It can be observed from the time response of DFT in Figure 2.9 (b) that the output is oscillatory in nature. The compensated phase angle is also oscillatory (refer Figure 2.9 (d)). Therefore, it can be concluded that 1-cycle DFT does not perform well if the signal contains sub-synchronous frequencies.

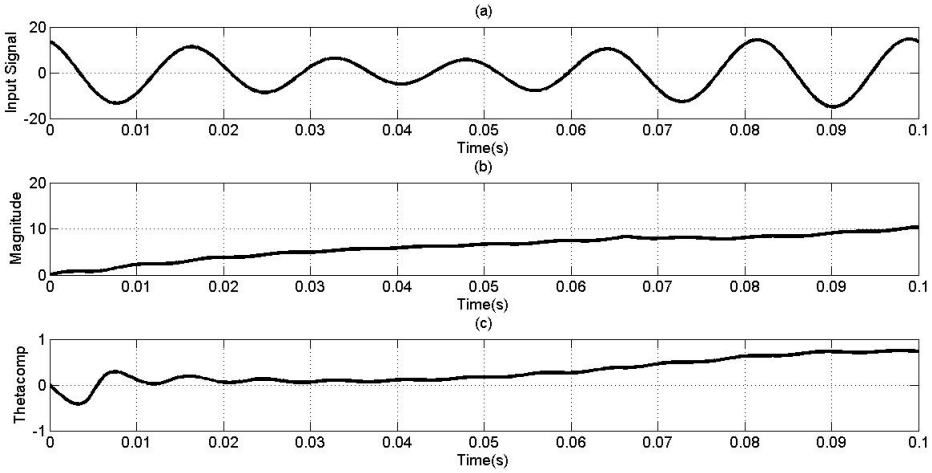

Figure 2.10: (a): Input signal with 50 Hz SSFC (b): transient response of 4-cycles DFT

Now, let us check the performance of 4-cycle DFT in the presence of SSFCs. Figure 2.10

(a) shows the input signal with a 50 Hz sub-synchronous frequency component. It can be observed that even 4-cycles DFT does not help in complete removal sub-synchronous components, since the phasors are still oscillatory.

2.4.3 CCVT Transients and Transient Performance of CCVTs

Figure 2.11 shows a typical CCVT circuit used in power system. The function of CCVT is to convert the high voltage into a lower level so that it can be used by protection, measurement and control equipment present in a substation. Another function of the CCVT is to isolate the low voltage substation network from the high voltage side.

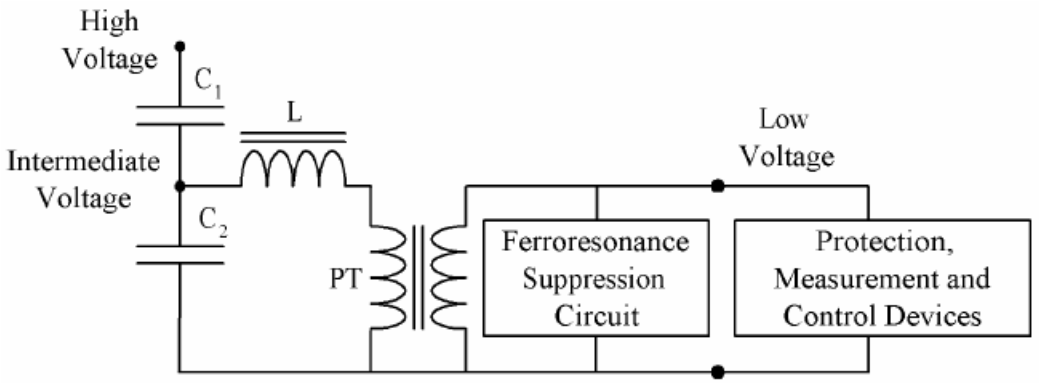

Figure 2.11: Typical CCVT circuit

The main components of a CCVT are a capacitive divider circuit consisting of C1 and C2, a series inductance L and an intermediate potential transformer (PT). The capacitive divider is a potential divider which scales down the high voltage, also known as primary voltage to some intermediate voltage level in the range of 10 kV to 20 kV. The series inductance compensates the equivalent capacitive reactance of the divider. Its inductance value is selected to obtain a reactance very close, but of the opposite sign to that of the divider at the rated fundamental frequency. The intermediate PT scales down the intermediate voltage to the normalized secondary voltage level of 110 or 120 V phase-phase required by the protection, measurement and

control equipments connected to the CCVT output. These equipments are also referred to as the CCVT burden.

The risk of ferro-resonance is present whenever a non-linear inductance, i.e., the PT, and capacitances are in the same circuit. The CCVT is protected against ferro-resonance by the ferro-resonance suppression circuit. Ferro-resonance produces overheating and can damage the intermediate PT, due to the high currents associated with ferro-resonance that saturates the core [1].

The CCVT distorts the voltage input signal received from the power system, since transients are produced on a voltage change condition. The voltage output from the CCVTs is needed by the protective relays to decide an operation. These relays typically need the amplitude and angle of the fundamental frequency component of the signal, which are extracted with the phasor estimation methods in numerical phasor form.

In order to compensate for the angle shift, the CCVT circuit is tuned. During transient conditions, the CCVT may produce secondary voltages which are significantly different from primary system voltage. During fault condition when the power frequency voltage is low, relay makes use of CCVT output for relaying applications. If a small transient component is present, it may make the relaying task difficult. The transient voltage produced by CCVT may be decaying and oscillatory mainly with sub-synchronous frequency components or a unidirectional wave (depending on the design of the CCVT, connected burden and the point of incidence on the voltage wave).

In order to avoid wrong decision making by the relays due to erroneous phasors as a result of CCVT transients, one option is to wait till the transients subside. This introduces delay in the response time, but will not affect the results. Similar to the decaying DC filter, a filter can be designed to compensate for the transients and after cleaning the voltage phasor can be estimated using DFT.

2.5 Techniques for Mitigating the Effects of Decaying DC

2.5.1 Mimic-DFT

As already seen from the MATLAB simulation results, the conventional full-cycle (1-cycle) DFT cannot effectively attenuate the lower frequency components. Thus unwanted errors in the form of overshoot and decaying oscillations results in the magnitude and angle of the estimated phasor. The total vector error will be even larger because of the phase angle error contribution. This total vector error cannot be tolerated when it comes to power system protection applications. Pre-filtering of the current signal prior to phasor estimation is mostly employed in practice to attenuate the negative effects of the decaying DC offset of the current signal. The filter used for this purpose, known as Mimic-filter, is a high-pass or band-pass filter which completely removes the decaying DC offset only when the time constant of the DC offset matches with the presumed one [31]. However, use of any pre-filter introduces a delay in response thereby slowing down the performance of the related protection algorithms. The time response of a typical Mimic-filter implemented in a commercial relay is about 1/3 of a cycle.

2.5.2 Cosine

Another technique which is being used in commercial relays for removal of decaying DC is Cosine filter [32]. It attenuates the negative effect of decaying DC offset. Unlike DFT, Cosine filter only uses the real filter of the DFT (see Figure 2.2 (a)). Essentially, the real part calculated 1/4 cycle back ($\frac{N}{4}$) gives the imaginary part. This method is as effective as the use of mimic filter and results into a transient response of 1+1/4 cycles.

2.6 Summary

This chapter first introduced the concept of phasor estimation and its application in power system protection. Importance of accurate phasor estimation was then discussed. The chap-

ter also explained the process of windowing which enables an accurate phasor estimation by calculating the phasor upon the arrival of every new sample. The chapter later discussed various methods available for phasor estimation. 1-cycle DFT and 4-cycles DFT were discussed at length. Different components of fault current were discussed and performance of each of the mentioned techniques was compared in the presence of decaying DC offset, harmonics and sub-synchronous frequency components. Cosine and Mimic-DFT were defined for filtering the decaying DC. To sum up Mimic-DFT and Cosine filter do a good job when it comes to removal of decaying DC and calculating the phasors. However, in terms of frequency response in the presence of SSFCs 4-cycle DFT performs better than conventional 1-cycle DFT, Mimic-DFT and Cosine filters.

Chapter 3

Series Compensation, Issues and Proposed Phasor Estimation Technique

3.1 Introduction

Series compensation is a proven and effective technique for increasing the transmission capacity of an existing transmission line. It is usually done on EHV long transmission lines responsible for transferring bulk power. In addition to the enhancement of transmission capacity, series compensation offers various other advantages. However, the addition of the series capacitors increases the complexity of transmission line which offers various challenges to the protection of transmission line. In series compensated transmission lines, current and voltage signals measured by the line protection system include considerable sub-synchronous frequency components (SSFCs) which are not sufficiently damped within a typical fault clearing time of line protection system. This does not allow accurate phasor estimation and thereby phasor-based fault location. This chapter presents an accurate algorithm which effectively filters out unwanted frequency components and noise to perform accurate phasor estimation for fault location in series compensated transmission lines. Mathematical analysis of the proposed method is presented and accuracy of the proposed method is established by estimating the pha-

sors of a theoretical signal using the proposed method. Results of the proposed method is then discussed with the existing techniques, i.e., Direct-Prony analysis and 4-cycle discrete Fourier transform algorithm. Before moving to the proposed algorithm, let us first talk about series capacitor's overvoltage protection system.

3.2 Series Capacitor's Overvoltage Protection System

Series capacitor along with its over-voltage protection system is often referred to as series compensating unit. In the event of any fault on transmission lines, the fault current flows through the series capacitors; as a result, the series capacitors are subjected to high stresses during the fault conditions. Therefore, protection of the capacitor from overvoltages is of paramount importance. The overvoltage protection system of the series capacitor termed as series capacitor protection unit (SCPU) is shown in Figure 3.1. SCPU contains the series capacitor and other components which provide the primary and back up protection to the series capacitor. Different components of SCPU are discussed below in detail.

1. **MOV**: MOV is a variable resistor which offers high resistance to normal load current and conducts, (i.e., offer lower resistance) during fault currents. Figure 3.2 shows the typical characteristics of an MOV. The MOV operates when a fault happens and the instantaneous voltage drop across the capacitor exceeds a predetermined level (V_{pk}).

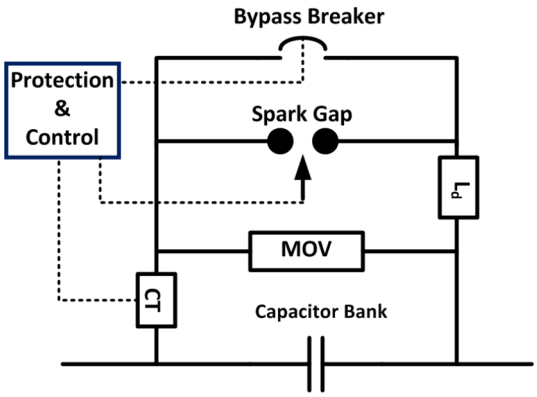

Figure 3.1: Series Capacitor Protection Unit (SCPU)

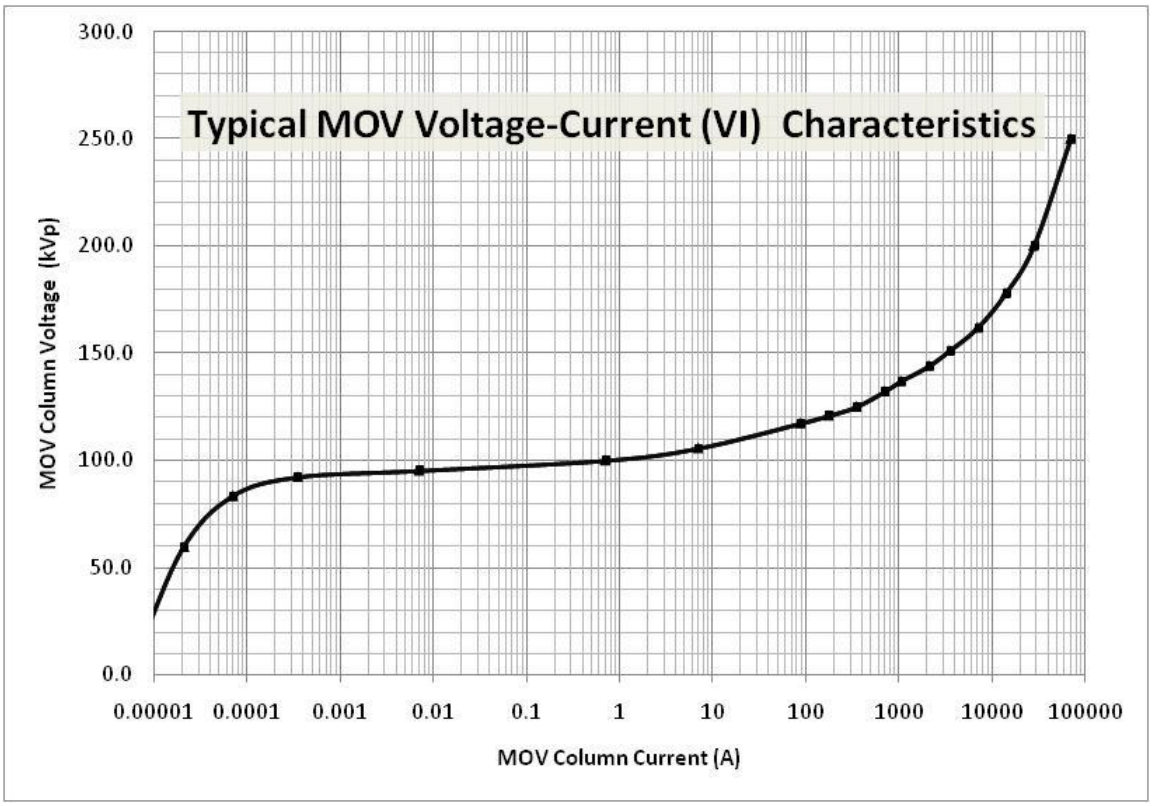

Figure 3.2: Characteristic of MOV [39]

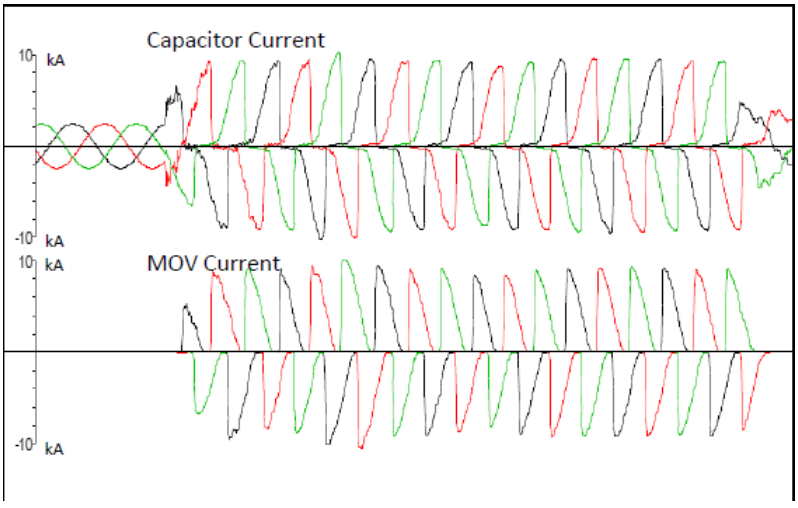

Figure 3.3: Three phases of MOV and Capacitor Current during a fault [39]

Design Parameters: An MOV is designed to maintain the capacitor voltage at or below the V_{pk}. V_{pk} is the rated protective level voltage of the capacitor and is calculated as

below:

$$V_{pk} = \sqrt{2}.I_{pr}.X_c \tag{3.1}$$

where I_{pr} is 2.0 to 2.5 of the rated bank current (I_r).

The function of the MOV is to limit the voltage across the capacitor. At the same time it also directs a large amount of fault current through it. MOVs are designed in a way so that they can carry the fault current for a maximum of 4-5 cycles. They are faster in action as they are always connected in parallel with series capacitor and need not to be triggered by a control signal. Whenever there is a fault, MOV is ready for protection. Figure 3.3 shows a fault scenario when MOV conducts. It can be observed that MOV conducts for a part of the cycle and for the rest of the part, the capacitor conducts. Hence, capacitor is always in circuit and need not to be reinserted. Being the primary protection for the capacitor, MOV itself needs to be protected. MOV is protected by means of electronic control signals and spark-gap which will be discussed later. The electronic circuitry keeps a watch on the energy accumulation in the MOV and the rate of energy absorption for its protection. Figure 3.4 shows the energy absorption by MOV for a three phase fault [39].

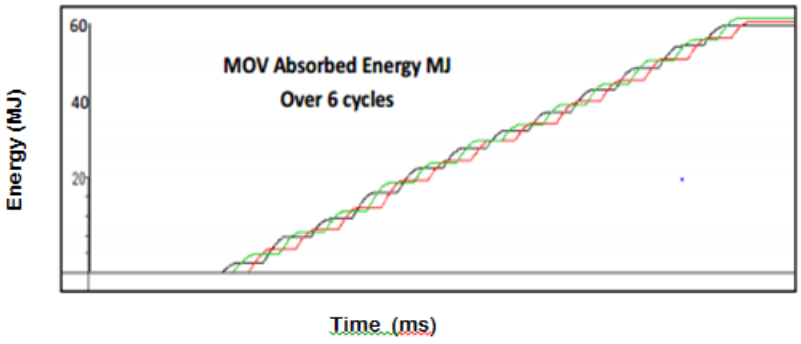

Figure 3.4: Energy absorption by MOV during a three phase fault [39]

2. **Spark-Gap**: As discussed in the previous section that the spark-gap provides primary

protection to MOV. It prevents the MOV from overheating. Spark-gap operates when the energy accumulated in the MOV column just exceeds its threshold limit. It also operates if the fault current is very high and the rate of energy accumulation is such that it will eventually touch the threshold limit. In the latter case, the spark-gap does not wait till the threshold and operates immediately. Typical operating time of a spark-gap is 1-2 ms.

3.2.1 Spark-Gap vs. MOV

In the early age of series capacitor technology, spark-gaps were used for overvoltage protection of the series capacitors [17]-[18]. Advancement of technology has replaced the spark-gaps with MOVs and new installations are mostly equipped with MOVs. MOVs are preferred over spark-gaps as they enable fast and more precise bypass and re-insertion of the series capacitor [10]. Modern SCPU is equipped with all the three components.

Spark-gaps on one hand completely shunts the capacitor during faults. Thus, the relay sees only two impedance, i.e., un-compensated or compensated. However, an MOV conducts for part of the cycle depending upon the magnitude of the fault current. Thus, in case of an MOV, the seen impedance by the relay is completely different. As referred in paper [17], this impedance can be seen as the series combination of resistance and capacitive reactance.

3. **Bypass Breaker**: Bypass breaker has got two functions. Firstly, it closes automatically in case of prolonged gap conduction. Secondly, it also allows operator to insert or bypass the series capacitor for maintenance.

3.2.2 Operation of MOV and its Impact on Fault Current

For the lower fault currents, if the voltage across the capacitor increases above its protective level, MOV conducts to protect the capacitor. However, if MOV conduction lasts longer and

the energy of the MOV reaches its threshold level, the spark-gap immediately flashes to protect the MOV. For very high fault currents, spark-gap flashes within 1 millisecond saving the MOV from unnecessary heating. Bypass breaker is employed to protect the spark-gap from prolonged conduction and also for bypassing the capacitor and MOV unit during maintenance. It should be noted that the bypass breaker operates on a three phase basis regardless of the fault type. Thus, it can be concluded that the operation of different protection components is greatly governed by the amplitude of the fault current. At the same time, the operation of SCPU impacts the fault current characteristics. For lower fault currents, MOV conduction not only protects the capacitor but its inclusion in the circuit also changes the fault loop impedance [17], which in turn changes the fault current measured by the relay. Also, MOV does not completely bypass the capacitor as a result of which there are SSFCs in the fault current and voltage. Phasor estimation in the presence of SSFCs is the main focus of this research.

If the fault current is high enough to immediately flash the spark-gap, the fault current will not have any SSFCs due to the series capacitor bypass; hence any of the conventional technique, i.e., Mimic-DFT or Cosine can be applied. For a range of fault currents, there is a possibility that the energy accumulated in MOV reaches to its threshold even before breaker interruption. If MOV bypasses before the last 1.25 cycle of breaker interruption, there is no need of the proposed technique and the last 1.25 cycle data can be applied to the Cosine or Mimic-DFT method. However, if the spark-gap flashes within the last 1.25 cycle, the data prior to spark-gap flashing should be applied to the proposed algorithm.

To sum up, the fault current measured by a relay in series compensated lines or its adjacent lines may include several SSFCs and DDOCs. In case of voltage signals, no DDOCs are expected but capacitor couple voltage transformer (CCVT) transients are added to SSFCs present in the voltage signal measured by the protection system.

As already discussed in Section 1.3, it is possible to damp SSFCs and DDOCs for online applications but it is not possible to effectively eliminate them for an accurate phasor estimation and hence a precise fault location. In order to achieve higher accuracy, an effective removal of

the transient components from the fault current signal is essential. Hence, the use of longer data window which includes the entire fault data from the fault inception to the breaker interruption is used and intensive computation is carried out in the presented work so as to fully identify the characteristics of the transient components of fault current signal and then compensate them to accurately estimate the fault current and voltage phasors. The proposed technique is therefore suitable for offline applications such as fault location. No prior study has been found in literature attempting to completely remove SSFCs from the fault signals and perform accurate offline phasor estimation. In order to carry out the identification of the components, Prony analysis has been employed in [14] for modal identification of current and voltage signals in series compensated lines which will be discussed further.

3.3 Prony Analysis

Prony analysis is a signal processing technique that extends Fourier analysis by directly estimating the frequency, damping, amplitude, and relative phase of the modal components present in a measured signal [38]. In Prony analysis, a linear parametric model is fit to a measured signal. The model is in the form of poles and residues that, collectively, constitute a modal decomposition of the signal. If the measured signal is the output of a linear dynamic system, then, under suitable conditions, the signal modes will be those of the system itself [40]. The Prony analysis is known to behave poorly when a signal is contaminated with noise [41]. It yields parameter estimates with a large bias due to its sensitivity to measurement noise. Therefore, it is only applicable when the signal to noise ratio is large. Prony analysis is also employed by [14] to find SSFCs present in the fault current signal of a series compensated line. It also mentions that the presence of SSFCs in the fault current signal introduces significant error in phasor estimation and thus phasor-based fault location.

Prony analysis is proposed in [42] and is commercially employed as reported in [43] to detect small signal oscillations. In such an application, it is important to collect sufficient data for

analysis to achieve acceptable accuracy and mitigate the adverse effect of noise. Neuro-Prony-based method is also proposed in [44] to estimate the frequency components of the faulted phase voltage and detect the arc extinction, thus enabling high speed single-phase reclosing.

3.4 Proposed Prony-DFT Technique

As mentioned earlier, Prony analysis is sensitive to noise and direct use of Prony method to analyze fault current and voltage of series compensated line results in a considerable error. This will be proved by theoretical analysis. Therefore, a new Prony-DFT technique is proposed which first uses an averaging digital filter to remove the fundamental component and its harmonics from the measured fault current/voltage signal. Then, Prony analysis is applied to the averaged transient signal to identify the most accurate parameters by using the curve-fitting. The parameters of the original transient signal are then estimated from averaged parameters by using the mathematical relationship derived in the next section. After identifying the parameters, the original transient signal is reconstructed. The reconstructed transient signal is then subtracted from the original fault signal to obtain the fundamental signal. This fundamental signal is then fed to 1-cycle DFT to estimate phasors. The process of averaging not only reduces the signal order but also attenuates the noise significantly which makes the use of Prony analysis more effective for the proposed technique.

3.4.1 Mathematical Analysis

In case of series compensated transmission lines, fault current or voltage can be represented as a combination of fundamental frequency component (I), its integer harmonics (II), transient frequency components including SSFCs, DDOCs and non-integer harmonics (III) and noise. In this section, even though the proposed technique is described only for a current signal, the same approach can be applied to a voltage signal as well. Therefore, considering all the components the fault current can be represented by (3.2). It is important to note here that ω_k^s is 0 in case of

DDOCs.

$$i(t) = \underbrace{A_1 cos(\omega_1 t + \theta_1)}_{\text{I}} + \underbrace{\sum_{j=2}^{M} A_j cos(j.\omega_1 t + \theta_j)}_{\text{II}} + \underbrace{\sum_{k=1}^{L} B_k e^{\frac{t}{\tau_k}} cos(\omega_k^s t + \theta_k^s)}_{\text{III}} + noise \tag{3.2}$$

where M is the total number of integer harmonics.

L is total number of transient components.

A_j and θ_j are magnitude and angle of the jth harmonic component, respectively; j=1 represents the fundamental frequency component.

ω_1 is the fundamental angular frequency.

B_k, τ_k, ω_k^s and θ_k^s are magnitude, time constant, angular frequency and angle of the k^{th} transient frequency component, respectively.

Fault current, i.e., $i(t)$, is passed through a moving average filter to obtain $i_{avg}(t)$ as defined in (3.3). To simplify the use of Prony analysis, it is assumed that the first sample of $i_{avg}(t)$ belongs to t=0 rather than t=T. Hence, (3.3) is defined from $t' = t$ to $t + T$ instead of $t' = t - T$ to t to compensate the time reference shift in Prony analysis. All operations in this section are expressed in continuous time domain for the sake of simplicity. The equations which will be derived are used as a close approximation of their discrete time equivalents.

$$i_{avg}(t) = \frac{1}{T} \int_t^{t+T} i(t')\, dt' \tag{3.3}$$

It is a known fact that the average value of the fundamental and its harmonic components over the period of fundamental frequency component (T) is zero. In addition, averaging significantly attenuates the noise present in the fault current signal. Therefore, we can rewrite (3.3) by only considering the term (III) as below.

$$i_{avg}(t) = \frac{1}{T} \int_t^{t+T} \sum_{k=1}^{L} B_k e^{\frac{t}{\tau_k}} cos(\omega_k^s t' + \theta_k^s)\, dt' \tag{3.4}$$

Integration by part theorem is employed to determine the analytical form of (3.4) which can be rewritten as in (3.5) [45].

$$i_{avg}(t) = \sum_{k=1}^{L} \tilde{B}_k e^{\frac{t}{\tau_k}} cos(\omega_k^s t + \widetilde{\theta_k^s}) \tag{3.5}$$

where

$$\tilde{B}_k = \frac{1}{T}[B_k . \frac{\tau_k}{1 + (\tau_k \omega_k^s)^2} . \sqrt{X_k^2 + Y_k^2}] \tag{3.6}$$

$$\tilde{\theta}_k^s = \theta_k^s - arg(X_k + jY_k) = \theta_k^s - atan2(\frac{X_k}{Y_k}) \tag{3.7}$$

$$X_k = \tau_k \omega_k^s . e^{\frac{T}{\tau_k}} cos(\omega_k^s T) - \tau_k \omega_k^s - e^{\frac{T}{\tau_k}} sin(\omega_k^s T) \tag{3.8}$$

$$Y_k = e^{\frac{T}{\tau_k}} cos(\omega_k^s T) + \tau_k \omega_k^s . e^{\frac{T}{\tau_k}} sin(\omega_k^s T) - 1 \tag{3.9}$$

It may be noted from (3.5) that the extracted signal through averaging filter, i.e., $i_{avg}(t)$, preserves its oscillation frequencies and time constants. However, the magnitudes and phase angles undergo a change. If $i_{avg}(t)$ is analyzed using Prony analysis, the extracted signal's parameters ($\tilde{B}_k, \omega_k^s, \widetilde{\theta_k^s}$ and τ_k) can be estimated. Using these parameters, X_k and Y_k can be calculated from (3.8) and (3.9), respectively. The transient signal parameters B_k and θ_k^s can then be calculated from (3.10) and (3.11). Equations (3.10) and (3.11) are directly derived from (3.6) and (3.7), respectively.

$$B_k = T\tilde{B}_k . \frac{1 + (\tau_k \omega_k^s)^2}{\tau_k \sqrt{X_k^2 + Y_k^2}} \tag{3.10}$$

$$\theta_k^s = \tilde{\theta}_k^s + atan2(\frac{X_k}{Y_k}) \tag{3.11}$$

3.4.2 Implementation

The process of obtaining accurate phasors for the proposed technique is shown in Figure 3.5. In the proposed algorithm, first, the sampled fault current $i[n]$, as represented by (3.12) is passed through an averaging digital filter.

$$i[n] = i(\frac{n}{f_s}), n = 0, 1...N_F - 1 \tag{3.12}$$

where N_F is the total number of fault current samples and f_s is the sampling frequency. The conventional averaging filter is an N tap digital filter and N is the number of samples per cycle and filter taps are equal to $1/N$. Use of the conventional filter is an accurate estimate of (3.3) only if the sampling frequency is very high.

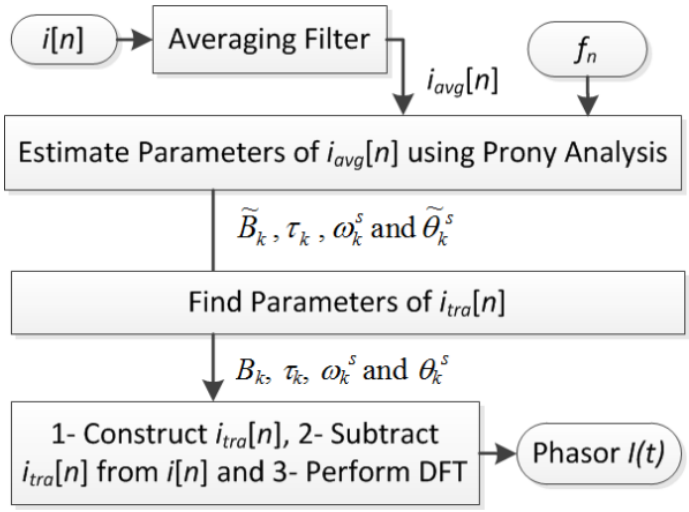

Figure 3.5: Flowchart of the proposed algorithm

In case of typical sampling rates in protective relays, small difference is observed between the responses of averaging filter in continuous and discrete time domains. Since the mathematical analysis for converting the averaged signal into original transient signal is presented in continuous time domain and is used as a close approximation to discrete time equivalents, the conventional digital filter can not accurately represent the averaged signal in continuous time. The two consecutive averaged samples are observed to have same positive and negative error in the average value. Since conventional averaging filter results in same positive and negative errors for consecutive averaged samples, on averaging the averaged value for sample 1 and sample 2 given by (3.13) and (3.14) we get the accurate average given by (3.15) which does not has error. In general, this new filter can be represented by (3.16) to achieve higher accuracy

for a typical sampling frequency in protection relays. Figure 3.6 shows the error(%) of both the conventional(ideal) and proposed averaging filter, for a test signal, i.e., $5e^{\frac{-t}{0.02}}\cos(194t + 85.9°)$. Sampling rate is assumed to be 64 samples per cycle, i.e., $N = 64$ and $f_s = Nf_n$. Fundamental frequency shown as f_n in Figure 3.5 is the estimated frequency to minimize the error during off-nominal frequency operation. As shown in Figure 3.6, the conventional averaging filter can introduce up to 1.8% of error while this is 0.02% in case of the proposed averaging filter. The performance of the proposed averaging filter is evaluated for test signals with different time constants, angular frequencies and initial angles. The results for different test signals (for different time constants and frequencies) are reported in appendix A.

$$i_{avg}[1] = \frac{1}{N}(i[1] + i[2] + ... + i[N]) \tag{3.13}$$

$$i_{avg}[2] = \frac{1}{N}(i[2] + i[3] + ... + i[N + 1]) \tag{3.14}$$

$$i_{avgnew} = \frac{1}{2N}[2 * (i[2] + i[3] + ... + i[N]) + (i[1] + i[N + 1])] \tag{3.15}$$

Generalizing (3.15) we get (3.16)

$$i_{avg}[n] = \frac{1}{N}\sum_{k=1}^{N-1} i[n - k] + (\frac{i[n] + i[n - N]}{2N}) \tag{3.16}$$

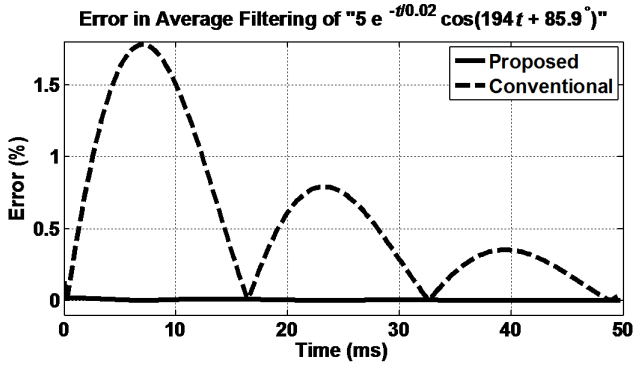

Figure 3.6: Error comparison of the ideal and proposed averaging filter

This filtered signal $i_{avg}[n]$ contains information about transient frequency components including SSFCs, DDOCs and non-integer harmonics. These components are identified by Prony analysis and compensated by the proposed algorithm. The length of $i_{avg}[n]$ after discarding initial one cycle of transient response of digital filter is $N_F - N$. Assuming that the fault current length is four cycles and N is 64, the length of $i_{avg}[n]$ after removal of the first cycle becomes 3 cycles = $3 * 64 = 192$ samples.

Prony function available in MATLAB signal processing toolbox is employed to identify and estimate parameters of different frequency components within $i_{avg}[n]$. Prony analysis can be carried out for different number of modes limited to half of the length of $i_{avg}[n]$, i.e., 96 in this case [41]. In the proposed technique, the minimum number of modes considered for Prony analysis is selected as 10. Lower number of modes results in less accurate estimation [14]. Therefore, Prony analysis is repeated for number of the modes between 10 and 96. The number of the modes defined for the prony analysis of the averaged signal determines signal order and hence the number of poles and zeros present in the signal. The prony returns same no of modes as defined in the beginning. However, not all the modes are relevant and only the most dominating modes (amplitude¿10% of signal amplitude) were choosen to construct the average signal. Due to the error in frequency estimation, it is possible that the averaged signal contains modes with frequency close to the fundamental and its integral harmonics. Reconstruction of these modes is avoided by excluding all the modes with frequencies within (3%)*j*f_n where j = 1 to 8 or frequencies above 8^{th} harmonics from signal identification process. The 3% threshold is selected assuming maximum 3% error in frequency tracking. 3% threshold ensures that if frequency tracking has more than 3% of error, the proposed algorithm should not incorrectly identify and compensate the fundamental component. In series compensated lines due to interaction of MOV in different phases, the presence of non-integer high frequency component is expected. For simulations done in this research work a frequency component 5.5*f_n was identified. In order to ensure proper compensation of such harmonics 8^{th} harmonic is selected conservatively as threshold. In each mode, the residue of the input signal ($i_{avg}[n]$)

and the estimated signal by Prony analysis is computed. The parameters ($\tilde{B}_k, \omega_k^s, \widetilde{\theta_k^s}$ and τ_k) corresponding to the mode which gives the minimum error or the best fit are chosen. If the minimum error is above the acceptable level, e.g., 5%, it is recommended to avoid signal compensation to avoid introducing any extra error.

B_k and θ_k^s are calculated as per (3.10) and (3.11). Finally, as shown in Figure 3.5, the transient signal ($i_{tra}[n]$) is reconstructed for N_F sample and subtracted from the original fault current signal i[n]. DFT is applied to the resulted signal to estimate the current phasor.

3.4.3 Theoretical Signal Analysis

In order to establish the accuracy and performance of the proposed Prony-DFT algorithm, the proposed technique is first tested for a theoretical signal. This theoretical signal consisting of constant fundamental frequency component, one DDOC and two SSFCs are generated for evaluation of the proposed technique. The parameters of different components are shown in Table 3.1.

In addition, the generated signal is contaminated by a uniform distribution noise with mean zero and standard deviation of 1%, equivalent to signal to noise ratio (SNR) of 40 dB of the fundamental frequency component which is normally expected in power system signals [22], 2^{nd} to 20^{th} integer harmonics with a total harmonic distortion (THD) of 5%. Any THD or combination of integer harmonics can be selected because the averaging filter and DFT will completely remove these high frequency components.

Table 3.1: Parameters of Theoretical Signal

	Fundamental	DDOC	SSFC1	SSFC2
Mag(kA)	3	0.23	4.4	8
Angle(degree)	-47	0	142	-17
f(Hz)	60	0	30	42
τ	-	-0.04	-0.024	-0.02

Figure 3.7 (a) shows the plot for the theoretical and the compensated signals after removal

of transient frequency components. It can be observed that the proposed technique has successfully removed all the SSFCs and DDOCs and the compensated signal is very close to a pure sinusoidal signal. Figure 3.7 (b) shows the average signal obtained from (3.16) and its Prony estimation. As it is illustrated that the average signal and the outcome of the Prony analysis are almost identical. Using the proposed technique, the transient signal $i_{tra}(t)$ is reconstructed using (3.8) to (3.11) (Figure 3.7 (c)). The compensated signal in Figure 3.7 (a) is obtained by subtracting the transient signal $i_{tra}(t)$ from the theoretical signal, i.e., $i(t)$. Figure 3.8 shows

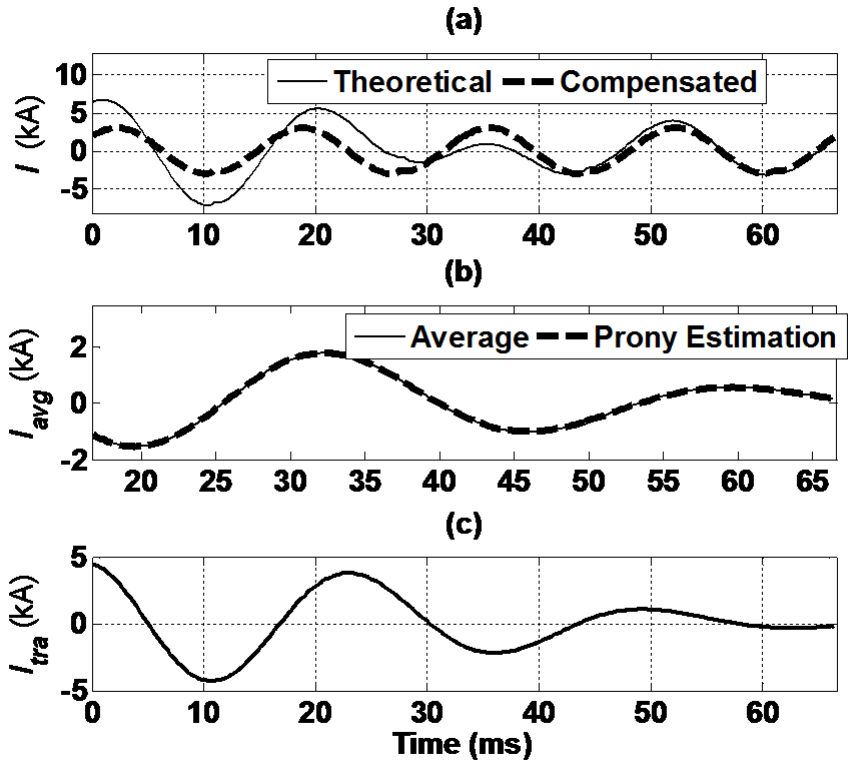

Figure 3.7: (a): Theoretical and the compensated signals, (b): averaged signal and its Prony estimation which are overlapping (c): transient signal constructed by the proposed technique.

the actual phasor of the theoretical signal $i(t)$ and its phasor estimation (magnitude and angle) using the proposed and 4-cycle DFT algorithms. Since for the latter algorithm only one phasor is estimated per four-cycle data, the estimated magnitude and angles are mentioned in text form in the Figure 3.8. As evident from this figure, the proposed method accurately estimates

the phasor of the fundamental frequency component which is 3 kA while the performance of 4-cycle DFT algorithm is adversely affected due to the presence of SSFCs.

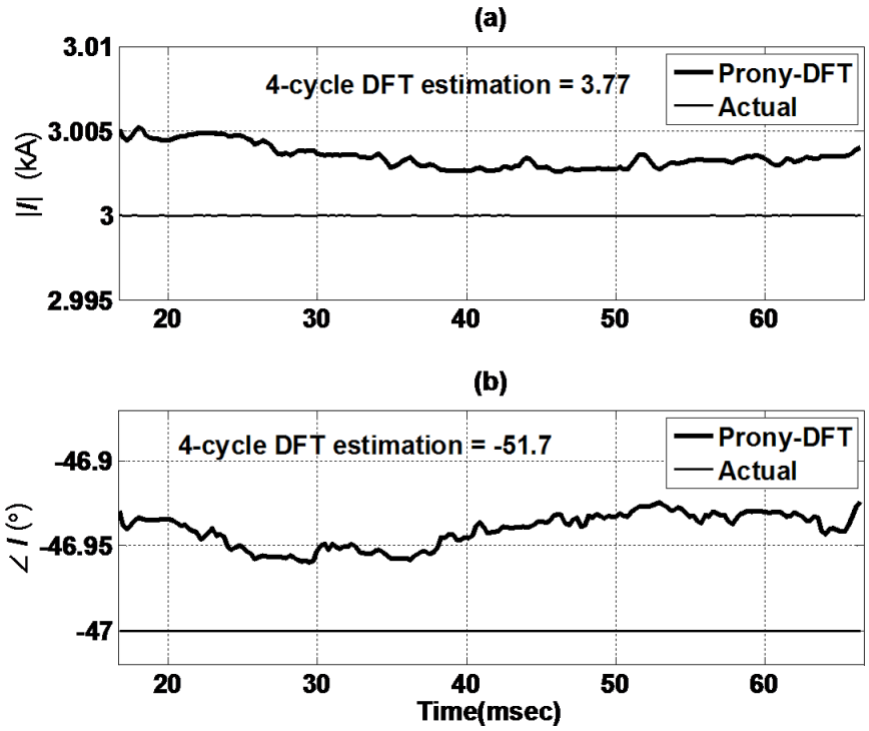

Figure 3.8: Phasor magnitude and angle estimated by Prony-DFT and 4-cycle DFT algorithms.

To better evaluate the effect of noise on the proposed technique, the theoretical signal shown in Table 3.1 including random noise is regenerated 100 times and applied to Prony analysis directly, the proposed Prony-DFT and 4-cycle DFT algorithms. In case of Direct-Prony analysis and 4-cycle DFT algorithm, one phasor value is obtained for the entire four-cycles fault current signal while for the proposed algorithm, the phasor values are estimated for each sample except the initial one cycle to exclude transients of DFT method. To be able to compare the results of the three techniques, the phasors values obtained through Prony-DFT is averaged over the last three cycles to obtain only one value. Phasor error ΔI is defined by (3.17).

$$\Delta I = \frac{|I_{Estimated} - I_{Actual}|}{|I_{Actual}|} \tag{3.17}$$

where $I_{Estimated}$ is the estimated phasor through any of the three techniques while I_{Actual} is the actual phasor, i.e., $3\angle -47^{\circ}$ in this study. Two performance indices are defined to be able to compare the results of the three techniques. The first index, i.e., M_{PE}, is the average of phasor error over 100 runs. This index indicates the expected value of phasor errors. As shown in Table 3.2, Prony-DFT shows 0.08% expected error which is about 37 times less than the one for Prony analysis, i.e., 2.96%. 4-cycle DFT algorithm also introduces significant error of about 27% due to the presence of SSFCs. The second index, i.e., the RSD (%), is the relative standard deviation of the phase error. This index indicates how phasor error is varying over 100 runs. In other words, it shows how sensitive the phasor estimation algorithm is to the noise. As expected, 4-cycle DFT is almost insensitive to the noise presence. As shown in Table 3.2, for this index, the Prony-DFT is about 27 times less sensitive to the noise as compared to direct Prony analysis. To study the effect of frequency estimation error on the proposed method, the

Table 3.2: Phasor Estimation Error

	Prony	Prony-DFT	4-cycle DFT
M_{PE}	2.96	0.08	25.84
RSD(%)	2.4	0.09	0.016

fundamental frequency of the theoretical signal is replaced with 59.9 and 59.8 Hz, respectively while the estimated frequency is set to 60 Hz. In this case, M_{PE} for 100 runs with harmonics and random noise are 1.8% and 3.78%, respectively. This level of error is still significantly smaller than the phasor values estimated by the 4-cycle DFT algorithm which are 25.95% and 26.1%.

3.5 Summary

In this chapter, series capacitor's overvoltage protection system and its components were discussed in detail. Function of MOV, spark-gap and bypass breaker was explained in detail. Operation of different components and how it impacts fault current characteristic were discussed.

In the later part of the chapter the proposed Prony-DFT technique was introduced. Prony analysis was discussed in brief. The derivation of mathematical formulas and how the proposed method was implemented were also discussed. Finally, the proposed Prony-DFT method was tested for a theoretical signal and the test results were compared with the other two technique, i.e., direct Prony and 4-cycle DFT in the last section of this chapter.

Chapter 4

Fault Location:PSCAD Simulation and Results

4.1 PSCAD Simulation and System Configuration

PSCAD/EMTDC is a general-purpose time domain simulation program for multi-phase power systems and control networks. It is mainly dedicated to the study of transients in power systems. A full library of advanced components allows a user to precisely model interactions between electrical networks and loads in various configurations. A graphical user interface and numerous control tools make PSCAD a convenient and interactive tool for both analysis and design of any power system.

PSCAD simulations are carried out so as to test the algorithm in an environment which is close to the real world's power system. Susceptibility and sensitivity of the algorithm to CT and CCVT transients, type of fault, harmonics, noise and other factors have been put to test by simulating the system in PSCAD environment. To evaluate the performance of the proposed technique, a 500 kV series compensated transmission line system is simulated in PSCAD/EMTDC. As shown in Figure 4.1, series compensation is considered at Bus A end. Capacitor coupled voltage transformers (CCVTs) are considered at the line ends to allow use

of the accurate and well proven fault location algorithm proposed in [46]. Frequency dependent distributed transmission line model is used for modeling lines 1 and 2. The transmission line system is series compensated at Bus A side for 67.5% of total inductive reactance of line 1 and line 2, which corresponds to an equivalent capacitance of 30 uF. The level of compensation is not varied for performing simulation studies as it will not impact the results. Even in the simulated cases the level of compensation varies due to MOV conduction for high fault currents. The effective reactance of the capacitor varies (reduces) when MOV conducts and hence the fault current experiences different levels of compensation for different types of fault, which can be as low as 30%. The rated current of the capacitor is considered as 1181 A. MOV rating after considering an overload factor of 1.5 is calculated as 153 kV. The source impedance ratios (SIRs) for A and B ends are set to 0.2 and 0.3, respectively. The parameters of the simulated line are shown in Table 4.1. These parameters are corresponding to a typical 500 kV system available in PSCAD/EMTDC.

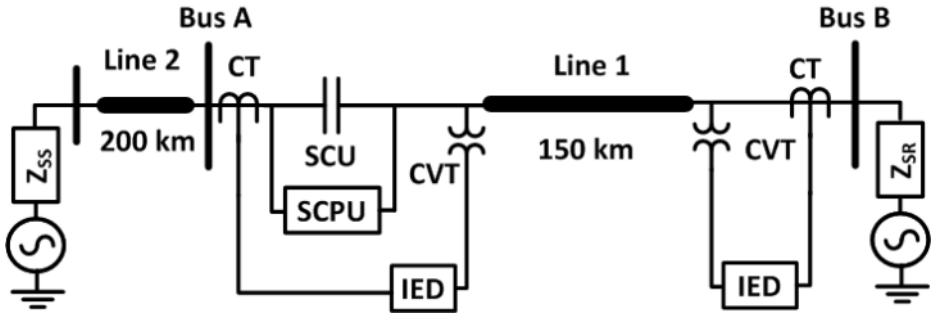

Figure 4.1: Single line diagram of the simulated system in PSCAD/EMTDC

Further, CT and CCVT models available in PSCAD/EMTDC are used for measuring the current and voltage respectively. The output of each instrument transformer is passed through a 2^{nd} order butter-worth anti-aliasing filter with a cutoff frequency of 1920 Hz and is recorded with the sampling rate of 20 kHz. In addition signals are contaminated with a noise with signal to noise ratio (SNR) of 40 dB. The recorded signal is imported in MATLAB and the sampling rate is decimated (down-sampled) to 3840 Hz. The decimated voltage and current signals are

converted to their corresponding primary values.

The measured voltage signals from both lines ends are passed on to the proposed Prony-DFT and 4-cycle DFT algorithms. Prony-DFT algorithm identifies and compensates CCVT transient, thus no CCVT transient filter is required. In case of 4-cycle DFT algorithm, consideration of CCVT transient filter increases the error value as 4-cycle DFT filter accumulates the transient response of CCVT transient filter. Therefore, CCVT transient filter is not included in both algorithms. In the simulation carried out, the MOV is not bypassed intentionally as discussed in Section 3.2.2.

Table 4.1: Transmission Line Parameters

	Positive Sequence	Zero Sequence
Impedance(Ω/km)	0.0179+j0.3748	0.3447+j1.216
Admittance(S/km)	0.1E-7+j4.378xE-6	0.1E-7+j2.747xE-6

4.2 Fault Location and Performance Comparison

4.2.1 Performance Evaluation

Figure 4.2 (a) shows the phase A instantaneous voltage measured by the intelligent electronic device (IED) located at substation A and its compensated signal obtained by the proposed algorithm in case of an AG fault occurring at 40% of the line from Bus A with a 10 ohm fault resistance at zero point on wave of voltage signal.

It can be seen that the measured voltage signal includes considerable unwanted frequency components due to CCVT transient and series compensation. The output of the averaging filter, i.e., $v_{avg}(t)$, and its estimation obtained by Prony analysis is shown in Figure 4.2 (b). As depicted here, Prony analysis has successfully found an accurate fit. Figure 4.2 (c) shows the transient signal, i.e., $v_{tra}(t)$, constructed by the proposed algorithm for the entire fault duration. The compensated voltage signal shown in Figure 4.2 (a) is obtained by subtracting the $v_{tra}(t)$

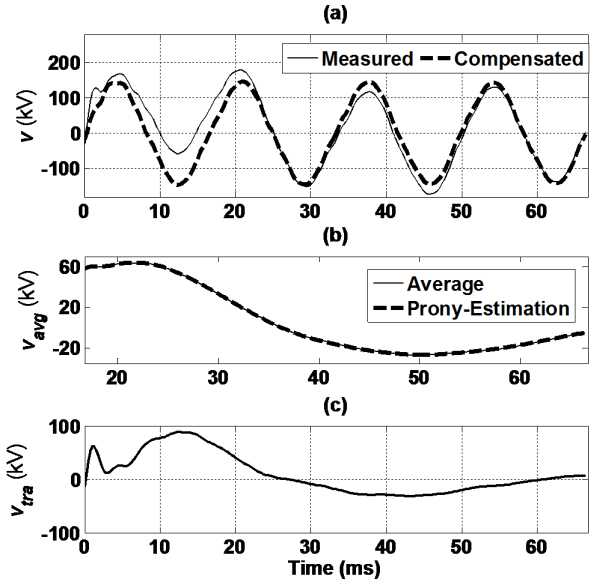

Figure 4.2: (a): Measured voltage signal generated by PSCAD/EMTDC and re-constructed compensated signal (b): average signal and its Prony estimation and (c): transient signal constructed by the proposed algorithm

from the signal measured by the instrument transformers. As it is evident from the Figure 4.2 (a), the compensated voltage signal is almost a pure 60 Hz sinusoidal signal.

Figure 4.3 (a) and (b) show the magnitude and angle for Phase A voltage phasors using Prony-DFT and 4-cycle DFT algorithms. As it is shown, the phasor estimated by the proposed technique is almost consistent and deviate only a little from its mean value. This indicates that the Prony-DFT algorithm significantly attenuates transient frequency components resulting in almost steady phasor magnitude and angle as compared to other techniques discussed in 2. As 4-cycle DFT only estimates one phasor value for the four-cycle data, the magnitude and angle of this phasor are printed in Figure 4.3 (a) and (b), respectively. The same approach used for voltage signals is applied to the current signals. Figure 4.4 (a) and (b) show the magnitude and angle for Phase A current phasor, respectively using Prony-DFT and 4-cycle DFT algorithms. Similar to the voltage signal, the proposed technique significantly attenuates transient frequency components for the current signal resulting in almost steady phasor magnitude and angle. Since the actual phasor values for both voltage and current signals are not known from

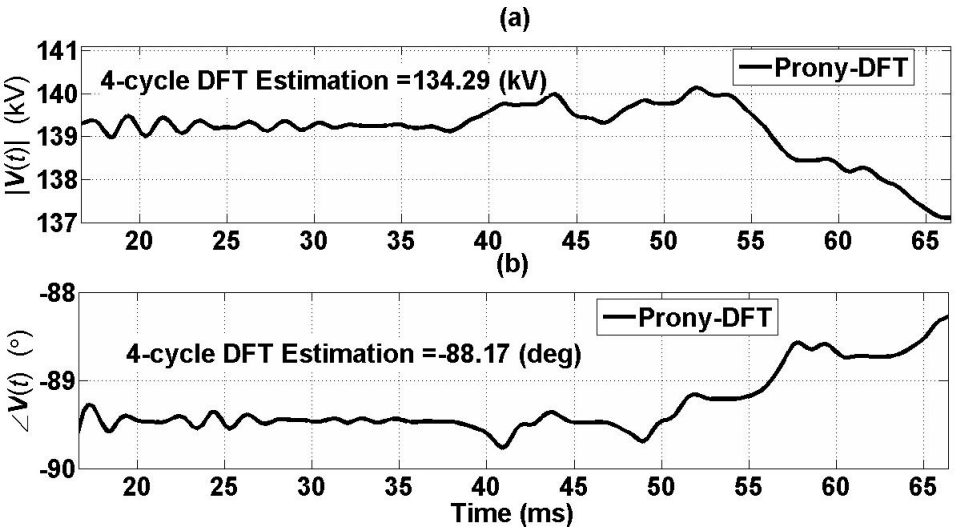

Figure 4.3: Phasor magnitude and angle of phase A voltage

PSCAD/EMTDC simulation, it is not possible to directly compare the accuracy of both techniques. Hence, an established fault location technique [46] is used to evaluate and compare the results of the proposed algorithm.

4.2.2 Comprehensive Fault Analysis

In order to further validate the performance of the proposed technique, a total of 84 fault scenarios are simulated in PSCAD/EMTDC using the system shown in Figure 4.1 for different fault locations (0 to 100% with steps of 20%), fault types (AG, BC, BCG, ABC), fault resistances (AG: 0Ω and 10Ω, BC and BCG:0Ω and 6Ω and ABC: 0Ω) and fault instances (zero and peak points on wave). In case of a three phase fault system is balanced and therefore ABC-G is not simulated purposely. Since both are symmetrical faults and system is balanced, the proposed technique will still perform accurately. Phasors are estimated through the Prony-DFT and 4-cycle DFT algorithms, and fault location is determined for the entire 84 cases. Fault current and voltages for all the three phases are available from PSCAD simulation but actual value of phasors are not known. Thus, finding and plotting the phasors for these 84 fault cases does not add any value to the test results because the phasors cannot be compared with an actual value

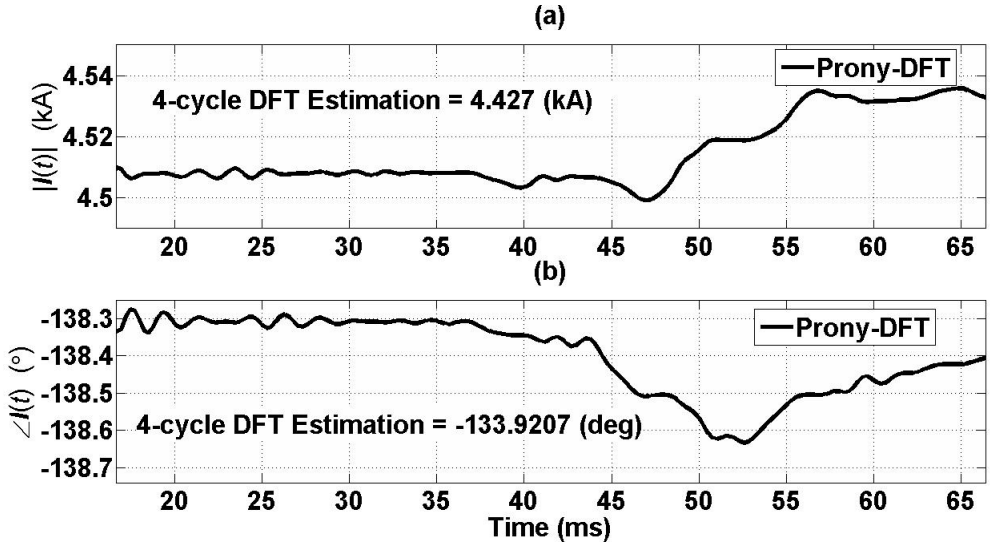

Figure 4.4: Phasor magnitude and angle of phase A current

and error in the phasor estimation cannot be estimated. Therefore, fault location is an effective tool to evaluate the performance of the proposed technique. Fault location in each case is determined using fault location algorithm which uses phasors computed using the proposed method and 4-cycle DFT. The method for reporting the result is described in the next paragraph.

In case of Prony-DFT algorithm, for each case, out of four cycles of fault samples data, the last three-cycles of estimated phasor can be utilized to determine the fault location as transient response of DFT algorithm is one cycle. To be able to compare the results of Prony-DFT algorithm with 4-cycle DFT, where only one phasor value and thereby one fault location is estimated, the fault locations determined based on Prony-DFT phasor estimation are averaged over the last three cycles, i.e., Approach 1, and the last one cycle, i.e., Approach 2. As shown in Figure 4.5, the results of both approaches are very close and overlapping in most of the cases though Approach 2 shows considerably higher error in few cases such as case 49 and 52 as compared to Approach 1. This indicates that the fault locations estimated based on Prony-DFT phasors are almost consistent with time. Nevertheless, it is recommended to average the fault location results over the last three cycles or the length of available phasor values. Figure 4.5 also shows the fault location estimated by 4-cycle DFT phasors for all 84 cases.

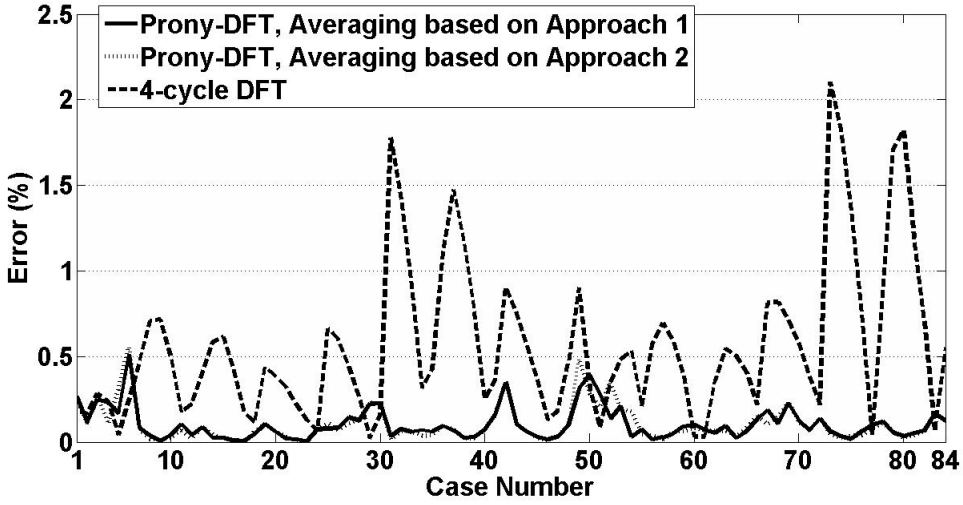

Figure 4.5: Fault location error (a): maximum error in the last 3 cycles (b): maximum error in the last cycle and (c): average error in the last cycle.

As it is shown, the errors of the fault location obtained through the proposed Prony-DFT both averaging approaches are considerably smaller than the ones obtained based on 4-cycle DFT in most of the cases. The averaged error of the 4-cycle DFT over 84 cases is 0.56% while this is 0.1% in case of Prony-DFT algorithm based on Approach 1. The fault location estimated through Prony-DFT is more accurate than the 4-cycle DFT in 86% of the cases. For rest of the 14% of cases when 4-cycle DFT give better results the sub-synchronous frequencies present in the signal falls in the range when it gets eliminated by the 4-cycle DFT (see frequency response of 4-cycle DFT). Finally, the maximum fault location error due the Prony-DFT Approach 1 is 0.51% while this is 2.1% in case of 4-cycle DFT.

As the fault location algorithm employed in this analysis is based on distributed line model and also exact transmission line parameters are used in the fault location algorithm, the only major possible source of error is the phasor estimation algorithm. This fact indicates the accuracy of the Prony-DFT and its effectiveness in removing transient frequency components.

4.2.3 Limitation

This technique requires 3-4 cycles of data for better estimation of parameters. The performance of the proposed method will be affected if the adequate amount of fault samples are not available. Limited amount of fault data will affect the accuracy but the technique can still be applied. Also no other technique is available to remove SSFCs from the fault signal. Even 4-cycle DFT would require 4-cycles of fault data.

4.3 Summary

In this chapter, the proposed technique was further tested with the help of PSCAD and MATLAB simulations. A typical 500 kV system was simulated in PSCAD. 84 cases of fault were examined for different fault types, fault locations, fault resistances and fault instances. According to the result of simulation, the proposed technique significantly reduces the error of fault location due to more accurate phasor estimation as compared to the 4-cycle DFT.

Chapter 5

Summary and Conclusion

5.1 Summary

In Chapter 1, different aspects of power system protection were discussed in detail. In the later part of the chapter under Section 1.1, the problem was defined and available solutions were discussed. Chapter 1 had also presented the insight to literature survey and author's objectives and contributions of the research. In Chapter 2 fundamentals of phasor estimation and various methods available for phasor estimation were discussed. 1-cycle and 4-cycles DFT were discussed at length and performance of each of them was compared and presented. Various transient component of fault signals were also discussed. Cosine and Mimic-DFT were defined as a mitigating technique foe decaying DC removal.

In Chapter 3, introduction to series compensation and its advantages were presented. In this Chapter author had also identified the issues with the fault signals (current and voltage) of a compensated line. Then in the later part of the Chapter, the proposed Prony-DFT technique was presented for estimating the accurate phasors in the presence of SSFCs. The technique was then validated with the help of a theoretical signal.

In Chapter 4, the proposed technique was further tested with the help of PSCAD and MATLAB simulations. Details of the test system and parameters of various components used for

developing a series compensated transmission line system in PSCAD were also provided. Simulated cases of faults were used to extensively test the proposed algorithm using an established fault location technique. Result comparison of the proposed method and the 4-cycle DFT were presented in the last section of this Chapter.

5.2 Contribution

This research work has resulted in following key contributions:

1. A new offline phasor estimation technique (refer publication 1) was proposed which can accurately estimate voltage and current phasors in the presence of multiple SSFCs in series compensated lines. The proposed algorithm is not sensitive to the presence of noise and harmonics.

2. Techniques proposed earlier in the literature were tested only for an assumed theoretical signal. In this study, in addition to testing on theoretical signal, the combination of PSCAD simulation and fault location in MATLAB was proposed to further evaluate the performance of the proposed technique. Since the phasor values for simulated PSCAD signal were unknown, fault location was used as a means to determine the accuracy of the proposed method. Testing of the proposed method using PSCAD simulated signal was more exhaustive as it also considers the non-linearity of the MOV and its resultant dynamic impedance.

5.3 Future Research Work

1. Devise the mathematical analysis in discrete time domain. In the presented research the mathematical analysis was done in continuous time domain and was used as a close approximation of the discrete time equivalents. The conventional digital averaging filter cannot accurately represent average of continuous time signal and results in erroneous

results. To take care of any error due to this a new type of averaging filter was introduced. Once the mathematical analysis is obtained in discrete domain, the conventional averaging filter can be employed for averaging.

2. Reduce the computation requirements by limiting the number of possible modes. Since the modes are varied from 10 to 96 in order to obtain accurate parameters in the presented research, work can be done to limit the number of modes and still have the desirable accuracy.

3. To test the algorithm with FACTS-based series compensation such as TCSC and SSSC. The technique presented was tested for fixed type of series compensation. However, with the penetration of FACTS devices into the power system, it would be a great value addition if the algorithm is tested for FACTS-based compensation.

4. To try the combination of Prony-DFT and fault location algorithm assuming CCVT at bus side to determine the overall error as fault location in this case would be more sensitive to phase errors.

Bibliography

[1] S. H. Horowitz, A.G. Phadke, ”Power system relaying”, Third edition, Wiley Press, April 2008.

[2] A.G. Phadke, J.S. Thorp, ”Synchronized phasor measurement and their applications”, First edition, Springer, August 2008.

[3] R.M. Mathur, R.K. Varma, ”Thyristor based FACTS controllers for electrical transmission system”, First edition, Wiley IEEE Press, February 2002.

[4] P. Kundur, ”Power system stability and control”,*EPRI Power System Engineering Series,* Tata McGraw-Hill, 2010.

[5] P.M. Anderson, ”Power system protection”, First edition, Tata McGraw-Hill, 1998.

[6] V.Cook, ”Fundamental aspects of fault location algorithms used in distance protection,” *Proc.IEE*, vol. 133, no. 6, Sept. 1986.

[7] R. Grunbaum, J.Samuelsson, ”Series capacitors facilitate long distance AC power transmission,” *Proc. 2005 IEEE PowerTech,* St. Petersurg, Russia.

[8] ”Series capacitors for increased power transmission capacity in the Finnish 400 kV grid,” *ABB AB, Vasteras, Sweden*, Application Note A02-0222 E, Nov. 2010.

[9] R. Grunbaum, J. Samuelsson, C.Li, ”Series capacitors for increased power transmission capacity of a 500 kV grid intertie,”.

[10] G.E. Lee, D.L. Goldsworthy, ”BPA’s pacific AC intertie series capacitors: experience, equipment and protection,” *IEEE transactions on power delivery,* vol.11, no.1, Jan. 1996.

[11] H.J. Altuve, J.B. Mooney, G.E.Alexander, ”Advances in series compensated line protection,” *Schweitzer Engineering Lab.Inc.*.

[12] K.W. Braun, G.H. Thumm, L. Kirschner, ”Design of the first asian 500 kV thyristor controlled series compensation scheme TCSC Tian Guang at Pingguo substation,” *Siemens, Erlangen, Germany*.

[13] C. Fecteau, ”Accurate fault location algorithm for series compensated lines using two terminal unsynchronized measurement and hydro quebec’s field experience,” *33rd Annual western protective relay conference,* Spokane,WA, 17-19 Oct., 2006.

[14] T. Maekawa, Y. Obata, M. Yamaura, Y. Kurosawa, H. Takani, ”Fault location for series compensated parallel lines,” *IEEE/PES asia pacific transmission and distribution conference and exhibition,* vol.2, pp. 824- 829, 6-10 Oct. 2002.

[15] J. Sadeh, N. Hadjsaid, A.M. Ranjbar, R. Feuillet, ”Accurate fault location algorithm for series compensated transmission lines,” *IEEE transactions on power delivery,* vol.15, no.3, pp.1027-1033, Jul 2000.

[16] M.G. Ahsaee, J. Sadeh, ”A novel fault-location algorithm for long transmission lines compensated by series FACTS devices,” *IEEE transactions on power delivery,* vol.26, no.4, pp.2299-2308,Oct.2011.

[17] D.L. Goldsworthy, ”A linearized model for MOV-protected series capacitors,” *IEEE transaction on power system,* vol. PWRS-2, no. 4, Nov. 1987.

[18] A.F. Elneweihi, F.P. Plumptre, et. al, ”Series capacitor bank protection,” *IEEE power systems relaying committee WG K13,* IEEE TP-126-0, 1998.

[19] J. Izykowski, E. Rosolowski, P. Balcerek, M. Fulczyk, M.M. Saha, "Accurate noniterative fault-location algorithm utilizing two-end unsynchronized measurements," *IEEE transaction on power delivery,* vol. 26, no. 2, pp. 547-555, April 2011.

[20] ABB research Ltd. Switzerland, "Method for fault location on series compensated power transmission lines with two-end unsynchronized measurement" U.S. Patent 2011/0082653, April 7, 2011.

[21] M. Al-Dabbagh , S.K. Kapuduwage, "Using instantaneous values for estimating fault locations on series compensated transmission lines," *Elsevier electric power systems research,* vol. 76, no. 13, p.p. 25-32, September 2005.

[22] M.R.D. Zadeh, A real time power system harmonic estimator considering fundamental frequency variation, *International journal of emerging electric power systems,* vol. 11, no. 4, Article 4, 2010.

[23] M.M. Saha, J. Izykowski, E. Rosolowski, B. Kasztenny, "A new accurate fault locating algorithm for series compensated lines," *IEEE transactions on power delivery,* vol.14, no.3, pp.789-797,Jul,1999.

[24] J. Izykowski, E. Rosolowski, P. Balcerek, M. Fulczyk, M.M. Saha, "Fault location on double-circuit series-compensated lines using two-end unsynchronized measurements," *IEEE transactions on power delivery,* vol.26, no.4, pp.2072-2080, Oct. 2011.

[25] C.S. Yu, C.W. Liu, S.L. Yu, J.A. Jiang, "A new PMU-based fault location algorithm for series compensated lines," *IEEE transactions on power delivery,* vol.17, no.1, pp.33-46, Jan 2002.

[26] W.J. Cheong, R.K. Aggarwal,"A novel fault location technique based on current signals only for thyristor controlled series compensated transmission lines using wavelet analysis and self organizing map neural networks," *Eighth IEE international conference on developments in power system protection,* vol.1, no., pp. 224- 227 Vol.1, 5-8 April 2004.

[27] M. Joorabian, ”Artificial intelligent based fault location technique for EHV series-compensated lines,” *International conference on energy management and power delivery, proceedings of EMPD ’98,* vol.2, no., pp.479-484 vol.2, 3-5 Mar 1998.

[28] Y. Wan, X. Yin, Z. Zhan., J. Tang, Z. He, ”A new method for identifying the fault location on series compensated lines based on transient fault information,” *4th international conference on electric utility deregulation and restructuring and power technologies (DRPT),* pp.78-82, 6-9 July 2011.

[29] M.M. Saha, J. Izykowski, E. Rosolowski, ”Fault location on series-compensated transmission line using measurements of current differential protective relays,” *Proceedings of the international symposium on modern electric power systems (MEPS),* vol., no., pp.1-6, 20-22 Sept. 2010.

[30] IEEE Guide for ”Determining fault location on AC transmission and distribution lines,” *IEEE StdC37.114-2004,* vol.,no.,pp.01-36,2005.

[31] G. Benmouyal, ”Removal of DC-offset in current waveforms using digital mimic filtering,” *IEEE transaction on power delivery,* vol. 10, no. 2, pp. 621-630, Apr 1995.

[32] E.O. Schweitzer and D. Hou, ”Filtering for protective relays,” *19th Annual western protective relay conference,* Spokane,WA, 1992.

[33] Y.S. Cho, C.K. Lee, G. Jang, H.J. Lee, ”An innovative decaying dc component estimation algorithm for digital relaying,” *IEEE transaction on power delivery,* vol.24, no.1, pp.73-78, Jan. 2009.

[34] S.H. Kang, D.G. Lee, S.R. Nam, P.A. Crossley, Y.C. Kang, ”Fourier transform-based modified phasor estimation method immune to the effect of the dc offsets,” *IEEE transaction on power delivery,* vol. 24, no. 3, pp. 1104-1111, July 2009.

[35] M.R.D. Zadeh, Z. Zhang, "A new DFT-based current phasor estimation for numerical protective relaying", *IEEE transaction on power delivery,* 2013.

[36] C.S. Yu, "A reiterative DFT to damp decaying dc and sub-synchronous frequency components in fault current," *IEEE transaction on power delivery,* vol. 21, no. 4, pp. 1862-1870, Oct. 2006.

[37] J.C. Gu , K.Y. Shen, S.L. Yu , C.S. Yu, "Removal of DC offset and sub-synchronous resonance in current signals for series compensated transmission lines using a novel fourier filter algorithm" *Elsevier electric power systems research,* vol. 76, pp. 327335, 2006.

[38] J.F. Hauer, C.J. Demeure, L.L. Scharf, "Initial results in Prony analysis of power system response signals," *IEEE transaction on power system,* vol. 5, no. 1, pp. 80-89, Feb 1990

[39] J. Woodworth, "MOV protection of series capacitor bank," *Arrestor Works,* July 2008.

[40] J.F. Hauer, "Application of Prony analysis to the determination of modal content and equivalent models for measured power system response," *IEEE transaction on power system,* vol. 6, no. 3, pp. 1062-1068, August 1991.

[41] S.L. Marple, "Digital spectral analysis with applications", Englewood Cliffs, New Jersey: Prentice-Hall Inc., 1987, pp. 304.

[42] D.J. Trudnowski, M.K. Donnelly, J.F. Hauer, "Estimating damping effectiveness of BPA's thyristor controlled series capacitor by applying time and frequency domain methods to measured response," *IEEE transaction on power system,* vol. 11, no. 2, pp. 761-766, May 1996.

[43] E.O. Schweitzer, A. Guzman, H.J. Altuve, D.A. Tziouvaras, J. Needs, "Real-time synchrophasor applications in power system control and protection," *Managing the change, 10th IET international conference on developments in power system protection (DPSP 2010),* pp. 1-5, March 29 2010-April 1 2010.

[44] F.D. Zahlay, K.S. Rama Rao, ”Neuro-Prony and Taguchi’s methodology-based adaptive autoreclosure scheme for electric transmission systems,” *IEEE transactions on power system,* vol. 27, no. 2, pp. 575-582, April 2012.

[45] U.L. Rohde, G.C. Jain, A.K. Poddar and A.K. Ghosh, ”Introduction to integral calculus: systematic studies with engineering applications for beginners” First Edition, John Wiley and Sons, 2012, pp. 97-120.

[46] J. Izykowski, E. Rosolowski, P. Balcerek, M. Fulczyk, M.M. Saha, ”Accurate noniterative fault-location algorithm utilizing two-end unsynchronized measurements,” *IEEE transactions on power delivery,* vol. 26, no. 2, pp. 547-555, April 2011.

Appendix A

Results of proposed averaging filter

As discussed in 3 that the conventional averaging filter introduces error if the sampling rate is not very high. But in the commercial relay environment a sampling rate of 64 samples/cycle is an industry standard. Since the mathematical analysis for converting the averaged signal into original transient signal is presented in continuous time domain and is used as a close approximation to discrete time equivalents, the conventional digital filter can not accurately represent the averaged signal in continuous time. In order to avoid errors due to conventional averaging a new N+1 averaging filter was introduced. The performance of the proposed averaging filter was evaluated for different frequencies and time constant for an assumed sub-synchronous frequency signal which is decaying. The signal is represented by A.1. The value of τ is varied from -0.02 to -0.2 in four steps. For each decay constant (τ) the sub-synchronous frequency is varied from 30 Hz to 50 Hz in three steps.

$$i(t) = A * e^{\frac{t}{\tau}} * cos(2\pi * f_s t + 45^\circ) \tag{A.1}$$

The absolute error due to conventional averaging and proposed averaging filter are plotted for all the 12 cases discussed above. It can be observed that the maximum absolute error for conventional averaging filter can be as high as 4%. However, the error in case of proposed filter remains very low ,i.e., close to zero.

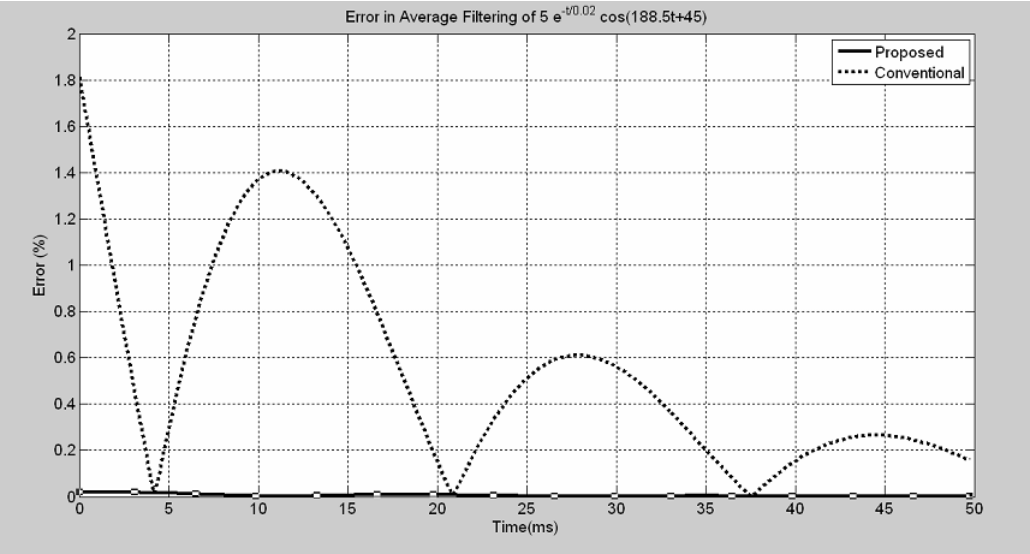

Figure A.1: Error comparison of the ideal and proposed averaging filter

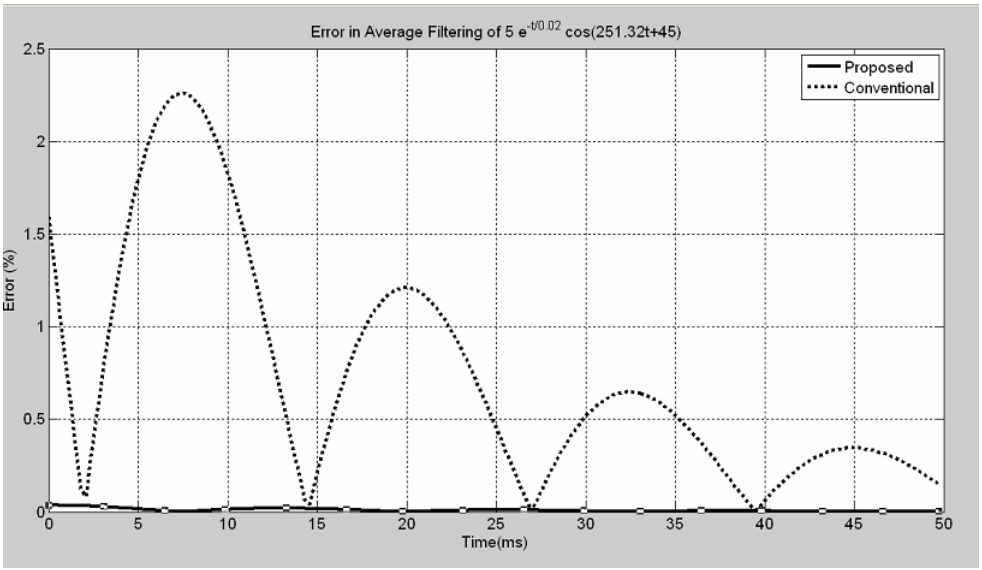

Figure A.2: Error comparison of the ideal and proposed averaging filter

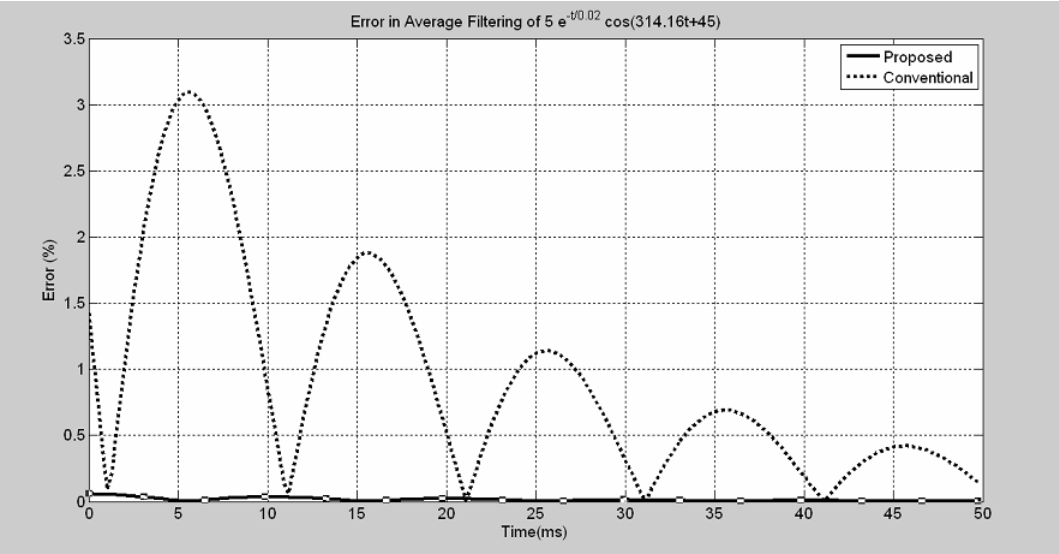

Figure A.3: Error comparison of the ideal and proposed averaging filter

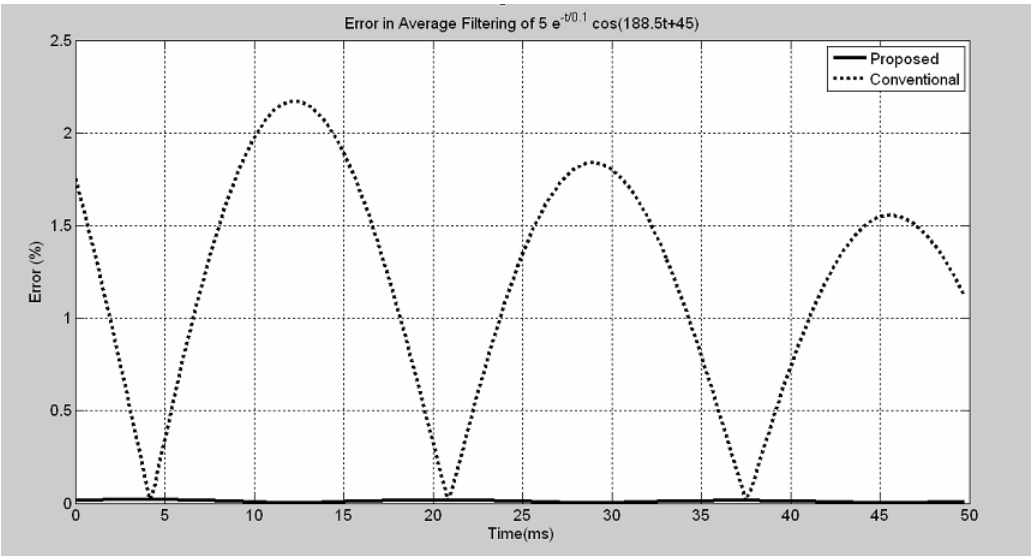

Figure A.4: Error comparison of the ideal and proposed averaging filter

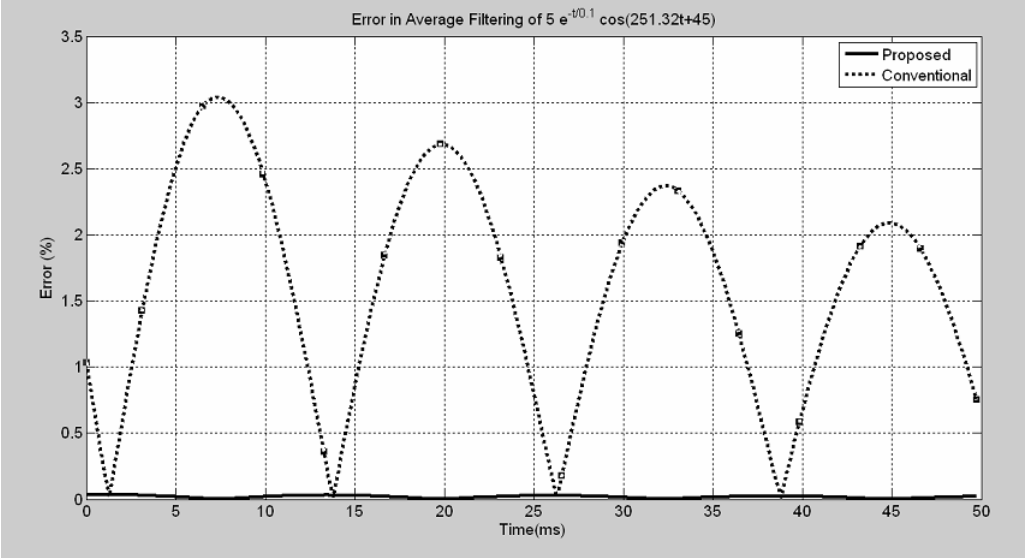

Figure A.5: Error comparison of the ideal and proposed averaging filter

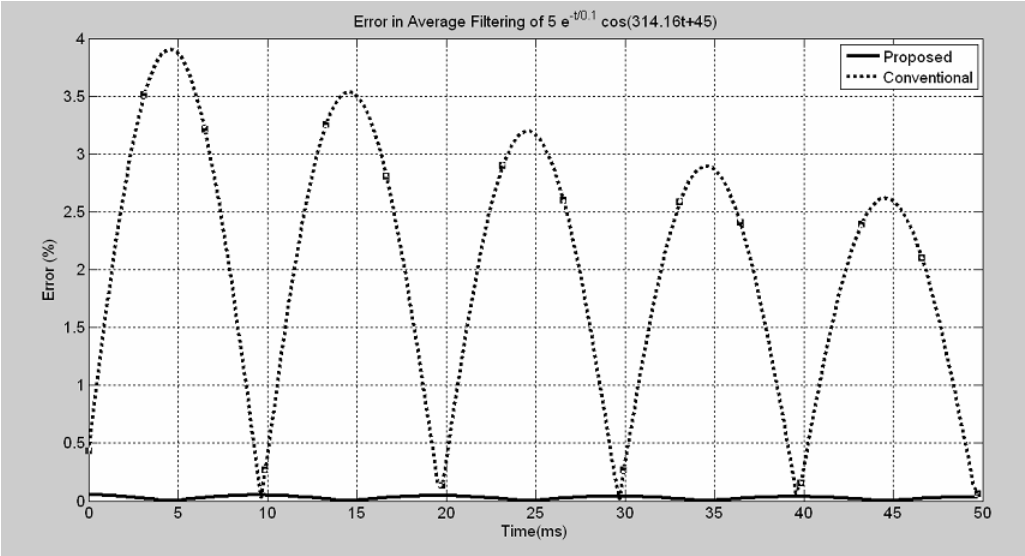

Figure A.6: Error comparison of the ideal and proposed averaging filter

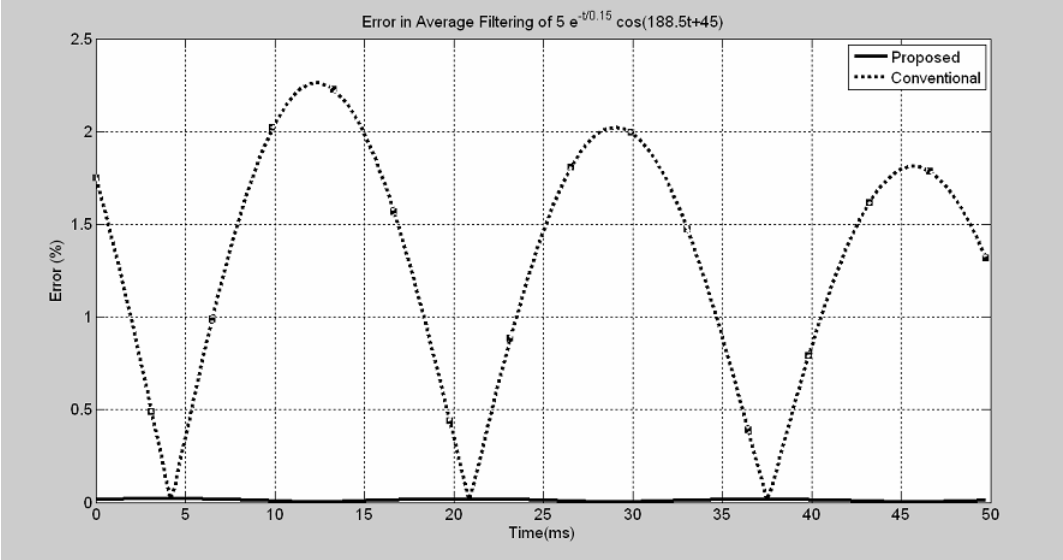

Figure A.7: Error comparison of the ideal and proposed averaging filter

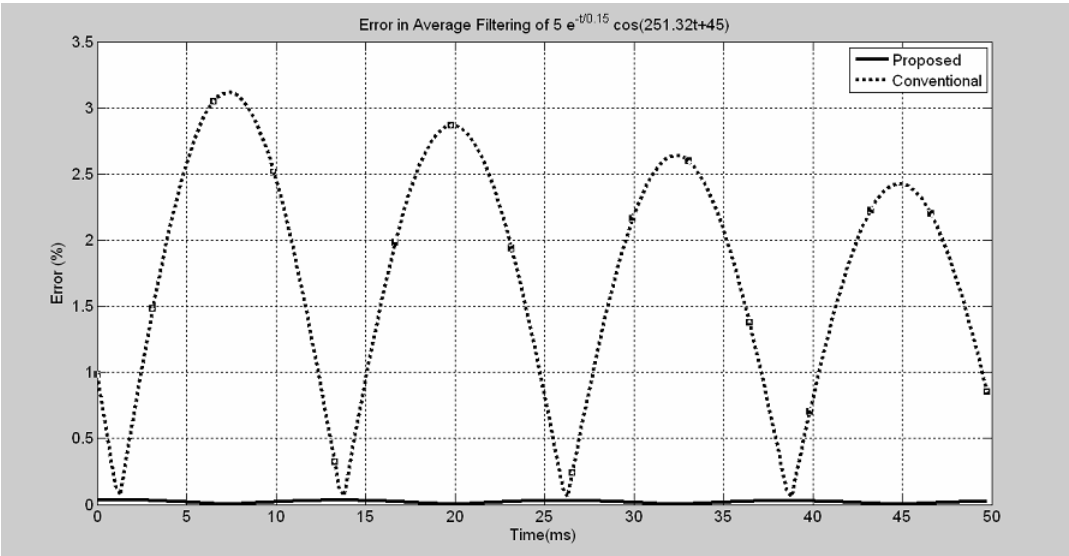

Figure A.8: Error comparison of the ideal and proposed averaging filter

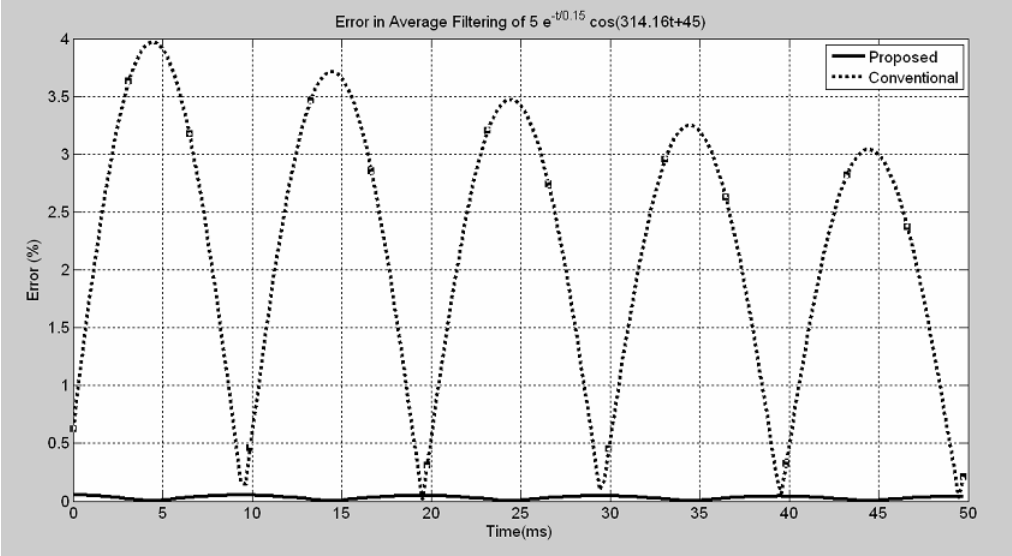

Figure A.9: Error comparison of the ideal and proposed averaging filter

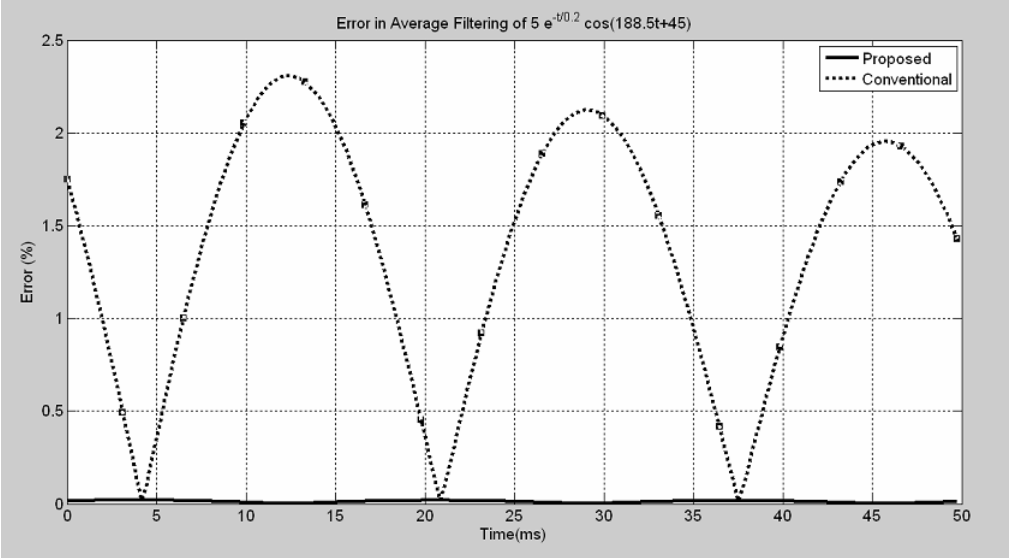

Figure A.10: Error comparison of the ideal and proposed averaging filter

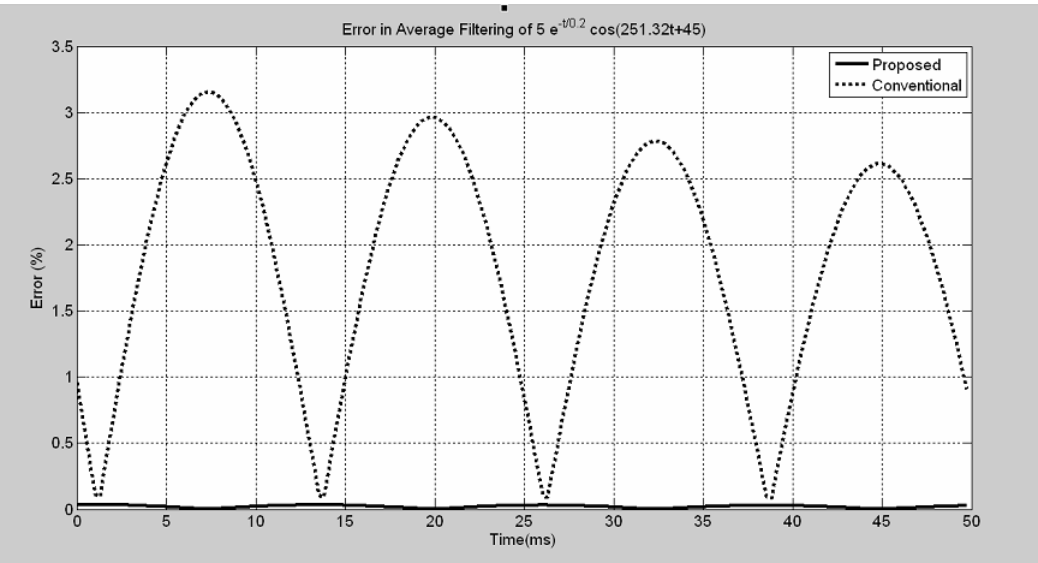

Figure A.11: Error comparison of the ideal and proposed averaging filter

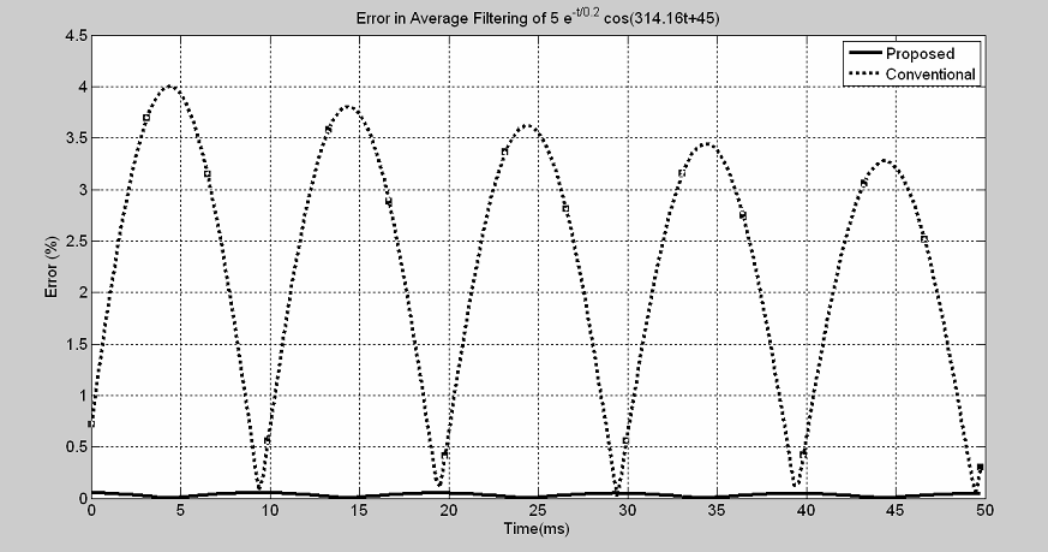

Figure A.12: Error comparison of the ideal and proposed averaging filter

Curriculum Vitae

Name:	Rubeena
Post-Secondary Education and Degrees:	S.T.D.B. Vidyalaya India 2003 - 2007 B.Tech (Honors), Zakir Hussain College of Engg and Tech, A.M.U. U.P., India. 2011 - 2014 MESc Western University London, ON
Related Work Experience:	Teaching Assistant at UWO 2007 - 2011 Engineer at Engineers India Ltd. 2011-2014 Sr. Engineer at Engineers India Ltd (On Sabbatical).

Publications:

1. R. Rubeena, M.R. Dadash Zadeh, T.P.S. Bains, "An accurate offline phasor estimation for fault location in series-compensated lines", *IEEE transactions on power delivery,* vol.PP, no.99, pp.1,1, January 2014.

2. M.R. Dadash Zadeh, R. Rubeena, "Communication-aided high-speed adaptive single-phase reclosing", *IEEE transactions on power delivery,* vol.28, no.1, pp.499-506, 2013.