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Enhanced Voltage-Sourced Inverters for Large-Scale Grid-Connected Photovoltaic Systems

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A thesis submitted in partial fulfillment of the requirements for the degree in Doctor of Philosophy

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Abstract

This thesis is mainly focused on (i) modeling of large-scale PV systems in order to study the factors that influence the capacity, efficiency, power quality and safety in connection with the power grid and (ii) proposing system- and circuit-level solutions and control strategies/techniques to improve the aforementioned factors.

To that end, a model for PV array is developed to study the mismatch power loss in different PV array interconnection methods, especially during the partial shading condition. Further, a two-MPPT structure is proposed to reduce the mismatch power loss in centrally structured PV systems.

Then, a single-stage VSC-based system is proposed to utilize the two-MPPT structure for better efficiency. The proposed system also doubles the DC-link voltage while respecting the safety standards, which in turn, increases the capacity and the efficiency of the central inverter.

To further improve capacity and efficiency, a two-stage system is proposed in which the variable MPP voltage of smaller sub-arrays are regulated, by dedicated DC-DC boost converters, at the inverter DC-side terminals. This lets the inverter use the full DC voltage permissible rating and reduces the ohmic loss in DC and AC wirings and in the transformer. The system employs a three-level NPC inverter which generates output with better power quality, facilitates the adoption of two-MPPT structure, and permits utilizing low-voltage (half-rated) switches. The system also promotes the modular/distributed structure which improves the efficiency under partial shading and enables the possibility of utilizing PV modules of different types, ratings, and alignments.

Finally, a mitigation technique is proposed in the inverter and grid-interface structures to prevent formation of damaging temporary overvoltages, which sometimes are produced in power systems by distributed generations including PV. The technique utilizes a four-leg inverter connected to a grid through a Y/YG isolation transformer.

The effectiveness of the proposed techniques and control strategies are demonstrated through time-domain simulation studies conducted in the PSCAD/EMTDC software environment.

Keywords: Control, Distributed Generator (DG), Fault, Grounding, Inverter-Based DG, Islanding, Maximum Power Point Tracking (MPPT), Modeling, Neutral-Point Clamped (NPC) Inverter, Partial Shading, Photovoltaic (PV) Systems, Power Systems, PV Array, Single-Stage PV System, Temporary Overvoltage (TOV), TOV Mitigation, Two-Stage PV System, Voltage-Sourced Inverter (VSI).

Dedication

To my parents,

my wife,

and the joy of my life, my daughter, Elina.

Acknowledgements

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List of Abbreviations and Symbols

3Ph	Three-Phase
AC	Alternating Current
ANN	Artificial Neural Network
BL	Bridge-Linked
CSI	Current-Sourced Inverter
DC	Direct Current
DER	Distributed Energy Resource
DG	Distributed Generator
EMC	Electromagnetic Compatibility
EMTDC	Electromagnetic Transients including DC
EPIA	European Photovoltaic Industry Association
HBC	Half-Bridge Converter
HV	High Voltage
IC	Incremental Conductance
LPF	Low Pass Filter
LV	Low Voltage
MIMO	Multi-Input-Multi-Output
MP	Maximum Power
MPDR	Maximum-Power Drop Ratio
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MV	Medium Voltage
NPC	Neutral-Point Clamped
P&O	Perturb and Observe
p.u.	Per-Unit
PCC	Point of Common Coupling
PI	Proportional-Integral
PLL	Phase-Locked Loop
PSCAD	Power System Computer-Aided Design
PV	Photovoltaic
PWM	Pulse-Width Modulation
SA	Sub-Array
SLG	Single Line-to-Ground

SP	Series-Parallel
TCT	Total Cross-Tied
THD	Total Harmonic Distortion
TOV	Temporary Overvoltage
TrOV	Transient Overvoltage
VSC	Voltage-Sourced Converter
VSI	Voltage-Sourced Inverter
YG	Grounded Wye (transformer connection)
ZSI	Z-Sourced Inverter

Chapter 1

Introduction

In recent years, renewable energy systems have attracted remarkable attention and investment in many countries [1], due to concerns about environmental issues, ever-increasing world's energy demand, and outlook of depletion of fossil fuel reserves [2]. Among renewable energy systems, photovoltaic (PV) systems are expected to play an important role in the future and, as such, a great deal of research effort is dedicated to enhancing their performance and efficiency, at both component and system levels. PV systems are either connected to a large independent grid and feed power to the grid or are separated from any grid and operate as the main power supply for a group of loads, mostly in remote buildings and communities.

1.1 Statement of Problem and Research Objectives

The aim of this research is to study the factors that limit the capacity, efficiency, power quality, and the safety of the grid-connected large-scale PV systems, and to propose appropriate solutions to improve those factors.

- Capacity: Although large-scale PV farms have reached a capacity of up to several hundred MW, the single PV inverter capacity is limited to about 1 MW, and larger power ratings are achieved by parallel connections of the smaller inverter units. Since one large inverter can offer better efficiency, lower cost, and easier implementation compared to the two parallel-connected (smaller) half-rated inverters, improving the capacity of the PV inverters can be one major contributing factor to further support the solar PV industries' fast growth.

- Efficiency: The efficiency of PV systems is affected by that of its components, including the PV array and inverter, and the system configuration. Different PV array configurations yield different levels of mismatch power loss, especially under partial shading conditions, and thus produce different total energy. Further, under normal operating conditions, the efficiency of different inverter and system configurations is affected by the switching power loss over the inverter switches and by the conduction power loss all over the DC- and AC-side cables, switches, filter, and transformer.

- Power quality: With the fast growth of distributed generators, including the PV, the quality of their produced power needs to be further improved in order to not adversely affect the hosting network's performance. This can be achieved through utilizing appropriate inverter structures, inverter control schemes, and/or better filters.

- Safe grid-integration: Among the many grid-integration issues of PV systems, which includes the fault ride-through capability, islanding detection, and ancillary services provision, the overvoltage produced by PV systems (like other distributed generators) is one subject of interest in this thesis. With the widespread penetration of distributed generators (DGs) in power systems, the grid and DGs are facing the ever-increasing problem of temporary overvoltages produced by DGs and their damages on utility equipment and customer loads, especially the single-phase ones. Appropriate solutions need to be worked out to prevent overvoltage formation and/or to suppress the produced overvoltage in the contributing DGs' structure.

Thus, this thesis aims to propose PV systems (consisting of array, inverter, and grid interface) which address all of the aforementioned characteristics and deliver better energy yield, higher capacity, better power quality, and safer integration with the utility network. To this end, PV array configurations and single- and two-stage as well as two- and multi-level inverter structures will be studied and appropriate structures and control strategies/schemes will be developed to achieve the defined goals.

Therefore, more specific objectives of this thesis are:

- To develop a PV array model in order to study the efficiency of different PV array interconnection methods in central-configured PV systems, especially during partial shading conditions, and to search for methods to mitigate the disproportionate mismatch power loss during partial shading and characteristic mismatch conditions.

- To develop a single-stage inverter to increase the capacity by addressing the DC voltage limitation imposed by national regulations and to enhance the energy yield of the system through reducing the aforementioned mismatch power loss.

- To study the restrictions of the conventional single-stage converters for higher power ratings, to develop a two-stage conversion system, based on neutral-point clamped (NPC) technology, to further improve the capacity, efficiency, and output power quality, and to introduce multi-MPPT and distributed PV array structures.

- To derive the mathematical model of the NPC inverter under special conditions discussed in this thesis in which the two PV sub-arrays utilized in the proposed two-MPPT structure, act as two independent DC power sources for the NPC inverter.

- To study the grid integration issues of the PV systems, especially the temporary overvoltage (TOV) problem caused by PV systems in the power network, and to propose appropriate mitigation techniques.

1.2 Background and Related Works

According to the EPIA data, the total PV generation connected to the electricity grid surpassed 100 GW in 2012 [3] and is expected to reach 300 GW in 2016 [4]. The installed-system prices continue to fall, and PV is becoming increasingly more cost competitive across regions with high electricity consumption than the domestic power generation. This, together with the improved efficiency of PV system components, especially the solar panels, and the environmental concerns related with conventional and nuclear power plants given the Fukushima nuclear plant disaster of 2011 [5], accelerate further growth of the PV industry, which in turn, further reduces the prices in a positive feedback form.

To maintain this fast growth, on the one hand, and to deal with potential power network problems and complexity because of the high penetration of PV systems, on the other hand, much research is being conducted on improving the PV systems' performance and profitability and on the safe and supportive integration of them within the grid.

1.2.1 PV Systems

PV panels and the inverter are the two main components, of a PV system, which determine the cost and the efficiency and performance of the entire system to the greatest

extent. However, other system parts, including the wirings, maximum power point tracking (MPPT) scheme, and grid interface, can considerably affect the overall efficiency. In fact, the system configuration or the components interconnection structure plays an important role in the technical and financial characteristics of a PV system.

PV System Configurations:

Regarding the interconnection of the PV array and the inverter, PV systems are normally categorized into four or five main groups, as shown in Figure 1.1, [6–9].

- Central structure:

  In the central structure the entire array, which is composed of a large number of series- and parallel-connected PV modules, is connected directly to the converter, which is normally a single-stage three-phase inverter. The power loss due to the partial shading and mismatch is high in this structure since even one shaded module affects the operating point of all the unshaded modules. However, for large-scale PV systems, where appropriate precautions are taken to minimize the shading and characteristic mismatch, the central structure is the most commonly practiced one because of the high efficiency of high-power inverters, their low cost and footprint, and simplicity of utilizing only one inverter [10].

- String structure:

  In string structure, each PV string, composed of a limited number of series-connected PV modules, is interfaced to the grid by a rather small inverter. The operating voltage of each PV string is determined, individually, by a corresponding MPPT scheme, thus, the mismatch power loss is reduced. However, for large-scale applications, the cost will be considerably high due to the large number of required inverters.

- Multi-string structure:

  The multi-string structure is a further development of the string structure, where in a two-stage system, several PV strings are connected to a central inverter through their dedicated DC-DC converters. Therefore, the operating voltage of each string is controlled individually, and the mismatch power loss is decreased. This structure has gained more popularity because of its better overall efficiency and the possibility

of distributed PV array configuration, different PV module type utilization, and different PV module orientation [11].

- AC modules and micro-inverters:

  The AC module is the integration of one PV module and a small inverter into one electrical device. Each AC module performs maximum power point tracking for, and harvests the optimum power from, its connected module. Therefore, it removes the mismatch power loss, and as such, is expected to offer better efficiency. On the other hand, it requires voltage amplification due to the low voltage of one module, which might affect the overall efficiency and cost. The inherent plug-and-play feature facilitates the utilization and installation of AC modules by non-technical people [12]. Micro-inverters share the same concept, advantages, and disadvantages with AC modules expect that they are not physically included inside the module structure and that recent ones can accept connection from two PV modules.

- Power optimizers:

  Power optimizers are small DC-DC converters dedicated to every module. They perform the MPPT task for their connected single module to eliminate the mismatch power loss and, therefore, are considered in the same category with the AC modules. However, since a central inverter is required to connect them to the grid, they can also be considered in the multi-string structure category.

AC modules are normally rated around 180-250 W, and therefore they are used in low-power (not more than a few kW) roof-top residential applications where the possibility of shading from neighboring buildings and trees is high. The string inverters are rated around 2-3 kW, or slightly higher for the 1000 VDC standard (in Europe), and as such are utilized in low- to medium-power residential and commercial/industrial roof-top applications. Their shading performance is low compared to the AC modules but is high compared to the central structures.

The multi-string and central structures' rating can reach up to about 1 MW, so are utilized in medium- to high-power commercial/industrial and utility-scale applications. The multi-string structure has better partial shading performance but can be expensive compared to the central structure, which is the most commonly practiced structure in large-scale applications since it also offers lower installation and maintenance costs, simplicity of grid interconnection and control, and central monitoring and control [13].

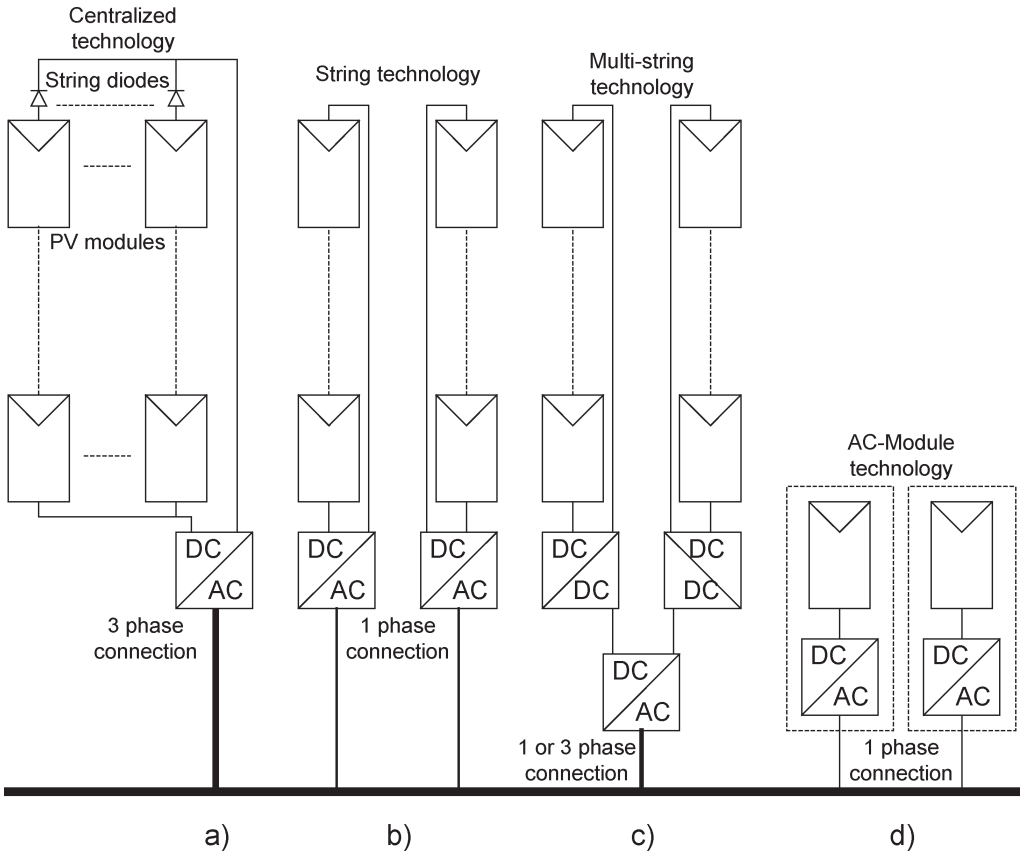

Figure 1.1: PV systems using a) centralized structure, b) string structure, c) multi-string structure, and d) AC module [7]

1.2.2 PV Arrays

The Problem of Partial Shading and Characteristic Mismatch:

As two influential factors in regards to the performance and efficiency of a PV system, the impact of characteristic mismatches amongst PV cells and the phenomenon of maximum-power drop due to partial shading have been the subjects of intense research.

In a PV system, PV modules are connected in series and in parallel in order to enable power generation and processing at an adequately large voltage level and efficiency. However, when PV cells in a module are shaded, they experience a significant power output drop and can even act as loads to other (unshaded) cells and modules. This phenomenon can result in hot spot formation in, and potential damage of, the shaded cell(s), in addition to a disproportionate maximum-power drop in the overall array. To circumvent the aforementioned issue, manufacturers typically install bypass diodes in anti-parallel with each group of 12-18 cells, in a module [14]. Nonetheless, the reduced

energy yield remains an issue to be further addressed through more effective PV module clustering configurations and MPPT algorithms.

Thus far, several power-electronic converter configurations [8, 9], and PV module clustering methods [15–18], have been proposed for mitigation of the maximum-power drop due to partial shading. Despite the existence of classes of high-power PV systems that employ a multitude of small converters, that is, one converter per sub-array [8,9], the use of one central high-power single-stage electronic converter for the entire PV system is very common for economical reasons and for the relative simplicity of the overall system. For this class of PV systems, the way that PV modules are clustered plays an important role in the performance of the PV system under partial shading conditions.

References [16] and [17] compare three common PV array configurations shown in Figure 1.2, i.e., the series-parallel (SP) configuration, the bridge-linked (BL) configuration, and the total cross-tied (TCT) configuration. Reference [16] has studied the characteristic mismatch phenomenon due to PV cell aging and shading, and has concluded that the TCT and BL configurations are superior to the SP configuration (with the TCL being the best). Reference [17] has adopted a more accurate model of a PV module that takes into consideration the dependence of the parameters on the operating condition. The model in [17] includes bypass diodes which are assumed to be connected in anti-parallel with every 18 PV cells; the model is tested through the exposure of modules and sub-modules to 30 different random profiles of insolation, and indicates the superiority of the TCT configuration in the sense that it provides a higher maximum power and exhibits lower variations in the maximum power point (MPP) voltage, compared to the BL and SP configurations. Reference [17] further implies that, as far as the characteristic mismatch issue is concerned, a lower number of series-connected modules is in favor of a lower array maximum-power drop. Such a practice, however, is in conflict with that of series connection of many modules for higher voltage and, thus, efficiency.

Some other researchers propose alternative solutions like reconfiguration of the PV modules inside the array to minimize the mismatch power loss of the entire array [19,20]. This strategy requires the application of a controllable switching matrix between the PV modules and the inverter. However, the implementation is costly and is not applicable to large-scale high-power systems.

On the other hand, maximum power point tracking of the PV array in the presence of partial shading and other characteristic mismatches is challenging and most conventional MPPT schemes cannot determine the global maximum from local ones and, thus,

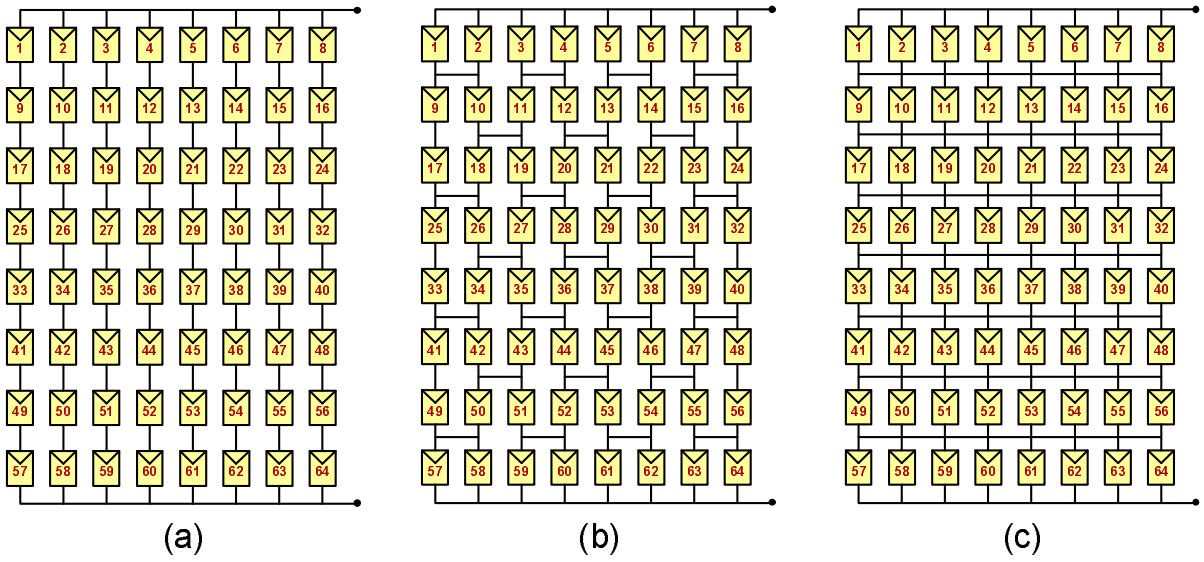

Figure 1.2: Different array configurations: a) series-parallel (SP), b) bridge-linked (BL) and c) total-cross-tied (TCT)

lose considerable power. Comparative studies on the MPPT schemes including perturb and observe (P&O), incremental conductance (IC), artificial neural network (ANN), and fuzzy-logic methods can be found in [21, 22].

1.2.3 PV Inverters

The grid-connected converters for PV applications perform two main tasks. They convert the DC power of the PV array into sinusoidal AC power in order to export to the utility grid and regulate the operating point of the PV array in order to derive maximum power out of the array.

The PV converters must be cost effective and should maintain high power efficiency over a wide range of input voltage and power since these variables are defined in very wide ranges as functions of solar irradiation and ambient temperature. Moreover, the converters must be highly reliable since most manufacturers offer a warranty of 25 years on 80% of initial efficiency. On the grid integration side, factors like power quality, fault ride-through capability, detection of islanding operation, and proper grounding should be insured in the converter design.

Classification of the PV Inverters:

A. Single-stage and two-stage converters

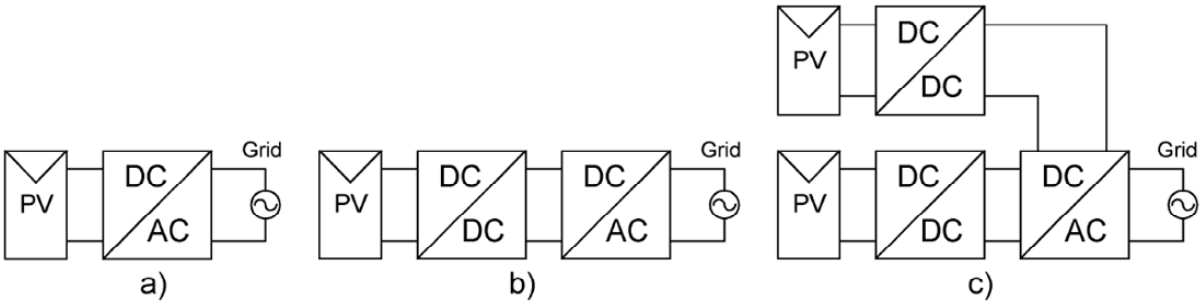

Figure 1.3: Different PV inverter topologies: a) single-stage, b) central two-stage, and c) distributed two-stage [7].

In single-stage systems the DC power of the PV array is directly converted to AC by an inverter, as shown in Figure 1.3(a). However, in two-stage systems, the variable DC voltage of the array is converted to a constant DC voltage in a primary DC-DC stage and is then converted to AC power by a second stage, the inverter. Figure 1.3(b) illustrates a central two-stage inverter topology in which all the PV modules connected in series and parallel as one array are interfaced with the grid by two equal size conversion stages, similar to the central structure described in Subsection 1.2.1. Figure 1.3(c), however, illustrates a distributed two-stage inverter topology in which two or more PV sub-arrays, consisting of a smaller number of series- and parallel-connected modules, are interfaced to the central inverter through their dedicated DC-DC converter. This modular concept renders better efficiency under partial shading and the possibility of utilizing PV modules of different types, ratings, and alignments [23].

The single-stage systems, compared to the two-stage ones, are normally more efficient and economical because the processing of power takes place in only one stage and avoids the power loss and cost of the extra stage. However, due to the variable nature of the MPP voltage of the array, especially during partial shading conditions when some modules might be bypassed by their protective bypass diodes, the inverter-side voltage of the isolating transformer is assigned a low value in order to prevent saturation of the inverter at the lowest DC-link operating voltage. This low AC voltage results in high current for a given power rating and causes large power loss at DC- and AC-side wirings and the transformer, especially in the case of high power rated inverters, due to the fact that the power loss is proportional to the square of current. The DC-DC converter in two-stage topologies converts the array/sub-array variable voltage to a constant voltage, slightly smaller than the maximum permissible DC voltage (which is 600 V for the North American systems unless the system is taken to the "behind the fence" [24]), at DC-link

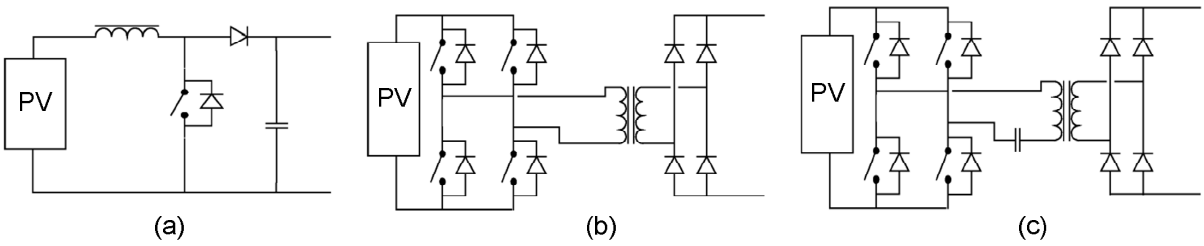

Figure 1.4: Different DC-DC converter topologies: a) boost converter, b) H-bridge DC-DC converter, and c) series resonant H-bridge DC-DC converter [6].

such that the central inverter can perform the conversion task at higher DC and AC voltage levels to improve the efficiency. Thus, also considering the better efficiency under partial shading, the distributed or modular two-stage inverter topology may offer better overall efficiency at high power ratings compared to the central single-stage one [25].

Voltage-sourced inverters (VSI), because of their control simplicity and higher efficiency and reliability, are the common choice for the central inverters, although limited applications of current-sourced inverters (CSI) [26–28] and, recently, Z-sourced inverters (ZSI) [29, 30] were also reported in the literature. The DC-DC conversion task, however, can be performed using many topologies including boost converters, buck-boost converters, and H-bridge DC-DC converters [6]. The boost converter, as shown in Figure 1.4(a), is the simplest and therefore can deliver better efficiency. The H-bridge DC-DC converter, shown in Figure 1.4(b), which in fact is a DC-AC-DC converter, performs both the DC-DC conversion task and the isolation task between the PV array and the grid through a high frequency transformer, which reduces power loss and transformer size. This characteristic is attractive for low- and medium-power PV systems which otherwise have to use a large size power-frequency isolation transformer between the inverter and the grid. However, for large-scale applications where the two isolation transformer and distribution step-up transformer can be merged into one, the boost converter is more cost effective. The series resonant H-bridge DC-DC converter, shown in Figure 1.4(c), is the improved version of the conventional H-bridge DC-DC converter with a soft-switching characteristic to reduce the switching losses.

B. Two-level and multi-level converters

Conventional DC-AC converters produce AC voltage through the selective connection, normally based on a PWM pattern, of the positive and negative terminals of the DC source through the semiconductor switches to the AC terminals, and thus, are called two-level converters. In contrast, there are other converters, called multi-level converters,

which use midpoint and other potential levels between the positive and negative levels of DC voltage, to produce the AC voltage. They can generate output voltage and, consequently, output current with less total harmonic distortion (THD) or better power quality. They also reduce the dv/dt stress of the output voltage and, thus, decrease the electromagnetic compatibility (EMC) problem [31]. Furthermore, because of the smaller (but more) partial DC voltage levels, the voltage rating of the semiconductor switches is reduced, so cheaper switches can be utilized. On the other hand, they need more switches, which may increase the converter cost and footprint. Neutral-point-clamped, flying capacitors, and cascaded H-bridge are three main multi-level converters used in industrial applications [32,33]. Figure 1.5(a) and (b) show the schematic diagram of one phase of the three-level version of the NPC and the flying capacitors multilevel inverters, respectively. Figure 1.5(c), however, illustrates one phase of a five-level cascaded H-bridge inverter, a topology which is normally adopted for multi-level inverters with five voltage levels or higher. The combination of these topologies, especially the hybrid cascaded NPC, is also used to implement multi-level inverters with a large number of voltage levels [34].

Among the introduced multi-level inverters, the NPC inverter, also known as the diode-clamped inverter, is simple and the most similar one to the conventional two-level converter in terms of control. The NPC inverter permits the employment of low-voltage switches (half-rated) compared to the conventional two-level VSI [35]. Furthermore, NPC uses one DC-link for the three-phase inverter, saving on the capacitor cost and space. Among the multi-level converters reported for medium- and high-power PV applications [6,36], the majority are three-level ones because the number of switches, and thus the cost, increase dramatically when the number of levels are increased.

C. Single-phase and three-phase grid connection

PV systems can be interfaced to the grid through single-phase or three-phase connections. The single-phase inverters, which connect the smaller PV arrays to the grid, suffer from a double-frequency pulsation in DC-link voltage, which decreases the power efficiency of the PV array [23]. To reduce the pulsation, larger DC-link capacitors should be utilized. In high power PV systems, the required size of the capacitors is too large to be considered technically and financially viable.

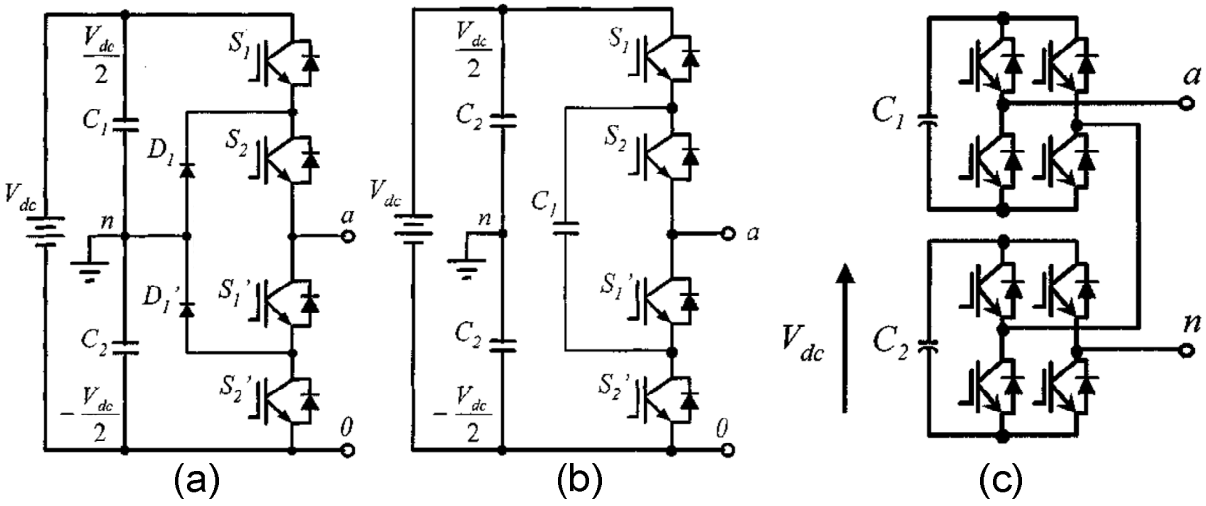

Figure 1.5: Multilevel inverter topologies: a) NPC, b) flying capacitors, and c) cascaded H-bridge [32].

1.2.4 Grid Integration of PV Systems

With the proliferation of distributed generators, the utility grid faces new possibilities including increased transmission and distribution network capacity, improved reliability, and provision of ancillary services by DGs, and new challenges including possible instability, protection complexity, and overvoltage problems caused by DGs.

Not long ago, distributed generators had to meet some few conditions and standards for connection to the grid, in order not to adversely affect grid performance. These conditions included production of high quality power with harmonic contents less than specific levels defined by IEEE Std. 519 [37], and detection of islanding and de-energizing the utility line during a predefined time window to avoid damage to the utility and customers equipment and personnel [38].

However, recently, it was realized that distributed generators, especially the inverter-based ones, can support the grid more actively in order to improve the performance and the capacity of the network. Therefore, the grid codes in most countries were redefined to include the new requirements for DGs to provide dynamic and static support during network fault and normal operation. For instance, the German grid code for connection of PV systems to the medium-voltage power grid requires dynamic grid support, or fault ride-through (FRT) capability, demanding that the generating plants have to stay connected during a fault, support the voltage by providing reactive power during the fault, and consume the same or less reactive power after the fault clearance [39].

Figure 1.6 illustrates the time required for a DG, connected to the grid at the medium-

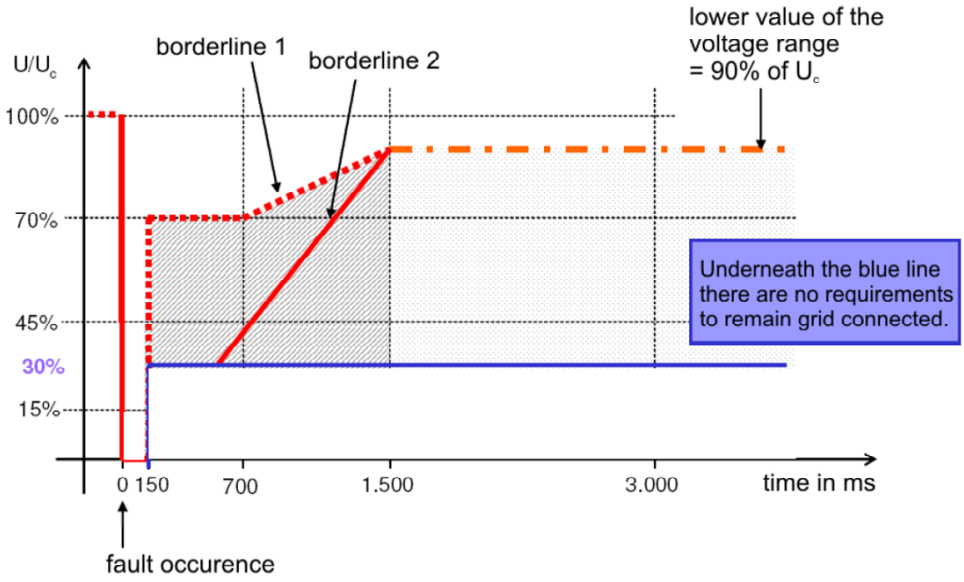

Figure 1.6: Voltage limit curves for a DG connected at medium-voltage level in case of a network fault [39].

voltage level, to stay connected depending on the severity of voltage drop in case of a network fault. For instance, the DG is expected to stay connected for 150 ms even if the voltage drops to about zero. Figure 1.7(a) shows the dynamic voltage support required from that DG in the case of a network fault, which is accomplished through the provision of reactive current/power as a function of network instantaneous voltage. Figure 1.7(b), however, shows the static voltage support required from that DG in normal operation, through the control of power factor (or provision of reactive power) as a function of network steady-state voltage. Finally, Figure 1.8 illustrates the required active power control capability to support the network frequency. As can be seen, the DG should be able to reduce its available real power as a function of grid frequency in case of an overfrequency condition in the network.

In PV systems, the control task is normally performed in synchronous dq frame synchronized with the grid voltage, which results in decoupled real and reactive power control through the decoupled d- and q-axis current control-loops [40, 41]. During the normal operation of a PV system, the d-axis current control-loop is utilized for the DC-link voltage regulation which results in maximum power production (operation of PV array at MPP voltage). In the case of overfrequency in the network, however, the power setpoint is calculated depending on the network frequency and is applied to the current control scheme, which results in the operation of a PV array with an operating voltage different than the MPP voltage. On the other hand, the reactive power setpoint for PV systems,

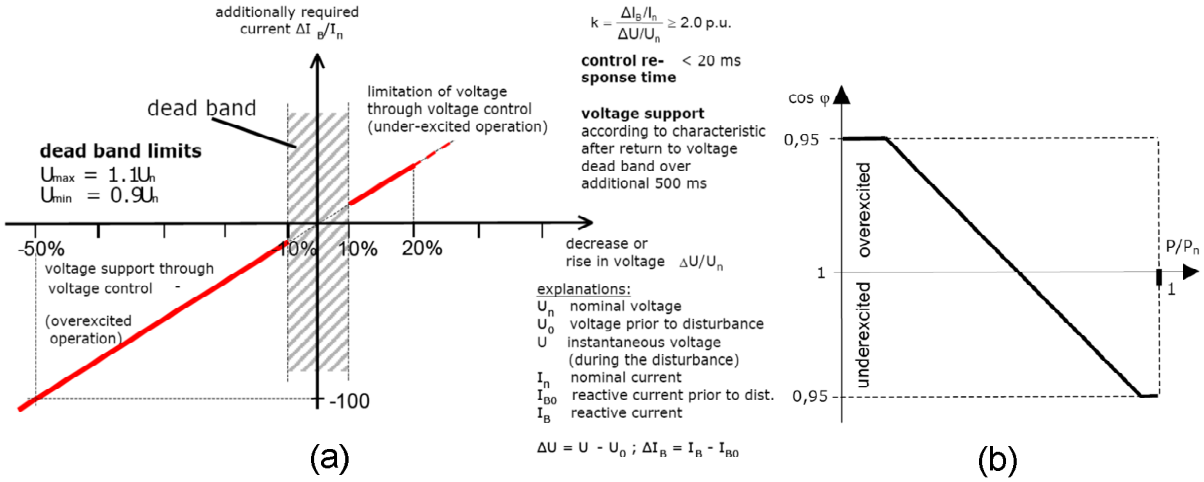

Figure 1.7: (a) Dynamic and (b) static voltage support required from a DG connected at medium-voltage level [39].

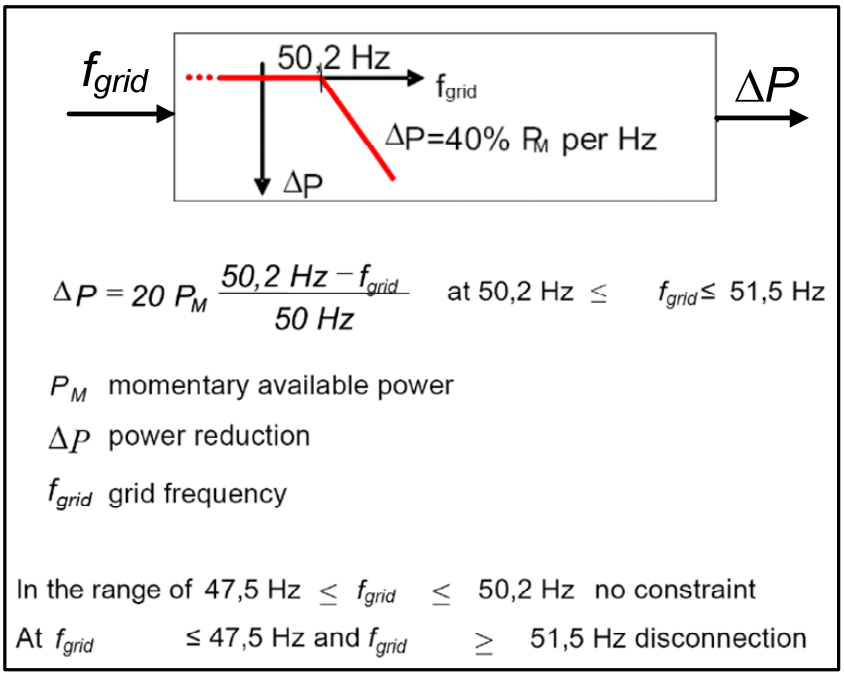

Figure 1.8: Active power control for frequency support required from a DG connected at medium-voltage level [39].

in normal operating condition, is set to zero or an small value to deliver unity power factor at the network connection point. However, in case of required dynamic or static voltage support, the reactive power setpoint is calculated accordingly, depending on the network voltage [40].

Temporary Overvoltage Problem:

Overvoltages in the power system can damage the utility equipment, customer loads (especially the single-phase ones), the DG itself, and the other DGs connected to the same network. There are several sources of overvoltages [42], [43]. Lightning strike is one of them, where the employment of surge arresters has been almost the only solution practiced so far to prevent its severe damage [44], especially at high voltage (HV) and medium voltage (MV) levels. Resonant overvoltages, including series resonance and ferroresonance, is another group of overvoltages faced mostly by induction and synchronous generators, where the power-factor-correction capacitors are also utilized [45]. Switching overvoltage, which is produced when a capacitor bank is switched on/off or when a breaker in an inductive line is opened, is another type of overvoltage in power systems and can be mitigated by appropriate switching mechanisms [46]. Another group of overvoltages, sometimes referred to as islanding overvoltage or ground-fault overvoltage, is produced in power lines hosting DGs and typically is the most severe when a single line-to-ground (SLG) fault incident is followed by islanding. This kind of TOV which is supplied by distributed generators in power systems, is hereafter referred to as the "DG-induced TOV".

While an old problem, the TOV problem, especially those imposed by PV systems and other inverter-based DGs, has recently gained more research attention. The reason is the increasing number of TOV occurrence in the network because of the increasing number of DGs connected to the network, especially at the connection points at medium voltage and low voltage (LV) distribution levels. The possibility of faults and islanding, which are the two contributing factors to the more severe DG-induced TOV cases [47], are high at the distribution LV and MV levels compared to the transmission HV level.

Reference [48] conducted a field test in which the effects of the DG-induced TOV were studied for several commercial inverters from different manufacturers. The authors reported phase-to-neutral TOV levels up to 3.58 $p.u.$ and TOV damages to revenue meters and other electronic devices for most of the tested inverters.

The most severe DG-induced TOV, as stated earlier, is produced when a SLG fault incident, in a feeder/line which has one or several DGs connected in parallel with the power system, is followed by an islanding of the DG with the fault source and a small local load. The islanding results from detection of the fault by the substation protection devices and by opening of the breaker or recloser, as shown in Figure 1.9. A similar scenario can happen in LV distribution lines when a SLG fault takes place between the

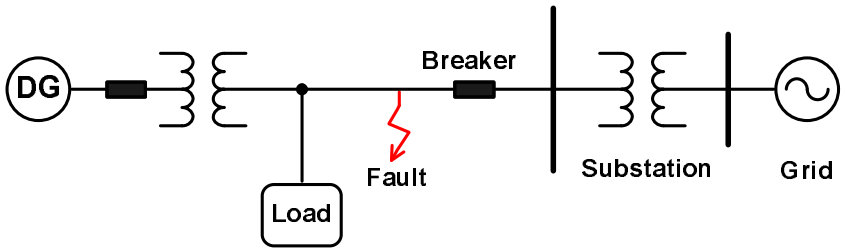

Figure 1.9: Schematic diagram of a typical DG interconnection with utility network.

DG interface transformer and a distribution step-up (from DG point of view) transformer.

Two mechanisms were discussed in the literature as bearing most of the responsibility for the formation of the aforementioned DG-induced TOV [42, 49, 50]. One mechanism is the neutral voltage displacement or neutral point shifting, which happens in delta-connected systems and wye-connected ones which are either ungrounded or grounded through a rather large impedance. As shown in Figure 1.10, when a SLG fault occurs, for instance at phase C, the neutral point assumes a potential equal to the potential of the faulted phase, so the single-phase loads connected between healthy phase A or B and neutral are subject to overvoltage up to 1.73 *p.u.* [51] (or even higher, up to 1.82 *p.u.*, when the network maintains an acceptable pre-fault voltage of 1.05 *p.u.*).

Another mechanism is the interruption of significant power export, where the power flow from DG to the grid is interrupted by a switch opening, and the DG is left islanded with an aggregate load with (much) smaller power consumption than the power produced by DG. Inverter-based DGs behave like a current source, so when the DG is islanded with a smaller aggregate load, the voltage of the island increases according to Ohm's Law [refer to Figure 1.9]. Based on the following equations, the TOV level, V_{TOV}, is proportional to the ratio of the DG's power output, S_{DG}, and the load power consumption, S_{load} [49].

$$V_{TOV} = I_{DG}.Z_{load} \simeq \left(\frac{S_{DG}}{V_{nom}}\right)\frac{V_{nom}^2}{S_{load}} \tag{1.1}$$

$$\frac{V_{TOV}}{V_{nom}} \simeq \frac{S_{DG}}{S_{load}} \tag{1.2}$$

Equation (1.2) provides an approximate value of the TOV amplitude when there is no fault in the island. If there is a SLG fault within the island, the TOV on the unfaulted phases will be more severe (with amplitude up to 150%).

Other mechanisms are also introduced in [49] and [50], including the ground potential rise (GPR) (which results from the finite conductivity of the physical ground connection),

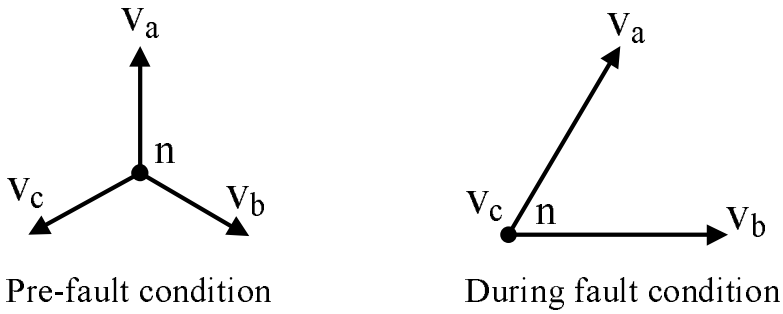

Figure 1.10: Voltage phasor diagram showing neutral voltage displacement during a SLG fault incident.

interruption of inductive currents, and inductive coupling between the faulted and unfaulted phases. The inductive coupling mechanism, which is important in induction and synchronous generators, has the least importance for inverter-based DGs due to their limited short-circuit current capacity.

To address the neutral voltage displacement, utility companies require "effective grounding" of the grid-connected DGs, which is defined by IEEE 142 [52] and is achieved through a four-wire multigrounded connection, the dominant power distribution network connection in North America. The effects of different DG interconnection transformer configurations on TOV were discussed in references [53] and [54].

References [47] and [49], however, challenge the "effective grounding" requirement for the inverter-based DGs by reasoning that it introduces a ground path for the zero-sequence currents resulted from unbalanced and nonlinear loads in normal operating conditions, which increase the power loss in the DG transformer, and a fault current source during SLG fault conditions, which can endanger the transformer and desensitize the protection facilities operation. Furthermore, reference [49] concludes that the interruption of significant power export is the main reason for the overvoltage produced by inverter-based DGs and that no neutral voltage displacement is involved since inverters act like a current source and do not maintain a special relationship between phase-to-phase voltages similar to what rotating machines do; thus, the effective grounding can not mitigate the produced TOV.

1.3 Major Contributions

The following are the most significant contribution of this thesis:

- A two-MPPT structure for centrally configured PV systems is proposed to reduce

the mismatch power loss over the PV array during partial shading, modules' aging, and characteristic mismatch conditions, which improves the energy yield of the entire PV system.

- The thesis then proposes a single-stage three-phase (still centrally configured) PV system that, utilizing an interface, applies the two-MPPT structure to the central inverter, and thus, features an enhanced maximum power point tracking capability, and an improved energy yield under partial shading conditions. Further, the proposed PV system can effectively double the maximum permissible DC voltage of a grounded conventional single-stage PV system, with no need for insulators, fuses, disconnects, and switchgear of a higher voltage class, with respect to safety/insulation standards or common system integration practices exercised for conventional grounded single-stage PV systems. The proposed PV system is realized through the parallel connection of an auxiliary half-bridge converter to the DC link of a conventional single-stage PV system and, therefore, is also an option for retrofit applications.

- The thesis further proposes a two-stage PV system (for large-scale grid-connected applications) which consists of multiple DC-DC boost converters and one large central inverter. The inverter is based on the NPC technology with a grounded DC-link midpoint. This enables a bipolar structure and doubles the net DC voltage, while the 600 V North American standard is respected. The boost converters independently control the DC voltages of their corresponding PV arrays, while their output voltages are regulated by the inverter. Further, they limit the DC-link voltage of the inverter if the power cannot be dispatched to the grid, for example, due to network faults or failure of the inverter. The proposed PV system also offers an enhanced MPPT performance and energy yield, due to its multi-MPPT capability. The NPC technology permits the employment of low-voltage switches for the inverter, despite the doubled net DC voltage.

- The thesis also studies the impact of power mismatch between the two DC sources on the performance of the inverter and develops a mathematical model for the calculation of the inverter mid-point current and its harmonic components, for three different pulse-width modulation (PWM) strategies. The mathematical model of NPC inverter can be found in literature for its conventional applications where it is utilized in connection with one single DC source and the two partial DC voltages

are obtained by a capacitive voltage divider. However, for the special application of NPC inverter in this thesis, where it is supplied by two independent DC sources, the model should be rederived.

- Finally, a TOV mitigation technique is proposed in this thesis to limit the magnitude of the damaging TOV generated by inverter-based DGs (including PV), when a single line-to-ground fault, followed by islanding, takes place in the network. This technique proposes a slight modification in the control structure of the voltage-sourced inverter and utilizes a four-leg inverter connected to grid through a Y/YG isolation transformer, in order to control the overvoltage of each individual phase.

1.4 Thesis Outline

The thesis is organized in six chapters as following:

In this chapter, an introduction to the subject and a literature review of the related works together with the research objectives and the major contributions of the thesis were outlined.

In Chapter 2, the issues related to the array part of a PV system are considered. A PV array model is developed and the effect of common array interconnection configurations on the mismatch power loss resulted from partial shading is studied. Then, a two-MPPT structure is proposed to mitigate the mismatch power loss. A new criterium for the array configurations performance comparison is also defined in that chapter.

Then, in Chapter 3, a single-stage two-level three-phase voltage-sourced inverter, which utilizes the two-MPPT structure to enhance the energy yield, is proposed. This inverter is also bipolar and doubles the DC-link voltage to improve the inverter capacity. The proposed PV system is realized through the parallel connection of an auxiliary half-bridge converter to the DC link of a conventional single-stage PV system. The principles of operation, mathematical modeling, and control schemes are presented and the performance and robustness of the proposed system are demonstrated for faulted as well as normal operating conditions by time-domain simulation studies conducted on a detailed switched model.

In Chapter 4, a bipolar two-stage three-level inverter is proposed to further improve the inverter capacity. The DC-DC converter fixes the variable voltage of the PV array to a voltage slightly less than the maximum permissible voltage, so the inverter performs

its DC-AC conversion task at the maximum possible voltage which results in a reduced power loss. The inverter utilizes NPC inverter which improves the power quality and permits the employment of low-voltage switches for the inverter, despite the doubled net DC voltage. Some technical problems such as potentially large mid-point DC current in case of partial shading, third-order harmonic ripples of partial DC-side voltages, and the DC-link voltage control in case of incidents like severe network fault are addressed in this chapter and appropriate solutions are given.

To design the controller schemes and strategies for the two-stage three-level NPC-based PV system, the mathematical model of the DC side of the NPC inverter is derived in Appendix A, for this unique application condition in which the two DC power sources connected to NPC inverter are not identical. In that appendix, the effect of different PWM strategies on the third-order harmonic ripples of the partial DC voltages are also investigated.

In Chapter 5, the temporary overvoltage problem in the power networks hosting distributed generators are discussed and a TOV mitigation technique is proposed. This technique utilizes a four-leg inverter connected to grid through a Y/YG isolation transformer with a slight modification on the control structure of the inverter. This technique prevents the formation of any overvoltage on any of the three phases. Another TOV mitigation technique is also proposed for the conventional three-leg inverter connected through widely utilized Δ/YG isolation transformer to reduce the magnitude of the TOV.

Finally, a summary of the thesis together with the suggestions for the future research subjects are presented in Chapter 6. The system parameters, used for the analysis and simulation of the proposed systems in this thesis, are listed in Appendices B, C, D, and E.

Chapter 2

PV Array Configuration

2.1 Introduction

In this chapter, the mismatch power loss problem in PV systems, which is caused by partial shading, PV panels' aging and characteristic mismatch, and/or snow/dust/debris on PV panels, is studied and a two-MPPT structure is proposed to mitigate the power loss. The mismatch power loss is dependent of both the whole PV system structure, being configured in central, string, multi string, or AC module structures, and the array interconnection type.

In this study, a model of a PV array is developed and the mismatch power loss in two main array interconnection structures, SP and TCL, are compared under different shading scenarios. Then, a two-MPPT structure, which splits the entire array into two sub-arrays and facilitates independent maximum power point tracking for each sub-array, is proposed and its performance is evaluated under the defined shading scenarios. For that purpose, a single-diode model of a commercial PV panel is developed and utilized in simulations with PSCAD/EMTDC software [55].

2.2 Shading and the Proposed Two-MPPT Strategy

Figure 2.1(a) illustrates a schematic diagram of an example SP-configured PV array, which consists of a number of parallel-connected strings of series-connected PV modules. In a conventional single-stage PV system, the array is interfaced with the grid, through an electronic power converter (not shown in Figure 2.1(a)), from terminals A and B. Thus, the converter enables MPPT by controlling the (dc) array voltage, V_{AB}. The SP

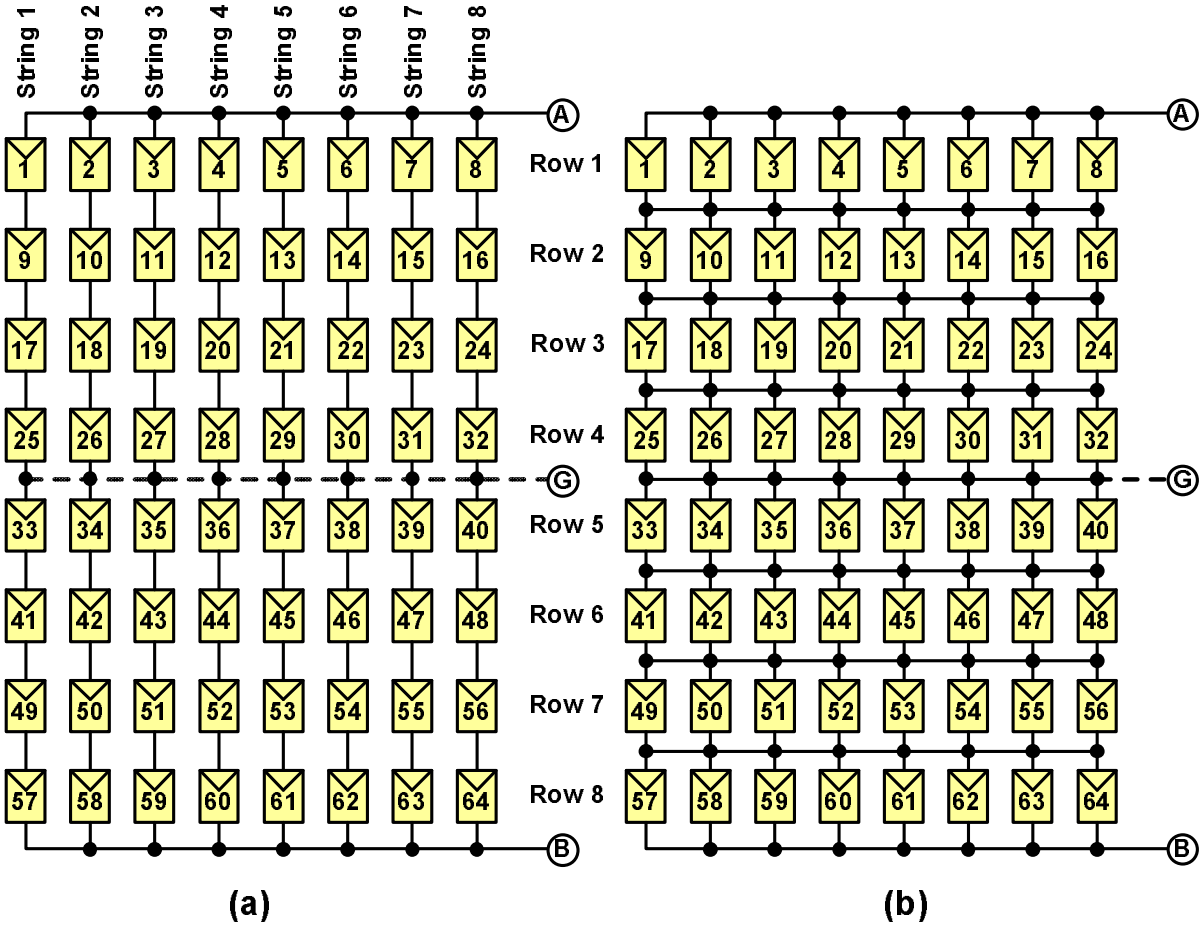

Figure 2.1: Schematic diagrams of a 64-module PV array, based on (a) SP configuration, and (b) TCT configuration. The dashed line in each configuration indicates the connection path for the proposed two-MPPT scheme.

configuration of Figure 2.1(a), although effective under a normal condition, exhibits a remarkable maximum-power drop if the array is exposed to an uneven solar irradiation, due, for example, to partial shading. To mitigate the effect of partial shading and the consequent maximum-power drop, the configuration of Figure 2.1(a) can be modified to that of Figure 2.1(b), known in the literature as the TCT configuration [16,17], in which the strings are also cross-connected; again, in a conventional single-stage PV system, the entire TCT array is interfaced with, and undergoes MPPT, by one power-electronic converter, from terminals A and B.

This section demonstrates that, the maximum-power drop of the configuration of Figure 2.1(b) can be further mitigated if the array is divided into two sub-arrays through the introduction of a center terminal, that is, terminal G [Figure 2.1(b)], such that each

sub-array independently undergoes MPPT through the control of the voltages V_{AG} and V_{GB}. Once this fact is established, in next Chapter a power-electronic converter system is introduced that enables the proposed two-MPPT strategy.

2.2.1 Shading Scenarios

For the study reported in this chapter, 1, 2, or 4 PV modules of the arrays of Figure 2.1(a) or Figure 2.1(b) are assumed to be shaded. Thus, a model of an 8×8 array of 64 PV modules, configured in the ways shown in Figure 2.1(a) and Figure 2.1(b), is constructed in the PSCAD/EMTDC software environment, and a number of shading scenarios are judiciously selected, simulated, and compared in terms of their maximum-power drops. As detailed in section 2.3, each module is a lumped representation of (M_s =) 54 series-connected identical basic PV cells and assumed to include one anti-parallel (bypass) diode for every 18 (series-connected) cells. Further, it is assumed that each shaded module receives a solar irradiation of 0.2 kW/m^2, one-fifth of the solar irradiation received by an unshaded module, that is, 1.0 kW/m^2.

For the one-MPPT scheme, the maximum power of the array is measured from terminals A and B, while terminal G is left untapped [see Figs. 2.1(a) and 2.1(b)]; for the two-MPPT scheme, however, the maximum powers of both sub-arrays are measured, from the terminals A-G and G-B, and summed up. The maximum power of, whether an array or a sub-array, is found by sweeping the corresponding terminal voltage, from a small value to a relatively large value.

For the TCT configuration, the following scenarios are simulated:

- Scenario #1: Only one module is shaded.
- Scenario #2: Two modules in different sub-arrays are shaded.
- Scenario #3: Two modules of a sub-array, but in two different rows, are shaded.
- Scenario #4: Two modules of a row are shaded.
- Scenario #5: A 2×2 block of four modules, all in one sub-array, is shaded.
- Scenario #6: A 2×2 block of four modules is shaded. However, unlike Scenario #5, two modules are located in one sub-array, whereas the other two lie in the other sub-array.

For the SP configuration, the shading scenarios are as follows:

- Scenario #7: Only one module is shaded.
- Scenario #8: Two modules of different sub-arrays and strings are shaded.
- Scenario #9: Two modules of a sub-array, but in different strings, are shaded.
- Scenario #10: A 2×2 block of four modules, all in one sub-array, is shaded.
- Scenario #11: A 2×2 block of four modules is shaded. However, unlike Scenario #10, two modules are located in one sub-array, whereas the other two lie in the other sub-array.

The abovementioned shading scenarios are chosen strategically. For the TCT configuration, the shading of a module results in a comparatively smaller current output and, thus, forces the other modules of the host row to produce slightly larger currents, such that the aggregate current delivered by the row equals the current output of each unshaded row; thus, the shaded module causes only a slight change to the operating points of the unshaded modules and, therefore, the overall maximum-power drop is fairly small. However, as the number of shaded modules in a row increases, the deviation of the array maximum-power from its value under a normal condition becomes larger, and the maximum-power drop increases disproportionately; these anticipations have been the main motivations behind Scenarios #3 and #4. Similarly, in the SP configuration, the existence of two or more shaded modules in one string results in a disproportionate increase in the maximum-power drop. Therefore, Scenario #8, which accounts for one shaded module per sub-array, and Scenario #9, which accounts for two shaded modules in one sub-array, were considered.

It should be noted that Scenarios #5, #6, #10, and #11 enable studying the impact of a more widespread shadow that simultaneously covers four modules in a 2×2 block. These scenarios take into account the combined effect of both series- and parallel-connected shaded modules.

2.2.2 Maximum-Power Drop Ratio

To characterize the performance of a PV array configuration under partial shading, a number of criteria have been introduced in the technical literature. These include the maximum power output of the shaded array [17, 56], the ratio of the maximum power output of the shaded array to the maximum power output under a normal condition [8],

and the ratio of the drop in the maximum power output of the shaded array to the maximum power output under a normal condition [16]. The aforementioned criteria, however, depend on the shaded area and number of shaded modules and, therefore, may not fully characterize the susceptibility of the configuration under study to partial shading. Thus, an alternative criterion, referred hereafter to as the "maximum-power drop ratio (MPDR)", is defined in this paper, as

$$\text{MPDR} = \frac{\text{Maximum-Power Drop of the Array}}{\text{Maximum-Power Drop of the Base System}}. \tag{2.1}$$

In (2.1), the base system is defined as a hypothetical n-module/n-converter PV system in which each module is independently controlled by one corresponding converter. To appreciate the usefulness of the MPDR, let us consider the case in which one module of the base system is shaded and, consequently, exhibits a maximum-power drop. In view of the independence of the modules in the base system, the maximum-power drop experienced by the overall array is the same as that experienced by the shaded module, and the MPDR is unity; intuitively, one finds the base system to be the most superior system in terms of the performance under partial shading, but, most likely, not economical or desirable from the system integration viewpoint. Alternatively, let us consider a general configuration in which the number of converters is lower than the number of modules, and that the shaded module is connected in series and/or in parallel with a number of other modules. In this configuration, the shaded module also affects the operating points of the other (unshaded) modules and, as such, will cause a maximum-power drop in them. Consequently, the array maximum-power drop in the general system is expected to be larger than that experienced by the base system, and the MPDR is therefor larger than unity. The forgoing example indicates that, the MPDR provides a measure of closeness of a PV system to the base system, in terms of the susceptibility to characteristic mismatch and partial shading. The MPDR can also be interpreted in the way that, a shaded module results in an array maximum-power drop that is, in general, several times larger than that of the shaded module on its own.

2.3 PV Module Model

Figure 2.2 illustrates a schematic diagram of the model employed in this study for simulating a PV array (sub-array). The model represents the aggregate effect of N_p parallel-

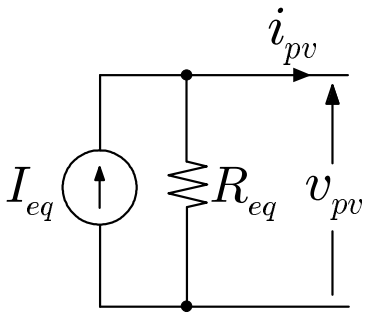

Figure 2.2: Circuit diagram of the PV array model employed for simulations.

connected strings of N_s series-connected identical PV modules; hereafter, each module in the set is referred to as "*the PV module*" and assumed to consist of M_s series-connected basic PV cells.

In the model of Figure 2.2, the Norton current source and resistance are formulated as

$$I_{eq} = N_p \left(\frac{R_p}{R_s + R_p} \right) I_i, \tag{2.2}$$

$$R_{eq} = \frac{N_s}{N_p} \left(R_s + R_p \right), \tag{2.3}$$

where the resistances R_s and R_p embed the aggregate effects of several structural resistances of *the PV module*, and the impact of the leakage current of the *p-n* junctions constituting *the PV module*. The model, referred in the literature to as the single-diode model, is governed by the following equations [57]. I_i is formulated as

$$I_i = I_g - I_o \left\{ exp \left[\frac{\beta(v_{pv} + R_s i_{pv})}{a} \right] - 1 \right\}, \tag{2.4}$$

where $exp(.)$ denotes the exponential function; i_{pv} and v_{pv} are, respectively, the terminal current and voltage of *the PV module*; I_g is a light-dependent current component; a is the diode ideality factor, and of a value typically in the range from 1 to 1.5; I_o is the (temperature-dependent) reverse saturation current of a *p-n* junction; and β is the so-called inverse thermal voltage, which is defined as

$$\beta = \frac{q}{M_s k \vartheta}, \tag{2.5}$$

where k is Boltzmann's constant ($1.3806503 \times 10^{-23}$ J/K), q is the electron charge

($1.60217646 \times 10^{-19}$ C), M_s is the number of series-connected PV cells, and ϑ is the p-n junction temperature in K.

I_g is a linear function of the solar irradiation S, and also depends on ϑ, as

$$I_g \simeq \left[I_{sc,n} + k_{I_{sc}} \left(\vartheta - \vartheta_n\right)\right] \left(\frac{S}{S_n}\right), \tag{2.6}$$

where $k_{I_{sc}}$ is the temperature coefficient of *the PV module* short-circuit current, and $I_{sc,n}$, S_n, and ϑ_n, respectively, denote the nominal values of the short-circuit current, solar irradiation, and junction temperature of *the PV module*. Similarly, *the PV module* open-circuit voltage, V_{oc}, is formulated as

$$V_{oc} \simeq V_{oc,n} + k_{V_{oc}}(\vartheta - \vartheta_n), \tag{2.7}$$

where $V_{oc,n}$ signifies the nominal value of the open-circuit voltage of *the PV module*, and $k_{V_{oc}}$ is the temperature coefficient of *the PV module* open-circuit voltage.

Equation (2.4) must hold for all operating points, including the open-circuit operating point at the nominal solar irradiation, represented by $v_{pv} = V_{oc}$, $i_{pv} = 0$, and $S = S_n$. Thus, based on (2.6) and (2.7), one deduces

$$I_o = \frac{I_{sc,n} + k_{I_{sc}}(\vartheta - \vartheta_n)}{exp\left[\beta\left(\frac{V_{oc,n} + k_{V_{oc}}(\vartheta - \vartheta_n)}{a}\right)\right] - 1}. \tag{2.8}$$

2.4 Simulation Results

A PV array model is prepared in PSCAD/EMTDC software using the formulas developed in the previous section, in order to measure the power output of the two PV arrays shown in Figure 2.1 under different shading scenarios defined in section 2.2.1; the parameters of the PV module used in this simulation are presented in Appendix B. Table 2.1 provides a summary of the study results, reporting the maximum power of the arrays, under both the one- and two-MPPT schemes, for each aforementioned scenario. For each scenario and scheme, Table 2.1 also reports the corresponding MPDR, with reference to a 64-module base system, while Figs. 2.3 and 2.4 provide a graphical illustration of the study results.

Figure 2.3 indicates that, for the TCT configuration the MPDR under the two-MPPT scheme is always smaller than, or at most equal to, the MPDR under the one-MPPT scheme. For example, in Scenario #1 where only one module is shaded, the operating

Table 2.1: MP and MPDR for Different Scenarios and MPPT Schemes

Scenario	Configuration	Modules Shaded	Scheme	Array Maximum Power (W)	MPDR
1	TCT	#1	1-MPPT	11696.8	2.22
			2-MPPT	11772.3	1.72
2	TCT	#1, 60	1-MPPT	11513.8	1.72
			2-MPPT	11513.8	1.72
3	TCT	#1, 30	1-MPPT	11513.8	1.72
			2-MPPT	11629.3	1.34
4	TCT	#1, 2	1-MPPT	10882.7	3.82
			2-MPPT	11321.2	2.36
5	TCT	#2, 3, 10, 11	1-MPPT	10611.7	2.36
			2-MPPT	11109.7	1.53
6	TCT	#26, 27, 34, 35	1-MPPT	10611.7	2.36
			2-MPPT	10611.7	2.36
7	SP	#1	1-MPPT	11568.7	3.07
			2-MPPT	11441.4	3.92
8	SP	#1, 60	1-MPPT	11253.5	2.58
			2-MPPT	10851.9	3.92
9	SP	#1, 30	1-MPPT	11253.5	2.58
			2-MPPT	10893.7	3.78
10	SP	#2, 3, 10, 11	1-MPPT	9756.6	3.78
			2-MPPT	10845.5	1.97
11	SP	#26, 27, 34, 35	1-MPPT	9756.6	3.78
			2-MPPT	9756.6	3.78
Reference Unshaded 8×8 Array				12030.9	-

point of the entire array is affected in the one-MPPT scheme; however, when the two-MPPT scheme is employed, the operating point of only half of the array is affected by the shaded module, whereas the other sub-array produces its normal maximum power. In Scenario #2 where two modules in different sub-arrays are shaded, the one- and two-MPPT schemes perform identically. In Scenarios #3 and #4 where the two shaded modules are located in the same sub-array, again the two-MPPT scheme is superior, since only the operating point of one sub-array is affected by the shaded modules. The reason for the larger maximum-power drop in Scenario #4, compared to Scenario #3, is explained by the fact that an increased number of shaded modules in a row results in a fairly large deviation of the operating point of the row. In Scenarios #5 and #6, to study a more realistic shading condition, a 2×2 block of 4 shaded modules is moved around within the array, to include both parallel- and series-connected modules. In Scenario #5

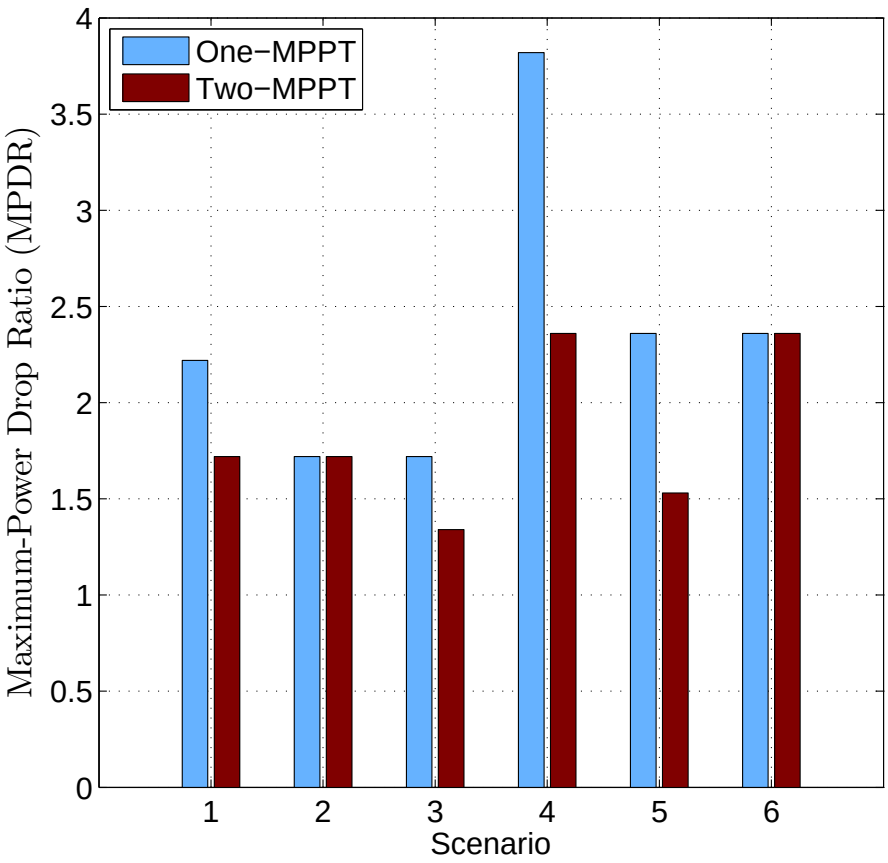

Figure 2.3: MPDRs under the one- and two-MPPT schemes for the TCT configuration.

where all the shaded modules are located in one sub-array, the two-MPPT scheme is more effective, whereas in Scenario #6 in which the shaded block is equally shared by both sub-arrays, the MPDRs of the one- and two-MPPT schemes are equal.

For the (conventional) one-MPPT scheme, the superiority of the TCT configuration over the SP configuration has already been reported in the literature [16] and [17], and also observed by this study (not discussed). Figure 2.4 indicates that the advantage is preserved under the proposed two-MPPT scheme; as Figure 2.4 shows, for geographically-identical shading scenarios, the MPDR of each shading scenario in the TCT configuration is lower than its counterpart in the SP configuration.

2.5 Conclusion

In this chapter, a model was developed for studying the mismatch power loss in PV arrays resulted from partial shading, modules' aging, and modules's characteristic mismatch.

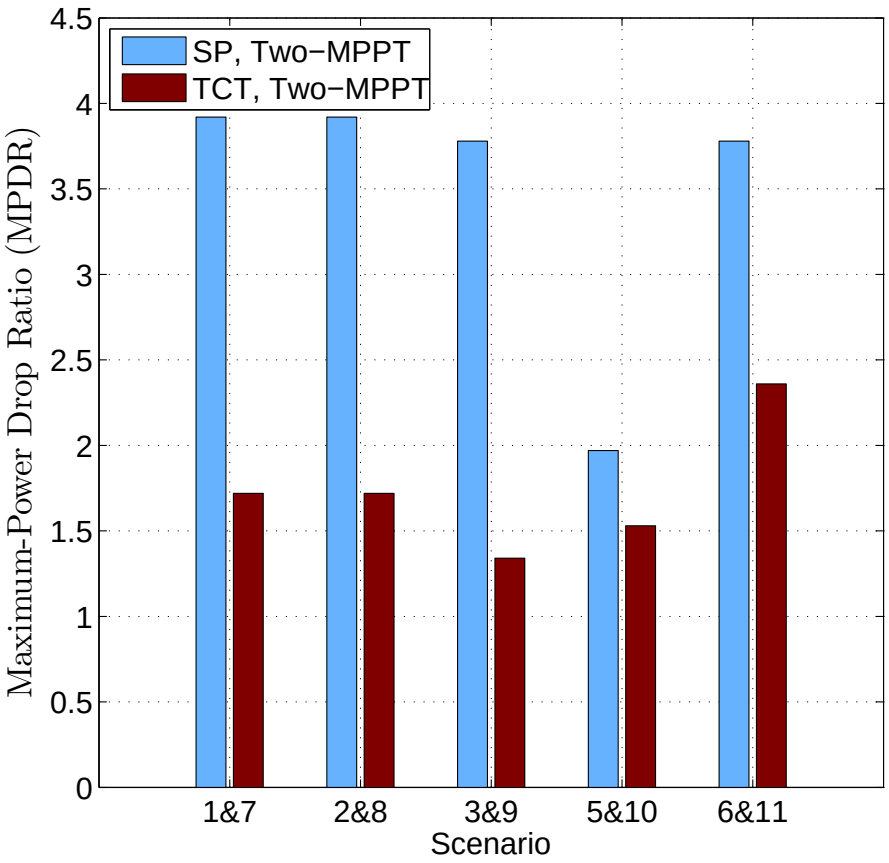

Figure 2.4: MPDRs for the SP and TCT configurations, under the two-MPPT scheme.

The effect of the PV array interconnection configurations was then studied which showed the superiority of the TCT configuration over the SP one. Further, a two-MPPT structure was proposed to reduce the mismatch power loss on the PV array and to improve the whole PV system efficiency. This structure will be utilized in next chapters, together with the proposed inverters, to improve the energy yield of the whole PV system.

Chapter 3

Two-Level Single-Stage Inverter

3.1 Introduction

This chapter proposes a single-stage three-phase PV system that features an enhanced maximum power point tracking capability, through utilizing the two-MPPT structure defined in Chapter 2, and an improved energy yield under partial shading conditions. Further, the proposed PV system can accommodate a DC voltage as large as two times the maximum permissible DC voltage of a conventional grounded single-stage PV system, with no need for insulators, fuses, disconnects, and switchgear of a higher voltage class. Thus, based on the proposed PV system, the power rating of a single-unit, conventional, grounded, single-stage PV system can be doubled, without compromising the prevalent standards for safety/insulation or the common system integration practices; presently, this is commonly achieved by the parallel connection of two independent smaller conventional PV systems. Alternatively, for a given power rating, the proposed PV system is expected to offer a comparatively higher efficiency, due to its increased voltage level and enhanced MPPT capability. The proposed PV system is realized through the parallel connection of an auxiliary half-bridge converter to the DC link of a conventional single-stage PV system and, therefore, can also be an option for retrofit applications.

3.2 Proposed Two-MPPT Single-Stage PV System

3.2.1 Structure and Principles of Operation

Figure 3.1 illustrates a simplified schematic diagram of a conventional single-stage PV system [58]. The kernel of the PV system is a current-controlled voltage-sourced converter

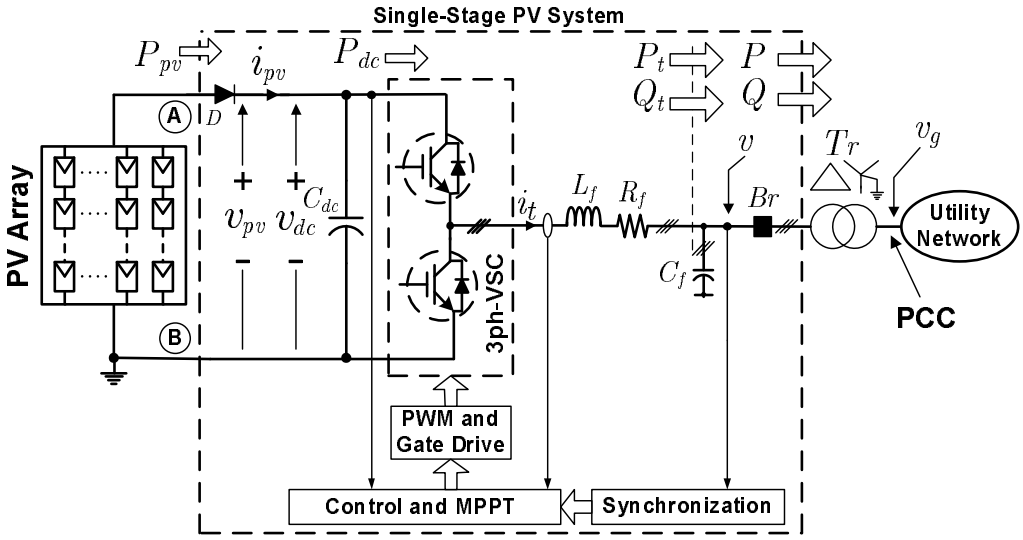

Figure 3.1: Schematic diagram of the conventional single-stage three-phase PV system.

(VSC) that interfaces a PV array with the utility grid. The PV array is connected to the VSC DC side through a series reverse-blocking diode, while the VSC AC side is connected to the grid, at the point of common coupling (PCC), through a three-phase LC filter and a coupling transformer. The reverse-blocking diode prevents current flow from the VSC to the PV array if the solar irradiation is low. The LC filter prevents the switching voltage and current harmonics generated by the VSC from penetrating into the grid. The VSC employs the pulse-width modulation (PWM) switching strategy, and controls the real and reactive power delivered to the grid. This, in turn, makes possible the regulation of the PV array (DC) voltage and enables MPPT. The DC-link capacitor, C_{dc}, provides a low impedance path for the high-frequency components of the VSC DC-side current and, therefore, eliminates the DC-link voltage ripple. As detailed in [58], the control is exercised in a dq-frame that is synchronized to the grid voltage vector, for example, through a phase-locked loop (PLL). The two-MPPT single-stage PV system proposed in this chapter is realized through modifications made on the conventional PV system of Figure 3.1, as explained below.

Figure 3.2 illustrates a schematic diagram of the proposed two-MPPT PV system. As Figure 3.2 shows, the proposed two-MPPT PV system is realized by augmenting the conventional PV system of Figure 3.1 with an auxiliary half-bridge converter. The auxiliary converter consists of a half-bridge transistor leg, a reactor, a shunt capacitive voltage divider, and the two reverse blocking diodes D_1 and D_2. The reactor connects the AC-side terminal of the half-bridge leg to the center point of the capacitive voltage

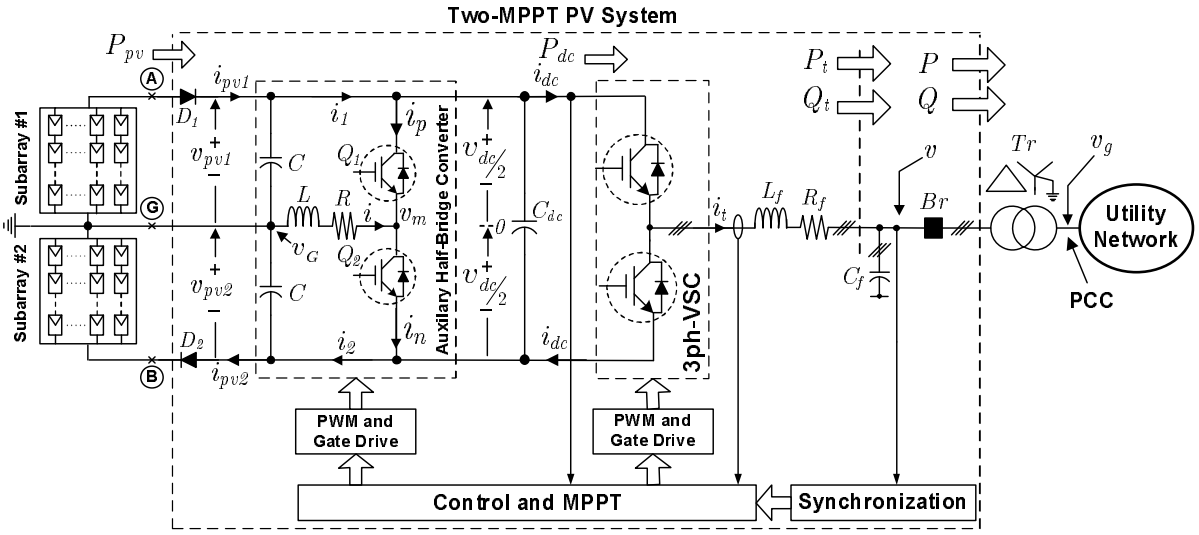

Figure 3.2: Schematic diagram of the proposed two-MPPT, single-stage, three-phase PV system.

divider, which, in turn, is connected to terminal G of the PV array [see also Figs. 2.1(a) and 2.1(b)]. The two transistors of the half-bridge leg are pulse-width-modulated in a complementary manner and control the voltage of terminal G of the PV array; this configuration enables independent control of the voltages v_{pv1} and v_{pv2}, in favor of an enhanced MPPT performance under partial shading conditions, as discussed in Section 2.2. L and R represent the inductance and resistance of the reactor, respectively. The latter also embeds the effect of the on-state resistance of the half-bridge leg transistors. Figure 3.2 indicates that the auxiliary converter can be viewed as a module that sits in parallel with the DC link of the conventional PV system, and also provides the third terminal that is required for the two-MPPT scheme. This feature is attractive in retrofit applications.

The other salient feature of the proposed two-MPPT PV system of Figure 3.2, i.e., apart from its enhanced MPPT capability, becomes apparent in view of the fact that terminal G of the PV array is solidly grounded. This, in turn, means that the DC-link voltage of the proposed two-MPPT PV system can be chosen as two times that of a conventional counterpart, for the same safety and insulation requirements. For example, North-American standards require that the voltage of a PV array be limited to a maximum of 600 V with reference to the ground [59]. In the PV system of Figure 3.1, this requirement translates into a maximum DC-link voltage of 600 V for the VSC, and results in large currents and sub-optimum efficiencies for a high-power PV system [59].

Although the trend is towards adoption of higher voltage levels, e.g. 1000 V, at least for "behind the fence" systems, the limited availability of fuses, disconnects, etc., in the 1000-V voltage class has presented the PV industry with a major challenge in its attempt to quickly move in that direction. By contrast, a maximum voltage of 600 V for each sub-array in the two-MPPT PV system of Figure 3.2 corresponds to a maximum DC-link voltage of 1200 V, that is, the rating of the proposed two-MPPT PV system can be doubled while the existing safety and insulation requirements are nonetheless respected.

It should be noted that the auxiliary half-bridge converter processes only the power difference between the two sub-arrays, not the entire power of them. Thus, the system is still considered as a single-stage system. The rating of the auxiliary half-bridge converter depends on the design criteria. If the system is expected to continue producing power even if one of the sub-arrays is disabled, for maintenance purpose or because of a fault in it, the rating of the auxiliary converter switches will be equal to the rating of the main inverter switches. However, if in an application, the power difference between the two sub-arrays is not expected to be higher than maximum 30% for example, and the auxiliary half-bridge converter is only expected to process that much power difference, the rating of the auxiliary converter switches will be 30% of the rating of the central inverter switches.

3.2.2 Mathematical Model

This subsection formulates a mathematical model for the two-MPPT PV system of Figure 3.2. The model describes the dynamics of the array voltages v_{pv1} and v_{pv2}, and will be employed in Section 3.2.3 for designing the control loops that regulate v_{pv1} and v_{pv2}. In the subsequent developments, all node voltages are expressed with reference to the DC-link virtual midpoint, that is, node "0" in Figure 3.2.

Dynamics of the reactor current, i, are governed by

$$L\frac{di}{dt} = -Ri + (\underbrace{\frac{v_{dc}}{2} - v_{pv1}}_{v_G}) - v_m \ , \tag{3.1}$$

$$L\frac{di}{dt} = -Ri + (\underbrace{-\frac{v_{dc}}{2} + v_{pv2}}_{v_G}) - v_m \tag{3.2}$$

where v_m represents the AC-side terminal voltage of the half-bridge leg. Adding both

sides of (3.1) and (3.2), and dividing the resultant by 2, one deduces

$$L\frac{di}{dt} = -Ri - \frac{1}{2}(v_{pv1} - v_{pv2}) - v_m \ . \tag{3.3}$$

For a pulse-width modulated half-bridge leg, v_m is formulated as

$$v_m = m\frac{v_{dc}}{2} \tag{3.4}$$

where m ($-1 \leq m \leq 1$) is the PWM modulating signal of the half-bridge leg, normalized to the amplitude of a symmetrical, high-frequency, triangular carrier waveform [60]. Thus, (3.3) can be rewritten as

$$L\frac{di}{dt} = -Ri - \frac{1}{2}x_1 - \frac{1}{2}mx_2 \tag{3.5}$$

where $x_1 = v_{pv1} - v_{pv2}$ is the difference between the sub-array voltages, and $x_2 = v_{dc} = v_{pv1} + v_{pv2}$ is the net DC-link voltage.

With reference to Figure 3.2, application of KCL to terminals A and B yields:

$$C\frac{dv_{pv1}}{dt} = i_{pv1} - i_1 \tag{3.6}$$

$$C\frac{dv_{pv2}}{dt} = i_{pv2} - i_2 \ . \tag{3.7}$$

Subtracting (3.7) from (3.6), one finds

$$\begin{aligned} C\frac{dx_1}{dt} &= -i_1 + i_2 + i_{pv1} - i_{pv2} \\ &= i + (i_{pv1} - i_{pv2}) \ . \end{aligned} \tag{3.8}$$

Application of KCL to the node where Q_1 meets the positive rail of the VSC DC link requires that

$$C_{dc}\frac{dx_2}{dt} = i_1 - i_p - i_{dc} \ . \tag{3.9}$$

Similarly, KCL for the node where Q_2 meets the negative rail of the VSC DC link requires that

$$C_{dc}\frac{dx_2}{dt} = i_2 - i_n - i_{dc} \ . \tag{3.10}$$

Adding both sides of (3.9) and (3.10), one obtains

$$2C_{dc}\frac{dx_2}{dt} = (i_1 + i_2) - (i_p + i_n) - 2i_{dc} \ . \tag{3.11}$$

On the other hand, adding both sides of (3.6) and (3.7) results in

$$i_1 + i_2 = -C\frac{dx_2}{dt} + (i_{pv1} + i_{pv2}) \ . \tag{3.12}$$

Substituting for $i_1 + i_2$ in (3.11), from (3.12), one deduces

$$(2C_{dc} + C)\frac{dx_2}{dt} = (i_{pv1} + i_{pv2}) - (i_p + i_n) - 2i_{dc} \ . \tag{3.13}$$

The currents through the upper and lower transistors of the half-bridge leg are formulated as [60]

$$i_p = -\left(\frac{1+m}{2}\right) i \tag{3.14}$$

$$i_n = \left(\frac{1-m}{2}\right) i \ . \tag{3.15}$$

Therefore, based on (3.14) and (3.15), $i_p + i_n = -mi$ and (3.13) can be rewritten as

$$\big(\underbrace{C_{dc} + \frac{C}{2}}_{C_e}\big)\frac{dx_2}{dt} = \frac{1}{2}(i_{pv1} + i_{pv2}) + \frac{1}{2}mi - i_{dc} \tag{3.16}$$

where $C_e = C_{dc} + C/2$ is hereafter referred to as the effective DC-link capacitance. The VSC DC-side current, i_{dc}, can in turn be expressed in terms of the real power that leaves the VSC AC side, that is, P_t [Figure 3.2]. Thus, $i_{dc} \approx P_t/v_{dc} = P_t/x_2$, and (3.16) can be rewritten as

$$C_e\frac{dx_2}{dt} = \frac{1}{2}(i_{pv1} + i_{pv2}) + \frac{1}{2}mi - \frac{1}{x_2}P_t \ . \tag{3.17}$$

v_{pv1} and v_{pv2} are expressed in terms of x_1 and x_2, as $v_{pv1} = (x_1 + x_2)/2$ and $v_{pv2} =$

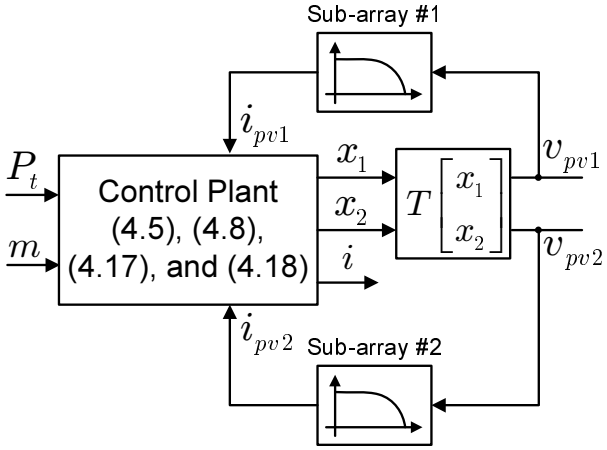

Figure 3.3: Block diagram of the system representing the dynamics of v_{pv1} and v_{pv2}.

$(-x_1 + x_2)/2$, which can be rewritten in the following matrix form:

$$\begin{bmatrix} v_{pv1} \\ v_{pv2} \end{bmatrix} = \underbrace{\begin{bmatrix} 0.5 & 0.5 \\ -0.5 & 0.5 \end{bmatrix}}_{T} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}. \tag{3.18}$$

Equations (3.5), (3.8), (3.17), and (3.18) constitute a state-space model for a nonlinear control plant for which m and P_t are the inputs, v_{pv1} and v_{pv2} are the outputs, and x_1, x_2, and i are the state variables; the control objective for this plant is to regulate v_{pv1} and v_{pv2} at their respective reference values, v^r_{pv1} and v^r_{pv2}, which are in turn determined by the MPPT schemes of Sub-array #1 and Sub-array #2, respectively. The control strategy and loops required to fulfill this objective are presented in the next subsection. Figure 3.3 illustrates a block representation of the described control plant.

3.2.3 Net and Differential DC-Link Voltage Controller

The control plant represented by (3.5), (3.8), (3.17), and (3.18) is a multi-input-multi-output (MIMO), nonlinear system and as such inherently difficult to control. Therefore, as discussed in the subsequent subsections, a combination of feed-forward and decoupling compensation techniques are employed to overcome the complications. The overall control task is managed by three distinct control loops: The first control loop is a current-control loop, based on (3.5), that regulates the reactor current i at its reference value i^r. The second control loop regulates the difference between the sub-array voltages, $x_1 = v_{pv1} - v_{pv2}$, based on (3.8) and in view of the fact that i is controlled by the first

loop. The third control loop regulates the DC-link net voltage, i.e., $x_2 = v_{dc} = v_{pv1} + v_{pv2}$, through the control of P_t, that is, the power that leaves the VSC AC-side terminals; this control loop is based on (3.17). The overall control system will have two reference commands, x_1^r and x_2^r, which are determined based on (3.18) from the reference commands v_{pv1}^r and v_{pv2}^r; these, in turn, are received from the MPPT schemes of Sub-array #1 and Sub-array #2, respectively. The assumption here is that, in addition to i, the sub-array currents (i_{pv1} and i_{pv2}) and voltages (v_{pv1} and v_{pv2}) are measured. The measurements are required, not only for the control, but also for independent MPPT of the two sub-arrays.

Reactor Current-Control Loop

The first control loop, illustrated in Figure 3.4, is the reactor current-control loop whose function is to regulate i at its reference value, i^r. The regulated current, in turn, will appear as an input to the control loop that regulates the voltage difference between the two sub-arrays. As (3.5) suggests, i can be controlled by the modulating signal m, while x_1 and x_2 are considered as undesirable inputs. Let m be determined based on the control law

$$m = \frac{-u_i - \frac{1}{2}x_1}{\frac{1}{2}x_2} \tag{3.19}$$

where u_i is a dummy control signal. Then, substituting for m from (3.19) into (3.5), one finds

$$L\frac{di}{dt} = -Ri + u_i \ . \tag{3.20}$$

Equation (3.20) represents a first-order system for which u_i and i are the input and the output, respectively. Let u_i be provided by a proportional-integral (PI) compensator,

$$K_i(s) = \frac{k_1 s + k_2}{s} \tag{3.21}$$

for which k_1 and k_2 are the proportional and integral gains, respectively. Then, if k_1 and k_2 are chosen as

$$k_1 = \frac{L}{\tau_i} \tag{3.22}$$

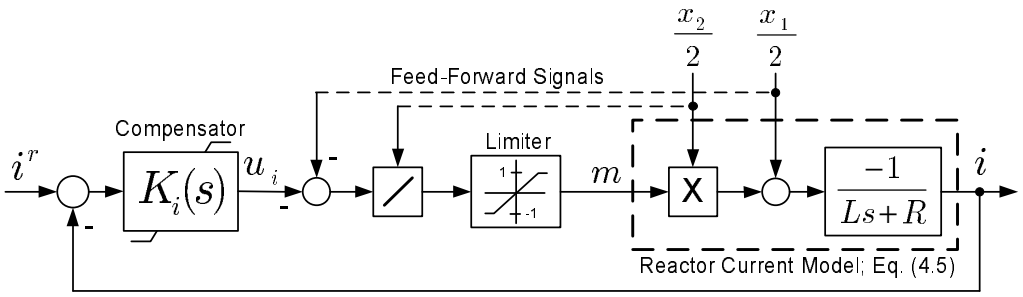

Figure 3.4: Block diagram of the reactor current-control loop.

and

$$k_2 = \frac{R}{\tau_i} \,, \tag{3.23}$$

one finds the following closed-loop transfer function

$$G_i(s) = \frac{I(s)}{I^r(s)} = \frac{1}{\tau_i \; s + 1} \tag{3.24}$$

in which the time constant τ_i is chosen to be a small value, subject to the limitations imposed by the inductance of the reactor and the switching frequency of the half-bridge leg.

Differential DC-Link Voltage Controller

The second control loop is based on (3.8), receives i^r as the control input, and regulates $x_1 = v_{pv1} - v_{pv2}$ as the output; for this control loop, the sub-arrays current difference, $i_{pv1} - i_{pv2}$, is the disturbance input. Figure 3.5 illustrates a block diagram of the second control loop, in which a measure of $i_{pv1} - i_{pv2}$ is included as a feed-forward signal, to improve the transient response of the closed loop system. Thus, i^r is calculated as

$$i^r = u_d - (i_{pv1} - i_{pv2}) \tag{3.25}$$

where u_d is the output of a compensator, $K_d(s)$. If a fast current control is assumed, i^r can be approximated by i in (3.25), and (3.8) is rewritten as

$$C\frac{dx_1}{dt} = u_d \tag{3.26}$$

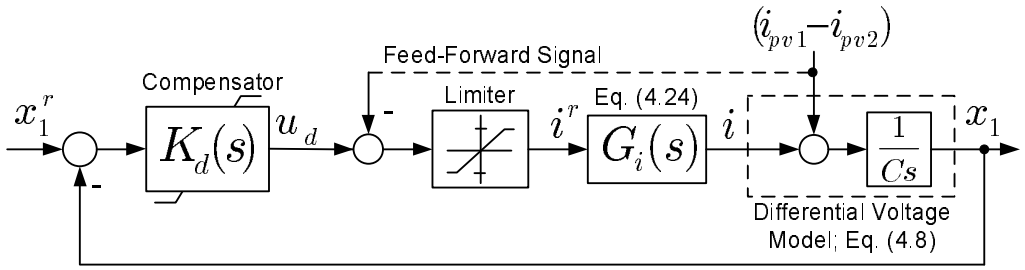

Figure 3.5: Block diagram of the differential DC-link voltage control loop.

which represents an integrator. To stabilize and control this plant, $K_d(s)$ is sufficient to be a PI compensator, say

$$K_d(s) = \frac{k_3 s + k_4}{s} \tag{3.27}$$

in which k_3 and k_4 are the proportional and integral gains, respectively; the gains can be calculated for an adequately large phase margin and closed-loop bandwidth, based on the assumption that $G_i(j\omega) \approx 1$ or $i \approx i^r$. As Figure 3.5 shows, i^r is limited by a saturation block to ensure protection of the half-bridge transistor leg against DC-side ground faults as well as normal transient excursions; the upper and lower limits should be symmetrically set to, for example, 1.2 times the maximum short-circuit current level of a sub-array. However, the output of $K_d(s)$ is symmetrically limited to a small value, in order to prevent an integrator wind up.

Net DC-Link Voltage Controller

The third control loop, shown in Figure 3.6, is the one that regulates the net DC-link voltage, v_{dc}, based on (3.17) and through the control of P_t. Thus, for this loop P_t is the input, $v_{dc} = x_2$ is the output, and $i_{pv1} + i_{pv2}$ and i are the undesirable inputs. On the other hand, in a three-phase VSC the control of the real and reactive power is commonly accomplished by dq-frame control of the VSC AC current, such that

$$P_t = \frac{3}{2}\,\widehat{v}\; i_{td} \tag{3.28}$$

and

$$Q_t = -\frac{3}{2}\,\widehat{v}\; i_{tq} \tag{3.29}$$

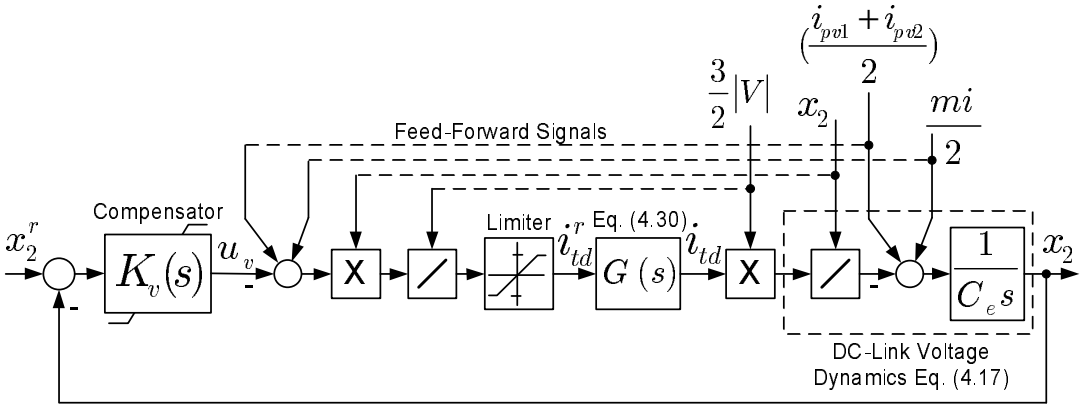

Figure 3.6: Block diagram of the net DC-link voltage control loop.

where $\widehat{v}$ is the magnitude of the voltage v_{abc}, and i_{td} and i_{tq} are the direct and quadrature components of the VSC AC current $i_{t,abc}$ [60]. As extensively discussed in Chapter 8 of reference [60], proper tuning of the VSC controllers ensures that

$$\frac{I_{td}(s)}{I_{td}^r(s)} = \frac{I_{tq}(s)}{I_{tq}^r(s)} = G(s) = \frac{1}{\tau_p s + 1} \tag{3.30}$$

where i_{td}^r and i_{tq}^r are the reference values for i_{td} and i_{tq}, respectively; τ_p is the time constant of the closed-loop step response, and is a design choice [60]. Thus, as Figure 3.6 illustrates, the error between v_{dc} and its reference value is processed by the compensator $K_v(s)$ and forms the control signal u_v. The control signal is, in turn, augmented with measures of the disturbance inputs $\frac{1}{2}(i_{pv1} + i_{pv2})$, $\frac{1}{2}mi$, $\frac{3}{2}\widehat{v}$, and x_2, such that i_{td}^r is determined as

$$i_{td}^r = \frac{2}{3}\left(\frac{x_2}{\widehat{v}}\right)\left[-u_v + \frac{1}{2}mi + \frac{1}{2}(i_{pv1} + i_{pv2})\right] \ . \tag{3.31}$$

$\widehat{v}$ can be obtained from the synchronization scheme of the PV system.

If, assuming a fast real-power control response, i_{td}^r is replaced by i_{td} in (3.31), then, combining (3.17), (3.28), and (3.31), one finds the effective control plant in the compact form

$$C_e \frac{dx_2}{dt} = u_v \tag{3.32}$$

which represents an integrator and can be readily controlled by a PI compensator, such

as

$$K_v(s) = \frac{k_5 s + k_6}{s} \tag{3.33}$$

for which the proportional and integral gains, k_5 and k_6, can be calculated for a reasonably large phase margin and closed-loop bandwidth, based on the assumption that $G(j\omega) \approx 1$. As Figure 3.6 shows, i_{td}^r is limited by a saturation block to ensure protection of the VSC against over-currents, for example, due to AC external faults. The saturation limits are typically set to 1.1-1.2 times the PV system rated AC current.

Equation (3.29) indicates that Q_t is proportional to i_{tq} and, thus, to i_{tq}^r in a steady state. The reactive power that the PV system delivers to the grid, Q, is the sum of Q_t and the reactive power supplied by the filter capacitor C_f. Typically, i_{tq}^r is set to a positive value such that Q_t is negative and equal in absolute value to the reactive power supplied by C_f, in order to ensure that the PV system exhibits unity power factor to the grid.

3.3 Simulation Results

To evaluate the effectiveness of the PV system of Figure 3.2 and its control strategy, a detailed switched model of a 1-MW system is constructed and simulated in the PSCAD/EMTDC software environment. The grid is represented by a balanced three-phase voltage source of which each phase is connected in series with a corresponding series RL branch; the source voltage, the per-phase inductance, and the per-phase resistance are 4.16 kV (line-to-line, rms), 0.63 mH, and 0.4 Ω, respectively. Each sub-array is modeled as a lumped representation of ($N_p =$) 144 parallel-connected strings of ($N_s =$) 18 series-connected PV modules; each module is, in turn, assumed to be composed of ($M_s =$) 54 identical basic PV cells. The model and parameters of the modules are introduced in Appendix C. The MPPT schemes employ the incremental conductance (IC) algorithm [21], and are updated once every 50 ms. Parameters of the PV system and its controllers are given in Appendix C.

The simulation results demonstrate the PV system performance under the start-up process, normal operating conditions, and DC- and AC-side faults. In the first two cases, the two MPPT schemes are disabled in order to allow a more clear evaluation of the proposed control strategy, free of periodic disturbances associated with the MPPT process. However, in the subsequent five cases, the system response is also demonstrated

under a more practical scenario in which the MPPT schemes are in effect.

3.3.1 Case 1: PV System Response Under Start-Up Process and Normal Operation

This case demonstrates the PV system overall response to a start-up process and normal operation. In this case, the two PV sub-arrays are exposed to a solar irradiation of 1.0 kW/m^2, and the reference commands v^r_{pv1} and v^r_{pv2} are imposed externally (i.e., no MPPT is exercised). Thus, v^r_{pv1} is assigned the value 400 V, from $t = 0$ s to $t = 0.6$ s, is stepped down to 300 V at $t = 0.6$ s, and is stepped up to 450 V at $t = 0.7$ s. Similarly, v^r_{pv2} is assigned the value 400 V until $t = 0.55$ s, is stepped up to 500 V at $t = 0.55$ s, and is stepped down to 350 V at $t = 0.65$ s. Until $t = 0.5$ s all controllers are disabled and the switching pulses of the VSC and those of the auxiliary half-bridge converter are blocked. However, the DC-link capacitors are pre-charged by the PV sub-arrays, up to the sum of the open-circuit voltages of the two sub-arrays, since the solar irradiation is adequately large. Otherwise, if the PV sub-arrays were subjected to a low solar irradiation, the anti-parallel diodes of the VSC would pre-charge the capacitors up to a net DC-link voltage about the peak value of the AC-side line-to-line voltage, through the pre-insertion resistors of the breaker Br (not shown in Figure 3.2).

Figure 3.7(a) and Figure 3.7(b) illustrate the responses of the sub-array voltages to their respective reference commands. The figures indicate that the responses are almost decoupled from one another and settle at their steady-state values in about 10 ms; perfect decoupling of v_{pv1} and v_{pv2} is not possible due to the limited speed-of-response of the reactor current-control scheme and also the fact that the net DC-link voltage is fairly robust to changes, due to the large DC-link (effective) capacitance. Figure 3.7(c) illustrates the waveform of the net DC-link voltage, which is a response to $v^r_{dc} = v^r_{pv1} + v^r_{pv2}$. Figure 3.7(d) and Figure 3.7(e) illustrate the waveforms of the two sub-array powers, P_{pv1} and P_{pv2}, respectively, and confirm that the power delivered by each sub-array is a function of the sub-array voltage, which, in turn, tracks its respective reference command.

3.3.2 Case 2: PV System Response to Unequal Solar Irradiations of Sub-Arrays

This case study demonstrates the PV system response to unequal sub-array solar irradiations, while no MPPT process is exercised. Initially, the PV system is in a steady-state,

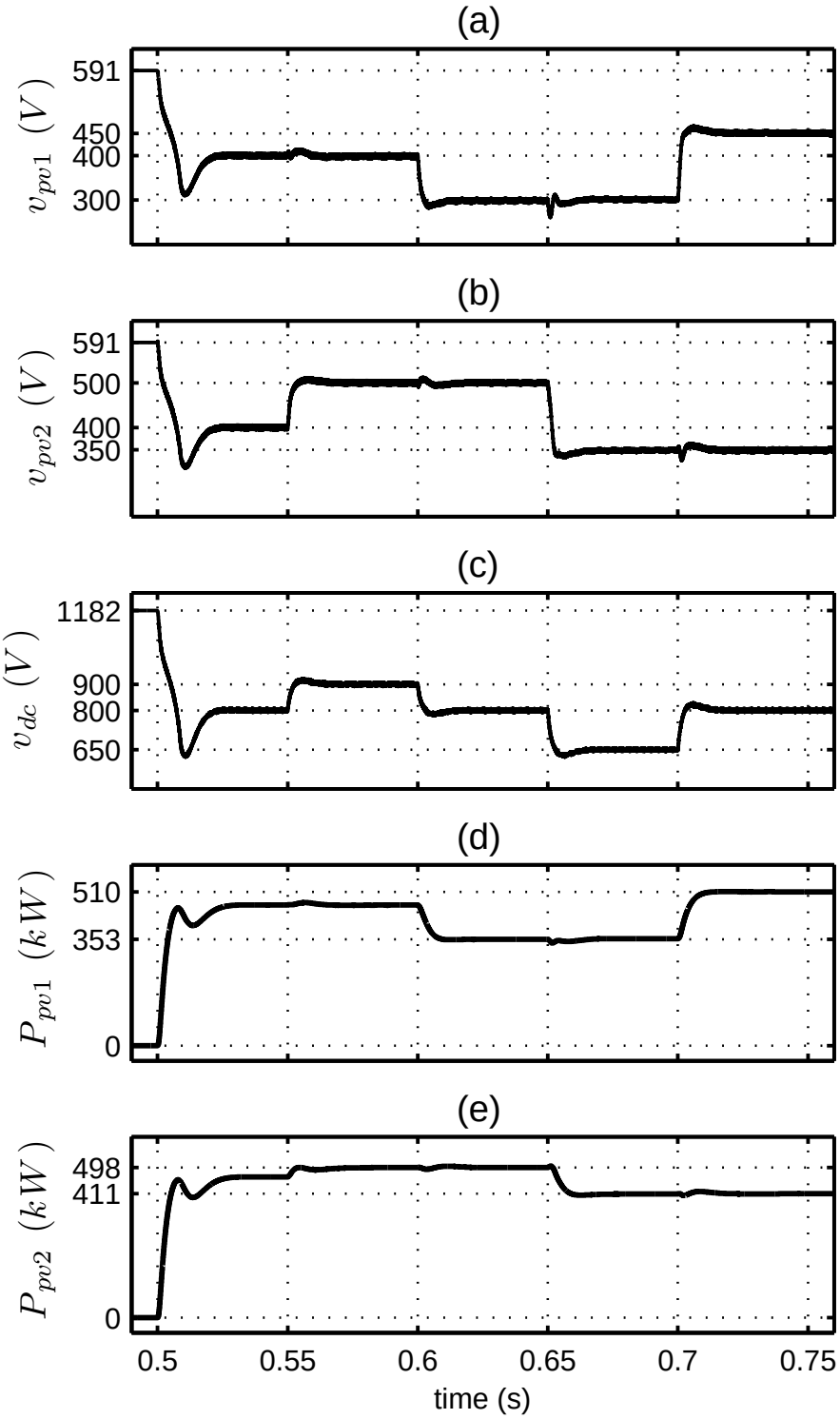

Figure 3.7: PV system overall response to stepwise changes in the sub-array voltage setpoints, from the start-up instant to a steady state, with no MPPT.

the two sub-arrays are subjected to a solar irradiation of 1.0 kW/m^2, and v^r_{pv1} and v^r_{pv2} are both set to 400 V. Subsequently, the solar irradiations of Sub-array #1 and Sub-array #2 assume the values (1.0, 0.5) from $t = 1.0$ s to $t = 1.05$ s, (0.5, 0.5) from $t = 1.05$ s to $t = 1.1$ s, (0.5, 1.0) from $t = 1.1$ s to $t = 1.15$ s, and (0.8, 1.0) from $t = 1.15$ s onward (the solar irradiation values are in kW/m^2). Figure 3.8 illustrates the current and voltage waveforms of the two PV sub-arrays, and the current waveform of the reactor.

Figure 3.8(a) and Figure 3.8(b) indicate that the steady-state values of i_{pv1} and i_{pv2} are proportional to the corresponding sub-array solar irradiations. However, as Figure 3.8(c) and Figure 3.8(d) show, v_{pv1} and v_{pv2} remain regulated at 400 V, due to the actions of the net and differential DC-link voltage controllers, except at the instants when the solar irradiation of a sub-array changes and results in short-term excursions in v_{pv1} and v_{pv2}. It is further observed that the transient excursions of v_{pv1} and v_{pv2} are approximately mirror images of each other. The reason is that the net DC-link voltage does not change significantly in response to a short-term disturbance, due to the large effective DC-link capacitance. The magnitudes of the excursions can be reduced if the partial DC-link capacitors are made larger and the reactor current-control loop is made faster; practical and cost considerations, however, limit both options. Figure 3.8(e) confirms that the difference between the sub-array currents flows through the reactor.

It is worth explaining the spikes observed on the current waveform of a sub-array at the instants when the solar irradiation of the other sub-array changes (for example, note the spike on i_{pv1} in Figure 3.8(a), at $t = 1.0$ s). These spikes are not due to changes in the photo-current component of the host sub-array; rather, they are caused by the transient excursions of the sub-array voltage and the, consequent, momentary shift in the sub-array operating point.

3.3.3 Case 3: PV System Response to Step Change in Solar Irradiation of One Sub-Array

In this test, the PV system response to a step change in the solar irradiation of one sub-array is demonstrated in Figure 3.9, while the MPPT process is in effect. The PV system is subjected to the same start-up process as those explained in Case #1, with both sub-arrays exposed to a solar irradiation of 1.0 kW/m^2. During the start-up period, each sub-array voltage setpoint is assigned by its respective MPPT scheme a constant value, for example, equal to 0.78 times a measure of the sub-array open-circuit voltage, sampled at about $t = 0.3$ s. Once the PV system start-up process is complete, the

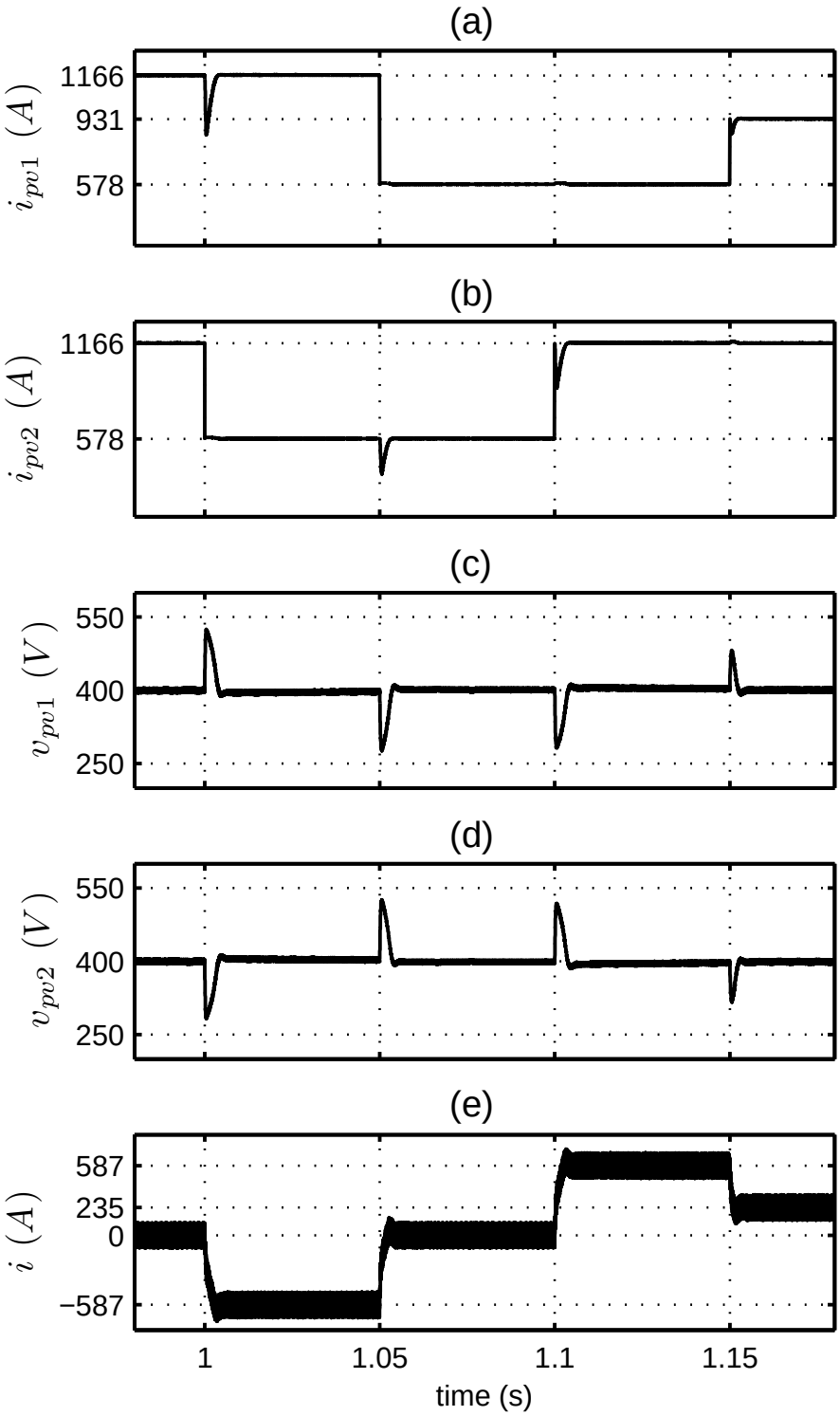

Figure 3.8: PV system response to unequal exposures of the sub-arrays to solar irradiation, with no MPPT.

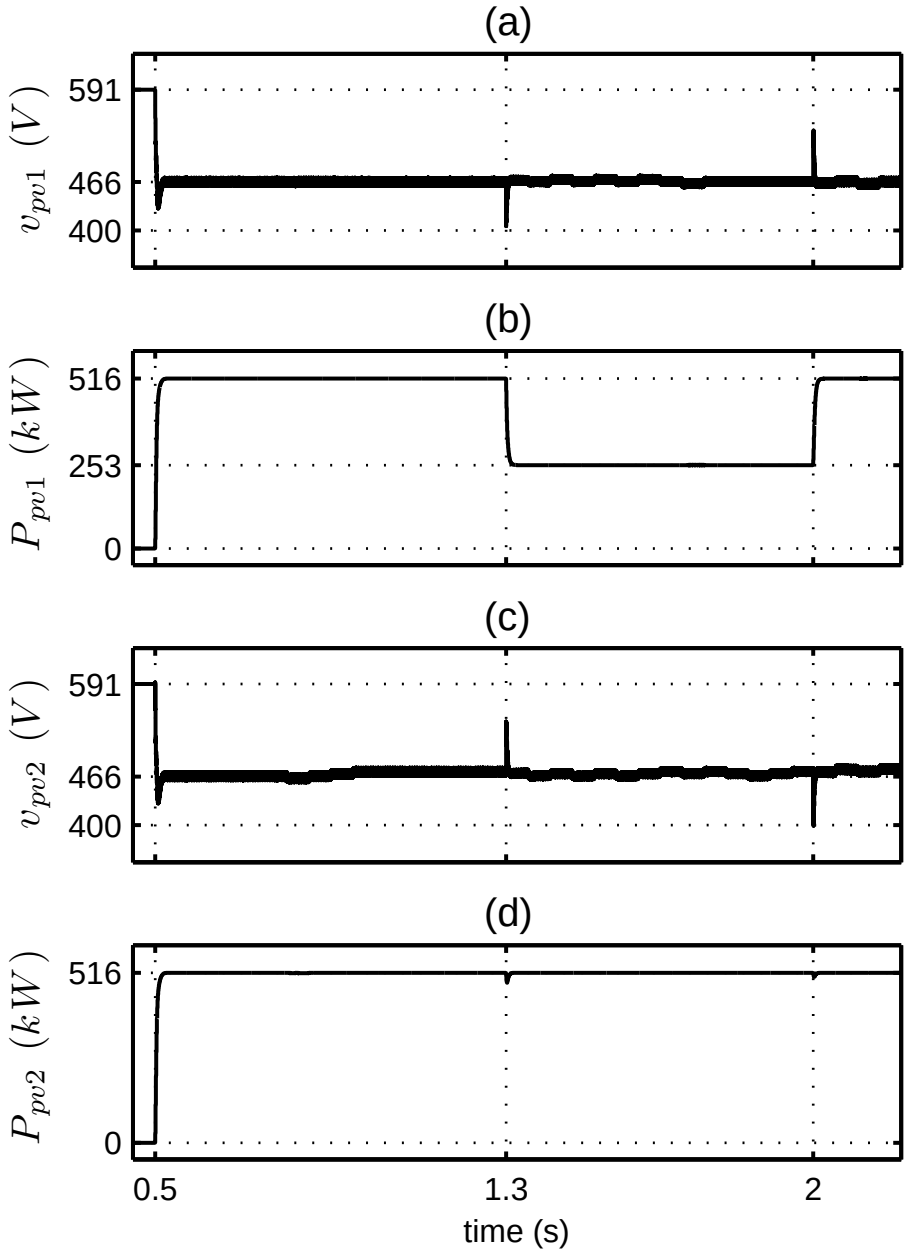

Figure 3.9: PV system response to a step change in the solar irradiation of one sub-array, with the MPPT process in place.

MPPT schemes start to dynamically issue the voltage setpoints v^r_{pv1} and v^r_{pv2} based on the IC algorithm. At $t = 1.3\ s$, the solar irradiation of Sub-array #1 assumes a stepwise decrease to 0.5 kW/m^2, which is reversed by a stepwise increase from 0.5 kW/m^2 to 1.0 kW/m^2, at $t = 2.0\ s$; all along, the solar irradiation of Sub-array #2 remains unchanged at 1.0 kW/m^2.

Figure 3.9(a) and Figure 3.9(c) indicate that, despite the significant difference in the

solar irradiations of the two sub-arrays over the period from $t = 1.3\ s$ to $t = 2.0\ s$, the two sub-array voltages are more or less the same, corresponding to their MPPs, except at $t = 1.3\ s$ and $t = 2.0\ s$ where they exhibit anti-phasal transient excursions of almost equal magnitudes. Hence, the stepwise decrease in the solar irradiation of Sub-array #1 results in a proportional drop in P_{pv1}, as Figure 3.9(b) shows, whereas P_{pv2} remains fairly undisturbed, as Figure 3.9(d) illustrates. The reason is that a reduction in the solar irradiation has an insignificant impact on the array open-circuit and MPP voltages (unless the solar irradiation is excessively low), but proportionally reduces the array short-circuit and MPP currents.

3.3.4 Case 4: PV System Response to Partial Shading of One Sub-Array

This test demonstrates the PV system response to an abrupt partial shading of Sub-array #1, while Sub-array #2 and the unshaded modules of Sub-array #1 receive a solar irradiation of 1.0 kW/m^2. It is understood that, under a partial shading condition the current of a sub-array remains more or less constant, whereas its voltage drops drastically. In this study, the aforementioned scenario is simulated by stepping down the number of rows in Sub-array #1, that is N_s, from 18 to 15, at $t = 1.5\ s$. This downsizing emulates the effect that the anti-parallel bypass diodes of the shaded modules clamp down to zero the voltages of 3 rows (out of 18 rows) of the sub-array. Thus, unlike Case #3 in which unequal solar irradiations resulted in a significant current mismatch between the two sub-arrays, in this case a significant voltage difference between the two sub-arrays manifests itself. Figure 3.10(a) and Figure 3.10(b) show that, in response to the disturbance, the MPPT scheme of Sub-array #1 finds the new MPP in less than 0.35 s. Compared to Sub-array #2, the steady-state MPP of Sub-array #1 corresponds to a lower voltage (of about 380 V) and power (of about 420 kW). Figure 3.10(c) and Figure 3.10(d) indicate that the disturbance makes transient impressions on the operating point of Sub-array #2, but has no steady-state impact on it.

3.3.5 Case 5: PV System Response to a Symmetrical AC Fault

This case demonstrates the robustness of the PV system to a symmetrical AC-side fault. Thus, the PV system is in a steady state while both sub-arrays receive a solar irradiation of 1.0 kW/m^2. Then, each high-voltage phase of the transformer Tr is temporarily

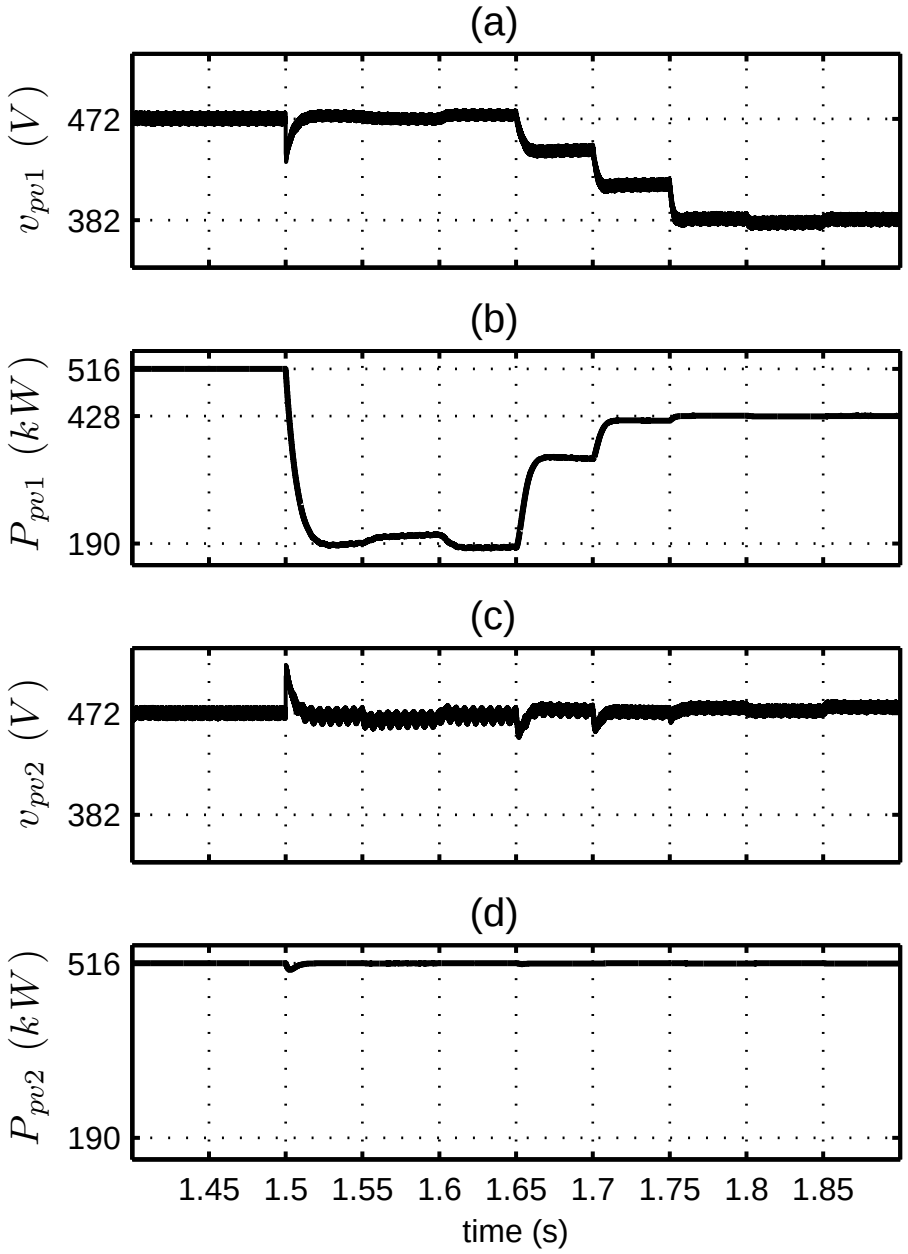

Figure 3.10: PV system response to partial shading of one sub-array, when the MPPT process is in place.

shorted to the ground, through a 0.4-mH inductance; the fault is incepted at $t = 2.0$ s and lasts for 0.1 s. Figure 3.11 illustrates the PV system response to the fault.

Figure 3.11(a) shows that, subsequent to the fault inception, the three-phase voltage drops to about 26% of its pre-disturbance value. Consequently, as Figure 3.11(b) shows, the PV system increases (the amplitude of) its AC-side current in order to maintain the pre-disturbance power output. However, the current magnitude is limited due to the ref-

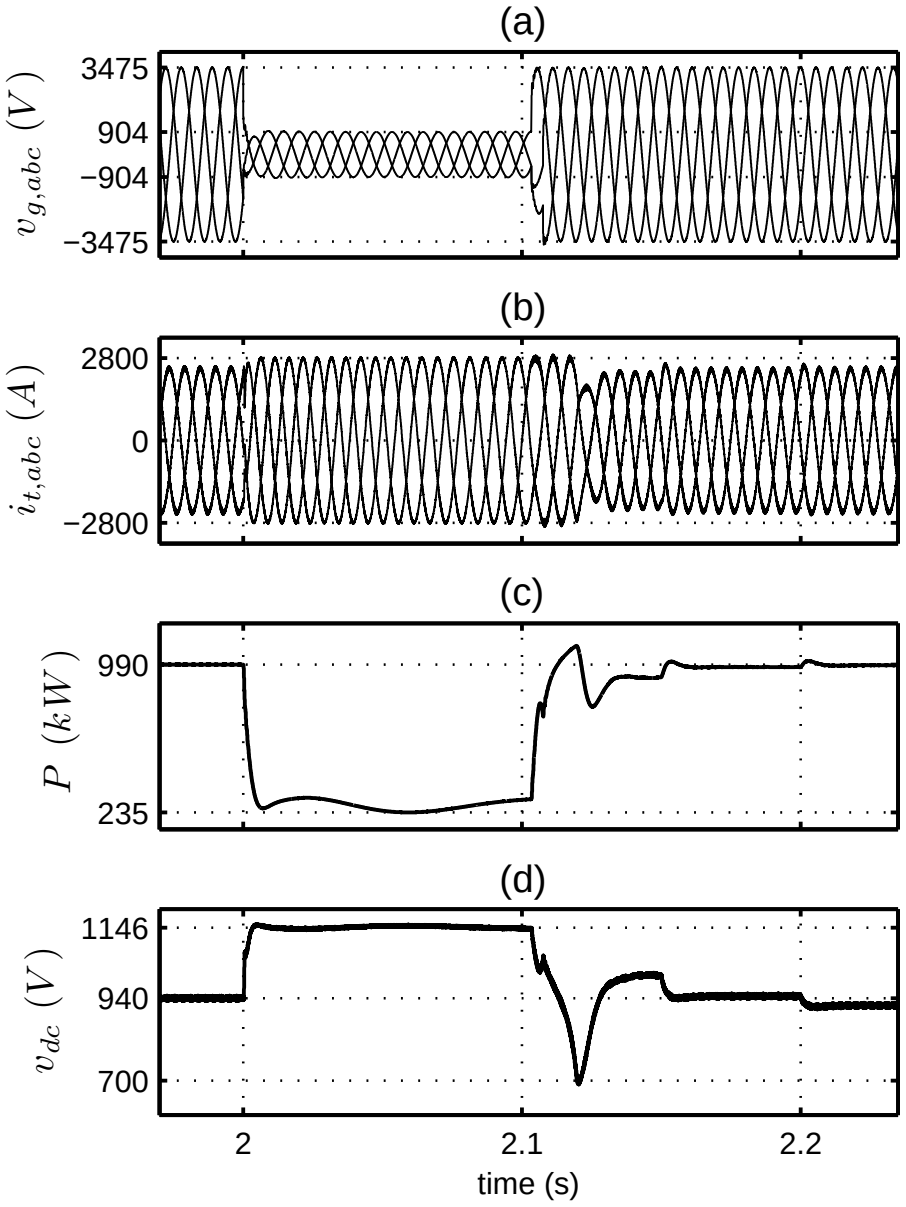

Figure 3.11: PV system response to three-phase-to-ground fault.

erence power saturation block (see Figure 3.6) and, therefore, insufficient to compensate for the severe voltage drop. Consequently, the power output drops as Figure 3.11(c) indicates. Since the PV sub-arrays keep energizing the DC link of the PV system, the power output drop results in a net DC-link voltage increase, up to the sum of the sub-array open-circuit voltages, as shown in Figure 3.11(d). Once the fault is cleared, the MPPT schemes bring back the PV system to its pre-disturbance MPP, in about 0.1 s, as Figure 3.11(c) and Figure 3.11(d) show.

3.3.6 Case 6: PV System Response to an Asymmetrical AC Fault

This case is similar to Case #5 except that the PV system is subjected to a single-phase to ground fault, through a 0.4-mH inductance. Thus, the AC-side voltage becomes severely unbalanced, as Figure 3.12(a) shows. The fault results in a limited increase in the PV system current, as Figure 3.12(b) shows; the current, nonetheless, retains its pre-disturbance balanced sinusoidal form. The imbalance and the positive-sequence amplitude drop of the AC-side voltage result in power output double-frequency pulsations and an average value drop, respectively, as Figure 3.12(c) shows. Consequently, as Figure 3.12(d) illustrates, the net DC-link voltage also fluctuates while its average value increases relative to the pre-disturbance condition. The PV system resumes its normal operation as soon as the fault is cleared at $t = 2.1\ s$, and the MPPT schemes rapidly reclaim the pre-disturbance MPP.

3.3.7 Case 7: PV System Response to a DC-Side to Ground Fault

This case demonstrates the robustness of the PV system to a DC-side ground fault. Initially, the PV system is in a steady state, while the sub-arrays receive a solar irradiation of 1.0 kW/m^2. Then, at $t = 1.5\ s$ terminal A of Sub-array #1 (see Figure 3.2) is shorted to the ground. Consequently, the diode D_1 become reverse-biased and isolates Sub-array #1 from the rest of the PV system. This, in turn, results in about 50% drop in the PV system power output, as Figure 3.13(a) shows. Moreover, as Figure 3.13(b) shows, the MPPT scheme of Sub-array #1 reduces v_{pv1} to a low voltage at $t = 1.55\ s$, that is, the first time that it is updated after the disturbance incident; this voltage is a fraction of an estimate of the sub-array open-circuit voltage and is enforced by the MPPT scheme whenever the sub-array current is sensed to be zero. This mechanism is particularly useful if a shadow suddenly extends over a large area of a sub-array and drops the sub-array open-circuit voltage inasmuchas it falls below the sub-array terminal voltage, which, in turn, would result in a negative or zero sub-array current (depending on whether or not a series diode is provided for the sub-array); this is the trap where many MPPT algorithms fall into and consequently lose the entire power output. Figure 3.13(c) shows that the fault has no steady-state impact on the voltage of Sub-array #2. Hence, Sub-array #2 retains its pre-disturbance power output. Figure 3.13(c) also shows the transient excursions of

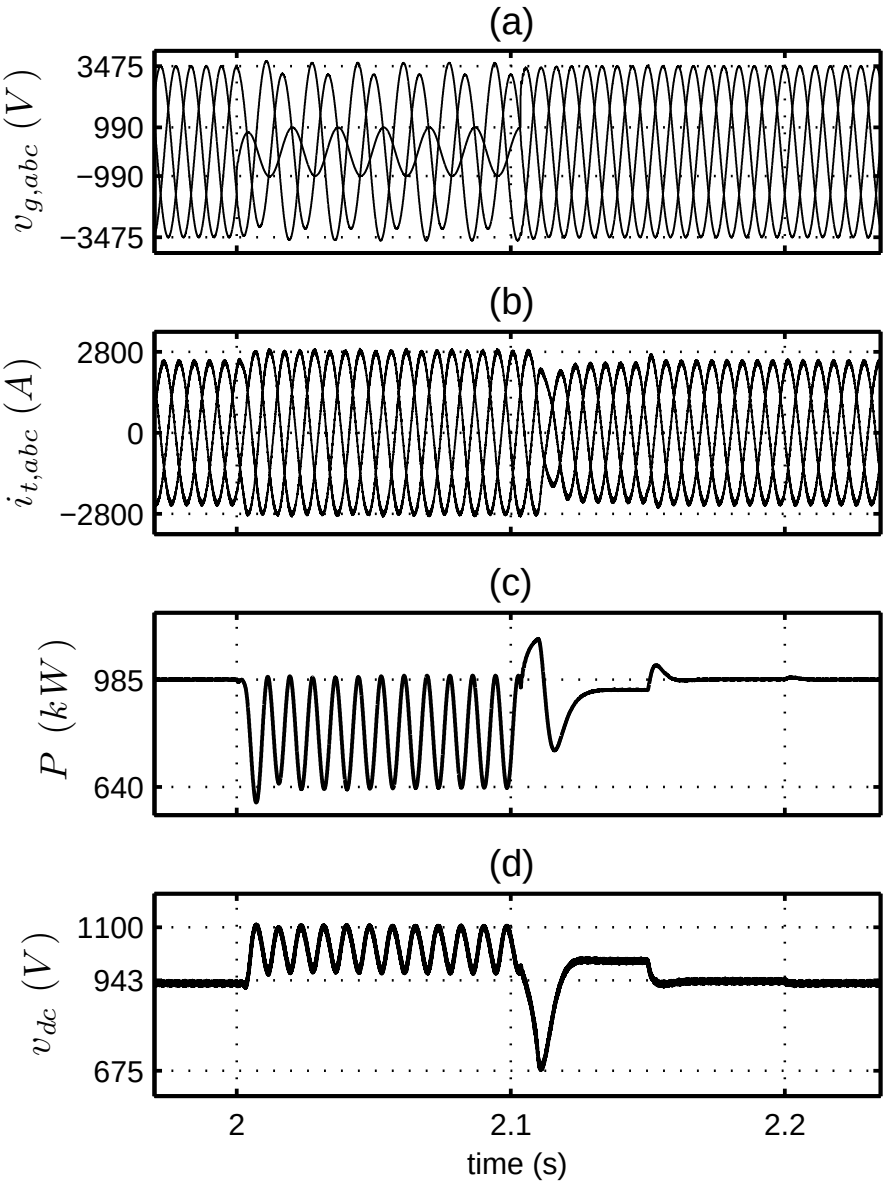

Figure 3.12: PV system response to a single-phase-to-ground fault.

v_{pv2} when v_{pv1} changes. As explained earlier, the transient excursions are due to the resilience of the net DC-link voltage to voltage variations. Figure 3.13(d) indicates that the reactor current shoots up to about 1115 A, which is equal to the current delivered by Sub-array #2 and transferred by the auxiliary half-bridge converter to the VSC; it should be noted that, during the fault presence, the current of Sub-array #1 is the same as the sub-array short-circuit current and circulates in the fault path. Figure 3.13(e) illustrates the waveforms of the three AC-side currents prior and subsequent to the fault occurrence.

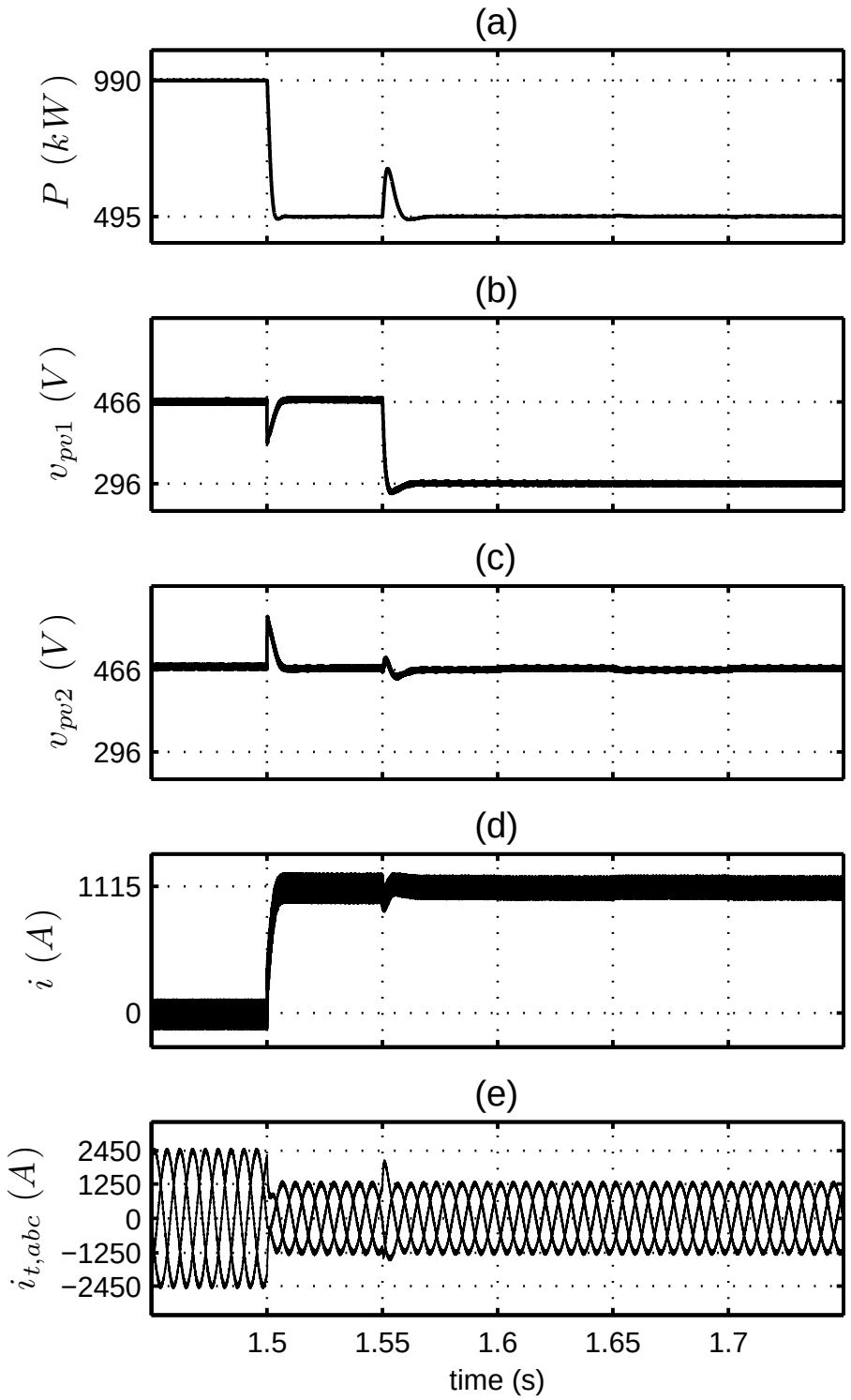

Figure 3.13: PV system response to a DC-side terminal to ground fault.

3.4 Conclusion

In this chapter, a single-stage three-phase PV system was proposed that features an enhanced MPPT capability, and an improved energy yield under partial shading conditions.

In addition, the proposed PV system can effectively double the maximum permissible DC voltage of a grounded conventional single-stage PV system, with no need for insulators, fuses, disconnects, and switchgear of a higher voltage class, with respect to safety/insulation standards or common system integration practices exercised for the grounded conventional PV systems. The proposed PV system is realized by the parallel connection of an auxiliary half-bridge converter to the DC link of a conventional single-stage PV system and, therefore, may also be attractive for retrofit applications.

Compared to a single-unit, conventional, grounded, single-stage PV system of the same power rating, the proposed PV system

- offers a superior energy yield due to its enhanced MPPT capability;
- runs at lower current levels and, therefore, lower conduction power losses. Even though the power losses associated with the DC reactor and the two additional semiconductor switches of the proposed PV system compromise the mentioned reduction in the system power loss, the overall efficiency of the proposed PV system is expected to be higher than that of a conventional counterpart, as the conduction power losses are proportional to the square of current;
- however, requires semiconductor switches of a higher voltage class, two more semiconductor switches, a center-tapped DC capacitor bank, and a DC reactor.

In many installations, high-power PV systems are realized through parallel connection of two half-rated, conventional, grounded, single-stage PV systems. Compared to such a two-unit PV system of the same overall power rating, the proposed PV system

- requires four fewer semiconductor switches, which run at the same current levels as those of the conventional system, and is thus expected to offer a higher efficiency, in spite of the power losses of the DC reactor and the center-tapped capacitor bank;
- effectively integrates two half-rated PV systems into one cubicle. Further, it avoids the interphase transformer that is required for parallelling the two half-rated PV systems. Therefore, the proposed PV system is expected to economize on the manufacturing costs and on the footprint;
- however, requires semiconductor switches of a higher voltage class, a center-tapped DC capacitor bank, and a DC reactor.

This chapter presented the mathematical model, principles of operation, and the control loops of the proposed single-stage PV system. The performance and robustness of the proposed single-stage PV system was demonstrated for faulted, as well as normal operating conditions, by time-domain simulation studies conducted on a detailed switched model.

Chapter 4

Three-Level Two-Stage Inverter

4.1 Introduction

Unlike their European counterparts, large-scale North American PV systems have a DC voltage limit of 600 V [24,59,61]. Although the limit can be relaxed for "behind the fence" systems, manufacturers still comply with it to avoid the issues associated with insulation and safety considerations for higher voltage classes. To maintain simplicity and high efficiencies, large-scale PV systems are typically based on the single-stage technology, that is, their hosted PV arrays are directly connected to a DC-AC inverter. However, the low DC voltage and existence of only one energy conversion stage require a relatively low AC voltage (and large currents) which compromises the efficiency improvements achieved through the single-stage technology. The low AC voltage also imposes non-optimal coupling transformer designs for integration with medium-voltage grids. In addition, in single-stage systems, large variability of the maximum power-point DC voltage results in poor utilization of the inverter power semiconductors. Furthermore, the existence of only one energy conversion stage implies a poor maximum power-point tracking performance and reduced energy yield, especially, under partial shading and/or array mismatch conditions. The aforementioned issues have placed a cap on the maximum economically viable rating of single-stage PV inverters, such that large-scale systems are commonly implemented through parallel connection of smaller units (up to a power rating of 1 MW).

This chapter proposes a two-stage PV system that largely overcomes the aforementioned issues. The proposed PV system consists of multiple DC-DC boost converters and one large inverter. The inverter is based on the neutral-point clamped (NPC) technology with a grounded DC-link midpoint. Thus, it enables a bipolar structure and doubles

the net DC voltage, while the 600 V standard is respected. The boost converters independently control the DC voltages of their corresponding PV arrays, while their output voltages are regulated by the inverter. Therefore, the proposed PV system offers an enhanced MPPT performance and energy yield. Under fault conditions, however, the boost converters automatically regulate their output terminal voltages and prevent the DC-link voltage from rising. The NPC technology permits the employment of low-voltage switches for the inverter, despite the doubled net DC voltage.

4.2 Proposed Bipolar Two-Stage PV System

4.2.1 Structure and Principle of Operation

Figure 4.1 shows a schematic diagram of the proposed PV system. As the figure shows, two similar PV sub-arrays are interfaced to the inverter, through a "boost converter pair". Each PV sub-array is composed of N_p parallel-connected PV strings. In turn, each string consists of N_s series-connected PV modules. N_s is chosen in such a way that the open-circuit voltage of each sub-array, under the worst temperature and solar irradiation condition, is marginally lower than the maximum permissible voltage of 600 V, whereas N_p is determined based on the power rating of the sub-array. The inverter is of the three-level NPC type with its DC-side midpoint grounded. The boost converter pair consists of two mirrored boost converters. Thus, as Figure 4.1 indicates, the output of each DC-DC boost converter is in parallel with the midpoint and one of the DC-link rails of the inverter. This also implies that the output voltage of each boost converter (approximately) equals that of one of the partial DC-side voltages of the inverter. Figure 4.1 also indicates that more than one pair of sub-arrays and boost converters may be interfaced with the inverter. Further, depending on the specifics of an installation, the boost converter pairs may be close to their sub-array pairs or, alternatively, close to the inverter (the system of Figure 4.1 assumes that the boost converter pairs are next to the corresponding sub-arrays).

Under normal operating conditions, the inverter regulates the partial DC-side voltages v_{dc1} and v_{dc2}, each at a level slightly lower than 600 V (575 V, for example). Therefore, since the midpoint of the system DC-link is grounded, the North American standard for maximum DC voltage is satisfied. Moreover, the net DC-link voltage is effectively doubled. Meanwhile, each boost converter of a pair controls the voltage of its corresponding sub-array and thus exercises independent MPPT. This, however, can cause the midpoint

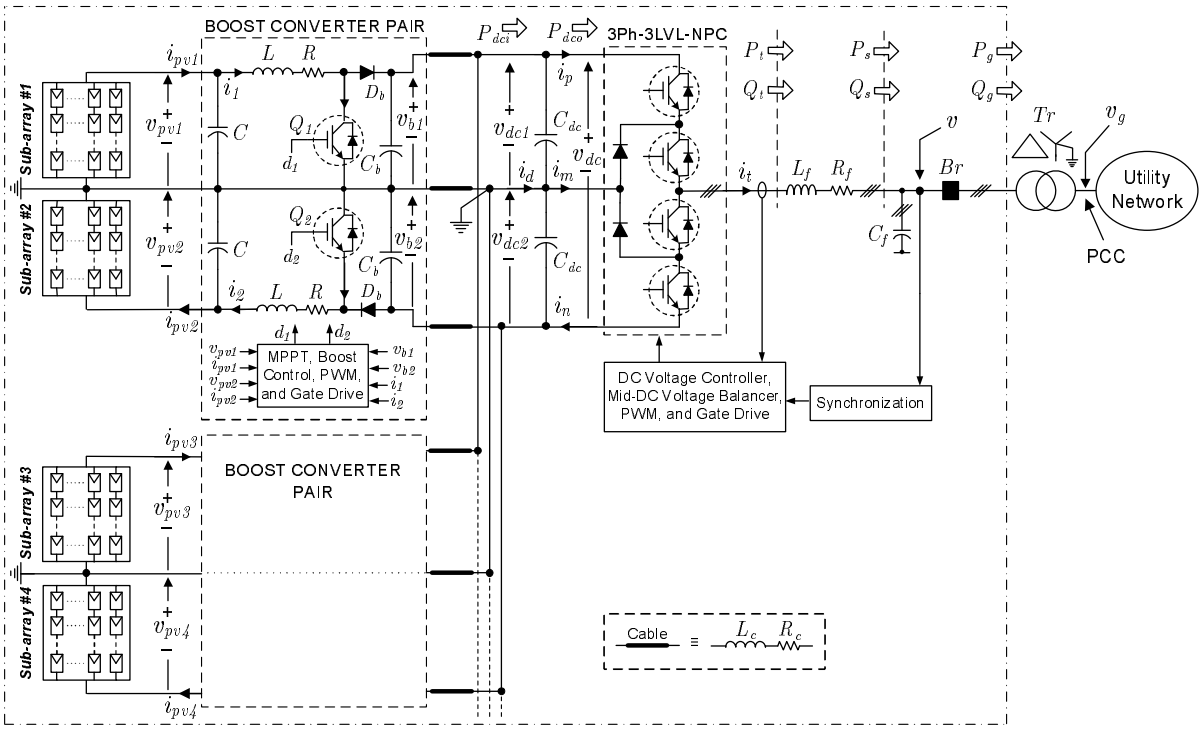

Figure 4.1: Schematic diagram of the proposed bipolar two-stage PV system.

current i_Δ to assume a large value, due to unequal solar irradiations that the two sub-arrays may be subjected to. The controller of the inverter must, therefore, compensate for the non-zero midpoint current, to maintain the regulation of v_{dc1} and v_{dc2}. If for any reason, for example, the occurrence of network faults, the inverter fails to transfer energy to the grid and, consequently, the DC-link voltage rises, the boost converters automatically switch to an output voltage control mode, to prevent a DC-link voltage runaway.

The midpoints of the NPC converter, the boost converter pairs, and the symmetrically-connected PV sub-arrays are connected together to the ground. Depending on the environmental parameters, the voltages and powers of the two symmetrically-connected PV sub-arrays can be variably different. Since the voltages of the NPC terminals are regulated to the equal $\pm 575\ V$, the magnitude of NPC positive and negative terminals DC currents can be different, resulting in DC current difference flowing into or out of NPC midpoint terminal. In case of large mismatch between the upper and lower sub-arrays, resulted, for instance, from partial shading, the midpoint DC current can be of large value. The flow of this potentially large current is facilitated by adding a DC value to the PWM modulating signals, which will be studied in detail in section 4.2.2.

The DC-link capacitors, C_{dc}, are used to bypass the current ripples produced by both the NPC inverter and the boost converters. As will be discussed later in subsection II-B3, the current ripples of third, sixth, and other harmonics of multiples of 3 in the NPC converter midpoint terminal produce similar harmonic ripples on the partial DC-side voltages of v_{dc1} and v_{dc2}. To limit these voltage ripples in order to employ the maximum permissible DC voltage swing, C_{dc} should be of large value and/or other techniques should be considered to decrease those ripples; one such technique will be discussed in section 4.2.2.

4.2.2 Mathematical Model and Control Architecture

Main Inverter AC Current Control

The inverter is current-controlled in a rotating dq frame whose d axis is aligned with the space phasor corresponding to the three-phase voltage v_{sabc}, by means of a phase-locked loop (PLL) [60]. Thus, the d- and q-axis components of the inverter AC current, that is i_{td} and i_{tq}, independently track their respective setpoints based on the following transfer function

$$\frac{I_{td}(s)}{I^r_{td}(s)} = \frac{I_{tq}(s)}{I^r_{tq}(s)} = G_i(s) = \frac{1}{\tau_i s + 1} \ , \tag{4.1}$$

where the time constant τ_i can be made sufficiently small by proper tuning of the current-control parameters [60]. In turn, i_{td} and i_{tq} enable the control of the inverter real- and reactive-power outputs as

$$P_s = \frac{3}{2} v_{sd} i_{td} \tag{4.2}$$

$$Q_s = -\frac{3}{2} v_{sd} i_{tq} \ , \tag{4.3}$$

where v_{sd} denotes the d-axis components of the voltage v_{sabc}. The setpoints i^r_{td} and i^r_{tq} are limited by saturation blocks to ensure protection of the inverter against network faults. The structures and tuning guidelines for the PLL and current-control scheme are extensively discussed in [60] and not repeated in this thesis.

In the remainder of this chapter, it will be discussed that real-power control enables regulation of the net DC-link voltage, and reactive-power control is employed for power factor control of the inverter.

Net DC-Link Voltage Regulation

Net DC-link voltage regulation is based on the principle of power balance

$$\frac{1}{4}C_{dc}\frac{dv_{dc}^2}{dt} = P_{dci} - P_{dco}, \tag{4.4}$$

where P_{dci} is the aggregate power output of all boost converters and P_{dco} is the power drawn by the inverter from the DC link. Ignoring the power loss of the inverter, one can approximate P_{dco} by the inverter power output P_s. Thus, (4.4) can be rewritten as

$$\frac{1}{4}C_{dc}\frac{dv_{dc}^2}{dt} = P_{dci} - \frac{3}{2}v_{sd}i_{td} \ . \tag{4.5}$$

Equation (4.5) indicates that the (square of) net DC-link voltage can be controlled by i_{td}^r. This is achieved through the control loop of Figure 4.2. As Figure 4.2 shows, a compensator, $K_v(s)$, processes the error between v_{dc}^2 and its setpoint, and determines the current setpoint i_{td}^r. Then, i_{td} tracks i_{td}^r, based on (4.1), and the loop is closed. In the control loop of Figure 4.2, the signals $(3/2)v_{sd}$ and P_{dci} are incorporated for feedforward compensation and better disturbance rejection. Assuming a fast current-control loop (implying $i_{td} \approx i_{td}^r$) and inclusion of the feedforward signals, one can approximate the control plant as

$$\frac{1}{4}C_{dc}\frac{dv_{dc}^2}{dt} = u_v \ , \tag{4.6}$$

where u_v is the compensator output [see Figure 4.2]. Thus, the open-loop gain represents an integrator, and $K_v(s)$ can be a simple proportional-integral (PI) compensator of the form

$$K_v(s) = \frac{k_3 s + k_4}{s} \ , \tag{4.7}$$

where k_3 and k_4 are the proportional and integral gains, respectively.

Partial DC-Side Voltage Balancing

The partial DC-side voltage balancer of the inverter ensures that $\langle v_{dc1}\rangle_0 = \langle v_{dc2}\rangle_0$, where $\langle\ \rangle_0$ denotes the DC component of the waveform calculated over one cycle of the power system frequency. Maintaining this balance is important for safe and proper operation of the three-level inverter [60]. In general, the imbalance between the two DC components

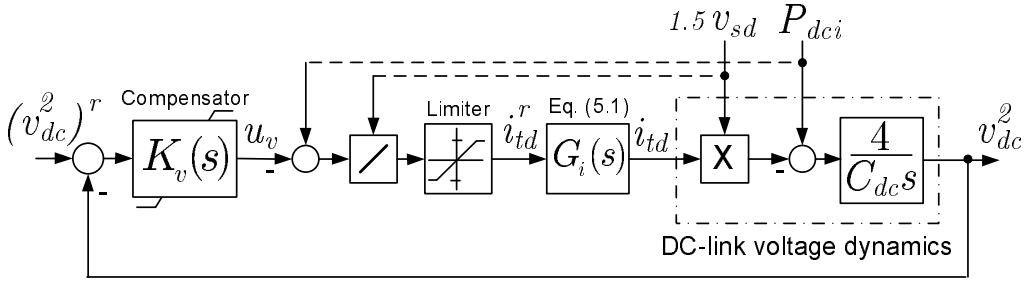

Figure 4.2: Block diagram of the net DC-link voltage regulator.

is caused by non-zero DC component of the inverter midpoint current i_m, due to imperfections. In the proposed PV system, however, the dominant effect is that of the current i_Δ [see Figure 4.1], which is likely to be large due to the naturally different operating conditions of the PV sub-arrays; the difference between $\langle i_m \rangle_0$ and i_Δ flows through the DC-side capacitors and results in drifts in $\langle v_{dc1} \rangle_0$ and $\langle v_{dc2} \rangle_0$.

To maintain the balance between $\langle v_{dc1} \rangle_0$ and $\langle v_{dc2} \rangle_0$, the current component $\langle i_m \rangle_0$ must be controlled in a control loop, which is referred to as the "partial DC-side voltage balancer" [60]. The partial DC-side voltage balancer, shown in Figure 4.3, compares the signal $\langle \Delta v_{dc} \rangle_0 = \langle v_{dc1} \rangle_0 - \langle v_{dc2} \rangle_0$ with zero, processes the error by the compensator $K(s)$, and determines the DC offset m_0 for the pulse-width modulation (PWM) modulating signals of the inverter:

$$\begin{cases} m_a(t) = m_0 + \hat{m}\cos[\varepsilon(t)] - k\hat{m}\cos[3\varepsilon(t)] \\ m_b(t) = m_0 + \hat{m}\cos[\varepsilon(t) - 2\pi/3] - k\hat{m}\cos[3\varepsilon(t)] \\ m_c(t) = m_0 + \hat{m}\cos[\varepsilon(t) - 4\pi/3] - k\hat{m}\cos[3\varepsilon(t)], \end{cases} \tag{4.8}$$

where $\varepsilon(t)$ is the angle that the space phasor corresponding to the signals $m_{abc}(t)$ makes against the α axis of the stationary frame; the constant k determines the magnitude of the third-order harmonic of $m_{abc}(t)$; and $\hat{m}$ is

$$\hat{m} = \sqrt{m_d^2 + m_q^2}\ , \tag{4.9}$$

where m_d and m_q are the dq-frame components of the space phasor corresponding to $m_{abc}(t)$. In the control loop of Figure 4.3, i_Δ acts as a disturbance input.

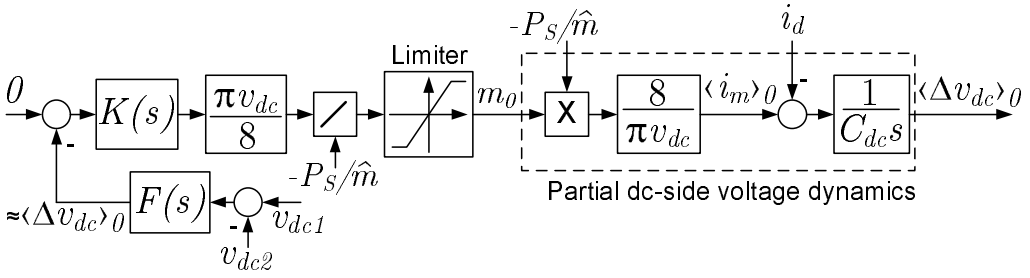

Figure 4.3: Block diagram of the partial DC-side voltage balancer.

Dynamics of $\langle \Delta v_{dc} \rangle_0 = \langle v_{dc1} \rangle_0 - \langle v_{dc2} \rangle_0$ are governed by [60]

$$\frac{d}{dt}\langle \Delta v_{dc} \rangle_0 = \frac{1}{C_{dc}} \left(-\frac{8P_s}{\pi v_{dc} \hat{m}} m_0 - i_\Delta \right). \tag{4.10}$$

As Figure 4.3 indicates, m_0 is determined as

$$m_0 = -\frac{\pi v_{dc} \hat{m}}{8P_s} u_k \ , \tag{4.11}$$

where u_k is the output of $K(s)$. Thus, the effective control plant is

$$C_{dc} \frac{d}{dt}\langle \Delta v_{dc} \rangle_0 = u_k \ , \tag{4.12}$$

which represents an integrator. Therefore, $K(s)$ can be a simple PI compensator of the form

$$K(s) = \frac{k_1 s + k_2}{s}, \tag{4.13}$$

where k_1 and k_2 are the proportional and integral gains. The DC component $\langle \Delta v_{dc} \rangle_0$ is obtained by passing the signal $v_{dc1} - v_{dc2}$ through a notch filter, $F(s)$, as Figure 4.3 shows. The notch filter is tuned to the third harmonic of the power system frequency.

Partial DC Voltage Ripple Mitigation

In a three-level inverter, the partial DC-side voltages, v_{dc1} and v_{dc2}, include triple-n harmonic fluctuations. Although the fluctuations are of opposite polarities and thus do not appear in the net DC-link voltage v_{dc}, they restrict $\langle v_{dc1} \rangle_0$ and $\langle v_{dc2} \rangle_0$ in terms of proximity to the maximum permissible voltage of 600 V and should be reduced as much as possible. One way of reducing the fluctuations is to increase the capacitance of

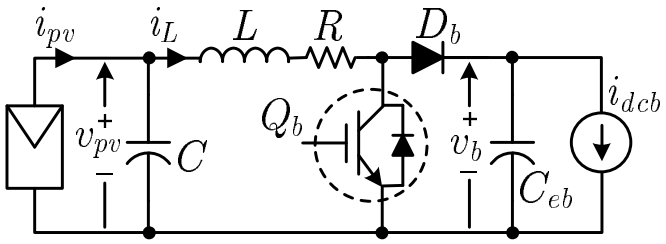

Figure 4.4: Circuit diagram of the boost converter.

the DC-side capacitors. A more economical solution, however, is to employ the third-order harmonic injected PWM represented by the modulating signals (4.8). As discussed in [60], the ripples are significantly reduced if the scale factor k is chosen to be 1/6; this is the conventional third-order harmonic injected PWM. The ripples can be further reduced if $k = 7/27$ [62]. The expense, however, is a 3% drop in the maximum AC voltage that the inverter can synthesize in its linear operating range, compared with the conventional third-order harmonic injected PWM. It should also be noted that the ripples become smaller as the inverter power factor approaches unity. Thus, for the proposed PV system, i^r_{tq} is assigned a value such that the power factor is unity if the inverter delivers 80% of its rated power output.

Boost Converter Control

The control of the traditional boost converter has been widely discussed in the literature. However, in a two-stage system such as the proposed PV system, in which the DC-link voltage is regulated by the second stage (inverter in the system of Figure 4.1, a failure of the second stage or occurrence of network faults can result in substantial DC-link voltage overshoots, if the first stage is not programmed to quickly and automatically reduce its power production. To circumvent the aforementioned situation, the boost converters of the proposed PV system, which normally maximize the power production of their respective PV sub-arrays, are controlled in such a way that they decrease their power outputs if the DC-link voltage exceeds a pre-specified threshold. This section provides the details of the control.

Figure 4.4 illustrates a simplified circuit diagram of one of the boost converters of a pair, where C_{eb} is the effective capacitance that the output of the boost converter views. Neglecting the effect of cables, C_{eb} is the sum of C_b and C_{dc}/n, where n is the number of boost converter pairs; i_{dcb} is equal to $\langle i_p \rangle_0 / n$ (for the upper converter of the pair) or $\langle i_n \rangle_0 / n$ (for the lower converter of the pair) [see Figure 4.1]. The control of the boost

converter is based on the following equations:

$$C\frac{dv_{pv}}{dt} = i_{pv} - i_L \tag{4.14}$$

$$C_{eb}\frac{dv_b}{dt} = -i_{dcb} + (1 - m_b)i_L \tag{4.15}$$

$$L\frac{di_L}{dt} + Ri_L = v_{pv} - (1 - m_b)v_b, \tag{4.16}$$

where m_b is the modulating signal of the boost converter, i_L is the inductor current, i_{pv} is the sub-array current, v_b is the converter output terminal voltage, and v_{pv} is the sub-array voltage. Equations (4.14) through (4.16) are averaged over one cycle of the switching frequency.

Figure 4.5(a) illustrates a control loop that is able to regulate the PV sub-array voltage v_{pv} at the setpoint v_{pv}^r, if the output terminal voltage v_b is free to change; v_{pv}^r is determined by a corresponding MPPT scheme. As the figure shows, first, based on (4.16), a current-control loop controls the inductor current i_L such that

$$\frac{I_L(s)}{I_L^r(s)} = G_b(s) = \frac{1}{\tau_b s + 1}, \tag{4.17}$$

where the time constant τ_b is a design choice. Then, an outer loop determines the current setpoint i_L^r and thus controls v_{pv} based on (4.14). Alternatively, Figure 4.5(b) illustrates a control loop, based on (4.15), that can regulate v_b, if the sub-array voltage v_{pv} is free to change. The loop of Figure 4.5(b) also employs the current-control scheme which was described as a part of Figure 4.5(a). The two control loops are combined as shown in Figure 4.5(c), such that at, any given time, only one of the two control loops generates the current setpoint i_L^r while the other loop is saturated. In other words, during normal operation when the DC-link voltage is regulated by the inverter, the output of the compensator $K_b(s)$ is saturated to a small value, and i_L^r is actively determined by $K_{pv}(s)$ to regulate v_{pv}. However, if the DC-link voltage rises, for example, during faults, the output of compensator $K_{pv}(s)$ is saturated. Consequently, $K_b(s)$ takes over the control of i_L^r to regulate v_b, and the DC-link voltage stops rising. The value of the setpoint v_b^r is chosen to be slightly larger than half of the DC-link voltage setpoint (about 590 V, for example). The integration of the two control loops is possible due to the fact that the feedforward signals i_{pv} and $i_{dcb}/(1-m_b)$ [see Figs. 4.5(a) and (b)] have equal steady-state values; this can be verified by setting the derivatives in (4.14) and (4.15) to zero. Further, m_b has been assumed to be 0.5, such that the factor $1/(1 - m_b)$ can be absorbed as a

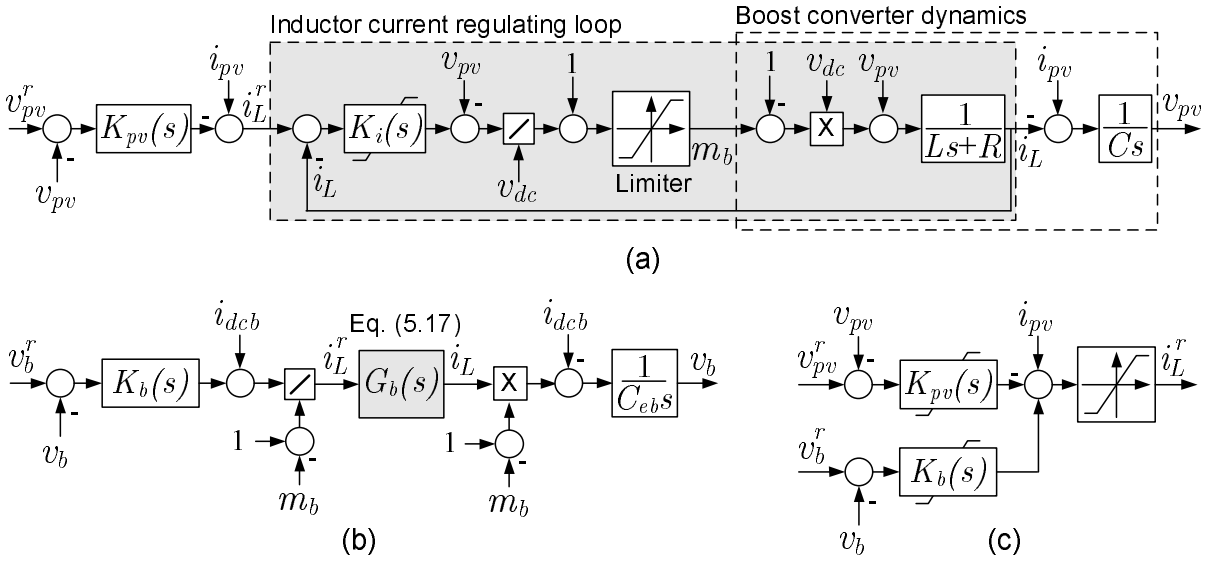

Figure 4.5: Block diagram of the boost converter control scheme.

constant factor by $K_b(s)$.

4.3 Simulation Results

The performance of the proposed PV system and the effectiveness of its control schemes are evaluated through a number of study cases conducted on a detailed model of the system in the PSCAD/EMTDC software environment [55]. The rating of the inverter is 1.5 MW. Four similar boost converter pairs interface eight 0.2 MW PV sub-arrays with the inverter. The MPPT schemes of the boost converters are based on the incremental conductance (IC) algorithm [21]. The PV system is interfaced with a typical North American medium-voltage distribution network, as shown in Figure 4.6; the network and load parameters can be found in [63]. The system and controller parameters are provided in Appendix D.

4.3.1 Case 1: PV system response under startup and normal operation

This study case demonstrates the PV system response during the startup process and normal operation. To address a non-ideal condition, the PV sub-arrays are assumed to have slightly different conditions. Initial configuration of the 8 sub-arrays are listed in Table 4.1, where SAi denotes the sub-array #i, G represents the solar irradiation level

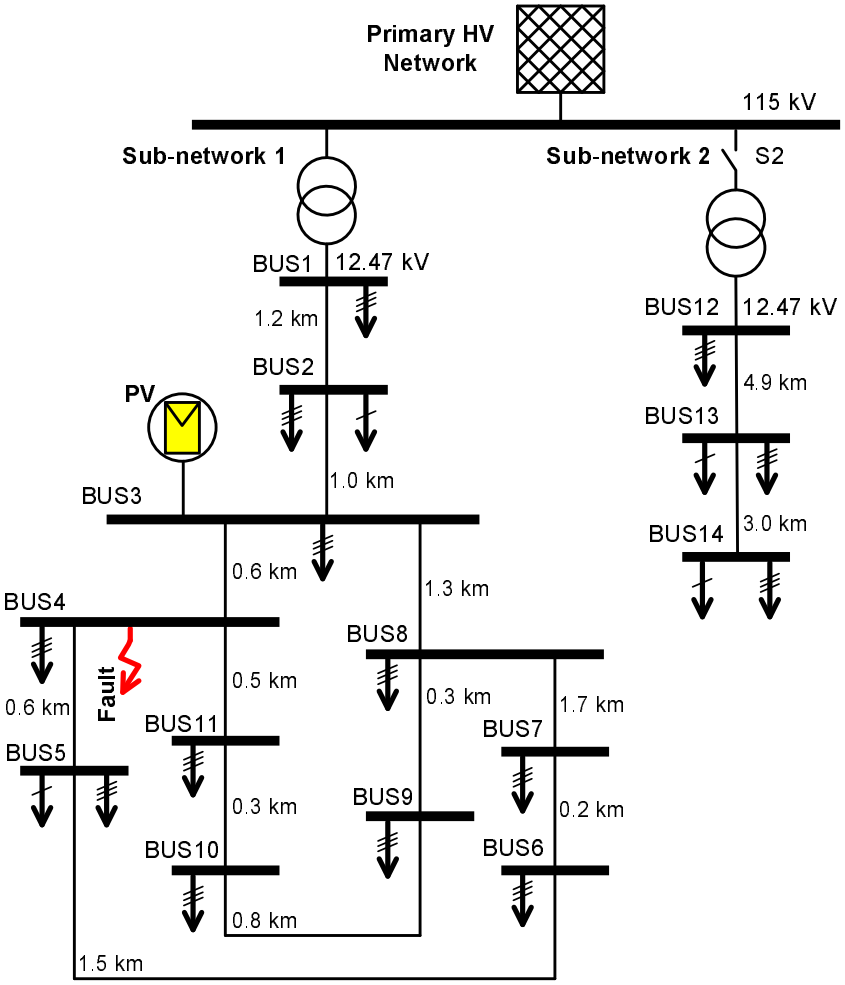

Figure 4.6: Schematic diagram of the test medium-voltage distribution network.

and N_s and N_p are the number of series- and parallel-connected PV modules in a sub-array, respectively; the junction temperature is chosen to be 25^oC for all sub-arrays. Until $t = 0.50\ s$, the inverter is disabled, but the DC-link capacitors are charged by the PV sub-arrays to the maximum open-circuit voltage of the corresponding sub-arrays. The inverter and its controllers are activated at $t = 0.50\ s$ and the four boost converter pairs are started one by one at $t = 0.52\ s$, $t = 0.54\ s$, $t = 0.56\ s$, and $t = 0.58\ s$; this is done to minimize the temporary fluctuations of the partial DC voltages. Thanks to the net DC-link voltage regulator and partial DC-side voltage balancer, the two partial DC voltages and the net DC-link voltage are regulated at their reference values, 575 V, 575 V, and 1150 V, respectively, as shown in Figure 4.7(a-c); the transient excursions due to the connection of the PV sub-arrays are small and negligible.

The partial DC voltages contain ripples of harmonics of multiples of 3 where third

Table 4.1: Initial configuration of PV sub-arrays

	SA1	SA2	SA3	SA4	SA5	SA6	SA7	SA8
$G(kW/m^2)$	1	1	1	0.8	1	1	0.9	1
N_s	17	17	17	17	17	15	17	17
N_p	58	58	58	58	58	58	50	50

harmonic ripples are the largest ones; as can be seen in Figure 4.7(a) and (b), especially between $t = 0.50\ s$, and $t = 0.52\ s$, the third harmonic ripples of the partial DC voltages are anti-phasal, resulting in a net DC-link voltage that is almost without third harmonic ripples as can be seen in Figure 4.7(c). The output power of the PV system increases as more sub-arrays start to operate, as Figure 4.7(d) illustrates. Consequently, the harmonic ripples of the DC voltages increase, since the amplitude of the inverter AC current increases.

4.3.2 Case 2: PV system response to shading and partial shading

In this study case, the performance of the PV system is evaluated under shading and partial shading conditions. Shading addresses the condition in which the solar irradiation is reduced for one entire sub-array, while in partial shading a part of a sub-array is shaded and consequently is bypassed by its protection bypass diodes; thus, to study partial shading, the number of series-connected PV modules in the sub-array, i.e., N_s, is decreased from its initial value. The system, initially, operates according to the conditions mentioned in Case #1. At $t = 0.9\ s$, the solar irradiation of SA2 is reduced from 1 to $0.5\ kW/m^2$. The partial DC voltages maintain their steady states after a short transient excursion, as shown in Figure 4.8(a) and (b). The sum of the powers produced by lower sub-arrays group (including SA2, SA4, SA6, and SA8), which was initially slightly less than that of upper sub-arrays group (including SA1, SA3, SA5, and SA7), decreases more with the shading of SA2 and the imbalance between the two groups' power grow. The partial DC-side voltage balancer, however, regulates the m_0, as can be seen in Figure 4.8(c), to let the difference current flow through the converter midpoint and to maintain the balance of the partial DC voltages. At $t = 1.1\ s$, the number of series-connected PV modules of SA6, N_{s6}, is dropped from 15 to 13, to simulate a partial shading case. At $t = 1.3\ s$, the solar irradiation of SA2 is increased back to $1\ kW/m^2$

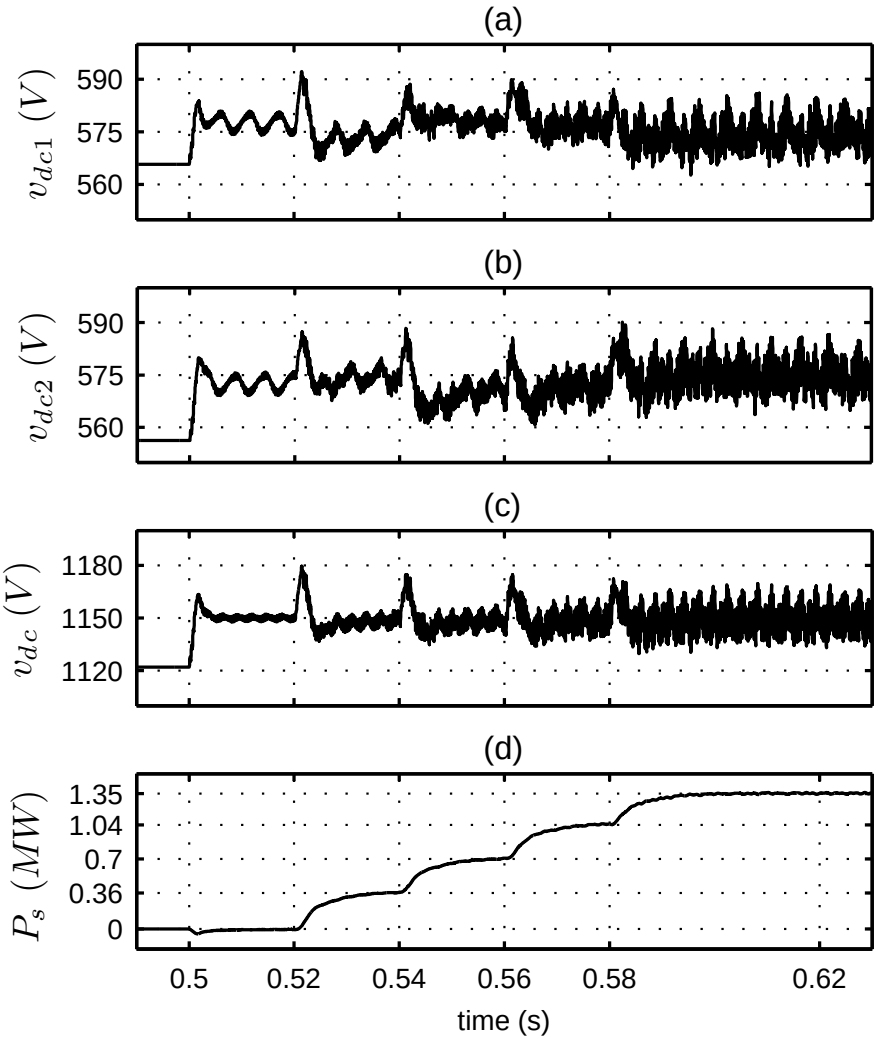

Figure 4.7: PV system response under startup process.

and at $t = 1.4\ s$, N_{s6} is increased to 17. As Figure 4.8(d) illustrates, the power output changes proportionally, and the partial DC-side voltage balancer equates v_{dc1} and v_{dc2} by choosing appropriate m_0; the variations of P_s and m_0 around $t = 1.5\ s$ are resulted from the operation of MPPT block of SA6.

4.3.3 Case 3: PV system response to a three-phase network fault

This case demonstrates the response of the PV system to a three-phase fault in the network. The fault takes place at BUS4 of the network [refer to Figure 4.6] by grounding all three phases through 1 mH inductances; the fault starts at $t = 0.8\ s$ and lasts

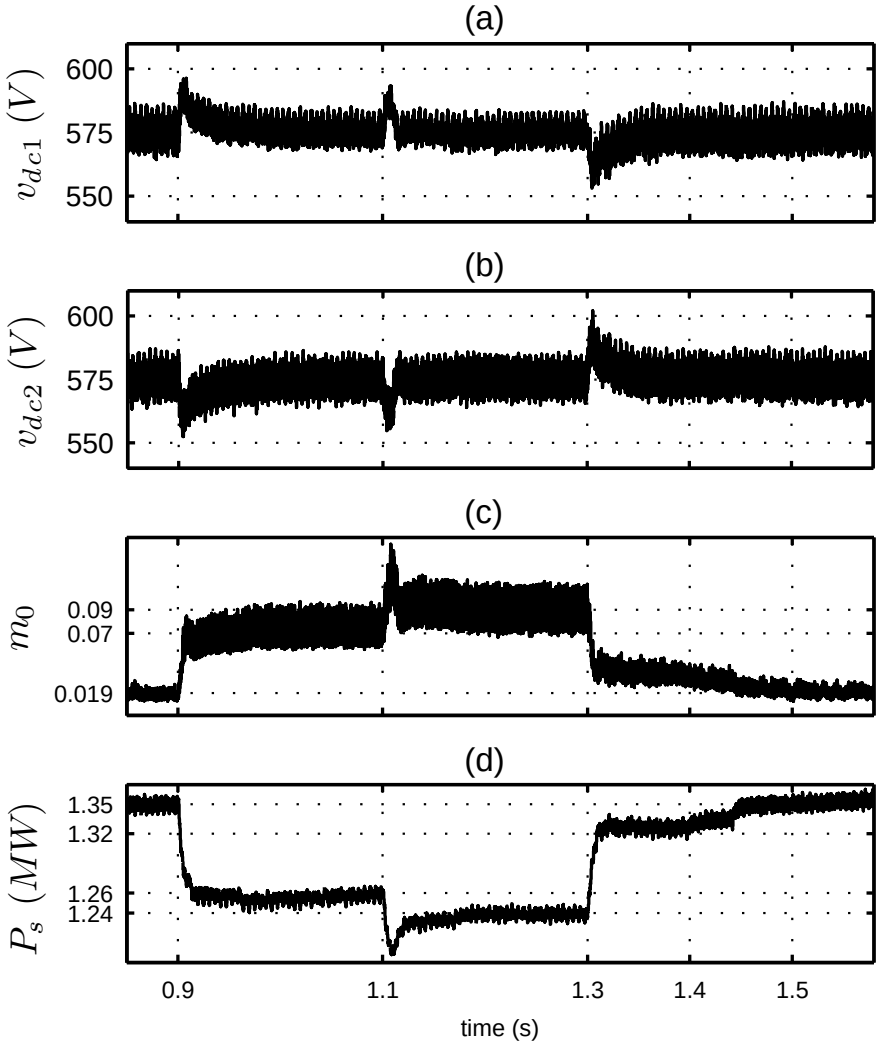

Figure 4.8: PV system response under shading and partial shading conditions.

for 0.1 s. Prior to the fault, the system operates in steady state mentioned in Case #1. After the fault inception at $t = 0.8$ s, the grid voltages, v_{gabc}, drop dramatically to %26 of its initial value, as shown in Figure 4.9(a). In order to produce the pre-disturbance power, the active power control scheme of the inverter increases the AC terminal currents, i_{tabc}. The currents, however, are limited by the inverter internal current protection mechanism which results in the reduction of the inverter power; the waveforms of the AC terminal currents and the inverter power are illustrated in Figure 4.9(b) and (c). While the AC power flow is disrupted, the first stage boost converters keep exporting the maximum power of the sub-arrays to the DC-link. This results in power accumulation in DC-link capacitors and the partial DC voltages start to increase dramatically. The

control loop proposed in Figure 4.5(b), however, limits the partial DC voltages to the v_b^r which is chosen slightly higher than $v_{dc}^r/2$, for instance 590 V. To achieve this goal, the controller of each PV sub-array decreases its power output, to reestablish the DC and AC power balance, by changing the operating voltage of the array from MMP voltage to a higher one; Figure 4.5(d-f) illustrate the waveforms of the partial DC voltages and the SA1 voltage, respectively. After fault clearance at $t = 0.9\ s$, grid voltage rises, AC terminal currents are decreased, and system power output increases to its pre-disturbance value. The AC power increase, however, decreases the net and partial DC voltages. Consequently, the controller $K_b(s)$, shown in Figure 4.5, is saturated and the controller $K_{pv}(s)$ gains back the control task which is the regulation of PV sub-array voltage to its reference value (equal to V_{MPP}) issued by its MPPT block.

4.3.4 Case 4: PV system response to a DC cable open-circuit fault

In this case, the response of the system to the open-circuit faults of two sub-arrays is demonstrated. First at $t = 1.2\ s$, the cable connecting the boost converter of SA5 to the inverter is disconnected, then at $t = 1.3\ s$, that cable of the SA6 boost converter is broken. Initially, the system is in a steady state defined in Case #1. At $t = 1.2\ s$, system loses one of its eight PV sub-arrays and the power is decreased as shown in Figure 4.10(a). The partial DC-side voltage balancer regulates the partial DC voltages through controlling m_0; Figure 4.10(b-d) illustrate the waveforms of m_0, v_{dc1}, and v_{dc2}, respectively. The output voltage of the disconnected boost converter, v_{b5}, is increased dramatically due to the accumulation of the corresponding PV sub-array's power in the output capacitor of the SA5 boost converter. Again, the control loop presented in Figure 4.5(b) starts to operate and decreases the setpoint of the boost converter inductor current, i.e., i_{L5}^r, to zero and effectively disables the boost converter. In a small fraction of millisecond, before the boost converter is turned off, its output voltage rises to a voltage higher than the maximum DC voltage. This is inevitable in rare fault cases and can be discharged through simple protection circuits. While the upper half of the boost converter connected to SA5 and SA6 is disabled, the lower half performs its normal task. Figure 4.10(e) and (f) depict the output voltages of the SA5 and SA6 boost converters. At $t = 1.3\ s$, when the cable of the SA6 boost converter is disconnected, the partial DC-side voltage balancer regulates m_0 and partial DC voltages, and the boost controller of SA6 disables the boost converter in order to limit its output voltage.

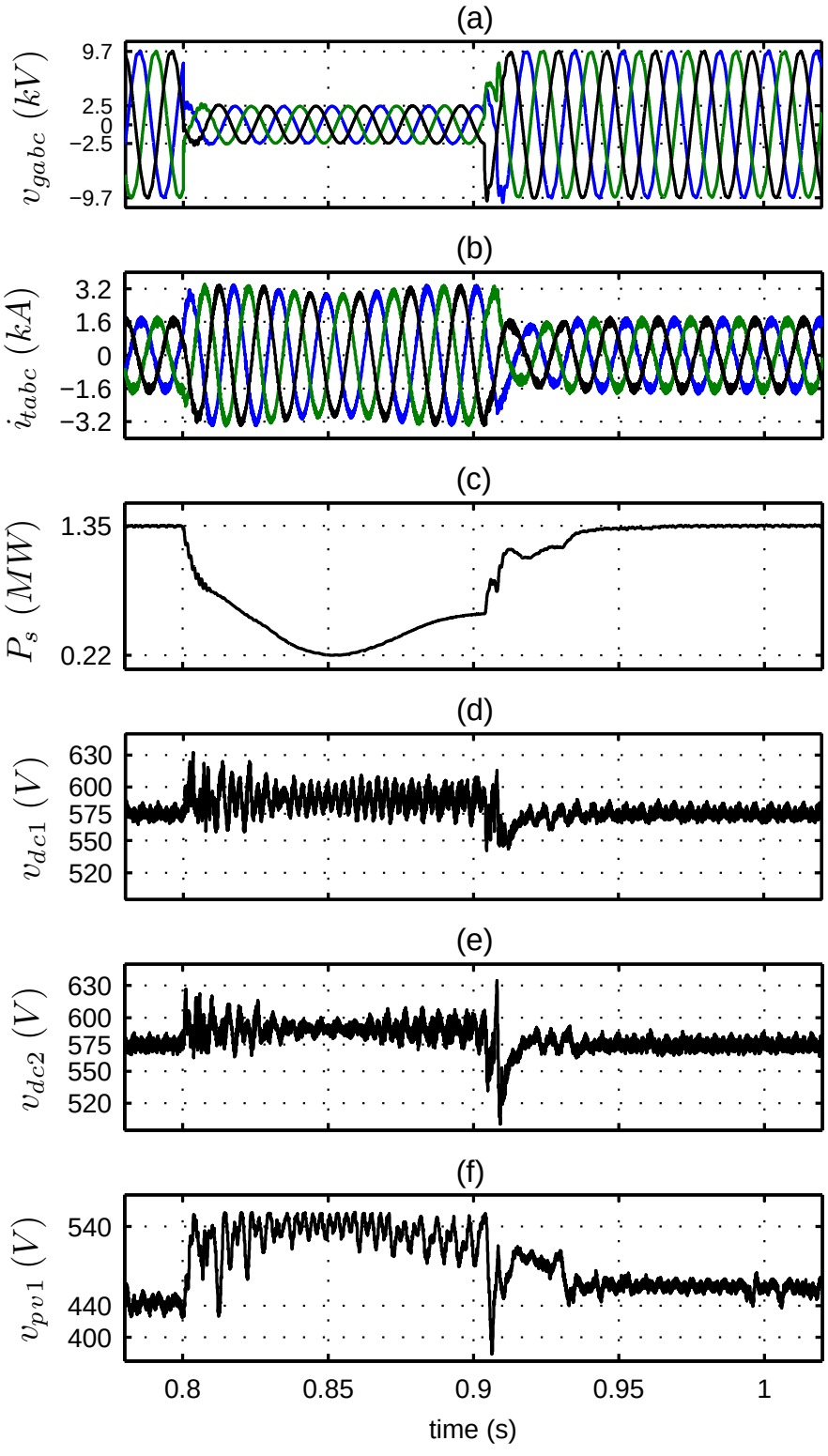

Figure 4.9: PV system response under a three-phase network fault condition.

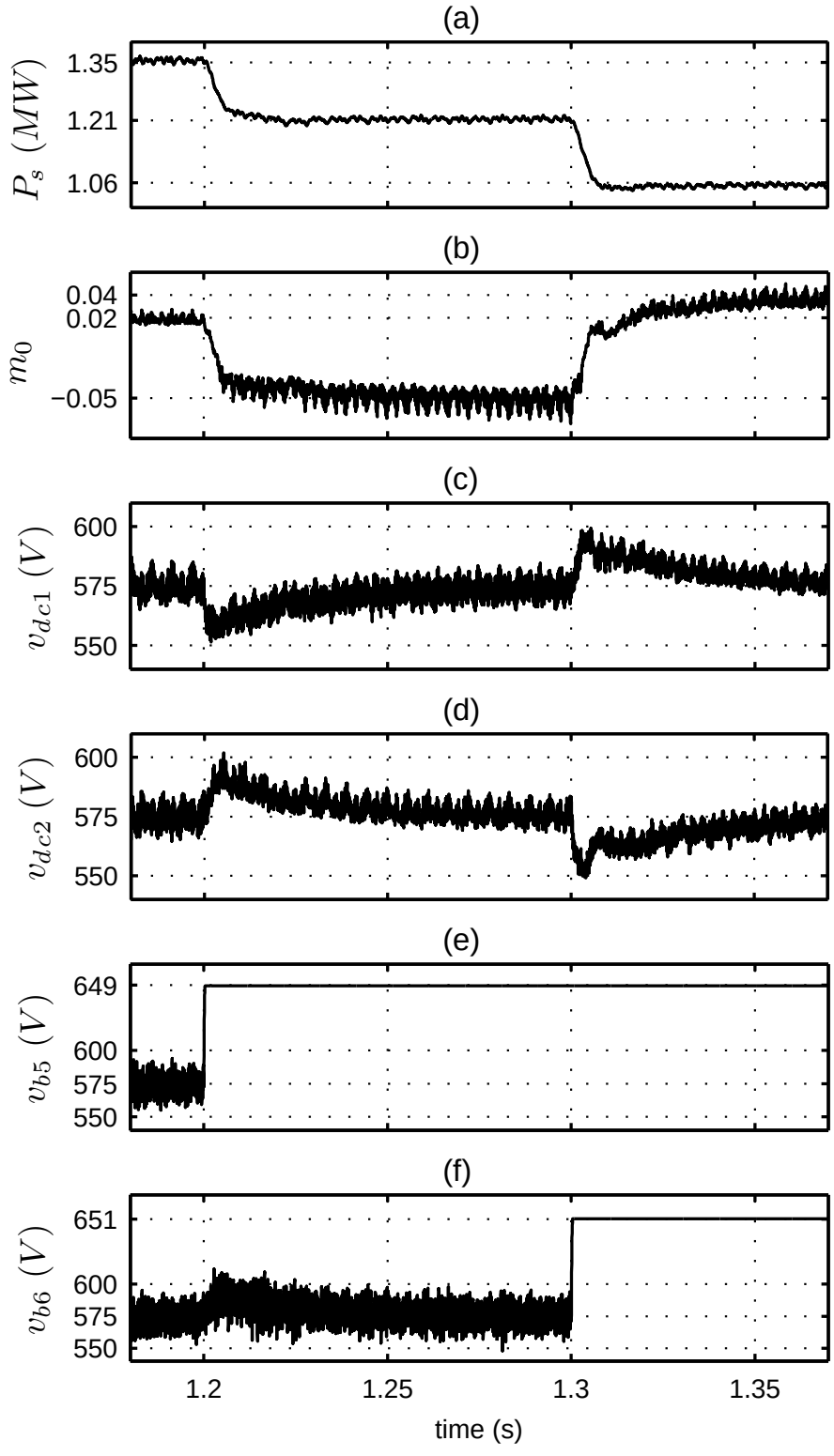

Figure 4.10: PV system response under a DC cable open-circuit fault condition.

4.4 Conclusion

In this chapter, a two-stage PV system was proposed for large-scale grid-connected applications. The proposed PV system consists of multiple DC-DC boost converters and one large inverter. The inverter is based on the NPC technology with a grounded DC-link midpoint, which enables a bipolar structure and doubling of the net DC voltage, while the 600 V standard is respected. The boost converters independently control the DC voltages of their corresponding PV arrays, while their output voltages are regulated by the inverter. Further, they can limit the DC-link voltage of the inverter if the power cannot be dispatched to the grid, for example, due to network faults. The proposed PV system also offers an enhanced MPPT performance and energy yield, due to its multi-MPPT capability. The NPC technology permits the employment of low-voltage switches for the inverter, despite the doubled net DC voltage. Principles of operation, mathematical model, and control schemes of the proposed PV system were described. Further, the performance of the proposed system was demonstrated through study cases including system startup, normal operation, shading and partial shading scenarios, and various faults.

Chapter 5

Temporary Overvoltage Mitigation in PV Systems

5.1 Introduction

This chapter deals with temporary overvoltage, one of the grid-integration issues of PV systems, which has been getting more serious recently because of ever-increasing integration of PV systems within distribution networks. This issue will be addressed in this chapter by proposing a modification to the inverter structure.

As discussed in section 1.2.4, DG-induced TOV is produced by distributed generators in power systems when a smaller aggregate local load is islanded with the DG, and is more severe when there is a SLG fault within the island. This scenario is not implausible, and can happen sometimes as follows. When a SLG fault incident takes place in a feeder/line which has one (or more DGs) connected in parallel with the power system, the substation protection devices detect the fault and open the breaker (or recloser opens)[refer to Figure 1.9]. This forms an island which contains the DG, fault source, and a local load, which altogether result in a potentially severe TOV if the power of the local load is smaller than that of the DG. This is in agreement with the conclusion of reference [49], in which the interruption of significant power export was introduced as the main reason for the formation of DG-induced TOV.

Surge arresters are the only widely utilized equipment, in HV and MV lines, to protect the customers and network equipment and personnel, from severe overvoltages. Surge arrestors are chosen such that they only respond to very severe overvoltages produced by lightning strikes, and operate by shorting the current path. No effective technical solution

has been proposed thus far to suppress, or to prevent the formation of, the (less severe, but still damaging) DG-induced TOV and other network-related overvoltages in MV and LV level distribution networks other than recommendations for "effective grounding" and proper transformer configuration selection.

This chapter proposes a technique to mitigate the DG-induced TOV produced by inverter-based distributed generators. The technique is implemented within the inverter control structure and prevents formation of the damaging DG-induced TOV. This is achieved by applying a limit for overvoltage beyond which the voltages of the affected phases are clipped through controlling the modulation signals.

It is noted that the discussed DG-induced TOV takes place for only a short period of time after the formation of island and before the DG is disabled by its own islanding detection scheme (not discussed in this study) which may not be as fast as the substation and network protection schemes; also, it should be noted that some grid codes, like the one shown in Figure 1.6, require the operation of DGs for a specified short period of time after fault. Therefore, the aim of the proposed scheme is to suppress the damaging overvoltage during that short period of time.

5.2 The Proposed Structure

The control task of a grid-connected PV inverter is normally performed in a synchronous dq frame, synchronized with the grid voltage. This simplifies the controllers' design and facilitates decoupling of the real- and reactive-power control loops through which the DC-link voltage regulation and reactive-power/power-factor control tasks are performed, respectively [40, 41]. In a conventional single-stage VSI-based PV system, as shown in Figure 5.1, the three-phase signals, i.e., the output currents and voltages, are measured/calculated and transformed to dq-frame signals. They are then processed within the control blocks together with the measured PV array current and voltage and the reference signals for power-factor/reactive-power and DC-link voltage, to produce the output pulse-width modulating signals, m_d and m_q. These output signals are then transformed, within the PWM & Gate Drive block, back to the three-phase signals, m_a, m_b, and m_c, which then produce the gate pulses for the inverter switches. During the normal operation of the inverter in the linear mode, the magnitude of the modulating signals m_a, m_b, and m_c, as well as their dq-frame counterpart's magnitude, i.e., $\sqrt{m_d^2 + m_q^2}$, are smaller than unity. Moreover, in VSIs, the terminal voltages are directly controlled by

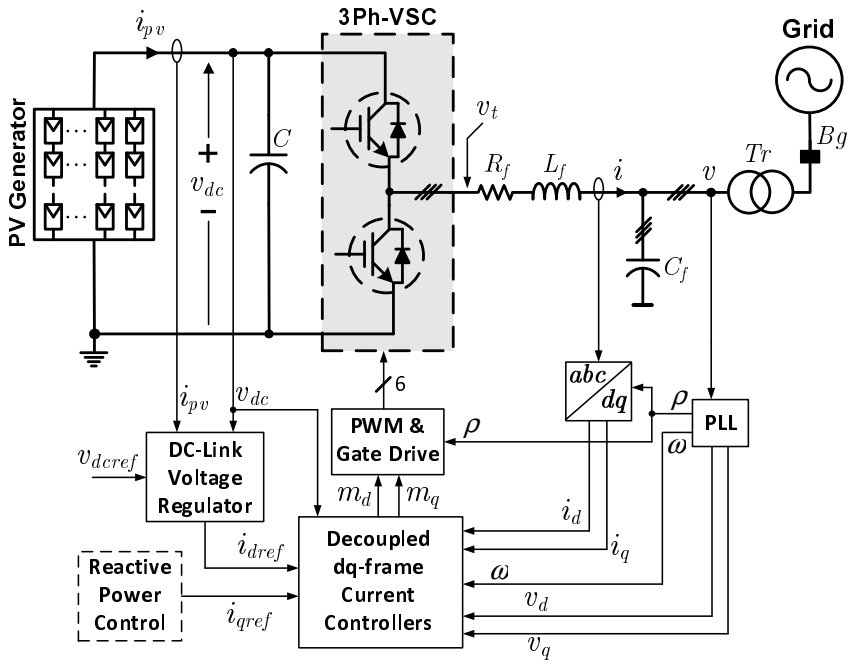

Figure 5.1: Schematic diagram of a conventional grid-connected voltage-sourced inverter.

these three-phase modulating signals through

$$\begin{cases} v_{ta}(t) = \frac{1}{2} v_{dc} m_a(t) \\ v_{tb}(t) = \frac{1}{2} v_{dc} m_b(t) \\ v_{tc}(t) = \frac{1}{2} v_{dc} m_c(t) \end{cases} \tag{5.1}$$

where v_{ta}, v_{tb}, and v_{tc} are the terminal voltages of the inverter and v_{dc} is the DC-link voltage, as shown in Figure 5.1. Therefore, the output voltage of each phase of the inverter can be directly controlled and limited, for instance in case of an overvoltage, by limiting the corresponding modulating signal.

Thus, in the proposed technique, the voltage of each phase is monitored and if an overvoltage is detected, the modulating signal of the corresponding phase is limited by a controllable saturation block to a value smaller than one. The block diagram of the proposed phase voltage limiting scheme is illustrated in Figure 5.2. In normal conditions, the saturation level is maintained at unity to let the VSI perform its normal power conversion task. However, in case of an overvoltage, a voltage higher than a prespecified level (for instance, 1.05 *p.u.*), the saturation level is reduced with a rather steep slope to a smaller level, for instance 0.5, to limit the overvoltage magnitude of the corresponding phase. The values for the slope and the level are design choices and are chosen to limit

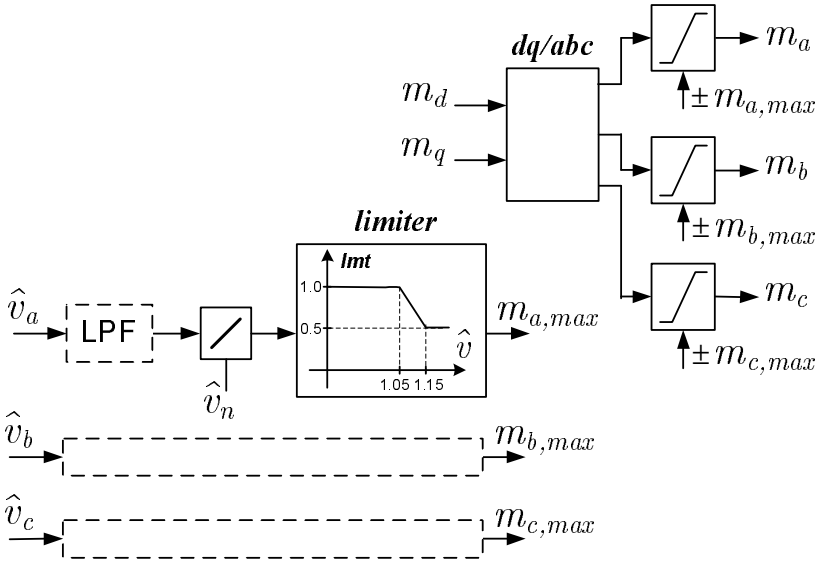

Figure 5.2: Schematic diagram of the proposed TOV mitigation technique.

the TOV at a specific acceptable range.

As shown in Figure 5.2, the peak value of three phase voltages, $\hat{v}_a$, $\hat{v}_b$, and $\hat{v}_c$, are measured and are normalized by dividing them by the nominal peak value of the grid voltage at the coupling point of the inverter, $\hat{v}_n$. The normalized values of the three phases are then applied to identical nonlinear transfer functions that produce the saturation levels, $m_{a,max}$, $m_{b,max}$, and $m_{c,max}$. These saturation levels, which are applied to the modulating signals' saturation blocks, decrease the modulating signal only when an overvoltage is detected. The low-pass filter (LPF) represents the intrinsic delay of the peak voltage measurement.

On the other hand, the individual control of the three phase voltages, both in the grid side and inverter side of the transformer, will not be possible unless a Y-Y transformer, grounded at both sides, is utilized. However, since the PV array, connected to the DC side of the inverter, is grounded in North American systems, the neutral point of the inverter-side winding of the transformer can not be connected to ground because of the potential difference between the DC-side ground and the AC-side neutral point; the AC-side reference potential is equal to the DC-link virtual mid-point potential, $v_{dc}/2$. Therefore, the neutral point of the inverter-side winding of the transformer is virtually grounded to the DC-link mid-point, by an extra switching leg, a half-bridge converter (HBC), which together with the conventional VSI form a four-leg inverter as shown in Figure 5.3. The HBC is operated at a constant duty cycle of 0.5 in order to provide the inverter DC-link mid-point potential $v_{dc}/2$ for the transformer neutral point. Further-

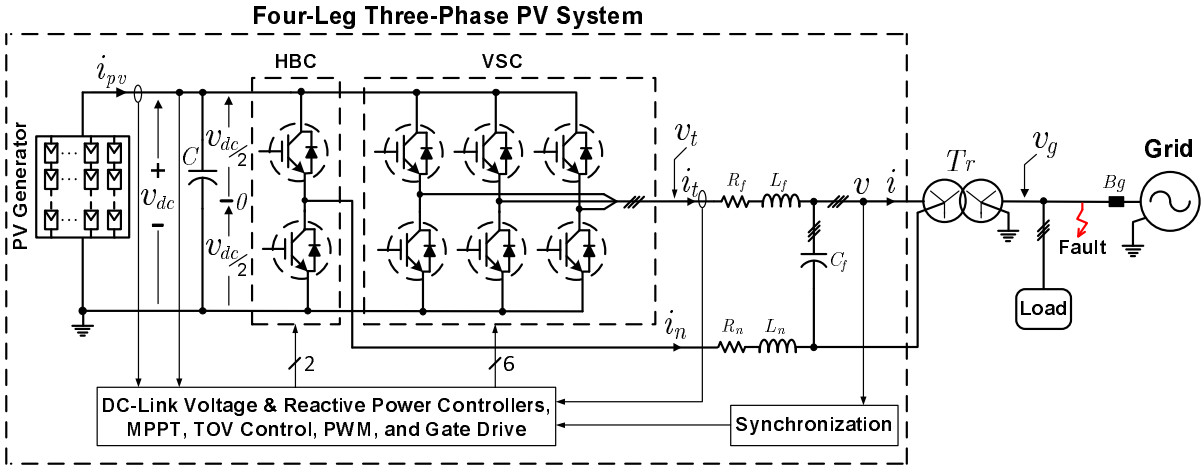

Figure 5.3: Schematic diagram of the proposed four-leg voltage-sourced inverter.

more, it is connected to the neutral point of the transformer through a small impedance, to limit the zero-sequence current from the inverter, and consequently to reduce the current rating of the switches employed in HBC. A Larger impedance reduces the control on individual phases and limits the TOV mitigation capability.

In the PV system under study, illustrated in Figure 5.3, the PV array is composed of many parallel- and series-connected modules and is modeled by the single-diode model discussed in [64] and [40]. The inverter modeling and control, including decoupled *dq*-frame current control, DC-link voltage regulator, and reactive-power control are similar to those discussed in [40], except for the need of a *dq*0-frame transformation, instead of the simplified *dq*-frame one. The *dq*0-frame transformation is required due to the existence of the zero-sequence current components in the four-wire structure of the three-phase inverter system. This is discussed in the following paragraphs. Further, as shown in Figure 5.3, the PV system utilizes an LC filter (composed of three-phase reactor, L_f, and capacitor, C_f) to reduce the low-order harmonic current components injected into the utility grid.

It is noted that the PV system, modeled here, utilizes only one transformer both to isolate the PV system from the grid and to step up the low-voltage output of the inverter to medium-voltage level to connect to the MV distribution network. This type of connection is practiced for the interconnection of high-power inverters to the grid. However, if two different transformers, an isolation transformer and a distribution one, are utilized, the same analysis will be valid for the control of the TOV provided that the distribution transformer has a YG/YG connection; this is required in order to independently control

the overvoltage of each three phases.

When the inverter is connected to an unbalanced grid through a four-wire Y connection, the inverter phase currents will include zero-sequence components, which in turn will introduce a nonzero transformer neutral potential. This requires the adaptation of a $dq0$-frame transformation instead of the well-known dq-frame one. The conversion of parameters between abc-frame and $dq0$-frame is achieved through [65]

$$f_{dq0} = K_s \times f_{abc} \tag{5.2}$$

and

$$f_{abc} = K_s^{-1} \times f_{dq0} \ , \tag{5.3}$$

where

$$K_s = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ \sin\theta & \sin(\theta - 2\pi/3) & \sin(\theta + 2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{5.4}$$

in which θ is the grid voltage angle that is approximated by the ρ, the angle synthesized by the PLL, as shown in Figure 5.1.

The inverter current model in $dq0$-frame was obtained from [41] and [66] and is shown in Figure 5.4, together with the proposed current loops. The zero-component loop is inherently decoupled from dq-component ones, while the d- and q-component loops, themselves, are decoupled by the addition of appropriate feed-forward signals. The zero-sequence impedance at the inverter terminals, denoted by R_0 and L_0 in Figure 5.4, are calculated as

$$R_0 = R_f + 3R_n \tag{5.5}$$

$$L_0 = L_f + 3L_n \tag{5.6}$$

As mentioned earlier, the DC voltage regulation is realized through the d-component current control loop and the q-component loop is utilized for reactive-power or power-factor regulation, as shown in Figure 5.4. The 0-component loop, however, can be used to control the zero-sequence components of the inverter voltage.

Although, the inverter utilizes one additional conversion leg, the current through that leg is negligible under the normal operating conditions and, therefore, the power loss over that extra leg will be negligible. Moreover, although the neutral current after fault is large, the current rating of the HBC is not too high since it conducts only a few cycles

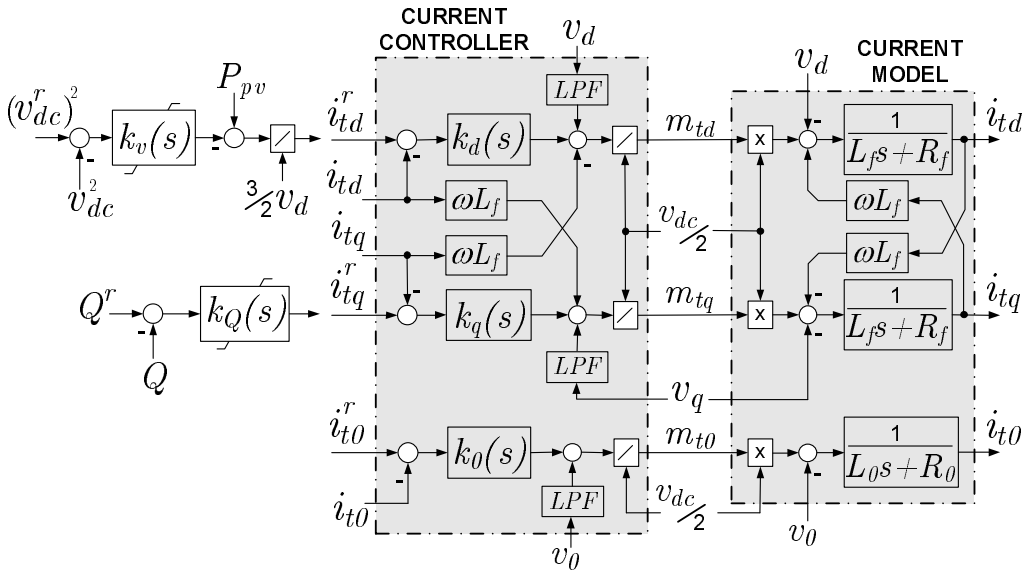

Figure 5.4: Schematic diagram of the current control in $dq0$-frame.

after fault and before the inverter is shot down immediately after islanding detection. Thus, the extra cost will not be high.

Furthermore, it is noted that the proposed technique suppresses all kinds of overvoltages within the inverter. Thus, the operation of the overvoltage detection algorithm utilized in the commonly used passive (overvoltage/undervoltage & overfrequency/underfrequency) islanding detection scheme will be incapacitated. Thus, other more complicated islanding detection techniques, like the one introduced in [67], will be required.

5.3 Simulation Results

To evaluate the effectiveness of the proposed TOV mitigation technique, a detailed switched model of the four-leg inverter-based PV system, shown in Figure 5.3, was simulated in PSCAD/EMTDC software environment [55]. The rating of the inverter and the transformer are 1.0 MVA, and the rating of the supplying PV array is 1.0 MW. The PV system is interfaced with a typical North American medium-voltage distribution network [63], however with reduced load impedances to realize a scenario with high amplitude of TOV. Parameters of the PV system, the network, and the aggregate load are given in Appendix E.

In order to demonstrate the performance of the proposed technique, first, a simulation result of the PV system without the implemented technique is given for comparison. Then, the response of the proposed technique will be shown and discussed.

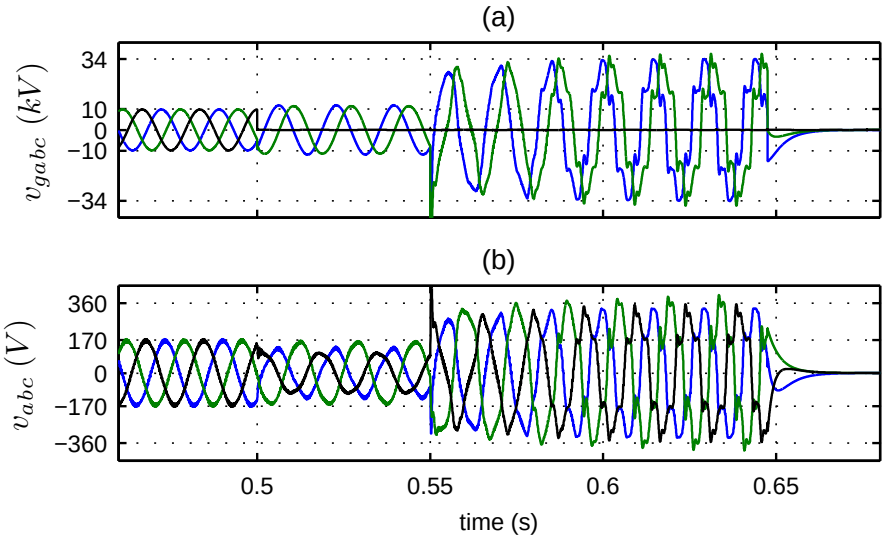

Figure 5.5: TOV produced in a PV system in response to a SLG fault followed by islanding (without the proposed TOV mitigation technique).

Figure 5.5 illustrates the response of the PV system, without the TOV mitigation technique, to consecutive fault and islanding incidents. A SLG fault takes place at $t = 0.5$ *sec* at the point shown in Figure 5.3. It is assumed that the substation protection circuitry detects the fault in 50 *ms* and opens the breaker B_g immediately. This islands the PV system at $t = 0.55$ *sec*. The PV system operates in islanded mode for 100 *ms* until it is disabled at $t = 0.65$ *sec* by its protection scheme, assuming that an effective islanding detection scheme was utilized. For a small load chosen to be supplied by the PV system during the islanded operation, overvoltages of 3.4 p.u. and 2.1 p.u. are produced in the grid side and inverter side of the transformer, respectively, as can be seen in Figures 3.7(a) and (b). A smaller local load results in a more severe TOV and a larger one produces a smaller TOV. This is in agreement with the interruption of significant power export mechanism explained in the Section 1.2.4.

The performance of the proposed technique is illustrated in Figure 3.8 through a similar case study, with the TOV mitigation technique implemented. The same sequence of events takes place and the same local load is utilized. As Figures 3.8(a) and (b) show, the magnitude of the overvoltages of both unfaulted phases are reduced and controlled to about 1.3 *p.u.* on both the grid side and the inverter side of the transformer. The voltage waveforms are not balanced and equal after islanding, since the PV system supplies an aggregate unbalanced load in this condition. Figure 3.8(c) shows the neutral point current, i_n. This current is relatively small during the normal operation of the inverter and

only assumes a large value, carrying the zero-sequence current and the current imbalance of the three phases during the fault condition. The current imbalance resulted from the fault and islanding produces ripples on the inverter output power waveform and DC-link voltage waveform as shown in Figures 3.8(d) and (e).

As explained earlier, a larger neutral line impedance, $R_n + j\omega L_n$, reduces the neutral line current and, consequently, the HBC switches' current rating (and the magnitude of ripples on output power and DC-link voltage waveforms under fault condition), but increases the TOV magnitude.

5.4 A Minimal Alternative

The TOV mitigation technique discussed earlier is an efficient solution to suppress any kind of overvoltage over any of three phases. It uses a four-leg inverter and needs a Y/YG isolation transformer. The cost of the extra leg and/or the type of isolation transformer might limit the adoption of the proposed technique in future inverters. For such cases, a minimal alternative is proposed, in which a considerable overvoltage mitigation is achieved for only a slight change in the inverter control, as illustrated in Figure 5.7. The amplitude of the three-phase voltage is calculated from $\sqrt{m_d^2 + m_q^2}$ and is normalized by dividing it by the nominal peak value of the grid voltage at the coupling point of the inverter, $\hat{v}_n$. Then, the normalized value is applied to a nonlinear transfer function, similar to the one used in Figure 5.3, which produces the saturation level, $m_{dq,max}$, which in this case is applied to m_d and m_q modulating signals, instead of the three-phase m_a, m_b, and m_c ones. Therefore the dq components of the voltages of the two sides of the transformer are controlled, instead of the individual three-phase voltages. Thus, the capability of the TOV mitigation is reduced, or the TOV amplitude is increased specially in grid side of the transformer, by a factor of up to $\sqrt{3}$. Figure 5.8 illustrates the response of the conventional three-leg three-phase inverter system, similar to the one shown in Figure 5.1, connected to grid through a Δ/Y isolation transformer. The same sequence of fault and islanding incidents, similar to that explained for the study cases in Section 5.3, is applied here and the same size load is being supplied by the PV system during the islanded operation. The three-phase voltages at the converter side of the transformer is effectively limited to about 1.26 *p.u.*, as seen in Figure 5.8(a), which shows a considerable improvement compared to the 2.1 *p.u.* from the unmitigated response seen in Figure 5.5(b). The three-phase voltages at the grid side of the transformer, however, are

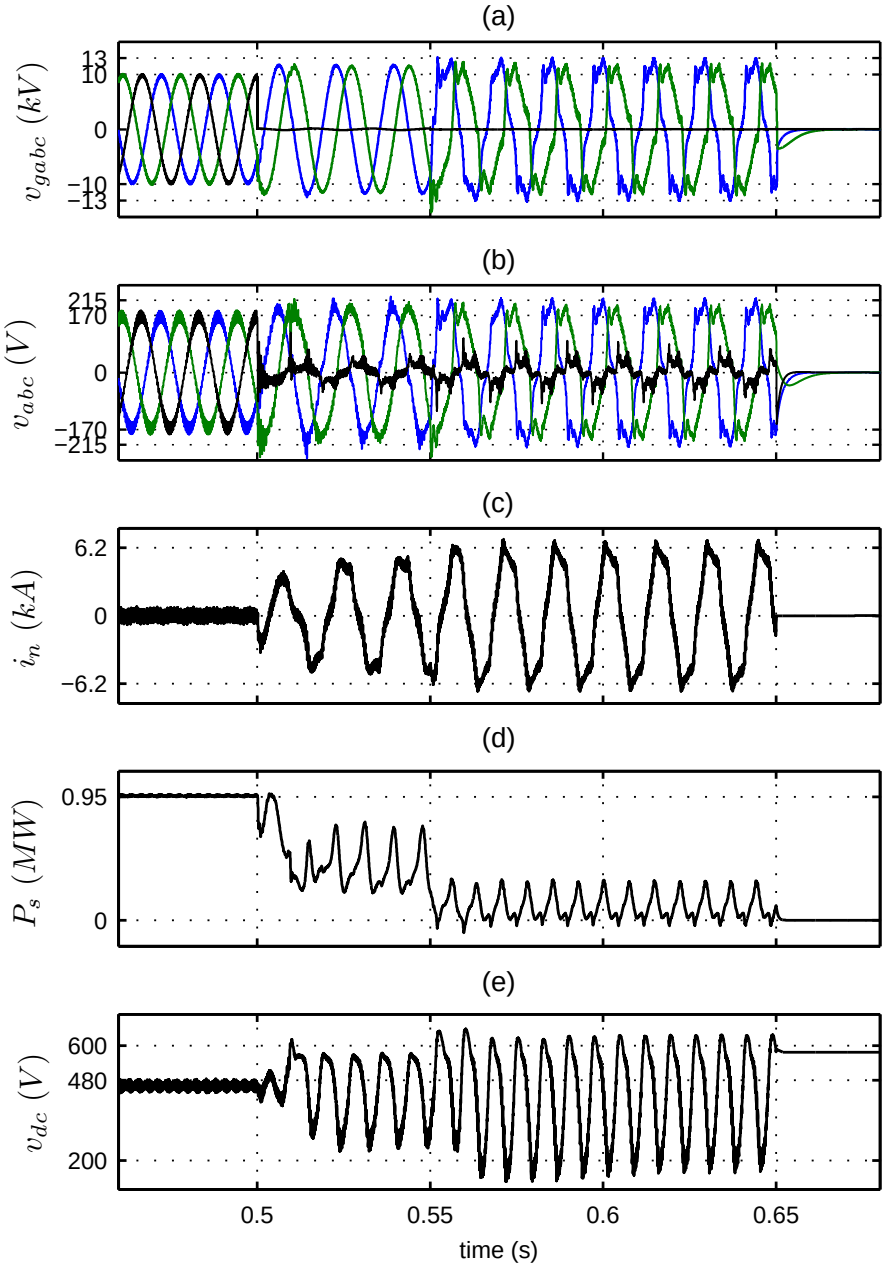

Figure 5.6: PV system response to a SLG fault followed by islanding, in presence of the proposed TOV mitigation technique.

limited to just 2.15 *p.u.*, as shown in Figure 5.8(b), which can still be a damaging TOV level, but are much better than the unmitigated level of 3.4 p.u. from Figure 5.5(a). The reason for such a high TOV is that the magnitude of one phase is almost zero, so the magnitude of the other unfaulted phases is equal to $\sqrt{3}$ of the 1.26 *p.u.* (the magnitude of the TOV in inverter side of the transformer). This is also seen in Figure 5.8(c) which

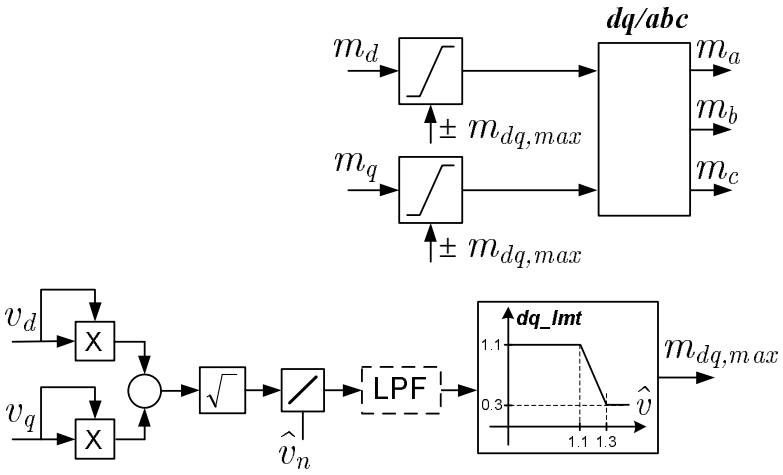

Figure 5.7: Schematic diagram of the minimal TOV mitigation technique.

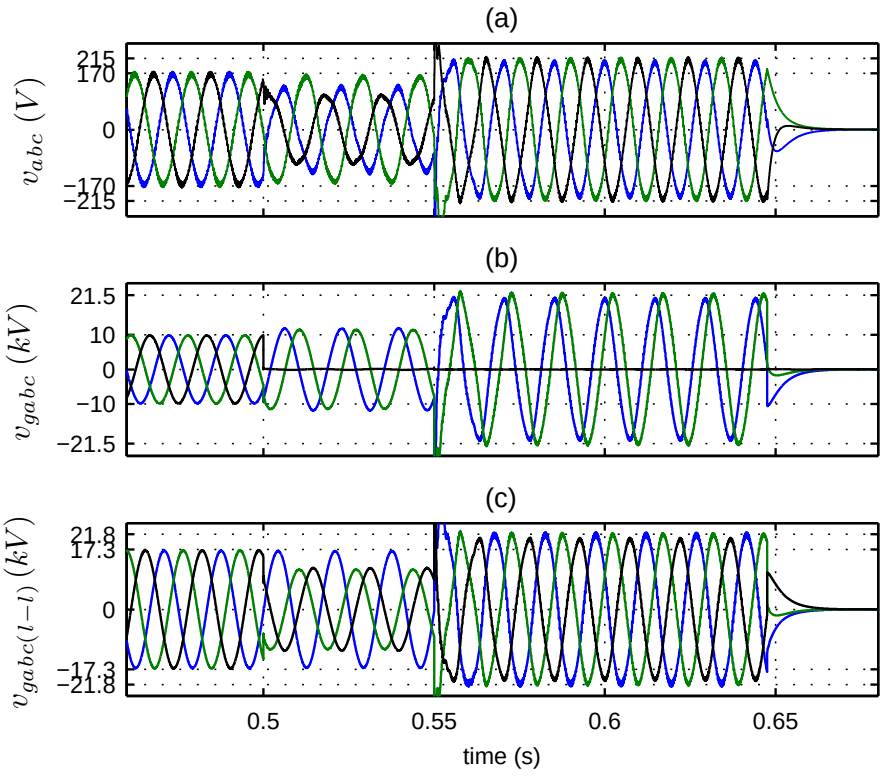

Figure 5.8: PV system response to a SLG fault followed by islanding, with the minimal TOV mitigation technique.

shows the line-to-line voltages limited to 1.26 *p.u.*.

5.5 Conclusion

A modification was proposed in the control structure of the voltage-sourced inverters, in order to limit the magnitude of, and thus to prevent the damages produced by, the TOV generated by inverter-based DGs, when a SLG fault occurs and is followed by an islanding. The proposed technique utilized a four-leg inverter and was connected to grid through a Y/YG isolation transformer, in order to control the overvoltage of each individual phase. The principles of the operation, the modeling of the system and the designed control loops were presented. The performance of the proposed structure was demonstrated by time-domain simulation studies conducted on a detailed switched model. An alternative minimal solution was also proposed to mitigate the overvoltage in the conventional three-leg VSI connected to grid through the Δ/Y isolation transformer.

Chapter 6

Summary, Conclusion and Future Works

6.1 Summary and Conclusion

This work focused on the improvement of the performance of the VSC-based PV interface systems for the large-scale grid-connected applications. The aim was to study the factors that limit, and to propose appropriate solutions to improve, the capacity, efficiency, power quality, and the safety of the grid-connected PV systems. Therefore,

- It was discussed, in Chapter 1, that the limit imposed by the safety standards on the maximum DC voltage (600 V for North American systems) limits the capacity and efficiency of large-scale PV systems.
- It was shown by simulation results, in Chapter 2, that the efficiency of PV arrays, especially under partial shading and characteristic mismatch, are affected by their interconnection structure, and that the total cross-tied configuration delivers the highest energy yield.
- Further, a two-MPPT structure was proposed to improve the efficiency under partial shading and characteristic mismatch, by splitting the PV array into two sub-arrays and performing their maximum power point tracking independently.
- In Chapter 3, a single-stage three-phase voltage-sourced inverter, which was realized by parallel connection of an auxiliary half-bridge converter to the DC link of a conventional single-stage PV system, was proposed to utilize the two-MPPT

structure to improve the overall efficiency under partial shading and characteristic mismatch.

- The proposed system was bipolar and doubled the DC-link voltage to improve the inverter capacity and performance while respecting the 600 V North American standard.

- In Chapter 4, a two-stage PV system was proposed to address the variable MPP voltage of the PV array which further limited the voltage rating of the single-stage inverters. A boost DC-DC converter was used to fix the variable voltage of the array to a fixed large voltage (slightly lower than the maximum permissible voltage, i.e., 600 V in North America) in order to increase the capacity of the inverter. The two-MPPT and bipolar structures were also utilized to further improve the capacity, efficiency, and performance.

- The two-stage system used the three-level NPC as its central inverter which produced output power with better quality (less THD) and utilized low-voltage switches (half-rated, compared to the conventional VSI) for the inverter, despite the doubled net DC voltage.

- The proposed two-stage system, also offered distributed and modular concept, through interfacing smaller PV sub-arrays with central inverter using dedicated boost DC-DC converters, which delivered better efficiency under partial shading and the possibility of utilizing PV modules of different types, ratings, and alignments.

- A modification was proposed in boost converter control scheme to limit the DC-link voltage of the inverter if the power cannot be dispatched to the grid, for example, due to network faults or failure of the inverter.

- A modified third-order harmonic injected PWM was utilized for the NPC inverter in order to reduce the third-order harmonic ripples of the partial DC voltages which otherwise limited the voltage rating and, consequently, the power capacity of the inverter.

- To design the controller schemes of the two-stage three-level NPC-based PV system, the mathematical model of the DC side of the NPC inverter was derived in

Appendix A, for the unique application condition in Chapter 4 in which the two DC power sources connected to NPC inverter were not identical.

- In Chapter 5, a temporary overvoltage mitigation technique was proposed for PV and other inverter-based distributed generators. The technique, which prevented the formation of any overvoltage on any of the three phases, utilized a four-leg inverter connected to grid through a Y/YG isolation transformer with a slight modification on the control structure of the inverter.

- A less effective TOV mitigation technique, as a minimal alternative, was also proposed for the conventional three-leg inverter connected through widely utilized Δ/YG isolation transformer to reduce the magnitude of the TOV.

6.2 Future Works

The following topics are suggested for future work:

- Developing models for real shadows of different shapes and sizes to study and simulate the mismatch power loss in large-scale PV arrays, of different sizes and interconnection types, using real insolation data; in this study, limited number of standard shading scenarios (of 1, 2, or 4 modules) were applied to an 8x8 array.

- Developing a more detailed model for the PV system, which includes all types of power losses in the system including the array mismatch power loss (from partial shading and ...), switching loss, and ohmic loss (on switches, DC wirings, AC wirings, and transformer) in order to compare the overall efficiency of single-stage systems (discussed in Chapter 3) and two-stage ones (discussed in Chapter 4); in this study the PSCAD model did not consider the switching loss. The optimum number of the sub-arrays and DC-DC converters can also be calculated by using such a model, in two-stage systems.

- Implementing an islanding detection scheme/strategy which effectively detects and isolates the PV system from power network, while utilizing the proposed TOV mitigation technique in Chapter 5.

Appendix A

Mathematical Modeling of the Three-Level NPC Inverter with Two Independent DC Sources

A.1 Introduction

The three-level NPC inverter offers advantages over the conventional two-level VSI, and has thus found many utility and industrial applications [31, 33]. Compared to the two-level NPC inverter, the semiconductor switches in a three-level NPC inverter are required to withstand only half the net DC-link voltage. Further, a three-level NPC inverter can simultaneously interface two independent DC sources with an AC grid. For example, the photovoltaic (PV) array of a grid-connected PV system can be split into two sub-arrays, for independent control and enhanced maximum power-point tracking (MPPT) [64]; Figure A.1 illustrates a possible implementation where the two PV sub-arrays are controlled by two corresponding DC-DC converters [68], before they are interfaced with the grid through the three-level NPC inverter.

To ensure high quality power production, the partial DC-side voltages of the NPC inverter should be kept equal. Commonly, the NPC inverter is supplied by a single DC power source, and the partial DC-side voltages are tapped from a capacitive voltage divider. Consequently, any DC component in the inverter mid-point current causes the partial DC-side voltages to drift, which affects the quality of the output power and can result in damages to the semiconductor switches. To resolve the issue, i.e., to balance the partial DC-side voltages, a small DC offset is added to the modulating signals of

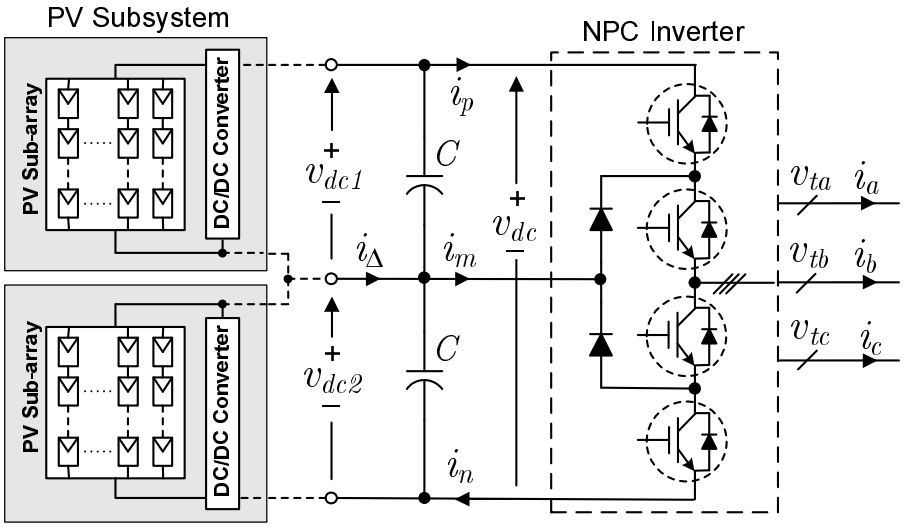

Figure A.1: Schematic diagram of a three-phase three-level NPC inverter, supplied by two PV subsystems.

the inverter [69, 70]. The offset results in the generation of a DC component in the mid-point current and balances the partial DC-side voltages. Reference [60] has derived a formula explaining the partial DC-side voltages and mid-point current for the NPC inverter, based on the assumption of a small DC offset for the modulating signals of the inverter.

If the NPC inverter is energized by two independent DC sources, for instance by two PV subsystems, the mid-point current of the inverter includes the current difference between the upper and lower DC sources, given that the partial DC-side voltages are equalized (to circumvent AC voltage harmonic distortions). This potentially large difference between the currents of the two sources corresponds to a large mid-point current, and calls for a large DC offset for the modulating signals of the inverter, a condition that has not been addressed in the literature, to the authors' best of knowledge.

Another issue is that the mid-point current and, consequently, the partial DC-side voltages of an NPC inverter include harmonic components of multiples of 3. Although the harmonic components of the partial DC-side voltages are anti-phaseal and therefore leave the net DC-link voltage almost free of distortions, they affect the voltage rating of, and impose additional voltage stress on, the semiconductor switches of the inverter. As shown in [71] and [62], the application of third-order harmonic injected PWM substantially reduces the aforementioned harmonic components. Moreover, compared to the conventional PWM, the third-order harmonic injected PWM enhances the maximum DC-to-AC voltage gain of the inverter.

This chapter develops a mathematical model for the mid-point current of the three-level NPC inverter. The model is based on the assumption that the mid-point current can have a large DC component; this would be the case if the NPC inverter serves as the central inverter in PV systems with two PV sub-arrays/subsystems for enhanced energy production. The developed model does not assume that the corrective DC offset of the PWM modulating signals are small, and also characterizes the major harmonic components of the mid-point current.

A.2 Mathematic Model of the NPC Inverter

The PWM modulating signals for an NPC inverter are in general of the form

$$\begin{cases} m_a(t) = m_0 + \widehat{m}\cos[\varepsilon(t)] - k\widehat{m}\cos[3\varepsilon(t)] \\ m_b(t) = m_0 + \widehat{m}\cos[\varepsilon(t) - 2\pi/3] - k\widehat{m}\cos[3\varepsilon(t)] \\ m_c(t) = m_0 + \widehat{m}\cos[\varepsilon(t) - 4\pi/3] - k\widehat{m}\cos[3\varepsilon(t)] \end{cases} \tag{A.1}$$

where m_0 is a DC offset, $\widehat{m}$ is the amplitude of the fundamental sinusoidal component, and k is the amplitude of the third-order harmonic component normalized to the amplitude of the fundamental component; $k = 1/6$ for the conventional third-order harmonic injected PWM [60, 71]. Assuming sufficient filtering the AC-side current of the inverter is characterized by:

$$\begin{cases} i_a(t) = \widehat{i}\cos[\varepsilon(t) - \gamma] \\ i_b(t) = \widehat{i}\cos[\varepsilon(t) - \gamma - 2\pi/3] \\ i_c(t) = \widehat{i}\cos[\varepsilon(t) - \gamma - 4\pi/3] \end{cases} \tag{A.2}$$

where $\widehat{i}$ denotes the amplitude of the current, and γ is the phase angle of the current relative to the fundamental component of the AC-side terminal voltage of the inverter. Assuming a three-wire connection at the AC-side of the NPC inverter, the DC-side mid-point current is calculated from [60]

$$i_m(t) = -[f_a(t) + f_b(t) + f_c(t)] \tag{A.3}$$

where

$$\begin{cases} f_a(t) = m_a(t) i_a(t)[sgn(m_a) - sgn(-m_a)] \\ f_b(t) = m_b(t) i_b(t)[sgn(m_b) - sgn(-m_b)] \\ f_c(t) = m_c(t) i_c(t)[sgn(m_c) - sgn(-m_c)] \end{cases} \tag{A.4}$$

the function $sgn(.)$ is defined as

$$sgn(x) = \begin{cases} 1 & for \quad x \geq 0 \\ 0 & for \quad x < 0 \end{cases} \tag{A.5}$$

In a balanced system, $f_b(t)$ and $f_c(t)$ have the same forms as that of $f_a(t)$, but are shifted by, respectively, $2\pi/3$ and $4\pi/3$ rad., relative to $f_a(t)$. Therefore, their sum equals zero for all harmonics other than the DC and multiples of 3:

$$i_m(t) = -3 f_a(t) \tag{A.6}$$

Substituting for $m_a(t)$ and $i_a(t)$ into (A.4), respectively from (A.1) and (A.2), one deduces

$$\begin{aligned} f_a(t) = & \Big\{ m_0 \widehat{i} \cos[\varepsilon(t) - \gamma] + \frac{\widehat{m}\widehat{i}}{2} \cos[2\varepsilon(t) - \gamma] + \frac{\widehat{m}\widehat{i}}{2} \cos(-\gamma) \\ & - \frac{k\widehat{m}\widehat{i}}{2} \cos[4\varepsilon(t) - \gamma] - \frac{k\widehat{m}\widehat{i}}{2} \cos[2\varepsilon(t) + \gamma] \Big\} \\ & \times [sgn(m_a) - sgn(-m_a)] \end{aligned} \tag{A.7}$$

The function $[sgn(m_a) - sgn(-m_a)]$ can be expanded by Fourier series. As Figure A.2 illustrates, the slope of the $m_a(\varepsilon)$ at the angle $\varepsilon = \pi/2$ is equal to

$$slope\ of\ m_a \Big|_{\varepsilon=\pi/2} \simeq -\frac{m_0}{\Delta\theta} \tag{A.8}$$

where $\Delta\theta$, as Figure A.2 indicates, is the difference between $\pi/2$ and the angle at which $m_a(\varepsilon)$ crosses zero. The slope of $m_a(\varepsilon)$ at $\varepsilon = \pi/2$ can also be calculated by evaluating the derivative of (A.1) with respect to ε, at $\varepsilon = \pi/2$:

$$slope\ of\ m_a\ at\ (\varepsilon = \pi/2)\ = \frac{dm_a(t)}{d\varepsilon} \Big|_{\varepsilon=\pi/2} = -\widehat{m}(1 + 3k) \tag{A.9}$$

Combining (A.8) and (A.9), one finds

$$\Delta\theta \simeq \frac{m_0}{(1+3k)\widehat{m}} \tag{A.10}$$

Knowing the zero-crossing points of $m_a(\varepsilon)$ at $\pi/2+\Delta\theta$ and $3\pi/2-\Delta\theta$, one can calculate the Fourier series of $[sgn(m_a) - sgn(-m_a)]$ as

$$\begin{aligned}
&[sgn(m_a) - sgn(-m_a)] \\
&\quad = \frac{2\Delta\theta}{\pi} + \frac{4}{\pi}\sum_{h=1,2,3,\ldots}^{+\infty}\frac{1}{h}\sin\left(\frac{h\pi}{2}+h\Delta\theta\right)\cos(h\varepsilon)
\end{aligned} \tag{A.11}$$

Substituting for $[sgn(m_a) - sgn(-m_a)]$ from (A.11) into (A.7), one gets

$$\begin{aligned}
f_a(t) =& \frac{\Delta\theta\widehat{m}\widehat{i}}{\pi}\cos\gamma + \frac{2\Delta\theta m_0\widehat{i}}{\pi}\cos(\varepsilon-\gamma) \\
&+ \frac{\Delta\theta\widehat{m}\widehat{i}}{\pi}\cos(2\varepsilon-\gamma) - \frac{k\Delta\theta\widehat{m}\widehat{i}}{\pi}\cos(4\varepsilon-\gamma) \\
&- \frac{k\Delta\theta\widehat{m}\widehat{i}}{\pi}\cos(2\varepsilon+\gamma) \\
&+ \frac{2\widehat{m}\widehat{i}}{\pi}\cos\gamma\sum_{h=1,2,\ldots}^{+\infty}\frac{1}{h}\sin\left(\frac{h\pi}{2}+h\Delta\theta\right)\cos(h\varepsilon) \\
&+ \frac{2m_0\widehat{i}}{\pi}\sum_{h=1,2,\ldots}^{+\infty}\frac{1}{h}\sin\left(\frac{h\pi}{2}+h\Delta\theta\right) \\
&\quad\times\{\cos[(h+1)\varepsilon-\gamma]+\cos[(h-1)\varepsilon+\gamma]\} \\
&+ \frac{\widehat{m}\widehat{i}}{\pi}\sum_{h=1,2,\ldots}^{+\infty}\frac{1}{h}\sin\left(\frac{h\pi}{2}+h\Delta\theta\right) \\
&\quad\times\{\cos[(h-2)\varepsilon+\gamma]+\cos[(h+2)\varepsilon-\gamma]\} \\
&- \frac{k\widehat{m}\widehat{i}}{\pi}\sum_{h=1,2,\ldots}^{+\infty}\frac{1}{h}\sin\left(\frac{h\pi}{2}+h\Delta\theta\right) \\
&\quad\times\{\cos[(h-4)\varepsilon+\gamma]+\cos[(h+4)\varepsilon-\gamma]\} \\
&- \frac{k\widehat{m}\widehat{i}}{\pi}\sum_{h=1,2,\ldots}^{+\infty}\frac{1}{h}\sin\left(\frac{h\pi}{2}+h\Delta\theta\right) \\
&\quad\times\{\cos[(h-2)\varepsilon-\gamma]+\cos[(h+2)\varepsilon+\gamma]\}
\end{aligned} \tag{A.12}$$

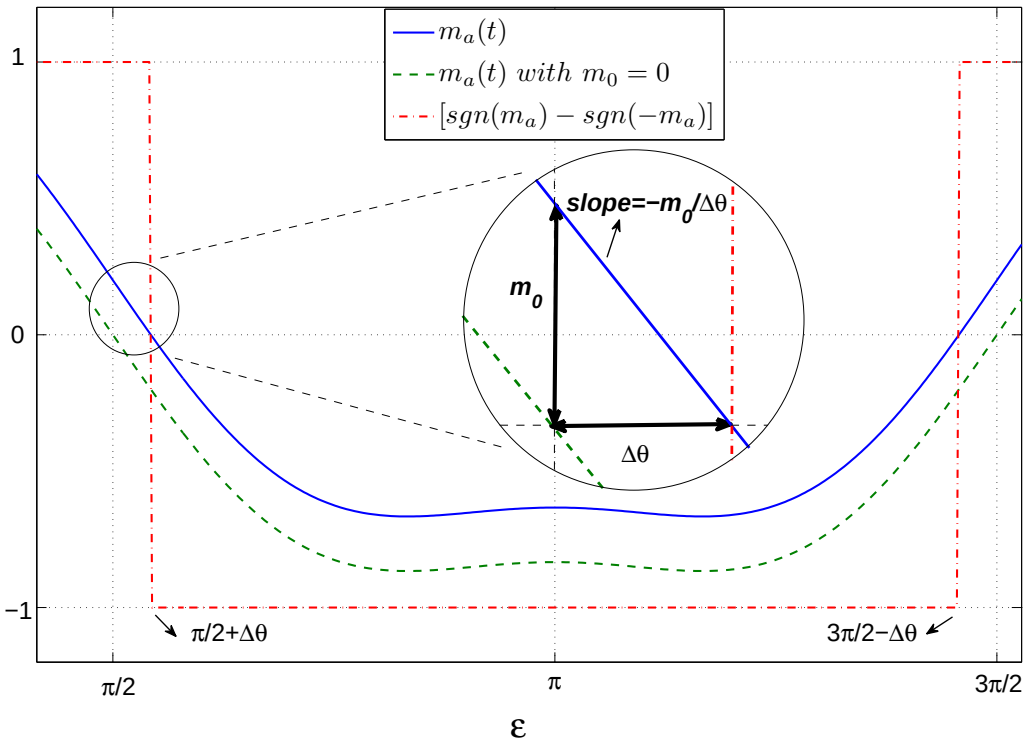

Figure A.2: Diagram illustrating the function $[sgn(m_a) - sgn(-m_a)]$.

Then, based on (A.6) and (A.12), the DC component and the harmonic components (of multiples of 3) of the mid-point current can be calculated; let us write them in the form

$$i_m = -3f_a(t) = \langle i_m \rangle_0 + \langle i_m \rangle_3 + \langle i_m \rangle_6 + ... \tag{A.13}$$

where the operator $\langle . \rangle_n$ denotes the amplitude of nth harmonic.

A.2.1 DC value of the mid-point current

The DC component of the mid-point current is calculated as

$$\begin{aligned}\langle i_m \rangle_0 = \Bigg[&- \frac{6m_0\widehat{i}}{\pi}\cos(\Delta\theta) - \frac{3\Delta\theta\widehat{m}\widehat{i}}{\pi} + \frac{3\widehat{m}\widehat{i}}{2\pi}\sin(2\Delta\theta) \\ &+ \frac{3k\widehat{m}\widehat{i}}{4\pi}\sin(4\Delta\theta) - \frac{3k\widehat{m}\widehat{i}}{2\pi}\sin(2\Delta\theta)\Bigg]\cos\gamma\end{aligned} \tag{A.14}$$

and if $\langle i_m \rangle_0$ is expressed in the form

$$\langle i_m \rangle_0 = -\frac{A_{dc}\, m_0\widehat{i}}{\pi}\cos\gamma\ . \tag{A.15}$$

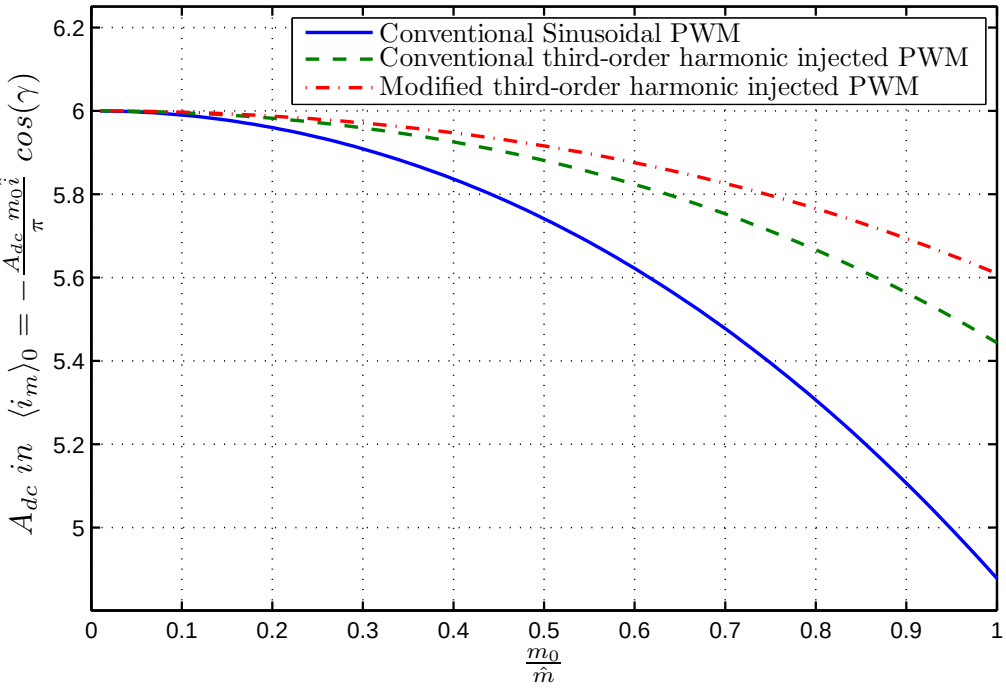

Figure A.3: Plot of A_{dc} versus $m_0/\widehat{m}$.

then the coefficient A_{dc} is

$$A_{dc} = 6\cos(\Delta\theta) + \frac{12\Delta\theta + 6(k-1)\sin(2\Delta\theta) - 3k\sin(4\Delta\theta)}{4(1+3k)\Delta\theta} \tag{A.16}$$

Figure A.3 depicts A_{dc} as a function of $m_0/\widehat{m}$, for the conventional PWM, conventional third-order harmonic injected PWM ($k = 1/6$) [71], and a modified version of the third-order harmonic injected PWM corresponding to $k = 7/27$; the modified third-order harmonic injected PWM eliminates the third-order harmonic ripples of the mid-point current [62]. As Figure A.3 shows, A_{dc} equals 6 in all three cases if $m_0 = 0$, but decreases as m_0 becomes larger. However, the ratio $m_0/\widehat{m}$ is considerably smaller than 0.5 in most applications. Therefore, A_{dc} is close to 6, especially if the two aforementioned third-order harmonic injected PWM techniques are employed, and can thus be considered a constant value (i.e., equal to 6) in most designs.

A.2.2 Third-order harmonic of the mid-point current

The third-order harmonic component of the mid-point current is calculated using (A.12) and (A.13), as

$$\langle i_m \rangle_3 = A_1 \, \widehat{mi} \cos\gamma \cos(3\varepsilon) + A_2 \, \widehat{mi} \sin\gamma \sin(3\varepsilon) \tag{A.17}$$

where

$$\begin{aligned} A_1 =& \frac{3+9k}{2\pi}\Delta\theta\left[2\sin(2\Delta\theta) - \sin(4\Delta\theta)\right] + \frac{6k-3}{\pi}\cos(\Delta\theta) \\ &+ \frac{2}{\pi}\cos(3\Delta\theta) + \frac{3k-3}{5\pi}\cos(5\Delta\theta) - \frac{3k}{7\pi}\cos(7\Delta\theta) \end{aligned} \tag{A.18}$$

$$\begin{aligned} A_2 =& \frac{3+9k}{2\pi}\Delta\theta\left[2\sin(2\Delta\theta) + \sin(4\Delta\theta)\right] - \frac{3}{\pi}\cos(\Delta\theta) \\ &+ \frac{3k+3}{5\pi}\cos(5\Delta\theta) + \frac{3k}{7\pi}\cos(7\Delta\theta) \ . \end{aligned} \tag{A.19}$$

Equation (A.17) can also be written in the form

$$\langle i_m \rangle_3 = A_{r3} \, \widehat{mi} \cos\left[3\varepsilon(t) + \zeta_1\right] \tag{A.20}$$

where

$$A_{r3} = \sqrt{A_1^2 \cos^2\gamma + A_2^2 \sin^2\gamma} \tag{A.21}$$

For conventional sinusoidal PWM, the amplitude of the third-order harmonic of the mid-point current is in the range

$$0.5093\widehat{mi} \leq \langle i_m \rangle_3 \leq 0.7639\widehat{mi} \tag{A.22}$$

where the minimum value, which corresponds to the unity power factor operation of the inverter (at the inverter AC-side terminals), is fairly large and can produce large third-order harmonic ripples in the partial DC-side voltages. By contrast, for the conventional third-order harmonic injected PWM technique [71], i.e., if $k = 1/6$, the amplitude of the

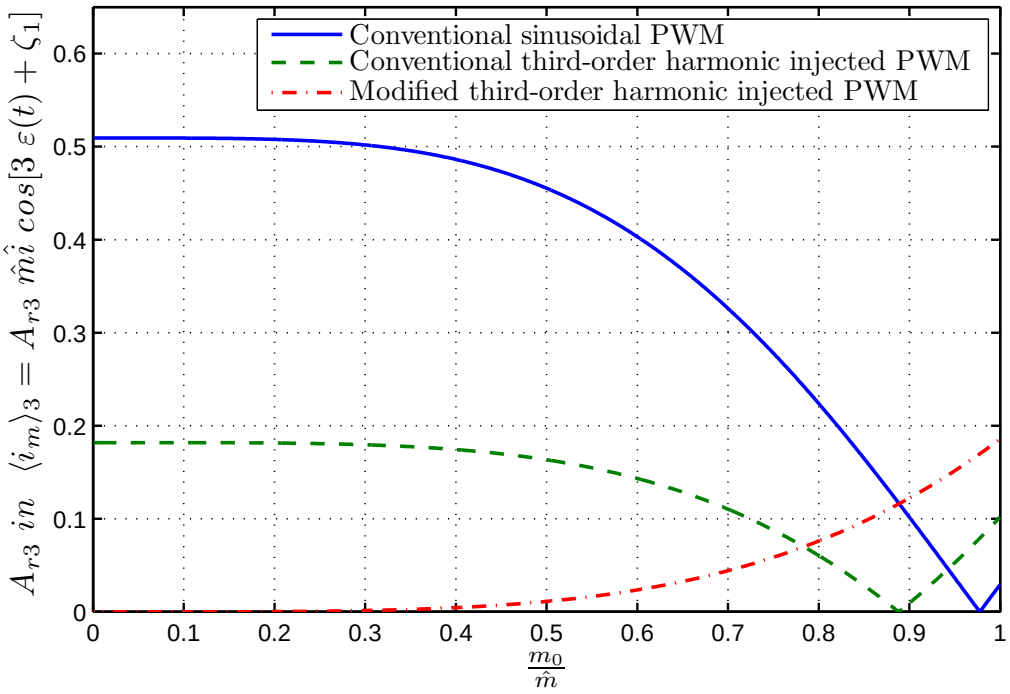

Figure A.4: Plot of A_{r3} versus $m_0/\widehat{m}$, for $\cos\gamma = 1$.

third-order harmonic component lies within the range

$$0.1819\widehat{mi} \leq \langle i_m\rangle_3 \leq 0.7094\widehat{mi} \tag{A.23}$$

which has a considerably smaller lower bound for unity power factor operation. The third-order harmonic ripples can be reduced further if, for a given power factor, k is chosen in such a way that A_{r3} in (A.21) becomes very small. For unity power factor operation, i.e., if $\cos\gamma = 1$, the third-order harmonic ripples are theoretically eliminates if $k = 7/27$ [62], and the range for the amplitude of the third-order harmonic becomes

$$0 \leq \langle i_m\rangle_3 \leq 0.6791\widehat{mi}\ . \tag{A.24}$$

Figure A.4 plots the coefficient A_{r3} versus $m_0/\widehat{m}$, for the three aforementioned PWM strategies and the unity power factor ($\cos\gamma = 1$).

As (A.21) indicates, the amplitude of the third-order current harmonic depends on the power factor; it increases as the power factor deviates from unity. This is illustrated in Figure A.5 where A_{r3} is plotted as a function of $m_0/\widehat{m}$, for $\cos\gamma = 0.95$. A comparison between Figure A.4 and Figure A.5 reveals that, for a given $m_0/\widehat{m}$, the coefficient A_{r3} is larger for $\cos\gamma = 0.95$ than for $\cos\gamma = 1$. This is especially the case if the modified

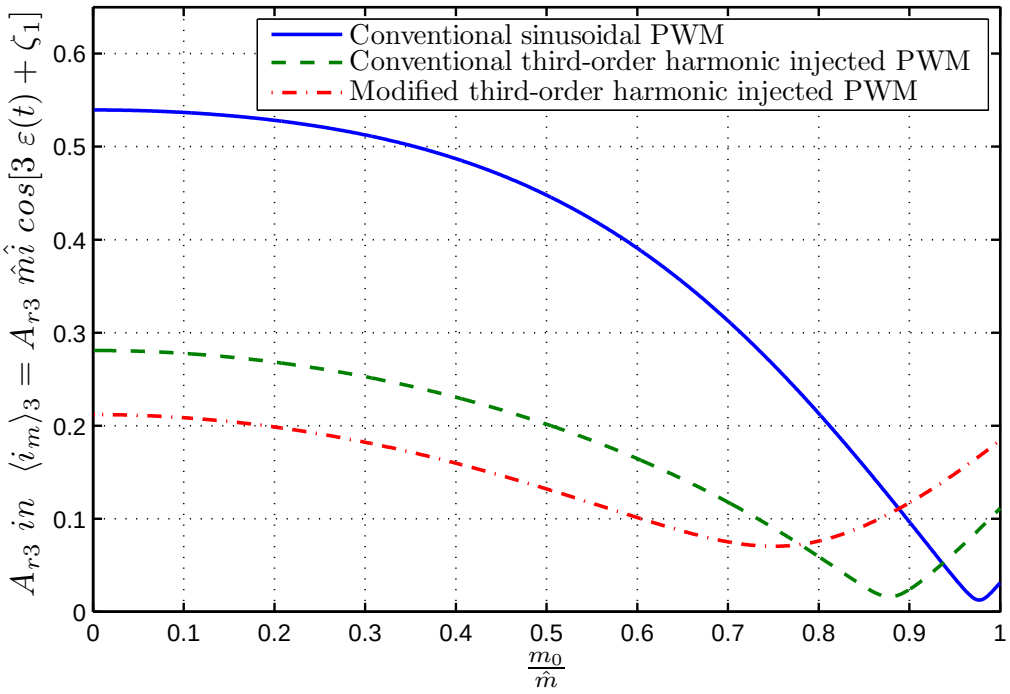

Figure A.5: Plot of A_{r3} versus $m_0/\widehat{m}$, for $\cos\gamma = 0.95$.

third-order harmonic injected PWM is employed.

A.2.3 Sixth-order harmonic of the mid-point current

The sixth-order harmonic component of the mid-point current is calculated based on (A.12) and (A.13), as

$$\langle i_m\rangle_6 = B_1\ \widehat{mi}\cos\gamma\cos(6\varepsilon) + B_2\ \widehat{mi}\sin\gamma\sin(6\varepsilon) \tag{A.25}$$

where

$$\begin{aligned} B_1 =& 6(1+3k)\Delta\theta\left[\frac{-1}{5\pi}\cos(5\Delta\theta) + \frac{1}{7\pi}\cos(7\Delta\theta)\right] \\ &- \frac{3k}{2\pi}\sin(2\Delta\theta) + \frac{3k-3}{4\pi}\sin(4\Delta\theta) + \frac{1}{\pi}\sin(6\Delta\theta) \\ &+ \frac{3k-3}{8\pi}\sin(8\Delta\theta) - \frac{3k}{10\pi}\sin(10\Delta\theta) \end{aligned} \tag{A.26}$$

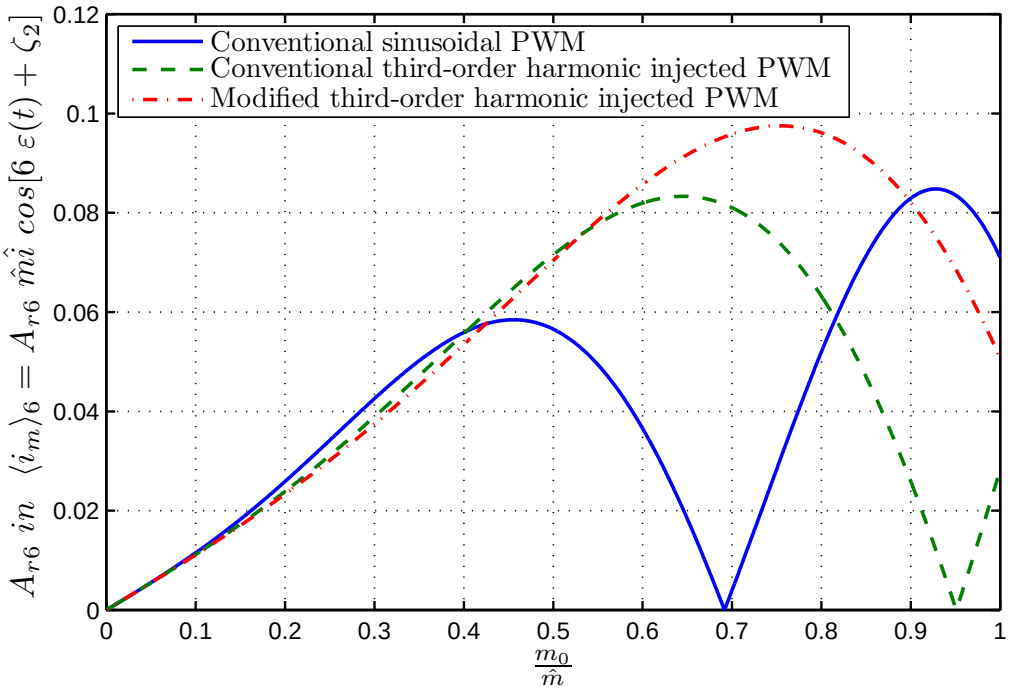

Figure A.6: Plot of A_{r6} versus $m_0/\widehat{m}$, for $\cos\gamma = 1$.

$$\begin{aligned} B_2 =& 6(1+3k)\Delta\theta \left[\frac{-1}{5\pi}\cos(5\Delta\theta) - \frac{1}{7\pi}\cos(7\Delta\theta)\right] \\ & - \frac{3k}{2\pi}\sin(2\Delta\theta) - \frac{3k+3}{4\pi}\sin(4\Delta\theta) \\ & + \frac{3k+3}{8\pi}\sin(8\Delta\theta) + \frac{3k}{10\pi}\sin(10\Delta\theta)\ . \end{aligned} \tag{A.27}$$

Equation (A.25) can be written in the form

$$\langle i_m\rangle_6 = A_{r6}\ \widehat{m}\widehat{i}\cos[6\varepsilon(t) + \zeta_2] \tag{A.28}$$

where

$$A_{r6} = \sqrt{B_1^2\cos^2\gamma + B_2^2\sin^2\gamma}\ . \tag{A.29}$$

Figure A.6 illustrates the coefficient A_{r6} as a function of $m_0/\widehat{m}$, for the three aforementioned PWM strategies and the unity power factor ($\cos\gamma = 1$). As Figure A.6 shows, A_{r6} is zero for $m_0 = 0$, but increases as $m_0/\widehat{m}$ becomes larger.

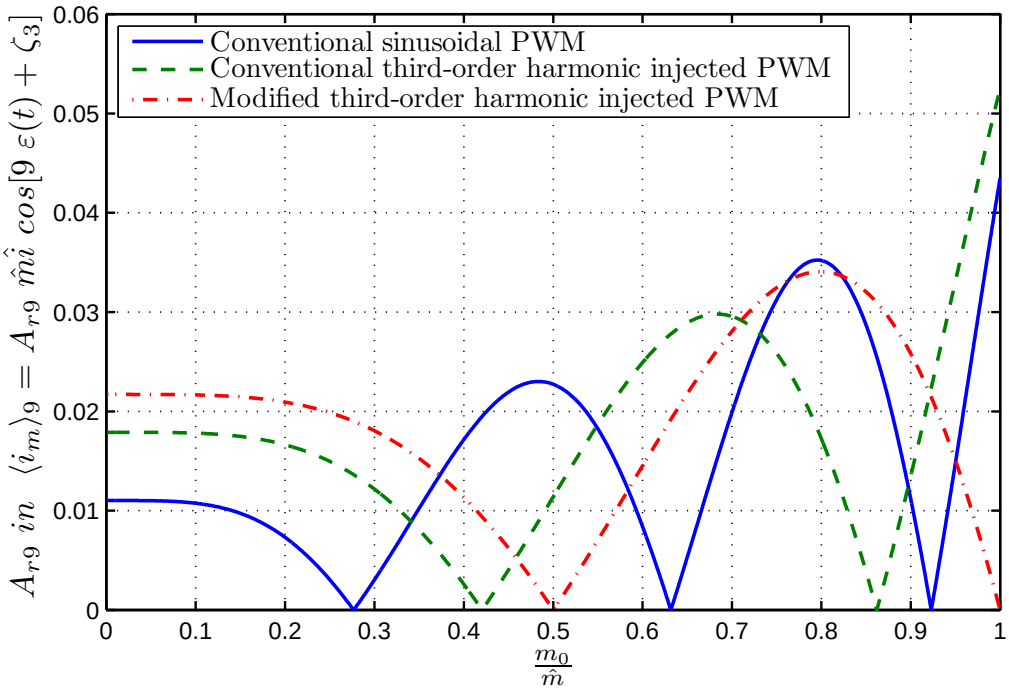

Figure A.7: Plot of A_{r9} versus $m_0/\widehat{m}$, for $\cos\gamma = 1$.

A.2.4 Ninth-order harmonic of the mid-point current

The ninth-order harmonic component of the mid-point current is calculated, using (A.12) and (A.13), as

$$\langle i_m\rangle_9 = C_1\ \widehat{mi}\cos\gamma\cos(9\varepsilon) + C_2\ \widehat{mi}\sin\gamma\sin(9\varepsilon) \tag{A.30}$$

where

$$\begin{aligned} C_1 =& 3(1+3k)\Delta\theta\left[\frac{-1}{4\pi}\sin(8\Delta\theta) + \frac{1}{5\pi}\sin(10\Delta\theta)\right] \\ &+ \frac{3k}{5\pi}\cos(5\Delta\theta) + \frac{3-3k}{7\pi}\cos(7\Delta\theta) - \frac{2}{3\pi}\cos(9\Delta\theta) \\ &+ \frac{3-3k}{11\pi}\cos(11\Delta\theta) + \frac{3k}{13\pi}\cos(13\Delta\theta) \end{aligned} \tag{A.31}$$

$$\begin{aligned} C_2 =& 3(1+3k)\Delta\theta\left[\frac{-1}{4\pi}\sin(8\Delta\theta) - \frac{1}{5\pi}\sin(10\Delta\theta)\right] \\ &+ \frac{3k}{5\pi}\cos(5\Delta\theta) + \frac{3k+3}{7\pi}\cos(7\Delta\theta) \\ &- \frac{3k+3}{11\pi}\cos(11\Delta\theta) - \frac{3k}{13\pi}\cos(13\Delta\theta)\ . \end{aligned} \tag{A.32}$$

Equation (A.30) can be written in the form

$$\langle i_m \rangle_9 = A_{r9}\ \widehat{m}\widehat{i}\cos[9\varepsilon(t) + \zeta_3] \tag{A.33}$$

where

$$A_{r9} = \sqrt{C_1^2 \cos^2\gamma + C_2^2 \sin^2\gamma}\ . \tag{A.34}$$

Figure A.7 plots the coefficient A_{r9} versus $m_0/\widehat{m}$, for the three aforementioned PWM strategies and the unity power factor ($\cos\gamma = 1$). Comparing Figure A.4, Figure A.6, and Figure A.7, one notices that, for small values of $m_0/\widehat{m}$, the ninth-order component is the second largest harmonic component of the mid-point current, after the third-order component.

A.2.5 Harmonic ripples of partial DC-side voltages

The mid-point current ripples translate into corresponding voltage ripples on the partial DC-side voltages, v_{dc1} and v_{dc2} [refer to Figure A.1]:

$$\begin{aligned} v_{dc1} = \frac{v_{dc}}{2} &+ V_{r3} sin(3\omega t + \zeta_4) + V_{r6} sin(6\omega t + \zeta_5) \\ &+ V_{r9} sin(9\omega t + \zeta_6) + ... \end{aligned} \tag{A.35}$$

$$\begin{aligned} v_{dc2} = \frac{v_{dc}}{2} &- V_{r3} sin(3\omega t + \zeta_4) - V_{r6} sin(6\omega t + \zeta_5) \\ &- V_{r9} sin(9\omega t + \zeta_6) + ... \end{aligned} \tag{A.36}$$

where $\omega = d\varepsilon/dt$ and

$$V_{r3} = \frac{A_{r3}\ \widehat{m}\widehat{i}}{6\omega C} \tag{A.37}$$

$$V_{r6} = \frac{A_{r6}\ \widehat{m}\widehat{i}}{12\omega C} \tag{A.38}$$

$$V_{r9} = \frac{A_{r9}\ \widehat{m}\widehat{i}}{18\omega C} \tag{A.39}$$

Amongst these, the third-order voltage ripples dominate due to both the larger magnitude of the third-order harmonic component of the mid-point current and the lower frequency compared to the 6th and 9th components.

From (A.20), (A.22), and (A.37), the amplitude of the third-order harmonic voltage

ripples as a function of the inverter power factor, for the conventional sinusoidal PWM, lies in the range

$$0.0849\frac{\widehat{m}\widehat{i}}{\omega C} \leq V_{r3} \leq 0.1273\frac{\widehat{m}\widehat{i}}{\omega C} \tag{A.40}$$

whereas, for the conventional third-order harmonic injected PWM, from (A.20), (A.23), and (A.37), the range becomes

$$0.0303\frac{\widehat{m}\widehat{i}}{\omega C} \leq V_{r3} \leq 0.1182\frac{\widehat{m}\widehat{i}}{\omega C} \tag{A.41}$$

Finally, the range for the modified third-order harmonic injected PWM, from (A.20), (A.24), and (A.37), becomes

$$0 \leq V_{r3} \leq 0.1132\frac{\widehat{m}\widehat{i}}{\omega C}\ , \tag{A.42}$$

which, as expected, exhibits a zero lower bound. However, in practice, the partial DC-side voltages will contain third-order harmonic ripples even if the modified third-order harmonic injected PWM is utilized, due to unbalanced network conditions and other imperfections.

The employment of the third-order harmonic injected PWM techniques also affect the DC-to-AC voltage gain of the inverter. The maximum line-to-line rms voltage at the inverter AC-side terminals, if the inverter is not over-modulated, is $\frac{v_{dc}}{2}\frac{\sqrt{3}}{\sqrt{2}}$ for the conventional sinusoidal PWM. The value increases by 15.4% if the third-order harmonic injected PWM is employed. However, for the modified third-order harmonic injected PWM, the improvement of the voltage gain drops from 15.4% to about 11.6%.

A.3 Conclusion

A mathematical model was developed for the three-phase three-level NPC inverter, considering the possibility of a large DC component in the inverter mid-point current. Based on the model, the DC component and the amplitudes of major harmonic components of the mid-point current and partial DC-side voltages were calculated. The results showed that, at least for modeling purposes, the effect of the corrective DC offset of the PWM modulating signals is negligible on the DC and harmonic components of the mid-point current.

Appendix B

PV Module Parameters for Chapter 2

Table B.1 provides the numerical values of *the PV module* parameters.

Table B.1: Parameters of *the PV module*

Parameter of *the PV module*	Value	Comments
number of series PV cells per module	54	M_s
module nominal short-circuit current	8.21 A	$I_{sc,n}$
module nominal open-circuit voltage	32.9 V	$V_{oc,n}$
p-n junction ideality factor	1.3	a
temperature coefficient of $V_{oc,n}$	-0.1 V/K	$k_{V_{oc}}$
temperature coefficient of $I_{sc,n}$	0.003 A/K	$k_{I_{sc}}$
equivalent series resistor	0.231 Ω	R_s
equivalent parallel resistor	598.4 Ω	R_p
nominal p-n junction temperature	298 K	ϑ_n
nominal solar irradiation	1.0 kW/m^2	S_n

Appendix C

System Parameters for Chapter 3

The PV system parameters are introduced in Table C.1.

Table C.1: PV System Parameters

System Parameter	Value	Comments
switching frequency	4860 Hz	81×60 Hz
C_{dc}	5000 μF	
C	500 μF	
L	200 μH	
R	4.3 $m\Omega$	
L_f	100 μH	
R_f	3.8 $m\Omega$	
C_f	369 μF	*wye* connection
voltage ratio of Tr	4.16/0.32 kV	Y/Δ
k_1	0.2 Ω	
k_2	4.3 Ωs^{-1}	
k_3	0.5 Ω^{-1}	
k_4	0.5 $(\Omega s)^{-1}$	
k_5	3.5 Ω^{-1}	
k_6	777 $(\Omega s)^{-1}$	
τ_p	0.5 ms	Eq. (3.30)

Appendix D

System Parameters for Chapter 4

The PV system parameters and compensators are introduced in Tables D.1 and D.2, respectively.

Table D.1: PV System Parameters

System Parameter	Value	Comments
switching frequency	3420 Hz	57×60 Hz
C_{dc}	8000 μF	
C_b	1000 μF	
C	1000 μF	
L	100 μH	
R	3 $m\Omega$	
L_c	24 μH	
R_c	7.4 $m\Omega$	
L_f	100 μH	
R_f	3 $m\Omega$	
C_f	200 μF	Δ connection
voltage ratio of Tr	0.69/12.47 kV	Δ/Y
τ_i	0.2 ms	Eq. (4.1)

Table D.2: The Compensators Parameters

Compensator	k_p and k_i	Units	Saturation Limits
$K(s)$	4, 200	Ω^{-1} and $(\Omega s)^{-1}$	-2, 2
$K_v(s)$	5, 2777.7	Ω^{-1} and $(\Omega s)^{-1}$	-2, 2
$K_{pv}(s)$	1.6667, 909.1	Ω^{-1} and $(\Omega s)^{-1}$	-0.2, 0.5
$K_i(s)$	0.5, 15	Ω and Ωs^{-1}	-1, 1
$K_b(s)$	6.8182, 7043.74	Ω^{-1} and $(\Omega s)^{-1}$	-0.4, 0

Appendix E

System Parameters for Chapter 5

The parameters of the PV system under study including those of PV array, inverter, transformer, grid, and controllers are listed in Table E.1.

Table E.1: PV System Parameters

Parameter	Value	Remarks
PV array rating	1.0 MW	
maximum dc-link voltage	600 V	
C	5000 μF	
inverter rating	1.0 MVA	
switching frequency	3060 Hz	51×60 Hz
L_f	30 μH	
R_f	2 $m\Omega$	
C_f	$200\nabla + 750Y$ μF	
L_n	5 μH	
R_n	16 $m\Omega$	
transformer rating	1.0 MVA	
transformer voltage ratio	208 V/12.47 kV	Y/Y
transformer positive sequence leakage reactance	0.1 $p.u.$	
transformer copper losses	0.005 $p.u.$	
islanded local load	$0.32 + j0.17$ MVA	
fault impedance	0.2 mH	
$k_d(s) = k_q(s)$	$0.06 + 4/s$	Figure 5.4
$k_0(s)$	$0.009 + 10/s$	
$k_v(s)$	$1.667 + 370/s$	
i^r_{tq}	0	
i^r_{t0}	0	
LPF	$(0.02s + 1)^{-1}$	Figure 5.2
LPF	$(0.00005s + 1)^{-1}$	Figure 5.4
LPF	$(0.005s + 1)^{-1}$	Figure 5.7

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