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Single-Stage Power Electronic Converters with Combined Voltage Step-Up/Step-Down Capability

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A thesis submitted in partial fulfillment of the requirements for the degree in Doctor of Philosophy

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Abstract

Power electronic converters are typically either step-down converters that take an input voltage and produce an output voltage of low amplitude or step-up converters that take an input voltage and produce an output voltage of higher amplitude. There are, however, applications where a converter that can step-up voltage or step-down voltage can be very useful, such as in applications where a converter needs to operate under a wide range of input and output voltage conditions such as a grid-connected solar inverter. Such converters, however, are not as common as converters that can only step down or step up voltage because most applications require converters that need to only step down voltage or only step up voltage and such converters have better performance within a limited voltage range than do converters that are designed for very wide voltage ranges. Nonetheless, there are applications where converters with step-down and step-up capability can be used advantageously.

The main objectives of this thesis are to propose new power electronic converters that can step up voltage and step down voltage and to investigate their characteristics. This will be done for two specific converter types: AC/DC single-stage converters and DC-AC inverters. In this thesis, two new AC/DC single-stage converters and a new three-phase converter are proposed and their operation and steady-state characteristics are examined in detail. The feasibility of each new converter is confirmed with results obtained from an experimental prototype and the feasibility of a control method for the inverter is confirmed with simulation work using commercially available software such as MATLAB and PSIM.

Dedication

To my family:

my wife Farnaz and my daughter Niki

my deceased father

my mother

and my sibling

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I would like to express my deep gratitude to my supervisor Dr. Gerry Moschopoulos for his support, guidelines and encouragement. His personality, broad knowledge and thoughtfulness are infinite values for me. Without his deep knowledge in Power Electronics, I was not able to pursue my education towards Ph.D. degree.

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List of Acronyms

Acronyms.	**Full Format**
AC	Alternating Current
APWM	Asymmetrical Pulse Width Modulation
CCM	Continuous Conduction Mode
CSI	Current Source Inverter
DC	Direct Current
DCM	Discontinuous Conduction Mode
FACTS	Flexible AC Transmission System
GM	Gain Margin
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
PF	Power Factor
PFC	Power Factor Correction
PLL	Phase Locked Loop
PM	Phase Margin
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
RCD	Resistor Capacitor Diode
THD	Total Harmonic Distortion
UPS	Uninterruptable Power Supply
VSI	Voltage Source Inverter
ZVS	Zero Volt Switching

List of Principal Symbols

Symbol.	**Application**
V_G	Grid Voltage
V_t	Terminal Voltage of the Inverter
I_{ref}	Reference Current of the Inverter
P(t)	Instantaneous Active Power
Q(t)	Instantaneous Reactive Power
v_G^d	Grid Voltage on d-axis
v_G^q	Grid Voltage on q-axis
$\hat{v}_G$	Grid Voltage Peak Amplitude
i_d	Current on d-axis
i_q	Current on q-axis
ω	Angular Rotational Speed
θ	Phase Angel
P_{in}	Input Power
P_{out}	Output Power
v_C^{ref}	DC Capacitor Reference Voltage
w_G^d	DC Capacitor Reference Energy
I_{PV}	PV Current
v_{PV}	PV Voltage
I_{SC}	PV Short Circuit Current
V_{OC}	PV Open Circuit Voltage
V_{DC}	DC Capacitor Voltage
D	Duty Cycle
T_s	Time Period
L_m	Magnetizing Inductance
V_{stress}	Switch Off Cycle Voltage
V_{rev}	Diode Reverse Voltage
V_{in}	Input Voltage
f_{sw}	Switching Frequency

V_{DS}	Switch Drain-Source Voltage
PFC	Power Factor Correction
PLL	Phase Locked Loop
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
RCD	Resistor Capacitor Diode
THD	Total Harmonic Distortion
UPS	Uninterruptable Power Supply
VSI	Voltage Source Inverter
ZVS	Zero Volt Switching

Chapter 1

Introduction

1.1 Power Electronics Converters

Power electronic converters use power semiconductor devices and other passive elements to convert electrical energy from the form supplied by a source to the form required by a load. They are widely used for many industrial applications as they are the interfaces between sources and loads, given that it is rare for an electrical source to match the requirements of any particular load. The input source can be the AC mains, a battery, a fuel cell, a solar panel, an electrical generator, etc. while the load can be a motor, telecom equipment, consumer electronics, a computer, etc.

There are basically four types of power converters: DC/DC, AC/DC, AC/AC and DC/AC. For each of these converter types, active semiconductor elements and passive components can be arranged in multiple possible structures or topologies. Ideally, a power electronic converter should cost nothing, should take up no size or weight, and should have 100% conversion efficiency. Since such a converter does not exist, power electronic designers are forced to make choices when considering what topology to use for a particular application and are forced to consider various trade-offs. For example, a converter topology that can operate with high power conversion efficiency may be inappropriate for a particular application if it is expensive and cost is the most important factor.

Power electronic converters, regardless of what type they are (AC/DC, DC/DC, etc.), are typically either step-down converters that take an input voltage and produce an output voltage of low amplitude or step-up converters that take an input voltage and produce an output voltage of higher amplitude. There are, however, applications where a converter that can step-up voltage or step-down voltage can be very useful, such as in applications where a converter needs to operate under a wide range of input and output voltage conditions. Such converters, however, are not as common as converters that can only step down or step up voltage because most applications require converters that need to only step down voltage or only step up voltage and such converters have better performance within a limited voltage range than do converters that are designed for very wide voltage

ranges. Nonetheless, there are applications where converters with step-down and step-up capability can be used advantageously and such converters are the main focus of the proposed research.

The proposed research has been divided into two halves, each with two research components, as follows:

Part I. Step-Down/Step-Up Buck-Boost Topologies for AC/DC Converters

Component A: Low Power Single-Stage Converters (< 200 W)

Component B: Higher Power Single-Stage Converters (> 200 W)

Part II. DC-AC Step-Up/Step-Down Inverter

Component A: A New Step-Up/Step/Down Inverter Converter

Component B: A Control Strategy for the New Converter

In this thesis, a literature review of the two halves of the research is performed; the proposed research is explained in detail in the following chapters of the thesis. In this chapter a brief introduction of the proposed methods and circuits will be presented.

1.2 AC/DC Single-Stage Buck-Boost Converters with PFC

AC/DC converters can be used in many applications such as in personal computers, battery chargers, telecommunication power supplies, etc. They should provide good power quality for the AC side so that the input current and the input voltage are sinusoidal and they are in phase at the line frequency. To ensure that this happens, they should be implemented with some sort of power factor correction (PFC) to shape the input current. It should be noted that the input current does not have to be perfectly sinusoidal, just sufficiently sinusoidal so that it meets certain regulatory standards such as IEC 61000-3-2 [1].

Typical AC/DC power converters with transformer isolation are implemented with two converter stages: an AC/DC conversion (rectifying) stage and an isolated DC/DC conversion stage. A block diagram of a two-stage AC/DC converter is shown in Fig. 1. An AC/DC boost converter is used in the rectifying stage for most applications and it

performs input PFC. The input current can either be discontinuous or continuous. The DC/DC converter is used to regulate the output voltage and it can be a forward, a flyback or any other step down isolated dc-dc converter. In order to reduce the cost, size, and complexity of having two converters to perform AC/DC conversion, single-stage converters have been proposed. Single-stage AC/DC converters simultaneously perform both input PFC and DC/DC power conversion with just a single converter [2] – [4]. They can be synthesized by combining an AC/DC front-end converter with a DC/DC converter (typically a flyback or a forward converter for lower power application and a full-bridge converter for higher power one) then removing all redundant elements. A single-stage converter usually has only one controller, which is used to regulate the output voltage. Unlike a two-stage converter, there is no controller to regulate the input voltage of the DC/DC section. A diagram of a single-stage converter is shown in Fig. 1.2.

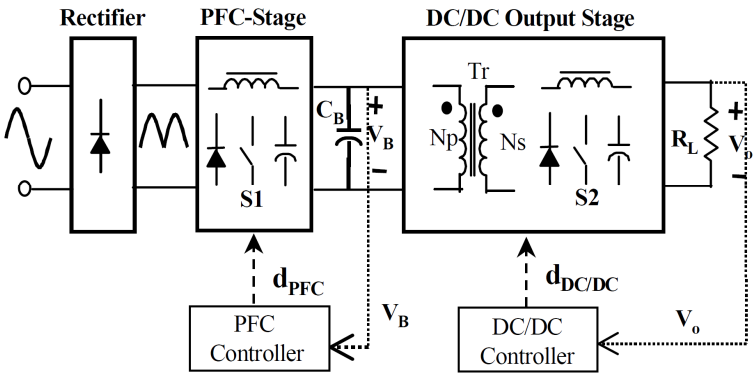


Fig. 1.1 Two-stage converter [5]

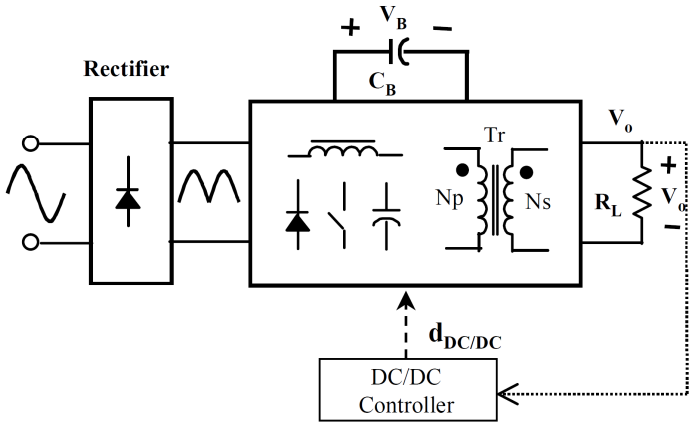


Fig. 1.2 Single-stage converter [5]

1.3 Low Power Single-Stage Converters (< 200 W)

A low power single-stage converter has either a flyback converter or a forward converter in its DC section. An example of such a converter is shown in Fig. 1.3. It can be seen that this converter combines an AC/DC boost (step-up) converter input section with a DC/DC flyback converter output section. The way this converter works is as follows: When the MOSFET switch is turned on, voltage is impressed across the input inductor, L_{in}, and the current through it rises. At the same time, DC bus capacitor voltage is impressed across the transformer and energy is placed in it as the output diode is reverse-biased. When the switch is turned off, current is transferred from the input inductor to the DC bus capacitor and the energy that was previously stored in the transformer is transferred to the output as the output diode is forward-biased. The switch is turned on at the start of the next switching cycle and the above actions are repeated. This is done throughout the AC line cycle. The following should be noted:

- The input current is discontinuous and consists of triangular peaks, as shown in Fig. 1.4. It can be seen that these peaks are bounded by a sinusoidal envelope so that the waveform is essentially sinusoidal, which results in a very good input power factor.
- Whatever energy is placed into the transformer during a switching cycle is transferred to the output by the end of the cycle. It is standard practice to design the transformer so that it is always fully demagnetized by the end of the switching cycle and contains no stored energy.

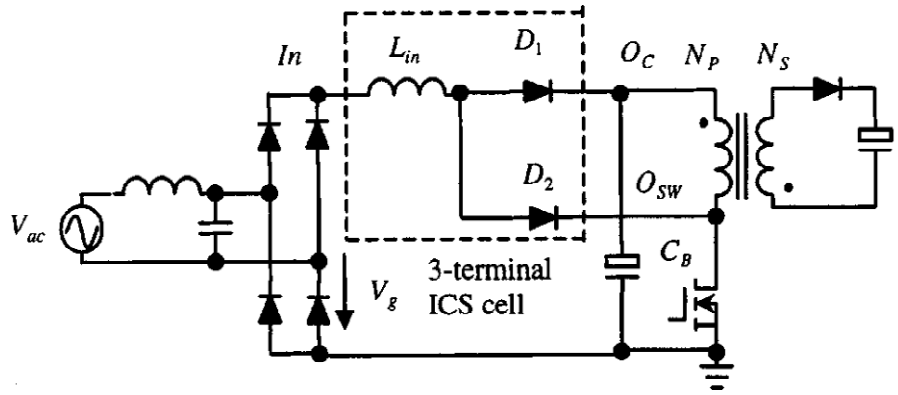


Fig. 1.3 Boost type lower power PFC [6]

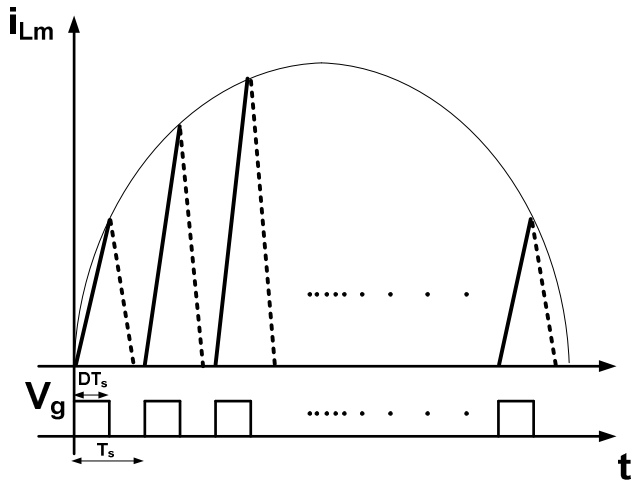


Fig. 1.4 Current in the input inductor

Most of the problems associated with single-stage converters such as the one shown in Fig. 1.3 are due to the wide ranging variation of the DC bus voltage. The DC bus voltage of a single-stage converter (the voltage across the capacitor at the input of the DC/DC flyback or forward section) is dependent on the input voltage and output load conditions as there is no controller that can regulate it. The input voltage can vary from $85V_{rms}$ to $265V_{rms}$ if the converter is designed to operate for the standard universal input voltage, and the load can vary from no-load to 100% full-load so that the DC bus voltage can vary considerably, even becoming excessive (> 800Vdc). Excessive DC bus voltages result in the need for higher voltage rated and bulkier DC bus capacitors, which increases size and cost, and higher rated semiconductor devices and transformers, which also increases cost as well.

Researchers have proposed the following techniques to try to limit the variation of the DC bus voltage and to ensure that it does not exceed 450 V_{dc}, which is a commonly accepted voltage limit:

- Bulk capacitor voltage feedback techniques [7]-[8] that use one or more auxiliary windings from the main power transformer to produce a counter voltage that limits the amount of voltage that is placed across the input inductor. Doing so reduces the charging current in the input inductor when the load is decreasing. Although this method is the easiest to implement, its main drawback is that it leads to the distortion

of the input current as it creates gaps in the current waveform as shown in Fig. 1.5 as there is no input current flow when the input voltage is low.

- Load current feedback techniques [9]-[10] that adjust the input current by using information that is sensed at the load. In this technique efficiency is low and the input current is much distorted.
- Direct power transfer techniques [10]-[18] that allow some of the power from the converter's input section to be transferred directly to the output instead of the DC bus capacitor, to reduce the amount of charge placed in this capacitor. Although these techniques do result in DC bus voltage reduction, this reduction may be insufficient to justify their cost.

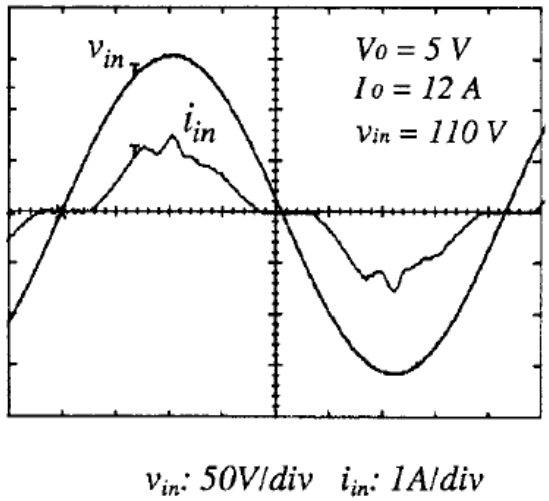


Fig. 1.5 Input current feedback technique

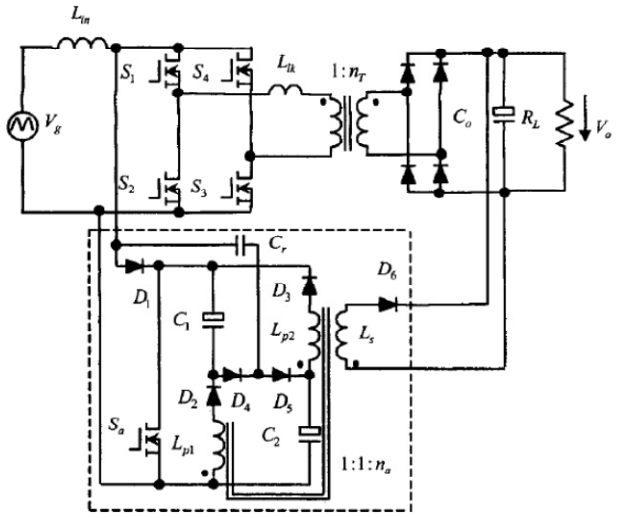
- Variable switching frequency techniques [19]-[20] that limit the amount of input power that is transferred to the DC bus capacitor by increasing the switching frequency at decreasing load and vice versa. Operating a converter with variable switching frequency, however, increases the size of the converter as it must be designed to operate at the lowest switching frequency and it complicates the design of the converter magnetics as they must be designed to operate over a wide range of switching frequencies instead of just one fixed frequency.

1.4 Higher Power Single-Stage Converters (> 200 W)

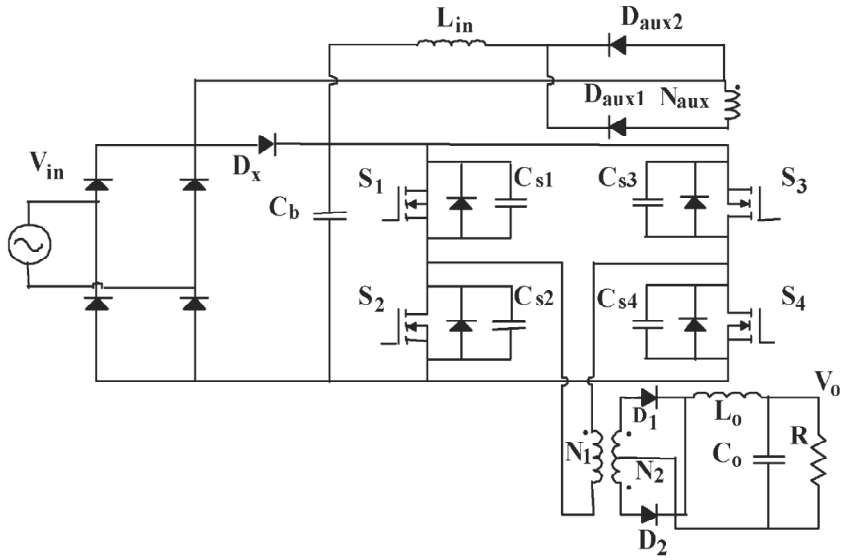
For the second component of the proposed research, an investigation was made to extend the research performed on low power single-stage AC/DC converters to higher power AC/DC converters (> 200W) [21]-[24]. In the previous section, it was stated that the main problem with single-stage converters is that the intermediate DC bus voltage (the voltage at the input of the DC/DC section) is unregulated and thus may become excessive under certain line and load conditions. It was also stated that this problem may be corrected using various methods, but these methods are flawed in some way.

Trying to design a higher power single-stage AC/DC converter is more challenging that trying to design a lower power single-stage AC/DC converter because higher power converters operate with a wider load range. The drawbacks that are associated with lower power converters become worse for higher power applications, given this wider load range of operation. Fig. 1.6 shows several higher power single-stage AC/DC converters, with the DC/DC section being a four-switch full-bridge converter instead of a single switch forward or flyback converter. These circuits have the following drawbacks:

- In [25] (Fig. 1.6(a)) and [26], researchers proposed a clamping technique for an AC/DC buck-boost converter that placed a flyback transformer in series with the full bridge section, but it could not operate with universal input voltage (85 $V_{rms} < V_{in} <$ 265 V_{rms}).
- In [21] and [27], the authors tried to limit the intermediate DC bus voltage to an acceptable range by using fairly large boost inductor components, but this made the converter bulky and created distortion in the zero-crossing regions of the AC input current.
- The most popular technique for higher power single-stage power conversion is to use auxiliary windings taken from the main power transformer [28] (Fig. 1.6(b)). This winding cancels out the DC bus voltage that is in front of the input boost inductor. The converter can be designed so that the DC bus voltage does not become excessive, but the input current is considerably distorted and a non-standard transformer with a non-standard design must be used to accommodate the extra windings.



a) Boost full-bridge and the aux. circuit [25]



b) Modified boost full-bridge [28]

Fig. 1.6 Higher power single-stage AC/DC converters

All the higher power converters described above are implemented with boost converter input sections. If the front-end boost converter section is replaced with a buck-boost (step-up/step-down) converter, then the DC bus voltage is less likely to become excessive. Few such converters have been proposed, however, and their advantages and disadvantages relative to boost-based single-stage topologies are not

well-known. The following buck-boost converters with full-bridge DC/DC sections have been proposed:

- In [29], a new buck-boost type single-stage converter was introduced. The converter combined two parallel buck-boost input sections with a resonant full-bridge DC/DC converter. The main disadvantages of this converter were that the converter was limited to low line and low power applications and the resonant inductor was large, in the range of mHs.
- Recently, researchers in [30]-[31] combined a buck-boost PFC section with a DC/DC full bridge converter to implement ballast equipped with power factor correction. In [32]-[33], the buck-boost PFC section was followed by a half-bridge resonant converter. All these converters, however, had difficulties producing a good input power factor except for light load conditions.

1.5 DC/AC Step-Up/Step-Down Inverter and Control

DC/AC inverters convert a DC input voltage into a single-phase or a three-phase AC output voltage. They are widely used in many industrial applications such as in motor drives, as part of solar and wind energy systems to transfer energy to the grid, in uninterruptible power supplies (UPS) for backup energy systems, in electrical appliances, etc. Inverters should be able to produce AC output voltages that are as close to ideal sinusoids as possible, to avoid injecting unwanted harmonics to the grid or load.

Inverters are generally either voltage-source inverters (VSIs) or current-source inverters (CSIs). VSIs can be considered to be step-down converters as the amplitude of the AC output voltage(s) can be less than that of the DC input. CSIs can be considered to be step-up converters as the amplitude of the AC output voltage(s) can be greater than that of the DC input. There are applications, however, where it is advantageous to have an inverter that can step up and step down voltage. This is especially true for solar and wind energy systems, where converters need to be able to operate under a very wide range of operating conditions in order to be able to maximize the amount of generated energy that can be transferred to the load or grid.

1.5.1 Step-Up/Step-Down Inverter Topologies

It is possible to implement a DC/AC inverter that can step up and step down voltage if a two-stage approach like the one shown in Fig. 1.7 is used. It can be seen that the converter in Fig. 1.7 has two converter stages – a DC/DC boost converter that can step up voltages and a single-phase VSI converter that can step-down voltages. If it is desired for this two-stage DC/AC converter to operate with maximum voltage gain (ratio of output to input voltage), all that must be done is to have the front-end boost converter operate with maximum step-up voltage gain and the inverter to operate with its maximum gain and not step down voltage. Conversely, if it is desired for the two-stage DC/AC converter to operate with minimal voltage gain (ratio of output to input voltage), all that must be done is to have the front-end boost converter operate with minimal step-up voltage gain (which can be achieved by not turning on the switch) and the inverter operating to step down voltage.

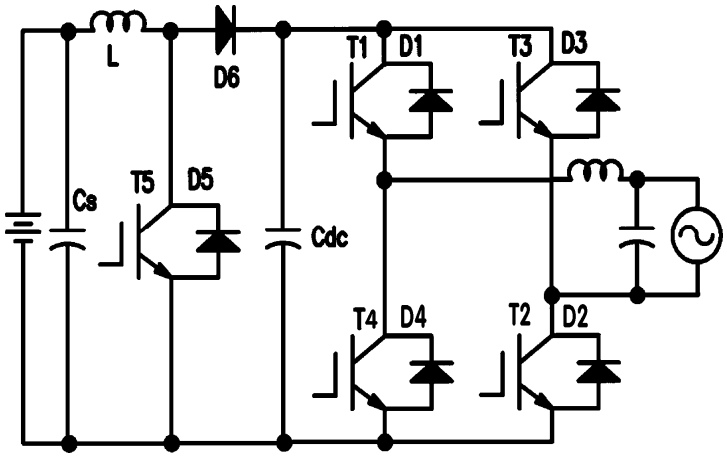


Fig. 1.7 Two-stage DC/AC converter

There are several disadvantages with the two-stage approach. The most notable ones are (i) cost, as two separate and independent converters are needed; (ii) component stress, as the front-end boost switch and front-end diode must conduct considerable current. As a result, DC/AC converters that can step up voltage and step down voltage using only a single stage have been proposed. Only a few such converters have been proposed, however, due to the topological constraints.

In [34], a single phase multi-level inverter has been proposed. The output voltage is the summation of two level separated inverters. At the same time, inverter is capable of boosting and energy transfer to output. It is not clear if the topology can be implemented as a 3-phase inverter. In [35], a very simple buck-boost inverter has been introduced. The concept is expandable to 3-phase system, however, the voltage zero crossing of the output waveform is distorted. In [36] and [37], single phase, single-stage grid connected buck-boost inverters were introduced. It is not clear whether or not the concepts are applicable for 3-phase networks. Moreover, the component count of the

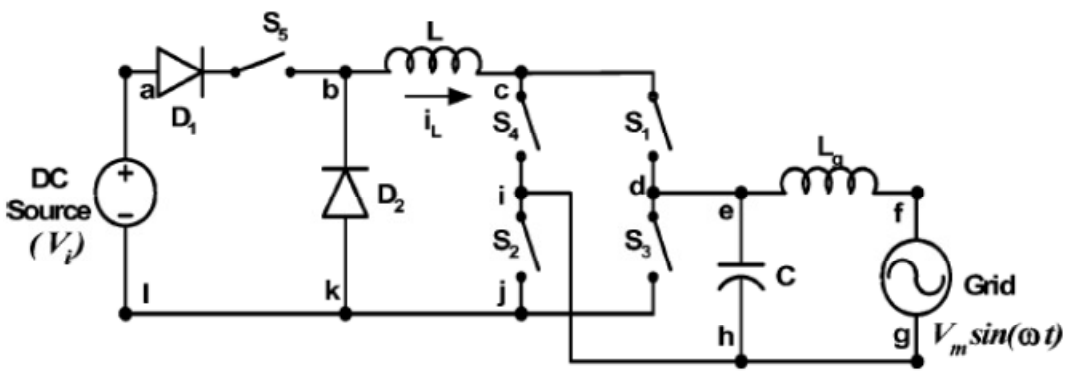


Fig. 1.8 Proposed circuit in [36]

both circuits are a major issue. Fig. 1.8 shows the circuit proposed in [36] as an example.

The most popular single-stage inverters with voltage step-up/step-down capability are so-called Z-source inverters [38]-[42]; a basic Z-source inverter is shown in Fig. 1.9. This converter has a passive element network consisting of inductors and capacitors attached between the input DC source and a six-switch inverter. This passive network, called a Z-source network, allows the six-switch inverter to short-circuit the DC bus (between the passive Z-source network and the input to the six-switch inverter) as there is no short-circuit across the Z-source network capacitors. The converter can step up voltage or step down voltage depending on whether the six-switch inverter operates with short-circuit states that allow the DC bus to be shorted. If the six-switch inverter does not have any short-circuit states, then it operates as a step-down converter; if it does, then it operates as a step-up converter.

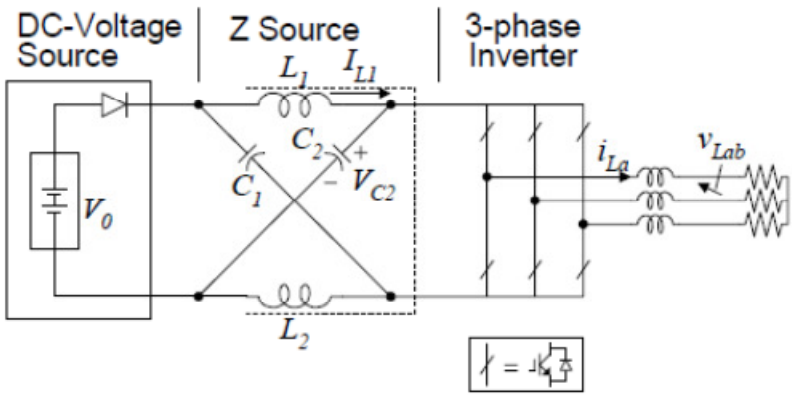


Fig. 1.9 Z-source inverter [38]

With respect to the control strategies of previously proposed converters with voltage step-down/step-up capability, these strategies tend to be topology-specific as, for example, the control of a z-source converter is different than that of a two-stage boost/VSI structure. These control strategies are generally discussed along with the topologies in the literature. If such inverters are used in solar energy systems to inject power into the grid, then the control strategy should allow an inverter to inject sinusoidal current to the grid, the DC bus voltage to a fixed desired voltage, and allow maximum power point tracking (MPPT) techniques to be used to extract the maximum available energy from solar panels.

1.6 Thesis Objective and Outline

The main objectives of this thesis are to propose new power electronic converters that can step up voltage and step down voltage, to investigate their characteristics, and to confirm their feasibility with experimental work obtained from prototype converters. This will be done for two specific applications: AC/DC single-stage power conversion and inverters, which perform DC/AC power conversion. Such voltage step-up/step-down converters have an advantage over more conventional converters that can only perform one of these functions as they can operate over a wider range of operating conditions.

The outline of this thesis is as follows:

In Chapter 2, a new single-phase AC/DC single-stage converter will be introduced. This converter is based on the conventional buck-boost converter, which has voltage step-up/step-down capability, and it will be examined whether this allows the converter's intermediate DC bus voltage to have significantly less variation than what is typically for most previously proposed single-stage converters, which have boost input sections. In this chapter, the new converter will be presented, and its basic operation and its modes of operation will be described. The converter's steady-state characteristics will be determined by mathematical analysis and the results of the analysis will be used to develop a procedure for the selection of key parameter values. The feasibility of this converter will be confirmed with results obtained from an experimental prototype.

In Chapter 3, the concepts discussed in Chapter 2 that are related to the use of buck-boost converter properties in AC/DC single-stage converters will be extended to a full-bridge converter designed for higher power levels. As a result, a new AC/DC single-stage buck –boost full-bridge converter will be proposed in the chapter. In the chapter, the operation of the converter will be explained, its characteristic curves will generated by a computer program and its components will be designed according to the results of the characteristics curves. An experimental prototype will be built to confirm the feasibility of the proposed converter and to confirm whether buck-boost converter principles can be used in higher power single-stage converters.

In Chapter 4, a new technique that can be used to extend the operating range of a three-phase inverter will be proposed. Since the proposed inverter is based on established principles that are related to well-known active-clamp converters, basic principles associated with such converters will be reviewed and it will be shown how an active clamp can be used to convert a conventional six-switch inverter into a voltage step-down/step-up converter. The operation of the inverter with the proposed active clamp technique will be confirmed with results obtained from a simple proof-of-concept prototype converter.

In Chapter 5, the control of the inverter proposed in Chapter 4 will be investigated. In this chapter, an appropriate control method for the inverter will be developed and the dynamics of a PV inverter system will be investigated for two distinct cases using a

model that will be developed in the chapter. In both cases, it will be determined whether sinusoidal output currents can be produced and whether the input current can be made to have little ripple so that maximum power point tracking techniques (MPPT) can be implemented.

In Chapter 6, the contents of the previous chapters will be summarized, conclusions will be stated, the main contributions of the thesis will be listed and topics for future work will be given.

Chapter 2

A Low Power AC/DC Single-Stage Converter with Reduced DC Bus Voltage Variation

A new low power single-stage AC/DC converter is proposed in the chapter. The outstanding features of the converter is that it can operate with a sinusoidal input current and a low primary-side DC bus voltage that is much less variable than that found in other single-stage converters. The operation of the converter is discussed in the chapter and its various modes of operation are explained in detail. An analysis of the converter's steady-state characteristics is performed and the results are used in the design of the converter. Experimental results obtained from a prototype converter are also presented.

2.1 Introduction

Single-stage AC/DC converters simultaneously perform both input power factor correction (PFC) and DC/DC power conversion with just a single converter [2]-[8]. They can be synthesized by combining an AC/DC front-end converter (typically a boost converter) with a DC/DC converter (typically a flyback or a forward converter) then removing all redundant elements. A single-stage converter usually has only one controller, which is used to regulate the output voltage. This means that the intermediate DC bus voltage – the DC voltage at the transformer primary side that needs to be stepped down - is therefore dependent on the input line and output load conditions and can thus vary considerably.

When a single-stage converter is synthesized from an AC/DC boost converter, as is the case with most single-stage converters, the intermediate DC bus voltage has the potential to become very high as it does not have a separate and independent front-end converter to regulate it. This is especially true when the converter is operating under light load conditions as the intermediate DC bus capacitor used to smooth out the voltage has less opportunity to discharge. Power electronics researchers have proposed many techniques to try to keep the bus voltage to a maximum level of less than 450 V to avoid large switch voltage stresses and capacitor size.

None of these techniques, however, significantly limits the variation in the DC bus voltage that can occur when the converter needs to operate under universal input line conditions. This can affect the design of the main power transformer as it must be designed to operate for all potential operating conditions. It can also affect the design of the converter with respect to hold-up time if this needs to be considered. A widely varying DC bus voltage means that the converter must have appropriate hold-up time when the DC bus voltage is low or high, which, in turn, means that the DC bus capacitors must be selected for several bus voltages instead of just one.

A new AC/DC single-stage converter is proposed in the chapter. The outstanding feature of this converter is that its DC bus voltage is far less dependent on its operating conditions than is the case for most previously proposed single-stage converters. The significant reduction in DC bus voltage variation allows for a reduction in DC bus capacitor size as the need to satisfy hold-up time requirements for both low and high DC bus voltage is done away with. In the chapter, the operation of the converter is discussed and its modes of operation are explained and analyzed. The analysis is used to develop a design procedure for the converter that is demonstrated with an example. The feasibility of the converter is confirmed with results obtained from an experimental prototype.

2.2 Converter Operation

The proposed single stage converter is shown in Fig. 2.1. It consists of a diode bridge rectifier, transformers T_1 and T_2, switch S, DC bus capacitor C, output capacitor C_o, and diodes D_1 to D_4. T_1 and T_2 have turns ratio of n_1 and n_2 respectively, and each contain a magnetizing inductance, L_{m1} and L_{m2}. Each magnetizing inductance can be considered to be parallel to ideal transformer; the leakage inductances of T_1 and T_2 are negligible.

The input current is discontinuous and is bounded by a sinusoidal envelope so that it is essentially a sinusoidal waveform with high frequency harmonic components. The magnetizing current of each transformer can be either discontinuous or continuous. For the purpose of simplicity, it will be assumed that these currents are discontinuous so that both transformers are fully demagnetized after the switch is turned off. Moreover making

the magnetizing current of T_2 discontinuous will make V_C less susceptible to load variation. The proposed converter has two distinct modes of operation, depending on the DC bus voltage, V_C. In one mode, transformer T_1 acts like an inductor while T_2 acts like a flyback transformer; in the other, both transformers act like flyback transformers. Both modes are described in this section.

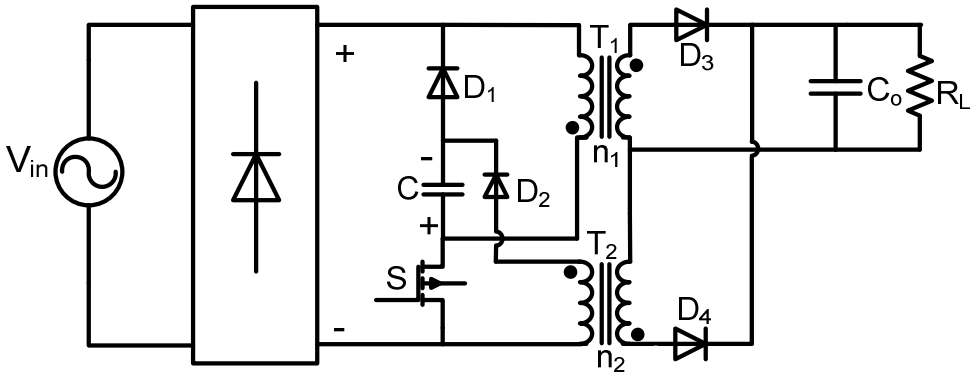


Fig. 2.1 The proposed converter

2.2.1 Mode 1 Single Flyback Transformer Mode of Operation

The converter is in this mode of operation when the DC bus capacitor voltage is less than n_1V_o. This means that diode D_3 never conducts and T_1 becomes like an input inductor as no energy is transferred to the output. T_2 is the only transformer in the converter that actually operates as a flyback transformer.

The converter goes through the following intervals when operating in the single flyback transformer mode of operation, with typical converter waveforms and equivalent circuit diagrams shown in Figs. 2.2 and 2.3 respectively:

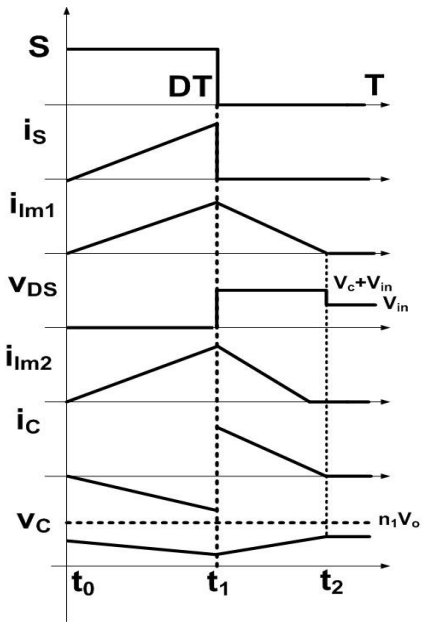


Fig. 2.2 Typical waveforms describing single flyback transformer mode when $n_1V_o < V_C$

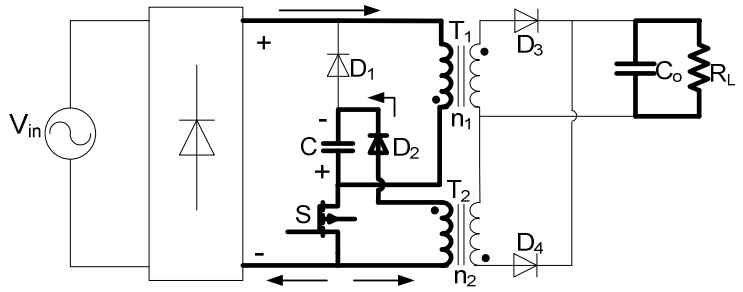


Fig. 2.3(a)

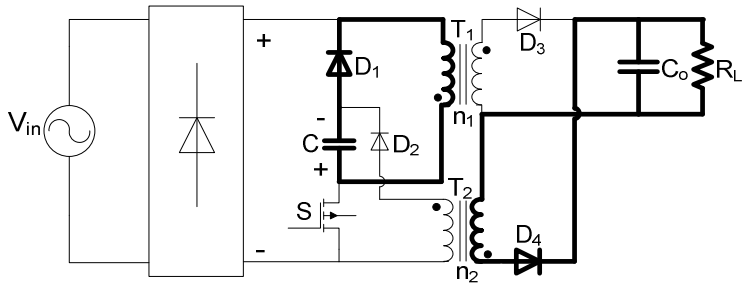


Fig. 2.3(b)

Fig. 2.3 Equivalent circuits

Interval 1 [t_0 ~ t_1](Fig. 2.3(a)): Switch S is turned on at t_0. The rectified input line voltage, $|V_{in}|$, is applied to the magnetizing inductance of T_1, L_{m1}. Current in L_{m1}, i_{Lm1}, begins to flow and increases linearly. Also during this interval, DC bus voltage V_C is applied across the magnetizing inductance of T_2, L_{m2}, causing its current, i_{Lm2}, to increase linearly through D_2. During this interval, there is no power transfer to the load, which is being supplied by C_o.

Interval 2 [t_1 ~ t_2](Fig. 2.3(b)): Switch S is turned off at t_1. All the energy that was placed in T_1 during Interval 1 is transferred to bus capacitor C during this interval. Also during this time, all the energy that was placed in T_2 during Interval 1 is transferred to the output through D_4. At some instant $t = t_2$, both T_1 and T_2 have been fully demagnetized and remain so, until the start of the next switching cycle.

2.2.2 Mode 2 - Dual Flyback Transformer Mode of Operation

The converter is in this mode of operation when the DC bus capacitor voltage is $V_C = n_1V_o$. Ideally, V_C can never exceed n_1V_o because diode D_3 conducts if it tries to do so, allowing energy that would otherwise charge C to be transferred to the output. During this mode, both T_1 and T_2 act like flyback transformers that demagnetize through their secondaries when switch S is off. It should be mentioned that a part of stored energy in the magnetizing inductance of T_1 goes to the DC bus capacitor after S has been turned off to make up for the drop in V_C that would otherwise occur due to the transfer of energy from C to T_2.

The converter goes through the following intervals when operating in the dual flyback transformer mode of operation, with typical converter waveforms and equivalent circuit diagrams shown in Figs. 2.4 and 2.5 respectively:

Interval 1 [t_0 ~ t_1](Fig. 2.5(a)): The converter operates in the same way as it does for Mode 1-Interval 1.

Interval 2 [t_1 ~ t_2](Fig. 2.5(b)): Switch S turns off at t_1. The converter operates in the same way as it does for Mode 1-Interval 2 as energy stored in T_1 is transferred to C to

make up for the drop in V_C after the previous interval. The DC bus voltage reaches n_1V_o at $t = t_2$. T_2 has not been fully demagnetized at this time.

Interval 3 [t_2 ~ t_3](Fig. 2.5(c)): At $t = t_2$, V_C is equal to n_1V_o and D_3 begins to conduct as it becomes forward biased. This releases the remaining energy stored in T_1 to the output. Also during this time interval, all the energy that was placed in T_2 during Interval 1 is transferred to the output through D_4. At some instant $t = t_3$, both T_1 and T_2 have been fully demagnetized and remain so, until the start of the next switching cycle.

In addition to the modes of operation, the following should also be mentioned about the operation of the proposed converter:

(i) Regardless of the mode of operation, the maximum voltage that is placed across S is placed while T_2 is demagnetizing and is

$$V_{s,max} = V_C + V_{in} \tag{2.1}$$

The voltage across S becomes V_{in} after T_1 has been demagnetized.

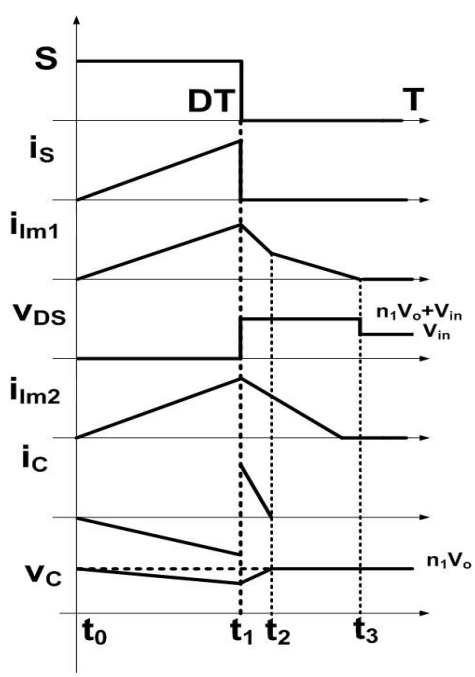
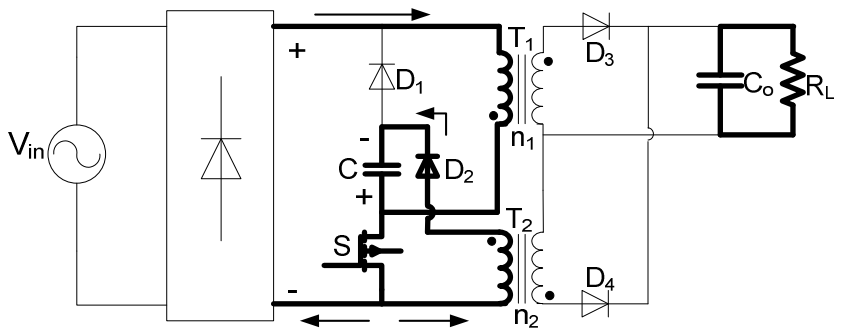
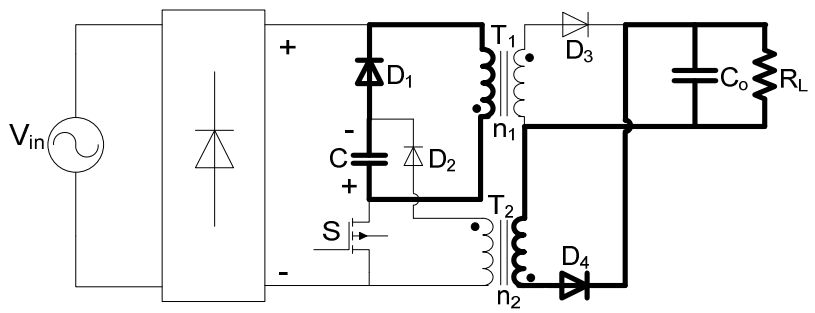


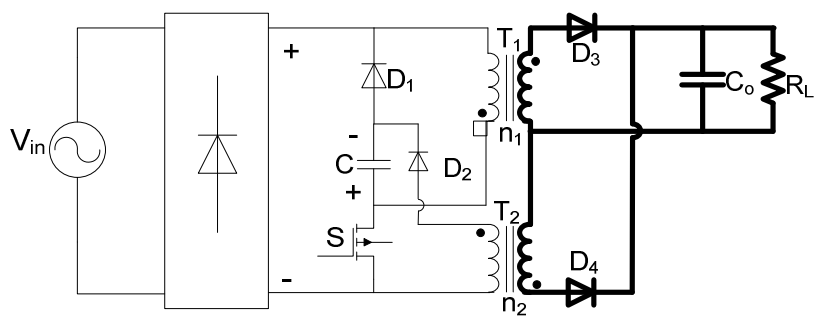
Fig. 2.4 Circuit waveforms when $n_1V_o = V_C$



(a)



(b)



(c)

Fig. 2.5 Equivalent circuits

(ii) In practice, when V_C touches n_1V_o, the converter is most likely to be in Mode 2 when the rectified input voltage $|V_{in}|$ is close its peak value as the energy stored in T_1 is

more than that transferred to T_2. During zero crossing of line cycle, the converter is most likely in Mode 1. Since the absorbed energy by L_{m1} in this area is less than injected energy from DC bus capacitor to the second transformer.

(iii) There are two mechanisms that help make the DC bus voltage in the proposed converter less variable than that of previously proposed single-stage AC/DC converters. One is the substitution of the input inductor with a flyback transformer, which acts to clamp the DC bus voltage. The second is that the input section is not based on the boost converter, but is instead based on a buck-boost converter operating with $D \leq 0.5$ like a buck converter. The combination of the two mechanisms reduces potential voltage variation better than just one mechanism by itself.

(iv) In a "real" converter prototype, voltage V_C may exceed n_1V_o slightly due to non-idealities in the transformer and the clamping diode D_3 such as leakage and winding inductance and diode forward voltage drop.

2.3 Steady-State Analysis and Design

The key parameters that affect the operation of the proposed converter are the magnetizing inductances of T_1 and T_2, L_{m1} and L_{m2}, and the turns ratio of T_1 and T_2, n_1 and n_2. A design procedure is needed to determine appropriate values for these parameters. This can be done by analyzing the converter's steady-state characteristics and reviewing a number of parameter combinations. The following assumptions can be been made to simplify the analysis:

- All components are lossless.
- The duty ratio of the converter remains constant during line cycle.
- The switching frequency is much higher than the input line frequency.
- C is large enough to assume that V_C is constant. There is no ripple over V_C or output voltage.
- T_1 has been substituted with an inductor. Based on technical needs n_1 will be fixed.

It should also be noted that the leakage inductances of T_1 and T_2 are neglected in the analysis. When the switch is turned off, leakage inductance energy from T_1 goes into C and leakage inductance energy from T_2 is dissipated by some snubber (typically a simple dissipative RCD snubber) that should be placed across T_2 to keep overvoltage spikes from appearing across the switch. Since the leakage inductance energy from T_2 comes from C, there is a situation where more energy is transferred to C than what would be under ideal circumstances with T_1 not having leakage inductance, but also more energy is transferred out of C than what would be under ideal circumstances with T_2 not having leakage inductance. In other words, there is additional energy coming into C, but there is also additional energy coming out of C as well so that the net effect on V_C is not as large as one might think. Since this is the case and since including leakage inductance in the analysis would make it very complicated with little benefit, leakage inductance has been neglected in the analysis.

A procedure for the selection of the converter's key component values (L_{m1}, L_{m2}, n_1 and n_2) is presented in this section and is demonstrated with an example. For the example, the converter will be designed for

Input voltage: $V_{in} = 85\text{-}265V_{rms}$

Output Voltage: $V_o = 48V_{DC}$

Maximum Output Power: $P_o = 100W$

Switching Frequency: $f_{sw} = 100kHz$

The converter will be designed so that (a) it operates with a fully discontinuous input current so that it is bounded by a sinusoidal envelope and contributes to an excellent input power factor, (b) the converter's maximum duty cycle does not exceed D = 0.5, and (c) there is no direct energy transfer from the primary of T_1 to the output when the input voltage is at its minimum value of V_{in} = 85 Vrms. Condition (c) helps to set the voltage across C at which n_1V_o should be set to clamp so that the variation of this voltage due to varying line and load conditions is minimized. Once this voltage has been established,

then the ratio of energy that is transferred to the output through one transformer relative to that through the other can be considered.

The design procedure can be summarized as follows:

(i) The procedure begins by considering the operation of the converter with transformer T_1 acting as an inductor L_{m1}, with no direct energy transfer taking place. This will help select a value for L_{m1}.

(ii) Next, values of L_{m2} and n_2 will be selected based on the value of L_{m1} that was previously selected.

(iii) Then, the operation of the converter implemented with T_1 having a magnetizing inductance of $L_1 = L_{m1}$ will be considered. A value of n_1 will be selected based on peak switch voltage stress.

(iv) Finally, a check of the converter's operation with the selected values of L_{m1}, L_{m2}, n_1, n_2 will be made based on the distribution of energy transferred to the load among transformers T_1 and T_2.

2.3.1 Selection of Magnetizing Inductance L_{m1}

The value of L_{m1} needs to be sufficiently low so that the magnetizing current of T_1 does not become continuous and the converter operates in input DCM. If the maximum allowable duty cycle is D = 0.5 and if it is possible for the converter to operate past the boundary between input DCM and input CCM, it is most likely to do so when D is at its maximum value of 0.5 and V_{in} is the minimum input line voltage [12]. Assuming that the input section is in DCM, then the following expression for L_{m1}, which is based on (2.2), must be satisfied [43]:

$$L_{m1} \leq \frac{D^2 V_{in}^2}{2 P_o f_{sw}} \tag{2.2}$$

The reader is referred to Appendix I for a detailed derivation of this relation. Substituting the appropriate parameter values into (2) gives

$$L_{m1} \leq \frac{0.5^2 \times (85Vrms)^2}{2 \times 100W \times 100kHz} = 90\mu H \tag{2.3}$$

Since the maximum output power of the converter is 100W, the value of L_{m1} cannot exceed 90 μH. The value of L_{m1}, however, should not be much lower than this in order to minimize the peak current in the input section of the converter and the peak current flowing through the switch. Moreover, if L_{m1} is lower than this value, then the duty cycle will also become lower and may, in fact, become too narrow when the input voltage is at its maximum rms value, which is not desirable. Therefore the value of L_{m1} has been set at L_{m1} = 90μH for this example.

2.3.2 Selection of L_{m2} and n_2

With the value of L_{m1} selected in the previous section, the next step is to select appropriate values of L_{m2} and n_2. For this step, the assumption that T_1 acts like an inductor and there is no direct transfer of energy from the input section of the converter to the output will continue to hold. The main criterion that will be used to select L_{m2} and n_2 is whether the level of the bus capacitor voltage V_C is high enough to completely demagnetize L_{m1} during the (1-D)T time in each switching cycle when the switch is off. This criterion must be satisfied so that the input current will be fully discontinuous. There is, however, no closed form equation or solution that can be used to determine whether this criterion is satisfied.

Since the magnetizing current of T_1 (input section transformer) and of T_2 (output section transformer) can be either fully discontinuous or "semi-continuous" as shown in Fig. 2.6, there are four possible current operating modes that need to be considered when trying to analyze the steady-state characteristics of the converter with a particular set of parameter values for a particular set of line and load conditions. These can be referred to as input discontinuous conduction mode (DCM), input semi-continuous conduction mode (CCM), output DCM, and output CCM, based on the magnetizing currents of the “input” transformer T_1 and the “output” transformer T_2.

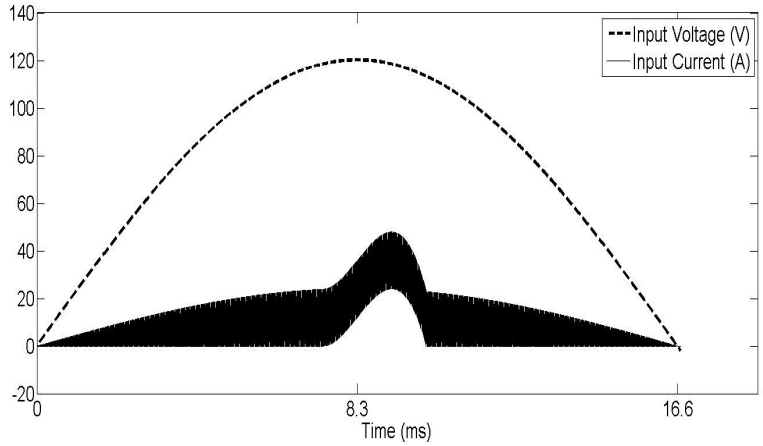


Fig. 2.6 Semi-continuous input current waveform

It is a fact that it is possible for the converter to operate in one of these four combinations of "input" / "output" modes makes it difficult to establish closed-form equations that can be used in an analysis, as it is not possible to determine in which of the four current modes the converter is operating in just by looking at the converter's line and load conditions and component values. As a result, some sort of computer program is needed to analyze the converter's steady-state characteristics.

Such a program can be developed based on the energy equilibrium that must exist at the DC bus capacitor when there is no energy that is directly transferred from the input to the output. The energy stored in the DC bus capacitor during a half input line cycle (rectified line cycle) must be the same as that removed from the capacitor during the same time, so that there is no net charge placed in the capacitor. This equilibrium can also be stated in terms of current – the average current that flows into the DC bus capacitor during a half line cycle must be the same as that which flows out during the same time so that there is no net average or DC current flowing in the capacitor. Once such equilibrium has been established for a set of operating conditions, only then does it become possible to analyze the converter's operation for this set of conditions.

If the input section is in CCM, then the energy transferred to the DC bus capacitor from the input is

$$W_{in-CCM} = \sum_{m=1}^{n} \int_{0}^{T_s} I_{avg} V_C dt \tag{2.4}$$

where V_C is the voltage of DC bus capacitor, C, T_s is the switching period, n is the number of switching cycles per line period, and I_{avg}, the average current absorbed by the capacitor during a switching cycle, is

$$I_{avg} = (I_1 + I_2)(1 - D)/2 \tag{2.5}$$

I_1 and I_2 are the minimum and maximum of the current during one switching cycle. Fig. 2.7 shows a typical waveform of i_{lm1} in CCM mode.

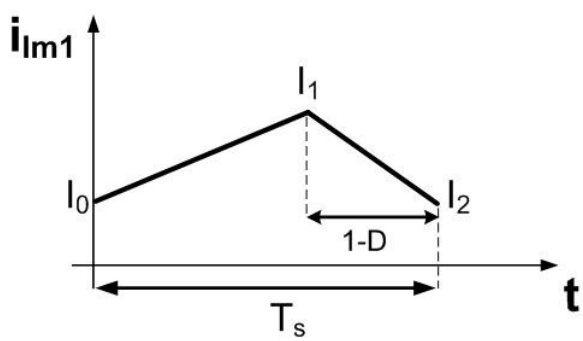


Fig. 2.7 Typical continuous current waveform

If the magnetizing current of T_1, i_{Lm1}, is fully discontinuous and the converter is operating with input DCM, then the energy transferred to the DC capacitor, C, from the input during a line cycle can be expressed in terms of an equation. This equation is

$$W_{in-DCM} = \int_{0}^{T_L} \frac{D^2 V_m^2}{4 L_{m1} f_s} dt \tag{2.6}$$

where V_m is the peak value of the input voltage, D is the duty ratio of the switch, L_{m1} is the magnetizing inductance of T_1, f_s is switching frequency and T_L is the line period. Equ. (2.6) is derived in the Appendix I.

When the output section is in CCM mode, the energy transferred out of C is

$$W_{out-CCM} = \int_0^{T_l} \frac{(V_C D)^2}{((1-D)n_2)^2 R} dt \tag{2.7}$$

where R is the load resistance and n_2 is the turn ratio of transformer T_2. Equ. (2.7) has been derived from $\int_0^{T_l} \frac{V_O^2}{R} dt$ and the voltage ratio of the flyback transformer in CCM Mode has been substituted into this integration. When the output section is in DCM mode, the energy transferred out of capacitor C is

$$W_{out-DCM} = \int_0^{T_L} \frac{D^2 T_s}{2L_{m2}} V_C{}^2 dt \tag{2.8}$$

It can be seen that V_C is either directly or indirectly related to the energy equations; therefore, what a computer program can try to do for a particular set of operating conditions and converter component values is to determine a value of V_C that can make W_{in} and W_{out} equal, regardless of which of the four possible combination of current conduction modes the converter is in. Such a procedure can be developed as follows for an operating point with input voltage V_{in}, output voltage V_o, switching frequency f_s, duty cycle D, output power P, and component values L_{m1}, L_{m2}, and n_2:

<u>*Step 1:*</u> Assume that i_{Lm2} is continuous then find a value of V_C by relating V_o to V_C using the standard CCM mode flyback equation

$$V_o = \frac{D}{(1-D)} \frac{V_C}{n_2} \tag{2.9}$$

and rearranging to get

$$V_C = \frac{V_o (1-D) n_2}{D} \tag{2.10}$$

<u>*Step 2:*</u> Confirm that i_{Lm2} is actually continuous using

$$I_{Lm2-\min} = \frac{V_C D}{((1-D)n_2)^2 R} - \frac{V_C D T_s}{2L_{m2}} > 0 \tag{2.11}$$

which subtracts the peak magnetizing current ripple from the average magnetizing current. If this equation is satisfied, then i_{Lm2} is actually continuous; otherwise, it is discontinuous and the bus voltage should be determined using

$$V_C = \frac{V_o}{D}\sqrt{\frac{2L_{m2}}{T_s R}} \tag{2.12}$$

Equs. (2.11) and (2.12) are standard flyback converter equations that can be found in power electronic textbooks such as [44]. The derivation of these equations is, therefore, not shown here.

Step 3: The energy that flows into the DC bus capacitor from the converter's input section should be calculated by using (2.4) or (2.6). Before doing so, it should be confirmed whether the input current is semi-continuous or fully discontinuous. If V_C is high enough to demagnetize T_1 by discharging L_{m1} over a time interval equal to (1-D) times the switching period when the input current is at its peak value, then the input current is fully discontinuous and (2.6) should be used; otherwise, the input current is semi-continuous and (2.4) should be used. Similarly, the energy that is transferred out of the DC bus capacitor should be calculated by (2.7) or (2.8), depending on whether i_{Lm2} is continuous or discontinuous as determined from the previous steps.

Step 4: If (2.4) or (2.6) is equal to (2.7) or (2.8), then the calculated DC bus voltage is valid. If not, then D should be changed and the procedure should be repeated until a value of D is found that generates a value of V_C that makes (2.4) or (2.6) match (2.7) or (2.8).

This procedure can be implemented in a computer program to calculate numerous valid operating points that can then be used to generate graphs of steady-state characteristic curves that can be used in the design of the converter. Fig. 2.8 shows a graph of curves of V_C vs. load power for different values of L_{m2} with input voltage V_{in} = $85V_{rms}$, L_{m1} = 90 μH, f_s = 100kHz and V_o = 48V. Fig. 2.8 shows a graph of V_C vs. load power curves for different values of n_2 with Vin = $85V_{rms}$, L_{m1} = 90 μH, f_s = 100kHz and V_o = 48V. The regions where L_{m1} is working in DCM or CCM mode have been differentiated in both graphs. It should be noted that (i) this step of the design procedure is iterative and the graphs shown in Figs. 2.8 and 2.9 are the results of the final iteration,

(ii) the graphs have been drawn for V_{in} = 85 Vrms because if the input current is fully discontinuous for low line and full load, then it will be so for all other operating conditions, (iii) the graphs have been drawn considering T_1 as an inductor.

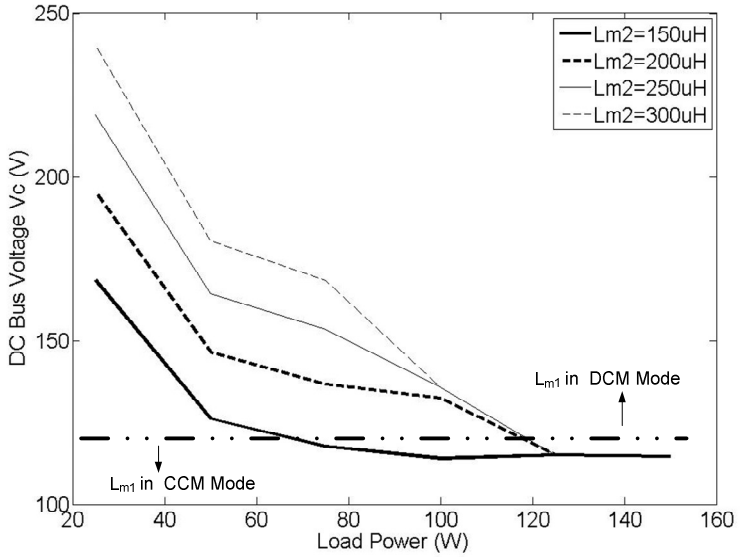


Fig. 2.8. DC bus voltage vs. load power for different values of L_{m2} with V_{in} = 85V_{rms}, L_{m1} = 90 μH, f_s = 100 kHz, V_o = 48V, and n_2 = 2.5.

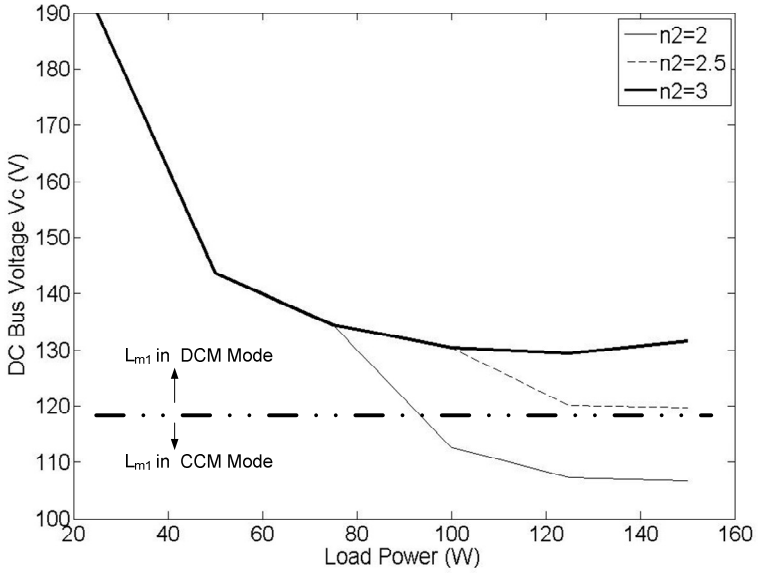


Fig. 2.9. DC bus voltage vs. load power for different values of n_2 with V_{in} = 85V_{rms}, L_{m1} = 90 μH, f_s = 100 kHz, V_o = 48V, and L_{m2} = 180 μH.

It can been seen in Fig. 2.8 that the L_{m2} = 150μH curve crosses into the CCM region of the graph at about P_o = 65W while the L_{m2} = 200μH curve does not cross into the CCM region until the output power exceeds $P_{o,max}$ = 100W. It can been seen in Fig. 2.9 that the n_2 = 2 curve crosses into the CCM region of the graph at about P = 90W while the n_2 = 2.5 curve does not cross into the CCM region until the output power exceeds $P_{o,max}$ = 100W. Based on Figs. 2.8 and 2.9, L_{m2} and n_2 have been selected to be 180 μH and 2.5 respectively to keep L_{m1} in the DCM mode for the whole load power range; moreover, T_2 remains in DCM with these selected values.

2.3.3 Selection of n_1

The next step of the procedure is to consider the operation of the converter with transformer T_1 able to transfer energy directly from the converter input section to the output. The previous steps have established a combination of L_{m1}, L_{m2}, and n_2 that ensure that the current flowing through T_1 is fully discontinuous throughout the line cycle even if the converter operates with low line and with a duty cycle D that does not exceed 0.5. The duty cycle limitation was confirmed in the generation of the characteristic curves shown in Figs. 2.8 and 2.9 so that all operation points on these curves satisfy this criterion.

Since the flow of energy directly from T_1 to the output results in a lower V_C voltage then what would result if there is no such flow, n_1 should be selected so that there is little, if any, direct energy transfer when the converter is operating with low line to keep the input current fully discontinuous and thus ensure an excellent input power factor. In other words, the operation of the converter with T_1 should be the same as if the transformer is implemented with some inductor L_1 under low line conditions. This is why the operation of the converter is just considered with an inductor L_{m1} instead of a transformer T_1 in the initial stages of the procedure.

The turn ratio of T_1, n_1, defines the voltage level of V_C when the converter enters Mode 2, the dual flyback mode of operation, as defined in Section II. It also defines the peak voltage stress across the converter switch as follows:

$$V_{stress} = \begin{cases} V_{in} + V_C & V_C \le n_1 V_o \\ V_{in} + n_1 V_o & V_C > n_1 V_o \end{cases} \tag{2.13}$$

Since the maximum voltage stress is V_{in}+ n_1V_o, rearranging (12) gives

$$n_1 \le \frac{V_{stress} - V_{in-\max}}{V_o} \tag{2.14}$$

If the peak voltage stress can be limited to 500V, based on previous iterations, then the maximum value of n_1 can be found from (14) to be

$$n_{1-\max} \le \frac{500 - 265\sqrt{2}}{48} = 2.65 \tag{2.15}$$

The value of n_1, however, cannot be too small as it would clamp V_C to a voltage that is too low to demagnetize T_1 based on what has been shown in Figs. 2.8 and 2.9. The graphs in these figures show that the minimum acceptable V_C (the value of V_C at the boundary of L_{m1} being in DCM or in CCM) should be 120V. Since this is the case and the output voltage is 48V, then a value of n_1 = 2.5 should be chosen as

$$V_{C-max} = 2.5 \times 48 = 120\ V \tag{2.16}$$

2.3.4 Energy Transfer Ratio

The final step of the procedure is to examine the ratio of energy transferred through T_2 to that transferred through T_1. It is expected that most of the energy from the input is transferred through T_2 when the input voltage is low and through T_1 when the input voltage is high - when the level of V_C tries to rise, but is clamped by T_1 and its secondary diode. Fig. 2.10 shows a graph of energy transfer ratio E = E_{T2}/E_{T1} vs input voltage with V_{in} for different values of L_{m2}. The curves were generated with L_{m1} = 90 μH, f_s = 100 kHz, V_o = 48V, P_o = 100W, n_1 = 2.5 and n_2 = 2.5. The amount of energy transferred through T_1, E_{T1}, and T_2, E_{T2}, was determined by the computer program. This was done for the maximum power of 100W by considering the following:

(i) Since it has been confirmed in previous procedure steps that the input section of the converter is operating in DCM mode, equ. (2.2) can be used to determine the converter's duty cycle D for different values of input voltage as $W_{in\text{-}DCM}$ = power times T_L and the other parameters are known.

(ii) Since it has been confirmed in previous converter steps that T_2 is fully demagnetized by the end of each switching cycle, and V_C = 120V, D, and the other parameters are known, equ. (2.8) can be used to find the amount of energy that is transferred through T_2, E_{T2}.

(iii) Since the amount of energy injected from the input to the converter and E_{T2} have been established, E_{T1} must be the difference between the two.

It can be seen from Fig. 2.10 that more energy goes directly to the output from T_1 if L_{m2} is greater than 180μH. If L_{m2} is less than 180μH, then V_C will be less than 120V and the input may no longer be fully discontinuous throughout the line cycle. What this does is that it makes T_1 the main power transformer through which power is transferred to the output and it increases the output ripple significantly as more of the 120Hz frequency component due to the rectified voltage of the input diode bridge is reflected to the output. This is especially true when V_{in} is at low line and the input current is at its maximum value. In order to change this ratio and ensure that a greater amount of energy is transferred through T_2, the value of n_1 must be increased so that less energy is transferred directly through T_1. Doing this, however, increases the voltage level at which V_C is clamped and increases drain-source voltage of the switch so that it exceeds 500V.

It should be mentioned that the magnetizing current of T_2, i_{Lm2} may become continuous with very large values of L_{m2}. As Fig. 2.10 shows, increasing L_{m2} reduces the transferred energy from this transformer sharply which is not a desired case; therefore, smaller values for L_{m2} are preferred. It should be noted that Fig. 2.10(b) is just a magnified portion of Fig. 2.10(a) and that E_{T2}/E_{T1} approaches infinity in Fig. 2.10(a) as V_{in} approaches 85 Vrms because the converter has been designed so that E_{T1} = 0 when the input voltage is 85 Vrms. The lowest value of V_{in} shown on the graph of Fig. 2.10(a) is V_{in} = 86 Vrms.

2.3.5 Diode Voltage Ratings

The maximum steady state reverse voltages of the diodes which are used in the converter are as follows:

$$V_{rev.-D1} = n_1 V_o + V_{in(peak)} = 2.5 \times 48 + \sqrt{2} \times 265 = 445\,V \tag{2.17}$$

$$V_{rev.-D2} = 2 n_2 V_o = 240\,V \tag{2.18}$$

$$V_{rev.-D3} = V_{in(peak)} / n_1 + V_o = 265\sqrt{2} / 2.5 + 48 = 197V \tag{2.19}$$

$$V_{rev.-D4} = Vdc / n_2 + V_o = 120 / 2.5 + 48 = 96 \tag{2.20}$$

2.4 Experimental Results

A 100-W experimental prototype was built to verify the working of the proposed configuration. The prototype was designed according to following specifications:

V_{in} = 85-265V_{rms}

V_o = 48V_{DC}

P_o = 100W

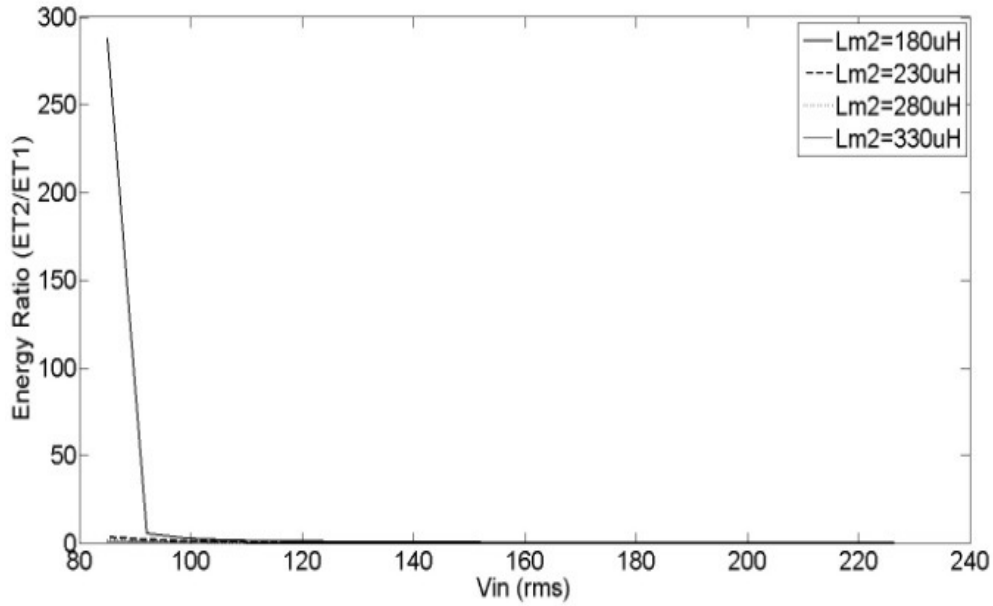
f_{sw} = 100kHz

The following devices were used for the semiconductors in that circuit:

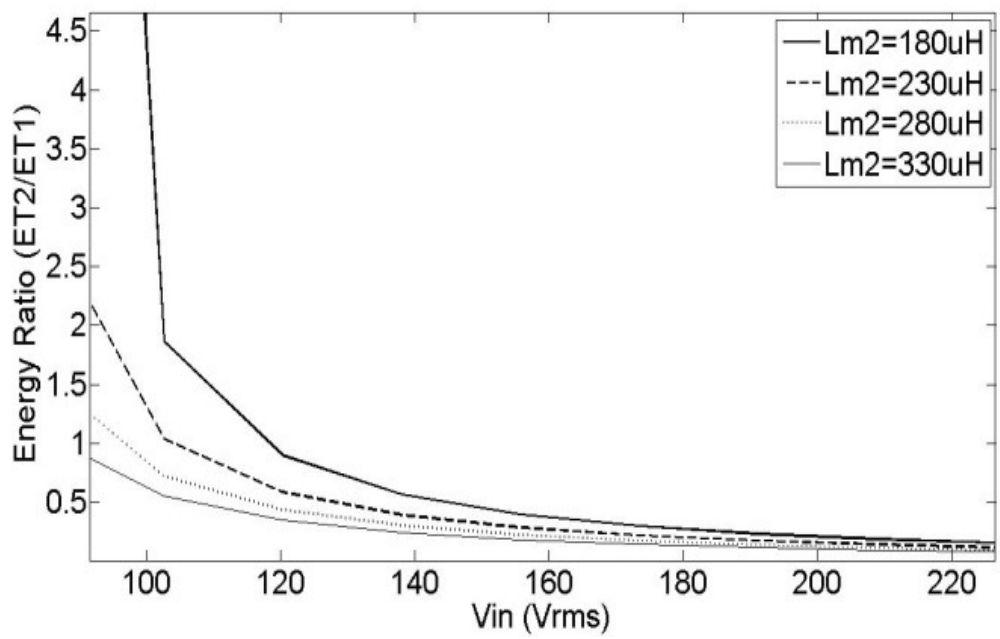
Main Switch: IRF840

D_1 and D_2: RHRP1560

D_3 and D_4: U1540



2.10(a)



2.10(b)

Fig. 2.10 Energy ratio (E_{T2}/E_{T1}) vs. rms input voltage V_{rms} with $L_{m1} = 90\mu H$, $f_s =$ 100kHz, $V_o = 48V$, $P_o = 100W$, $n_1 = 2.5$ and $n_2 = 2.5$.

Figs. 2.11 – 2.15 show typical switch voltage waveforms and typical primary and secondary current waveforms of T_1 and T_2 for different input voltages. Fig. 2.11 shows that T_1 and T_2 are working in DCM mode when the input voltage is at its minimum and that both transformers are fully demagnetized after the switch is turned off. Fig. 2.12 shows the same currents and voltage for the maximum input voltage. As can be seen, V_{DS} reduces to input voltage when T_1 has been completely discharged. Fig. 2.13 shows the output current of T_2 and the drain-source voltage of the switch when input voltage is at the minimum and the load is at its maximum value. It shows that T_2 is completely discharged within the switching cycle. It should be noted that overvoltage spikes that could appear across the switch due to the leakage inductance of T_2 have been snubbed by a typical RCD snubber that has been placed across the switch.

Fig. 2.14 shows drain-source voltage of the switch and secondary current of T_2 when input voltage is at its maximum voltage. It shows that T_2 is fully demagnetized before the start of the next switching cycle. Fig. 2.15 shows an input voltage waveform and the envelope of the secondary current of T_1. It can be seen that the current through T_1 is higher when the input voltage is high, which means that more energy is transferred to the output during this time.

Fig. 2.16 shows the input voltage and filtered current waveforms when the input voltage is 100 and 230Vrms. In both cases, the filtered input current confirms that sinusoidal current waveforms can be achieved by the converter as long as the input section is working in DCM mode. Fig. 2.17 shows the harmonic content of the converter when it is operating at V_{in} = 100Vrms and V_{in} = 230Vrms. It can be seen that the converter satisfies IEC 61000-3-2 standards. Fig. 2.18 shows the DC bus voltage vs. input voltage for different load power conditions. These results confirm that the DC bus voltage is almost fixed for different load and input voltage conditions. This makes it easier to satisfy hold- up time requirements for all different load and input voltage conditions if such a feature is needed.

It should be noted that the bus voltage is not clamped to exactly n_1V_o = 120V because of non-idealities in the converter components and transformers such as leakage inductance. The increase in V_C that occurs when the input voltage is increased is due to

the fact that primary and secondary leakage inductances have voltage drops that become larger as more current flows in T_1, which is what happens as input voltage is increased.

Fig. 2.19(a) shows the efficiency vs. load power when input voltage is equal to $230V_{rms}$. Fig. 2.19(b) shows the efficiency of the converter vs. different input voltage when load power is 100 W. The measured efficiency was found to be very similar to other previously proposed single-stage converters, but the proposed converter has a better input current harmonic content and a nearly fixed DC bus voltage [11]. This allows the converter to operate with smaller DC bus capacitors and smaller sized transformers as they do not have to handle the voltages that these components must handle in other converters. This is especially true if hold-up time is a consideration.

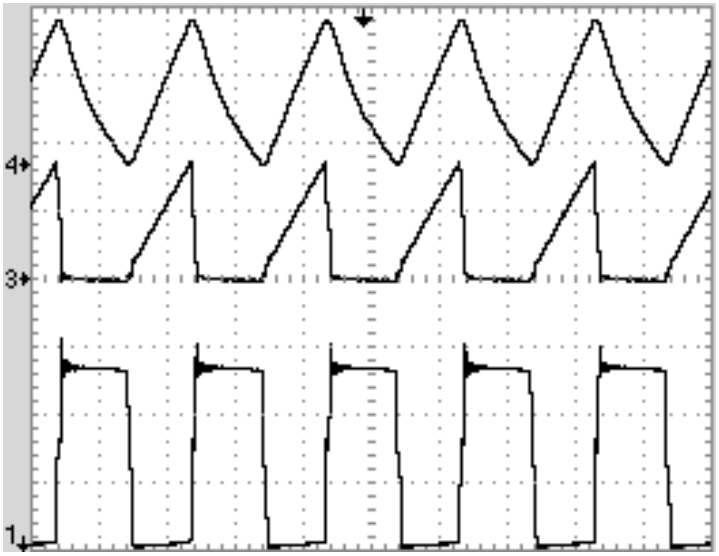


Fig. 2.11 Primary current of T_1 (upper signal), primary current of T_2 (middle signal) and drain-source voltage of the switch (lower signal),

$P = 100W$, $V_{in} = 85V_{rms}$, $V_o = 48V$, $I = 2A/div$, $V_{DS} = 100V/div$, $t = 5\mu s/div$

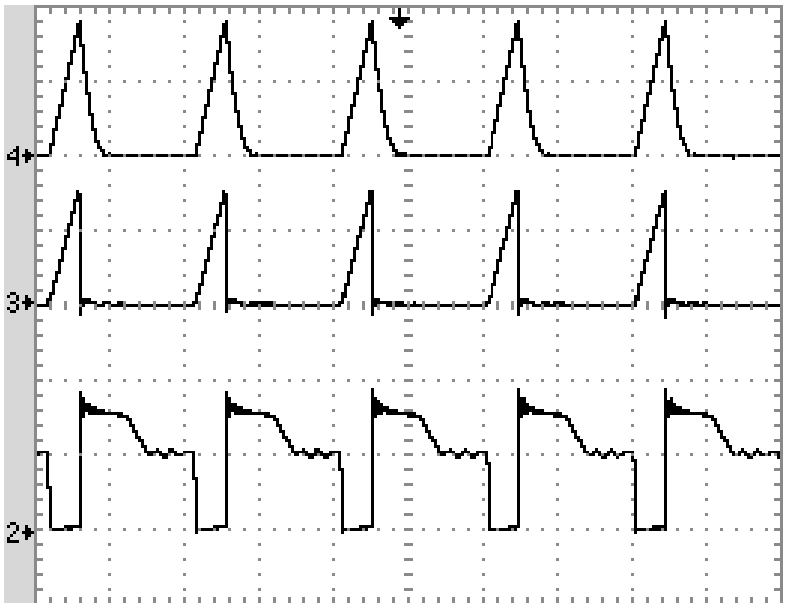


Fig. 2.12 Primary current of T_1 (upper signal), primary current of T_2 (middle signal) and drain-source voltage of the switch (lower signal),
P = 100W, V_{in} = 230V_{rms}, V_o = 48V, I_{T1} = 2A/div, I_{T2} = 1A/div, V_{DS} = 250V/div, t = 5µs/div

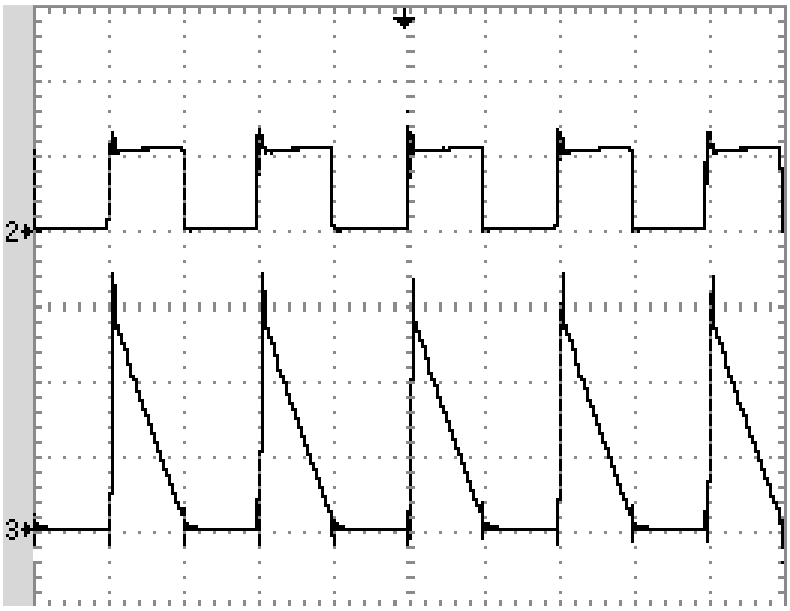


Fig. 2.13 Drain-source voltage of the switch (upper signal) and output current of T_2 (lower signal) P = 100W, V_{in} = 85V_{rms}, V_o = 48V, V_{DS} = 250V/div, I = 2A/div, t = 5µs/div

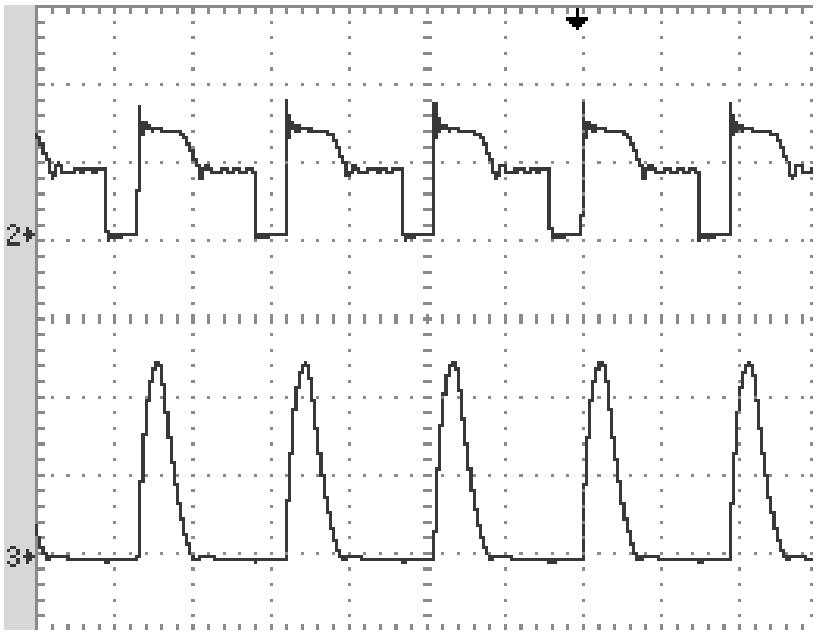


Fig. 2.14 Drain-source voltage of the switch (upper signal) and output current of T_1 (lower signal) P = 100W, V_{in} = 230V_{rms}, V_o = 48V, V_{DS} = 250V/div, I = 2A/div, t = 5µs/div

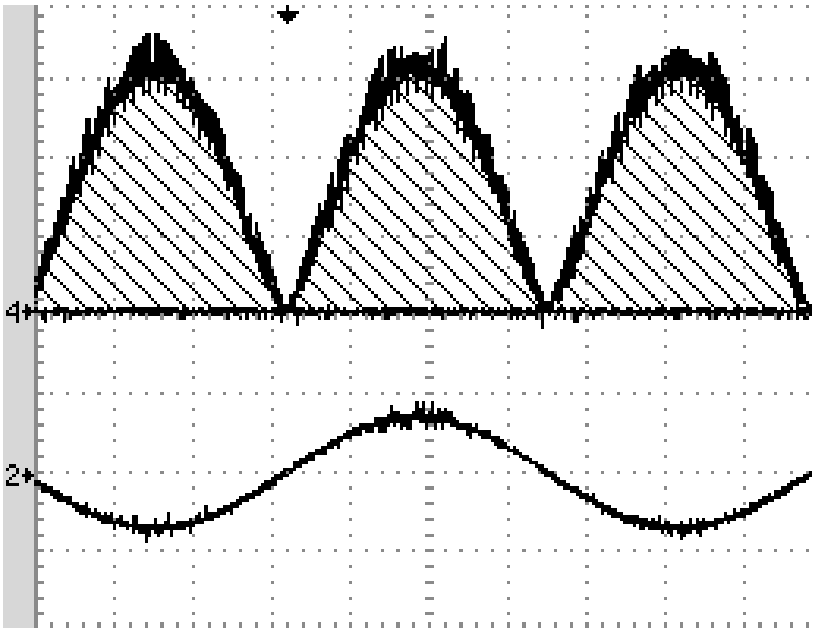
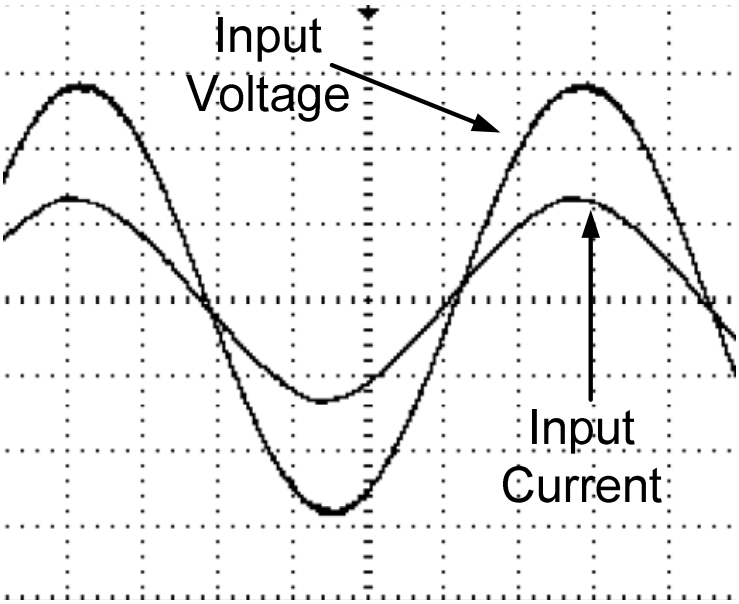


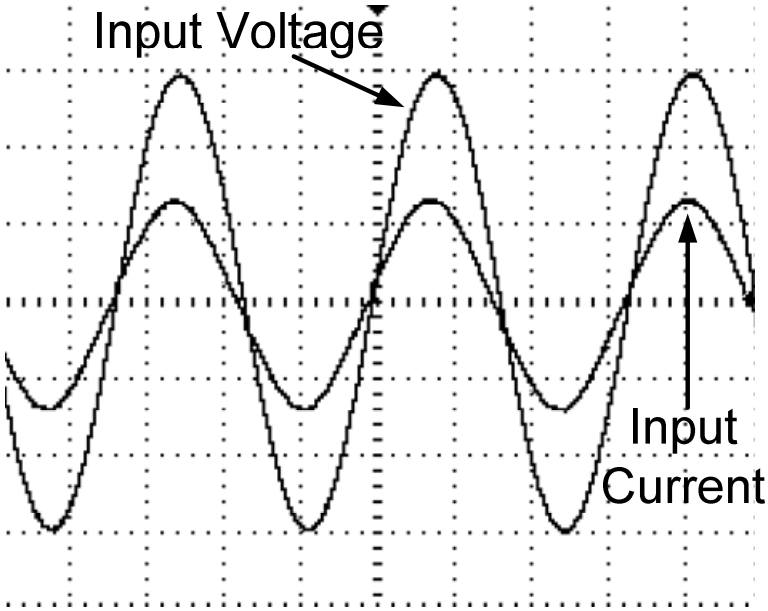
Fig. 2.15 Peaks of the output current from secondary winding of T_1 (upper signal) and input voltage (lower signal)

P = 100W, V_{in} = 230V_{rms}, V_o = 48V, I = 5A/div, V = 500V/div, t = 2.5ms/div.



(a): $V_{in} = 100V_{rms}$

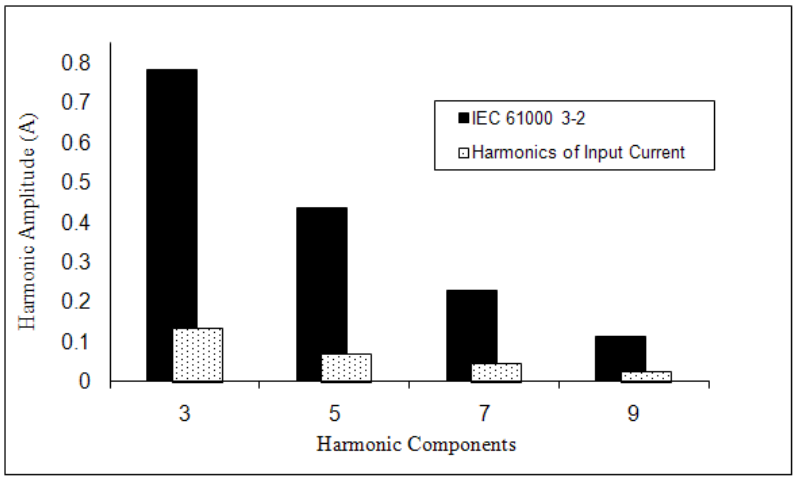
V = 50V/div, I = 1A/div, t = 2.5ms/div



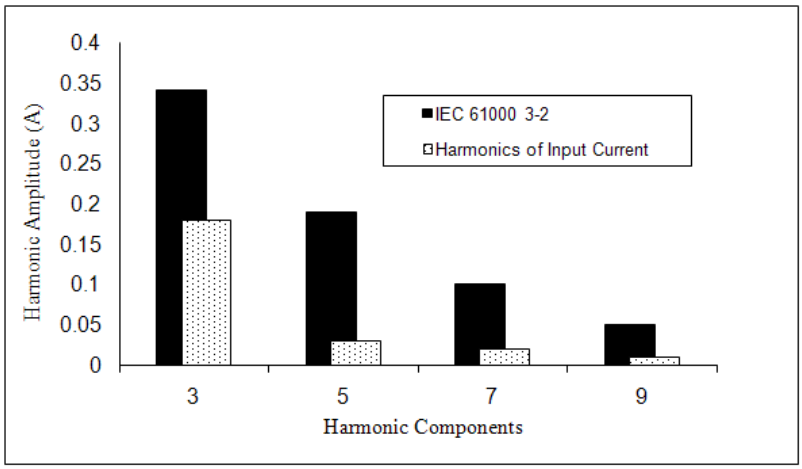
(b): $V_{in} = 230V_{rms}$

V = 100V/div, I = 500 mA/div, t = 5ms/div

Fig. 2.16 Input voltage and current waveforms



(a) V_{in}=100V



(b) V_{in} =230V

Fig. 2.17 Harmonic components of input current when P_o = 100W and V_o = 48V for two different input voltage

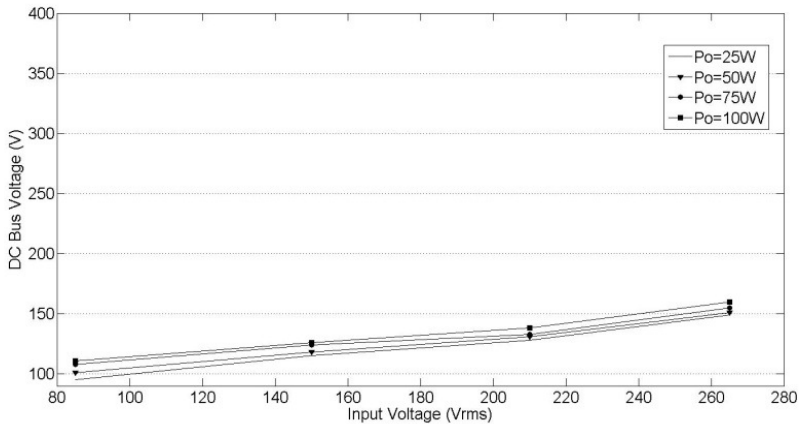
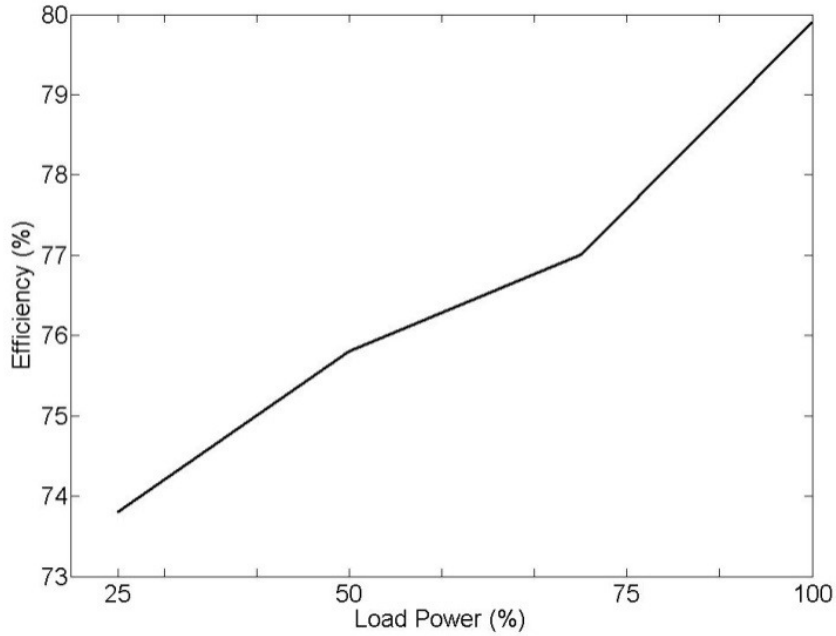
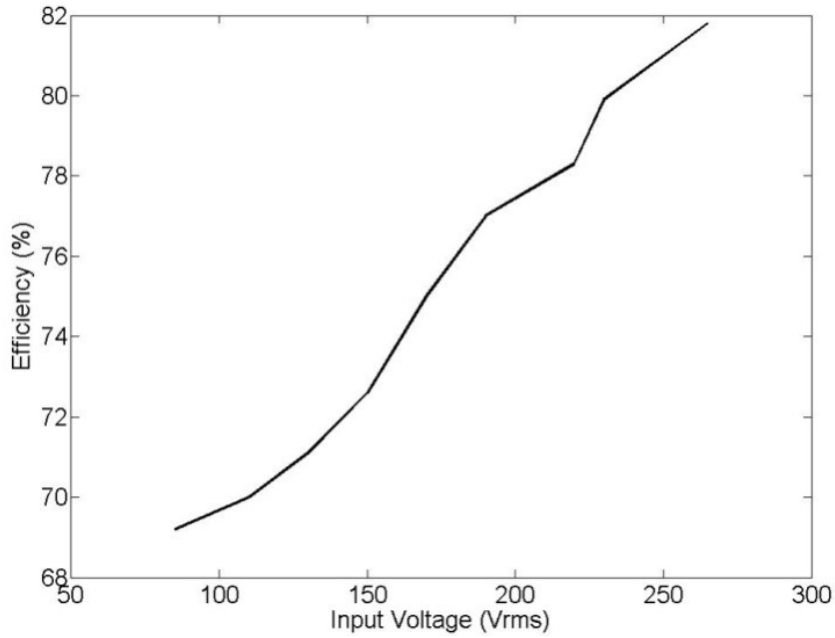


Fig. 2.18 DC bus voltage vs. input voltage for different load power



(a) Efficiency vs. load power ($V_{in} = 230V_{rms}$)



(b) Efficiency vs. V_{in} (load power = 100%)

Fig. 2.19 Efficiency of the converter

2.5 Conclusion

In this chapter, a new single-stage high-power factor converter is proposed. The proposed converter uses a buck-boost input section that can step up or step down input voltage and a voltage clamping mechanism at the DC bus. The outstanding feature of this converter **is** that its DC bus voltage variation is significantly less than of other single stage converters, which allows smaller sized components to be used. This is the result of buck-boost type input section and clamping of V_C by the secondary winding of T_1 to n_1V_o. In the chapter, the operation of the converter was explained, and key characteristic equations were derived and used to design the converter. The feasibility of the converter – its ability to operate with a nearly fixed DC bus voltage regardless of line and load conditions and its ability to operate with an excellent input power factor - were confirmed with results obtained from an experimental prototype.

Chapter 3
Analysis and Design of an AC/DC Single-Stage Buck-Boost Full-Bridge Converter

3.1 Introduction

In the previous chapter, a new low power AC/DC single-phase, single-stage converter was proposed. In order to confirm the feasibility of buck-boost converter principles for higher power applications, a buck-boost type single-stage full-bridge converter is proposed in this chapter. In the chapter, the operation of the converter is explained and steady-state analysis is discussed. Based on this analysis, design considerations for the DC bus voltage, input inductor, transformer turn ratio and output inductor are examined and a design procedure is determined and demonstrated with an example. Experimental work is presented at the end of this chapter to confirm the feasibility of the proposed full-bridge converter.

3.2 Converter Operation

Fig. 3.1 shows the proposed converter. The converter combines an AC/DC buck-boost power factor correction (PFC) converter and a DC/DC full bridge converter. The buck-boost input section consists of L_1, the buck-boost inductor, C, which is the DC bus capacitor, and freewheeling diode D_1. The full-bridge DC/DC converter consists of switches S_1 to S_4, a transformer and diodes D_4 and D_5. L_2 and C_o form the output filter and diodes D_2 and D_3 are blocking and freewheeling diodes respectively.

Switch S_2 is the shared switch between two different parts of the converter. It works as the buck-boost switch and one of the switches of full bridge DC/DC converter. The input inductor L_1 is connected to switch S_2 to shape the input current and performs power factor correction. When this switch is turned off, the stored energy in the inductor L_1 goes to DC bus capacitor. When two diagonal switches are on, the DC bus voltages is placed over the primary winding of the transformer and sends the stored energy in that capacitor to the output through the secondary winding of the transformer and diodes D_4 and D_5.

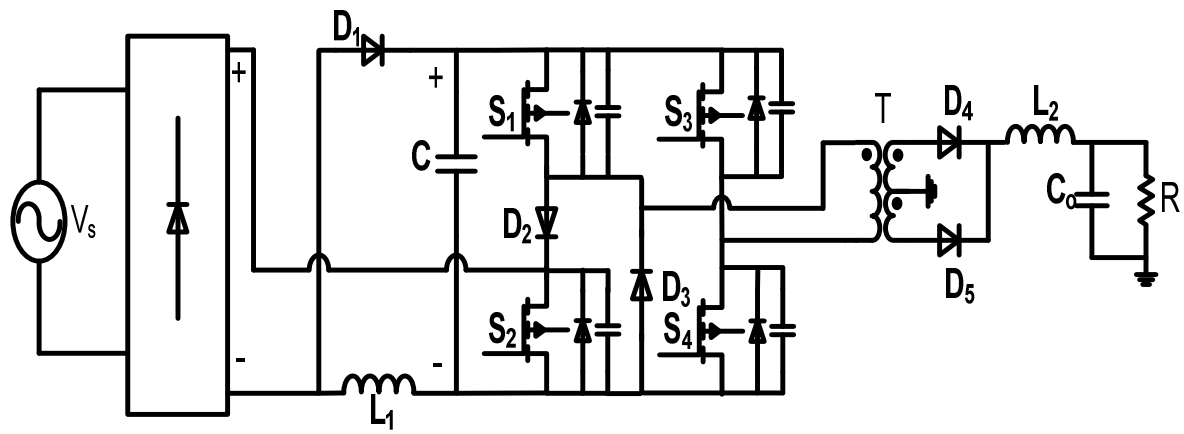


Fig. 3.1 Proposed converter

The converter's modes of operation are shown in Fig. 3.2. Each mode can be described as follows:

Mode 1 (t_0-t_1): S_2 is turned on at $t = t_0$. Prior to $t = t_0$, there was no current in input inductor L_1 and the converter was in a freewheeling mode of operation with current flowing through D_3 and S_4. After $t = t_0$, current in L_1 starts to rise and the converter continues to be in a freewheeling mode.

Mode 2 (t_1-t_2): S_4 is turned off at $t = t_1$. During this mode, current is transferred from S_4 to the body diode of S_3 and flows into the DC bus capacitor, C, and through D_3. S_3 is turned on sometime during this mode in preparation for the next mode. Current continues to rise in L_1.

Mode 3 (t_2-t_3): At $t = t_2$, the current through S_3 reverses direction and current from both the full-bridge section and the buck-boost section flow through S_2. The converter is in an energy-transfer mode as voltage is impressed across the transformer primary and energy from bus capacitor C is transferred to the output.

Mode 4 (t_3-t_4): S_3 is turned off at $t = t_3$ and current is transferred to the body diode of S_4 sometime during this mode. Also during this mode, S_4 is turned on in preparation for the next mode and the freewheeling current from the converter's full-bridge section and the input current are flowing through S_2. There is no voltage impressed across the transformer primary and no energy is transferred from primary to secondary.

Mode 5 (t_4-t_5): S_2 is turned off at $t = t_4$ and current is eventually transferred to the body-diode of S_1 sometime during this mode. S_1 is turned on sometime during this mode in preparation for the next mode. The current that was flowing through L_1 now flows to C through D_1 and falls as it does so.

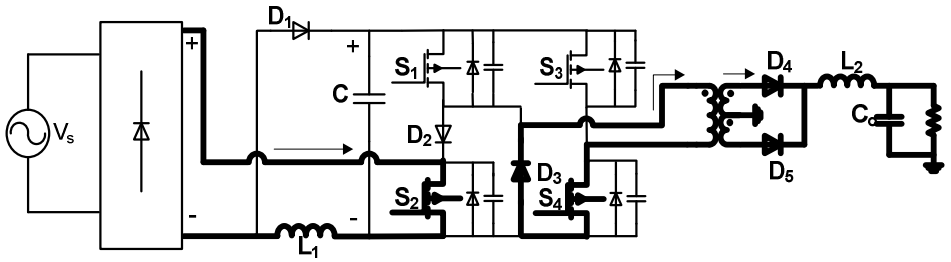
Mode 6 (t_5-t_6): The current through S_1 reverses direction at $t = t_5$ and the converter is in an energy-transfer mode as voltage is impressed across the transformer primary and energy from bus capacitor C is transferred to the output. The current through L_1 continues to fall as it flows through D_1 and C.

Mode 7 (t_6-t_7): At $t = t_6$, current stops flowing through L_1 since L_1 is working in discontinuous current mode (DCM) and the full-bridge section continues to be in an energy-transfer mode.

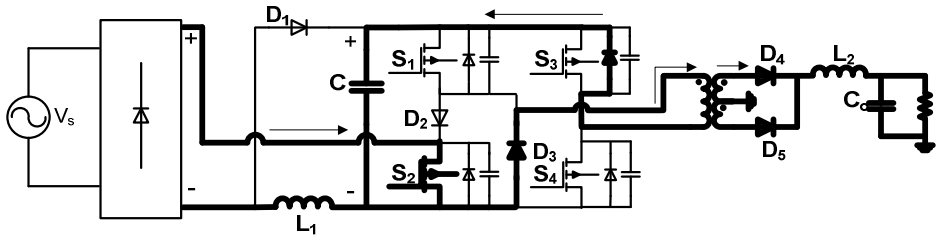
Mode 8 (t_7-T_S): S_1 is turned off at $t = t_7$ and current is eventually transferred to D_3 sometime during this mode. The converter is in a freewheeling mode and continues to be until $t = T_S$, which is the end of the switching cycle and the start of a new one.

The following should be noted:

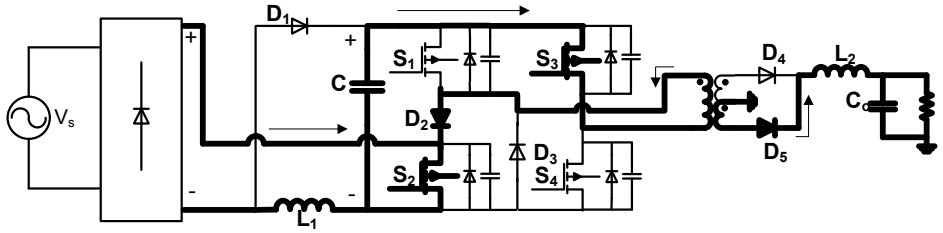
- The converter switches operate with asymmetrical pulse width modulation (APWM). This means that S_2 and S_4, which are the two bottom converter switches, are allowed to be on for time intervals in which duty cycle $D>0.5$. This is especially true when the converter is operating under maximum load and minimum input voltage conditions. The gating signals for switches S_1 and S_3 are the complement of those of the two bottom switches with the signal of S_1being the compliment of that of S_2 and the signal of S_3 being the compliment of that of S_4. This is unlike the phase-shift PWM that is typically used in DC/DC converter where all the switches have a gating signal that is half the switching cycle ($D = 0.5$) and the gating signals of the switches of one converter leg are phase-shifted with respect to those of the other leg.



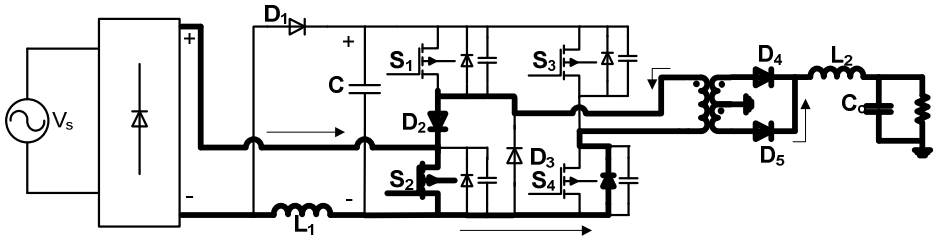
(a) Mode 1



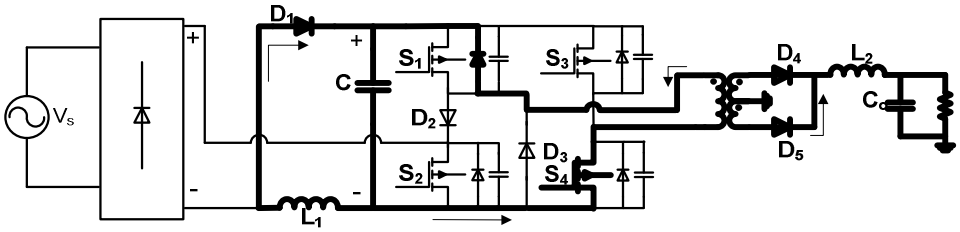
(b) Mode 2



(c) Mode 3



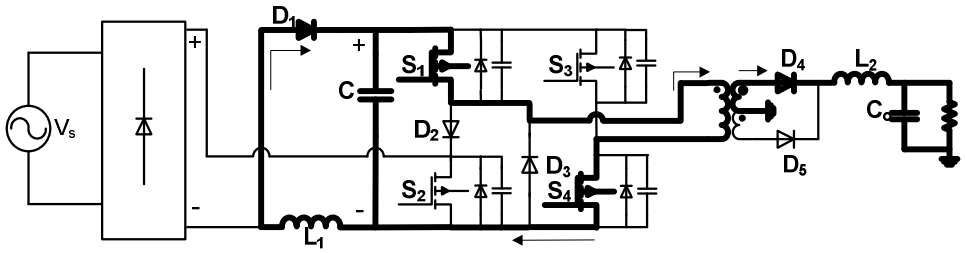
(d) Mode 4



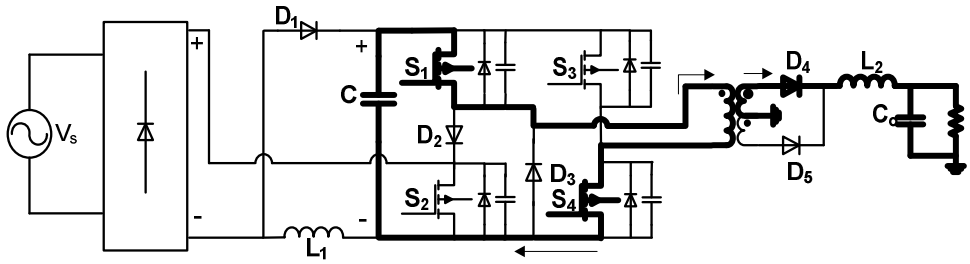
(e) Mode 5

Fig. 3.2 Different modes of operation

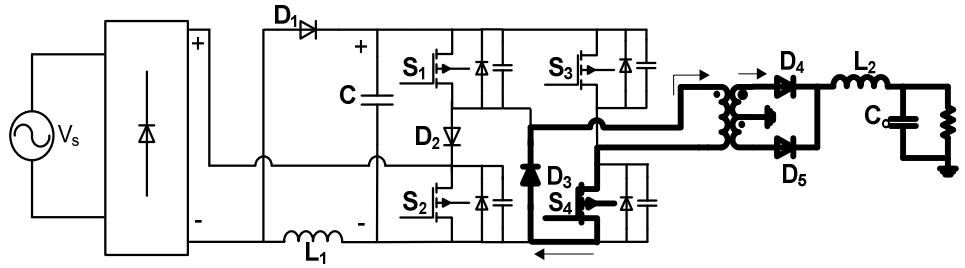
To be continued in the next page.



(f) Mode 6



(g) Mode 7



(h) Mode 8

Fig. 3.2 Different modes of operation

If conventional phase-shift PWM is used, then the peak current in S_2 and the input inductor will be very high if the maximum on-time of S_2 is limited to D=0.5 for maximum load and minimum input voltage situation.

- Diode D_2 is required to limit the freewheeling path of the buck-boost current to L_1, C and D_1. If this diode is left out, there will be a path through the primary winding of the transformer, S_2, L_1 and the input diode bridge. This will make the input current continuous, which is not desirable as the input current will no longer be discontinuous and bounded by a sinusoidal envelope. This will result in increased input current harmonic distortion and reduced power factor.
- Diode D_2 blocks the body diode of S_2. In order to open a freewheeling path, diode D_3 is required in the converter.

  Fig 3.3 shows typical converter waveforms.

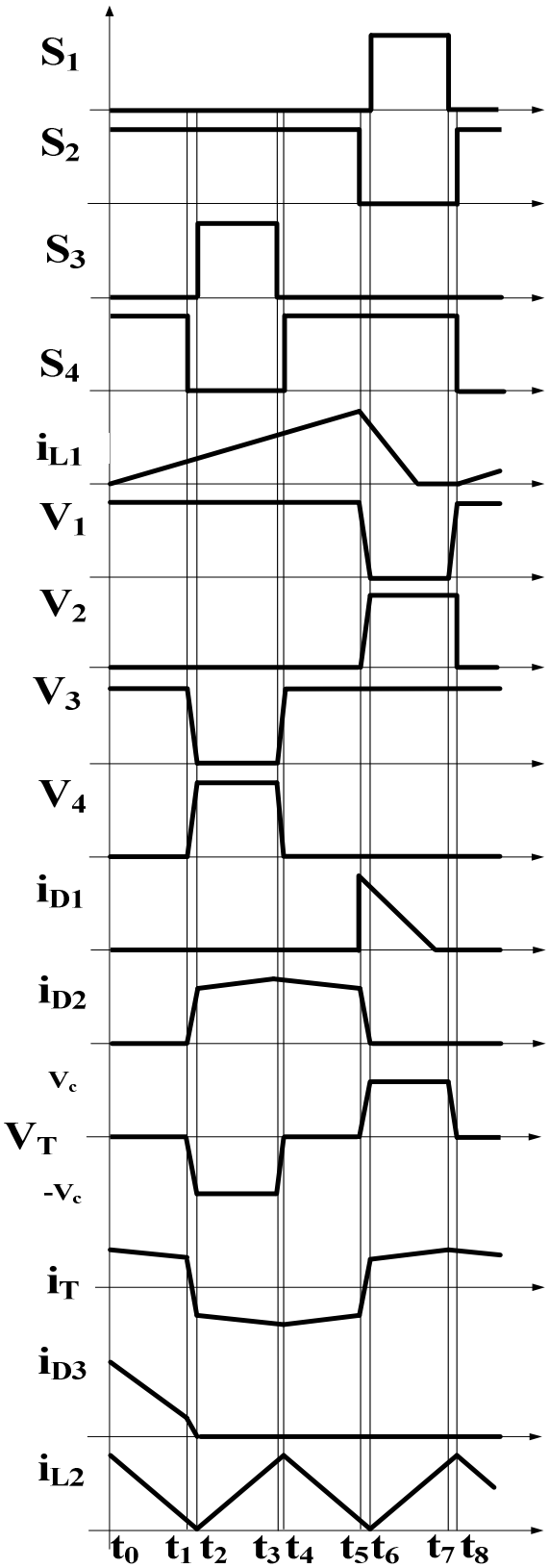


Fig. 3.3 Typical waveforms

3.3 Steady State Analysis

In order to design the converter properly, the key parameter that should be known in different load and input voltage situation is the voltage of DC bus capacitor, which is V_C. Unlike a conventional two-stage converter, V_C is not solely regulated by the AC–DC boost PFC stage and cannot be purposefully kept constant. This voltage can be derived by noting that an energy equilibrium must exist for capacitor when the converter is in steady-state operation. The energy pumped into the capacitor from the input section must be equal to the energy that capacitor provides to the output, so that the net DC current flowing in and out of C must be zero during a half-line cycle. V_C , however, cannot be determined by an equation with a closed-form solution, due to the various possible combinations of input and output modes of operation, but must instead be determined using a computer program.

The following steps explain the algorithm that has been written as a computer program to determine the voltage of the capacitor:

- Assume a duty cycle as an initial "guess" (i.e., D=0.5).
- Assume that the output current is continuous; then, use (3.1) to find $_{VC}$.

$$V_C = \frac{V_o n}{D} \tag{3.1}$$

  V_o is output voltage of the converter and n is the transformer turn ratio.

- With this value of V_C, verify that the output current is continuous by seeing that the peak output current ripple does not exceed the average output current I_o.

$$I_o > \frac{1}{2}\frac{(V_C/n - V_o)}{L_2}\frac{D}{2f_s} \tag{3.2}$$

  f_s is the switching frequency.

- If this relation is satisfied, then V_C is equal to the value determined in (3.1). If not, then the output current is discontinuous and V_C must be determined using (3.3), which has been derived for DCM.

$$V_C = \frac{n(V_o + \sqrt{V_o^2 + \frac{4P_oL_of_s}{D^2}})}{2} \tag{3.3}$$

P_o is load power.

- With V_C known, find the average current that flows out of capacitor C during a half-line cycle using either (3.4) for CCM or (3.5) for DCM.

$$I_{C,out} = \frac{I_oD}{n} \tag{3.4}$$

$$I_{C,out} = \frac{V_CD}{4n^2L_2}(\frac{V_C}{nV_o} - 1)D^2 \tag{3.5}$$

- Determine the average current that is fed to C from the input during a half-line cycle using (3.6)

$$I_{avg} = \sum_{j=0}^{k} \frac{I_{j,peak}}{2} \tag{3.6}$$

$$\mathrm{I_{peak}} = \int_0^{\mathrm{T_s}} \frac{\mathrm{V_P Sin(\omega t)}}{\mathrm{L_1}} \mathrm{dt} \tag{3.7}$$

- If (3.6) is equal to (3.4) or (3.5), this means that the converter is operating under steady-state conditions with the initial value of D that was "guessed". If not, then D should be changed and the above steps repeated until it is ensured that the converter is operating under steady-state conditions.

3.4 Converter Characteristics

Based on the analysis of the converter's steady-state characteristics that was described in the previous section of this chapter, a set of graphs of characteristic curves that show the

effects that certain key parameters have on the operation of the converter can be generated. Examples of such graphs are shown in Figs. 3.4 to 3.6.

Fig. 3.4 shows a graph of DC bus capacitor voltage vs. load for different values of L_1. It can be seen that for lower input inductor values, the DC bus voltage is lower when the load has its higher values and vice versa. This is due to the fact that the converter is working with APWM. When the input inductor has a lower value, the duty cycle shrinks to less than 0.5 and converter goes to the buck mode. The voltage over the transformer is wider with lower values to send the same amount of energy to output when L_1 has its higher values. But lower values of L_1 result in higher peak currents through this inductor and through S_2. Fig. 3.5 shows the DC bus voltage vs. load power for various output inductor values. For the higher values of L_2, the DC bus voltage is higher since the output inductor goes into continuous conduction mode (CCM) for the whole range of load power.

Fig. 3.6 shows the DC bus voltage vs. load power for different values of transformer turn ratio. It can be seen that for lower values of n and for higher values of load power, the input inductor current is continuous. This is due to the fact that the DC bus voltage is not high enough to de-energize the input inductor completely during the switch off time (1-D)T. On the other hand, higher values of n, increase the DC bus voltage to more than 450 V, which is undesirable, and it increases the voltage stress of the converter components.

Considering the above mentioned characteristic curves the components of the converter have been selected as follows:

$L_1 = 40\mu H$

$L_2 = 5\ \mu H$

$n = N_1/N_2 = 5$

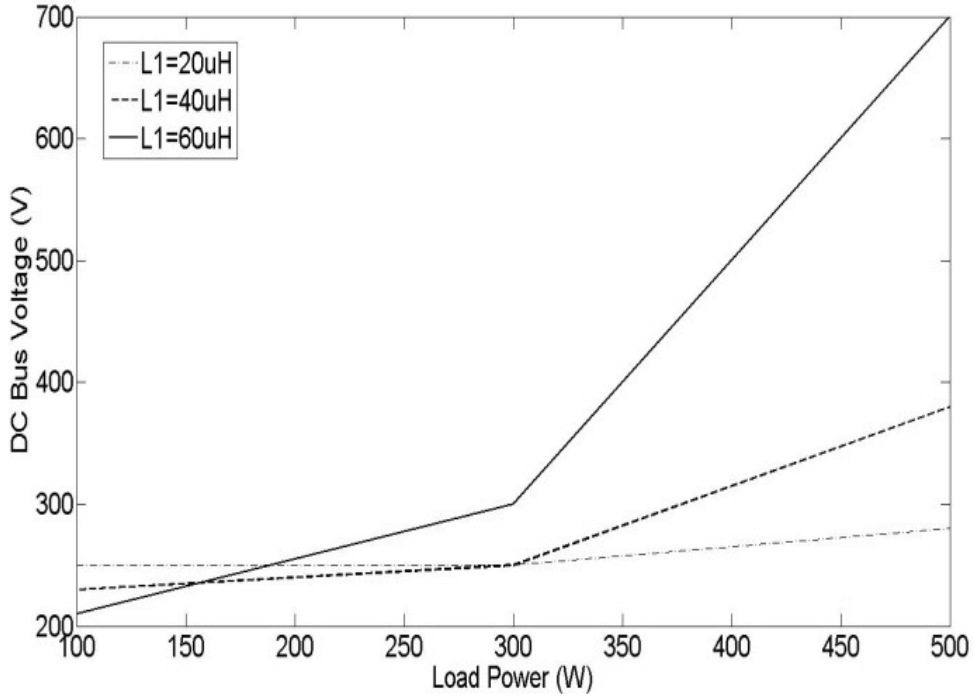


Fig. 3.4 DC bus voltage vs. load power for different values of L_1 when n=4 and L_2=5μH (V_{in} = 85V_{rms} and V_o = 48V)

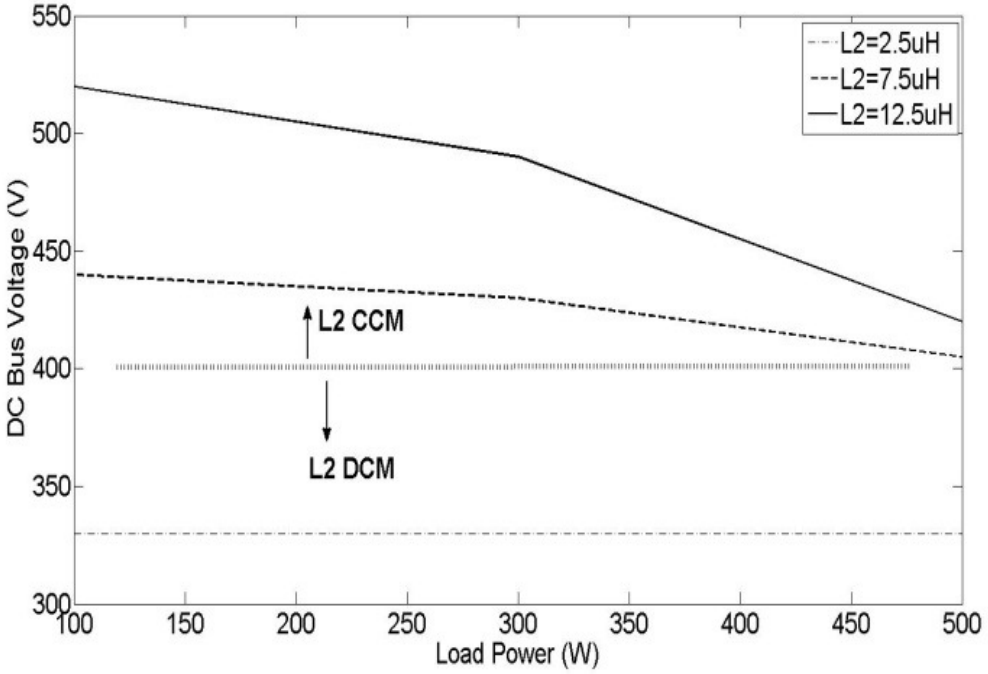


Fig. 3.5 DC Bus voltage vs. load power for different values of L_2 when L_1=40μH and n=4 (V_{in} = 85V_{rms} and V_o = 48V)

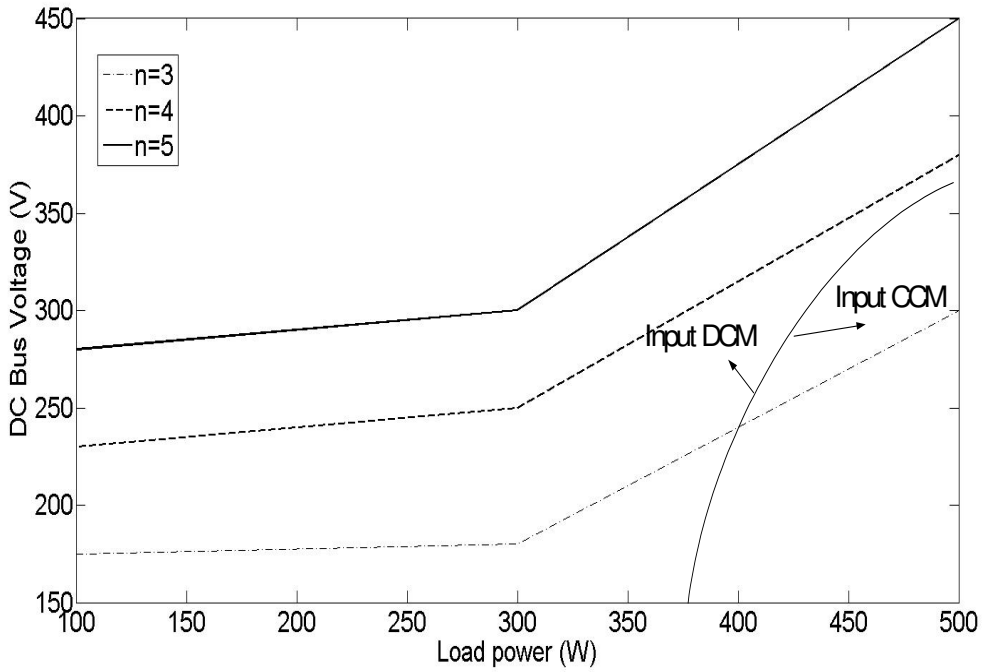


Fig. 3.6 DC bus voltage vs. load power for different values of n when L_1=40μH and L_2=5μH (V_{in} = 85V_{rms} and V_o = 48V)

3.5 Experimental Results

An experimental prototype was built to confirm the feasibility of the converter. The specifications of the converter were as follows:

- Input voltage V_{in} = 85-265 V_{rms}
- Output voltage V_o = 48 V
- Switching frequency = 100 kHz
- Maximum load power = 500 W

Typical experimental waveforms can be seen in Fig. 3.7 to 3.10. It can be seen in Fig. 3.7 that the converter can operate with a near unity input power factor without input current distortion. This is because the input current is discontinuous and bounded by a sinusoidal envelope. Fig. 3.8 shows the drain-source voltage of S_1 and the inductor current. It can be seen that the inductor current is discontinuous. It should also be noted that the lack of distortion in the input current is unlike what is found in most boost-based

single-stage converters, which rely on auxiliary windings taken from the main power transformer to keep the DC bus voltage below 450 V. These windings limit the conduction angle of the input section of the converter and it is this limitation that caused the input current to be distorted.

It can be seen in Fig. 3.9 that the output inductor current waveform is at the boundary of continuous-discontinuous at full load. Fig. 3.10 shows a graph of DC bus voltage (voltage across capacitor C) vs. load power for two different input voltages. It can be seen that the DC bus voltage has much less variation the entire line range, from 20% to full load, than what is typically found in a boost-based single-stage converter. The DC bus voltage is almost fixed for the maximum input voltage. This makes the converter especially attractive for applications where hold-up is an issue.

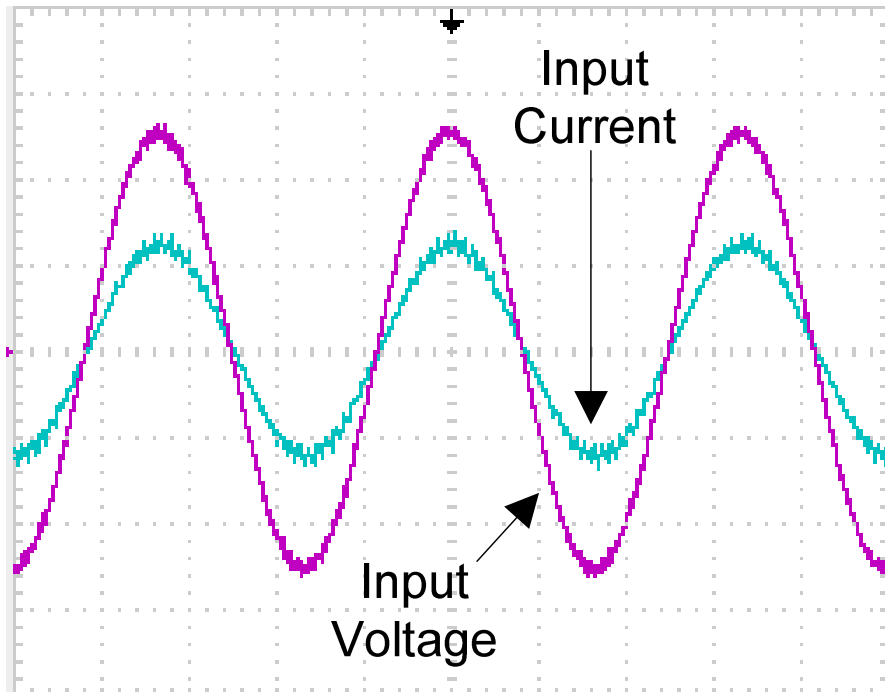


Fig. 3.7 Input voltage and current
V=50 V/div, I=5 A/div, t=5 ms/div

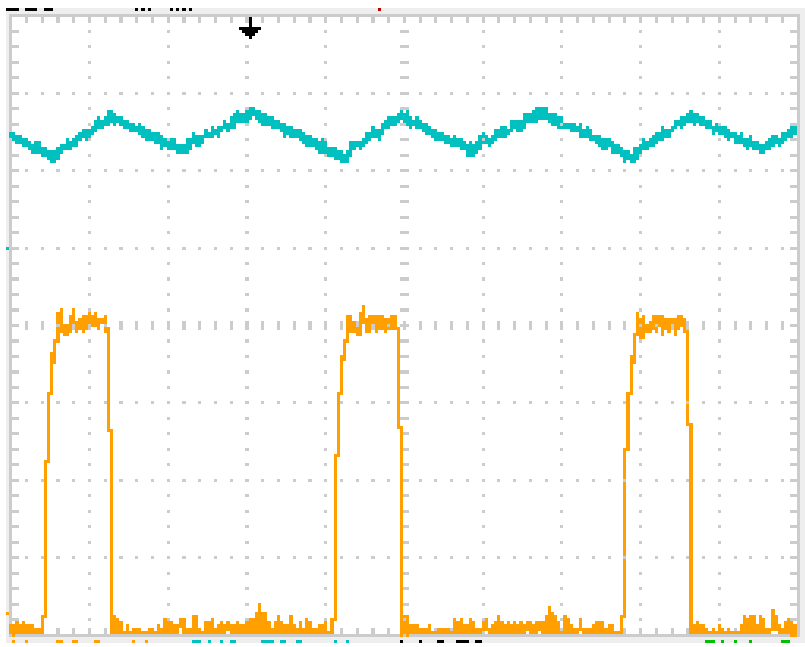


Fig. 3.8 Output current (upper signal), and drain source voltage of S_4 (lower signal) V=100 V/div, I=5A/div, t=2.5us/div

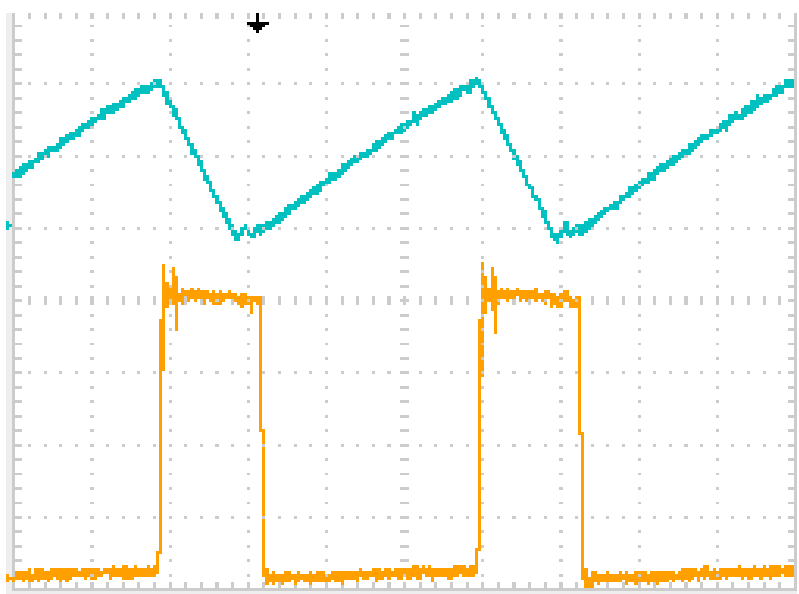


Fig. 3.9 Current through L_1 (upper signal), and drain source voltage of S_2V=100 V/div, I=10A/div, t=1us/div

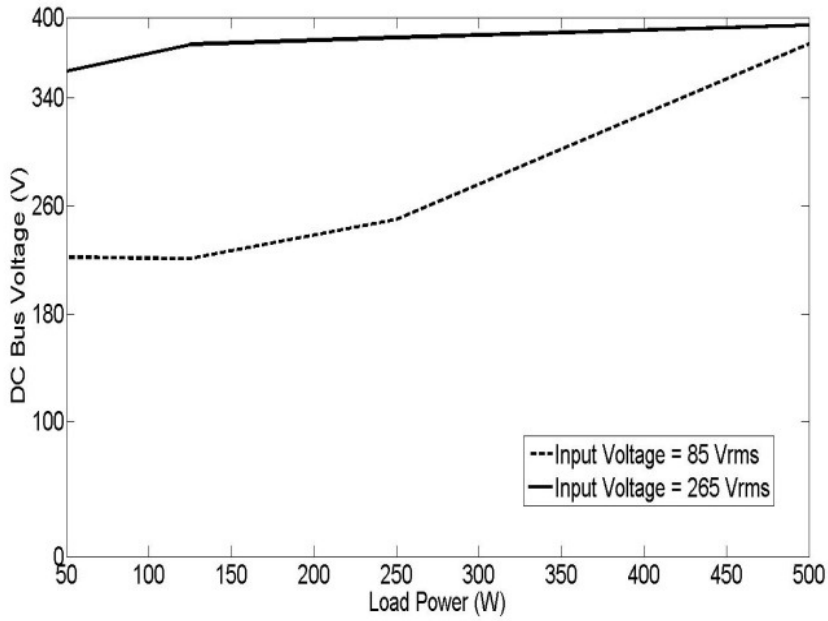


Fig. 3.10 DC bus voltage vs. input voltage for different load power

3.6 Conclusion

A new AC/DC single-stage PWM full-bridge converter was proposed in the chapter. The input section of this converter was designed based on the buck-boost converter. The attractive features of the converter are that it can operate with near unity input power factor, and a DC bus voltage that is always less than 450 V and that has much less variation with line and load change than boost-type single-stage converters. In the chapter, the operation of the converter was explained, its key steady-state characteristics were determined by mathematical analysis and were shown with graphs of steady-state characteristic curves, and its components were designed according to these characteristic curves. Results obtained from an experimental prototype confirmed the feasibility of the proposed converter.

Chapter 4

A New Three-Phase Inverter with Active Clamp Operating Range Extension Technique

4.1 Introduction

The focus of Chapters 2 and 3 of this thesis was to investigate the use of the basic buck-boost converter topology to develop new AC/DC single-phase, single-stage converters that do not have the key drawback that single-stage converters based on boost converters do, which is a potentially excessive intermediate DC bus voltage. Single-stage converters that are based on buck-boost converters have input sections with an inherent voltage step-up/step-down capability so that their input sections can try to step down the input AC voltage when it is high and try to step down the input voltage when it is high. As a result, the variation of the intermediate DC bus voltage is significantly reduced, which allows the rest of the converter to be "better-designed" so that the input current is less distorted than is the case for boost-based single-stage converters.

Just as converters with voltage step-up/step-down capability can be used advantageously for single-stage converters that must be available to operate with a very wide range of line conditions (85 -265 V_{rms}), so too can inverters with such capability be used for applications that require DC to AC conversion for a wide range of operating conditions. Given the nature of such converters, however, the approaches that were suitable for the single-stage converters in Chapters 2 and 3 are not suitable for inverters, and therefore new approaches are required.

In this chapter, a new inverter that uses active clamp technology to step up and step down voltage is proposed. This chapter will begin by reviewing general active clamp theory, then introducing the new inverter and explaining its modes of operation. The chapter will explain the advantageous features of the new inverter compared to previously proposed inverters with voltage step-up/step down capability and will present experimental results that confirm the feasibility of the new inverter.

4.2 Review of Active Clamp Converters

An active clamp consists of a capacitor placed in series with an active switch. It is widely used in power converters as an auxiliary circuit that is attached parallel to their main power switches. The term "active clamp" is derived from the fact that the active clamp capacitor is used to clamp voltage spikes that are caused by the turning off of a converter's main power switches and the fact that an active clamp contains an active switch as opposed to containing purely passive elements. The use of active clamps is very popular in low power flyback and forward converters as a means to make the main power MOSFET switch of these converters turn on with zero-voltage switching (ZVS). In the case of forward converters, they also provide a means by which the power transformer can be reset without the use of a tertiary winding.

Active clamps are also popular in higher power converters with four or six main power switches such as voltage-fed DC/DC full-bridge converters (with bulk capacitor at the input of the full-bridge), current-fed DC/DC full-bridge converters (with bulk inductor at the input of the full-bridge), single-phase and three-phase voltage source inverters (VSIs), and single-phase and three-phase current source inverters (CSIs). As with lower power flyback and forward converters, an active clamp can be used in each of these converters to help the main power switches turn on with ZVS and to suppress voltage spikes that can be caused by the turning off of the main converter switches.

4.2.1 An Active-Clamped Voltage-Fed DC/DC Converter

Consider the converter shown in Fig. 4.1. It is a standard pulse-width modulated (PWM) DC/DC full-bridge converter, but with an active clamp circuit connected across its input and a small input inductor added between its input and the input DC source. The converter works as a standard PWM full-bridge converter with standard phase-shift control [45]-[46] except when the converter is about to exit a freewheeling mode of operation (the transformer primary voltage is zero, no energy transfer is taking place, and transformer primary current flows through either the top upper switches or the two lower switches) and enter an energy transfer mode (diagonally opposed bridge switches are on, voltage is impressed across the transformer primary, and energy is transferred from the

input to the output through the transformer). When the converter is about to exit a freewheeling mode, then the active clamp switch is turned on before any full-bridge switches are turned on.

Since the converter is designed so that energy from the input is placed in the active clamp capacitor sometime during the switching cycle, the voltage across the active clamp capacitor will be larger than the input voltage so that current begins to flow from the active clamp capacitor to the input. When the current through the input inductor rises to a sufficient level, the active clamp switch is turned off so that the output capacitance of the switch that is about to be turned on can be discharged by the transformer primary current and the input inductor. This switch can be turned on with zero-voltage switching (ZVS) as soon as current begins to flow through its body-diode.

The critical mode when the input inductor current generated by the turning off of the active clamp switch is used to discharge switch output capacitance is shown in Fig. 4.2; a more detailed explanation of the converter's ability to operate with ZVS can be found in [49]. It should be noted that the active clamp can be activated to help the leading leg switches of a PWM full-bridge converter turn on with ZVS as well as the lagging leg switches, which are the switches that are involved in switching transitions whenever the converter is about to exit a freewheeling mode of operation, as described above. Doing so, however, is generally not necessary as the reflected output inductor current is available to discharge the output capacitances of the leading leg switches whenever the converter is about to exit an energy-transfer mode and enter a freewheeling one.

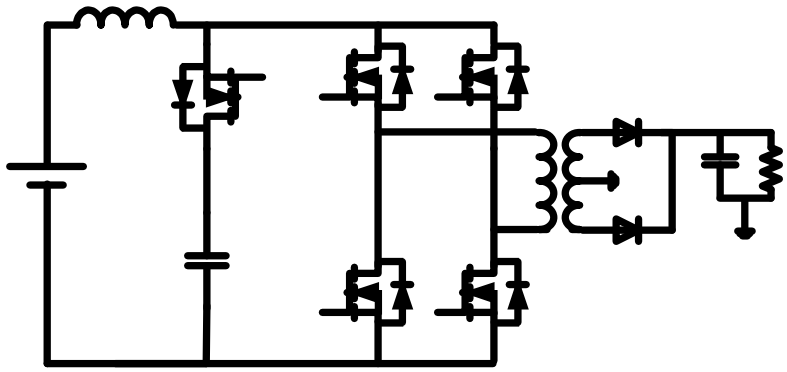


Fig. 4.1 DC/DC full-bridge converter with active clamp circuit

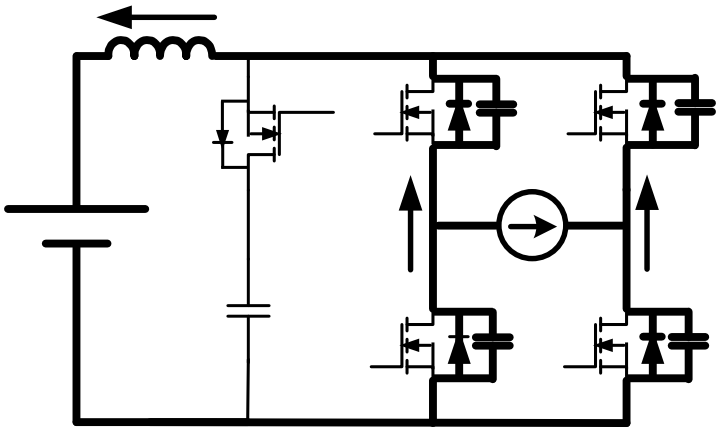


Fig. 4.2 Output capacitor discharge mode

4.2.2 An Active-Clamped Current-Fed DC/DC Converter

The input inductor of the converter shown in Fig. 4.1 must be fairly small in order to allow current to flow through both directions – towards the full-bridge, which is normal operation, and towards the input source, which is for ZVS operation, as shown in Fig. 4.2. If this inductor is made larger, then the converter can be made to operate like a current-fed DC/DC converter. The main full-bridge section can operate with either all four switches on (corresponding to the boost switch of a single-switch DC/DC boost converter being on) or with two diagonally opposed switches on (corresponding to the boost switch of a single-switch boost converter being off an input inductor current flowing through the output).

During the alternating sequence of the primary side DC bus being shorted then not-shorted, energy is placed into the active clamp capacitor during any switching transition when converter switches are turned off and the capacitor is allowed to discharge through the full-bridge whenever any pair of diagonally opposed switches is on. The active clamp switch is never on whenever the DC bus is shorted as this would result in shoot-through current in the full-bridge switches that can damage them. An example of a short-circuit mode of operation is shown in Fig. 4.3.

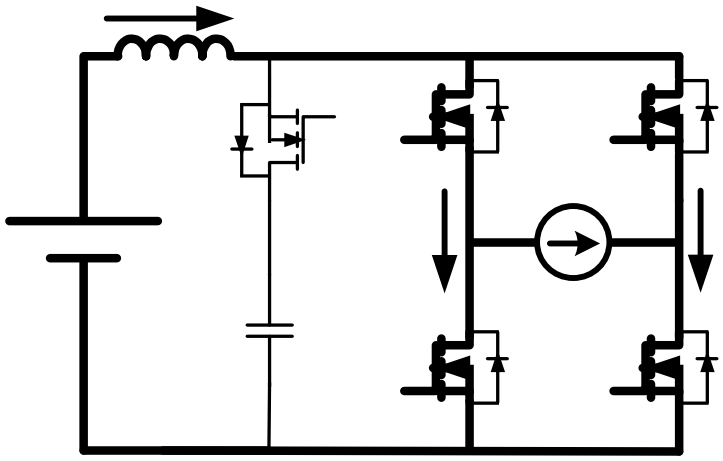


Fig. 4.3 Short-circuit mode of operation

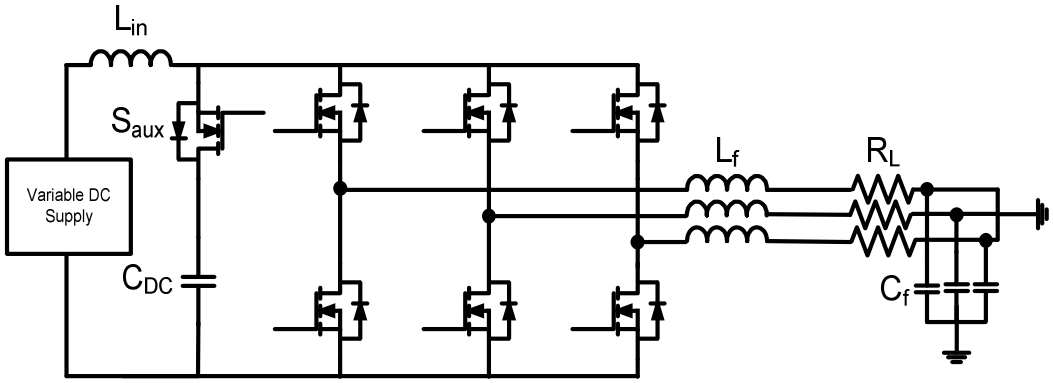
It should be noted that the switches in the current-fed PWM DC/DC converter can turn-on with ZVS due to the additional energy that is placed into the transformer primary when the active clamp switch is turned on. This additional energy, in the form of transformer primary current, can be used to discharge the output capacitances of switches that are about to be turned on so that they turn on with no voltage across them.

4.3. Extending the Range of Converter Operation with an Active Clamp

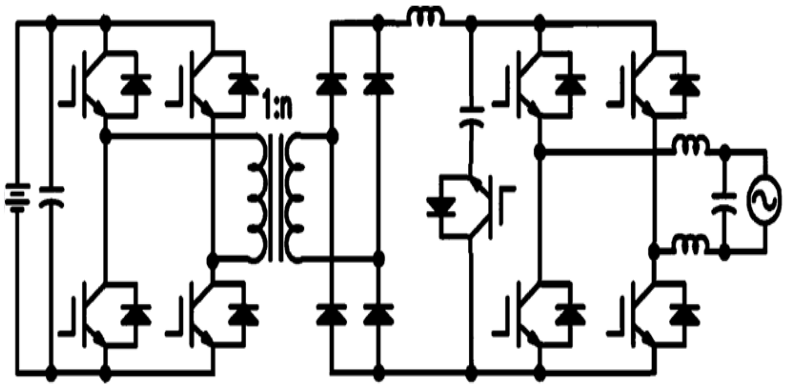
Thus far in this chapter, it has been explained that that the active clamp full-bridge topology shown in Fig. 4.1 can be operated as a voltage-fed PWM converter that can step-down voltage, or as a current-fed PWM converter than can step-up voltage. With this in mind, it is possible to design and operate an active clamp converter that can both step-up voltage and step-down voltage, depending on what is desired for particular operating conditions. Doing so is useful when it is considered that the converter, therefore, can operate with an extended operating range as it can step-down voltage whenever its input voltage is high and can step-up voltage whenever its input voltage is low. In other words, an active clamp converter can operate with an input voltage/output voltage ratio that a converter that can only step-down voltage and a converter that can only step-up voltage cannot.

The following should be noted:

- Although the discussion thus far in this chapter has focused on active clamp full-bridge converters, the concept of using an active clamp to extend converter operating range can be applied to other converters including single-phase inverter and three-phase inverters. For example, Fig. 4.4(a) shows an active clamp implemented in a three-phase inverter and Fig. 4.4(b) shows an active clamp implemented in a single-phase inverter that is embedded in a two-stage DC/DC/AC system.



a) Active clamp and 3-phase inverter



b) Active clamp in two stage inverter

Fig. 4.4. Active clamp in 3-phase and single phase inverters

- A converter with an active clamp can be operated in one of two ways when operating in step-down voltage mode. It can be operated as described in Section II of this letter and ZVS operation of the main converter switches can be achieved, or it can be operated with the active clamp switch always on, in which case the active clamp

capacitor forms a low pass input filter with the input inductor. The first way of operation can be used high switching frequency operation, preferably with low current as the input inductor must be small to allow the ZVS of the main converter switches to occur; the input inductor must be able to handle bidirectional current similar to what a bidirectional buck/boost ZVS-PWM converter must handle [50]-[51]. The second way can be used for low frequency operation where switching losses are of less concern. For the remainder of this chapter, the second way of operation will be assumed.

Examples of applications where it is beneficial for converters to operate with an extended operating range include the following:

- Converter that can step-up or step-down voltage can be very useful in alternative energy systems such as photovoltaic (PV) power systems, where converters need to be able to operate under a very wide range of input voltages. For example, a converter in a PV system can be designed so that it operates as a step-down converter under normal operation, but has the capability to step-up voltage if the voltage of the variable DC source (i.e. PV cells) goes less than an appropriate level. This step-up/step-down feature can be taken advantage of in converter for alternative energy applications to maximize the amount of generated energy that can be transferred to the load or grid.
- Many AC-DC converters are two-stage converters that consist of an AC-DC front-end converter followed by a DC/DC converter, which is typically a full-bridge converter. Such converters can have so-called hold-up requirements where the output voltage must continue to be regulated for a certain specified amount (the hold-up time) if the AC source voltage is unable. Being able to extend the operating range of a voltage-fed DC/DC converter that is the back-end converter of a two-stage AC-DC converter is possible if the converter is implemented with an active clamp and is able to step up voltage. In other words, a back-end full-bridge converter can operate like a voltage-fed converter under normal circumstances and like the current-fed converter described in Section III whenever the AC input is out and hold-up time capability is needed.

It should be noted that for the above two application example, the "normal" operation for the inverter is in step-down mode. It is only when the input voltage drops below a certain level that the inverter enters into step-up mode and the inverter returns into step-down when the input voltage is restored. Since there is a bulk capacitor at the input of the inverter, in the active clamp, the transition from step-up mode to step-down mode and vice versa is gradual as the voltage at the input of the inverter cannot suddenly change due to the bulk capacitor.

There have been several previously proposed converters that can step-down and step-up input voltage and some of these were reviewed in Chapter 1. These converters will be briefly reviewed again so that the features of the new active clamp based inverter can be better appreciated. Previously proposed converters with voltage step-up / step-down capability have at least one of the following drawbacks:

- Converters that are based on other basic converters that can step up and step down voltage, such as topologies that are based on buck-boost and Cuk converters [52]-[53], cannot operate as well as buck and boost-based converters. For example, there are numerous PWM schemes for buck-type inverters (VSIs) and boost-type inverters (CSIs), which are the two standard inverter topologies. An inverter with an active clamp can operate like a VSI when it is stepping down voltage and like a CSI when it is stepping up voltage. Buck-boost and Cuk based inverters need to operate with non-standard and exotic PWM scheme and cannot operate with standard PWM schemes, which offer better performance. The proposed converter can operate with such standard schemes.
- They are two-stage converters like the one shown in Fig. 4.5, which has a DC/DC boost converter followed by a VSI. Some of the weaknesses of this converter are (i) the boost switch and the boost diode must conduct the full input current, which places stress on these switches; (ii) there are significant conduction losses due to the fact that the full input current flows through the diode. Similar issues can be in the Cuk inverter/rectifier proposed in [54] where the full input current must flow through a Cuk converter switch and several capacitors. A converter with an active clamp for step-up/step-down operation does not have any series components that must conduct the full source current.

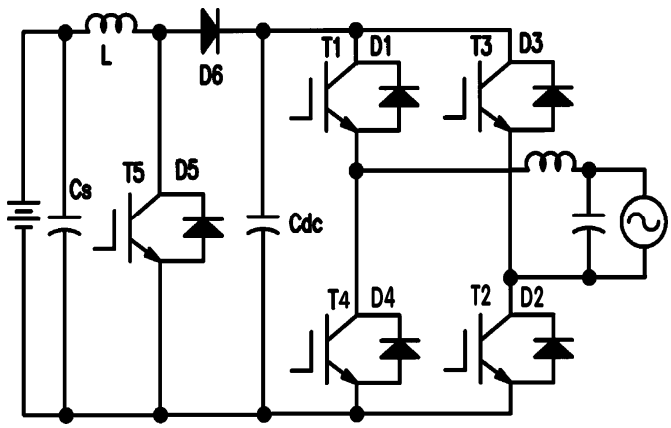


Fig. 4.5 Non isolated buck-boost inverters [59]

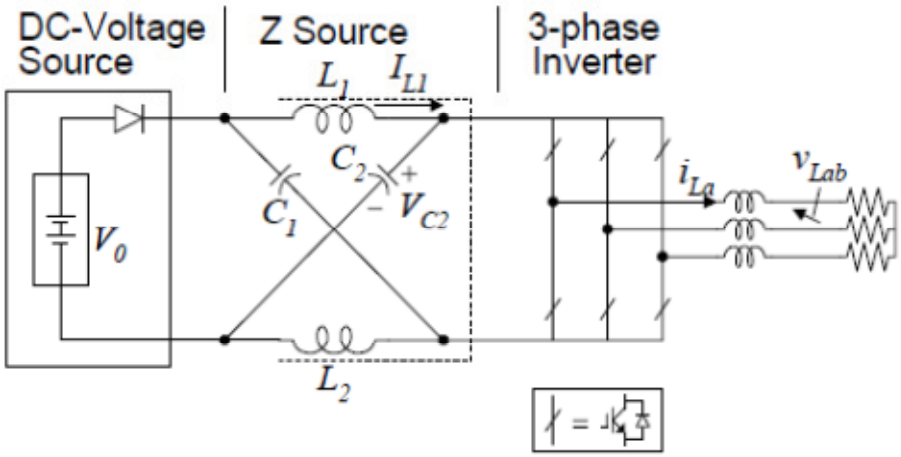


Fig. 4.6 Z-source inverter [38]

- They are so-called single-stage Z-source inverters [38]-[40], [55]-[56] like the basic Z-source inverter shown in Fig. 4.6, that can either step-up or step-down voltage, depending on whether the inverter operates with short-circuit states. The main drawbacks of Z-source inverters are (i) the passive element network is bulky; (ii) the input diode must conduct the full input current. The proposed converter has less passive components so that it is less bulky.
- When operating in boost mode, all the inverter switches in the proposed inverter can be turned on and current can be shared among these switches. This means that there is no switch that must conduct the full input inductor current, unlike most previously proposed converters. As a result, the current stress placed on the switches can be

reduced and if these switches are MOSFETs, then conduction losses can be reduced as well.

- In grid connected applications, the converter is capable of reactive power injection to the grid, unlike converter like a z-source inverter where there is no capacitor that is directly connected across the inverter. When the auxiliary switch is set to be always on, the inverter can be made to operate as a STATCOM [57].

4.4 Proposed Active Clamp Inverter

As an example of an active clamp converter with step-up/step-down voltage capability, the inverter shown in Fig. 4.4(a) is briefly discussed in this section and its feasibility is confirmed with results obtained from an experimental prototype.

The inverter shown in Fig. 4.4(a) is like a conventional VSI with an input LC filter between the variable DC source and the inverter, but with one difference – an auxiliary switch is placed between the DC bus capacitor and the DC bus. The way the converter works is as follows: When the converter is operating in step-down voltage mode, the auxiliary switch is always on and the converter operates exactly the same as a conventional VSI. When the converter is operating in step-up voltage mode, the auxiliary switch is turned off whenever the DC bus is shorted by turning on all six inverter switches so that the full input voltage is placed across the input inductor; this increases the amount of energy that can be placed in this inductor, which also increases the amount of energy that can be transferred to the output and the converter's voltage gain. It should be noted than the inverter can be a stand-alone inverter, as shown in Fig. 4.4(a) or a grid connected one, as shown in Fig. 4.7.

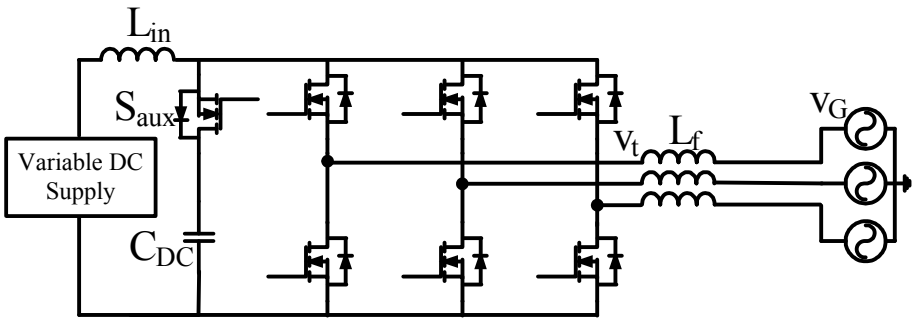


Fig. 4.7 Proposed inverter in grid-connected mode

It can be used in low power applications as a micro inverter or in higher power applications where a three-phase AC output is needed.

Fig. 4.8 shows the inverter's key modes of operation. In Fig. 4.8(a), the inverter is in the boost mode and all six bridge switches are on. In Figs. 4.8(b) and (c), the inverter is in an energy transfer mode. The only difference between Figs. 4.8(b) and 4.8(c) is the flow of energy in and out of the DC bus capacitor, which is dependent on instantaneous three-phase load voltage and the difference in current between that provided by the source and that absorbed by the inverter. Fig. 4.8(d) shows the freewheeling mode of operation where current freewheels in the inverter.

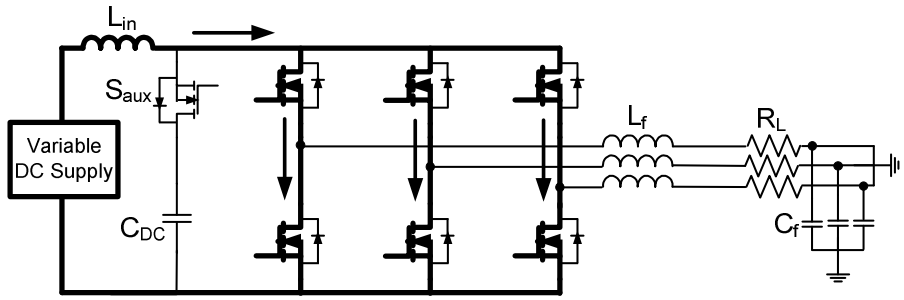
4.5 Experimental Results

A simple proof-of-concept three-phase inverter laboratory prototype was built to confirm the feasibility of the step-up/step-down active clamp technique. Its components and specifications were as follows: L_{in} = 2 mH, C_{DC} = 400 μF, L_f = 2 mH, C_f = 1.5 μF. P_o = 500 W, input DC voltage: 180 – 340, DC bus voltage: 310V, output AC line voltage V_o = 120 $V_{rms.}$

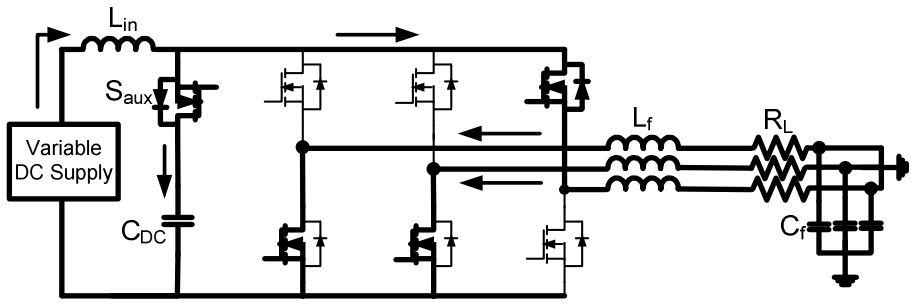
Fig. 4.9 shows the output voltage, output current and DC bus voltage of the inverter when the inverter is working in voltage step-down or VSI mode and Fig. 4.10 shows the gating signals of two upper and lower switches of the inverter in this mode. The auxiliary switch was always on in this mode (making the converter like a regular VSI with an LC input filter) and regular SPWM was used as the PWM pattern. The inverter was operated in the exact same manner as a conventional three-phase VSI.

Fig. 4.11 shows the output voltage, output current and DC source voltage of the inverter when the inverter is working in voltage step-up or CSI mode and Fig. 4.12 shows gating signal patterns of the auxiliary switch and the two upper and lower switches of the inverter in this mode. As can be seen from Fig. 4.12, the gating signal of the auxiliary switch is synchronized to those of the inverter switches so that this switch is off whenever both upper and lower switches are on. It should be noted that standard SPWM for CSIs was used as the PWM method for CSI operation [58].

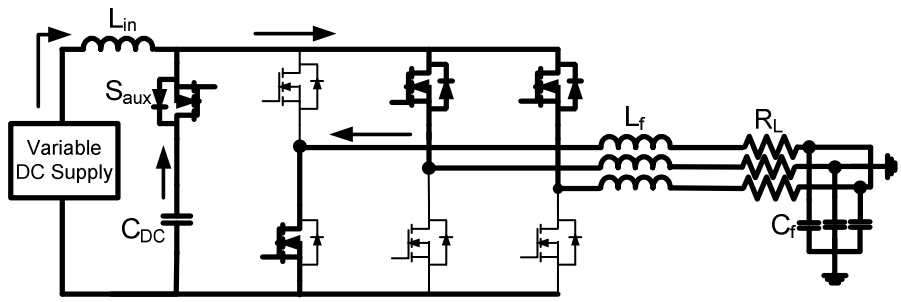
In both cases, the DC bus capacitor voltage is about 320V_{DC}.



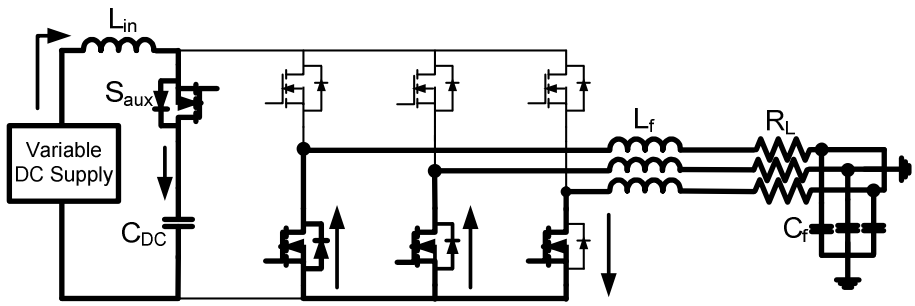
(a) Boost



(b) Energy transfer



(c)Energy transfer



(d) Freewheeling

Fig. 4.8 Modes of operation

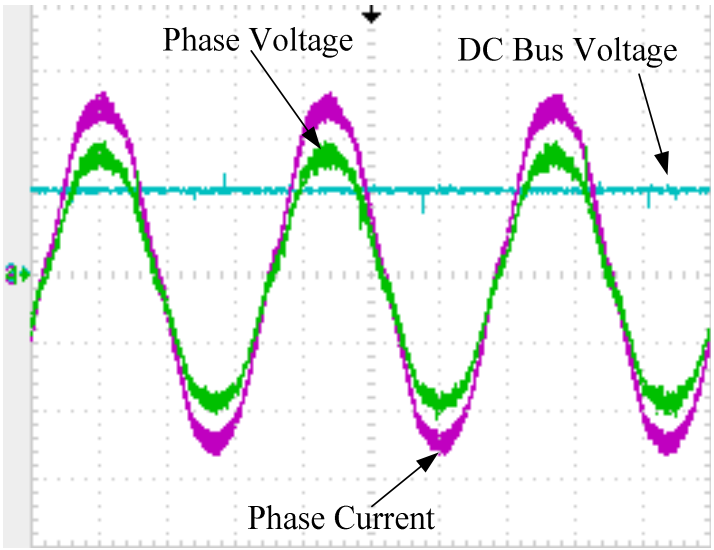


Fig. 4.9 VSI output voltage, output current and DC bus voltage waveforms

(v_{ac} 100v/div, i_{ac} 1A/div, v_{dc} 250/div, t = 10ms/div.)

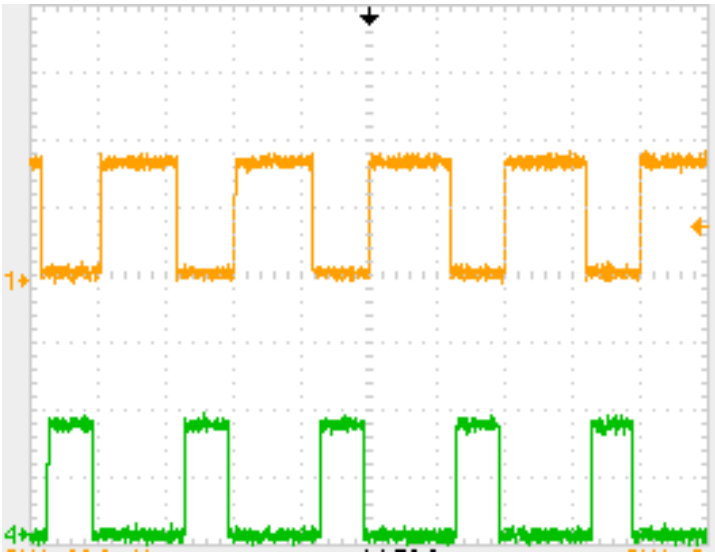


Fig. 4.10 VSI PWM pattern

Upper signal: Upper switch gate signal, Lower signal: Lower switch gate signal (10V/div, t = 25μs/div)

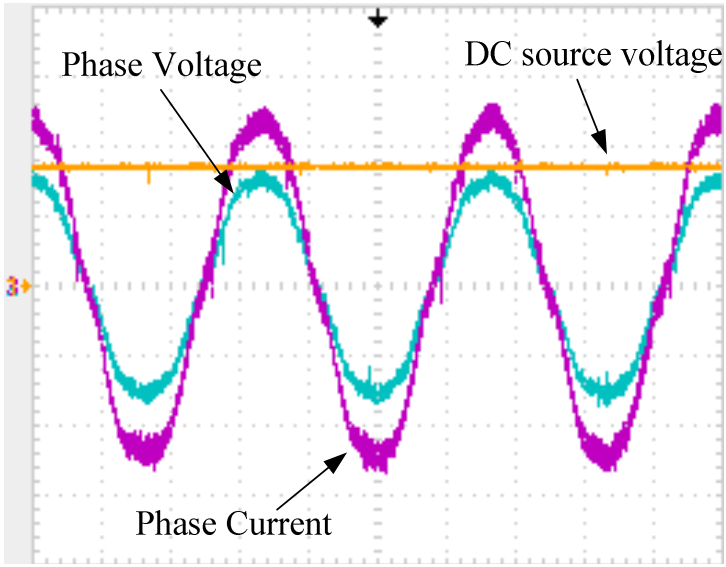


Fig. 4.11 CSI output voltage, output current and input DC source voltage waveforms

(v_{ac} 100v/div, i_{ac} 1A/div, v_{dc} 100v/div, t = 10ms/div)

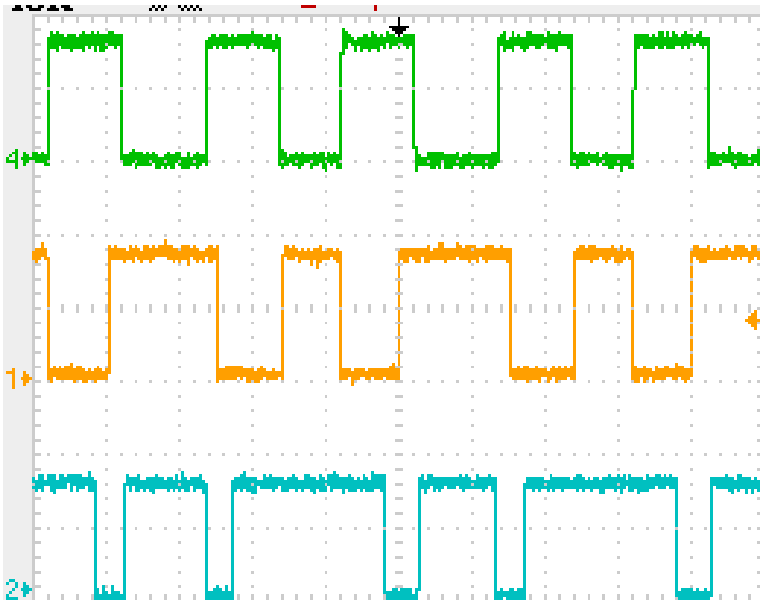


Fig. 4.12 CSI PWM pattern

Upper signal: Aux. switch gate signal, Middle signal: Upper switch gate signal, Lower signal: Lower switch gate signal (V: 10V/div, t = 25µs/div)

4.6 Conclusion

In this chapter, a new technique that can be used to extend the operating range of a three-phase inverter was proposed. Although the technique is novel, it is based on established principles related to well-known active-clamp converters. It was shown that some converters with active clamps can step down voltage while others can step up voltage and that it is possible to derive active clamp converters that can do both.

Active clamp converters with step-down/step-up capability can operate in various modes (i.e. with ZVS and without). For this chapter, emphasis was placed on operating active clamp converters in step-down mode with step-up mode operation occurring only when the inverter input voltage (active-clamp capacitor voltage) has dropped below an appropriate value. With this type of operation, the active clamp switch is always on when the inverter is in step-down mode so that the converter's equivalent circuit is like a standard VSI or full-bridge converter with an input LC filter.

The later part of the chapter examined how the proposed active clamp technique can be implemented in an inverter. The inverter can be used as a stand-alone converter or as part of an overall converter system. The advantageous features of the inverter are that it has identical characteristics as a conventional voltage-source inverter when it is in step-down mode, it can be implemented with standard PWM techniques for VSI and CSI, none of its components carry the full input inductor current when it is in step-up mode, and it is capable of injecting reactive power to the grid. The operation of the inverter with the proposed active clamp technique was confirmed with results obtained from a simple proof-of-concept prototype converter.

Chapter 5

Control of the Proposed Voltage Step-Up/Step-Down Inverter

5.1. Introduction

In this chapter, the control of the inverter that was proposed in the previous chapter will be investigated. There are two key control issues that need to be examined. The first is the control of the AC side of the converter to ensure that sinusoidal output waveforms are produced and that the DC bus capacitor voltage that the six-switch bridge see is fixed. It will be assumed in this chapter that the output of the inverter is being fed to the grid. The second key issue that needs to be examined is the current that is fed from the PV panels to the inverter. The ripple on this current must be minimized as much as possible so that the inverter can be implemented with maximum power point tracking techniques (MPPT) that will enable it to extract the maximum power that is available from the PV panels at any given time.

This chapter will begin by briefly reviewing voltage mode and current mode control methods for the AC output waveforms of the three-phase inverter and it will be explained why current mode control is preferred. Based on current mode theory and on conventional three-phase frame to two-axis frame transformation theory, a model will be developed that will be used to investigate the control of the AC output of the proposed inverter and the DC bus capacitor voltage. Once this is done, the control of the DC side current will be investigated. It will be shown how the ripple of this current can be minimized so that the proposed inverter can be implemented with MPPT techniques, if desired. The control of the inverter AC output and DC input will be developed and implemented in computer simulation. The results of computer simulations will be used to confirm the feasibility of the control techniques developed in this chapter.

5.2. Control of Inverter AC Output

This chapter is divided into three sections. This section will discuss the control of the inverter AC output, Section 5.3 will discuss the control of the inverter DC input, and

Section 5.4 will discuss various case studies that will be implemented in simulation and will present key results from various simulations.

5.2.1 General Control Methods of Voltage Source Inverters (VSIs) in Grid-Connected Applications

Fig. 5.1 shows a block diagram of a conventional inverter system fed by solar panels. This system typically consists of a voltage-source inverter that converts the dc voltage obtained from the solar panels into an AC output, output inductors that filter out undesirable AC harmonics at non-fundamental frequencies that are caused by the switching of the inverter devices, and a controller that accepts signals that are sensed from the solar panel output and the grid voltage and produces signals to turn the inverter devices on and off at appropriate times. The inverter output can be controlled using voltage-mode control, which is a typical control method for high power voltage-source inverters (VSIs) and inverter-based flexible AC transmissions system (FACTS) devices. With voltage mode control, if the phase angle and the amplitude of the VSI's output, V_t, is made to be the same as the phase angle and the amplitude of the grid voltage, V_G, then the active and reactive power produced by this control method can be controlled independently [59]. Voltage mode control, however, does not provide over-current control naturally and thus must be implemented with some additional protection scheme to deal with severe faults that can be dangerous.

Current-mode control is another well-known control method that is used in grid-connected inverters. A block diagram of a typical current-mode control scheme is shown in Fig. 5.2. In this method, the grid side current is measured and is fed to the input of the controller and the controller fixes the current at the AC terminal; the terminal voltage amplitude and the phase angle are defined by the result. This method has two advantages over the voltage control method: The first is that active and reactive power with respect to the grid voltage can be controlled independently of each other by controlling the output current of the converter; active and reactive power control is more flexible in this approach. The second is that current mode control has inherent current protection so that

if any fault occurs at the grid side of the inverter, the inverter will be automatically protected by the control scheme.

Since current-mode control has these advantages over voltage-mode, it was selected as the control scheme for the proposed inverter. In order to develop a procedure for the design of the controller, its characteristics must be determined first by mathematical analysis. This analysis is presented in the next sections of this chapter.

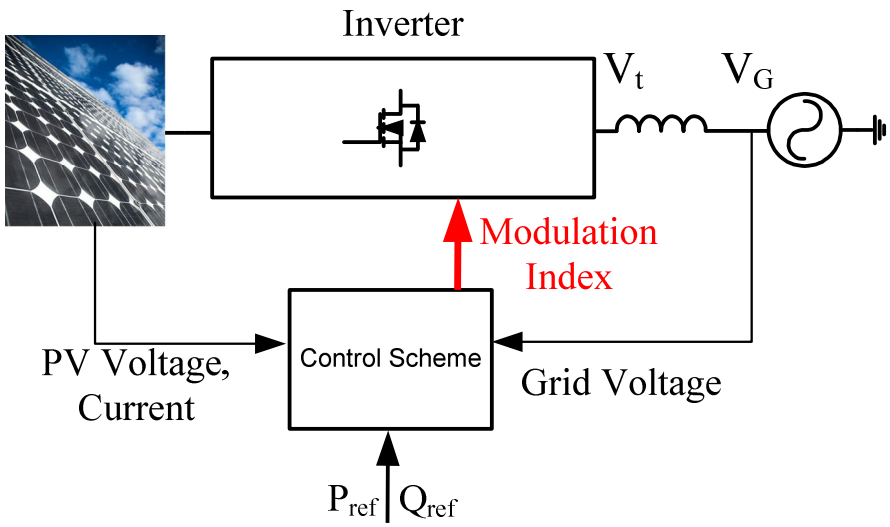


Fig. 5.1 Voltage-mode control of the grid-connected inverter

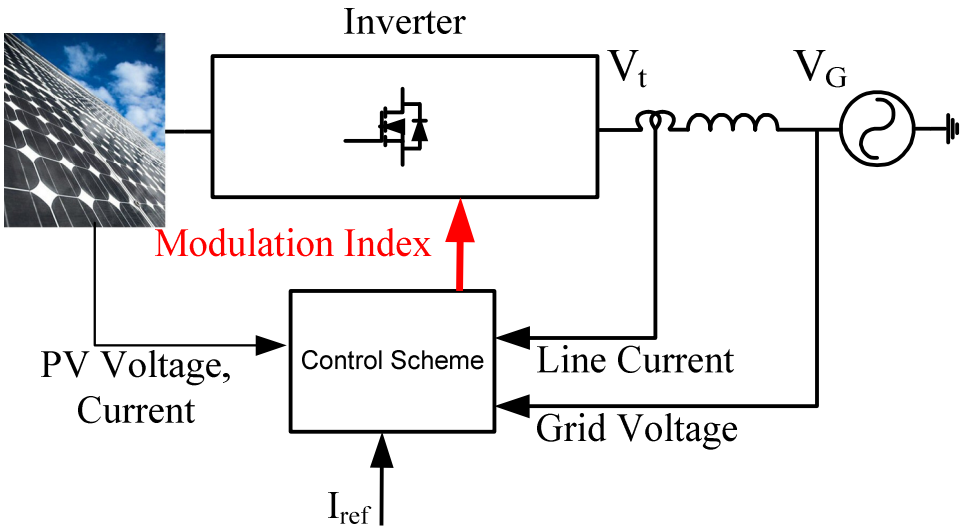


Fig. 5.2: Current-mode control of the grid-connected inverter

5.2.2 Realization of Power in the αβ-Frame

Three-phase systems operate in real-time in the so-called abc frame where the three time-varying input phase voltages must be considered. It is very difficult to analyze, model and design a controller for such systems because the parameters are in a sinusoidal time frame that makes necessary the design of a separate multi-input/multi-output controller for active and reactive power for each phase, which requires a multi input – multi output controller. In order to avoid such complexity, researchers have defined other frames that are simpler to use than the abc-frame. One such frame is the αβ-frame which is a time-varying two-dimensional space. Parameters from the abc-frame can be converted to new parameters in the αβ-frame by applying a mathematical transformation. In this section, the parameters that are considered are ones associated with active and reactive power.

Consider a balanced three phase sinusoidal abc-frame system. Its phases are the three phase voltages, $f_a(t)$, $f_b(t)$ and $f_c(t)$, and each phase has a 120 degree phase difference with respect to the other phases; each phase has the same angular frequency. A space phasor that is suitable for the two-dimensional time-varying αβ-frame can be defined as

$$\vec{f}(t) = \frac{2}{3}\left[e^{j0} f_a(t) + e^{j\frac{2\pi}{3}} f_b(t) + e^{j\frac{4\pi}{3}} f_c(t)\right] \tag{5.1}$$

with

$$f_a(t) + f_b(t) + f_c(t) = 0 \tag{5.2}$$

for a balanced three-phase system. $\vec{f}(t)$ can be separated into one real and one imaginary components, with each component corresponding to an axis of the αβ-frame

$$\vec{f}(t) = f_\alpha(t) + j f_\beta(t) \tag{5.3}$$

where f_α and f_β are α and β axis components of αβ-frame respectively. Taking (5.1) and expanding it so that its real and imaginary components can be determined, the relation between abc-frame parameters and αβ-frame parameters can be established as follows:

$$\begin{bmatrix} f_\alpha(t) \\ f_\beta(t) \end{bmatrix} = \frac{2}{3} C \begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \tag{5.4}$$

where

$$C = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{5.5}$$

With this transformation from abc-frame parameters to αβ-frame parameters established, the next step is to consider the transformation of power from the abc-frame to the αβ-frame. In a three-phase balanced network ($i_a(t) + i_b(t) + i_c(t) = 0$) , the instantaneous real power in the time domain (abc-frame) can be expressed as

$$P(t) = v_a(t)i_a(t) + v_b(t)i_b(t) + v_c(t)i_c(t) \tag{5.6}$$

where $v_a(t)$, $v_b(t)$ and $v_c(t)$ are the individual phase voltages and ia(t), ib(t) and i(c) are the corresponding phase currents. If the voltages and currents in (5.6) are replaced by their corresponding space vectors, then the result is as follows:

$$\begin{aligned} P(t) = {} & Re\{\vec{v}(t)e^{j0}\}Re\{\vec{i}(t)e^{j0}\} + Re\left\{\vec{v}(t)e^{-j\frac{2\pi}{3}}\right\}Re\left\{\vec{i}(t)e^{-j\frac{2\pi}{3}}\right\} \\ & + Re\{\vec{v}(t)e^{-j\frac{4\pi}{3}}\}Re\{\vec{i}(t)e^{-j\frac{4\pi}{3}}\} \end{aligned} \tag{5.7}$$

This result is due to the fact that in (1), $f_a(t)$, $f_b(t)$, and $f_c(t)$ can be retrieved from the corresponding space phasor, based on the following equations:

$$f_a(t) = Re\{\vec{f}(t)e^{-j0}\} \tag{5.8a}$$

$$f_b(t) = Re\left\{\vec{f}(t)e^{-j\frac{2\pi}{3}}\right\} \tag{5.8b}$$

$$f_c(t) = Re\left\{\vec{f}(t)e^{-j\frac{4\pi}{3}}\right\} \tag{5.8c}$$

Based on the fact that $Re\{x\}Re\{y\} = (Re\{xy\} + Re\{xy^*\})/2$, the instantaneous real power is equal to

$$P(t) = Re\left\{\frac{3}{2}\vec{v}(t)\vec{i}(t)^*\right\} \tag{5.8}$$

and instantaneous reactive power is

$$Q(t) = Im\left\{\frac{3}{2}\vec{v}(t)\vec{i}(t)^*\right\} \tag{5.9}$$

Equations (5.8) and (5.9) are similar to the traditional active and reactive power equations, which are

$$P(t) = vi\cos(\varphi) \tag{5.10}$$

$$Q(t) = vi\sin(\varphi) \tag{5.11}$$

where v is phase voltage, i is phase current and φ is the phase difference between v and i. Equations (5.10) and (5.11) are valid only for ideal three-phase systems where the voltages and currents are purely sinusoidal.

Equations (5.8) and (5.9), $\vec{v}(t)$ and $\vec{i}(t)$ can be substituted by their αβ-frame components so that substituting $\vec{v}(t)$ and $\vec{i}(t)$ by $v_\alpha + jv_\beta$ and $i_\alpha + ji_\beta$ respectively gives

$$P(t) = \frac{3}{2}[v_\alpha(t)i_\alpha(t) + v_\beta(t)i_\beta(t)] \tag{5.12}$$

$$Q(t) = \frac{3}{2}[-v_\alpha(t)i_\beta(t) + v_\beta(t)i_\alpha(t)] \tag{5.13}$$

5.2.3 Realization of Power in the dq-Frame

Equations (5.12) and (5.13) were derived for the active (P) and reactive (Q) power in the αβ-frame. Although a transformation from a three-dimensional space to a simpler two-dimensional space was achieved, there are several considerations that need to be taken into account. One is (5.12) and (5.13) are not decoupled so that a change in a parameter in one of these equations affects the other equation, making the independent control of P and Q impossible. Another is that the αβ-frame is still a time-varying frame, which makes the design of a controller challenging. As a result, there needs to be another transformation, but this time from a two-dimensional time-

varying frame to a two-dimensional stationary frame, which can be called the dq-frame. Transforming parameters from the αβ-frame to the dq-frame results in DC values that are more easily controllable.

The relation between αβ-frame and dq-frame parameters can written as [60]

$$\vec{f}(t) = f_\alpha + jf_\beta = \hat{f}e^{j(\theta_0 + \int \omega(\tau)d\tau)} \tag{5.14}$$

where $\omega(\tau)$ is the time-varying frequency and is equal to the grid voltage frequency, θ_0 is the initial phase angle of the three-phase signal corresponding to the αβ-frame, $\hat{f}$ is the space phasor amplitude, and τ is an integral variable. The transformation from αβ-frame to dq-frame can be defined as [60]

$$f_d + jf_q = (f_\alpha + jf_\beta)e^{-j\epsilon(t)} \tag{5.15}$$

where–ε(t) is defined as the phase difference between the αβ-frame and the dq-frame. Based on this equation, the transformation from αβ-frame to dq-frame can be expressed as

$$\begin{bmatrix} f_d(t) \\ f_q(t) \end{bmatrix} = R[\varepsilon(t)] \begin{bmatrix} f_\alpha(t) \\ f_\beta(t) \end{bmatrix} \tag{5.17}$$

where

$$R[\varepsilon(t)] = \begin{bmatrix} \cos\varepsilon(t) & \sin\varepsilon(t) \\ -\sin\varepsilon(t) & \cos\varepsilon(t) \end{bmatrix} \tag{5.18}$$

If ε(t) is chosen as $\varepsilon_0 + \int \omega(\tau)d\tau$, then the dq-frame can be expressed as

$$f_d + jf_q = \hat{f}e^{j(\theta_0 - \varepsilon_0)} \tag{5.16}$$

As can be seen from (5.16), the dq-frame is stationary because there are no time-varying parameters so that the design of a controller can be simplified considerably as only DC values need to be considered.

By considering voltage and current in the dq-frame as $\vec{v}(t) = \left(v_d + jv_q\right)e^{j\epsilon(t)}$ and $\vec{\imath}^*(t) = \left(i_d - ji_q\right)e^{-j\epsilon(t)}$ respectively, active and reactive power can be defined as follows:

$$P(t) = \frac{3}{2}\left[v_d(t)i_d(t) + v_q(t)i_q(t)\right] \tag{5.19}$$

$$Q(t) = \frac{3}{2}\left[-v_d(t)i_q(t) + v_q(t)i_d(t)\right] \tag{5.20}$$

Based on these equations, both P and Q will be independently controllable by i_d and i_q respectively if v_q=0.

The equations that have been derived so far in this chapter are general equations for abc-frame to αβ-frame and αβ-frame to dq-frame transformations. Considering specifically the grid voltage ($v_G(t)$ in Fig. 5.2), the active and reactive power going into the grid can be determined by transforming this voltage from the abc-frame to the dq-frame then considering (5.19) and (5.20). If the q-component of the grid voltage is zero, then active and reactive power can be controlled independently of each other.

$v_G(t)$ in Fig. 5.2 can be divided into the following two dq-frame components:

$$v_G^d = \hat{v}_G \cos(\omega_0 t + \theta_0 - \rho) \tag{5.21}$$

$$v_G^q = \hat{v}_G \sin(\omega_0 t + \theta_0 - \rho) \tag{5.22}$$

where $\hat{v}_G$ is the peak value of the line to neutral voltage of the grid, ω_0 is the angular rotational speed of the grid voltage, θ_0 is the initial phase angle of the three-phase signal corresponding to the αβ-frame, and ρ is the phase-shift angle by which the equations are transferred from the αβ-frame to the dq-frame. Considering (5.22), if ρ can be adjusted so that it is always equal to $\omega_0 t + \theta_0$, then v_G^q will be zero. According to (5.19) and (5.20), the active and reactive power injected to the grid in Fig. 5.2 can be controlled by adjusting i_d and i_q respectively.

This control can be implemented with a Phase Locked Loop (PLL), as shown in Fig. 5.3. The input parameter to this control system is the grid voltage angle and the PLL defines its output in such a way that it follows the grid angle with minimum error. Parameter ρ can therefore be adjusted so that it is always equal to $\omega_0 t + \theta_0$, which makes

v_G^q will be zero. As the result, active and reactive power injected to the grid can be controlled independently, according to (5.19) and (5.20).

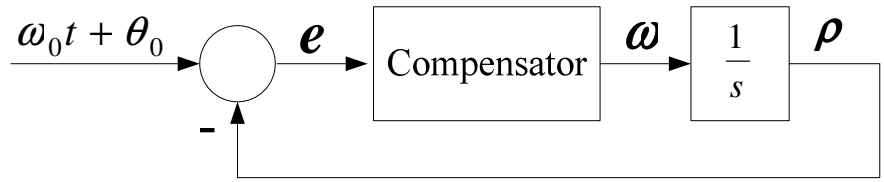


Fig. 5.3 Control diagram of a PLL

5.2.4 Dynamics of a Single-Stage Grid-Connected Inverter

In the previous section, it was shown how active and reactive power injected into the grid can be controlled independently by considering the three-phase AC output in a two-axis dq frame and controlling the q-axis parameter so that it is zero. With this in mind, the next step of the investigation is to determine how output inductor current can be controlled to achieve this active power / reactive power decoupling. Since output inductor current can be controlled by controlling the operation of the inverter, this section will examine appropriate inverter control methods. It will be assumed that the converter switches and the output inductors are lossless.

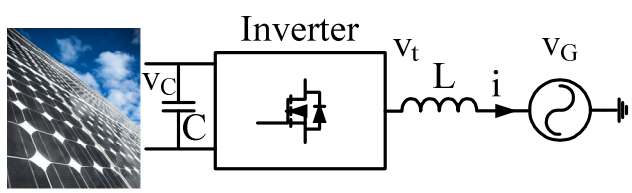


Fig. 5.4 Single-stage grid-connected inverter

Consider the following equation, which relates the output inductor current to the difference between the inverter output voltage and the grid voltage which has been shown in Fig 5.4:

$$L\frac{d}{dt}\vec{\imath} = \vec{v}_t - \vec{v}_G \tag{5.23}$$

where $\vec{v}_t = \hat{v}_t e^{j(\theta_0 + \int \omega(\tau) d\tau)}$, $\vec{v}_G = \hat{v}_G e^{j(\theta_0 + \int \omega(\tau) d\tau)}$ and $\vec{\imath} = \hat{\imath} e^{j(\theta_0 + \int \omega(\tau) d\tau)}$. This equation is an expression in the αβ-frame. If the αβ-frame to dq-frame transformation is used, which has been explained in Section 5.2.3, then (5.23) can be expressed in the dq-frame as

$$L \frac{d}{dt} i_{dq} e^{j\rho} = v_t^{dq} e^{j\rho} - \hat{v}_G e^{j(\omega_0 t + \theta_0)} \tag{5.24}$$

Eq. (5.24) can be expanded then decomposed into real and imaginary axes as follows

$$L \frac{di_d}{dt} = L \frac{d\rho}{dt} i_q - v_t^d - \hat{v}_G \cos(\omega_0 t + \theta_0 - \rho) \tag{5.25}$$

$$L \frac{di_q}{dt} = -L \frac{d\rho}{dt} i_d - v_t^q - \hat{v}_G \sin(\omega_0 t + \theta_0 - \rho) \tag{5.26}$$

with the angular rotational speed of the grid voltage ω defined as

$$\omega = \frac{d\rho}{dt} \tag{5.27}$$

Since a PLL can track ω, then $\hat{v}_G \sin(\omega_0 t + \theta_0 - \rho)$ will be equal to zero, according to Fig. 5.3. Considering (5.21) and (5.22), equations (5.25) and (5.26) can be re-written as

$$L \frac{di_d}{dt} = L\omega i_q - v_t^d - v_G^d \tag{5.28}$$

$$L \frac{di_q}{dt} = -L\omega i_d - v_t^q \tag{5.29}$$

which represent the amount of instantaneous power injected to the grid as this is dependent on output inductor current since the grid voltage is fixed.

The energy that is injected to grid is dependent on the DC bus capacitor at the inverter input as it is this capacitor that stores the energy from the solar panels. It is desirable to minimize the ripple of the voltage across this capacitor to minimize the ripple that may be transferred to the AC side and appear in the output inductor current so that this voltage must be controlled in some way. Consider the following equation, which relates DC bus capacitor voltage to the difference in instantaneous power between the output of the solar panels and the input of the inverter

$$Cv_c\frac{dv_c}{dt} = p_{in} - p_{out} \tag{5.30}$$

where p_{out} is the instantaneous output power of the inverter and p_{in} is output power of the solar cell, as shown in Fig. 5.5.

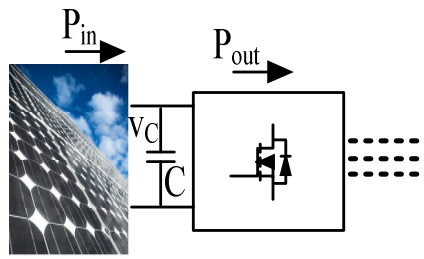


Fig. 5.5 Power balance at the DC bus capacitor

p_{out} can be written as

$$p_{out} = \frac{3}{2}v_G^d i_d \tag{5.31}$$

since p_{out} is the same as the active power that is injected into the grid, as was determined from (5.19) with $v_q(t) = 0$. Since the inverter and the output inductor in each phase is assumed to be lossless, the power to the inverter is equal to power transferred to the grid so (30) can be written as

$$Cv_c\frac{dv_c}{dt} = p_{in} - \frac{3}{2}v_G^d i_d \tag{5.32}$$

Equations (5.28), (5.29) and (5.32) show the relations between DC bus capacitor voltage, AC output inductor current and power transferred to the grid. With these equations, the design of an appropriate controller for the VSI can be considered and the system can be represented as a multivariable nonlinear system in a state space format with state-space parameters

$$x = [i_d \quad i_q \quad v_c] \tag{5.35}$$

In order to represent the equations in a state-space format, v_t^d and v_t^q, which represent the terminal voltage of the inverter in the dq-frame, should be related to the DC capacitor voltage. This can be done as follows [60]:

$$v_t^d = v_c u_d \tag{5.33}$$

$$v_t^q = v_c u_q \tag{5.34}$$

where u_d and u_q are control signals that are coming from the appropriate control system. Equations (5.35), (5.28), (5.29) and (5.32) can be combined with (5.33) and (5.34) to obtain the following result, which is in state-space format:

$$\begin{cases} \dot{x}_1 = \omega x_2 - \frac{1}{L} x_3 u_d - \frac{1}{L} v_G^d \\ \dot{x}_2 = -L\omega - x_3 u_d \\ \dot{x}_3 = \dfrac{p_{in}(x) - \frac{3}{2} v_G^d x_1}{c x_3} \end{cases} \tag{5.36}$$

where $P_{in}(x)$, the power that is coming from the input DC source, is generally a nonlinear function of the state variables. Fig. 5.6 shows the inverter and control system block diagrams for three defined state variables, based on (5.36)

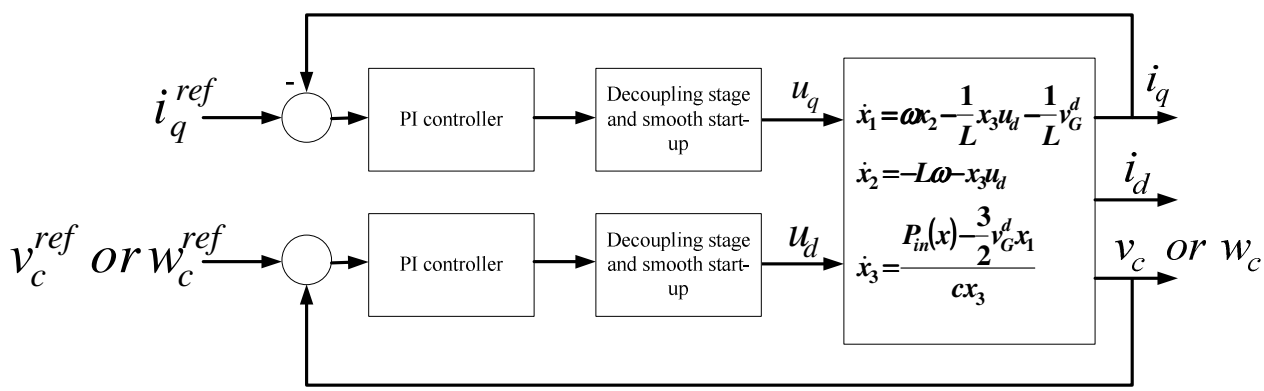


Fig. 5.6 Control loops of grid-connected current control VSI

As the block diagram shows, two separate controllers are required to control i_q and v_c (w_c). i_q^{ref} should be fixed to zero to minimize the amount of reactive power injected to the grid. v_c^{ref} or w_c^{ref} should be fixed to a predefined reference value to keep the DC capacitor voltage fixed to a certain level. In this way, whatever energy is coming from PV goes automatically to the grid as the voltage (or energy) of the DC capacitor is kept

constant by the controller. What this means is that any extra energy that is fed to the capacitor flows through the inverter and output filter to the grid.

5.3 Control of Inverter DC Input

With the control scheme discussed in the previous section, the DC capacitor voltage can be made to be fixed. With such a fixed voltage, the next step in developing an overall control scheme for the PV system is to consider the input section, which includes the PV panel output voltage and the input to the inverter. The focus of this section, will be on how maximum power can be extracted from the PV panels and on how the ripple or fluctuations of the current flowing out of these panels can be minimized to ensure maximum power extraction techniques can be properly implemented.

5.3.1 Maximum Power Point Tracker Techniques

Maximum power point tracker (MPPT) techniques are used to ensure that the maximum available energy at the PV side is sent to the grid or load side. Such techniques are needed as the current vs. voltage and the power vs. voltage characteristics of a PV cell are highly nonlinear, as can be seen in Fig. 5.7. These characteristics are dependent on climate conditions as PV current is dependent on sunlight intensity and PV voltage is dependent on temperature. It can be seen in Fig. 5.7 that there is a maximum power point on the P-V curve; the main objective of any MPPT algorithm is to ensure converter operation at this operating point.

There are several different methods for controlling the maximum power of the system. The most well-known methods are “Curve-Fitting Technique”, “Perturb and Observe”, “Incremental Conductance” and “Hill-Climbing” [61]. Each algorithm has its advantages and disadvantages. Since PV panels are usually installed in arrays or in matrix format, the power curve of the resulting PV system consists of a several local maximum power points. The MPPT algorithm should be able to reject all of these operating points except for the point that is the maximum point for the overall system and not be fooled by local maximum points.

5.3.2 Comparison Between Single-Stage and Double-Stage PV Inverters in terms of MPPT techniques

The interface between the PV panels and the grid can be implemented with either a single-stage or a two-stage structure. A single-stage structure uses single inverter to interface the PV panels with the grid while a two-stage structure either uses two separate power electronic converters or has some active components between an inverter and the PV panels.

In a single-stage voltage source inverter (VSI), a maximum power point (MPP) can be obtained by monitoring the instantaneous power that is delivered to the grid and by varying the DC bus voltage level [62]. For example, Vmp is the PV panel voltage at which a MPP can be obtained in Fig. 5.7. If an MPPT algorithm is implemented in a PV system with PV panels having this characteristic, the MPPT algorithm should monitor the active power that is injected to the grid and adjust DC side voltage so that the PV panels operate with Vmp voltage. Referring to the control scheme shown in Fig. 5.6, a separate control system is needed to set v_c^{ref} or w_c^{ref} .

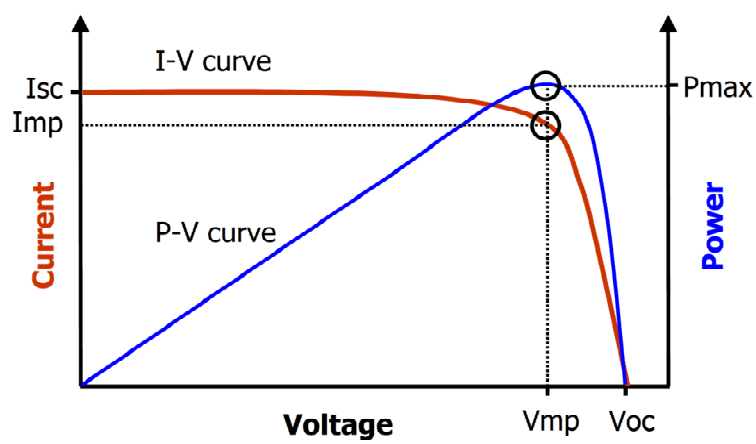


Fig. 5.7 Typical I-V and P-V of a PV panel

An MPPT technique with greater flexibility can be implemented in two-stage structures as two converter stages allow for more options than a single converter. The inverter proposed in the previous chapter, which is shown in Fig. 5.8 as being connected to the grid, can be considered to be a two-stage structure. This is because the DC bus switch, S_{aux}, can be used to control the input power to the VSI and the DC bus capacitor

voltage is controlled by the inverter. Since the inverter input parameters can be controlled, therefore, there is no need to change the amount of injected power to the grid to find the MPP and the MPPT algorithm can be implemented by considering only the DC side and the auxiliary converter switch.

Since the DC bus capacitor voltage is fixed by the inverter as shown in Fig. 5.6, the duty cycle of the auxiliary switch can be varied to adjust the DC voltage at the output of the PV panels so that the PV panels operate at the MPP. The output voltage and current of the PV panels should be as pure DC as possible to avoid oscillation that may deflect the operating point of the PV panels from the MPP and may create power oscillations at the gird as well.

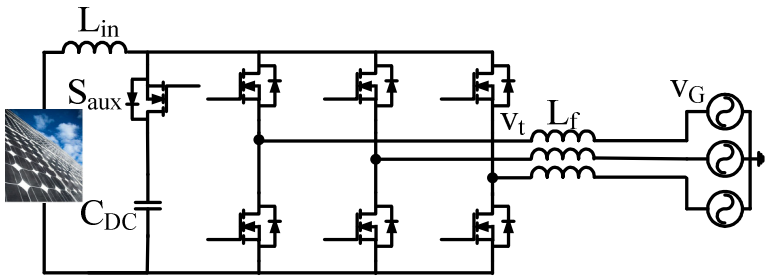


Fig. 5.8 Proposed inverter in grid-connected format

A MPPT algorithm is very sluggish compared to other control algorithms for PV inverters as temperature and sunlight intensity are not fast varying. Although fast inner control loops may be needed to track electrical parameters, any outer control loop that is based on a MPPT algorithm does not have to be fast, which reduces the complexity of the inverter control structure. As a result, any MPPT algorithm that can be implemented for the proposed inverter is considered as a set-point with respect to the other control loops, just as other researchers have done for other inverters [63], and thus the implementation of MPPT methods in the proposed converter will not be considered in this thesis.

5.3.3 Control Algorithm for the Input Inductor (L_{in}) Current Controller

In order to minimize the current ripple in the input filter inductor (L_{in} in Fig. 5.8) a controller that can fix the current in L_{in} based on an MPPT set-point is needed. The PV panel terminal voltage and the current in L_{in} are two related and mutual parameters.

Considering Fig. 5.7, if one of these parameters is fixed to a certain level, then the other will be fixed automatically. In this way, it is sufficient to select one of parameters based on the MPPT set-point. It should be noted that, in addition to minimizing current ripple, the control the current in L_{in} provides natural current protection for the DC side.

In this section, a controller for the current in L_{in} is considered. In order to do so, only the input section of the PV system shown in Fig. 5.8 will be examined so that the overall PV system can be reduced to what is shown in Fig. 5.9. In Fig. 5.9, an additional capacitor has been placed across the terminal of the PV panels to further smooth out voltage fluctuations. Moreover, the inverter bridge and DC capacitor voltage has been considered as an equivalent fixed DC energy source, V_{DC}, in Fig. 5.9 so that the energy stored in L_{in} can be considered to be transferred to V_{DC} when the circuit is in energy transfer mode.

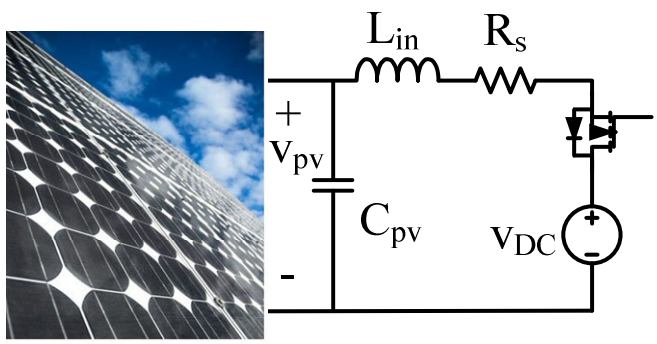
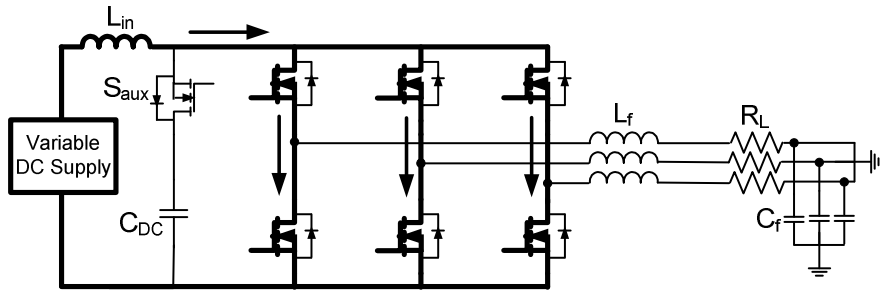


Fig. 5.9 Boost section modeling with respect to the fixed DC bus voltage

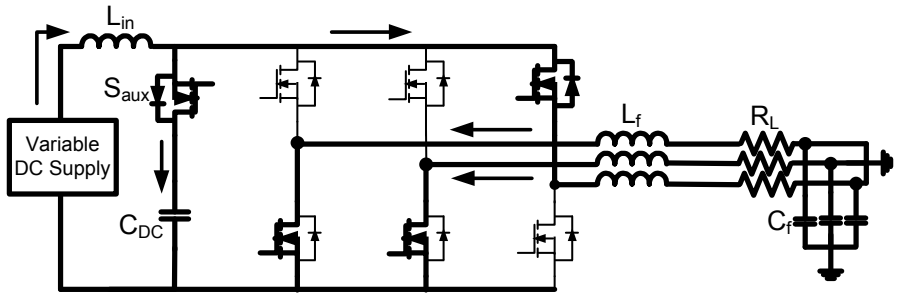
Referring to the operation of the proposed circuit in the previous chapter, two different modes are considered for the circuit when it is working in step-up mode - boost mode and energy transfer mode. These modes are reproduced in Fig. 5.10.

In boost mode, when all six switches of the inverter bridge are on, the relation between the PV panel voltage and the current in L_{in} can be written as follows:

$$v_{pv} = R_{s1} i_L^{in} + L_{in} \frac{d i_L^{in}}{dt} \tag{5.37}$$



(a) Boost



(b) Energy transfer

Fig. 5.10 Different modes of operation of auxiliary switch and input filter

where R_{s1} is the combined equivalent resistance of L_{in} and the switches of the inverter bridge. In energy transfer mode, the relation between the PV panel voltage, current in L_{in} and V_{DC} can be written as follows:

$$v_{pv} = R_{s2} i_L^{in} + L_{in} \frac{di_L^{in}}{dt} + v_{DC} \tag{5.38}$$

where R_{s2} is the equivalent resistance of L_{in} and the body diode of the MOSFET. Since R_{s1} and R_{s2} have very similar values in practice, they can be substituted with R_s.

In order to design the controller, state-space averaging methods can be used [60]. Using such methods, an average model of the system is needed and this can be obtained as follows:

$$D v_{pv} = D R_s i_L^{in} + D L_{in} \frac{di_L^{in}}{dt} \tag{5.39}$$

$$(1-D) v_{pv} = (1-D) R_s i_L^{in} + (1-D) L_{in} \frac{di_L^{in}}{dt} + (1-D) v_{DC} \tag{5.40}$$

where D is the duty cycle, the time duration in which the circuit is in boost mode. If (39) and (5.40) are summed, then the result is

$$v_{pv} = R_L^{in} i_L^{in} + L_{in} \frac{d i_L^{in}}{dt} + (1 - D) v_{DC} \tag{5.41}$$

which is the average model of the input filter. In this model, the output voltage, which is the DC capacitor voltage, is always fixed by the inverter controller; v_{pv} and i_L^{in} are the two variables that should be controlled. As was previously mentioned, if one of these variables, for example i_L^{in}, is controlled, then the other will be fixed automatically. The target of the control method is i_L^{in}, which can be controlled by changing D.

Based on (5.41), a control scheme such as the one shown in Fig. 5.11 can be developed. Fig. 5.11 shows the control loop that can regulate inductor current i_L^{in} to the desired reference current i_L^{ref}, which is the set-point defined by the MPPT algorithm based on available power at the PV side. It should be noted that since the variation of the PV panel voltage is very sluggish, this voltage and the voltage across capacitor C_{pv} in Fig. 5.9 are almost the same during transient conditions and thus there is no need to consider the two voltages separately in the modeling procedure.

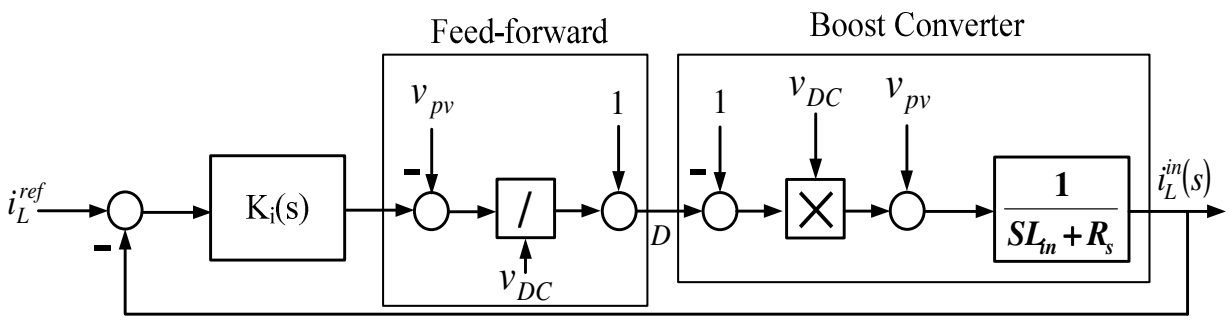


Fig. 5.11 Block diagram of the proposed input filter control scheme

5.4. Case Studies

In order to confirm the operation of the proposed inverter in grid-connected format (Fig. 5.8) with the proposed control scheme, two different case studies were considered. The first was the operation of the overall system with a disturbance in v_{pv} and the second was the operation of the overall system with a disturbance in i_L^{ref}. Although these two disturbances can be modeled as ramp signals because the rate of change in both cases is sluggish in practice, they were modeled as step change signals to better prove the stability of the system.

For the two case studies, the parameters of the system were as follows:

$$v_{pv} = 290 - 500\ V$$

$$v_{DC} = 500 - 600\ V$$

$$L_{in} = 2\ mH$$

$$R_s = 0.2\ Ohm$$

$$L_f = 3\ mH$$

$$Maximum\ Output\ Power = 1.6\ kW$$

$$C_{DC} = 400\ \mu F$$

$$C_{pv} = 200\ \mu F$$

$$Grid\ Voltage_{rms} = 110\ V \text{ (Phase to neutral)}$$

$$Aux.switch\ PMW\ frequency = 40\ kHz$$

Key parameters for the PV panel voltage input (Fig. 5.8) are presented in Table I and the PV panel P-V and I-V curves are shown in Fig. 5.13 and 5.14.

Table 1: The details of the PV cell

Number of Cells Ns	850
Standard Light Intensity S0	1000 w/m^2
Ref. Temperature	25˚C
Series Resistance	0.008 Ohm
Shunt Resistance	1000 Ohm
Short Circuit Current	8 A
Saturation Current	2.16e-8 A
Band Energy Eg	1.12
Ideality Factor A	1.2
Temperature Coefficient Ct	0.0024
Coefficient Ks	0
Maximum available power	1.6 kW

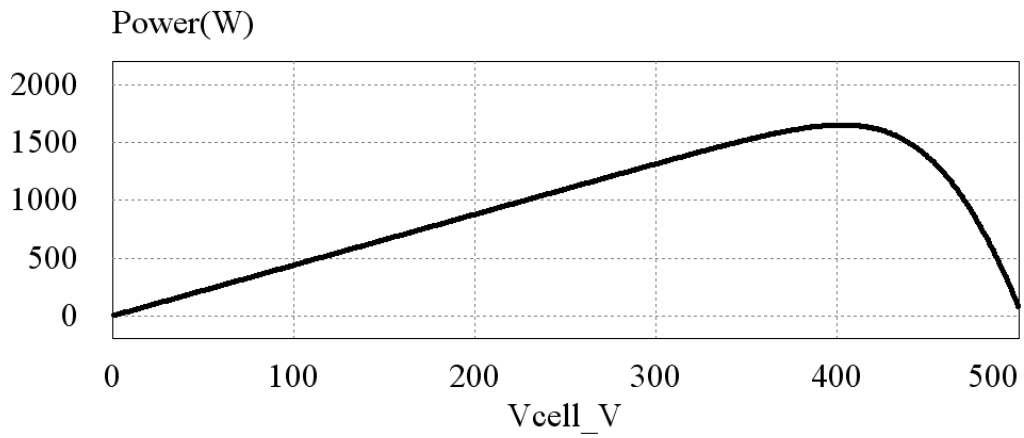


Fig. 5.12 P-V curve of the PV cell

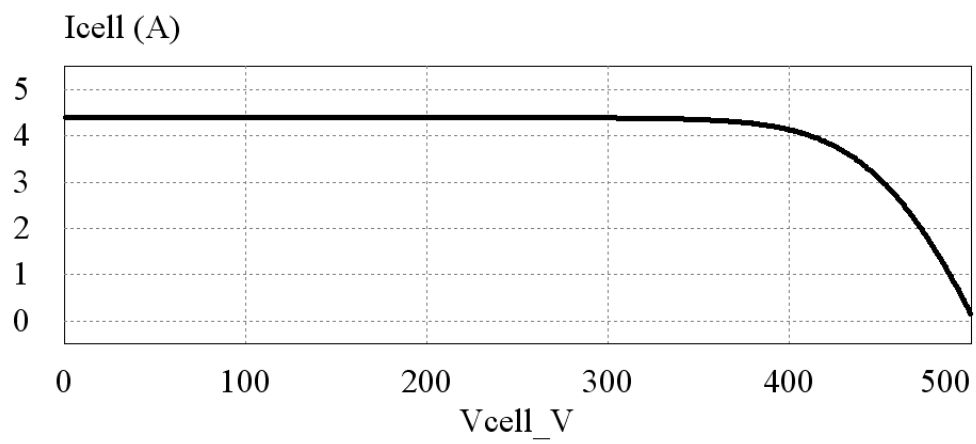


Fig. 5.13 I-V curve of the PV cell

The compensation control block, $K_i(s)$ in Fig. 5.11, was designed by using SISOTOOL, a controller design toolbox in MATLAB [64], to achieve the following gain margin (G.M.) and phase margin (P.M.):

$$\mathrm{G.M.} = \inf$$

$$\mathrm{P.M.} = 90 \text{ deg.}$$

The result of the design is that $K_i(s)$ can be expressed as

$$K_i(s) = \frac{500}{s} + 25 \tag{5.42}$$

5.4.1 Step Changes in v_{pv}

Using the system parameters mentioned above, the PV cell details listed in Table I, the P-V and I-V curves in Figs. 5.12 and 5.13 respectively and the compensator control block expressed in (5.42) a circuit simulation model was developed in PSIM, a software dedicated to power electronic converter simulation [65]. The PSIM model was used to simulate the two case studies. For the first case study, the PV panel output voltage (input to the system) was dropped about 20% as a worst-case scenario and the input inductor current set point was kept the same – a situation that can happen in real life when temperature increases. The step change happens at t=0.4s. Although this temperature change is generally gradual in practice, it was considered as a step change in the simulation model to prove the stability of the system under worst-case conditions.

Fig. 5.14 shows the sinusoidal output current of the inverter and i_d and i_q as they were defined in the dq-frame representation shown in Fig 5.6. As can be seen, i_d is stabilized and i_q returns to zero after the disturbance, which confirms that the proper operation and the stability of the inverter. Fig. 5.15 shows the input inductor current, the auxiliary switch current and the PV current. It can be seen that all these signals are stabilized after the disturbance. Fig. 5.16 shows the DC bus voltage (inverter input voltage), the PV voltage and the output signal of the controller.

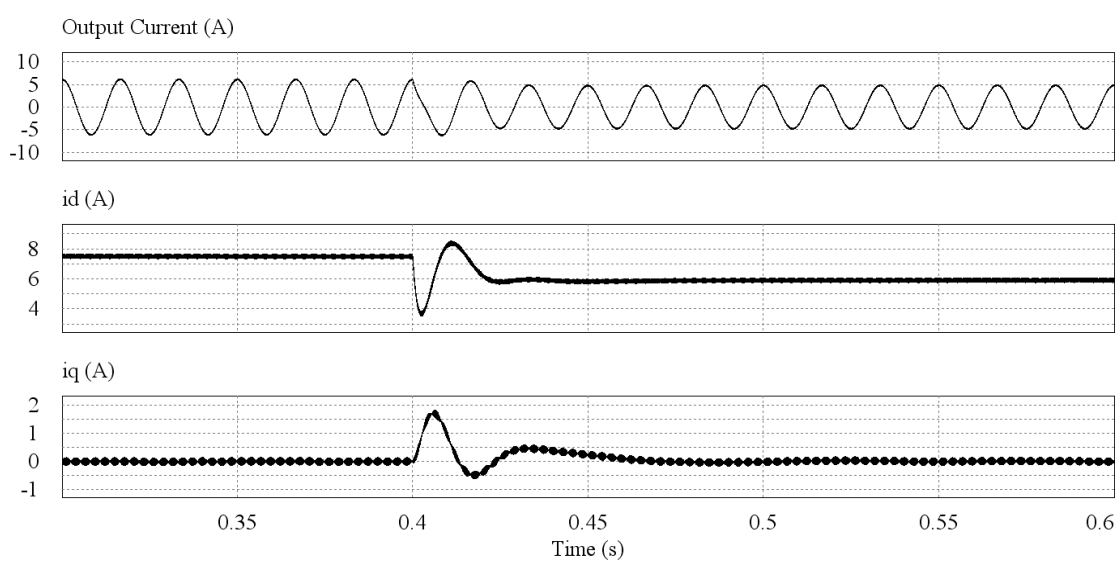


Fig. 5.14 Output current, i_d and i_q of the inverter

It can be seen that the DC bus voltage immediately returns to its set point after a disturbance and that the control signal, which is the input to the PWM controller, is increased to a new level. It should be noted that there is no fluctuation on v_{pv}, which simplify the implementation of a MPPT algorithm.

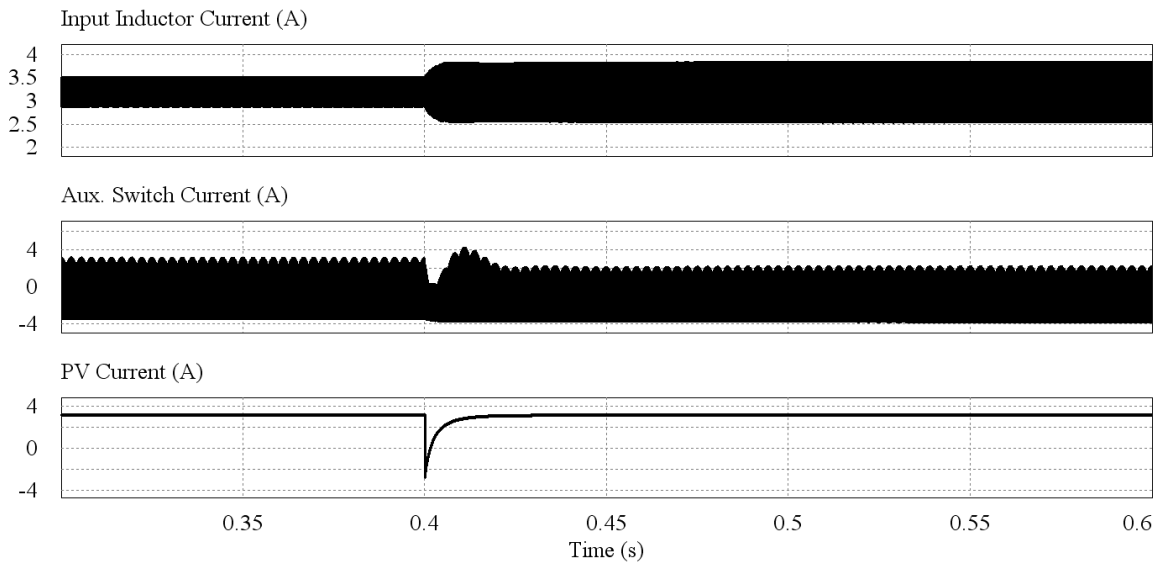


Fig. 5.15 Input inductor current, auxiliary switch current and PV current

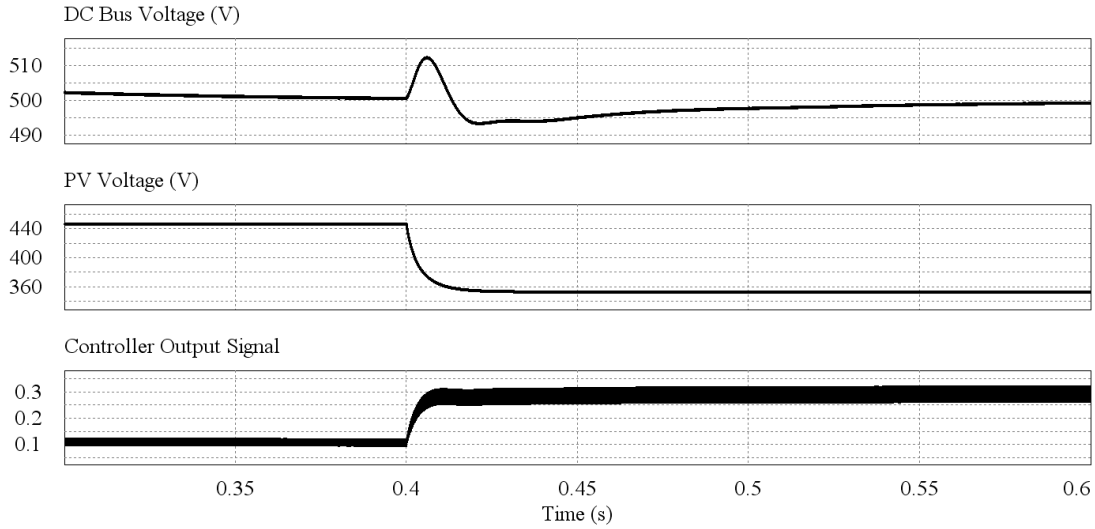


Fig. 5.16 DC bus voltage, PV cell voltage and output signal of the controller

5.4.2 Step Changes in i_L^{ref}

For this case study, a step change was made to the input inductor current reference signal i_L^{ref} and the PV panel voltage was kept constant for the PSIM simulation. At t=0.75s, the step change on i_L^{ref} is about 30%., from 3.2 A to 2.2 A, which can happen when the intensity of the sunlight on the PV panels changes. Fig. 5.17, 5.18 and 5.19 show waveforms of the same variables as for the previous case. It can be seen that these variables can all be stabilized as in the previous case.

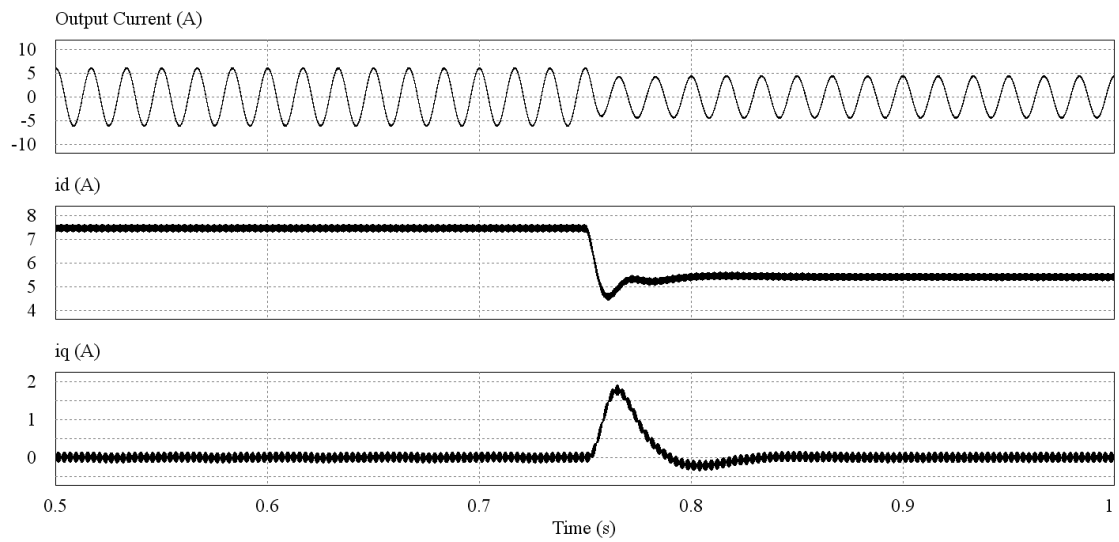


Fig 5.17 Output current, i_d and i_q of the inverter

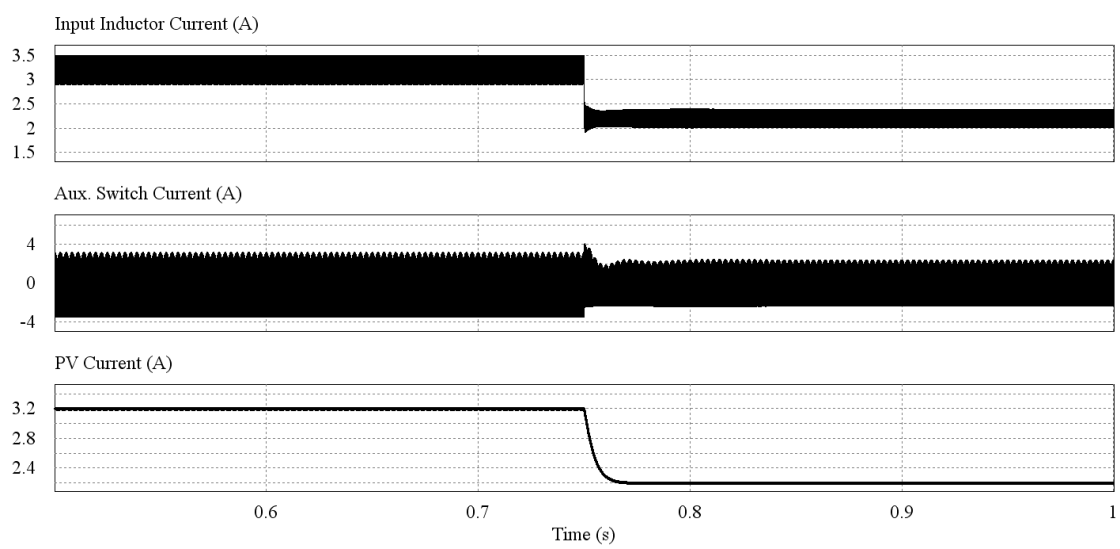


Fig. 5.18 Input inductor current, auxiliary switch current and PV current

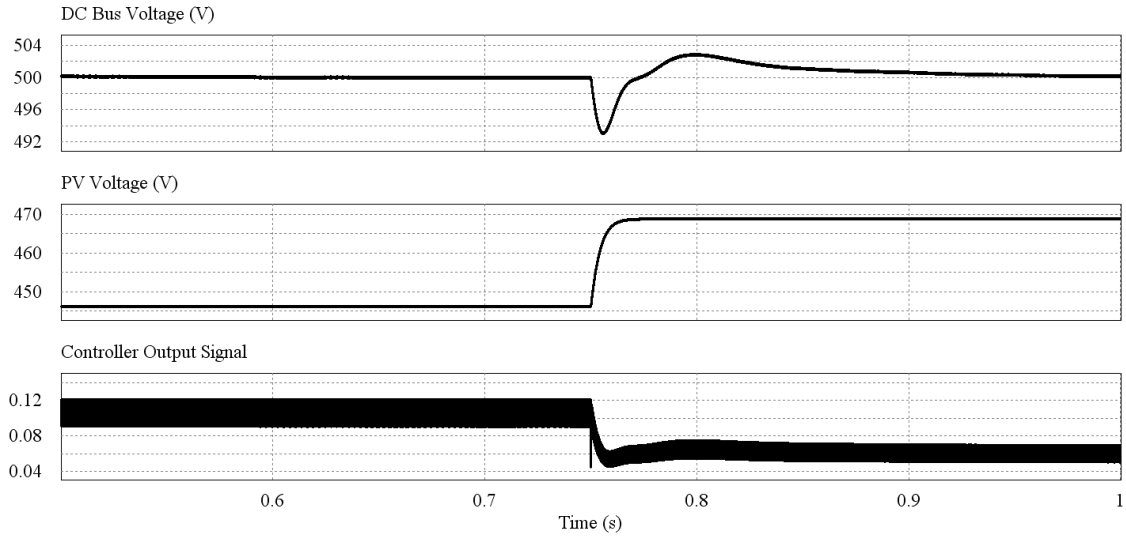


Fig. 5.19 DC bus voltage, PV cell voltage and output signal of the controller

5.5. Conclusion

In this chapter, the control of the inverter that was proposed in the previous chapter was investigated. Two key control issues were examined, the control of the AC side of the converter and the current that is fed from the PV panels to the inverter. For the first control issue, a model that was based on current mode theory and on conventional three-phase frame to two-axis frame transformation theory was developed. As a result of the model, a control scheme that could allow the inverter to produce output AC waveforms that were sinusoidal with little distortion and a control scheme that could produce a fixed DC bus capacitor voltage could be developed.

With the development of a control scheme that could fix the DC bus voltage, it was possible to focus on a control scheme that could minimize the ripple on the current that is fed from the PV panels to the inverter, which was the second key control issue that was investigated in this chapter. The significance of reducing this ripple is that it allows maximum power point tracking (MPPT) schemes that can extract the maximum energy that is available from the PV panels at any given instant, thus increasing the efficiency of the overall system. For this thesis, however, the investigation of MPPT techniques was

considered to be outside its scope and since the dynamics of MPPT methods are sluggish, it was assumed that the PV panels operated around a predetermined set point.

The dynamics of the PV inverter system were investigated using a model that considered the two key control issues and that was implemented in PSIM software. Two cases were studied using this model – the first involved changing the PV panel output voltage and the second involved changing the input inductor reference current. In both cases, it was shown how sinusoidal output currents could be produced, how the DC capacitor voltage could remain fixed, and how the input inductor current could have little ripple, even when the inverter PV system was subjected to worst-case disturbances.

Chapter 6

Conclusion

6.1. Summary

The main objective of this thesis has been to investigate the properties and characteristics of power electronic converters that can step up voltage and step down voltage. Such converters have an advantage over more conventional converters that can only perform one of these functions as they can operate over a wider range of operating conditions.

In Chapter 1, certain basic power electronic principles that are related to the thesis work were reviewed. It was stated in the chapter that the focus of the thesis would be on two distinct applications where converter with step up/down capability can be used: AC-DC single-stage converters with input power factor correction (PFC) and DC-AC inverters. Each of these applications was split up into two research topics - a new AC-DC single-stage converter and a new AC-DC full-bridge single-stage converter based on the basic buck-boost topology for the first application and a new three-phase inverter topology and its control for the second. The thesis outline and objectives were also stated.

In Chapter 2, a new single-phase AC-DC single-stage converter was introduced. Single-stage converters in general are converters that can convert input AC voltage into an intermediate DC bus voltage and convert the intermediate DC bus voltage into the required DC output voltage using just a single converter with just a single controller to regulate the output voltage. Although single-stage converters are simpler and less expensive than two-stage converters that have a front-end AC-DC stage and a back-end DC-DC stage, they have several drawbacks that make them less attractive than two-stage converters. Most of these drawbacks are due to the fact that they do not have a controller to regulate the intermediate DC bus voltage, unlike two-stage converters. As a result, the intermediate DC bus voltage is left uncontrolled and can vary considerably as is dependent on the input line and the load. It may become excessive (> 800 V – 1000 V) under certain operating conditions unless the converter is designed in a way to prevent

this from happening. Previously proposed design solutions, however, degrade the performance of the converter considerably and thus an alternative solution was proposed in Chapter 2.

The single-stage converter proposed in Chapter 2 uses two mechanisms to keep the intermediate DC bus voltage almost constant regardless of the input line and the output load. The first mechanism is to base the converter's input AC-DC section on a buck-boost converter instead of a boost converter and the second was to use a clamping mechanism to clamp the DC bus voltage. In Chapter 2, the new single-stage converter was introduced and its basic operation and its modes of operation were described. The converter's steady-state characteristics were determined by mathematical analysis and the results of the analysis were used to develop a procedure for the selection of key parameter values. The feasibility of this converter was confirmed with results obtained from an experimental prototype.

In Chapter 3, the concepts discussed in Chapter 2 that were related to the use of buck-boost converter properties in AC-DC single-stage converters were extended to a full-bridge converter designed for higher power levels. As a result, a new AC-DC single-stage buck –boost full-bridge converter was proposed in the chapter. The attractive features of the converter are that it can operate with near unity input power factor, and a DC bus voltage that is always less than 450 V and that has much less variation with line and load change than boost-type single-stage converters. In the chapter, the operation of the converter was explained, its characteristic curves were generated by a computer program and its components were designed according to the results of the characteristics curves. An experimental prototype was built to confirm the feasibility of the proposed converter.

In Chapter 4, a new technique that can be used to extend the operating range of a three-phase inverter was proposed. Although the technique was novel, it was based on established principles related to well-known active-clamp converters. It was shown that some converters with active clamps can step down voltage while others can step up voltage and that it is possible to derive active clamp converters that can do both. Active clamp converters with step-down/step-up capability can operate in various modes and emphasis was placed on operating active clamp converters in step-down mode with step-

up mode operation occurring only when the inverter input voltage (active-clamp capacitor voltage) has dropped below an appropriate value. With this type of operation, the active clamp switch is always on when the inverter is in step-down mode so that the converter's equivalent circuit is like a standard VSI or full-bridge converter with an input LC filter.

The later part of the chapter examined how the proposed active clamp technique can be implemented in an inverter. The inverter can be used as a stand-alone converter or as part of an overall converter system. The advantageous features of the inverter are that it has identical characteristics as a conventional voltage-source inverter when it is in step-down mode, it can be implemented with standard PWM techniques for VSI and CSI, none of its components carry the full input inductor current when it is in step-up mode, and it is capable of injecting reactive power to the grid. The operation of the inverter with the proposed active clamp technique was confirmed with results obtained from a simple proof-of-concept prototype converter.

In Chapter 5, the control of the inverter that was proposed in the previous chapter was investigated. Two key control issues were examined, the control of the AC side of the converter and the current that is fed from the PV panels to the inverter. For the first control issue, a model that was based on current mode theory and on conventional three-phase frame to two-axis frame transformation theory was developed. As a result of the model, a control scheme that could allow the inverter to produce output AC waveforms that were sinusoidal with little distortion and a control scheme that could produce a fixed DC bus capacitor voltage could be developed.

With the development of a control scheme that could fix the DC bus voltage, it was possible to focus on a control scheme that could minimize the ripple on the current that is fed from the PV panels to the inverter, which was the second key control issue that was investigated in this chapter. The significance of reducing this ripple is that it allows maximum power point tracking (MPPT) schemes that can extract the maximum energy that is available from the PV panels at any given instant, thus increasing the efficiency of the overall system. For this thesis, however, the investigation of MPPT techniques was considered to be outside its scopes and since the dynamics of MPPT methods are sluggish, it was assumed that the PV panels operated around a predetermined set point.

The dynamics of the PV inverter system were investigated using a model that considered the two key control issues and that was implemented in PSIM software. Two cases were studied using this model – the first involved changing the PV panel output voltage and the second involved changing the input inductor reference current. In both cases, it was shown how sinusoidal output currents could be produced, how the DC capacitor voltage could remain fixed, and how the input inductor current could have little ripple, even when the inverter PV system was subjected to worst-case disturbances.

6.2. Conclusion

Based on the results of the work presented in this thesis, the following can be concluded:

- For the low power single-stage converter presented in Chapter 2, it is possible to have an intermediate DC bus voltage that is almost constant, regardless of line and load variations, along with an input current that is almost sinusoidal. In other words, the implementation of a mechanism to clamp the intermediate DC bus voltage has little, if any, effect on the input current waveform..
- For the higher power single-stage converter presented in Chapter 3, the converter can operate with an input current that is sinusoidal and in phase with the input voltage and with a DC bus capacitor voltage that is less than 450 V and that has less variation with input line that was is typically seen in boost-based single-stage converters. This is especially true when the converter is operating with heavy load.
- For the higher power single-stage converter presented in Chapter 3, the DC bus voltage has little variation with respect to load when the converter is operating with high input voltage, but that it varies significantly with load when it is operating with low input voltage. This is because when the converter is operating at low line, there can be significant variation in the converter duty cycle, which affects the energy equilibrium at the DC bus capacitor and thus the DC bus capacitor voltage. This, however, is not the case when the converter is operating with high input voltage as the duty cycle range is restricted and any changes in duty cycle over the load range are minor.

- For the inverter proposed in Chapter 4, sinusoidal output waveforms can be produced regardless of whether the converter is operating in voltage step-down mode or in voltage step-up mode. This is because when the inverter is operating in voltage step-down mode, it is operating just like a conventional voltage-source inverter (VSI) and thus it can operate with standard pulse-width modulation (PWM) techniques for VSIs and when it is operating in voltage astep-up mode, it can operate with standard PWM techniques for CSIs. In other words, it can be concluded that the proposed inverter can operate with standard PWM techniques when operating under either mode so that standard sinusoidal output waveforms can be produced.
- For the control technique proposed in Chapter 5, it is possible to decouple the control of the output AC waveforms that are fed to the grid and the current that comes out of the input DC source. This is because it is possible to fix the DC bus capacitor voltage and control the AC output current with one control scheme while controlling the current that is drawn from the DC source PV panels (and thus the maximum available power) with a second control scheme.

6.3. Contributions

The main contributions of this thesis are as follows:

- A new low power single-stage converter based on a buck-boost input section was proposed. The outstanding feature of this converter is that its DC bus capacitor voltage is almost immune to any changes in the input line voltage or the output load because of a mechanism that clamps the DC bus voltage to a predetermined level. Few, if any, previously proposed single-stage converters have this particular feature. The feature is advantageous as it simplifies the design of the converter since it does not have to operate with an extremely variable voltage, as is the case for most other converters, and the size of the DC bus capacitor can be reduced as it does not have to be overdesigned to deal with a very wide range of operating conditions.
- A new higher power single-stage full-bridge converter was proposed. The main features of the new converter are that it can operate with an input current that is

sinusoidal and in phase with the input voltage and with a DC bus capacitor voltage that is less than 450 V and that has less variation with input line than what is typically seen in boost-based single-stage converters. The existence of such features result in the simplification of the design of the converter and, like the converter proposed in Chapter 2, the reduction of the size of the DC bus capacitors because the DC bus voltage has much less variation.

- A new three-phase inverter was proposed. The proposed inverter has voltage step-up/step-down capability without the drawbacks of other previously proposed inverters with similar capability. Such drawbacks include a series diode, numerous additional components, and high current stresses in components.
- A suitable control method for the new inverter was proposed. This method allows for the decoupled control of the input and output currents of a PV system. The control method makes the use of maximum power point tracking (MPPT) techniques possible in the proposed converter as well as ensuring that sinusoidal currents can be injected into the grid.

6.4. Future Work

- The converter proposed in Chapter 2 was a low power converter based on the conventional flyback converter. Future work can be conducted to see whether the proposed clamping mechanism approach can be extended to higher power converters based on other fundamental topologies.
- The control method for the proposed inverter was confirmed with standard, widely used computer simulation tools such as MATLAB and PSIM. Future work can involve the experimental implementation of this control method. Given that the results of the software tools used in this study are generally accepted by power electronic researchers, nonetheless the feasibility of the control method should be further confirmed.
- Active clamp technology was used to develop a new inverter with voltage step-up / step-down capability. Future work can involve extending this approach to other

converters where such a capability would be useful, such as DC-DC converters for renewable energy systems.

Appendix A

Calculation of Average Input Power/Cycle in DCM

If the input current of the proposed converter is fully discontinuous then the input current over a half-line cycle will look like the current waveform shown in Fig. A1. The current rises when the switch is on and falls when the switch is off. The average power that is injected into the converter during a half-line cycle can be calculated as follows:

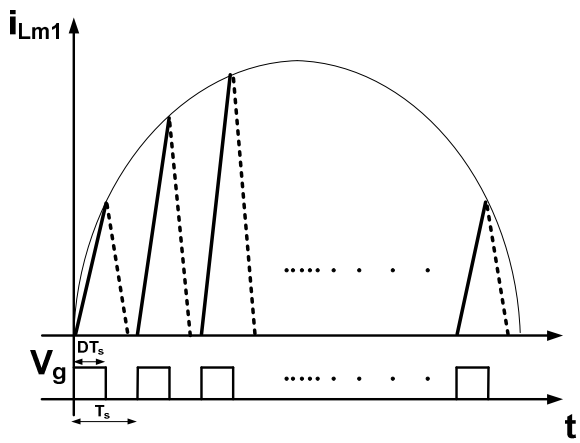


Fig. A1: Input current waveform

The instantaneous power injected to the converter is:

$$p(t) = v_{in}(t) i_{in}(t) \tag{A1}$$

The average power during a switching cycle is:

$$P_{avg} = \frac{1}{T_s} \int_0^{DT_s} P(t) dt \tag{A2}$$

Since the line frequency is much lower than switching frequency, the input voltage can be assumed to have a constant value of $V_m \sin(\omega k)$ during any switching cycle k; therefore equ. (A2) can be rewritten as

$$P_{avg} = \frac{V_m \sin(\omega k)}{T_s} \int_0^{DT_s} i_{in}(t) dt = V_m \sin(\omega k)\, i_{avg} \tag{A3}$$

The value of i_{avg} in the switching cycle k is

$$i_{avg}(k) = \frac{\int_0^{DT_s} i_{in}(t)dt}{T_s} = \frac{V_m D^2 T_s \sin(\omega k)}{2L_{m1}} \tag{A4}$$

The average of the input power during a half-line cycle can be found by substituting these values into equ. (A2), but the integration area is in half a line cycle

$$P_{in-avg} = \frac{2}{T_L}\int_0^{\frac{T_L}{2}} P_{avg}dt = \frac{2}{T_L}\int_0^{\frac{T_L}{2}} [V_m \sin(\omega t)]\left[\frac{V_m D^2 T_s \sin(\omega t)}{2L_{m1}}\right]dt = \frac{D^2 V_m^2}{4L_{m1}f_s} \tag{A5}$$

Integration of (A5) over half a line cycle gives (2.6).

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Teaching Experience

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2) **Behineh Niru Spadan Company, Isfahan, Iran**
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- Designed and implemented monitoring and data collector software for electrical power analyzer, fault recorder, electrical meter tester and industrial data logger
- Field test of electrical power analyzer, fault recorder, electrical meter tester and industrial data logger
- Commissioning and installation of stationary electrical meter tester, power analyzer and data logger
- Power quality consultancy with industries and electrical distribution companies

- Design of special power meter for "Mobarake Steel Complex, Railway"

Honors and Awards

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Scientific and professional activities

- Presentation at several professional and scientific conferences in English and Farsi (IEEE APEC, IEEE ECCE, etc.)
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  Summer 2006
- Attending ISO 14000-1training workshop in NIGC.
  Spring 2006
- Attending Gas Station and Gas Transmission Lines training workshops at NIGC (one month training period at NIGC training center) Isfahan, Iran
  Fall 2004
- Mentoring 6 undergraduate students for their internship in Behineh Niru Spadan Co.
  summer 2003 - 2004
- Co-op student in Iranian Electrical Grid Management (Isfahan)
  Summer 1996