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Delay Extraction Based Equivalent Elmore Model For RLC On-Chip Interconnects

Shamsul Arefin Siddiqui
The University of Western Ontario

Supervisor
Dr. Anestis Dounavis
The University of Western Ontario

Graduate Program in Electrical and Computer Engineering
A thesis submitted in partial fulfillment of the requirements for the degree in Master of Engineering Science

DELAY EXTRACTION BASED EQUIVALENT ELMORE MODEL FOR RLC ON-CHIP INTERCONNECTS

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Shamsul Arefin Siddiqui

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The University of Western Ontario
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THE UNIVERSITY OF WESTERN ONTARIO
School of Graduate and Postdoctoral Studies

CERTIFICATE OF EXAMINATION

Supervisor

_____
Dr. Anestis Dounavis

Supervisory Committee

Examiners

_____
Dr. Len Luyt

_____
Dr. Quazi Mehbubar Rahman

_____
Dr. Rajiv K. Varma

The thesis by

Shamsul Arefin Siddiqui

entitled:

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Abstract

As feature sizes for VLSI technology is shrinking, associated with higher operating frequency, signal integrity analysis of on-chip interconnects has become a real challenge for circuit designers. For this purpose, computer-aided-design (CAD) tools are necessary to simulate signal propagation of on-chip interconnects which has been an active area for research. Although SPICE models exist which can accurately predict signal degradation of interconnects, they are computationally expensive. As a result, more effective and analytic models for interconnects are required to capture the response at the output of high speed VLSI circuits. This thesis contributes to the development of efficient and closed form solution models for signal integrity analysis of on-chip interconnects. The proposed model uses a delay extraction algorithm to improve the accuracy of two-pole Elmore based models used in the analysis of on-chip distributed RLC interconnects. In the proposed scheme, the time of fight signal delay is extracted without increasing the number of poles or affecting the stability of the transfer function. This algorithm is used for both unit step and ramp inputs. From the delay rational approximation of the transfer function, analytic fitted expressions are obtained for the 50% delay and rise time for unit step input. The proposed algorithm is tested on point to point interconnections and tree structure networks. Numerical examples illustrate improved 50% delay and rise time estimates when compared to traditional Elmore based two-pole models.

Keywords

Delay, distributed RLC model, interconnects, moment matching, simulation, tree, VLSI, CAD.

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ABBREVIATIONS

AWE	ASYMPTOTIC WAVEFORM EVALUATION
CAD	COMPUTER AIDED DESIGN
CFH	COMPLEX FREQUENCY HOPPING
CPU	CENTRAL PROCESSING UNIT
IC	INTEGRATED CIRCUITS
MEMS	MICRO ELECTRO MECHANICAL SYSTEMS
MNA	MODIFIED NODAL ANALYSIS
ODE	ORDINARY DIFFERENTIAL EQUATION
PDE	PARTIAL DIFFERENTIAL EQUATION
PRIMA	PASSIVE REDUCED ORDER INTERCONNECTS MACROMODELING ALGORITHM
PUL	PER-UNIT-LENGTH
RC	RESISTIVE-CAPACITIVE
RLC	RESISTIVE-INDUCTIVE-CAPACITIVE
SPICE	SIMULATION PROGRAM WITH INTEGRATED CIRCUIT EMPHASIS
VLSI	VERY LARGE SCALE INTEGRATION
TEM	TRANSVERSE ELECTROMAGNETIC

SI	SIGNAL INTEGRITY
CMOS	COMPLEMENTARY METAL OXIDE SEMICONDUCTOR
MOS	METAL OXIDE SEMICONDUCTOR
SSN	SIMULTANEOUS SWITCHING NOISE
ITRS	INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

CHAPTER 1

INTRODUCTION

1.1 Background Review and Problem Identification

The process of creating integrated circuits by combining hundreds of thousands of transistors into a single chip is usually referred to very-large-scale-integration (VLSI). VLSI began in early 1970s when complex semiconductor and communication technologies were being developed. Now a days, VLSI circuits and integrated circuit (IC) chips find application in numerous fields like mobile and satellite communication, computer hardware, micro-electromechanical systems (MEMS) devices, robotics and other electronic systems. VLSI circuit density and complexity has exponentially increased over the years leading to miniaturization of electronic systems, increase in speed of production from circuit specifications to actual hardware development and a resulting decline in prices of electronic devices. The rapid decrease in featured size has followed by a commensurate increase in operating frequencies. At gigahertz range [1] frequencies, design of clocks has been very critical which mainly determines the speed of operation of such circuits. As anticipated by Moore's law, the number of transistors in an integrated circuit (IC) has doubled every two to three years. Modern ICs are now composed of millions of transistors switching simultaneously within a fraction of a second.

At present, 32 nm technology is in production and microprocessor clock frequencies are well above GHz range. The speed of an electrical signal in an IC is governed by two components. The first component is the switching time of an individual transistor, known as transistor gate delay, and the second one is the signal propagation time between transistors, known as wire delay or interconnect delay. In modern VLSI circuits, major challenges include layout optimization, high power dissipation at high frequencies of operation, increased interconnect delays, crosstalk noise between mutually coupled interconnects and simultaneous switching noise (SSN) in the power/ground plane pair. It has been analyzed that signal integrity problems in interconnects determines the performance of overall circuits. It is important to predict signal degradation like propagation delay, crosstalk noise, signal overshoot, ringing and attenuation in the early design cycles [2]-[5] which can critically affect system response. Using computer aided design (CAD) tools for signal integrity, simulations have replaced the more time-consuming and inefficient practice of circuit development and testing at every stage of the design cycle for modern IC circuitry. However interconnect simulations suffer from a myriad of issues which require sophisticated CAD tools for analysis.

In the past, interconnects were modeled as a single lumped capacitance. Then lumped resistance-capacitance (RC) models were introduced in the analysis of the performance of on-chip interconnects [6], [7]. However, the electrical length of interconnects have become a significant fraction of the fundamental and harmonic wavelength of the transient signal [8] at the gigahertz speed of operation with multiple devices switching simultaneously. This means inductance effect will come into play

when dealing with these high speed interconnects. At such high speeds, interconnects must be modeled as distributed resistive-inductive-capacitive (RLC) transmission lines as opposed to lumped resistive-capacitive (RC) models to account for the non monotonic nature of the response [9].

Since overall circuit performance depends on interconnect delay, low dielectric metals like copper has been used in IC technology to decrease the line resistance and capacitances [10]. However this does not significantly decrease the line inductances. This has led to inductive line effects being a significant contributor to signal degradation. As the inductive effect of the line becomes dominant, the propagation delay of the line increases. Since feature sizes shrink in deep sub-micrometer technology to 90nm and beyond, signal propagation delay in interconnect has been found to outweigh the gate delay [10], [11]. This delay, if not effectively quantified can cause improper triggering and timing uncertainty. Line inductance can also lead to effects like ringing and non-monotonic response contaminated with spurious glitches on active lines.

As mentioned in the previous paragraphs, on-chip interconnects were modeled as RC lines and single-pole Elmore-based models [6], [12]–[14] were most widely used to estimate signal delay. However predicting signal waveform in tree structure interconnects has been prime concern. Elmore based model is used as a delay model for the buffer insertion in RC trees and wire sizing [15]-[24]. The popularity of this model is due to the fact that it has analytic expression for predicting 50% delay and rise time which is computationally fast and well suited for considering simulations of millions of transistors in VLSI circuits. Traditional Elmore based models have

limitations modeling RLC distributed interconnect networks, since these RLC lines may give non monotonic responses. As a result modeling RLC interconnects for modern circuit designers has been the centre of intense research [25]-[43]. To predict signal transients in high-speed interconnects, the lines are modeled as single line, coupled line and tree structure interconnects. In broad perspective there are mainly two ways to model on-chip interconnects which are SPICE macromodels and closed-form analytic models.

SPICE is the most common simulation tool that generally uses numerical integration or convolution techniques to provide accurate results. SPICE macromodels include both lumped model and models based on delay extraction using techniques such as method of characteristics [25]. The conventional lumped models or rational approximation models (such as PRIMA [44], MRA [29]-[30], compact differences [45]) represent interconnects as resistive, inductive and capacitive circuit elements or as ordinary differential equations (ODE). However for high frequency applications, the signal delay can be significant. These algorithms approximate the propagation delay implicitly without using delay extraction. Nonetheless to model long lines with significant delay these algorithms require higher order rational approximations to accurately capture the delay of the signal leading to inefficient transient SPICE simulation. For more compact class of models the method of characteristics [25] has been used which is based on extracting the line-propagation delay [26]-[30] .Since the delay terms can account for the high frequency characteristics of an interconnect, these models allow more compact discretization of the line and lead to smaller matrices when applied to low loss, long lines. Simulation of on-chip interconnects using lumped models

or method of characteristic algorithms requires numerical integration or convolution techniques which obviously provide excellent accuracy but they are computationally expensive to be used in layout optimization [23] since this requires simulating circuit networks composed of millions of logic gates.

In order to avoid the computational complexity of SPICE simulations closed-form analytic models have been developed. In order to derive closed form analytic models for on-chip interconnects, far end transistor is modeled as parasitic capacitor and near end transistor is modeled as resistor serially connected to a voltage source. These models are usually effective for obtaining the far end solutions. Such circuit scenarios represent a point-to-point interconnect system in IC designs ([16]-[24]) useful for initial design or layout optimization cycles and use simple low order rational function to approximate the transfer function so that it can be easily converted to the time-domain in a closed form manner without requiring any numerical integration. Since these methods don't use numerical integration of large matrices they are computationally more efficient. Single pole Elmore based RC model [12] was the first analytic closed form model for on-chip interconnects. Considering the inductance effect of RLC interconnects, two pole model (second order approximation) was developed in order to capture non monotonic responses of RLC lines. To obtain more accurate models, multi-pole transfer functions [12]-[14], [31]-[32], traveling-waveform technique [34]-[35], modified Bessel function [37]-[40] and Fourier analysis [41] were introduced later on. However, extending these techniques to efficiently analyze RLC tree structures is a challenging task.

Even though Elmore based models have limited accuracy, they are commonly used to analyze integrated circuits composed of millions of gates, since it is often impractical and time consuming to use accurate modeling techniques to evaluate the signal delay at each node in the circuit . These techniques can provide quick relative delay estimates of different paths in large circuit networks, allowing for more in-depth and time consuming simulations to be performed on critical paths. The difficulty, in modeling inductive dominant RLC interconnects is that these networks may exhibit significant signal delays. Elmore based models rely on one or two pole approximations to estimate the delay. As a result, it is extremely difficult to capture the delay of longer lines of interconnect. To overcome this problem a new algorithm is proposed in this thesis.

1.2 Objectives and Contributions

The objective of this work is to use a delay extraction technique to improve the accuracy of two-pole Elmore-based models for RLC interconnects. Since inductive dominant RLC interconnects may exhibit significant signal delays, it is extremely difficult to model these networks using only a two-pole transfer function. As a result, the proposed algorithm provides a mechanism to explicitly model the signal delay caused by RLC on-chip interconnect without significantly increasing the computational complexity of the model.

The proposed delay extraction based equivalent Elmore model is derived from the second order approximation of distributed RLC model since they provide better accuracy compared to lumped RLC model. In the proposed scheme, the time of fight signal delay

is extracted without increasing the number of poles or affecting the stability of the transfer function. This algorithm is used to obtain the far end time domain responses for both unit step and ramp inputs. From this analysis, analytic fitted expressions are obtained for the 50% delay and rise time for unit step inputs using curve fitting techniques. The proposed algorithm is tested on point to point single line interconnects and balanced and unbalanced tree structure networks. Numerical examples illustrate improved 50% delay and rise time estimations when compared to traditional Elmore based two-pole models.

1.3 Organization of the Thesis

The thesis is organized as follows. Chapter 2 reviews the challenges of interconnect simulation in detail. Contributions made in literature to address these problems are also reviewed with special emphasis on some of the latest closed form models proposed. Chapter 3 deals with the proposed algorithms and shows the development of this model. Extracting the time of fight signal delay, the model is developed using the idea of second order approximation of distributed RLC model for both unit step and ramp inputs. Using curve fitting techniques, analytic expressions are provided for the 50% delay and rise time signals for unit step inputs. Chapter 4 deals with several numerical examples (single line, balanced and unbalanced tree structures) to proof the validity of the proposed model with HSPICE analysis and traditional two pole model for both unit step and ramp inputs of different rise times. The thesis is concluded with chapter 5 which summarizes the proposed work and also lists future related work.

Chapter 2

LITERATURE REVIEW

2.1 Introduction

There are many different technologies in which chips can be made but complementary metal oxide semiconductor (CMOS) technologies are the most important and common technologies for very large scale integrated (VLSI) applications such as computers, digital signal processing, telecommunication, medical image processing, cryptography and digital control systems. CMOS circuitry dissipates less power than logic families with resistive loads. Since this advantage has increased and grown more important, CMOS processes have become very popular and dominate, thus the vast majority of modern integrated circuit manufacturing is on CMOS processes [46].

In a CMOS technology, doped silicon substrate is used to fabricate MOS device with a gate of polysilicon on top of a thin layer of oxide. Then n+ or p+ doping is used to make drain and source of the transistor. At first some voltage is applied to gate in order to create the channel between source and drain. Then voltage is applied at the drain terminal As a result, current flows from drain to source. In order to interconnect transistors, a stack of metal layers is available to the designer. Lower level metal layers have higher resistance values and upper level metal layers have lower resistance values. Also the parasitic capacitances and inductances of on-chip interconnect vary from one metal layer to another.

TABLE 2.1
INCREASING CLOCK SPEED IN IC TECHNOLOGY

Year	Technology (nm)	Maximum Clock Speed (GHz)
2004	90	4
2007	65	6.7
2010	45	11.5
2013	32	19.3
2016	22	28.8

As Moore's law predicts, the number of transistors in an integrated circuits (IC) will double every two to three years. For over 30 years, the feature size of CMOS technology has shrunk to dimensions into the nanometer region. According to International Technology Roadmap for Semiconductors (ITRS) [47], [48], feature sizes will further decrease at the rate of 0.7x per generation [1]. As a result of this continuous scaling, higher circuit speeds, lower power and larger packing densities of transistors are achieved. At present, Intel has started producing 32 nm technology microprocessor with a clock frequencies of well above GHz. The speed of an electrical signal in an IC depends on transistor gate delay (i.e. switching time) and the interconnect delay. Since interconnect delay is more important that switching delay, modeling of on-chip interconnects have been an intense area for research.

2.2 VLSI Interconnect with Physical and Electrical Parameters

As technology is scaled, interconnect delay starts to dominate the gate delay which is shown in Fig. 2.1. Because of high operating frequencies and technology shrink inductance effect can no longer be ignored. Inductance is a physical property of a closed current loop. Inductive coupling can occur over a long distance, whereas capacitive

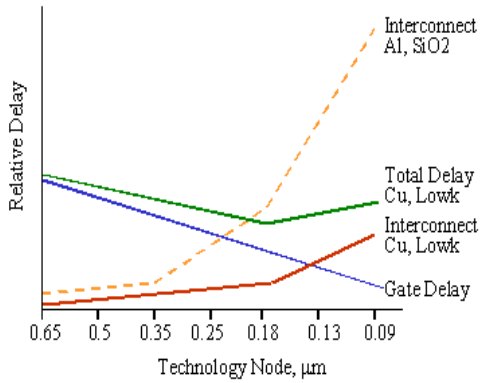


Fig. 2.1 Interconnect and gate delay with IC technology evolution.[47]

coupling is limited to adjacent interconnects. As a result, it is not straightforward to extend the existing parasitic extraction approach to perform inductance extraction in on-chip interconnects.

Interconnects in VLSI and integrated circuits can be considered as strip lines or microstrip transmission lines. For microstrip lines it consists of a conductive strip of controlled width on a low-loss dielectric material mounted on a conducting ground plane. Microstrip is by far the most popular structure, especially for VLSI and other integrated circuits. The major advantage of microstrip is that all active components can be mounted on top of the board. The physical structure of such interconnect is shown in Fig. 2.2 where w, t, h are the interconnect width, height (or thickness), inter-layer dielectric thickness respectively. Interconnect width, height and length can be controlled by the circuit designer. Transmission lines are best described by Telegraphers equation where per unit length resistance, inductance and capacitance (R , L ,C) are needed. From the physical design of interconnect structures it is important to extract the electrical parameters of the interconnect in terms of per unit length resistance (R), capacitance (C) and inductance (L) before performing the timing analysis in the design flow. In standard

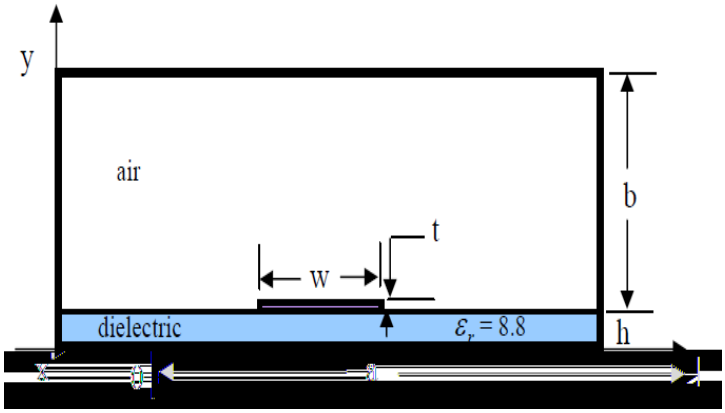


Fig. 2.2 Cross-section of a single-strip shielded transmission line

cell design, quick interconnect parasitic extraction and delay estimation are done at the place and route stage for optimum placement. These extraction becomes important since the interconnect design affects every stage of the design flow.

There are usually two ways to extract interconnect electrical parameters from their physical parameters. One is analytical expressions which are fast to calculate and another way is to use field solver [49], [50]. Analytical expressions of the interconnect per unit length resistance and capacitance are given by following equations [51] for the structure shown in Fig 2.2

$$R = \frac{l}{tw} \tag{2.1}$$

$$C = l.\left[\frac{2\pi\varepsilon_0\varepsilon_r}{\ln(h/t)} + \frac{(\omega - 0.5t)\varepsilon_0\varepsilon_r}{h}\right] \tag{2.2}$$

where ε_0 and ε_r are dielectric constant, and relative permittivity respectively. The interconnect inductance equation is from the predictive technology model [52]

$$L = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + 0.5 + \frac{0.22(w+t)}{l}\right] \tag{2.3}$$

where μ_0 is the permeability in free space.

Another approach for determining the per unit length parameters is to use 2-D and 3-D electro-magnetic field-solvers [50], [53]. In HSPICE the physical parameters of interconnect based on latest technology can be given to extract the electrical R, L, C parameters. Field solver provides better accuracy when compared to analytical formulas at the expense of computational complexity. Once the electrical parameters are identified, it is necessary to develop a model to estimate the delay. There are several closed form interconnect models which have been developed over the years. Next section will discuss some of those closed form models.

2.3 Introduction to Closed Form Interconnect Modeling

Analysis of on-chip interconnects are based on either simulation techniques or closed-form analytic formulas. When it comes to modeling of on-chip interconnects for signal integrity verification, the most important difficulty is the numerical integration problem. This is because the distributed interconnects are best described by Telegraphers partial differential equations which can provide an exact transfer function for the far end response in the frequency domain only. However it does not have an exact time domain representation. To provide an accurate time domain representation, numerical integration techniques [54] are required at every time step. Simulation tools such as SPICE use numerical integration or convolution techniques at every time step to provide accurate results. However, these techniques are computationally expensive to be used in layout optimization [34].

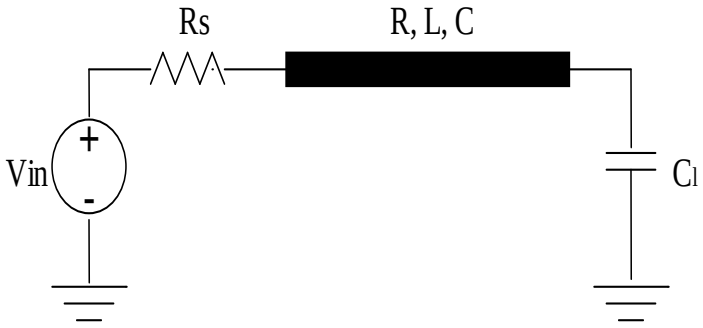


Fig. 2.3: Circuit Model for Single Line Interconnect

For an iterative layout design of densely populated integrated circuits composed of hundred millions of gates, accurate analytic models are needed to efficiently predict the delay and rise times of interconnects. One of the traditional methods was to express the frequency domain transfer function of interconnects as a simple rational function which could then be converted to poles and residues form [12]-[14], [31]-[33]. As poles and residues have a direct representation in the time domain, the interconnect response can now be evaluated without numerical integration at every time step. Using this idea, on-chip interconnects were analyzed as single-pole Elmore-based RC models [6], [12]-[14] to estimate signal delay at early stages. In current integrated circuit designs, wire inductance can no longer be ignored due to higher operating speeds and longer electrical line lengths. Thus, analytic RLC interconnect models are required to efficiently characterize the signal responses of today's high-performance integrated circuits.

All of the above factors contribute to make on-chip interconnect modeling highly challenging. Closed form models are important because of their simplicity while maintaining reasonable accuracy as compared to SPICE. The next section deals with various closed form models proposed in the literature.

2.4 Review of Closed Form RLC Interconnect Models

2.4.1 Frequency Domain Representation of Transfer Function

The analysis of on-chip RLC interconnects starts with Telegraphers equation in frequency domain. All closed form RLC models assume a quasi-TEM mode of signal propagation. This means that the effect of imperfect line conductors and inhomogeneous surrounding medium resulting in a component of the mutually transverse electric and magnetic fields along the line axis is considered negligible [3]. The Telegrapher's equations are a pair of linear differential equations which describe the voltage and current on a transmission line with distance and time. The equations come from Oliver Heaviside who in the 1880s developed the transmission line model. These equations are [55]

$$\frac{\partial}{\partial x}V(x,s) = -(R + sL)I(x,s)$$
$$\frac{\partial}{\partial x}I(x,s) = -sCV(x,s) \tag{2.4}$$

where s is Laplace transform variable, x is the position variable; $V(x,s)$ and $I(x,s)$ represent the voltage and current of the transmission line respectively in the frequency domain; R, L and C are the per-unit-length resistance, inductance and capacitance respectively. The per unit length conductance G is assumed to be negligible for on-chip interconnects. The solution of (2.4) can be expressed using the exponential matrix as

$$\begin{bmatrix} V(l,s) \\ -I(l,s) \end{bmatrix} = e^{\Phi l}\begin{bmatrix} V(0,s) \\ I(0,s) \end{bmatrix} \tag{2.5}$$

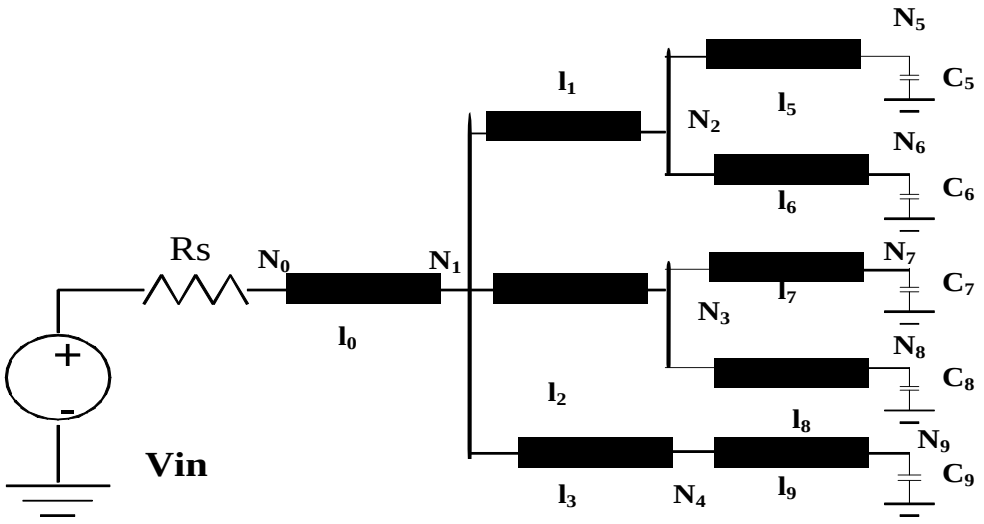


Fig. 2.4: Circuit Model Tree Structure Interconnects

where $$\Phi = \begin{bmatrix} 0 & -Z \\ -Y & 0 \end{bmatrix} \tag{2.6}$$

$Z=R+sL$, $Y=sC$ and l is the length of the transmission line. The exponential matrix of (2.5) can be expressed using the *cosh* and *sinh* functions as shown below [55]:

$$\begin{bmatrix} V(l,s) \\ -I(l,s) \end{bmatrix} = \begin{bmatrix} \cosh(\, l\sqrt{ZY}\,) & -Y_0^{-1}\sinh(l\sqrt{YZ}\,) \\ -Y_0\sinh(l\sqrt{YZ}\,) & \cosh(l\sqrt{ZY}\,) \end{bmatrix} \begin{bmatrix} V(0,s) \\ -I(0,s) \end{bmatrix} \tag{2.7}$$

where $Y_0 = Y(\sqrt{YZ}\,)^{-1}$. Now we look the circuit network for a RLC interconnect line which is shown in Fig. 2.3. This represents a point-to-point interconnection driven by a transistor (modeled as voltage source V_{in} serially connected to a linear resistance R_s) and connected to the next gate (modeled as a capacitance C_l) and is commonly used in VLSI design theory [17]-[30]. Considering this interconnect circuit as shown in Fig. 2.3, the boundary conditions are represented as

$$V_{in} = V(0,s) + R_s I(0,s) \tag{2.8}$$

$$V(l,s) = -sC_l I(l,s) \tag{2.9}$$

Using (2.7)-(2.9), the far end transient response of single line interconnect can be described as

$$V_f = \frac{V_{in}}{(1+sR_sC_l)\cosh(\Gamma) + (R_sY_0 + sC_lY_0^{-1})\sinh(\Gamma)} \tag{2.10}$$

where $\Gamma = (l\sqrt{YZ})$.

Figure 2.4 shows an example of a distributed RLC tree which is often used to analyze clock distribution networks. In that example, a driver with an output resistance is R_s connected to the root of the tree N_0. All of the output nodes (N_5.....N_9) are called leaves and connected with load buffers which can be used to drive the *RLC* trees in the next level. The load buffers are modeled by capacitors. All of the branches in the tree are represented by distributed RLC lines. The tree can be balanced or unbalanced; but unbalanced trees exhibit more complex characteristics than balanced trees [41].

The output voltage V_{out}^i from the voltage source to a certain node N_i is [41],

$$V_{out}^i = \frac{V_{in} \cdot Z_{L,0}}{R_d + Z_{L,0}} \prod_k \frac{1}{\cosh(\Gamma_k) + (Z_{0,k} / Z_{L,k})\sinh(\Gamma_k))} \tag{2.11}$$

where Γ_k and $Z_{0,k}$ are the propagation operator and characteristic impedance of the k^{th} line, respectively; $Z_{L,k}$ is the input impedance observed at node N_k, and k is the index

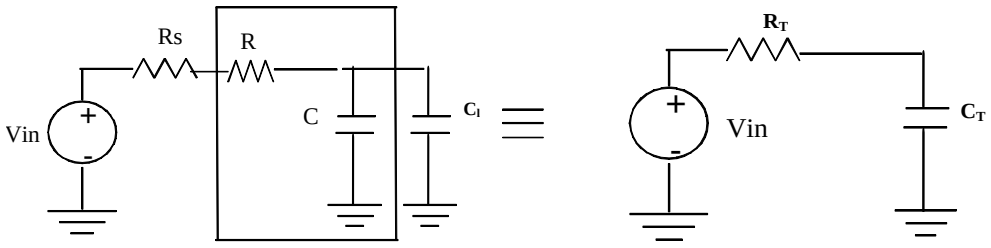


Fig. 2.5: Circuit model of Elmore RC interconnect.

following each branch in the path from node N_0 to N_i. If node N_j branches out to a single interconnect k (such as nodes N_4 of Fig. 2.4), then the input impedance $Z_{L,j}$ is defined as

$$Z_{L,j} = Z_{0,k} \frac{Z_{L,k} \cosh \Gamma_k + Z_{0,k} \sinh \Gamma_k}{Z_{0,k} \cosh \Gamma_k + Z_{L,k} \sinh \Gamma_k} \tag{2.12}$$

If node N_j branched out to multiple interconnects (such as node N_1 of Fig. 2.4), then the input impedance $Z_{L,j}$ at node N_j is the parallel combination of the input impedances of the downstream branches which are connected to node N_j.

These transfer functions of single line and tree structure interconnect (2.10), (2.11) have no direct representation in the time domain and thus real-time prediction of delay of RLC interconnects. Various closed form models [12]-[14], [31]-[41] were developed to provide efficient representation of (2.10)-(2.12) in time domain and will be now discussed.

2.4.2 Elmore Delay Based Models (Single Pole Model)

One of the earliest and popular models for SI verification in interconnects was the Elmore delay based models as proposed in [12]. For ease of presentation without loss of

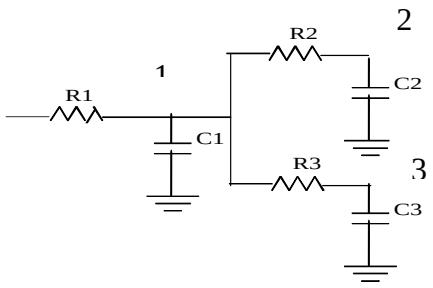


Fig. 2.6: Circuit Model Elmore RC Tree Structure Interconnects

generality, each interconnect is explained as simple lumped RC circuits as shown in Fig. 2.5. This model is commonly used in VLSI design theory [17]-[30].

Transfer function of such RC circuit is given by

$$H(s) = \frac{1}{(1 + sR_T C_T)} \tag{2.13}$$

where $R_T = R_s + R$ and $C_T = C_l + C$ are the total interconnect resistances and capacitances respectively which includes sources resistance and load capacitance. Now if the input is a unit step function, then the time domain solution is given by

$$V_{out}(t) = (1 - \exp(-t / T_D) \tag{2.14}$$

where T_D represents the time constant which is $R_T C_T$.

Elmore model is particularly appealing for tree structure interconnects where each interconnect in tree structure is considered as lumped RC circuits which is shown in Fig. 2.6. The transfer function of such tree structure at node *i* is given by

$$H(s) = \frac{1}{(1 + s\sum_k C_k R_{ik})} \tag{2.15}$$

where k is the index that covers every capacitor in the circuit; R_{ik} is the common resistance respectively, from the input to the node i and k [12],[56]. This first-order approximation matches the first moment of the transfer function at node i but approximates the higher-order moments by

$$m_i = \left(-\sum_k C_k R_{ik} \right)^i \tag{2.16}$$

as seen by the expansion

$$H(s) = 1 + m_1 s + m_2 s^2 + ... = 1 - s\left(-\sum_k C_k R_{ik} \right) + s^2 \left(-\sum_k C_k R_{ik} \right)^2 + ... \tag{2.17}$$

Elmore model is basically single pole model (first order approximation).There is a simple closed-form solution for the time constant T_{D_i} for the tree shown in Fig. 2.6. The time constant at node i is given by

$$T_{D_i} = \sum_k C_k R_{ik} \tag{2.18}$$

The equation of 50% delay for unit step input becomes

$$t_{50\%} = 0.693 T_D \tag{2.19}$$

Since, the delay of an exponential function of (2.14) is well defined and easy to analyze, this model was very popular among circuit designers. However, this model does not consider inductance effect which is very obvious when modern switching speeds touched the GHz range. As a result transient response of interconnects may become non

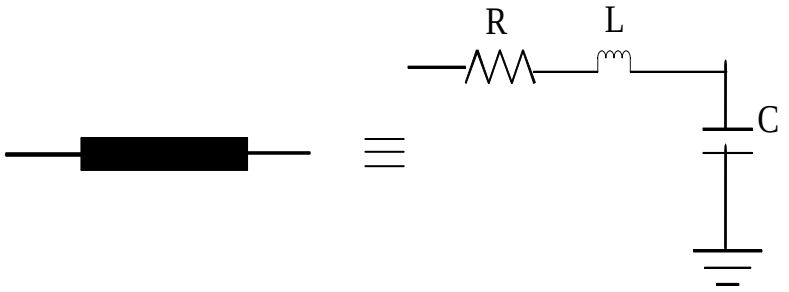


Fig. 2.7: Lumped RLC Section for Equivalent Elmore Delay

monotonic due to the large line inductances. For such cases instead of RC model, RLC models (two pole) or even multi-pole models are required.

2.4.3 Equivalent Elmore Delay Model (Two Pole Lumped Model)

The transfer functions of (2.10) and (2.11) include hyperbolic functions of the complex frequency variable *s* and do not have a direct representation in the time domain. This makes it difficult to analytically predict the signal delay of interconnect networks. As a result the extension of equivalent two-pole Elmore delay models for RLC tree networks is developed in [42]-[43],[56]. For the case of two pole lumped model [56], single line interconnect is represented as lumped resistive-inductive-capacitive (RLC) elements as shown in Fig. 2.7. As a result, the circuit of Fig. 2.7 has second order transfer function which is given by

$$H(s) = \frac{1}{LCs^2 + RCs + 1} \tag{2.20}$$

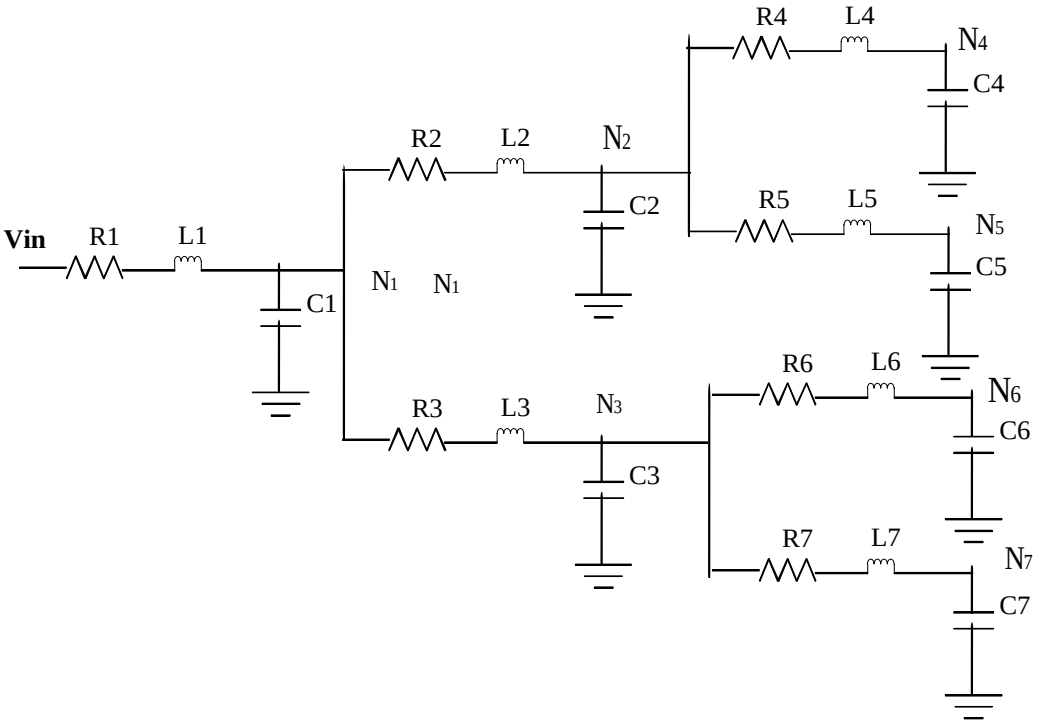


Fig. 2.8: Circuit model for lumped *RLC* trees

This transfer function is expressed in terms of its damping factor ζ and natural frequency ω_n as

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.21}$$

where

$$\zeta = \frac{RC}{2\sqrt{LC}} \qquad \& \qquad \omega_n = \frac{1}{\sqrt{LC}} \tag{2.22}$$

The poles of the transfer function of (2.21) are

$$P_{1,2} = \omega_n(-\zeta \pm \sqrt{\zeta^2 - 1}\ ) \tag{2.23}$$

For the case of tree structure network, each interconnect in the tree is modeled as lumped resistive-inductive-capacitive (RLC) elements, as shown in Fig. 2.8. Typically, moment matching techniques are used to express the transfer functions of this tree structure interconnect as a power series [43]

$$H(s) = \frac{V_{out}}{V_{in}} \approx 1 + m_1 s + m_2 s^2 \approx \frac{1}{1 + b_1 s + b_2 s^2} \tag{2.24}$$

where the moments m_j are

$$m_j = \frac{1}{j!} \cdot \frac{d^j H(s)}{ds^j}, \qquad j = 1,2,.... \tag{2.25}$$

and

$$b_1 = -m_1 \;\; b_2 = m_1^2 - m_2 \tag{2.26}$$

The first two moments of this tree network at node N_j can be calculated using the following simple closed-form expressions [56] where first moment is similar to equation (2.16) of RC circuit of Fig. 2.8.

$$m_1^i = \sum_k C_k R_{ik} \tag{2.27}$$

$$m_2^i = \left(\sum_k C_k R_{ik} \right)^2 - \sum_k C_k L_{ik} \tag{2.28}$$

where k is the index that covers every capacitor in the circuit; R_{ik} and L_{ik} are the common resistance and inductance, respectively, from the input voltage node to node N_i and N_k [56].

For the general RLC tree shown in Fig. 2.8, the voltage drop at any node as N_i compared to the input voltage is

$$V_{in}(s) - V_i(s) = \sum_k C_k V_k(s) s(R_{ki} + L_{ki} s) \tag{2.29}$$

If the input is a unit impulse, $V_{in}(s)$ is equal to 1.0 and the voltages at the nodes of the tree are the unit impulse responses of these nodes. Thus, the normalized transfer function $g_i(s)$ at node N_i of tree structure is given by $V_i(s)$ and is

$$g_i(s) = 1 - \sum_k C_k V_k(s) s(R_{ki} + L_{kI} s) \tag{2.30}$$

Using the moment matching techniques ω_{n_i} and ζ_i at this transfer function of node N_i of general tree structure is given by

$$\zeta_i = \frac{\sum_k C_k R_{ik}}{2\sqrt{\sum_k C_k L_{ik}}} \qquad \& \qquad \omega_{ni} = \frac{1}{\sqrt{\sum_k C_k L_{ik}}} \tag{2.31}$$

The time constants RC and $\sqrt{LC}$ in single line structure are replaced by the summations of the equivalent time constants in the tree structure.

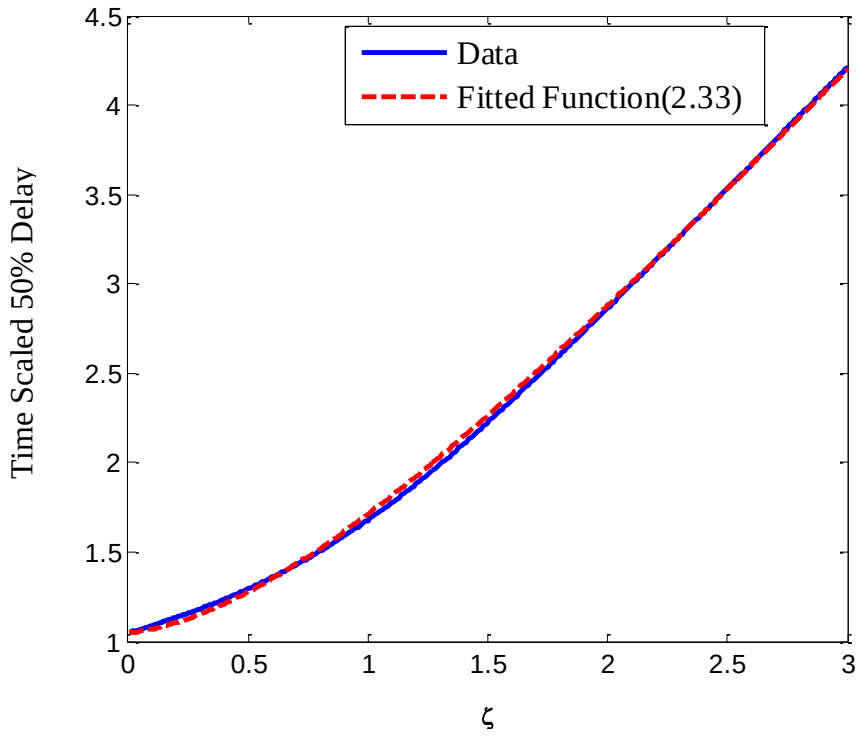
Once the transfer function of single line or tree structure interconnect is obtained in the form of damping factor and natural frequency, the time domain response of (2.21) for a step input with supply voltage of V_{DD} is given by

$$V_{out}(t_n) = V_{DD} + \frac{V_{DD}}{2\sqrt{\zeta^2 - 1}}\left(\frac{e^{t_n(-\zeta+\sqrt{\zeta^2-1})}}{-\zeta+\sqrt{\zeta^2-1}} - \frac{e^{t_n(-\zeta-\sqrt{\zeta^2-1})}}{-\zeta-\sqrt{\zeta^2-1}} \right) \tag{2.32}$$

where t_n is a dimensionless time variable defined as $t_n = t\omega_n$. The output voltage of (2.32) is a nonlinear function with respect to the variable ζ. As a result, an analytic formula is not directly available for the 50% delay since the solution of (2.32) is obtained iteratively using methods such as Newton-Rhapson's method. For this reason, (2.32) is solved for various values of ζ by setting V_{out} to $0.5V_{DD}$ and solving for t_n. Fig. 2.9 plots the time scaled 50% delay for various values of ζ. The results of this analysis are stored and fitted to the following functions [56]

$$t_{50\%} = (1.047e^{-\zeta/0.85} + 1.39\zeta)/\omega_n \tag{2.33}$$

where $t_{50\%}$ corresponds to 50% delay with respect to time *t*. This equation is like the extension of 50% delay of single pole Elmore model of (2.19) considering inductance effect of the interconnect. Equation (2.32) can also be used to calculate the rise time by setting V_{out} to $0.1V_{DD}$ and $0.9V_{DD}$ and solving t_n for different values of ζ. Fig. 2.10 plots the time difference of V_{out} to reach $0.1V_{DD}$ to $0.9V_{DD}$. Similar fitted expressions can also be obtained for the rise time response [56].



2.9: Time Scaled 50% delay versus ζ

So the expression of rise time is given by [56]

$$t_r = (6.017e^{-\zeta^{1.35}/0.4} - 5e^{-\zeta^{1.25}/0.64} + 4.39\zeta)/\omega_n \qquad (2.34)$$

where t_r corresponds to the rise time.

2.4.4 Two Pole Distributed RLC Interconnect Model

The exact transfer function of single line and distributed *RLC* trees are hyperbolic, but very complicated. In [43], the accuracy of the two pole model is improved by directly approximating the distributed hyperbolic functions of (2.10) and (2.11) as a power series

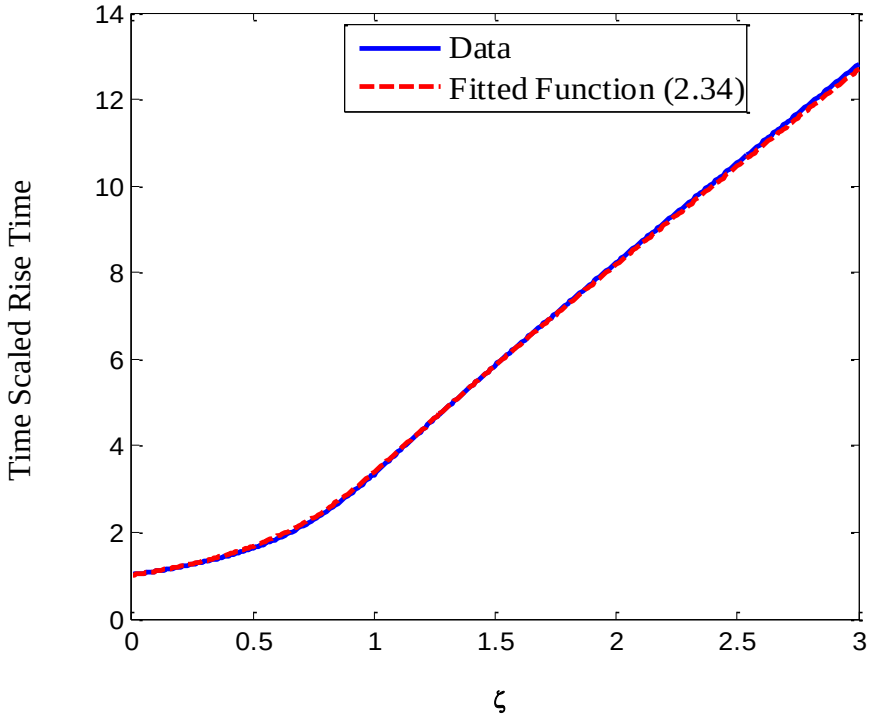


Fig. 2.10: Time Scaled rise time versus ζ

$$\cosh\Gamma_k \approx 1+\frac{1}{2!}R_kC_kl_k^2s+(\frac{1}{2!}L_kC_kl_k^2+\frac{1}{4!}R_k^2C_k^2l_k^4)s^2 \tag{2.35}$$

$$Z_{0,k}\sinh\Gamma_k \approx R_kl_k+(L_kl_k+\frac{1}{3!}R_k^2C_kl_k^3)s+(\frac{2}{3!}R_kL_kC_kl_k^3+\frac{1}{4!}R_k^3C_k^2l_k^5)s^2 \tag{2.36}$$

$$Z_{0,k}^{-1}\sinh\Gamma_k \approx C_kl_ks+(\frac{1}{3!}C_k^2R_kl_k^3)s^2 \tag{2.37}$$

to convert the transfer function to the form of (2.24) as

$$H(s)=\frac{1}{1+b_1s+b_2s^2} \tag{2.38}$$

where

$$\zeta = \frac{b_1}{2\sqrt{b_2}} \qquad \& \qquad \omega_n = \frac{1}{\sqrt{b_2}} \tag{2.39}$$

In [43], it is shown that the Maclaurin series approximation from (2.35)-(2.37) to obtain the moments of the transfer function of (2.38) are more accurate than the moments calculated from the lumped model since the distributed RLC model are directly derived from the hyperbolic functions of (2.10) and (2.11). Once the transfer function of (2.38) is derived the fitted expressions of (2.33) and (2.34) can be used to analytically calculate the 50% delay and the rise time.

Elmore based models such as the fitted expression of (2.33) & (2.34) are widely used in VLSI circuit design for fast delay estimation due to its computational efficiency. However, the accuracy of Elmore models is limited since two poles may not be accurate enough to capture the high frequency effects and signal delays of RLC lines. The next chapter provides a methodology to improve Elmore based two pole model of RLC interconnects by extracting the delay from the transfer function.

Chapter 3

Delay Extraction Based Equivalent Elmore Model For RLC On-Chip Interconnects

3.1 Abstract

In this chapter a delay extraction algorithm is utilized to improve the accuracy of two-pole Elmore based models used in the analysis of on-chip distributed RLC interconnects. In the proposed scheme, the time of flight signal delay is extracted without increasing the number of poles or affecting the stability of the transfer function. This algorithm is used for both unit step and ramp inputs. From the analysis, analytic fitted expressions are obtained for the 50% delay and rise time for unit step input. For ramp input, a lookup table can be created for the 50% delay and rise time. Since the time of flight delay is extracted from the transfer function, the proposed algorithm provides a mechanism to improve the accuracy of two-pole Elmore-based models without significantly increasing the computational complexity.

Elmore based models rely on one or two-pole transfer functions to estimate the delay. As a result, these approximations are not capable of capturing the early transient responses required for predicting long signal delays and rise times caused by inductive dominant on-chip interconnects.The proposed model basically extends the concepts of two pole model [43], [56] to obtain the time domain analysis for any balanced and unbalanced complex tree structures using delay extraction techniques. The transfer

function is obtained analytically in terms of predetermined coefficients and the per unit length parameters. As a result, the proposed model provides a mechanism to improve the accuracy for cases when inductive effects are significant, length of the line increases or when rise time of the signal becomes sharper. The algorithm is used for various single and tree structures interconnect scenarios for both unit step and ramp inputs.

The organization of the chapter is as follows: Section 3.2 develops the proposed delay extraction based equivalent Elmore model for unit step input. Analytic fitted expressions have been obtained for calculating 50% delay and rise time. Then the model is extended for ramp inputs in section 3.3 where prediction of 50% delay and rise time has also been discussed.

3.2 Proposed Model for Unit Step Input

Even though Elmore based models have limited accuracy, they are still commonly used to analyze integrated circuits composed of millions of gates, since it is often impractical and time consuming to use accurate modeling techniques to evaluate the signal delay at each node in the circuit The objective of this work is to use a delay extraction algorithm to improve the accuracy of this Elmore-based models for RLC interconnects.

3.2.1 Extracting Time of Flight Delay

As illustrated in chapter 2, moment matching techniques are used to express the transfer functions of on-chip RLC interconnect as follows [43]

$$H(s) = \frac{1}{1 + b_1 s + b_2 s^2} \tag{3.1}$$

Equation (3.1) usually refers to Elmore based two pole model. The proposed algorithm uses a delay extraction based rational approximation to improve the accuracy of (3.1). The first two moments of (3.1) are calculated using the same conventional moment matching techniques such as the methodologies described in section 2.4.3 and 2.4.4. In this paper, the procedure outlined in [43] is used since the hyperbolic approximations of (2.35)-(2.37) were shown to be more accurate than the lumped model moment calculations of (2.27)-(2.28). Once, the moments of the transfer function are calculated, the time of flight delay T_d is extracted from (2.21) as proposed in [57] to obtain

$$H(s) \approx \frac{\omega_n^2 \cdot \left(1 + sT_d + 0.5 s^2 T_d^2\right) \cdot e^{-sT_d}}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.2}$$

where $1 + sT_d + 0.5 s^2 T_d^2$ corresponds to a Maclaurin series approximation of e^{sT_d}. The delay operator e^{-sT_d} ensures that the voltage at the far end appears only after the time-of-flight delay T_d. Furthermore, the Maclaurin series approximation of e^{sT_d} only changes the numerator of (3.2) and does not increase the number of poles or affect the stability of the transfer function. For the interconnect network of Fig. 2.3, a lower bound estimate of the time of flight delay is

$$T_d = l\sqrt{LC} \tag{3.3}$$

which corresponds to the propagation delay of a lossless line. This provides a reasonable

estimate of the amount of delay that should be extracted from (3.2), since the voltage signal at the far end can only appear after T_d delay has occurred with respect to the input voltage at the near end [57]. For the interconnect tree network of Fig. 2.4, a lower bound estimate of the time of flight delay at node N_i is calculated as a summation of propagation delay of lossless lines as

$$T_d^i = \sum_k l_k \sqrt{L_k C_k} \tag{3.4}$$

where k is the index following each branch in the path from node N_0 to N_i. The time domain response of (3.2) corresponding to a step input with supply voltage of V_{DD} can be expressed as

$$V_{out}(t_n) = V_{DD}\left(1 + K_1 e^{-t_n(\zeta+\sqrt{\zeta^2-1})} + K_2 e^{-t_n(\zeta-\sqrt{\zeta^2-1})}\right)u(t_n) \tag{3.5}$$

where

$$K_1 = \frac{1-\tau(\zeta+\sqrt{\zeta^2-1})+0.5\tau^2(\zeta+\sqrt{\zeta^2-1})^2}{2(\sqrt{\zeta^2-1})(\zeta+\sqrt{\zeta^2-1})} \tag{3.6}$$

$$K_2 = \frac{-1+\tau(\zeta-\sqrt{\zeta^2-1})-0.5\tau^2(\zeta-\sqrt{\zeta^2-1})^2}{2(\sqrt{\zeta^2-1})(\zeta-\sqrt{\zeta^2-1})} \tag{3.7}$$

The coefficient $u(t_n)$ is the unit step response, $t_n = (t - T_d)\omega_n$ and $\tau = T_d\omega_n$. The output voltage of (3.5) is zero for $t < T_d$ due to the unit step. At $t = T_d$, the value of (3.5) will depend on the normalized extracted delay variable τ. When $\tau = 0$, (3.5) reduces to

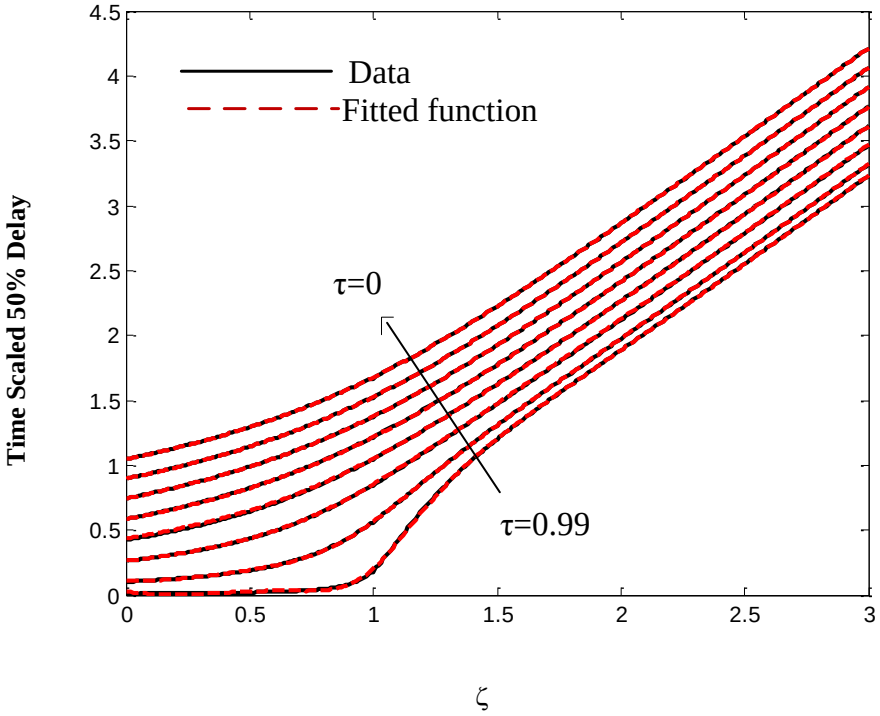


Fig. 3.1 The time scaled 50% delay for different values of τ and ζ

the equation of (2.32).

To calculate the 50% delay requires solving the nonlinear function of (3.5) for specific values of ζ and τ. Fig. 3.1 shows the solution of (3.5) for various values of ζ and τ by setting V_{out} to $0.5V_{DD}$ and solving for t_n. The results of this analysis can be stored or fitted to some function to obtain quick estimates of the 50% delay. Let the fitted function be defined as $f_{50\%}(\zeta,\tau)$. Thus, the 50% delay with respect to time *t* can be calculated as

$$t_{50\%} = T_d + \frac{f_{50\%}(\zeta,\tau)}{\omega_n} \tag{3.8}$$

Note, when the time of flight delay is not extracted (i.e. $\tau = 0$), the fitted expression of $f_{50\%}(\zeta,\tau)$ will give similar 50% delay predictions as (2.33).

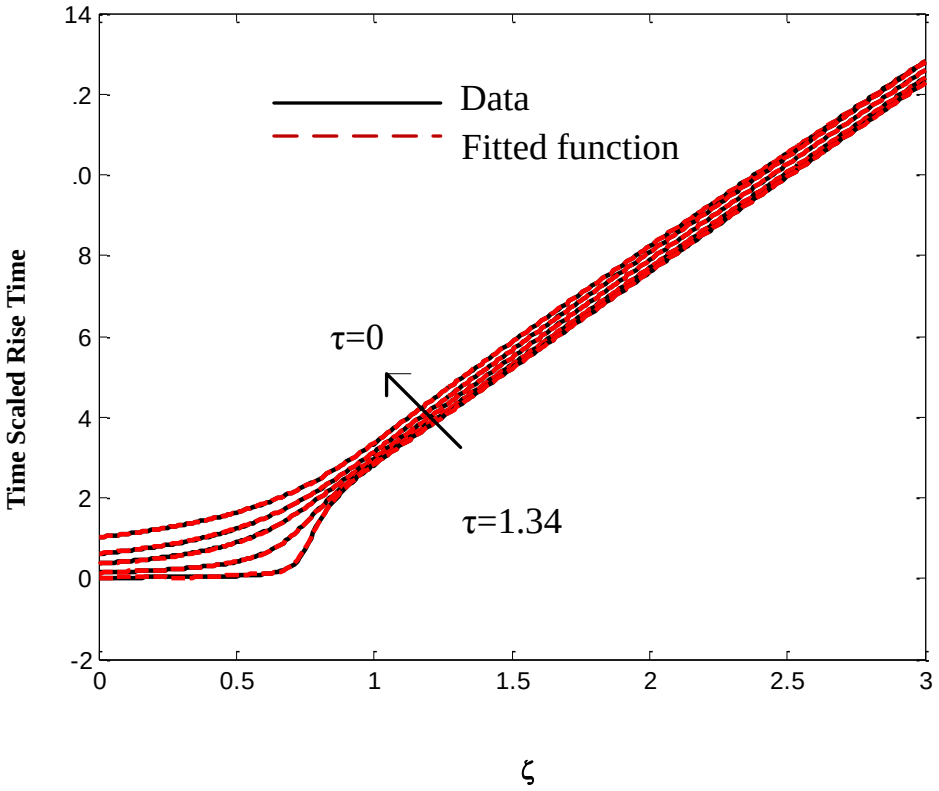


Fig. 3.2 The time scaled rise time for different values of τ and ζ

Equation (3.5) can also be used to calculate the rise time by setting V_{out} to $0.1V_{DD}$ and $0.9V_{DD}$ and solving t_n for different values of ζ and τ. The results of this analysis are shown in Fig. 3.2 which plots the time difference of V_{out} to reach $0.1V_{DD}$ to $0.9V_{DD}$. Let the fitted function for the rise time be defined as $f_{rise}(\zeta,\tau)$. Thus the rise time with respect to time *t* can be calculated as

$$t_{rise} = \frac{f_{rise}(\zeta,\tau)}{\omega_n} \tag{3.9}$$

Section 3.2.2 discusses how $f_{50\%}(\zeta,\tau)$ and $f_{rise}(\zeta,\tau)$ are fitted to the data values of Fig.

3.1 and Fig. 3.2, and how these functions are used to calculate the 50% delay and rise times.

3.2.2 Fitted Functions for $f_{50\%}(\zeta,\tau)$ and $f_{rise}(\zeta,\tau)$

The numerical solutions for the 50% delay is fitted to rational functions for specified ranges of τ as

$$f_{50\%}(\zeta,\tau)=\begin{cases} N_1/D_1 & 0\le\tau\le 0.2 \\ N_2/D_2 & 0.2<\tau\le 0.4 \\ N_3/D_3 & 0.4<\tau\le 0.6 \\ N_4/D_4 & 0.6<\tau\le 0.8 \\ N_5/D_5 & 0.8<\tau\le 0.9 \\ N_6/D_6 & 0.9<\tau\le 0.99 \\ 0 & \tau\ge 1 \end{cases} \tag{3.10}$$

where N_i and D_i are defined as polynomials with respect to ζ ,

$$N_i = a_{i,0}+a_{i,1}\zeta+a_{i,2}\zeta^2+a_{i,3}\zeta^3+a_{i,4}\zeta^4$$

$$D_i = b_{i,0}+b_{i,1}\zeta+b_{i,2}\zeta^2+\zeta^3 \tag{3.11}$$

and $a_{i,j}$ and $b_{i,j}$ are polynomials with respect to τ ,

$$a_{i,j}=\alpha_{i,j,0}+\alpha_{i,j,1}\tau+\alpha_{i,j,2}\tau^2+\alpha_{i,j,3}\tau^3$$

$$b_{i,j}=\beta_{i,j,0}+\beta_{i,j,1}\tau+\beta_{i,j,2}\tau^2+\beta_{i,j,3}\tau^3 \tag{3.12}$$

The coefficients of $\alpha_{i,j,k}$ and $\beta_{i,j,k}$ are listed in Table 3.1 and Table 3.2. The curve fitting for $f_{50\%}(\zeta,\tau)$ is only performed up to $\tau\le 0.99$ since the variance of $f_{50\%}(\zeta,\tau)$ is

significant when ζ is high and the extracted delay ranges from $0.99 < \tau < 1$. As a result, higher order rational approximations would be required to fit $f_{50\%}(\zeta, \tau)$ from $0.99 < \tau < 1$.

From (3.5), when $\tau \geq 1$, the output voltage at $t = T_d$ is $V_{out}(t = T_d) \geq 0.5V_{DD}$ for all values of ζ. Thus $f_{50\%}(\zeta, \tau) = 0$ for $\tau \geq 1$ and the 50% delay predicted by (3.8) is mainly due to the extracted delay (i.e. $t_{50\%} = T_d$). As a result, (3.8) will underestimate the 50% delay when $\tau \geq 1$ since this calculation does not include the effects of the per-unit-length resistance *R*, series resistance R_s and load capacitor C_l. The proposed model can provide different 50% delay estimates by modifying (3.8) to extract different amounts of delay as

$$t_{50\%} = kT_d + \frac{f_{50\%}(\zeta, k\tau)}{\omega_n} \tag{3.13}$$

where *k* is a scaling factor selected to ensure that $k \cdot \tau$ is less than one or falls within the ranges of the fitted function $f_{50\%}(\zeta, \tau)$. The scaling factor *k*, enables a smaller delay to be extracted from (3.2) instead of using (3.3)-(3.4). When *k* is set to zero, the 50% delay predicted by (3.13) is similar to (2.33) (i.e. zero delay is extracted from (3.2)).

To calculate the 50% delay the following rule of thumb is followed, which attempts to include the effects of the per-unit-length resistances, series resistance and load capacitors for cases when τ is close to one or over one.

$$
\begin{aligned}
& t_{50\%} = T_d + \frac{f_{50\%}(\zeta,\tau)}{\omega_n} && 0 \le \tau \le 0.98 \\
& \left.\begin{aligned}
& \textit{if} \left(T_x = kT_d + \frac{f_{50\%}(\zeta, k\tau = 0.98)}{\omega_n} \right) > T_d \\
& \quad t_{50\%} = T_x \\
& \textit{else} \\
& \quad t_{50\%} = T_d + \frac{f_{50\%}(\zeta,\tau = 0.98)}{\omega_n}
\end{aligned}\right\} && \tau > 0.98
\end{aligned}
\tag{3.14}
$$

If the extracted delay using (3.3) and (3.4) causes $\tau \le 0.98$, then (3.14) uses (3.8) to calculate the 50% delay. If extracted delay using (3.3) and (3.4) causes $\tau > 0.98$, then (3.13) is used, where the scaling factor *k* is selected such that $k \cdot \tau = 0.98$. The scaling factor *k*, allows a smaller delay to be extracted such that the output voltage at the extracted delay is $V_{out}(t = kT_d) < 0.5V_{DD}$ and the transition period to reach $V_{out} = 0.5V_{DD}$ includes the impediments of the per-unit-length resistances, series resistance and load capacitors. However, when ζ is low, the 50% delay predicted by (3.13) may yield $t_{50\%} < T_d$, which is not physically possible since the voltage at the far end can only appear after T_d delay has occurred with respect to the input voltage at the near end [57]. As a result, (3.13) is only used when $t_{50\%} > T_d$, otherwise the 50% delay should be slightly over T_d and is estimated using

$$
t_{50\%} = T_d + \frac{f_{50\%}(\zeta,0.98)}{\omega_n} \tag{3.15}
$$

Note that both (3.13) and (3.15) use $f_{50\%}(\zeta,0.98)/\omega_n$. When the contribution of $f_{50\%}(\zeta,0.98)/\omega_n$ is significant, (3.14) uses (3.13) to calculate the 50% delay since this

will make $t_{50\%} > T_d$. When (3.13) does not satisfy $t_{50\%} > T_d$, the contribution of $f_{50\%}(\zeta,0.98)/\omega_n$ is relatively low and (3.14) uses (3.15) to calculate the 50% delay. This usually corresponds to an inductive-capacitive dominant network, where low values of ζ cause $f_{50\%}(\zeta,\tau)$ to decrease (see Fig. 3.2). In this scenario, the 50% delay is mainly due to T_d as predicted by (3.2). However, $t_{50\%} = T_d$ does not include the delay influences due to the per-unit-length resistances, series resistance and load capacitors. To improve the 50% delay estimate, the function of $f_{50\%}(\zeta,0.98)/\omega_n$ is added to (3.15) to include these effects.

The numerical solutions for the rise time is also fitted to rational functions for specified ranges of τ as

$$f_{rise}(\zeta,\tau) = \begin{cases} N_{r1}/D_{r1} & 0 \le \tau \le 0.22 \\ N_{r2}/D_{r2} & 0.22 < \tau \le 0.44 \\ N_{r3}/D_{r3} & 0.44 < \tau \le 0.88 \\ N_{r4}/D_{r4} & 0.88 < \tau \le 1.11 \\ N_{r5}/D_{r5} & 1.1 < \tau \le 1.33 \\ 0 & \tau \ge \sqrt{1.8} \approx 1.34164 \end{cases} \tag{3.16}$$

where N_{ri} and D_{ri} are defined as polynomials with respect to ζ,

$$N_i = a^r_{i,0} + a^r_{i,1}\zeta + a^r_{i,2}\zeta^2 + a^r_{i,3}\zeta^3 + a^r_{i,4}\zeta^4 + a^r_{i,5}\zeta^5$$

$$D_i = b^r_{i,0} + b^r_{i,1}\zeta + b^r_{i,2}\zeta^2 + b^r_{i,3}\zeta^3 + \zeta^4 \tag{3.17}$$

The coefficients of $\alpha^r_{i,j,k}$ and $\beta^r_{i,j,k}$ are listed in Table 3.3 and Table 3.4. Once

TABLE 3.1

COEFFICIENTS OF $\alpha_{i,j,k}$

	j / i	0	1	2	3	4
$\alpha_{i,j,0}$	1	9.0213028957213	-0.52002231195006	2.362101690758197	0.563191990612	1.5823872352561
	2	10.264566953478	-0.01554390322000	2.889071463278857	0.515067856181	1.6365812921766
	3	-47.403528389451	-28.9764859689464	-0.24685990745238	-5.06587672519	-1.575542571587
	4	28.301840842192	22.330160625387	21.320139866462	4.598199829119	0.8502852216206
	5	-7.258203818329	12.335321069538	5.3248058863799	2.738184077116	6.9296294393022
	6	-72.08103057783	266.7515835824658	-588.9864706708	263.3430338481	105.26207953608
$\alpha_{i,j,1}$	1	-8.460788071761	3.527738691827600	-1.7868530539725	-0.97340830311	-0.001476898823
	2	-23.763788517414	-2.43306934956625	-8.009374173386924	-0.0478945946	-0.666681240706
	3	375.34428532929	174.2121228418589	1.652822678320948	24.10166053956	21.540760037651
	4	-114.9076576691	-79.935236347528	-75.846756335463	-7.77235327903	1.1432892251704
	5	26.194560011856	-42.183261662620	-14.127303787700	-3.80762259716	-21.19409267996
	6	236.76163797965	-862.311729251835	1908.9742692272	-847.747237192	-339.9620538476
$\alpha_{i,j,2}$	1	-1.800931248953	1.820487108407566	-0.3707109118679	-0.60059675085	0.0318294704271
	2	62.037520966409	24.62604401962565	23.8285294000543	-6.21876900073	2.7657509228355
	3	-852.2749830443	-324.413412221138	-3.3184912203897	-26.3709828568	-48.14636380131
	4	158.90909929518	95.316631443529	89.8805709580265	0	-0.281304500281
	5	-27.83712400668	47.816120066613	10.7164076440579	-2.03900836353	27.147255070583
	6	-255.8992115893	929.089452295064	-2064.190975158	909.4234548081	371.68478951209
$\alpha_{i,j,3}$	1	0	0	6.85628038835035	2.623426126036	-0.507037343861
	2	-91.77171448885	-27.5772387580119	-24.142229648649	13.66863724912	-4.297057094903
	3	600.73418437215	192.745734773314	212.30514951779	0	34.374880248783
	4	-73.53493736538	-38.3244086145732	-33.761822139158	0	0
	5	8.8870710878002	-18.4157971935378	0	0	-11.25852446795
	6	91.248271078542	-334.087483010346	746.47333554401	-328.308465394	-135.4207979435

TABLE 3.2

COEFFICIENTS OF $\beta_{i,j,k}$

	j / i	0	1	2
$\beta_{i,j,0}$	1	8.613824666908954	-3.662194874735159	1.800930171393833
	2	11.0907141810951	-4.663884458620657	2.158296775716884
	3	-120.417803595699	45.9274611081304	-25.7679758956128
	4	66.4567185897558	-17.7224984722917	2.456712551272433
	5	45.8258199545479	-58.2874787359551	47.2533502346019
	6	865.106915927380	-1516.191451983524	794.283139003956
$\beta_{i,j,1}$	1	-0.041125800063642	0.044012921266307	0.009056451353493
	2	-30.0644860959776	12.516618345750294	-4.127351852794886
	3	845.430085885382	-349.3894030751437	176.2207651699743
	4	-270.2047562906737	99.2746200174789	-6.730200090249853
	5	-175.5203072506074	230.7226058300037	-170.9516301165219
	6	-2825.600818190934	4949.479853335178	-2587.024382123916
$\beta_{i,j,2}$	1	0.848931685396748	-0.976390603880459	-0.215895932808289
	2	122.2343298297111	-53.213270840375664	15.430672176741551
	1	-1803.246519137808	804.8881251324483	-367.5528908864673
	4	369.5919208781667	-166.8330888505323	8.933975900669028
	5	228.6837993326621	-304.6330652436234	209.6315481635663
	6	3086.540266735930	-5396.678649085249	2814.812350348027
$\beta_{i,j,3}$	1	-8.555590763338637	15.492816283283725	-1.424401823057440
	2	-173.3075700068836	89.687578761316317	-20.688116357217538
	1	1222.357545790275	-584.5155107465026	245.5727125667448
	4	-165.6138661891531	83.7630467091441	-4.455887524014941
	5	-97.1122989152980	129.8348632303627	-86.2216925030304
	6	-1124.616807728859	1961.853615936612	-1022.766166738894

TABLE 3.3

COEFFICIENTS OF $\alpha^{r}_{i,j,k}$

	i \ j	0	1	2	3	4	5
$\alpha^{r}_{i,j,0}$	1	1.2322981736182	-1.02851254239	0.1544780170304	2.9987471253908	-5.43742970312	4.2403749733927
	2	0.4658582043758	5.04252481259	-0.473861261572	-01.91383625932	-00.0555777596	6.8352966095538
	3	9.2473810846620	-2.44152823972	7.1291410894606	4.6525976129295	8.31260522763	2.5950529243614
	4	60.751051233061	-6.82853190933	-15.74529428646	227.74330544450	-189.74388506	-18.13626145218
	5	-3.097967296943	-40.5326965521	270.52312191488	-579.7948747913	418.969004604	-4.278333844765
$\alpha^{r}_{i,j,1}$	1	0.0535602969182	-0.08591060253	0.0212101061328	0.0369834200149	-0.04499481714	-0.004271562508
	2	7.0260129032901	-61.8303879145	6.7141654851516	49.766781023873	-54.7674542748	-26.75004218203
	3	-38.90567359365	5.86931381304	-32.14092083415	-14.42776662217	-59.3501454638	9.290153185725
	4	-180.1115617428	27.9782342769	50.436798106717	-679.1557542068	594.900021278	70.945268248786
	5	7.9060921750755	102.124634717	-680.8567216252	1459.9672371948	-1059.78099597	24.044885383982
$\alpha^{r}_{i,j,2}$	1	-0.513896773179	0.93117047841	-0.300871921515	-0.335485277013	0.46401595813	0.0794737390126
	2	-19.76059741067	205.616719055	-23.85574243288	-164.2956079553	181.960463076	90.509780020005
	3	61.667744053475	-6.30146507298	46.169992906718	36.387968565347	76.4031241206	-15.37858725406
	4	177.90254028273	-35.1377851688	-50.60032006604	670.24815870814	-619.809061809	-73.07688479349
	5	-6.367252689053	-86.2830118787	571.24555451821	-1221.884356016	883.352561001	-21.80021893914
$\alpha^{r}_{i,j,3}$	1	0	0	0	0	0	-0.207169708053
	2	14.451083927423	-220.587216502	27.471328652114	175.64002279173	-196.040710448	-100.7340106623
	3	-33.02337993540	3.29885910705	-21.05830460288	-27.66181784236	-26.3074468863	8.3868970411592
	4	-58.47663019594	13.9498217768	15.517205764576	-216.3477486839	209.374194997	24.792022111517
	5	1.6322480078705	24.4804212615	-160.4718572330	342.57240435480	-246.94526132	6.5218033494768

.

TABLE 3.4

COEFFICIENTS OF $\beta_{i,j,k}^{r}$

	i \ j	0	1	2	3
$\beta_{i,j,0}^{r}$	1	1.211587608488638	-2.05162928558536	2.042210218367738	-1.55873699121421
	2	0.941006553918567	5.0916341351250	-7.0921391180348	3.4582160742154
	3	15.2030134924340	-19.9653600923949	15.1646923537146	-2.24391204870225
	4	118.9356701047606	-189.82226531738	168.7864013569272	-83.4171047017991
	5	25.679695629594214	30.6547246848665	-34.8491399807634	70.3858530264564
$\beta_{i,j,1}^{r}$	1	0.049865955329878	-0.10131031092261	0.069914855639354	-0.0193449151565
	2	2.299771444231987	-72.0789519424431	93.1529141271554	-51.4282933696436
	3	-70.2331926651397	91.3348024169421	-67.7938103152162	6.06155422097951
	4	-351.8206993575230	576.164997058308	-512.027493437917	260.023260177533
	5	-67.768457403138896	-102.321271301402	80.82543955094357	-175.22747665975
$\beta_{i,j,2}^{r}$	1	-0.480984435243962	1.037286442945819	-0.76169401640458	0.23556061732040
	2	-5.181830039467304	236.671294917510	-310.485692762809	172.659360608741
	3	114.8036302822211	-151.056199965156	113.0717077967981	-14.3530943765016
	4	346.2181741952572	-579.630350335650	514.9643651807950	-268.22463308389
	5	59.916919772245720	112.2691146368511	-60.3929646698437	143.214782834897
$\beta_{i,j,3}^{r}$	1	0	0	0	0
	2	0	-249.479217857748	336.2350782046465	-189.4561264279
	3	-61.2959007918778	82.3407826839700	-62.3007912140839	-14.353094376501
	4	-113.1515207629811	192.8282518238725	-170.929668734861	90.5602970982523
	5	-17.553248189566055	-41.2628448023109	15.17043729138193	-39.321738444847

again, the curve fitting of $f_{rise}(\zeta,\tau)$ is only performed up to $\tau \le 1.33$ since the variance of $f_{rise}(\zeta,\tau)$ is significant when ζ is high and the extracted delay ranges from $1.33 < \tau < \sqrt{1.8}$. For the rise time calculations, when $\tau \ge \sqrt{1.8}$, the output voltage of (3.5) at $t = T_d$ is $V_{out}(t = T_d) \ge 0.9V_{DD}$ for all values of ζ. This causes the rise time predicted by (3.9) to be $t_{rise} = 0$, due to the unit step in (3.5). To estimate, the transition period of the rise time for $\tau > 1.33$, (3.9) is modified to

$$t_{rise} = \begin{cases} \dfrac{f_{rise}(\zeta,\tau)}{\omega_n} & 0 \le \tau \le 1.33 \\ \dfrac{f_{rise}(\zeta, k\tau = 1.33)}{\omega_n} & \tau > 1.33 \end{cases} \tag{3.18}$$

where is a scaling factor selected such that $k \cdot \tau = 1.33$. When *k* is set to zero, the rise time predicted by $f_{rise}(\zeta,0)/\omega_n$ is similar to the rise time given by (2.34). By using *k* to extract a smaller delay for $\tau > 1.33$, the output voltage of (3.5) is $V_{out}(t = kT_d) < 0.9V_{DD}$ and a transition period for the rise time can be calculated using (3.18).

3.3 Proposed Model for Ramp Input

This section develops the far end time domain response of on-chip RLC interconnect for ramp inputs. From this discussion the way of predicting 50% delay and rise time for ramp input is provided.

3.3.1 Time Domain Solution for Ramp Input

For the case of ramp input, edge rate (i.e., rise or fall) of the input signal V_{in} has to be included. As a result it should be modeled as ramp function such as

$$V_{in}(t) = V_{DD}\frac{tu(t) + (t - t_r)u(t - t_r)}{t_r} \tag{3.19}$$

where t_r is the rise time. The Laplace-domain representation of (3.19) can be expressed as

$$V_{in}(s) = V_{DD}\frac{(1 - e^{-st_r})}{s^2 t_r} \tag{3.20}$$

Using the input signal of (3.20), the time domain response of (3.2) corresponding to a ramp input with supply voltage of V_{DD} can be expressed as

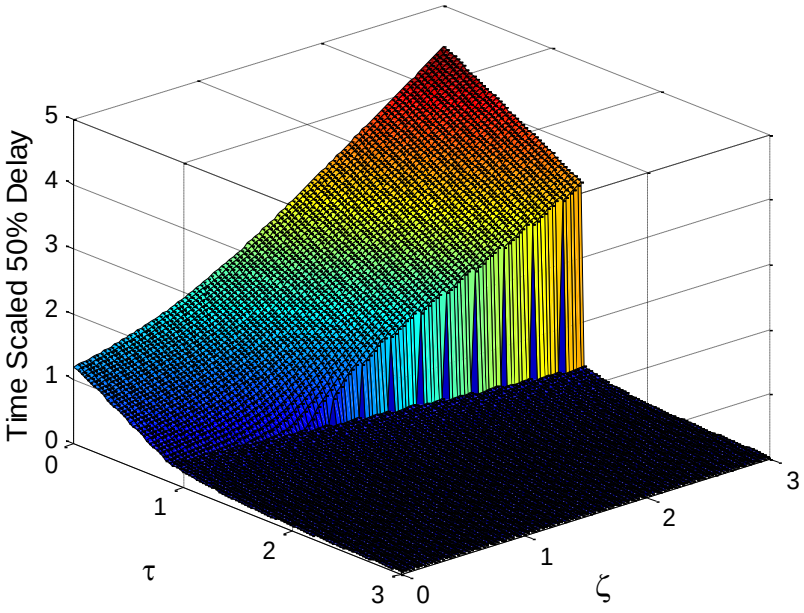
$$\begin{aligned} V_{out}(t) = V_{DD}&\left(\frac{t_n}{t_r} + \frac{(-\tau - 2\zeta)}{P} + \frac{C_1}{P}e^{-t_n(\zeta+\sqrt{\zeta^2-1})} + \frac{C_2}{P}e^{-t_n(\zeta-\sqrt{\zeta^2-1})}\right)u(t_n) \\ -V_{DD}&\left(\frac{t_{nr}}{t_r} + \frac{(-\tau - 2\zeta)}{P} + \frac{C_1}{P}e^{-t_{nr}(\zeta+\sqrt{\zeta^2-1})} + \frac{C_2}{P}e^{-t_{nr}(\zeta-\sqrt{\zeta^2-1})}\right)u(t_{nr}) \end{aligned} \tag{3.21}$$

where,

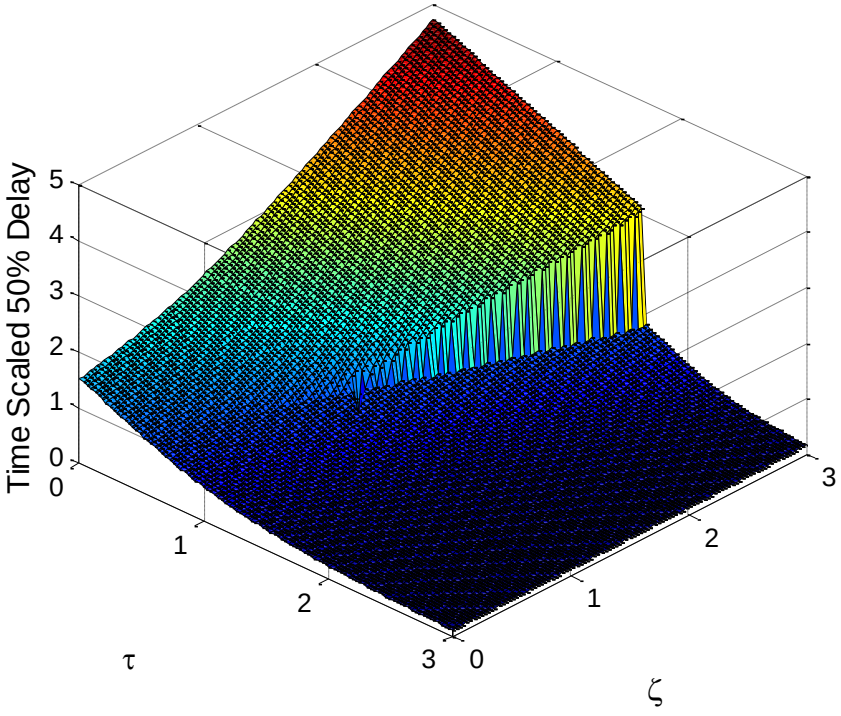
$$C_1 = -\frac{1 + \tau(\zeta + \sqrt{\zeta^2 - 1}) - 0.5\tau^2(\zeta + \sqrt{\zeta^2 - 1})^2}{2(\sqrt{\zeta^2 - 1})(\zeta + \sqrt{\zeta^2 - 1})} \tag{3.22}$$

$$C_2 = \frac{1 + \tau(\zeta - \sqrt{\zeta^2 - 1}) + 0.5\tau^2(\zeta - \sqrt{\zeta^2 - 1})^2}{2(\sqrt{\zeta^2 - 1})(\zeta - \sqrt{\zeta^2 - 1})} \tag{3.23}$$

The coefficient $u(t_n)$ and $u(t_{nr})$ is the unit step response, $t_n = (t - T_d)\omega_n$ and $t_{nr} = (t - T_d - t_r)\omega_n$ respectively and here $\tau = T_d\omega_n$ and $P = t_r\omega_n$. In this case, to calculate the 50% delay and rise time requires solving the nonlinear function of (3.21) for specific values of ζ, τ and P.



(a)



(b)

Fig. 3.3 The time scaled 50% delay for different values of τ and ζ (a) P=0.3 (b) P=4

3.3.2Prediction of 50%Delay and Rise Time for Ramp Input

The output voltage of (3.21) is a nonlinear function with respect to three variables which are ζ, τ and *P*. As a result, an analytic formula is still not available for the 50% delay and rise time. The solution of (3.21) is obtained iteratively using methods such as Newton-Rhapson. The nonlinear equation of (3.21) can be solved for various ranges of ζ, τ and *P* by setting V_{out} to $0.5V_{DD}$ to get the 50% delay. The results of this analysis can be used to create a look up table. With the knowledge of this look up table , 50% delay can be obtained using interpolation techniques. The advantage of this approach is to avoid solving nonlinear equation of (3.21). This is crucial when dealing with large scale VLSI circuits composed of hundreds of millions of transistors for early layout design.

On-chip RLC interconnects may have complex conjugate poles in frequency domain. As a result they have non monotonic response in time domain. For the case of step input, solving the nonlinear equation of (3.5) for 50% delay and rise time results in a continuous function with respect to τ and ζ. That is why the functions were fitted to rational approximations which are discussed in section 3.2.2. For ramp inputs, 50% delay is not a continuous function with respect to ζ, τ and *P*. Since this is not continuous, it is very hard to fit these functions using rational approximations. This problem is illustrated in Fig. 3.3. This figure is created for two specific values of *P=0.3* and *P=4* and for various ranges of ζ, τ solving the nonlinear function of (3.21). From the figures, the discontinuity of the time scaled 50% function is clearly visible for both values of *P* and

this is even true for many ranges of *P*. That`s why it is very challenging to approximate this as a rational function. In order to calculate the rise time, equation (3.21) can also be used by setting V_{out} to $0.1V_{DD}$ and $0.9V_{DD}$ and solving the time for different values of ζ, τ and *P*. Like the 50% delay, time scaled rise time is also a discontinuous function for many ranges of *P*. As a result the nonlinear function of (3.21) can be solved for a priory values of ζ, τ and *P* for calculating the 50% delay and rise time and the results can be stored in a look up table.

The implementation details of how to create the look up table for the 50% delay and rise time are not discussed in this thesis since the objective of this work is to illustrate the improved accuracy of the proposed method compared with the two pole Elmore based model of [59] which also considers the ramp input. Numerical examples are provided in chapter 4 in order to show the better accuracy of the proposed algorithm.

3.4 Conclusions

In this chapter, a delay extraction based rational approximation is proposed to improve the accuracy of Elmore based two pole model where the time of fight signal delay is extracted without increasing the number of poles or affecting the stability of the transfer function. From this analysis, analytic fitted expressions are obtained for the 50% delay and rise time for unit step input and look up table is proposed to calculate those parameter for ramp inputs. The next chapter will present numerical examples to demonstrate the validity of the proposed algorithm.

Chapter 4

Numerical Examples

4.1 Introduction

This chapter presents the numerical examples to demonstrate the validity of the proposed method. Examples of single line, symmetrical tree structure (balanced and unbalanced) and unsymmetrical tree structure are shown here to see the difference between the two pole model and the proposed model. In section 4.2, proposed algorithm is tested selecting unit step response for different lines lengths of those examples. Different ramp inputs are also used to observe the results in section 4.3 and finally a conclusion is provided in section 4.4. The results were obtained using MATLAB R2010b operating on Bolen Custom built T7400 64-bit workstations with clock speed 3.33 GHz and are also compared with HSPICE and conventional two pole model [43],[56].

4.2 Selecting Unit Step Input:

4.2.1 Example 1 - Single Line Interconnect

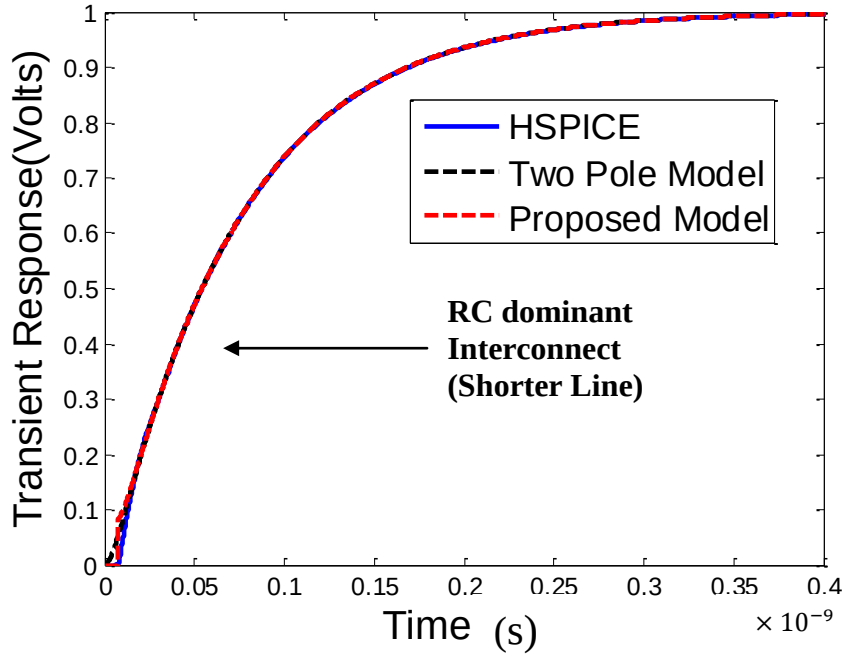
A single *RLC* line proposed in [58] is considered which models the on-chip interconnect using 65-nm technology. Three different wire types, whose *RLC* parameters were extracted using field solvers [50], [53], are analyzed. The wire widths and per unit length *R, L, C* parameters are shown in Table 4.1. Wire thickness is 319nm for all cases. At first the length of the line is set to 0.05cm and then line length is increased to 0.2 cm.

TABLE 4.1
SINGLE LINE INTERCONNECT PARAMETERS

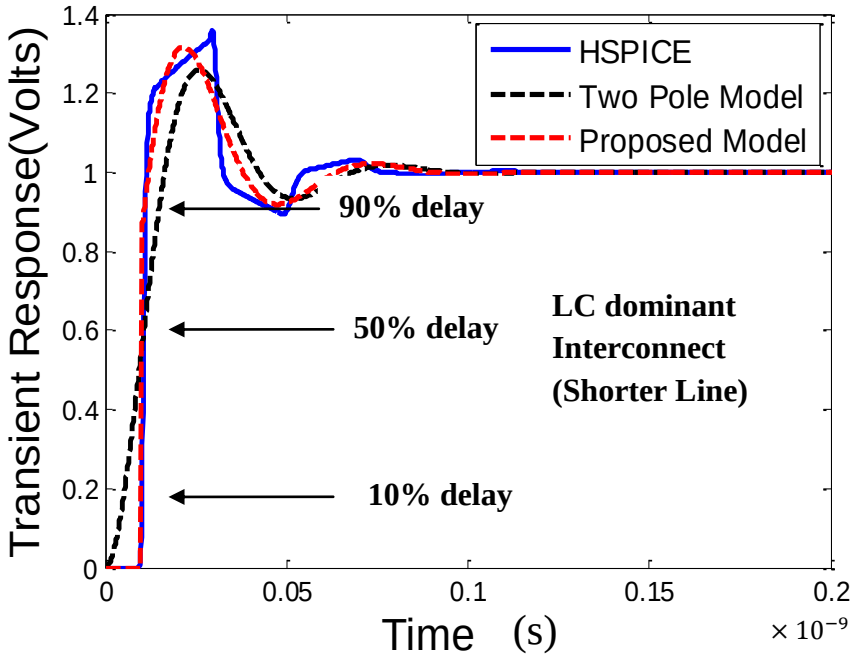
Width(μm)	R(Ω/cm)	L(nH/cm)	C(fF/cm)
0.5	1610	13.1	1.64
1	806	12.2	2.43
1.5	538	11.6	3.22

Equation (3.5) is used to get the time domain response of the proposed model for unit step response. The 50% delay and rise time calculated with the proposed model (equation (3.13) and equation (3.18)) is compared with conventional two pole model (equation (2.33) and equation (2.34)) and HSPICE for various resistive and capacitive loads of R_s and C_l. The results are shown in Table 4.2 and Table 4.3. The far end time domain transient responses of proposed model, two pole model and HSPICE are plotted in Fig. 4.1 and 4.2 for 0.05cm and 0.2 cm respectively.

When the line length is very short (such as 0.05cm) the improvement of the proposed model as compared to two pole model is moderate for the 50% delay where average error drops from 8.9 to 8.1 overall (*RC* and *LC* dominant interconnects), however the proposed model predicts rise time more accurately(10.94% average error as compared to 220%). This is due to the fact that shorter line lengths do not have significant signal delay and hence the proposed delay extraction algorithm offers only minor improvements for the 50% delay. From Fig. 4.1 it is seen that for very short lines of *RC* dominant interconnects (Fig. 4.1 (a)), two pole model and proposed model are almost same. However for *LC* dominant interconnects (Fig. 4.1 (b)), even for shorter lines proposed model is more accurate than two pole model when compared with HSPICE.

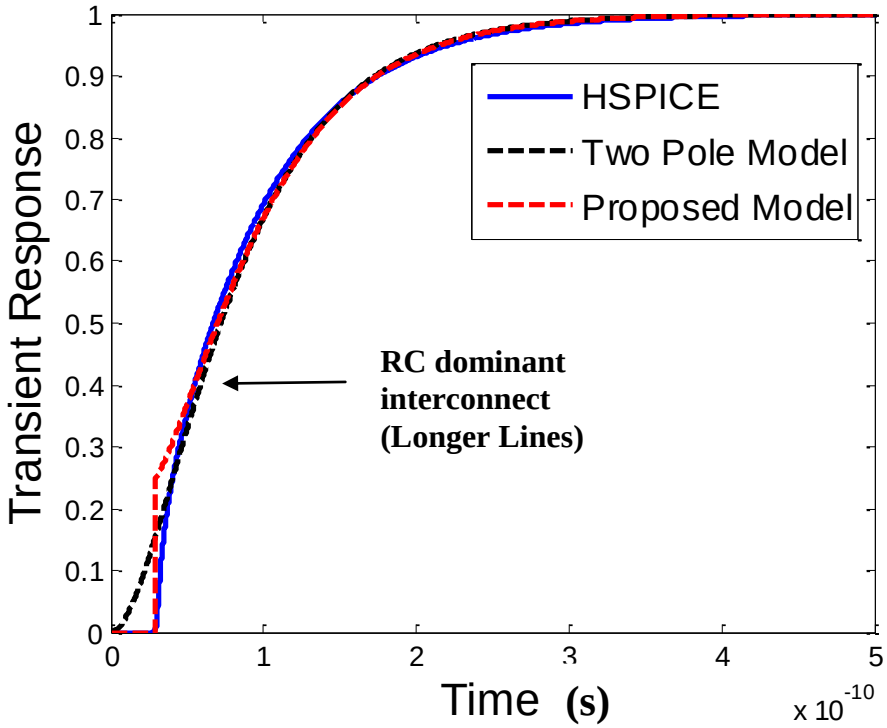


(a)

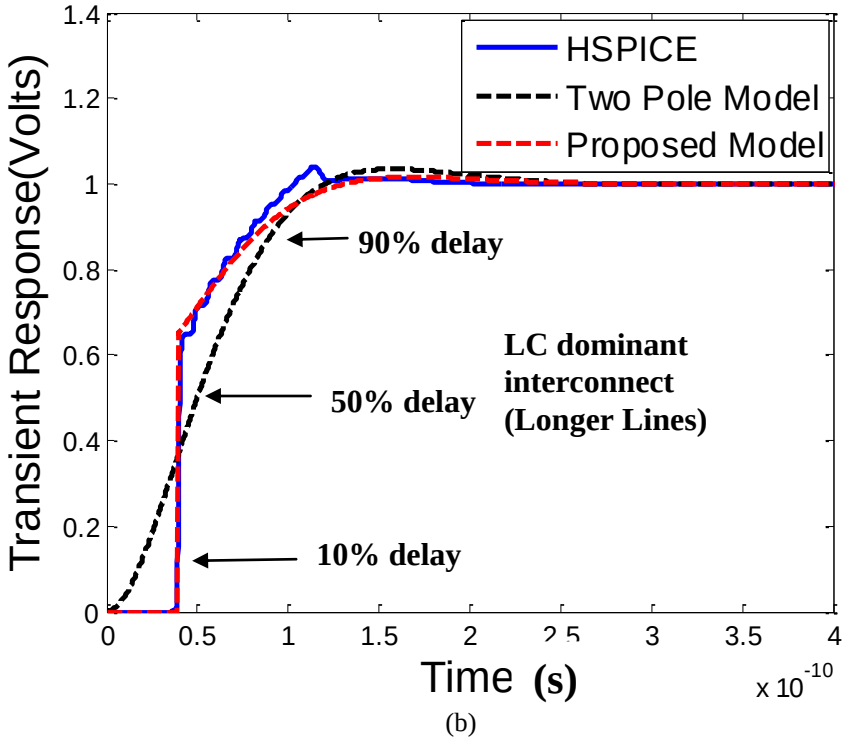


(b)

Fig. 4.1: Transient response of Example in 4.2.1 for 0.05cm line length (a) Line width (*w*) is 0.5µm, Rs=200 Ω, C*l*=100 fF.(b) Line width (*w*) is 1.5µm, Rs=20 Ω, C*l*=10 fF.



(a)



(b)

Fig. 4.2: Transient response of Example in 4.2.1 for 0.2cm line length (a) Line width (*w*) is 0.5µm, Rs=200 Ω, C*l*=200 fF. (b) Line width (*w*) is 1.5µm, Rs=20 Ω, C*l*=20 fF.

TABLE 4.2
COMPARISONS OF 50% DELAY AND RISE TIME FOR SINGLE LINE INTERCONNECT OF PROPOSED MODEL WITH CONVENTIONAL TWO POLE MODEL AND HSPICE FOR UNIT STEP INPUT.THE LINE LENGTH IS 0.05 CM. (EXAMPLE 4.2.1)

Width (μm)	Rs (Ω)	Cl (fF)	ζ	τ	HSPICE		Two Pole Model		Proposed Model	
					50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)
0.5	20	10	0.48	1.18	8.4	1.93	7.83	11.20	7.9	2.7
	50	50	0.79	0.83	12.1	16.9	13.36	25.38	11.72	18.7
	100	100	1.23	0.61	22	52.2	23.51	59.54	22.88	53.81
	200	200	2.09	0.41	54.23	156.6	54.29	164.74	54.22	158.32
1	20	10	0.4	1.26	9.5	1.3	8.26	11.12	8.8	1.28
	50	50	0.73	0.95	12.1	12.5	13.06	23.53	9.9	15.38
	100	100	1.23	0.74	20.1	49.5	22.8	57.69	21.95	50.7
	200	200	2.22	0.51	52.9	154.5	53.28	163.05	53.2	158.64
1.5	20	10	0.4	1.29	10.6	1.04	9.18	12.31	9.95	1
	50	50	0.75	1.03	12.7	11.9	14.1	26.06	10.2	16.51
	100	100	1.32	0.82	20.4	54.8	24.58	64.49	23.62	56.58
	200	200	2.4	0.58	55.5	169.8	57.21	176.62	57.24	171.6
Average Error %							8.93	219.98	7.9	10.94
Maximum Error %							20.49	1083.65	19.6	39.9

When the line length is increased (0.2cm), it is very clear that proposed algorithm gives better accuracy in calculating both 50% propagation delay and rise time for all types of interconnects (*RC* and *LC* dominant). From Table 4.3 it is shown that average error drops down to 3.4% from 13.87% and maximum error drops down to 8.6% from 30.54% for 50% delay. For rise time average error drops down to 4.7% from 31.9%

and maximum error drops down to 14.72% from 112%. This is due to the fact that longer line lengths have greater signal delay and the proposed algorithm captures this delay through its delay rational approximation.

TABLE 4.3
COMPARISONS OF 50% DELAY AND RISE TIME FOR SINGLE LINE INTERCONNECT OF PROPOSED MODEL WITH CONVENTIONAL TWO POLE MODEL AND HSPICE FOR UNIT STEP INPUT. THE LINE LENGTH IS 0.2 CM. (EXAMPLE 4.2.1)

Width (μm)	Rs (Ω)	Cl (fF)	ζ	τ	HSPICE		Two Pole Model		Proposed Model	
					50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)
0.5	20	10	0.95	0.88	48.9	91.5	55.08	118.81	47.21	93.19
	50	50	1.06	0.70	67.3	142.9	73.60	170.66	69.97	145.23
	100	100	1.2	0.55	96.4	228.1	102.37	256.29	99.61	234.01
	200	200	1.46	0.38	163.7	429.9	169.18	465.12	166.10	436.18
1	20	10	0.79	1.07	37.1	52.1	48.43	92.56	35.41	59.77
	50	50	0.96	0.89	54.5	107.8	64.49	140.61	55.14	110.7
	100	100	1.18	0.71	83.8	196.9	91.72	227.49	88.1	199.1
	200	200	1.54	0.51	151.2	406.8	156.56	439.34	154.1	416
1.5	20	10	0.73	1.14	40.2	42.8	50.19	90.79	40.3	48.32
	50	50	0.95	0.97	52.2	102.1	67.34	145.36	50.1	111.34
	100	100	1.23	0.79	85.8	211.9	97.68	247.79	93.18	215.74
	200	200	1.68	0.57	161.3	446.1	169.89	490.21	167.91	462.86
Average Error %							13.87	31.9	3.4	4.7
Maximum Error %							30.54	112.13	8.6	14.72

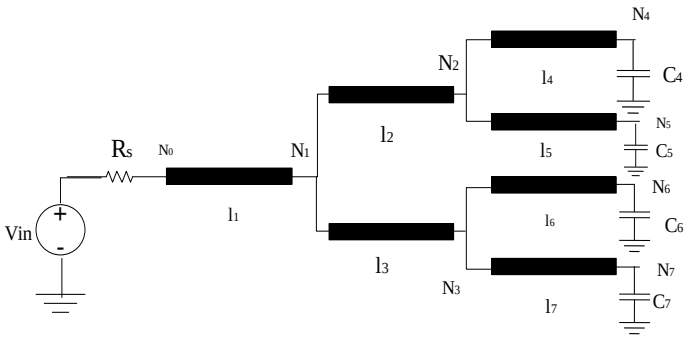


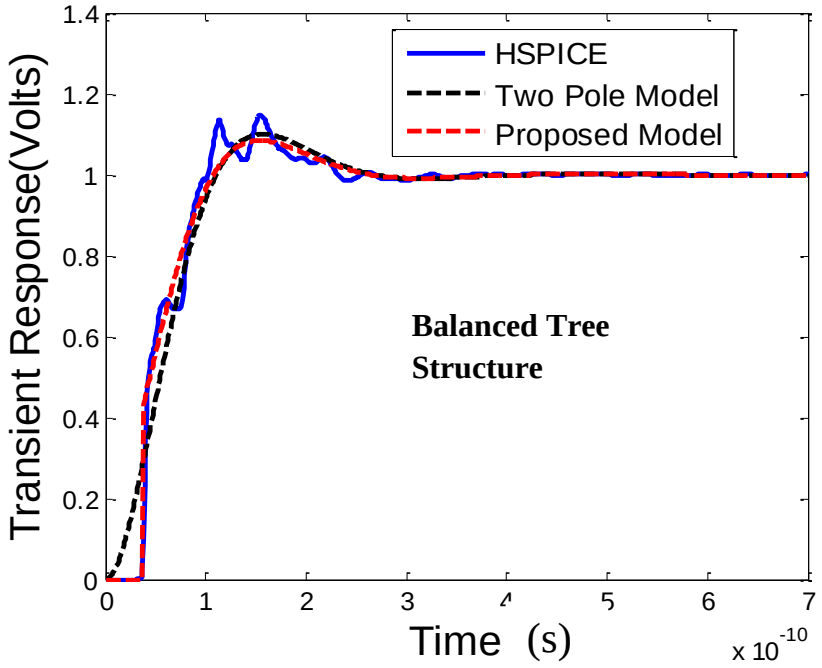
Fig. 4.3 Example of symmetrical tree structure

4.2.2 Example 2 – Symmetrical Tree Structure Interconnect

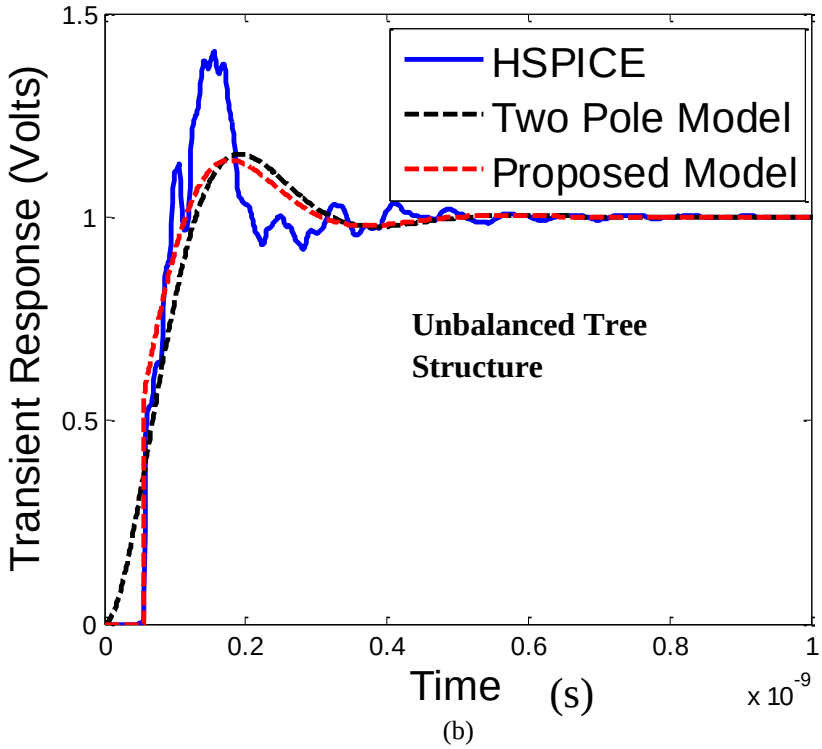
The symmetrical tree structure shown in Fig. 4.3 is analyzed in this section. For simplicity, the branches are assumed to have the same width of 6 μm. The width of each interconnect in the tree structure is 10 μm and the spacing is 6 μm. The interconnect parameters of such a structure are R=39 Ω/cm, L=4.3 nH/cm, and C=3.6 pF/cm [41]. The normalized wire lengths and load capacitances shown in Fig. 4.3 are listed in Tables 4.4 and Table 4.5 for both balanced and unbalanced structures where l_x and C_x are the normalized reference lengths and capacitances, respectively.

TABLE 4.4
TREE STRUCTURE INTERCONNECT LENGTHS NORMALIZED TO L_x

Index	l_1	l_2	l_3	l_4	l_5	l_6	l_7
Balanced	.05	0.1	0.1	0.15	0.15	0.15	0.15
Unbalanced	.05	0.2	0.1	0.2	0.1	0.1	0.05



(a)



(b)

Fig. 4.4: Transient response of symmetrical tree structure of node N_4
(a) Balanced Tree of Normalized line length l_x =0.1cm, Rs=10 Ω, C_x=80 fF.
(b) Unbalanced Tree of Normalized line length l_x =0.1cm, Rs=10 Ω, C_x=20 fF.

TABLE 4.5
CAPACITANCE NORMALIZED TO C_x

Index	C_5	C_6	C_7	C_8
Balanced	1	1	1	1
Unbalanced	2	1	2	.5

TABLE 4.6
COMPARISONS OF 50% DELAY AND RISE TIME FOR SYMMETRICAL TREE STRUCTURE INTERCONNECT OF PROPOSED MODEL WITH CONVENTIONAL TWO POLE MODEL AND HSPICE FOR UNIT STEP INPUT. FOR TREE EXAMPLE OUTPUTS ARE OBSERVED AT NODE N_4

Example	l_x (cm)	Rs (Ω)	C_x (fF)	ζ	τ	HSPICE		Two Pole Model		Proposed Model	
						50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)
Balanced Tree	0.5	10	80	0.53	0.88	23.9	25.1	27.40	41.1	23.5	24.77
	0.5	10	200	0.59	0.77	28.5	35.2	32.61	51.43	29.87	36.24
	1	10	80	0.60	0.92	43.08	48.99	54.30	86.12	44.4	51.5
	1	10	200	0.62	0.85	50.59	60.5	60.43	99.04	52.4	66.46
Unbalanced Tree	0.5	10	20	0.42	1.12	30.77	15.84	30.47	41.48	29.5	12.35
	0.5	30	20	0.70	1.09	34.09	24.72	36.94	65.48	32.3	34.9
	0.5	10	500	0.63	0.60	66.2	67.29	64.3	106.23	62.1	85.62
	0.5	30	500	1.4	0.55	100.8	258.9	109.82	295.96	107.6	276
	1	10	20	0.5	1.1	59.1	36.3	64.37	93.77	57.4	33.05
	1	30	20	1.0	1.02	85.1	134.6	94.18	211.53	67.7	163.27
	1	10	500	0.65	0.72	113.1	103.6	100.91	180.55	107.33	133.41
	1	30	500	1.21	0.64	158.6	374.8	170.29	428.56	164.9	383.74
Average Error %								10.61	79.32	4.5	14.81
Maximum Error %								26.04	164.89	20.45	41.18

Results of two pole model, HSPICE and proposed model are shown in Table 4.6. The far end time domain responses at node N_4 of this tree structure (balanced and unbalanced) are plotted in Fig. 4.4. As it is shown from Table 4.6, for balanced and unbalanced tree structures the accuracy of proposed model has also improved as compared to two pole model where average error drops down to 5.4% from 10.61% and maximum error drops down to 20.45% from 26.04% for 50% delay. For rise time average error drops down to 14% from 79% and maximum error drops down to 41% from 164%.

4.2.3 Example 3 – Unsymmetrical Tree Structure Interconnect

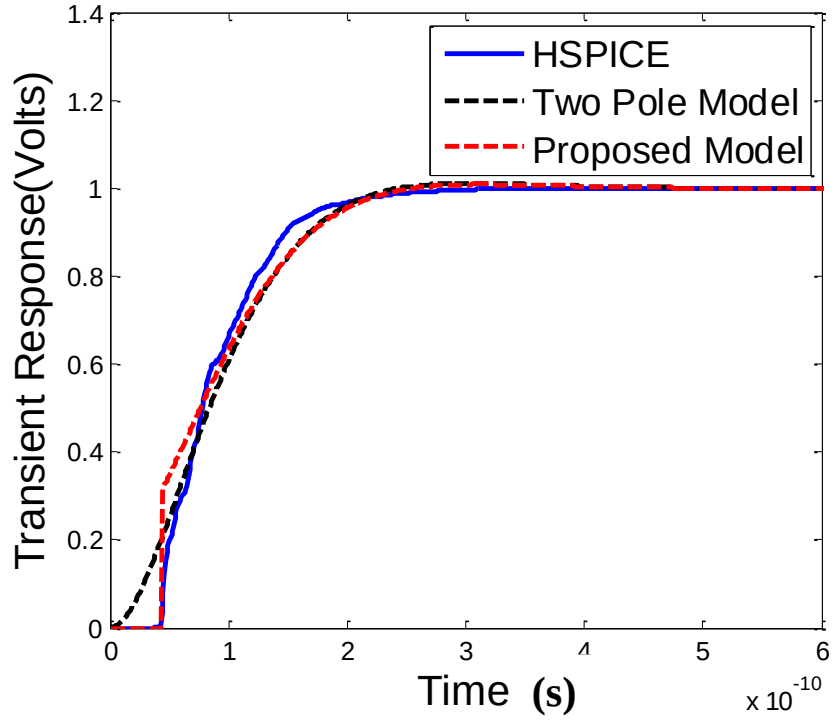
The unsymmetrical tree structure shown in Fig. 2.4 has been analyzed in this section. Here the interconnect parameter of width 1.5μm of Table 4.1 has been considered in each interconnect section of Fig. 2.4. The normalized wire lengths and load capacitances shown are listed in Tables 4.7 and Table 4.8. Results of two pole model, HSPICE and proposed model are shown in Table 4.9.Two nodes have been considered in this structure, node N_5 and node N_7.The far end time domain responses at N_5 and node N_7 of this tree structure are plotted in Fig. 4.5

TABLE 4.7
INTERCONNECT LENGTHS NORMALIZED TO L_x FOR UNSYMMETRICAL TREE STRUCTURE

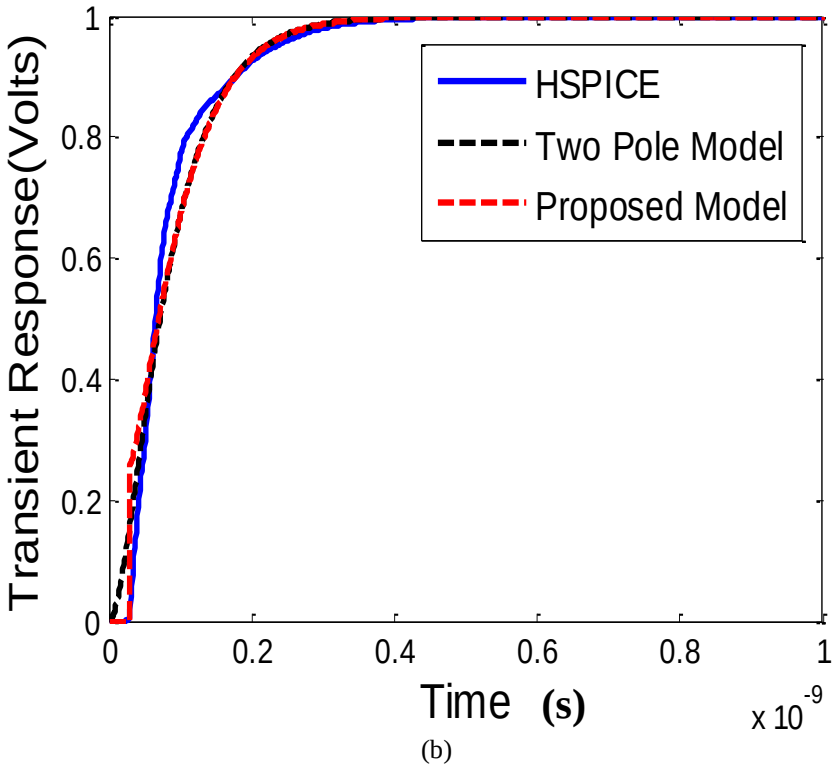
Index	l_1	l_2	l_3	l_4	l_5	l_6	l_7	l_8	l_9
Length	.05	0.2	0.1	0.05	0.2	0.1	0.15	0.1	0.1

TABLE 4.8
CAPACITANCE NORMALIZED TO C_x

Index	C_5	C_6	C_7	C_8	C_9
Capacitances	2	1	2	0.5	1



(a)



(b)

Fig. 4.5: Transient response of unsymmetrical tree structure (a) Normalized line length l_x =0.05cm, Rs=10 Ω, C_x=20 fF. (Node N_5) (b) Normalized line length l_x =0.05cm, Rs=10 Ω, C_x=100 fF.(Node N_7)

TABLE 4.9
COMPARISONS OF 50% DELAY AND RISE TIME FOR UNSYMMETRICAL TREE STRUCTURE INTERCONNECT OF PROPOSED MODEL WITH CONVENTIONAL TWO POLE MODEL AND HSPICE FOR UNIT STEP INPUT. OUTPUTS ARE OBSERVED AT NODE N_5 AND NODE N_7

l_x (cm)	Rs (Ω)	C_x (fF)	ζ	τ	Node	HSPICE		Two Pole Model		Proposed Model	
						50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)
0.5	10	20	0.82	0.80	N_5	775.9	103.55	846.75	165.85	761.04	126.5
0.5	10	20	1.01	0.93	N_7	49.5	102.99	53.8	120.95	44.81	96.2
0.5	10	100	0.89	0.63	N_5	102.0	171.6	110.00	227.32	105.10	187.83
0.5	10	100	1.08	0.71	N_7	65.4	146.1	73.31	172.86	69.83	148.01
0.5	30	20	1.00	0.69	N_5	101.5	197.2	108.44	243.13	102.9	204.55
0.5	30	20	1.61	0.94	N_7	60.22	187.23	73.92	210.70	72.76	187.21
0.5	30	100	1.05	0.54	N_5	134.1	282.8	141.42	327.77	137.10	292
0.5	30	100	1.61	0.69	N_7	85.8	258.1	100.57	286.46	99.1	264.3
1	10	20	1.00	0.56	N_5	249.1	495.9	265.22	595.87	256.3	521.9
1	10	20	1.66	0.94	N_7	139.3	376.1	151.46	435.88	149.6	389.0
1	10	100	1.03	0.49	N_5	297.8	612.6	311.85	711.07	303.47	636.84
1	10	100	1.58	0.73	N_7	171.1	454.5	186.89	529.21	184.4	484.12
1	30	20	1.08	0.49	N_5	299.3	648.8	316.2	743.81	307.7	672.77
1	30	20	2.31	0.98	N_7	180.4	551.1	195.21	600.31	195.6	558.6
1	30	100	1.10	0.43	N_5	356.0	775.1	370.86	880.70	361.5	804.9
1	30	100	2.05	0.72	N_7	218.2	652.2	237.63	718.25	237.2	677.42
Average Error %								9.13	19.19	6	5.05
Maximum Error %								22.75	60.16	20.8	22.16

From Table 4.9, it also shows that for unsymmetrical tree structure, proposed model has improved the accuracy of conventional two pole model in calculating 50% delay and rise time calculation.

4.2.4 Summary of the Results:

As discussed in section 3.2.2, when $\tau \leq 1$, the output voltage at the time point of the extracted delay ($t = T_d$) is less than the 50% of the input signal $V_{out}(t = T_d) \leq 0.5V_{DD}$. As a result the calculation for the 50% delay of the proposed algorithm is always better than the conventional two pole model. For the case when $\tau \geq 1$ the output voltage at $t = T_d$ is passed the 50% delay of the input signal ($V_{out}(t = T_d) \geq 0.5V_{DD}$). As a result, the proposed method sometimes underestimates the actual 50% delay even though it adds the extracted delay with the fitted function of τ=0.99 which may be very small because of low values of ζ. However for the prediction of rise time the proposed model is always better than the two pole model since there is no issue of initial condition. Overall results of single line, symmetrical and unsymmetrical tree structure interconnect yield significant improvements of the Elmore based two pole model in terms of calculating 50% delay and rise time.

4.3 Selecting Ramp Input:

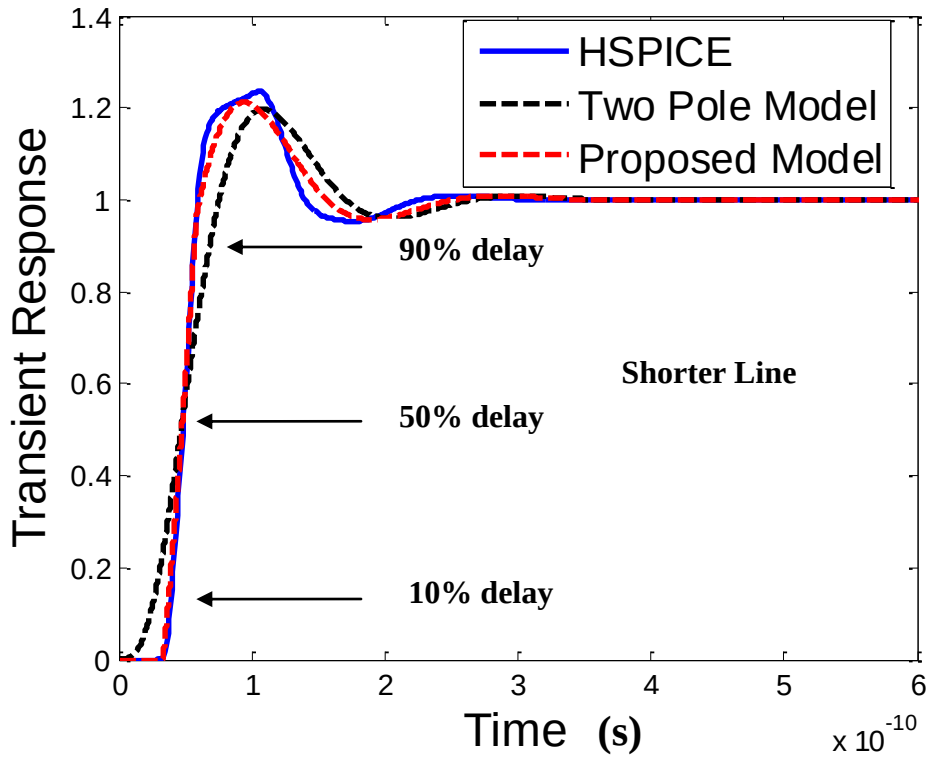
When the rise time of input signal gets very sharp (i.e. unit step) in time domain, that means it has so many high frequency components. If the system has unit step input, two pole model might not always be accurate enough in capturing those high frequency components. As a result there is more error in calculating 50% delay and rise time for

unit step input. When the input signal becomes ramp, it has less high frequency components as compared to unit step input. As a result the two pole Elmore model and the proposed method will have better accuracy in predicting 50% delay and rise time for ramp input signals. However, since the proposed algorithm is based on delay extraction it will even improve the accuracy of the two pole model. In this section numerical examples of single line, symmetrical (balanced and unbalanced) and unsymmetrical tree structure interconnects discussed in section 4.2 are also presented to illustrate the improved accuracy of the proposed method over Elmore based two pole model [59].

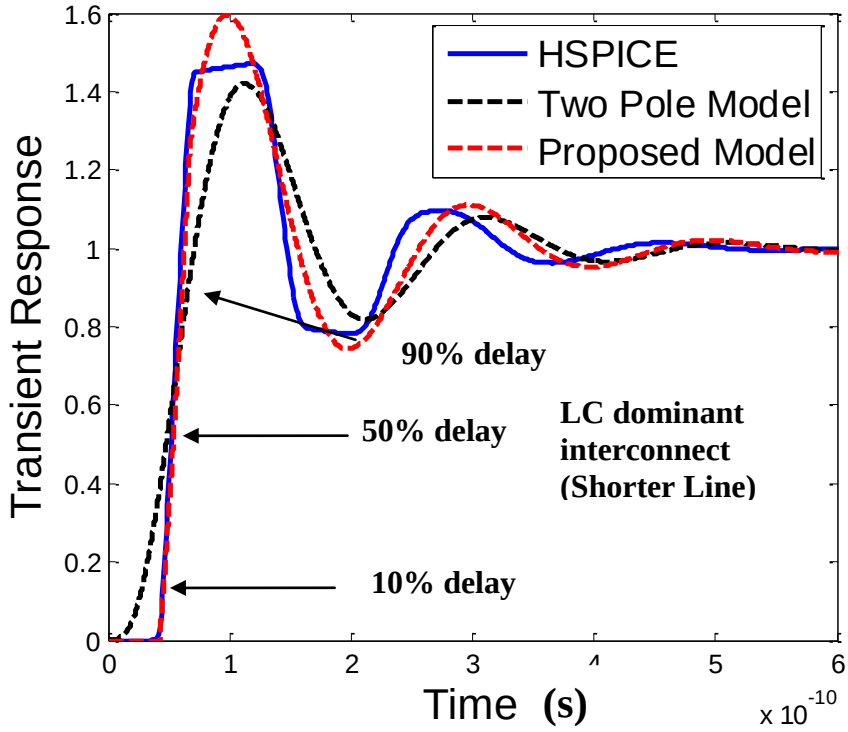
4.3.1 Example 1 - Single Line Interconnect

A single RLC line proposed in [41] is considered. The interconnect structure is analyzed for a height of h = 1 μm and the conductor width is varied to w = 2 μm, w = 5 μm and w = 10 μm. The corresponding per unit length parameters for w = 2 μm are R = 88.29 Ω /cm, L = 15.38 nH/cm and C = 1.8 pF/cm; for w = 5 μm are R = 35.5 Ω /cm, L = 13.6 nH/cm and C = 3.3 pF/cm; and for w = 10 μm are R = 22 Ω/cm, L = 12.6 nH/cm and C = 4.9 pF/cm. The algorithm is now tested for ramp response with a rise time of 0.025 ns and 0.1 ns.

Equation (3.21) is used to get the time domain response of the proposed model for ramp input. The 50% delay and rise time calculated with the proposed model is compared with conventional two pole model and HSPICE analysis for various resistive and capacitive loads of R_s and C_l also and the results are shown from Table 4.10 to Table 4.13. Table 4.10 and Table 4.11 show the results when input signal is ramp of 0.025ns rise time for 0.2cm and 0.5cm respectively. The corresponding far end time domain

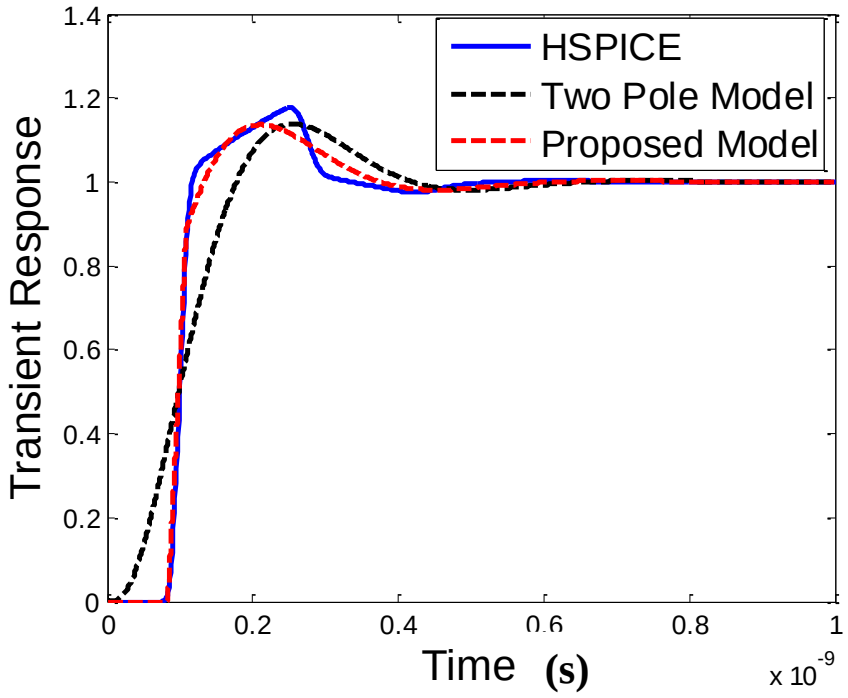


(a)

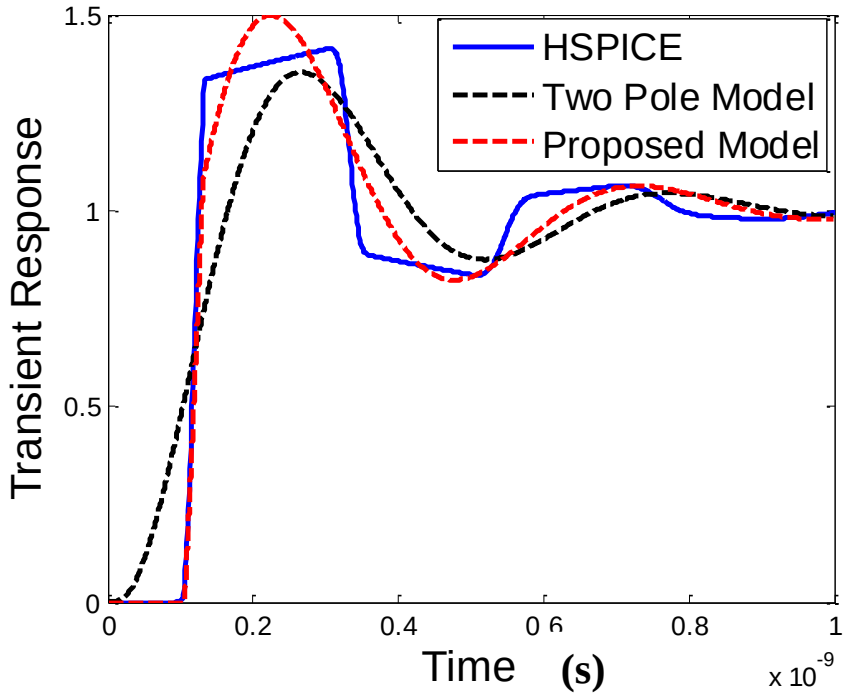


(b)

Fig. 4.6: Transient response of Example in 4.3.1. For ramp input of 0.25ns for 0.2cm of line length (a) Line width (w) is 10µm, Rs=50 Ω, Cl=50 fF. (b) Line width (w) is 5µm, Rs=20 Ω, Cl=10 fF.

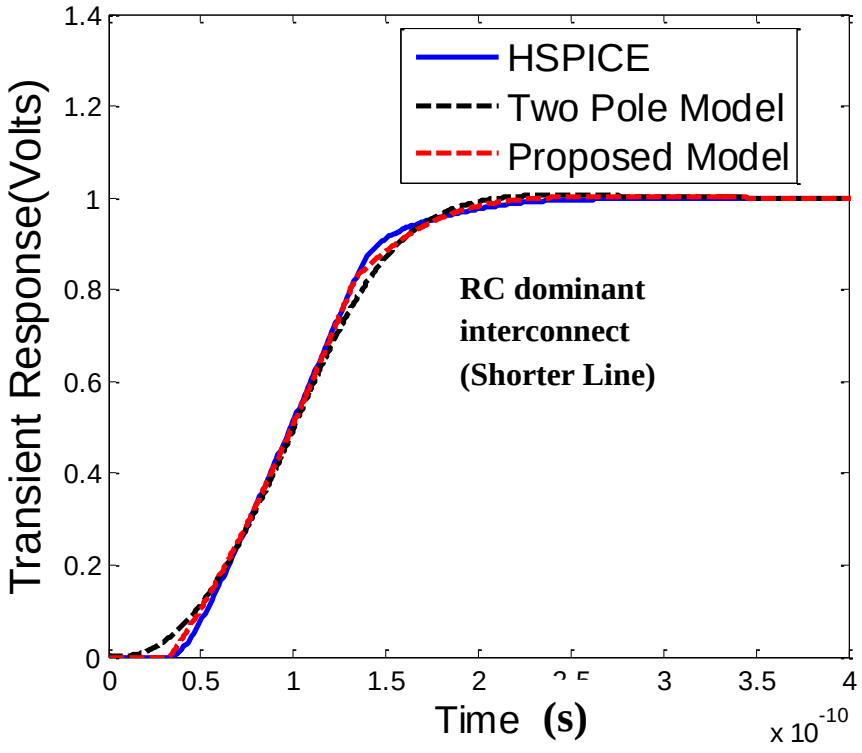


(a)

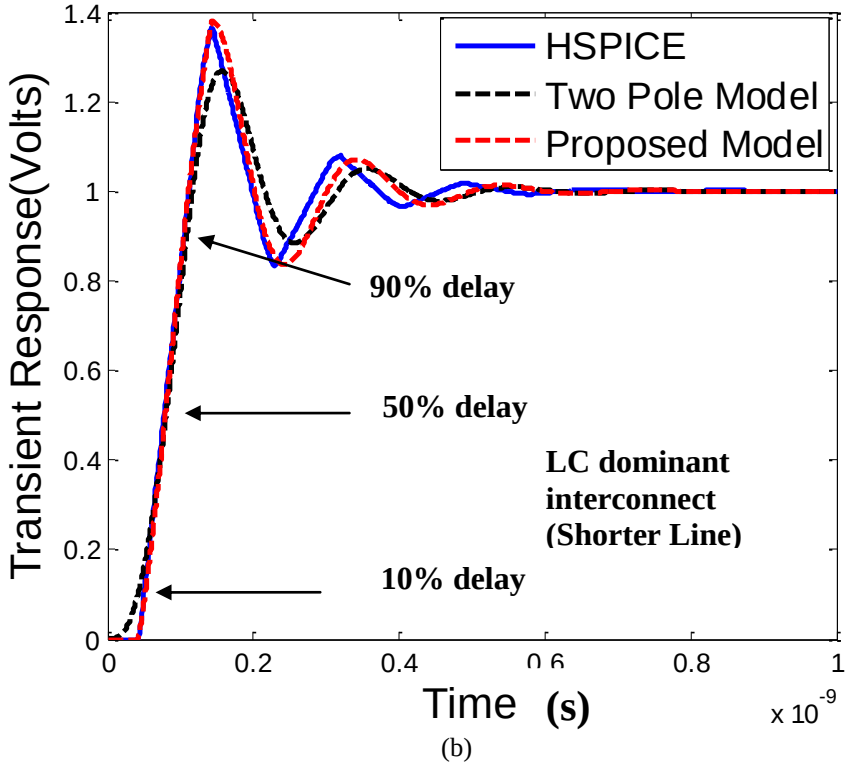


(b)

Fig. 4.7: Transient response of Example in 4.3.1. For ramp input of 0.025ns for 0.5cm of line length (a) Line width (*w*) is 10µm, Rs=50 Ω, C*l*=50 fF. (b) Line width (*w*) is 2µm, Rs=20 Ω, C*l*=10 fF.

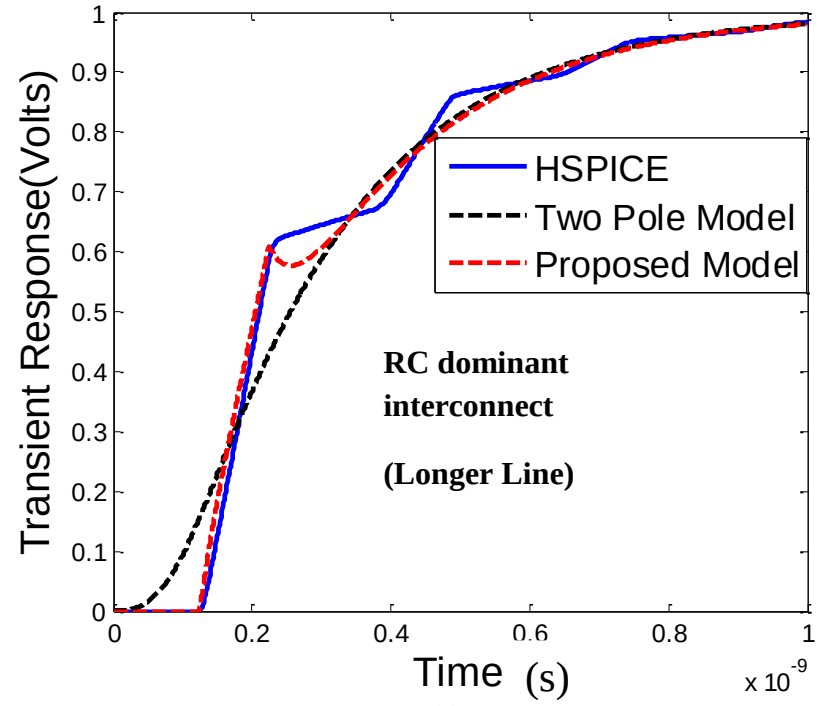


(a)

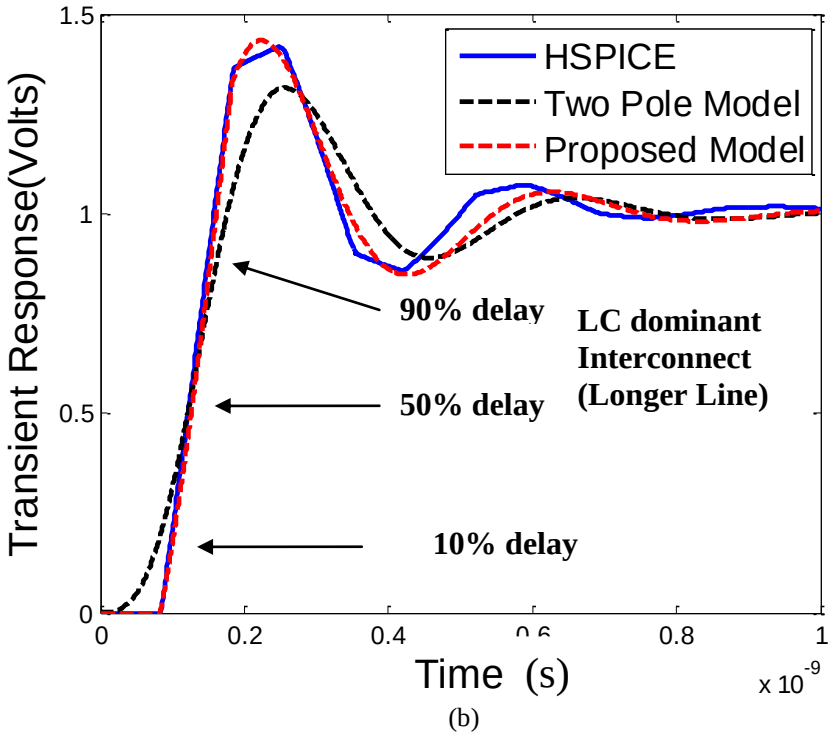


(b)

Fig. 4.8: Transient response of Example in 4.3.1. For ramp input of 0.1ns for 0.2cm of line length (a) Line width (w) is 10µm, Rs=100 Ω, Cl=100 fF. (b) Line width (w) is 2µm, Rs=20 Ω, Cl=10 fF.



(a)



(b)

Fig. 4.9: Transient response of Example in 4.3.1.For ramp input of 0.1ns for 0.5cm of line length (a) Line width (*w*) is 10µm,Rs=100 Ω, C*l*=100 fF.(b) Line width (*w*) is 2µm, Rs=20 Ω, C*l*=10 fF.

TABLE 4.10
COMPARISONS OF 50% DELAY AND RISE TIME FOR RAMP RESPONSE OF 0.025NS OF PROPOSED MODEL WITH CONVENTIONAL TWO POLE MODEL AND HSPICE. THE LINE LENGTH IS 0.2 CM. (EXAMPLE 4.3.1)

Width (μm)	Rs (Ω)	Cl (fF)	ζ	P	τ	HSPICE		Two Pole Model		Proposed Model	
						50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)
2	20	10	0.22	1.03	1.36	42.5	13.54	39.9	33.1	44.5	15.6
	50	50	0.45	0.92	1.23	48.3	18.8	46.8	44.4	47.5	20.4
	100	100	0.83	0.82	1.09	56.1	53.4	59.7	80.7	52.9	70
5	20	10	0.26	0.82	1.38	51.7	13.7	47.5	40.8	53.6	16.3
	50	50	0.58	0.77	1.30	57.32	19.87	56.6	61.4	56.5	21.7
	100	100	1.12	0.71	1.20	66	119	76.3	140.5	61.5	132
10	20	10	0.31	0.70	1.39	59.2	14.6	54.7	49.1	61	17.2
	50	50	0.72	0.67	1.33	65.3	22.3	66.7	83.4	63.7	22
	100	100	1.39	0.63	1.25	74.33	205.6	96.1	215	69.6	199.9
Average Error %								8.85	141.28	4.0	12.87
Maximum Error %								29.29	273.99	6.82	31.09

responses are plotted in Fig. 4.6 and Fig. 4.7. Another ramp input of 0.1ns rise time is applied and results are shown in Table 4.12 and Table 4.13 .Their time domain responses are plotted in Fig. 4.8 and Fig. 4.9 for 0.2cm and 0.5cm respectively.

From Table 4.10 to Table 4.13, it is visible that overall error (two pole, proposed model) goes down significantly when input signal becomes ramp. Since the interconnect delay has been extracted the proposed model becomes even more accurate than the two pole model for ramp input and it improves the accuracy where the average error drops

TABLE 4.11
COMPARISONS OF 50% DELAY AND RISE TIME FOR RAMP RESPONSE OF 0.025NS OF PROPOSED MODEL WITH CONVENTIONAL TWO POLE MODEL AND HSPICE. THE LINE LENGTH IS 0.5 CM. (EXAMPLE 4.3.1)

Width (µm)	Rs (Ω)	Cl (fF)	ζ	P	τ	HSPICE		Two Pole Model		Proposed Model	
						50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)
2	20	10	0.32	0.4	1.36	93.54	14.5	95.6	82.7	85.1	16.5
	50	50	0.53	0.38	1.27	99.68	24	98.1	112.1	97.9	24.3
	100	100	0.87	0.35	1.16	108.5	157.9	124.2	196.5	101.7	166.3
5	20	10	0.31	0.33	1.38	116.8	15	103.6	103.3	118.2	19
	50	50	0.63	0.31	1.32	121.9	20.7	122.9	154.8	120	22
	100	100	1.12	0.29	1.24	131	260.6	165.9	339.9	123.1	303.5
10	20	10	0.35	0.28	1.39	134.1	15.2	120.8	125.3	136	19
	50	50	0.75	0.27	1.34	140	29	148.4	213.6	138.5	42.5
	100	100	1.37	0.25	1.27	150.8	491	216.7	516	141.3	470.3
Average Error %								12.96	388.31	3.8	16.17
Maximum Error %								43.7	724.34	9.02	46.55

down to 8.85% from 4% for ramp input of 0.025ns and 4.3% to 1% for ramp input of 0.1ns for shorter line lengths(0.2cm). Moreover the rise time prediction is even better for proposed model than the two pole model where average error drops down to 12% from 141% for ramp input of 0.025ns and 4% to 21% for ramp input of 0.1ns for 0.2cm line lengths.

From Fig. 4.6 and Fig. 4.8 it is evident that even for RC dominant interconnects in shorter lines, proposed model is better than two pole model. For LC dominant

TABLE 4.12
COMPARISONS OF 50% DELAY AND RISE TIME FOR RAMP RESPONSE OF 0.1NS OF PROPOSED MODEL WITH CONVENTIONAL TWO POLE MODEL AND HSPICE. THE LINE LENGTH IS 0.2 CM. (EXAMPLE 4.3.1)

Width (μm)	Rs (Ω)	Cl (fF)	ζ	P	τ	HSPICE		Two Pole Model		Proposed Model	
						50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)
2	20	10	0.22	4.10	1.36	67.44	52.66	70.1	61.69	68.36	51.55
	50	50	0.45	3.68	1.22	79.72	66.36	82.18	76.04	80.17	69.01
	100	100	0.83	3.27	1.09	98.56	93.34	109.8	157.1	99.23	105.87
5	20	10	0.26	3.27	1.38	77.48	54.86	80.34	67.11	79.2	53.01
	50	50	0.58	3.06	1.30	92.04	73.47	94.78	90.01	92.37	75.8
	100	100	1.12	2.83	1.20	115.1	168.6	117.9	161.8	115.8	163.48
10	20	10	0.31	2.80	1.39	86.5	57.82	89.3	73.79	88.42	56.23
	50	50	0.71	2.67	1.33	79.72	66.36	82.17	76.03	80.17	68.9
	100	100	1.39	2.52	1.25	131	220.3	137.3	226.6	131.5	227.3
Average Error %								4.3	21.55	1.00	4.32
Maximum Error %								11.48	68.31	2.22	13.42

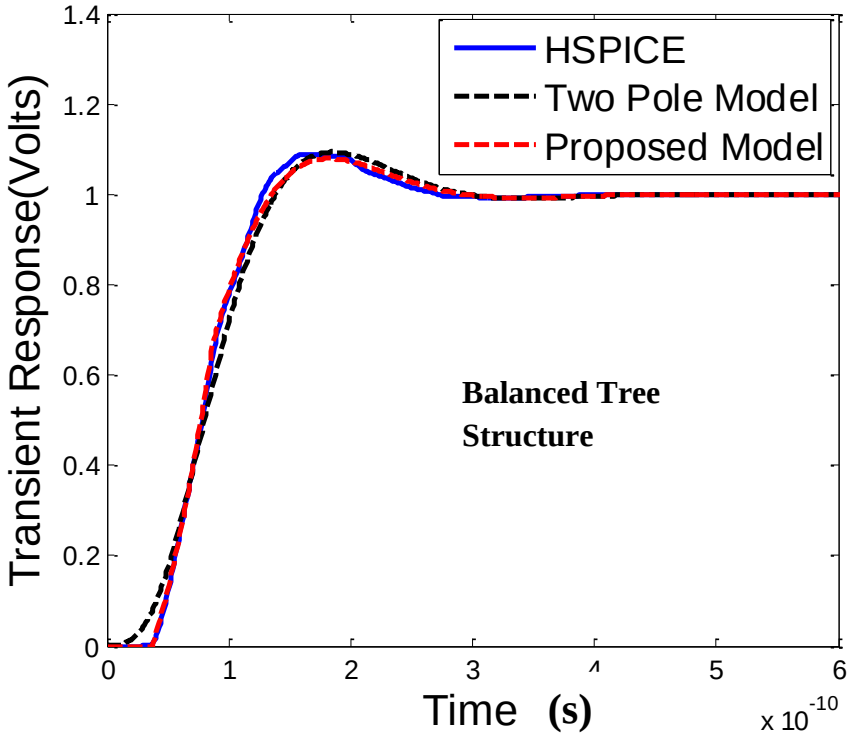
interconnects significant improvements are still visible.

Next the length of the line is increased to 0.5 cm. As it is expected the proposed model is giving even better results. For ramp input of 0.025ns the average error drops down to 3.% from 13% and for ramp input of 0.1ns average error drops from 7.28% to 2% .It is important to mention that as rise time of the ramp signal gets increased the results are becoming better which is discussed at the start of section 4.3. Like previous cases the prediction of rise time is excellent for proposed model as compared to two pole

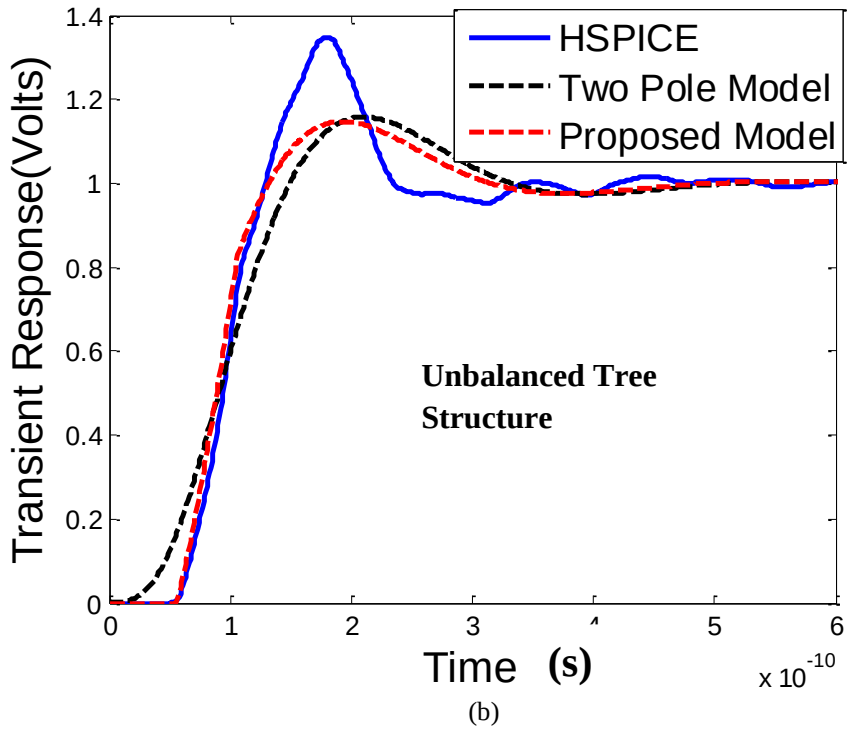
TABLE 4.13
COMPARISONS OF 50% DELAY AND RISE TIME FOR RAMP RESPONSE OF 0.1NS OF PROPOSED MODEL WITH CONVENTIONAL TWO POLE MODEL AND HSPICE. THE LINE LENGTH IS 0.5 CM. (EXAMPLE 4.3.1)

Width (μm)	Rs (Ω)	Cl (fF)	ζ	P	τ	HSPICE		Two Pole Model		Proposed Model	
						50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)
2	20	10	0.32	1.64	1.36	121.8	58.77	121.5	98.9	126.2	61.01
	50	50	0.53	1.53	1.27	135.3	74.09	136.5	127.79	136	77.2
	100	100	0.87	1.40	1.16	210.5	508.6	255.1	519.3	205.2	493.8
5	20	10	0.31	1.30	1.38	143.9	59.1	140.3	116.16	149.3	62.1
	50	50	0.63	1.25	1.32	159.4	79.5	161.3	167.17	159.3	81
	100	100	1.12	1.17	1.24	184	294.7	205.4	347.1	180.5	333.0
10	20	10	0.35	1.12	1.37	163.4	61.7	157.8	135.97	168.5	64.9
	50	50	0.75	1.08	1.34	181.5	86.4	187.4	222.57	180.1	88.4
	100	100	1.37	1.02	1.27	210.5	508.6	255.2	519.3	205.3	494.5
Average Error %								7.28	71.95	2.08	4.57
Maximum Error %								21.24	157.6	3.75	13

model. For ramp input of 0.025ns the average error drops down to 16% from 388% and for ramp input of 0.1ns average error drops from 71% to 4% in calculating rise time. The results validate that as the line length of interconnect and the slope of input ramp signal increase, the accuracy gets improved. Next sections will show the results for tree structure interconnects for ramp inputs.

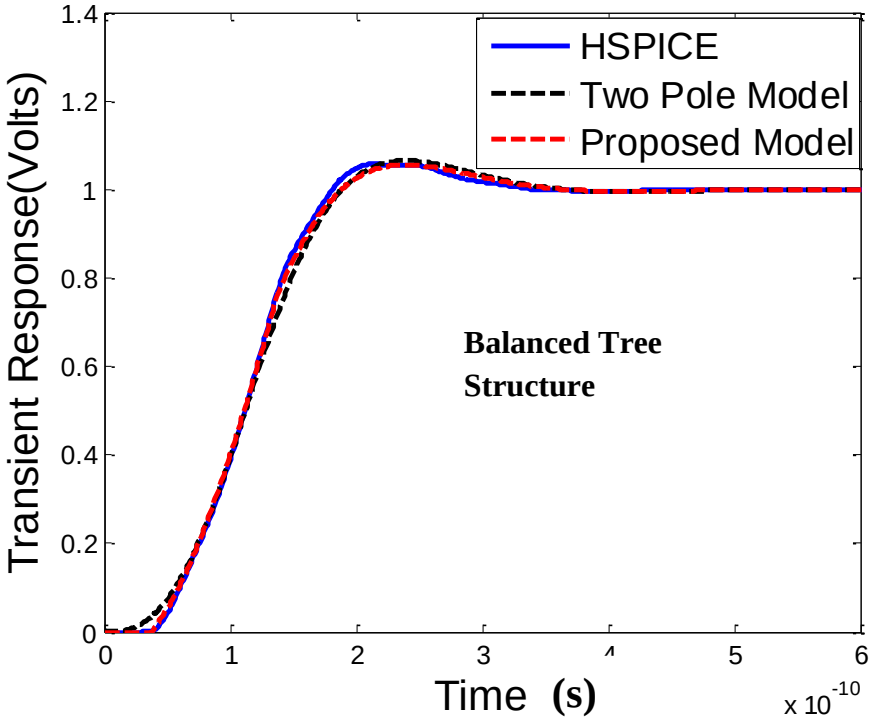


(a)

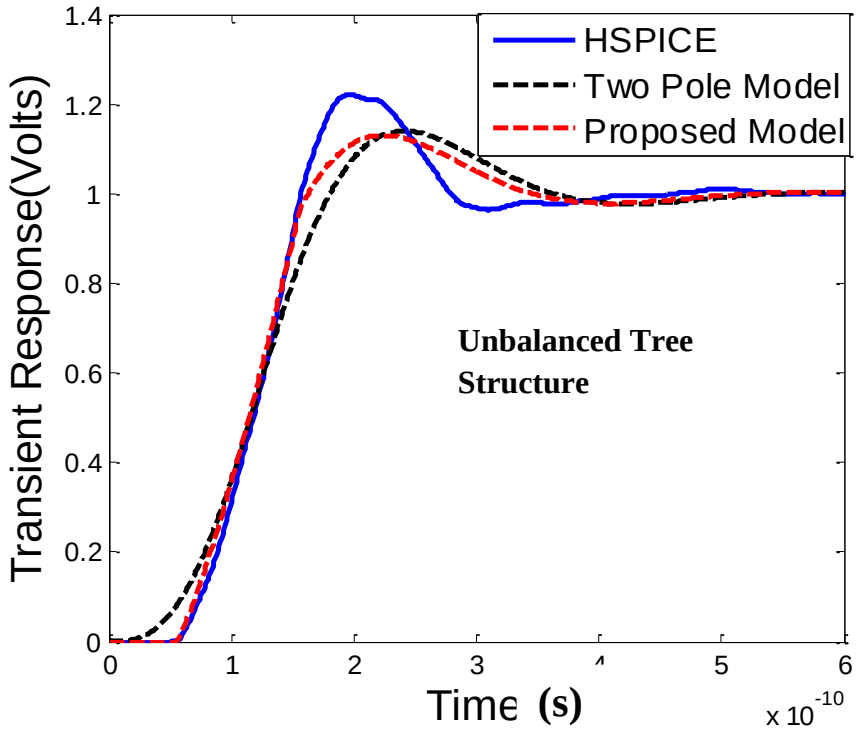


(b)

Fig. 4.10: Transient response of tree structure of node N_4 for ramp input of 0.05ns rise time
(a) Balanced Tree of Normalized line length l_x =0.1cm, Rs=10 Ω, C_x=80 fF.
(b) Unbalanced Tree of Normalized line length l_x =0.1cm, Rs=10 Ω, C_x=20 fF.



(a)



(b)

Fig. 4.11: Transient response of tree structure of node N_4 for ramp input of 0.1ns rise time
(a) Balanced Tree of Normalized line length l_x =0.1cm, Rs=10 Ω, C_x=80 fF.
(b) Unbalanced Tree of Normalized line length l_x =0.1cm, Rs=10 Ω, C_x=20 fF.

4.3.2 Example 2 – Symmetrical Tree Structure Interconnect

The symmetrical tree structure discussed in section 4.2.2 is analyzed in this section except the input is ramp signal of 0.05ns and 0.1ns. The far end time domain

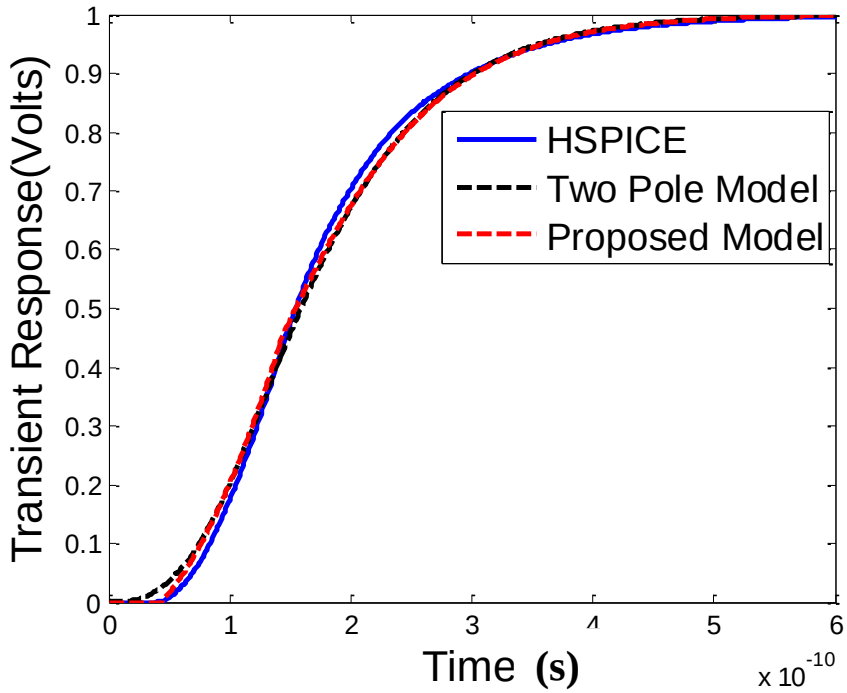
TABLE 4.14
COMPARISONS OF 50% DELAY AND RISE TIME FOR SYMMETRICAL TREE STRUCTURE INTERCONNECT OF PROPOSED MODEL WITH CONVENTIONAL TWO POLE MODEL AND HSPICE FOR RAMP INPUT OF 0.05NS. FOR TREE EXAMPLE OUTPUTS ARE OBSERVED AT NODE N_4

Example	l_x (cm)	Rs (Ω)	C_x (fF)	ζ	P	τ	HSPICE		Two Pole Model		Proposed Model	
							50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)
Balanced Tree	0.5	10	80	0.53	2.37	0.88	52.79	42.27	53.2	48.87	52.54	43.51
	0.5	10	200	0.59	2.05	0.77	58.28	49.68	58.37	55.9	57.8	52.52
	1	10	80	0.59	1.24	0.92	78.1	67.37	80.3	80.7	77.2	68.08
	1	10	200	0.63	1.13	0.85	82.94	74.3	86.3	90.5	81.69	80.5
Unbalanced Tree	0.5	10	20	0.42	2.00	1.12	57.0	35.5	55.56	48.5	56	38.1
	0.5	30	20	0.99	1.91	1.07	69.6	71.1	71.3	95	67.7	93.3
	0.5	10	500	0.63	1.07	0.60	92.5	70.2	89	96.3	88.6	94.2
	0.5	30	500	1.40	0.97	0.55	126.7	257.4	134.1	277.0	133.0	275.4
	1	10	20	0.5	0.99	1.11	94	53	88.8	88	90.3	52
	1	30	20	1.00	0.91	1.02	108.6	104	118.9	189.3	101.8	150.5
	1	10	500	0.65	0.64	0.72	136	107.1	133	157	126.5	142.6
	1	30	500	1.21	0.57	0.64	181	373	192	391	190.2	385.3
Average Error %									3.81	32.02	3.32	15.07
Maximum Error %									9.48	82.02	6.99	44.71

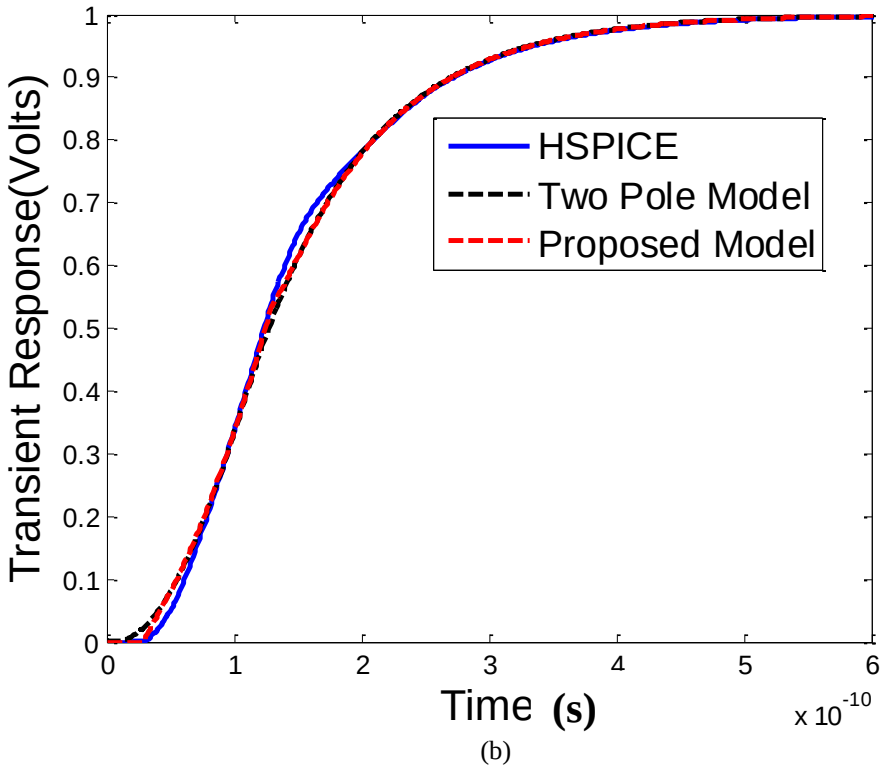
TABLE 4.15
COMPARISONS OF 50% DELAY AND RISE TIME FOR SYMMETRICAL TREE STRUCTURE INTERCONNECT OF PROPOSED MODEL WITH CONVENTIONAL TWO POLE MODEL AND HSPICE FOR RAMP INPUT OF 0.1NS. FOR TREE EXAMPLE OUTPUTS ARE OBSERVED AT NODE N_4

Example	l_x (cm)	Rs (Ω)	C_x (fF)	ζ	P	τ	HSPICE		Two Pole Model		Proposed Model	
							50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)
Balanced Tree	0.5	10	80	0.53	4.74	0.88	75.08	75.96	75.9	77.5	75.35	76.12
	0.5	10	200	0.59	4.11	0.77	81.84	79	82.62	82	82.12	79.9
	1	10	80	0.59	2.48	0.92	105.1	89.5	105.8	99.5	104.8	91
	1	10	200	0.63	2.27	0.85	111.6	98.5	112.3	108.7	111	101.9
Unbalanced Tree	0.5	10	20	0.42	3.99	1.12	75.52	62.6	77.73	73	76.1	67.6
	0.5	30	20	0.99	3.81	1.10	95.2	106.9	98.57	118	97.5	117.5
	0.5	10	500	0.63	2.14	0.60	117.5	91.5	116.5	113	116.8	112
	0.5	30	500	1.40	1.95	0.55	155	273	161.3	288	160.1	287.3
	1	10	20	0.50	1.98	1.11	117.9	74.8	115.6	103.3	115.1	79.1
	1	30	20	1.00	1.82	1.02	141.9	214	145.1	200.1	138.9	202.9
	1	10	500	0.65	1.29	0.72	160.4	121.3	158.8	167	152.8	155.1
	1	30	500	1.21	1.14	0.64	208.2	382.4	219	397.1	216.5	394.4
Average Error %									2.2	14.13	1.5	7.8
Maximum Error %									5.19	38.16	4.74	27.86

transient responses are plotted for balanced and unbalanced tree structure in Fig. 4.10 and Fig. 4.11 for 0.05ns and 0.1ns of rise time respectively. Table 4.14 and Table 4.15 show the corresponding results. Results clearly show that proposed model has improved the accuracy in calculating 50% delay and rise time for both cases.



(a)



(b)

Fig. 4.12: Transient response of unsymmetrical tree structure for ramp input of 0.1ns rise time
(a) Normalized line length l_x =0.05cm,Rs=10 Ω, C_x=100 fF. (Node 5)
(b) Normalized line length l_x =0.05cm, Rs=30 Ω, C_x=20 fF.(Node 7)

TABLE 4.16

COMPARISONS OF 50% DELAY AND RISE TIME FOR UNSYMMETRICAL TREE STRUCTURE INTERCONNECT OF PROPOSED MODEL WITH CONVENTIONAL TWO POLE MODEL AND HSPICE FOR RAMP INPUT OF 0.1NS. OUTPUTS ARE OBSERVED AT NODE N_5 AND NODE N_7

l_x (cm)	Rs (Ω)	C_x (fF)	Node	ζ	P	τ	HSPICE		Two Pole Model		Proposed Model	
							50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)	50% Delay (ps)	Rise Time (ps)
0.5	10	20	N_5	0.82	1.82	0.79	134.6	132.82	136.9	159.9	132.6	154.7
0.5	10	20	N_7	1.01	3.19	0.93	105.2	119.6	107.3	133.1	106.7	130.9
0.5	10	100	N_5	0.89	1.46	0.63	158.1	187	160.5	208	156.9	206.8
0.5	10	100	N_7	1.08	2.46	0.72	121.8	164.1	125.7	175.28	123.7	173.9
0.5	30	20	N_5	1.00	1.58	0.69	154.8	215.27	159.1	228.16	154.9	227.5
0.5	30	20	N_7	1.62	3.24	0.94	123.5	211.15	127.3	215.9	124.4	214.5
0.5	30	100	N_5	1.05	1.25	0.54	186.4	291.2	190.5	300	189	299.1
0.5	30	100	N_7	1.61	2.38	0.69	143.6	275.46	153.3	281.9	152.1	280.4
1	10	20	N_5	1.01	0.65	0.56	299.6	498.9	311	529.8	307.3	519.5
1	10	20	N_7	1.66	1.62	0.94	193.5	381.5	201.9	416.2	200	415.4
1	10	100	N_5	1.03	0.56	0.49	350.1	645.3	356.4	628	354	631.9
1	10	100	N_7	1.58	1.26	0.73	222.5	458.5	236	501.3	235.6	498.5
1	30	20	N_5	1.08	0.57	0.50	350	644.2	360.8	665.4	358.2	663.1
1	30	20	N_7	2.31	1.68	0.98	232	550.1	246.9	581.2	247	580.1
1	30	100	N_5	1.1	0.49	0.43	406.2	776.3	413.7	791.4	412.1	790.8
1	30	100	N_7	2.05	1.24	0.72	269.5	653	288.3	690.1	288.2	686.7
Average Error %									3.6	6.7	2.72	5.6
Maximum Error %									7	20.39	6.94	16.47

4.3.3 Example 3 – Unsymmetrical Tree Structure Interconnect

The same unsymmetrical tree structure discussed in section 4.3.2 is also analyzed in this section with ramp input of 0.1ns and the corresponding results are shown in Table 4.16 for node N_5 and node N_7. Transient responses of HSPICE, two pole model and proposed model are plotted in Fig. 4.12. Results from this example also validate the better accuracy of proposed model as compared to two pole model.

4.3.4 Summary of the Results

For the case of ramp inputs, the output voltage at the time point of the extracted delay ($t = T_d$) is always less than the 50% of the input signal ($V_{out}(t = T_d) \leq 0.5V_{DD}$). As a result, overall results of single line, symmetrical and unsymmetrical tree structure interconnect is always better for the proposed model than the conventional two pole model.

4.4 Conclusions

In this work, a delay extraction based equivalent Elmore model is proposed for on-chip RLC interconnects. In the proposed scheme, the time of fight signal delay is extracted without increasing the number of poles or affecting the stability of the transfer function. The proposed algorithm is used for both unit step and ramp inputs of different rise times. Usually in the case of unit step inputs, for very short lines of *RC* dominant interconnects two pole model and proposed model gives similar accuracy. However for

all *LC* dominant interconnects proposed algorithm predicts 50% delay and rise time more precisely for both longer and shorter lines. In the case of ramp inputs proposed method is usually more accurate for both *RC* and *LC* dominant interconnects. For the unbalanced and unsymmetrical tree structure interconnects, the expression of the transfer function is complicated and there exists higher order poles in the hyperbolic functions. The transient responses of unbalanced tree networks are far more complicated than balanced tree networks. As a result instead of using two poles, sometimes higher order poles are required in order to capture more accurate time domain transient responses. As we increase the rise time of ramp inputs the accuracy is getting better which is shown in those examples. Since we extract the delay of the interconnect, the rise time calculation has always better for all examples. In the end we can say this algorithm yields significant improvements of two pole model.

Chapter 5

Conclusions

5.1 Summary

This thesis describes a delay extraction based analytic model for on-chip RLC interconnects used in VLSI circuits. The rapid decrease in feature size and associated growth in circuit complexity, coupled with higher operating speeds, has made the analysis of on-chip interconnects a critical aspect of system reliability, speed of operation, and cost. Since the overall circuit performance depends mostly on the delay of interconnects rather than the delay of devices, designers must consider the effect of interconnects at the early stages of the design cycle to ensure circuit performance and reliability.

Chapter 2 reviewed the closed form interconnect modeling that has been developed over the years. The analysis of on-chip interconnects can be performed using simulation techniques such as SPICE, however they are computationally expensive in early stage of layout optimization when dealing with millions of logic gates. As a result the importance of closed form analytical formulas has been emphasized. Closed-form analytic formulas require per unit length resistance, inductance and capacitances (R, L, C). How these electrical parameters can be extracted from the physical parameters has been discussed in this chapter. Closed form formulas have the difficulty of numerical integration problem because of Telegraphers partial differential equations. Those equations can provide an exact transfer function for the far end response in the frequency

domain but not in the time domain. Therefore in chapter 2, single-pole Elmore-based RC model was mentioned. Due to the limitations of RC model, equivalent Elmore based RLC models were discussed and it was shown how two pole approximations are done using moment matching techniques. Expressions for 50% delay and rise time were given for two pole model. Even though Elmore based two pole model have the limitations of capturing long signal delay and high-frequency effects caused by inductive dominant *RLC* lines, this model still has been widely used to analyze integrated circuits composed of millions of gates, since it is often impractical and time consuming to use accurate modeling techniques to evaluate the signal delay at each node in the circuit.

In Chapter 3, the proposed algorithm has been developed. Since Elmore based models rely on one or two-pole transfer functions to estimate the delay, these approximations are not capable of capturing the early transient responses required for predicting long signal delays and rise times. As a result, a delay extraction based equivalent Elmore model has been proposed to improve the accuracy of two-pole models for RLC interconnects. The proposed algorithm extracts the time of fight delay to obtain a delay rational approximation without increasing the number of poles or affecting the stability of the transfer function. Unit step and ramp inputs are applied to get the time domain response at the far end. From this analysis, analytic fitted expressions are derived for the 50% delay and rise time for unit step response. A look up table has been proposed to predict those parameters for ramp inputs. Since the time of flight delay is extracted from the transfer function, the proposed algorithm provides a mechanism to improve the accuracy of two-pole Elmore-based models.

In Chapter 4, numerical examples are provided to demonstrate the validity of the proposed method. Single line and symmetrical and unsymmetrical tree structure examples (both balanced and unbalanced) are given using different line lengths and different RLC parameters. Algorithm is tested for both unit step and ramp inputs of different rise times. Numerical examples illustrate improved 50% delay and rise time estimates when compared to traditional Elmore based two-pole models.

The proposed model provides several advantages in compared to traditional two pole model for analysis of on-chip interconnects. Since number of poles does not increase, there is no question of instability. Therefore this model still maintains the stability of the system. Also for inductive dominant interconnects and longer line lengths this algorithm improves the results of Elmore based RLC models without significantly increasing the computational complexity.

5.2 Future Work

The analysis of on-chip interconnect mainly focuses on the timing aspects but with increasing operating speed and decreasing feature size, energy consumption of these interconnects is also important. In VLSI circuits an increasing portion of energy is dissipated in interconnects [60]. As a result the demand for accurate and efficient model for energy dissipation in on-chip interconnects has also been intense area for research as technology scales down. This is particularly true when inductance effect is dominant and when the width of the interconnect structure increases [60].

In order to model the energy consumption for on-chip RLC interconnects, accurate prediction of driving point impedance and transition time (which is rise time) of

the output voltage is very important [60]. The proposed delay extraction algorithm may provide better estimation of the driving impedance. However this model surely gives better prediction of the rise time of the output signal. As a result this model may provide improved results for energy consumption in on-chip interconnects.

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CURRICULUM VITAE

PERSONAL INFORMATION

Name: Shamsul Arefin Siddiqui

Place of Birth: Dhaka, Bangladesh

Date of Birth: 23rd September, 1987

RESEARCH INTERESTS:

Modeling of on-chip interconnects for signal integrity verification, development of simulation algorithms of high speed VLSI circuits & systems, MEMS devices, digital circuit design, determination of chirality of carbon nanotube.

ACADEMIC BACKGROUND:

- Master of Engineering Science (M.E.Sc.) in Electrical and Computer Engineering from University of Western Ontario, London, Ontario, Canada.
- Bachelor of Science (B.Sc.) in Electrical and Electronic Engineering from Bangladesh University of Engineering and Technology (BUET) , Dhaka , Bangladesh

PROFESSIONAL EXPERIENCE:

- Graduate Research Assistant under the supervision of Dr. A. Dounavis, Department of Electrical and Computer Engineering, University of Western Ontario from Sept., 2010 till present.
- Graduate Teaching Assistant, Department of Electrical and Computer Engineering, University of Western Ontario from Sept. 2010 till present.
- Lecturer, Department of Electrical and Electronic Engineering, American International University-Bangladesh (AIUB) from Jan. 2010 to Aug. 2010

ACADEMIC AWARDS RECEIVED

- Awarded **Dean's List Scholarship** in 2nd, 3rd, 4th academic year of undergraduate level (2006-2009) from Bangladesh University of Engineering and Technology (BUET) , Dhaka , Bangladesh
- Awarded **University Merit Scholarship** in 2nd, 3rd, 4th academic year of undergraduate level (2006-2009) from Bangladesh University of Engineering and Technology (BUET) , Dhaka , Bangladesh
- Awarded **Board Scholarship** by Higher Secondary Education Board, **Government of Bangladesh**, 2005-2009
- Awarded **Board Scholarship** by Secondary Education Board, **Government of Bangladesh**, 2003-2004