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Low Power AC-DC and DC-DC Multilevel Converters

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Graduate Program in Electrical and Computer Engineering
A thesis submitted in partial fulfillment of the requirements for the degree in Doctor of Philosophy
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By

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Graduate Program in Engineering Science

Department of Electrical and Computer Engineering

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Abstract

AC-DC power electronic converters are widely used for electrical power conversion in many industrial applications such as for telecom equipment, information technology equipment, electric vehicles, space power systems and power systems based on renewable energy resources. Conventional AC-DC converters generally have two conversion stages – an AC-DC front-end stage that operates with some sort of power factor correction to ensure good power quality at the input, and a DC-DC conversion stage that takes the DC output of the front-end converter and converts it to the desired output DC voltage. Due to the cost of having two separate and independent converters, there has been considerable research on so-called single-stage converters – converters that can simultaneously perform AC-DC and DC-DC conversion with only a single converter stage. In spite of the research that has been done on AC-DC single-stage, there is still a need for further research to improve their performance.

The main focus of this thesis is on development of new and improved AC-DC single-stage converters that are based on multilevel circuit structures (topologies) and principles instead of conventional two-level ones. The development of a new DC-DC multilevel converter is a secondary focus of this thesis. In this thesis, a literature survey of state of the art AC-DC and DC-DC converters is performed and the drawbacks of previous proposed converters are reviewed. A variety of new power electronic converters including new single-phase and three-phase converters and a new DC-DC converter are then proposed. The steady-state characteristics of each new converter is determined by mathematical analysis, and, once determined, these characteristics are used to develop a procedure for the design of key converter components. The feasibility of all new converters is confirmed by experimental results obtained from proof-of-concept prototype converters. Finally, the contents of the thesis are summarized and conclusions about the effectiveness of using multilevel converter principles to improve the performance of AC-DC and DC-DC converters are made.

KEY WORDS: Single-Phase AC-DC Rectifiers, Three-Phase AC-DC Rectifiers, Power Factor Correction, Single-Stage Converters, DC-DC Converters, Multilevel Converters.

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Last but not least I would like to thank my wife and my parents for their love and support without which I could not have been able to make it through the frustrations of the past few years.

To my lovely wife

and

my parents

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Acronyms

AC	Alternate Current
DC	Direct Current
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
EMI	Electro-Magnetic Interference
MOSFET	Metal Oxide Silicon Field Effect Transistor
PF	Power Factor
PFC	Power Factor Correction
PWM	Pulse Width Modulation
PSM	Phase Shift Modulation
RMS	Root Mean Square
SSPFC	Single-Stage Power Factor Correction
THD	Total Harmonic Distortion
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZVZCS	Zero Voltage Zero Current Switching
TL	Three Level

Abbreviations

v	Volt
A	Ampere
$\mathbf{V_{in}}$	Input Voltage
$\mathbf{V_o}$	Output Voltage
$\mathbf{I_{in}}$	Input Current
$\mathbf{I_o}$	Output Current
$\mathbf{V_{rec}}$	Rectified AC Voltage
$\mathbf{V_{dc}}$	DC Voltage
$\mathbf{V_{ab}}$	Differential Voltage Between Node 'a' and Node 'b'
D	Duty Cycle
$\mathbf{f_{sw}}$	Switching Frequency
t	Time
$\mathbf{C_O}$	Output Capacitor
$\mathbf{L_O}$	Output Inductor
$\mathbf{R_o}$	Output Resistive Load
$\mathbf{L_{in}}$	Input Inductance
$\mathbf{D_x}$	Diode x
$\mathbf{S_x}$	Diode x
µ	Micro
k	Kilo
H	Henry
F	Farad

Chapter 1

1. Introduction

Power electronics is the application of semiconductor devices for the control and conversion of electric power. Power electronic converters can be found in any application that needs to modify a form of electrical energy (i.e. change its voltage, current or frequency). They can be classified according to the type of the input and output. As a result, power electronic converters can be;

- AC to DC (rectifier)
- DC to DC
- DC to AC (inverter)
- AC to AC

The main focus of the research for this thesis has been mainly on AC-DC with so-called multilevel or three-level structures, with some of this work extended to DC-DC converters. In this thesis, several new converter topologies are proposed, their steady-state characteristics are determined by mathematical analysis, and their design is examined. The feasibility of each proposed converter is confirmed with experimental results obtained from a proof-of-concept prototype and the main points of the thesis are summarized at the end.

1.1. Single-Phase AC-DC Converters (Rectifiers)

AC-DC converters are typically used in many industrial and commercial applications including personal computers, battery chargers, telecommunication power supplies, etc. Switch mode AC-DC converters are the first block in any power conversion system that supplies power from an AC source such as the utility mains to any load. An AC-DC power supply should operate in such a way that the input current and voltage are purely sinusoidal and in phase with each other to comply with harmonic standards and thus ensure a good input power factor [1]. Such harmonic standards include IEC 1000-3-

2 [2], IEC 1000-3-4 [3] and IEEE-519-1992 [4]. As a result, power factor correction (PFC) techniques are typically used in AC-DC power converters to ensure that these standards are met.

The concept of power factor originated from the need to quantify how efficiently a power converter utilizes the current that it draws from an AC power system. The true power factor at the power converter is defined as the ratio of average power to apparent power, or

$$pf_{true} = \frac{P_{avg}}{P_{app}} \tag{1.1}$$

If the power factor is less than one, they have to supply more current to the power converter for a given amount of power use.

1.1.1. Power Factor Correction Techniques

There are several PFC techniques that can be used to remove current harmonics and thus improve the overall system power factor. The two main methods to eliminate or at least reduce the input line current harmonics are

- Passive power factor correction
- Active power factor correction

1.1.1.1. Passive Power Factor Correction

One of the simplest and most straightforward methods to reduce input current harmonics is by using passive circuits. A passive circuit consisting of passive reactive elements can be located either at the input or at the output side of the input rectifier of an AC-DC converter. Several passive PFC techniques have been investigated in the literature, such as adding an LC filter at the output of the diode bridge rectifier, as shown in Fig.1.1. Passive PFC techniques have several advantages and disadvantages. High efficiency, low EMI and simple implementation are the advantages of these techniques, but the main drawback is that they make the converter heavy and bulky. This drawback limits the applications in which passive PFC methods can be used [5].
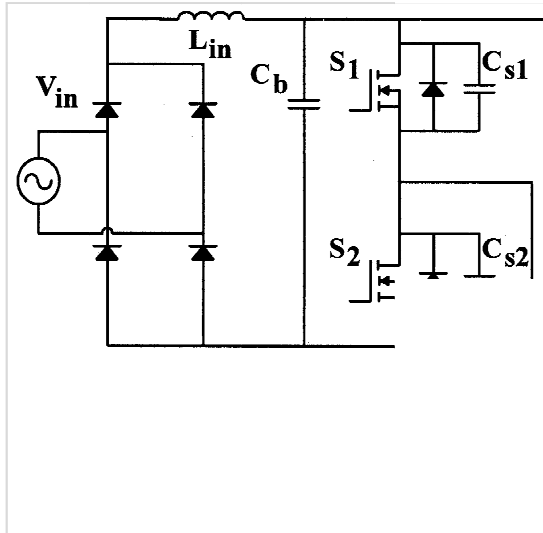
Fig.1.1. Two-stage AC-DC PWM converter

1.1.1.2. Active Power Factor Correction

Active power factor correction (PFC) techn

the input current drawn by the AC-DC converter

the input voltage waveform; therefore, the input

has many advantages over passive PFC such a

content, smaller converter size due to the ability

lighter weight. Active PFC methods, however

passive PFC methods because of the challenges

converter [5].

There are two general types of active

transformer isolation: two-stage PFC techniques

techniques are discussed below.

A. Two-Stage PFC Converter

Typical AC-DC power converters with tra

two converter stages: an AC-DC conversion (re

conversion stage. A block diagram of a two-stage

AC-DC boost converter is used in the rectifying stage for most applications and it actively shapes the input line current so that it is almost sinusoidal, with a harmonic content compliant with agency standards. The input current can either be discontinuous or continuous. The DC-DC converter is used to regulate the output voltage and it can be a forward, a flyback or any other step down isolated DC-DC converter.
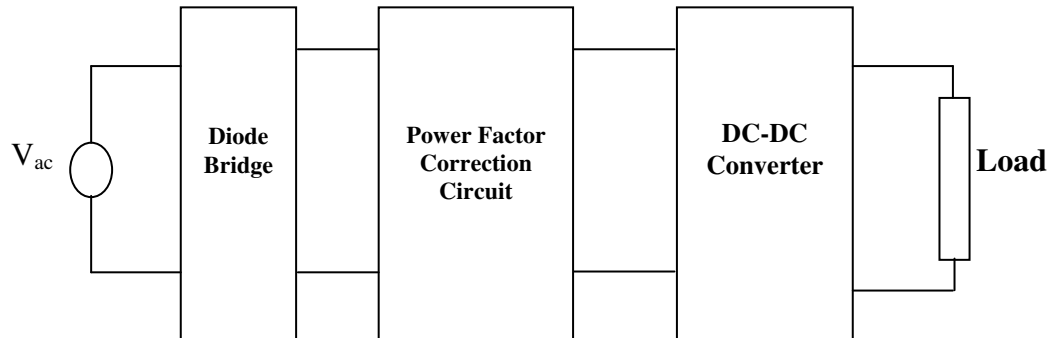
Fig.1.2. Block diagram of standard two-stage PFC AC-DC converter.

B. Single-Stage PFC Converter

Although two-stage PFC converters are attractive because they can operate with a high input power factor, they can be expensive because they have two switch-mode converters in their topologies. The cost and complexity of the overall two stage converter has led to the emergence of single-stage power-factor-corrected (SSPFC) converters. Efforts have been made to develop smaller converters with fewer switches that can comply with regulatory agency standards and be more cost effective than two-stage converters, with the same performance. SSPFC circuits are required to provide the features of both the power factor correction in addition to those of the DC-DC converter cascaded with it.

1.1.2. Review of Single-Phase Single-Stage PFC Converters

There have been numerous publications about SSPFC converters, particularly for low-power AC-DC flyback and forward converters [6]–[24]. These cheaper and simpler converters are widely used in industry and their properties and characteristics have been

well established. Research on the topic of higher power AC-DC single-stage full-bridge converters, however, has proved to be more challenging, and thus there have been much fewer publications [25]-[32].

Previously proposed single-stage AC-DC full-bridge converters can be classified as belonging among the following types:

- **_Resonant converters:_** These converters have resonant elements such as inductors and capacitors that are connected in series and/or parallel to the primary of their power transformer [27], [32]. They must be controlled using variable switching-frequency control. As a result, it is difficult to optimize their design (especially their magnetic components) as they must be able to operate over a wide range of switching frequency.

- **_Current-fed PWM converters:_** These converters have a boost inductor connected to the input of the full-bridge circuit; one such converter is shown in Fig. 1.3. Although they can achieve a near-unity input power factor, they lack an energy-storage capacitor across the primary-side dc bus, which can result in the appearance of high voltage overshoots and ringing across the dc bus. The lack of such a capacitor also causes the output voltage to have a large low-frequency 120-Hz ripple that limits their application.
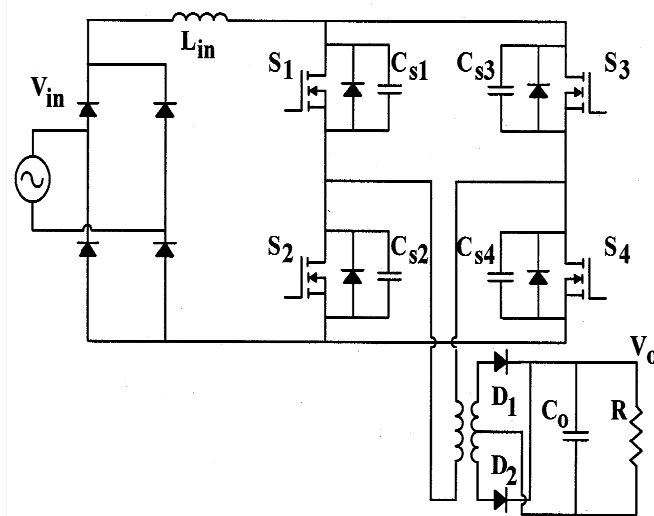
Fig.1.3. Boost-based current-fed AC-DC PWM integrated full-bridge converter [26].

- ***Voltage-fed PWM converters:*** These converters have a large energy-storage capacitor connected across their primary-side dc bus [26], [28]-[31], as shown in Fig.1.4. These converters do not have the drawbacks of resonant and current-fed SSPFC converters. They operate with fixed switching frequency, and the bus capacitor prevents voltage overshoots and ringing from appearing across the dc bus and keeps the 120-Hz ac component from appearing at the output.
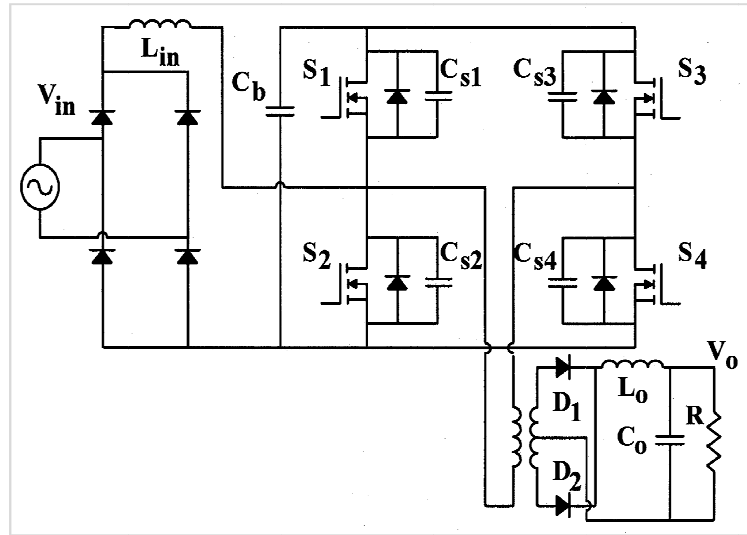
(a) Voltage-fed PWM full-bridge converter [26]
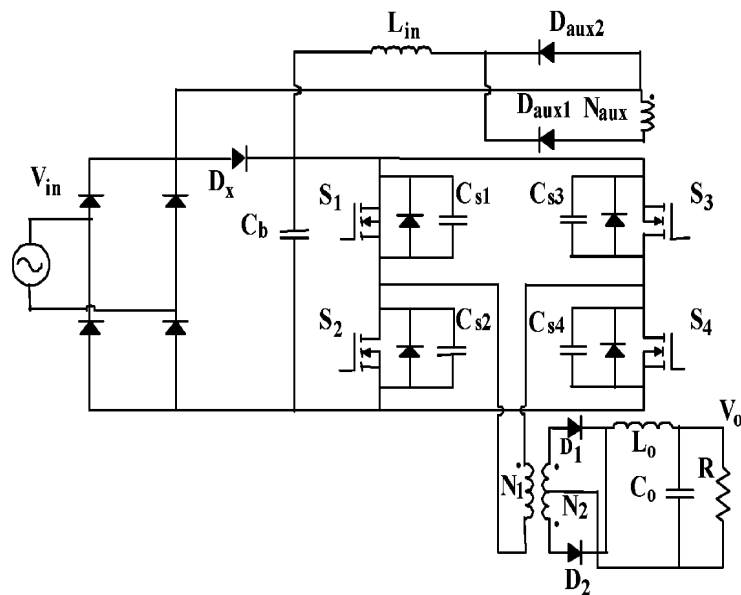
(b) Voltage-fed PWM full-bridge converter with auxiliary winding [28]

Fig.1.4. Some voltage-fed PWM full-bridge converters.

Although voltage-fed, single-stage PWM full-bridge converters seem to be the most promising single-stage converters, they have disadvantages that have limited their use. Most of these drawbacks are because

- They are controlled by a single-controller and the dc bus voltage is left unregulated;

- They are implemented with two-level topologies that subject the converter components to high voltage stresses.

Due to these disadvantages, voltage-fed converters have the following drawbacks:

- The primary-side dc bus voltage of the converter may become excessive under high-input-line and low-output-load conditions. Since the dc bus voltage is left unregulated, it is dependent on the converter's input line and output load operating conditions and component values. The high dc bus voltage results in the need for higher voltage rated devices and very large bulk capacitors for the dc bus. For example, the converters in [26], [28]-[29] have a dc bus voltage of 600 V.

- The input power factor of a single-stage voltage-fed converter is not as high as that of current-fed converters. For example, the converter proposed in [28] has an input current that is neither continuous nor discontinuous, but is "semi-continuous" with a considerable amount of distortion.

- The converter operates with an output inductor current that is discontinuous for all operation conditions. This results in the need for components that can handle high peak currents, and additional output filtering to remove ripple [26]-[32].

Most of the drawbacks of voltage-fed SSPFC PWM converters are due to the fact that their switches can be exposed to very high voltages (> 800 V). The converter can be designed to limit this voltage by decreasing the output inductor or increasing the input

inductor, but doing so results in the above-mentioned drawbacks. If the converter can somehow be designed so that its switches are exposed to less voltage, then there will be less need to degrade the performance of the converter.

DC-AC multilevel converters that limit the voltage that their switches are exposed to half the dc bus voltage have been proposed in the power electronics literature and are widely used in high voltage, low switching frequency applications [33]-[39]. They limit the switch voltage by using two bulk capacitors across the dc bus instead of one so that the midpoint of the bulk capacitors, which is half the dc bus voltage, can be used as a connection point in the converter. Attempts have been made by researchers to implement voltage-fed multilevel AC-DC SSPFC converters as a way to relax the switch stress limitations placed on non-multilevel (two-level) converters, such as in [27], [32] and [40]-[45]. Although these converters are promising, they still have many of the problems of previously proposed two-level SSPFC converters stated above such as distorted input currents, discontinuous output currents, and the need for variable switching frequency.

1.2. Three-Phase AC-DC Converters (Rectifiers)

In the later chapters of this thesis, an investigation will be made on whether concepts that can be used for single-phase multilevel SSPFC converters can be extended to higher power three-phase converters. In this section, previously proposed three-phase SSPFC converters are reviewed and their drawbacks are stated.

1.2.1. Review of Three-Phase Single-Stage PFC Converters

As with single-phase AC-DC power conversion, three-phase AC-DC power conversion with input power factor correction (PFC) and transformer isolation is typically done using two converter stages - a six-switch front-end ac-dc converter is used to do the PFC and the dc bus voltage regulation and a four-switch full-bridge converter is used to do the DC-DC conversion. This two-stage approach, however, is expensive and complicated – even more so with three-phase converters than with single-phase converters - as it needs ten active switches along with associated gate drive and control

circuitry. Moreover, the converter must be operated with sophisticated control methods that require the sensing of certain key parameters such as the input currents and voltages; this is especially true if online PWM techniques are used.

Researchers have tried to reduce the cost and complexity of the standard converter by modifying the AC-DC front end converters. Proposed alternatives have included:

- Using three separate AC-DC boost converter modules as shown in Fig.1. 5 [46]. Although the modularity of this approach makes it attractive, it needs three switch-mode converters making it expensive and complex.

- Using a reduced switch AC-DC converter as shown in Fig.1.6 [47] as the first stage converter of a two-stage converter. Although this approach is cheaper than conventional two-stage converters that use six-switch converters as the first stage converter, it is only modestly so.

- Using a single-switch boost converter as shown in Fig.1.7 [48]. Although this approach reduces the cost of the first stage AC-DC converter considerably, two separate switch-mode converters are still needed to perform three-phase AC-DC power conversion with transformer isolation.
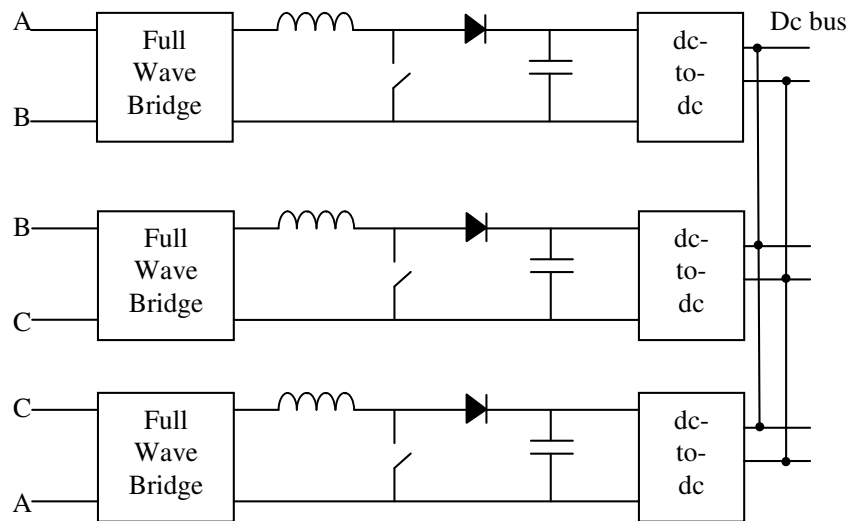
Fig.1.5. Three separate AC-DC boost converter modules [46].
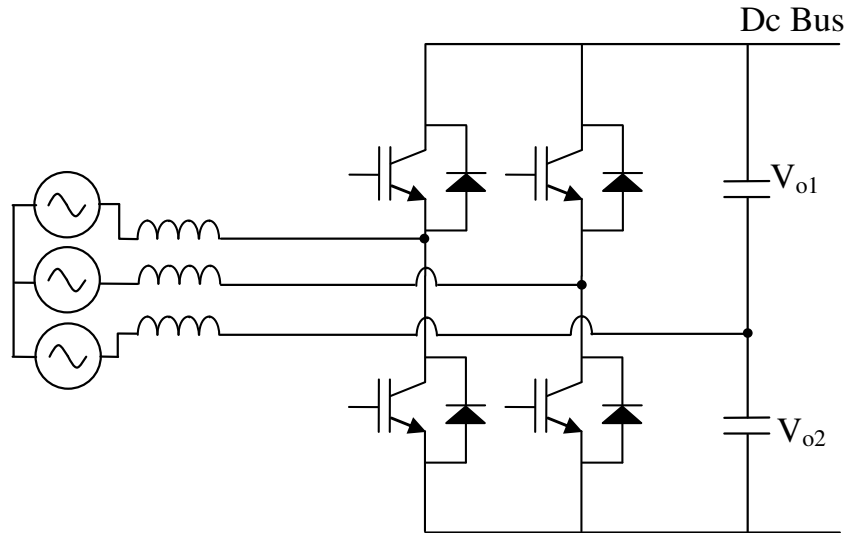
Fig.1.6. Reduced switch AC-DC converter [47].
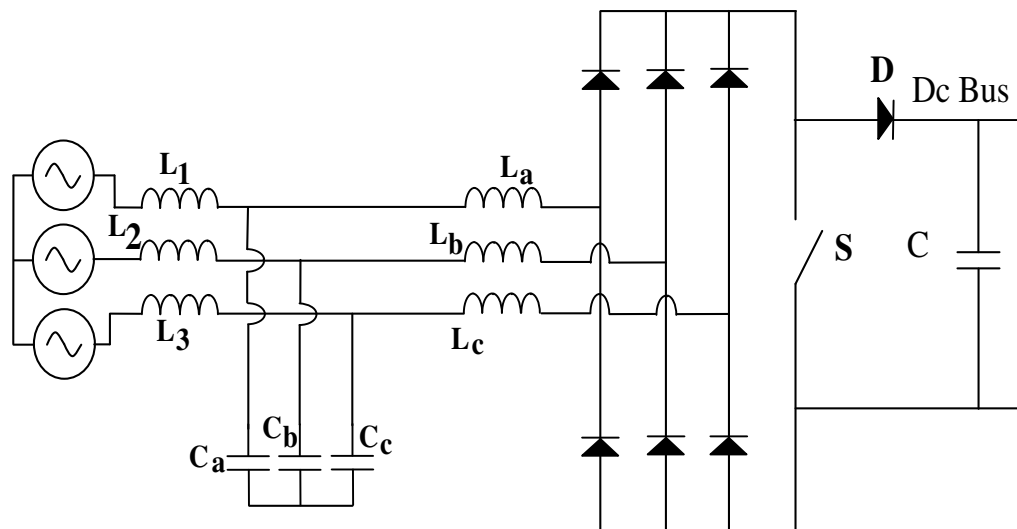
Fig.1.7. Single-switch boost converter [48].

Researchers have tried to further reduce the cost and complexity associated with three-phase AC-DC power conversion and PFC by proposing single-stage converters that integrate the functions of PFC and isolated DC-DC conversion in a single power converter [49]-[58]. Several examples of single-stage converters are shown in Fig.1.8. These single-stage converters, however, have similar drawbacks as those of single-phase

SSPFC that have limited their widespread use. Since these drawbacks are the same as those discussed above for single-phase converters, they are not discussed here.
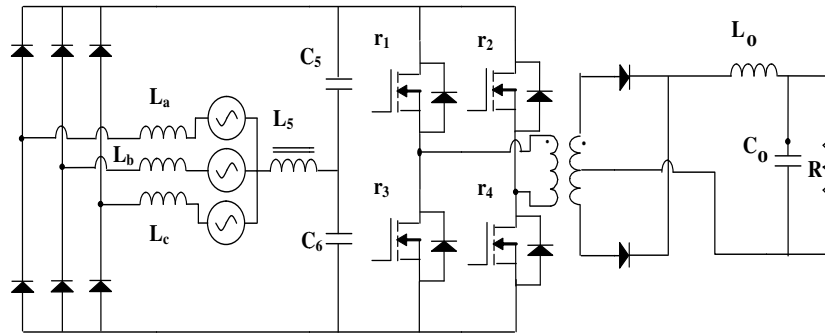
(a) [50]
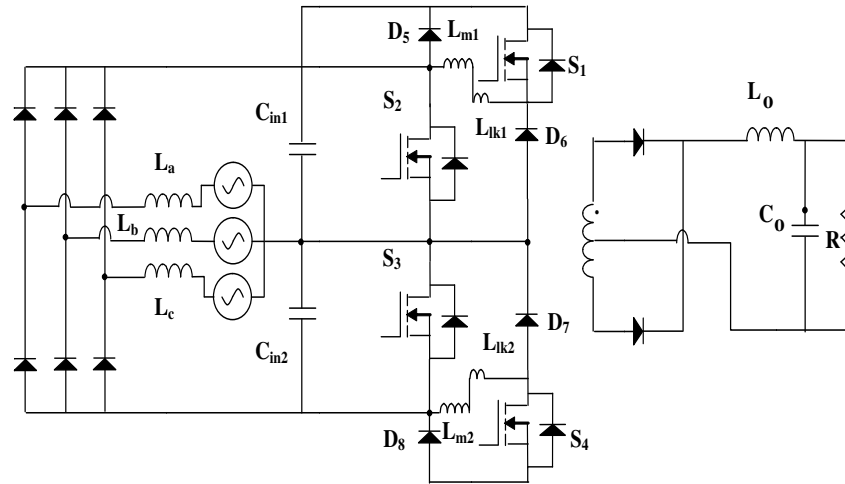
(b) [51]
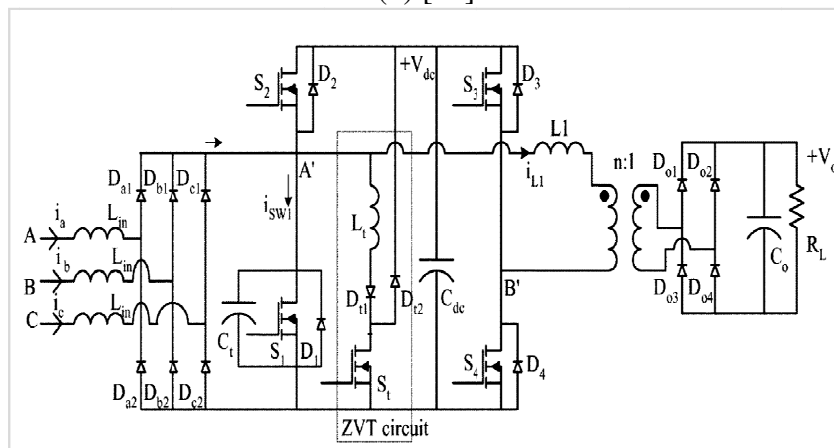
(c)[52]

Fig.1.8. Three-phase, single-stage, AC-DC converters.

Since the problems associated with three-phase SSPFC converters are similar to those of single-phase SSPFC converters, it would seem that the solutions to these problems would be similar as well. It is not automatic, however, that a single-phase solution is appropriate for three-phase converter and vice versa, that a three-phase solution can be implemented in a single-phase converter. This is because of the different power levels and the fact that some topologies make use of the three-phase neutral connection, which is not possible in single-phase converters.

1.3. DC-DC Converters

Although the main focus of this thesis is on single-phase and three-phase multilevel SSPFC converters, the use of multilevel converter concepts to improve the performance of DC-DC full-bridge converters is investigated in this thesis. The conventional two-level PWM full-bridge DC-DC converter is shown in Fig.1.9 [59]. The way this converter works is as follows: The converter is in an energy-transfer mode when a pair of diagonally opposed switches is on and the input DC voltage is impressed across the transformer primary. The converter is in what is called a freewheeling mode of operation when a pair of top switches (S_1, S_3) or bottom switches (S_2, S_4) is on and no voltage is impressed across the transformer.

The converter operates with inherent soft switching (ZVS) turn-on of its switches as available primary transformer energy is used to discharge the output capacitances of the switches just before they are turned on. This is especially true when the converter is operating under heavy load conditions, but not so for light load conditions as there is less current flowing in the converter. Thus, less available transformer energy exists to discharge the output capacitances of the switches.
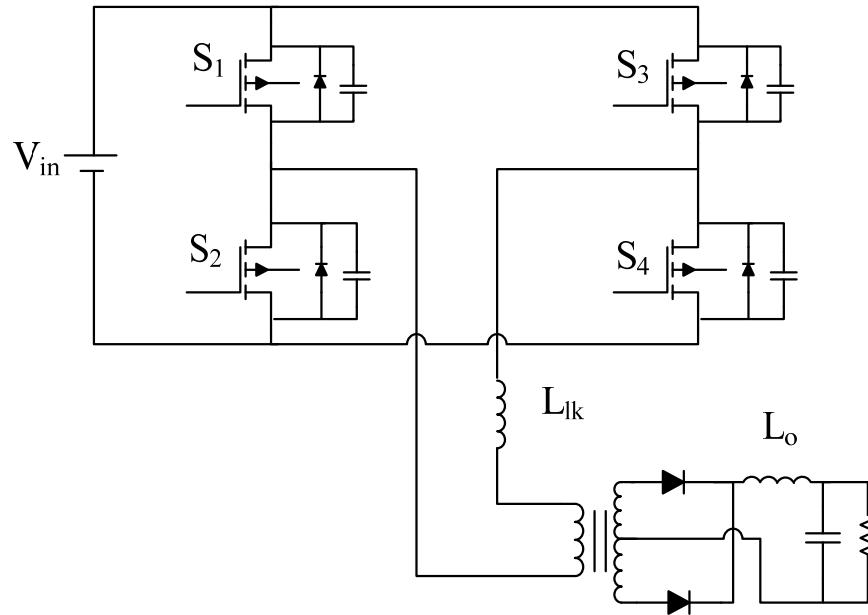
Fig.1.9. DC-DC isolated full-bridge converter [59].

1.3.1. Review of DC-DC Converters

The two-level ZVS-PWM full-bridge (ZVS-PWM-FB) converter has two key drawbacks that relate to efficiency:

- Circulating current
- Light load operation

These drawbacks are discussed in detail below.

1.3.1.1.   Circulating Current

The load range over which the converter can operate with ZVS can be increased if the amount of current that circulates in the transformer primary side of the converter is also increased. This can be done by reducing the transformer primary to secondary turns ratio or by adding some passive circuitry to the converter's primary that allows for more current flow [60]-[64]. Increasing the amount of current circulating in the primary, however, results in an increase in conduction losses and switch turn-off losses and these

losses can offset any gains in efficiency due to ZVS. The end result is that although the ZVS range may be extended, the load range over which there is an advantage for doing so may not be as expected and heavy load efficiency may suffer as well.

A number of power electronics researchers have tried to take the opposite approach and try to reduce primary circulating current in the ZVS-PWM-FB converter as much as possible – particularly when the converter is in a freewheeling mode of operation when either both of its top or both of its bottom switches are on. In this case, no voltage is impressed across the transformer primary and current just circulates in the transformer primary during this mode and contributes to conduction losses as no energy is transferred to the output from the primary side and current. Researchers have thus proposed zero-voltage-zero-current methods to eliminate freewheeling mode circulating current [65]-[70], but this results in the loss of ZVS in some of the converter switches.

Circulating current and ZVS capability are inversely related as more circulating current means a wider load range for ZVS operation as there is more energy available to discharge the switch output capacitances, but more conduction losses and turn-off losses. It is, therefore, standard practice for ZVS-PWM-FB converter designs that the range of ZVS operation be limited to loads greater than 25%-50% full-load so that conduction losses caused by circulating current do not become excessive.

1.3.1.2. Light Load Efficiency

As the use of electrical equipment and consumer electronics has exploded due to the demands of society, the issue of light load efficiency has become more urgent in recent years because of the need to conserve as much energy as possible. Consequently, there has been increased interest by power electronics personnel to improve light load efficiency of their converters. What this means is the standard practice for ZVS-PWM-FB converter designs that the range of ZVS operation be limited to loads greater than 25%-50% full-load is becoming less acceptable.

When the converter is operating with a light load, there is less current flowing in the converter and thus less available transformer energy to discharge the output

capacitances of the switches. This means that the converter switches do not turn on with ZVS and thus have switching losses. Since the losses caused by the energy that is stored in the switch output capacitances and dissipated in the switches when they are turned on are fixed, they become dominant when the converter operates with light load and thus the ZVS-PWM-FB converter has poor efficiency.

It was proposed in [59] to improve light load efficiency by adding a separate optimally designed "mini-converter" to the main converter that would operate only when under light load conditions in place of the main power converter. Although this approach did improve light load efficiency significantly, it did so at the expense of increased cost and complexity as the mini-converter required two additional active switches and needed to be operated with sophisticated control methods.

1.4. Thesis Objectives

In order to mitigate the drawbacks that two-level converters have, new three-level multilevel AC-DC and DC-DC converters are proposed in this thesis. The main advantage that three-level converters have over two-level converters is that their main power switches are exposed to half the voltage that the switches in two-level converters are exposed to. This advantage can be used to improve converter efficiency and to improve converter performance in general. The main objectives of this thesis are as follows:

- To propose a new single-phase, single-controller, AC-DC multilevel converter that has improved steady-state characteristics and improved performance than other previously proposed converters of the same type.
- To propose modifications to this new converter that result in improved performance.
- To determine how the new converter operates with a second controller that is dedicated to regulating its transformer primary-side DC bus voltage.
- To determine whether the principles associated with the new single-phase converter can be extended to three-phase converters.

- To propose a new three-phase AC-DC multilevel converter that has inherent interleaved operation that reduces the input current ripple.

- To propose a new multilevel DC-DC converter that takes advantage of the multilevel concepts derived from the research to improve performance.

- To determine the steady-state characteristics of all new converters proposed in the thesis so that they can be properly designed.

- To derive design procedures for all new converters proposed in the thesis.

- To confirm the feasibility of all new converters proposed in this thesis with experimental results obtained from proof-of-concept prototypes.

1.5. Thesis Outline

The thesis is comprised of the following six chapters. Following is a briefing of each chapter;

In Chapter 2, a new three-level, single-stage single-phase power-factor-corrected (SSPFC) AC-DC PWM converter that operates with a single controller is proposed. The proposed converter can operate with universal input voltage (90– 265 Vrms) and with better performance than previously proposed converters of the same type. The operation of the new converter is explained in detail and analyzed, and its steady-state characteristics were determined. The converter's design is discussed and a design procedure is established and demonstrated with an example. Experimental results obtained from a prototype are presented to confirm the feasibility of the new converter and its ability to meet IEC 1000-3-2 standards for electrical equipment.

In Chapter 3, two modifications to the SSPFC converter introduced in Chapter 2 are proposed. The first modification is the addition of a simple auxiliary circuit that allows the converter to operate with improved output characteristics without compromising its light-load performance. The second modification is to make some change to the original converter topology to allow it to operate with conventional pulse shift modulation. The

two modifications are discussed in the chapter and their effectiveness in improving converter performance is confirmed with experimental results.

The operation of the single-stage converter proposed in Chapter 2 with two controllers in examined in Chapter 4. The second controller is used to regulate the intermediate dc bus voltage on the primary side of the main power transformer, which is standard practice in two-stage AC-DC converters. The converter's operation with two controllers and the design of the converter is discussed in the chapter. The effect of the second controller on the converter's operation is studied based on experimental results obtained from a prototype converter.

In Chapter 5, the single-phase converter proposed in Chapter 2 is modified for three-phase operation to determine if the concepts and principles associated with this converter can be extended to three-phase operation. The new three-phase converter is then modified by implementing it with interleaved sections. The operation of both new three-phase SSPFC multilevel converters are explained in detail and analyzed, their steady-state characteristics are determined, and their design is examined discussed. The feasibility of the converters is confirmed with experimental results obtained from prototype converters.

The multilevel concepts examined in previous chapters of the thesis are used to develop a new three-level DC-DC converter that is proposed in Chapter 6. In the chapter, the basic operation of the converter is explained, its features are stated, and its design is investigated. The feasibility of the converter is experimentally confirmed with results obtained from a prototype converter.

In Chapter 7, the contents of the thesis are summarized, the conclusions that have been reached as a result of the work performed in thesis are presented, and the main contributions of the thesis are stated. The chapter concludes by suggesting potential future research that can be done based on the thesis work.

Chapter 2

2. Single-Phase Single-Stage Three-Level Power Factor Correction AC-DC Converters

2.1. Introduction

Voltage-fed, single-stage power factor correction (SSPFC) full-bridge converters are attractive because they cost less than two-stage converters, but their use has been limited because of the drawbacks that they have. Most of these drawbacks are because they are controlled by a single controller that regulates the output voltage so that the dc bus voltage is left unregulated. As a result, the primary-side dc bus voltage of these converters may become excessive under high-input-line and low-output-load conditions. Measures can be taken to limit the dc bus voltage so that does not become excessive, but these measures affect the performance of voltage-fed, SSPFC full-bridge converters in several ways, including the following:

- The input power factor of a single-stage voltage-fed SSPFC converter is not as high as that of current-fed converters.
- The output inductor current of a single-stage voltage-fed SSPFC converter is discontinuous for all operation conditions, which results in higher secondary-side component peak current stresses.

The performance of voltage-fed, SSPFC full-bridge converters can be improved if the limit on the dc bus voltage (typically < 450 V) is relaxed. This is not something that can be done for SSPFC full-bridge converters that are based on two-level topologies, but this can be done for converters that are based on three-level, multilevel topologies as the primary-side switching devices of these converters are exposed to half the peak voltage stress that those of two-level converters are. As a result, the dc bus voltage limit can be doubled for multilevel converters, but the peak voltage stress of the switches is the same as that of two-level type topologies.

In this chapter, a new AC-DC SSPFC PWM multilevel converter is proposed. The basic operation of the converter is explained as are the various modes of operation that the converter goes through during a switching cycle. The steady-state characteristics of the converter are determined by mathematical analysis and are used to develop a procedure for the design of key converter components. The feasibility of the new converter is confirmed with results that were obtained from an experimental prototype.

2.2.   A New Single-Phase Single-Stage Three-Level Power Factor Correction AC-DC Converter

One of the new AC-DC multilevel SSPFC converters that is proposed in this work is shown in Fig.2.1. The proposed converter is a novel, efficient and cost effective single-phase voltage-fed SSPFC that can operate with universal input voltage range (90– 265 V_{rms}) with wide output load variation (from 10% of full load to a full load that is greater than 500 W), fixed frequency PWM control, excellent power factor, a continuous output inductor current for load more than 50%, without its components being exposed to excessive peak voltage stresses. This combination of features does not exist in the present power electronics literature.

2.3.   Operation of the Proposed Converter

The proposed converter, shown in Fig.2.1, consists of an AC input section, a three-level DC-DC converter, and dc link circuitry that is based on auxiliary windings taken from the main power transformer and that contains an inductor L_{in} and two diodes. The dc link circuit acts like the boost switch in an AC-DC PFC boost converter. Whenever two converter switches are ON, a voltage is impressed across each auxiliary winding so that the voltage across one of the windings cancels out the voltage across the dc link capacitors (sum of the voltage across C_1 and C_2). This is analogous to the boost switch being ON and current in L_{in} (which can be considered to be the boost inductor) rises. Whenever only one converter switch is ON, no voltage is impressed across any of the auxiliary windings so that there is no voltage cancellation of the dc link voltage.
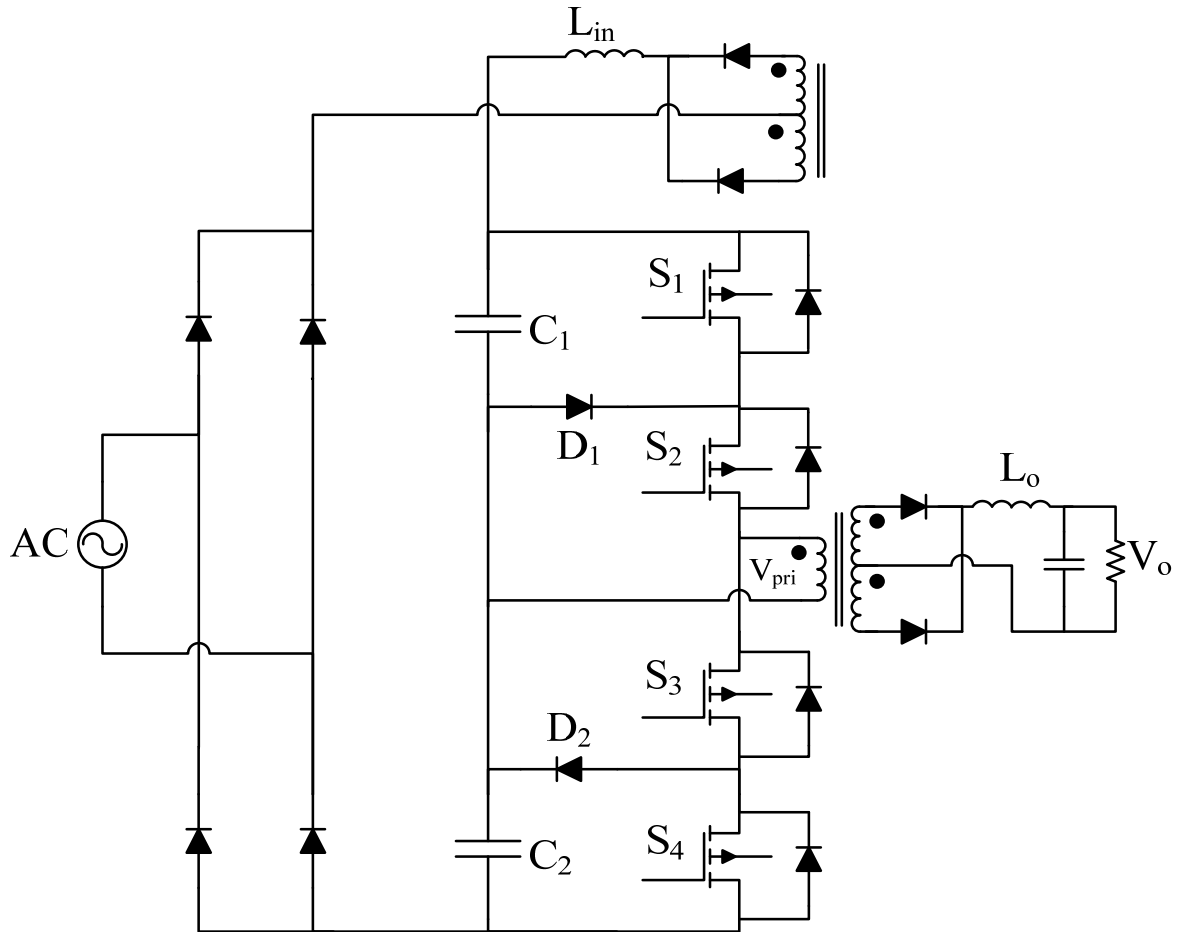
Fig.2.1. Proposed single-stage three-level converter.

This is analogous to the boost switch being OFF and current in L_{in} falls. If the converter is designed so that it operates with a constant duty cycle and a discontinuous L_{in} current throughout the line cycle, then input PFC can be achieved without introducing any significant low frequency component to the output as the peak current in L_{in} tracks the sinusoidal wave shape of the rectified supply voltage.

Typical converter waveforms are shown in Fig.2.2, and equivalent circuit diagrams that show the converter's modes of operation are shown in Fig.2.3 and 2.4 with the diode rectifier bridge output replaced by a rectified sinusoidal source and thick lines representing the paths of current conduction. The converter has the following modes of operation:
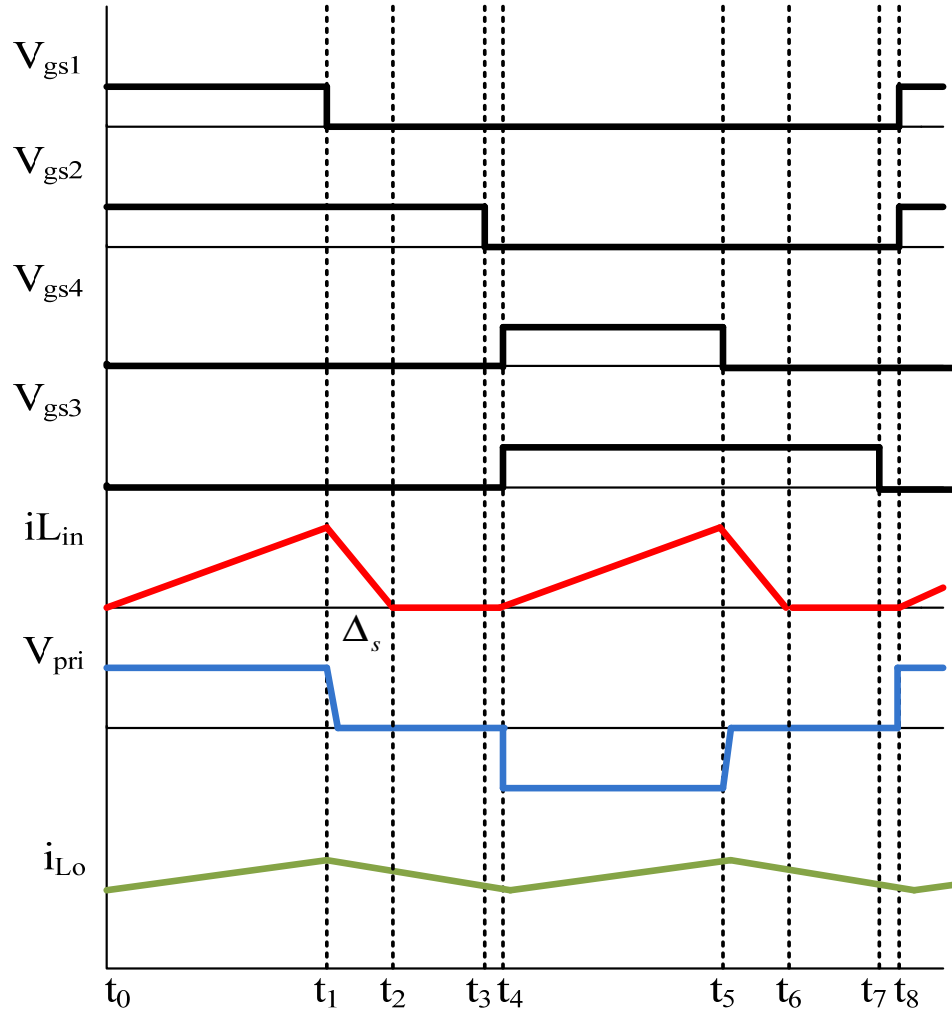
Fig.2.2. Typical waveforms describing the modes of operation.

Mode 1 (t₀ < t < t₁): During this mode, switches S_1 and S_2 are ON and energy from the dc-link capacitor C_1 flows to the output load. Since the auxiliary winding generates a voltage that is equal to the total DC-link capacitor voltage (sum of C_1 and C_2), the voltage across the auxiliary inductor is the rectified supply voltage.

This allows energy to flow from the AC mains into the auxiliary inductor during this mode, and the auxiliary inductor current increases, according to

$$i_{L_{in,k}}(t) = \frac{|v_{s,k}|}{L_{in}} \cdot t \qquad (2.1)$$
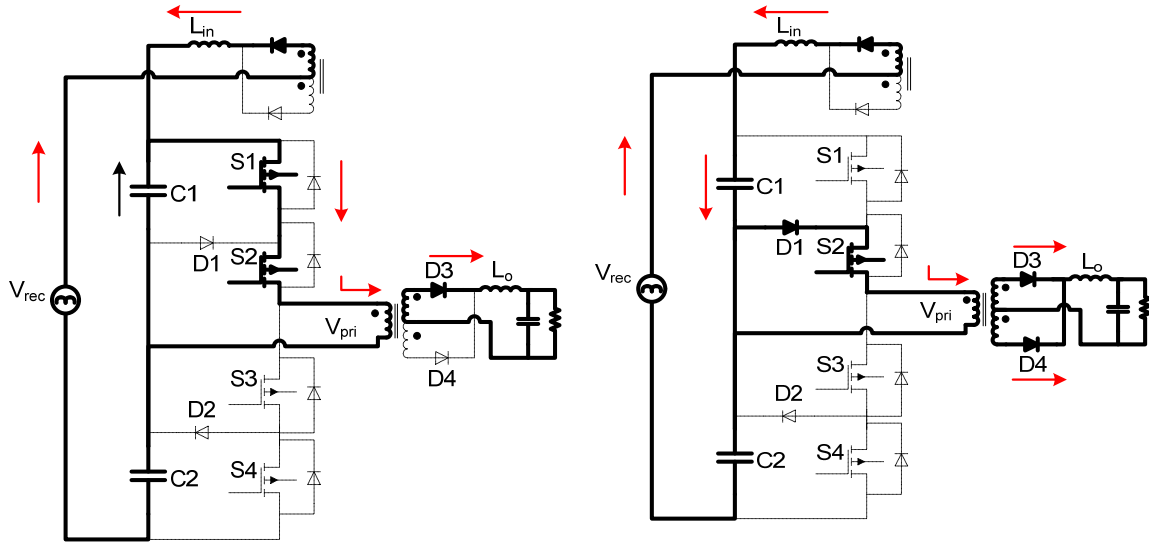
(a) Mode 1 ($t_0 < t < t_1$)

(b) Mode 2 ($t_1 < t < t_2$)
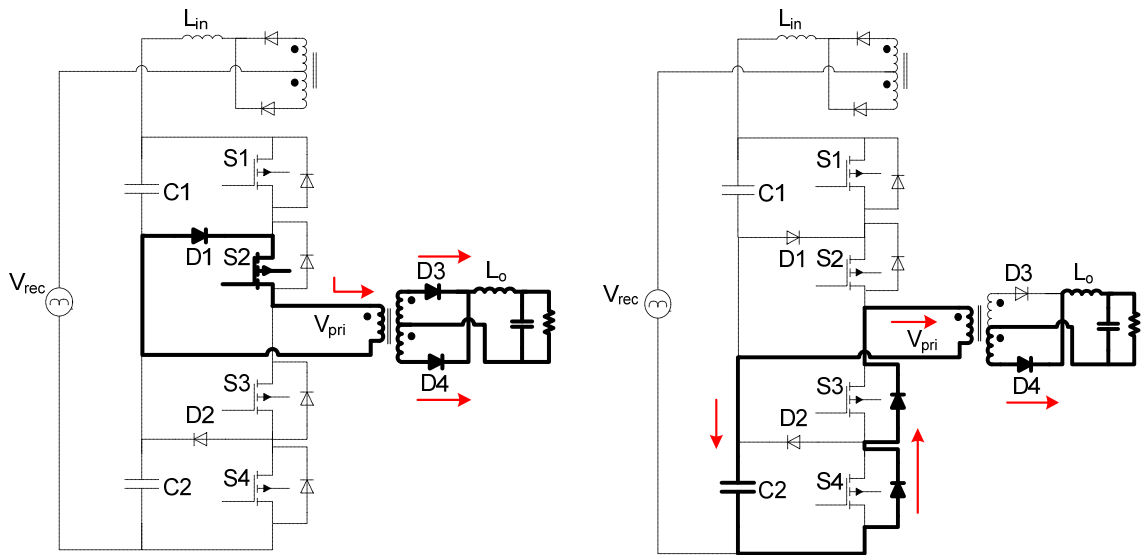
(c) Mode 3 ($t_2 < t < t_3$)

(d) Mode 4 ($t_3 < t < t_4$)

Fig.2.3. Modes of operation. (Mode 1-4)

where $|v_{s,k}|$ is the rectified AC supply voltage during switching cycle interval k. The supply voltage can be considered to be constant within a switching cycle as the switching frequency is much higher than the line frequency. The current in the auxiliary inductor L_{in} at the end of Mode 1 is

$$i_{L_{in,k,max}} = \frac{|v_{s,k}|}{L_{in}} \cdot \frac{D}{2f_{sw}}$$

(2.2)

Duty cycle, D, is defined as the time when S_1 and S_2 are both ON during the first half cycle or when S_3 and S_4 are both ON during the second half cycle. These two cases correspond to energy transfer modes of operation. Since D is defined with respect to a half switching cycle $T_{sw}/2$ or $1/2f_{sw}$, (where f_{sw} is the switching frequency) the duration that is used in equ. (2.2) is $D/(2f_{sw})$.

Similarly, the output inductor current can be expressed as;

$$i_{L_o}(t) = \frac{(V_{bus}/2N) - V_L}{L_o} \cdot t$$

(2.3)

where V_{bus} is the average DC-link voltage, V_L is the load voltage and N is the transformer ratio between input and output ($N = N_{pri}/N_{sec}$). If the output inductor current is continuous then peak ripple current can be expressed as

$$\Delta i_{L_o} = \frac{(V_{bus}/2N) - V_L}{L_o} \cdot \frac{D}{2f_{sw}}$$

(2.4)

Mode 2 ($t_1 < t < t_2$): S_1 is OFF and S_2 is ON during this mode. The energy stored in L_{in} during the previous mode is completely transferred into the DC-link capacitor. The amount of stored energy in the auxiliary inductor depends upon the rectified supply voltage. This mode is a freewheeling mode as the primary current freewheels through S_2

and D_1 and the output inductor current freewheels through both secondary diodes. This mode ends when the current in L_{in}, i_{Lin}, reaches zero.

Since the voltage across L_{in} during this mode is $|V_{s,k}| - V_{bus}$, i_{Lin} can be expressed as

$$i_{Lin,k}(t) = i_{Lin,k,max} - \frac{V_{bus} - |v_{s,k}|}{L_{in}}.t \tag{2.5}$$

The duration of this mode can be expressed as $\Delta_{s,k}/2f_{sw}$. Using this expression along with (2.2) and (2.5) with $i_{Lin,} = 0$ gives

$$\Delta_{s,k} = \frac{|v_{s,k}|}{V_{bus} - |v_{s,k}|}.D \tag{2.6}$$

Equation (2.6) shows that the duration of this mode is time varying along one ac supply period. In order to assure a discontinuous input current, $\Delta_{s,k}$ must satisfy the expression $D + \Delta_{s,k} < 1$ at any interval k and load conditions. Using (2.6), this constraint can be written as

$$V_{bus} > \frac{|v_{s,k}|}{1-D} \tag{2.7}$$

An expression for the output inductor current can be obtained by noting that the voltage across the output inductor is equal to $-V_L$; this current can be expressed as

$$i_{Lo}(t) = i_{Lo,max} - \frac{V_L}{L_o}.t \tag{2.8}$$

The peak output ripple current can be expressed as

$$\Delta i_{Lo} = -\frac{V_L}{L_o}.\frac{1-D}{2f_{sw}} \tag{2.9}$$

and the following can be obtained from (2.4) and (2.9):

$$V_o = \frac{V_{bus}}{2N} \cdot D \qquad\qquad (2.10)$$

Mode 3 ($t_2 < t < t_3$): S_2 is the only switch that is ON during this mode. There is no current flowing through L_{in} and the converter remains in a freewheeling mode.

Mode 4 ($t_3 < t < t_4$): No converter switch is ON during this mode as the current in the transformer primary charges capacitor C_2 through the body diodes of S_3 and S_4. This mode ends when switches S_3 and S_4 are switched on and a symmetrical half-period begins. The output inductor current continues to freewheel in the secondary of the transformer during this mode.

Mode 5($t_4 < t < t_5$): This Mode is the same as Mode 1 except that S_3 and S_4 are ON and energy flows from capacitor C_2 into the load.

Mode 6 ($t_5 < t < t_6$): This Mode is the same as Mode 2 except that S_3 is ON.

Mode 7 ($t_6 < t < t_7$): This Mode is the same as Mode 3 except that the primary current circulates through S_3 and diode D_2.

Mode 8 ($t_7 < t < t_8$): This Mode is the same as Mode 1 except that the current in the primary of the transformer charges capacitor C_1 through the body diodes of S_1 and S_2. This mode ends when the S_1 and S_2 are turned ON and the converter reenters Mode 1.
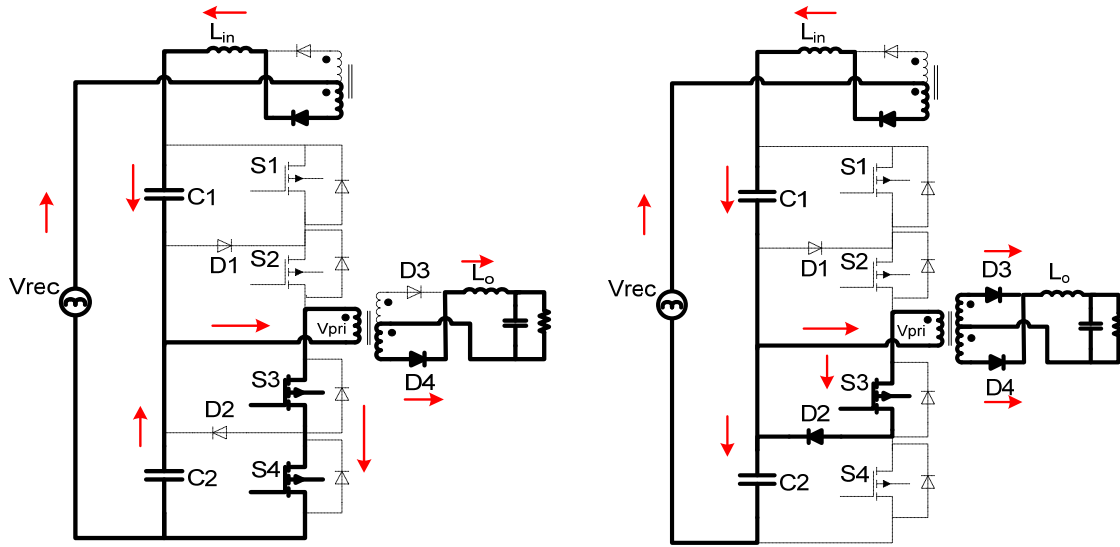
(a) Mode 5 ($t_4 < t < t_5$)

(b) Mode 6 ($t_5 < t < t_6$)
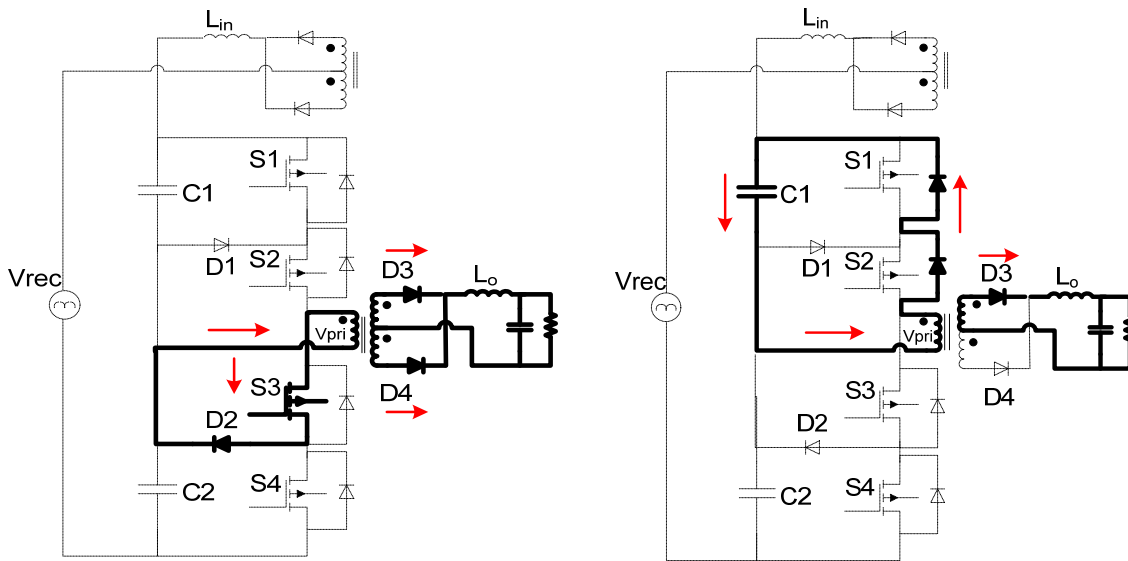
(c) Mode 7 ($t_6 < t < t_7$)

(d) Mode 8 ($t_7 < t < t_8$)

Fig.2.4. Modes of operation. (Mode 5-8)

2.4.   Features of the Proposed Converter

The Proposed converter has the following features:

- The converter can operate with universal input voltage range (90– 265 Vrms) with wide output load variation (from 10% of full load to a full load that is greater than 500 W).

- The converters provide high power factor at input ac line current that complies with the IEC1000-3-2. It is because it can have higher dc bus voltage.

- The converter can operate with continuous output inductor current for load more than 50% without its components being exposed to excessive peak voltage stresses.

- The voltage stress for each switch is just half of the dc bus voltage due to multilevel structure.

2.5.   Steady State Analysis

The key parameter that must be derived from an analysis of any integrated converter is the DC-link voltage because it is only then that other parameters such as input current can be determined. Unlike a conventional two-stage converter, this voltage is not regulated by a separate AC-DC boost PFC stage and varies considerably, depending on the line and load; however, it can be determined for any set of operating conditions by noting that an energy equilibrium must exist for the dc-link capacitors when the converter is in steady-state operation. The energy pumped into the capacitors from the input section must be equal to the energy that they provide to the output, so that the net dc current flowing in and out of must be zero during a half-line cycle.

This energy equilibrium, however, cannot be determined using equations with closed-form solutions due to the various possible combinations of input and output modes of operation; it must instead be determined using a computer program. If it is assumed that the converter has ideal semiconductors and an ideal transformer with no leakage inductance and negligible magnetizing current, then the dc-link voltage can be determined for any operating point with a given input voltage V_{in} , output voltage V_L , switching frequency f_{sw}, input inductor L_{in}, output inductor L_o, transformer turns ratio $N = N_{pri}/N_{sec}$, and output current I_o can be determined as follows:

1) Assume a duty cycle D as an initial "guess" (i.e., D=0.5).

2) Assume that the output current is continuous then use (2.10) to find V_{bus}

$$V_{bus} = \frac{2V_0 N}{D}$$

(2.11)

With this value of V_{bus}, verify that the output current is continuous by seeing that the peak output current ripple does not exceed the average current I_o

$$\frac{1}{2}\frac{\frac{V_{bus}}{2N} - V_o}{L_o} \cdot \frac{D}{2f_{sw}} < \frac{P_o}{V_o}$$

(2.12)

If this relation is satisfied, then V_{bus} is equal to the value determined in (2.11). If not, then the output current is discontinuous and V_{bus} must be determined using (2.13), which has been derived for DCM

$$V_{bus} = 2N.\frac{V_0 + \sqrt{V_o^2 + \frac{16P_o \cdot L_o \cdot f_{sw}}{D^2}}}{2}$$

(2.13)

With V_{bus} known, find the average current that flows out of the capacitors during a half-line cycle using either (2.14) for CCM or (2.15) for DCM

$$I_{C_{bus,out-avg}} = \frac{I_o \cdot D}{2N} \tag{2.14}$$

$$I_{C_{bus,out-avg}} = \frac{D^2}{4N.L_o.f_{sw}} \cdot \left(\frac{V_{bus}}{2N} - V_o\right) \tag{2.15}$$

Determine the average current that is fed from the input to the capacitors during a half-line cycle using

$$I_{C_{bus,in-avg}} = 2f_{in}. \sum_{k=0}^{m} \int_{t^*}^{t_k} \left[\frac{v_{in,k} - V_{bus}}{L_{in}}(t - t^*) + I_{in,k}^*\right].dt \tag{2.16}$$

$I_{in,k}^*$ is the peak input current value during a switching cycle k. If (2.16) is equal to (2.14) or (2.15), then the converter is confirmed to be operating under steady-state conditions and the value of V_{bus} that has been calculated is valid. If not, then the operating point for which is to be determined is not a valid operating point and the procedure must be repeated for a different value of D. The flowchart shown in Fig.2.5. shows the full analysis procedure.

This procedure can be repeated to determine V_{bus} (or any other parameter) for multiple operating points so that graphs of steady-state characteristic curves can be generated for design purposes. The converter operating characteristics for any given input and output voltage are dependent on three key parameters: transformer turns ratio N, input inductance L_{in} and output L_o. The effect that each of these parameters has on V_{bus} can be seen with graphs of characteristic curves that have been generated with a computer program based on the procedure described above, varying the parameter while keeping the others fixed.

Such graphs are shown in Fig.2.6. Based the following observations can be made based on these graphs:

- It can be seen in Fig.2.6 (a) that V_{bus} decreases as the transformer turns ratio N is decreased and all the other parameters are kept constant.

- It can be seen in Fig.2.6 (b) that V_{bus} decreases as L_{in} is increased and all other parameters are kept constant.

- It can be seen from Fig.2.6 (c) that V_{bus} rises as L_o is increased and all the other parameters are kept constant. Varying L_o has a slight effect on V_{bus} for higher output loads when the output is operating in CCM, but has a more pronounced effect at lower output loads when the output is in DCM.

- Fig.2.6 (d) shows the effect of input voltage on the dc-link voltage. As can be seen, increasing the input voltage increases the dc-link voltage as well.

```
                    ┌─────────────────────┐
                    │  Initial value for D │
                    └──────────┬──────────┘
                               ▼
        ┌──────────────────────────────────────┐
   ┌───▶│ Output is CCM and    V_bus = 2V_o N/D │
   │    └──────────────────┬───────────────────┘
   │                       ▼
  Yes                                          No
  Output is CCM              ◇               Output is DCM
          ┌────────────────◇ ◇────────────────┐
          │         (1/2)·((V_bus/2N − V_o)/L_o)·(D/2f_sw) < P_o/V_o
          ▼                                    ▼
  V_bus = 2V_o N/D              V_bus = 2N·(V_o + √(V_o² + 16P_o L_o f_sw/D²))/2
          ▼                                    ▼
  I_Cb,out−avg = I_o D/2N        I_Cb,out−avg = D²/(4NL_o f_sw)·(V_bus/2N − V_o)
          └──────────────────┬────────────────┘
                             ▼
   I_Cb,in−avg = 2f_in Σ ∫ [(V_in,k − V_bus)/L_in (t−t*) + I*_in,k] dt
                             ▼
                         ◇        ◇          Yes
                      ◇ I_Cb,out−avg = I_Cb,in−avg ◇──────▶ ( D is Correct )
                         ◇        ◇
                             │ No
                             ▼
                    ┌──────────────────┐
                    │  Select Another D │
                    └──────────────────┘
```
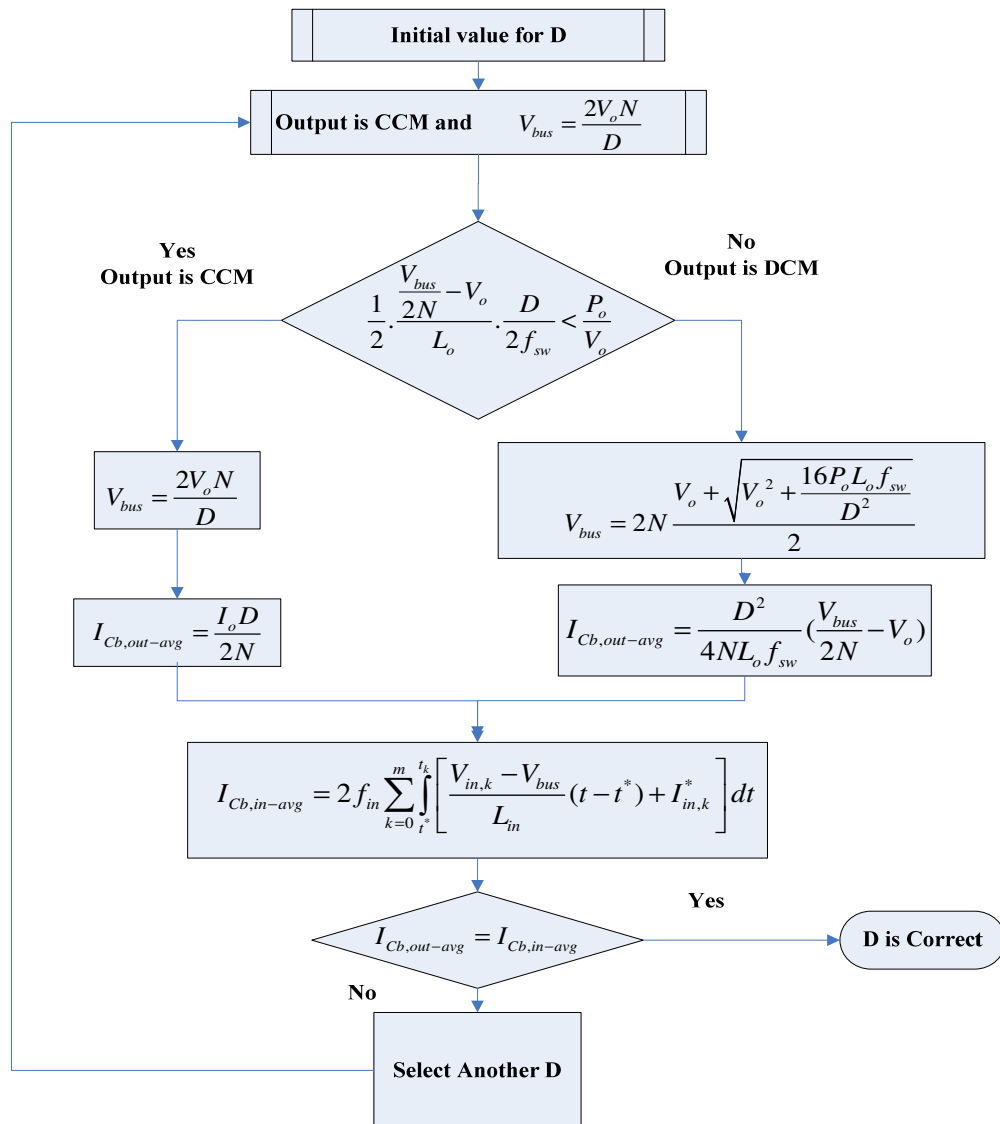

Fig.2.5. The procedure of steady state analysis for determining the dc bus voltage
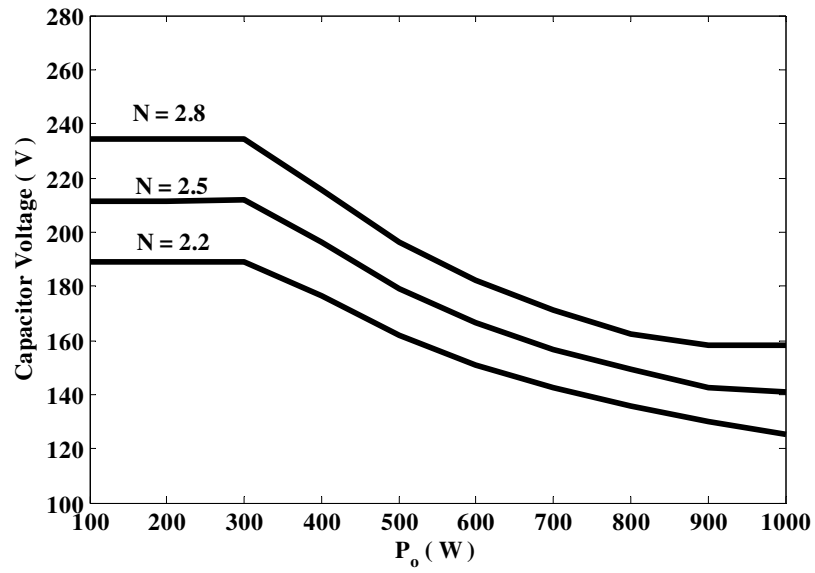
(a) Effect of transformer ratio value N on dc bus voltage ($L_{in}=35\mu H$, $L_o=15\mu H$)
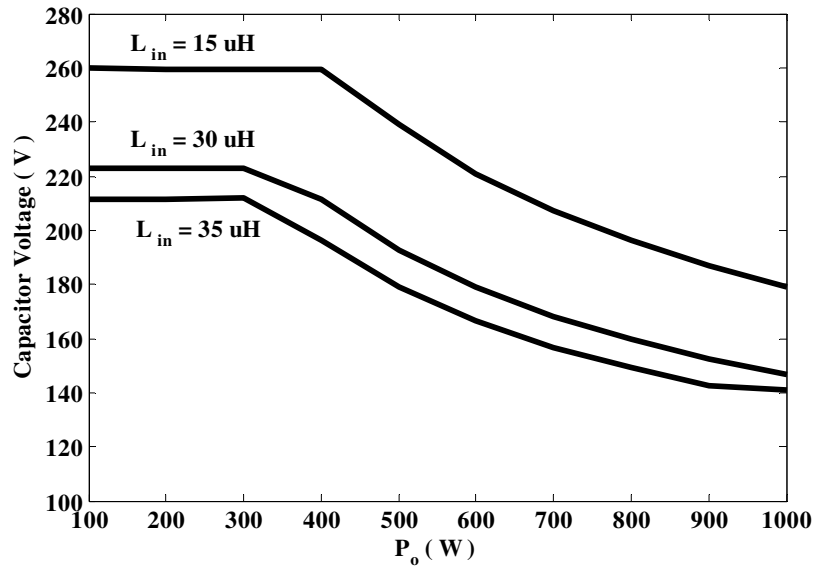
(b)Effect of input inductor value Lin on dc bus voltage (N=2.5, Lo=15μH)
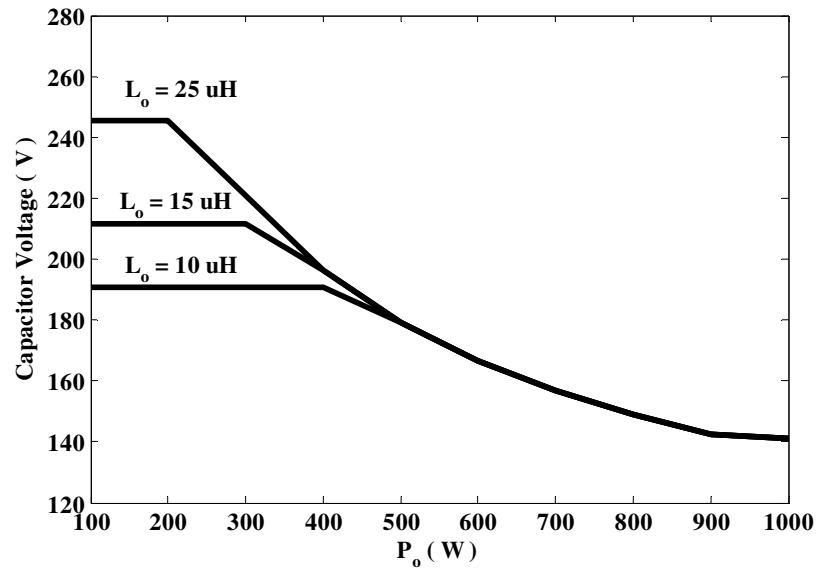
(c) Effect of output inductor value Lo on dc bus voltage (N=2.5, Lin=35µH)
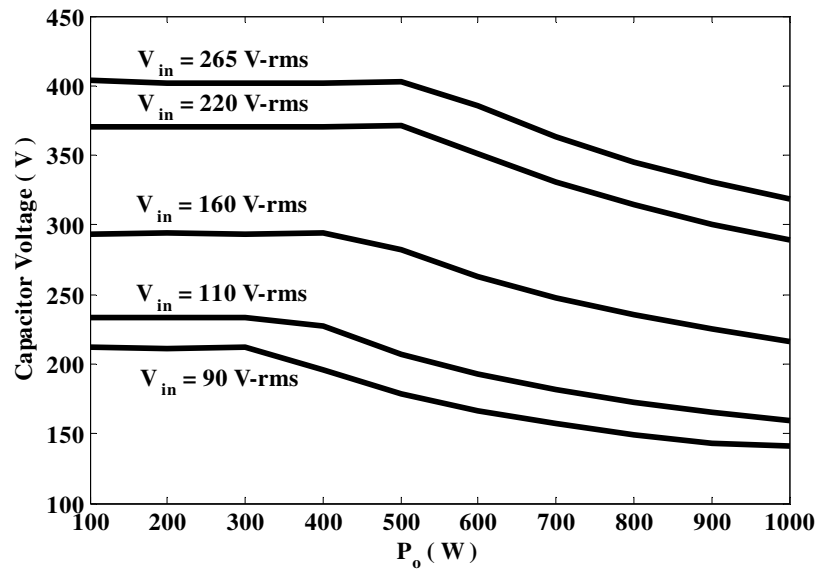
(d) Effect of input voltage V_{in} on dc bus voltage (N=2.5, L_{in}=35μH, L_o=15μH)

Fig.2.6. Steady-state characteristic curves (V_{in}=90V_{rms}, V_o=48V, f_{sw}=50kHz).

These characteristics are consistent with those of most single-stage AC-DC converters. A detailed explanation as to why the converter has these particular characteristics can be found in [31].

2.6. Balancing of DC Bus Capacitors

It should be noted that since the converter is a multilevel converter, that the dc bus voltage can be split equally among the capacitors so that the capacitors and the converter switches are not exposed to the full dc bus voltage, but are exposed to half of it. This allows for greater flexibility in the design of the converter as there is less need to constrain the dc bus voltage, as will be shown in the next section. It is the greater flexibility in the converter design that allows for improvements in the performance of a single-stage full-bridge converter.

Since the converter is a multilevel converter, it should be implemented with some sort of capacitor voltage balancing technique to ensure that the voltage across each bus capacitor is the same. Various such techniques have been proposed in the literature, including techniques that sense the capacitor voltages and adjust the duty cycle of the converter switches appropriately. For this work, an auxiliary circuit that is composed of a transformer with a turns ratio of $N_{aux1}/N_{aux2} = 1$ and two diodes D_{aux1} and D_{aux2} was used, as shown in Fig.2.7 [78]. This circuit is very simple, small, and handles only a small fraction of the overall power that is processed by the converter. It should be noted that any other voltage balancing technique could have been used.

The basic principle behind the auxiliary circuit is that if the voltage across one capacitor begins to be greater than the other by more than a diode drop, then one of the diodes begins to conduct as energy is transferred away from the capacitor with the higher voltage. Since the auxiliary circuit does not allow for large differences in bus capacitor voltage, the amount of energy that needs to be transferred away at any given time is small. When the auxiliary circuit is added to the main circuit, it is most likely to come into play during Modes 1 and 5 of operation as this is when the most current will flow

through one of the bus capacitors. The auxiliary circuit works as follows during these modes:
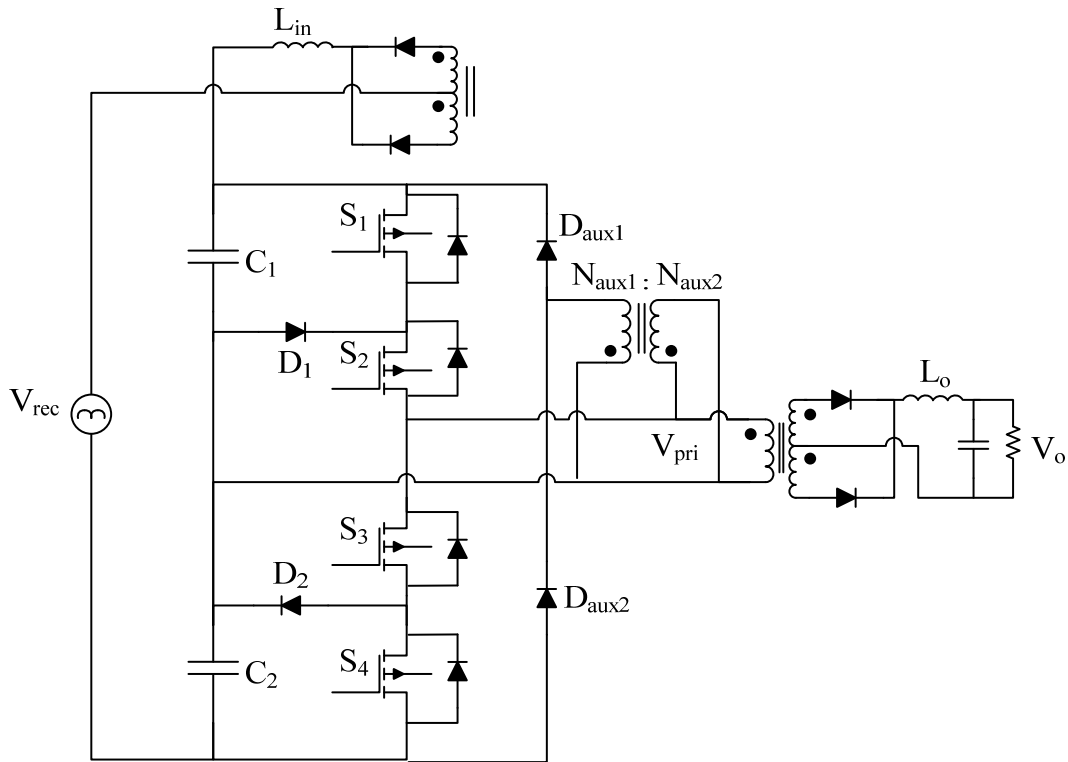
Fig.2.7. Proposed single-stage three-level converter with auxiliary circuit.

Mode 1 ($t_0 < t < t_1$)(Fig.2.8(a)): During this mode, switches S_1 and S_2 are ON and energy from the dc-link capacitor C_1 flows to the output load. Since the auxiliary winding generates a voltage that is equal to the total dc-link capacitor voltage (sum of C_1 and C_2), the voltage across the auxiliary inductor is the rectified supply voltage. This allows energy to flow from the ac mains into the auxiliary inductor during this mode, and the auxiliary inductor current increases.

At the beginning of this interval, if there exists any unbalance between the voltages of the two dc-bus capacitors, such that $V_{C1} > V_{C2}$, the auxiliary circuit starts conducting through diode D_{aux2} to balance the voltage difference across C_1 and C_2.
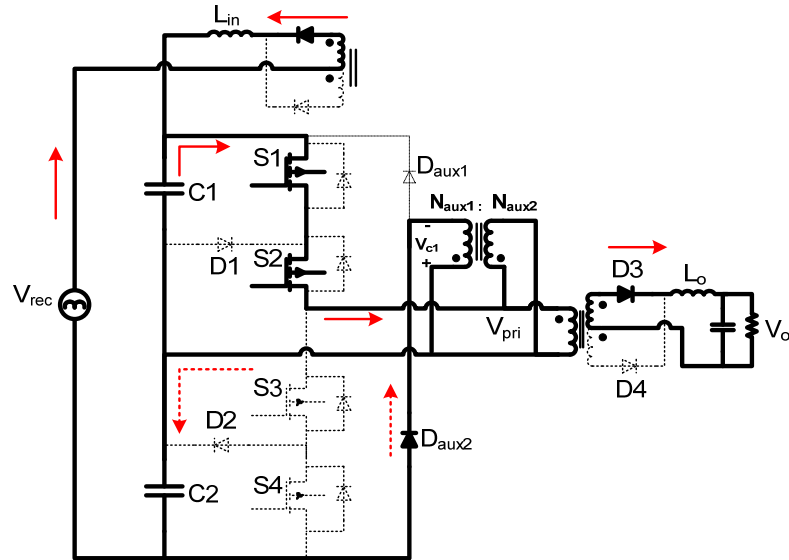
(a) Mode 1 with auxiliary circuit.
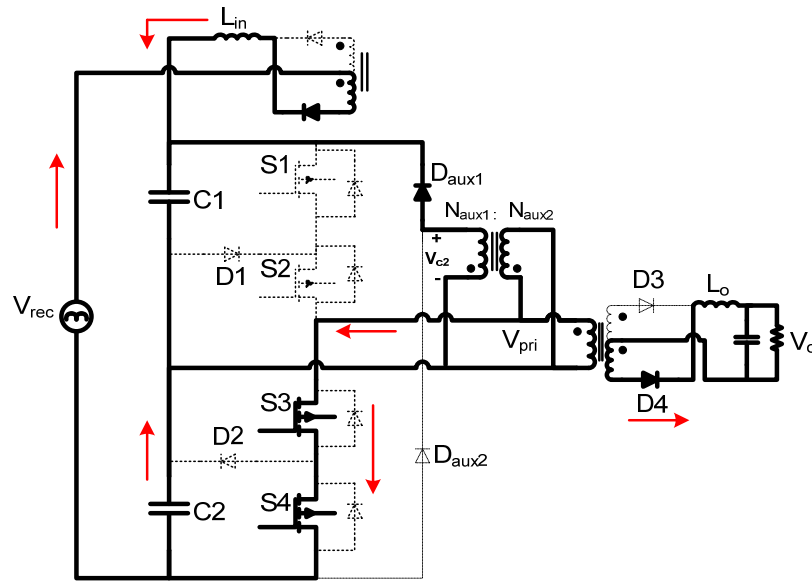
(b) Mode 5 with auxiliary circuit.

Fig.2.8. Modes of operation with auxiliary circuit.

Mode 5($t_4 < t < t_5$):(Fig.2.8(b)): This mode is the same as Mode 1 except that S_3 and S_4 are ON and energy flows from capacitor C_2 into the load. Similarly, in Mode 5, when $V_{C2} > V_{C1}$, the auxiliary circuit starts conducting through diode D_{aux1} to balance the voltage difference across the capacitors.

2.7.   Converter Design

A procedure for the design of the converter is presented in this section and is demonstrated with an example. The following criteria should be considered when trying to design the converter:

1) The energy-storage capacitor voltage V_{bus} should not be excessive. The value of V_{bus} should be kept below 800 V (400 V for each capacitor) if possible so that the use of bulkier, more expensive capacitors can be avoided.

2) Excessive peak output and input currents should be avoided if possible.

3) The input line current must satisfy the necessary regulatory agency requirements of harmonic content such as IEC1000-3-2.

A design procedure for the selection of converter components based on the characteristic curves presented in the previous sections of this paper is given along with an example to illustrate how the converter can be designed. The converter is to be designed with the following parameters for the example:

Input voltage: V_{in} = 90−265 V_{rms}

Output voltage: V_o = 48 V

Maximum output power: P_o = 1000 W

Switching frequency: $f_{sw} = {}^1\!/T_{sw}$ = 50 kHz

Maximum capacitor voltage: 400 V for each capacitor

Input current harmonics: IEC1000-3-2 for Class D electrical equipment.

It should be noted that the design procedure is iterative and only the last iteration is shown here.

Step 1: Determine Value for Turns Ratio of Main Transformer N:

N is an important parameter as it affects the amount of reflected load current that is available at the transformer primary to discharge the bus capacitors. Fig.2.6 (a) is an example of how the value of N affects the primary-side dc bus voltage. If N is very high, then there is little reflected load current available to discharge the bus capacitors, which can result in an extremely high dc bus voltage. If N is low, then the primary current may be very high as there will be a high amount of current circulating in the transformer primary, which will create significant conduction losses. A trade-off between high values of N and low values of N, therefore, must be considered when selecting a value of N.

Selecting a value of N, however, cannot be done with a simple equation and must be done using some other method. One way of doing so is to use the computer program described in the previous section of this paper to examine a wide range of potentially valid combinations of L_o and L_{in} – combinations that allow the converter to work for the two most extreme line and load conditions: high line, light load and low line, full load. For this particular design example, numerous graphs of characteristic curves for different values of N were generated and based on these graphs, a value of N = 2.5 is selected as an appropriate value.

As a check to see if this value makes sense, equation (2.10) - which shows the relation between V_{bus} , D, V_o and N – can be used. For this check, the operation of the converter at minimum input line when it operates with minimum primary-side dc bus voltage $V_{bus,min}$ and maximum duty cycle D_{max} should be considered. If the converter can produce the required output voltage and can operate with discontinuous input and continuous output currents in this case, then it can do so for all cases. Substituting $V_{bus,min}$ and maximum duty cycle D_{max} into equation (2.10) gives

$$V_{bus,min} = \frac{2V_o}{D_{max}} \cdot N \qquad (2.17)$$

Substituting V_o = 48, N = 2.5, and D_{max} = 0.8 (0.8 has been selected as a conservative D_{max} to provide some margin) gives

$$V_{bus,min} = \frac{2(48)}{0.8} \cdot (2.5) = 300\ V \tag{2.18}$$

A bus voltage of $V_{bus,min}$ = 300 V or V_{bus}/2 = 150 V is acceptable. If a very low value of $V_{bus,min}$ = 100 V or a value of $D_{max} > 1$ would have been found based on equation (2.17), then the value of N under consideration would have been unacceptable and another value would have to be considered. It should be noted that the dc bus voltage has not been determined yet. All that has been determined thus far is a value of N that can operate with an acceptable duty cycle for an acceptable minimum dc bus voltage.

Step 2: Determine Value for Inductor L_{in}:

The value for L_{in} should be low enough to ensure that the input current is fully discontinuous under all operating conditions, but not so low as to result in excessively high peak currents. This can be done using the computer program with the following equations, which are based on the descriptions given in Section III .

For the case where L_{in} is such that the input current remains discontinuous for all operating conditions, the average input power can be expressed as

$$P_{in} = \frac{1}{T_{su}} \int_0^{T_{su}} |v_{s,k}| \cdot i_{s,k} d_{w_k}\ t = \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} |v_{s,k}| \cdot i_{s,k} \tag{2.19}$$

where f_{su} is the input ac frequency and $f_{sn} = 2f_{sw}/f_{su}$ and

$$i_{s,k} = \frac{(D + \Delta_s)}{2} \cdot i_{L_{in,max}} = \frac{1}{4} \cdot \frac{D^2}{L_{in} \cdot f_{sw}} \cdot \frac{|v_{s,k}|}{1 - \frac{|v_{s,k}|}{V_{bus}}} \tag{2.20}$$

By substituting the value of $i_{s,k}$ in (20), P_{in} can be expressed as

$$P_{in} = \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} |v_{s,k}| \cdot i_{s,k} = \frac{D^2}{8.L_{in}.f_{sw}} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \frac{|v_{s,k}|^2}{1 - \frac{|v_{s,k}|}{V_{bus}}} \tag{2.21}$$

By assuming that $P_{in} = P_o$, the following equation can be derived:

$$L_{in} = \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} |v_{s,k}| \cdot i_{s,k} = \frac{D^2}{8.P_o.f_{sw}} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \frac{|v_{s,k}|^2}{1 - \frac{|v_{s,k}|}{V_{bus}}} \tag{2.22}$$

The worst case to be considered is the case when the converter operates with minimum input voltage and maximum load since if the input current is discontinuous under these conditions, it will be discontinuous for all other operating conditions and thus an excellent power factor will be achieved. $V_{in} = 90$ V_{rms} and $V_{bus} = 300$ V as calculated in Step 2 are used to determine L_{in} at the boundary condition for the input section with D = $D_{max} = 0.8$ and $P_{in} = P_o = 1000$ W. As a result, a value of $L_{in} = 38.5$ μH can be found. For this design, $L_{in} = 35$ μH is used.

Step 3: Determine Value for Output Inductor L_o:

Ideally, the output inductor L_o should be designed so that the output current is made to be continuous under most operating conditions. The reality, however, is doing so may result in an excessive dc bus voltage. As a compromise, the value of L_o should be such that the output inductor current is continuous when the converter is operating with heavy loads and discontinuous when the converter is operating with light loads.

Fig.2.6 (c) shows a graph of curves of bus capacitor voltage ($V_{bus}/2$) vs. load for various values of L_o, with N = 2.5 and $L_{in} = 35$ μH, which are the values of N and L_{in} that were selected in the previous steps. This graph shows the effect that L_o has on the bus capacitor voltage. When the converter is operating with heavy load, it does not matter what the value of L_o is if the output inductor current is continuous. It is when the load is reduced that the capacitor voltage becomes different with different L_o as the current in L_o

start becoming discontinuous. The flat portion of each curve in Fig.2.6 (c) represents the load range where the current through Lo is discontinuous while the curved or "non-flat" region is the region where the current through L_o is continuous. It can be seen from Fig.2.6 (c) that the boundary point between continuous current mode (CCM) and discontinuous current mode (DCM) output inductor current occurs at a lighter load as L_o is increased.

The value of L_o should be the largest value that allows the converter to operate with non-excessive capacitor voltages, non-excessive being defined as less than 450 V, which is a standard definition for two-level converters. The worst case for this is when the input is at maximum line and thus a graph of capacitor voltage vs. load for the values of N and L_{in} selected in the previous steps, N = 2.5 and L_{in} = 35 µH and the value of L_o under consideration is needed. Such a graph for L_o = 15 µH is shown in Fig.2.6 (d).

It can be seen from this graph that the maximum bus capacitor voltage is approximately 400 V. Since a higher value of L_o would probably result in the bus capacitor voltage exceeding 450 V or being close to 450 V without margin, a value of L_o = 15 µH is therefore chosen for the output inductor.

As a final check, the value of $V_{bus,min}$ should be looked at given the importance of this parameter as explained in Steps 1 and 2 of this procedure. It can be seen from Fig.2.6 (d) that $V_{bus,min}/2$ occurs when the line voltage is 90 Vrms (low line) and the load is at its maximum and that this value is approximately 150 V or $V_{bus,min}$ = 300 V. The chosen combination of N, L_{in}, L_o therefore is acceptable and the design procedure can be ended.

It should be noted that a value of L_o = 15 µH is considerably higher than what is typically found in most other single-stage full-bridge converters, which must operate with very low output inductor values to prevent the dc bus voltage from becoming excessive.

2.8.　　　Experimental Results

An experimental prototype of the proposed converter was built to confirm its feasibility. The prototype was designed according to the following specifications:

Input voltage V_{in} = 90-265 V_{rms}

Output voltage V_o = 48 V

Output power P_o = 1000 W

Switching frequency f_{sw} = 50 kHz.

The main switches were FDL100N50F, and the diodes were UF1006DICT. The input inductance is L_{in} = 35 µH, L_o = 15 µH and dc-Bus capacitors, C_1, C_2 = 2200 µF. The auxiliary transformer ratio was 1:2 and the main transformer ratio was 2.5:1. Typical converter waveforms are shown in Fig.2.9, 2.10 and 2.11.

Fig.2.9 (a) and (b) show the gating signals of the four switches; the converter works like a standard dc-dc multilevel full-bridge converter. Fig.2.10 (a) shows typical voltage waveforms of the top switches. The multilevel converter provides the capability of operating at reduced voltage stresses across the switches, as the switch voltage is limited to half the dc-bus voltage. Fig.2.10 (b) shows the voltage across the primary side of the main transformer, which is the same as that of a full-bridge converter. Fig.2.11 (a) shows the input voltage and input current before filtering; it can be seen that the input current has no deadbands. Fig.2.11 (b) shows the output inductor current.
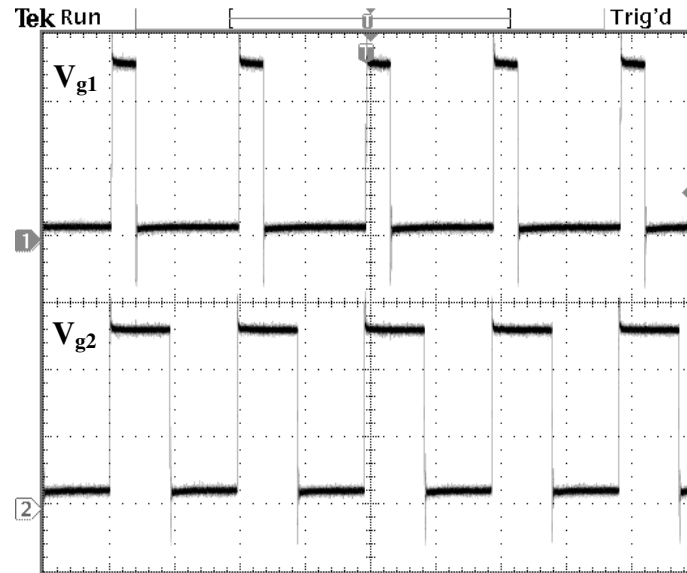
(a) Switch gating pulses V_{gs1}, V_{gs2} (V: 5 V/div., t: 10 μs/div.)
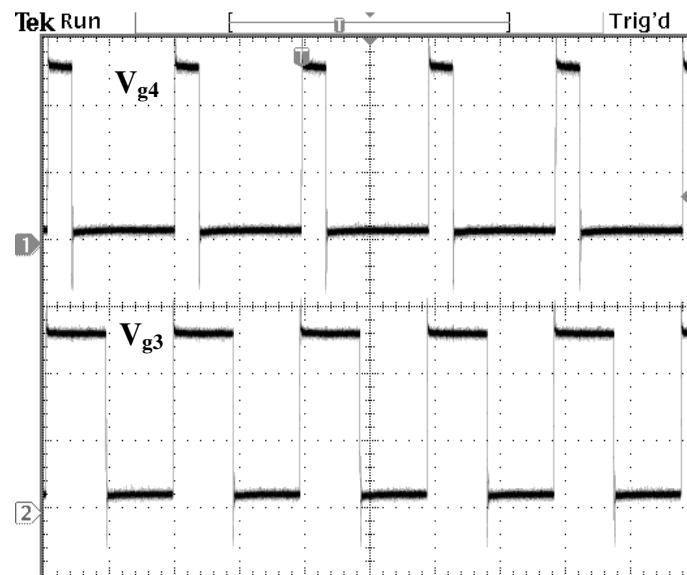
(b) Switch gating pulses Vgs4,Vgs3 (V: 5 V/div., t: 10 μs/div.)

Fig.2.9. Experimental results. (a)Switch gating pulses V_{gs1}, V_{gs2} , (b)Switch gating pulses V_{gs4}, V_{gs3}
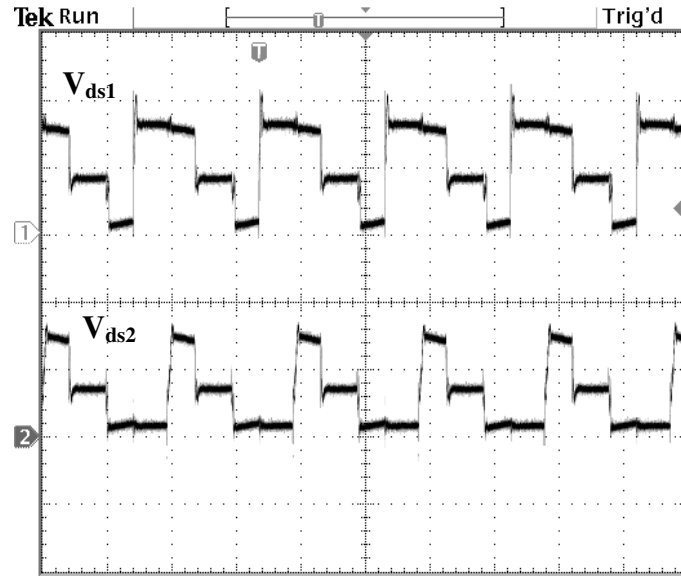
(a)   Top switch voltages V_{ds1} and V_{ds2} (V: 100V/div., t:10 µs/div.)
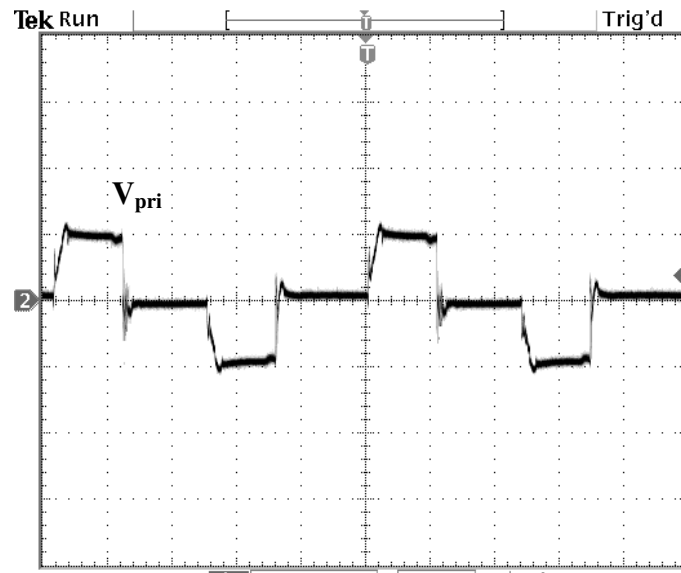
(b)   Primary voltage of the main transformer (V:150V/div.,t: 4 µs/div.)

Fig.2.10. Experimental results. (a) Top switch voltages Vds1 and Vds2, (b) Primary voltage of the main transformer.
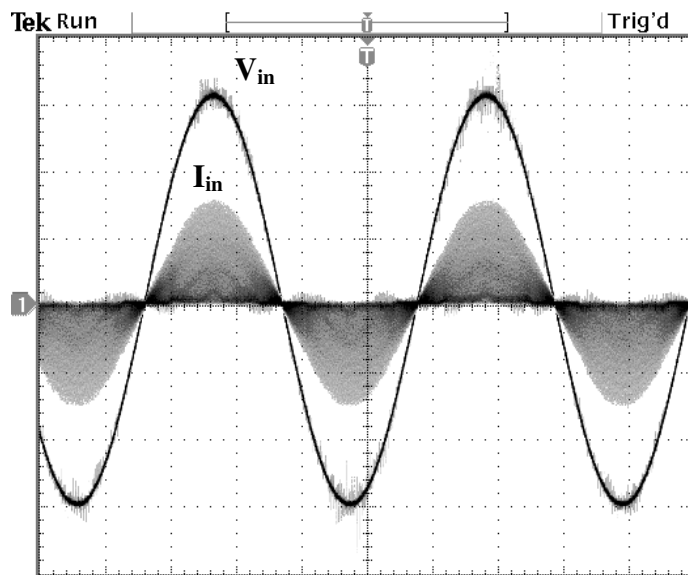
(a) Input current and voltage (V: 50 V/div, I: 25 A/div)
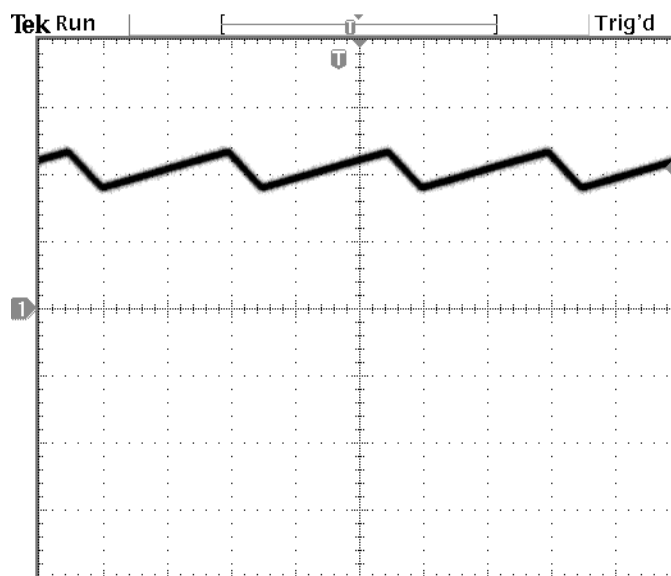
(b) Output inductor current (I:10A/div., t: 4 μs/div.)

Fig.2.11. Experimental results. (a) Input current and voltage, (b) Output inductor current.

Fig.2.12 shows the experimental efficiency at different value of output power and Fig.2.13 shows the experimental efficiency at different value of input voltages. Fig.2.14 shows the dc bus voltage at different value of output power. Input power factor at different values of output power is shown in Fig.2.15. Fig.2.16 and 17 show input current harmonic at V_{in} = 230 Vrms and V_{in} = 100 Vrms respectively and can meet the IEC1000-3-2 Class A standard for electrical equipment.

As can be seen from the experimental results and characteristic graphs, the proposed converter is a higher power voltage-fed SSPFC that can operate with universal input voltage range (90– 265 Vrms), wide output load variation (from 10% of full load to a full load that is greater than 500 W), PWM control, excellent power factor, a continuous output inductor current, without its components being exposed to excessive peak voltage stresses.

The superior performance of the proposed converter can be clearly seen when compared to the converters that were presented in [79], which reviewed and compared the performance of a number of SSPFC converters operating at 30 kHz. When comparing the proposed converter with the converters reviewed in that paper, it can be seen that the proposed converter operates with similar converter efficiency even though its switching frequency was almost two times higher, and with higher dc bus capacitor voltages, which increases the peak voltage stresses of the converter switches.
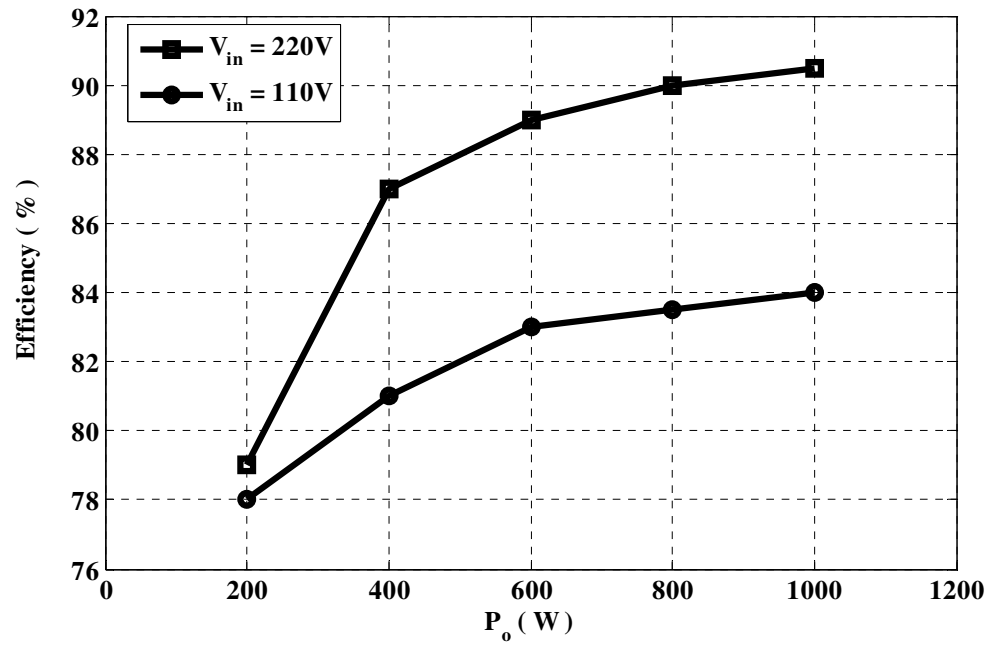
Fig.2.12. Experimental efficiency at different value of output power.
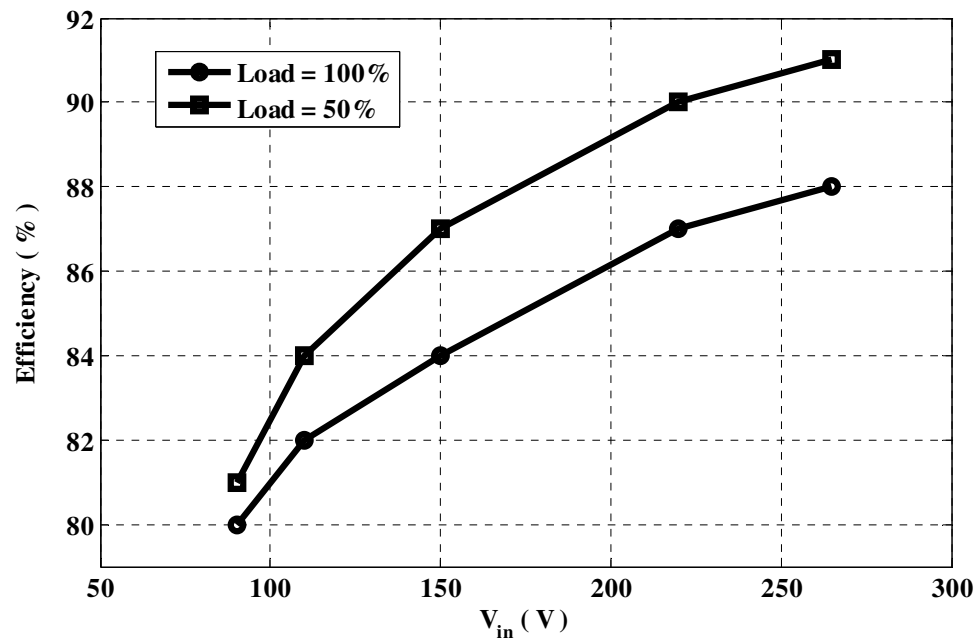
Fig.2.13. Experimental efficiency at different value of input voltage.
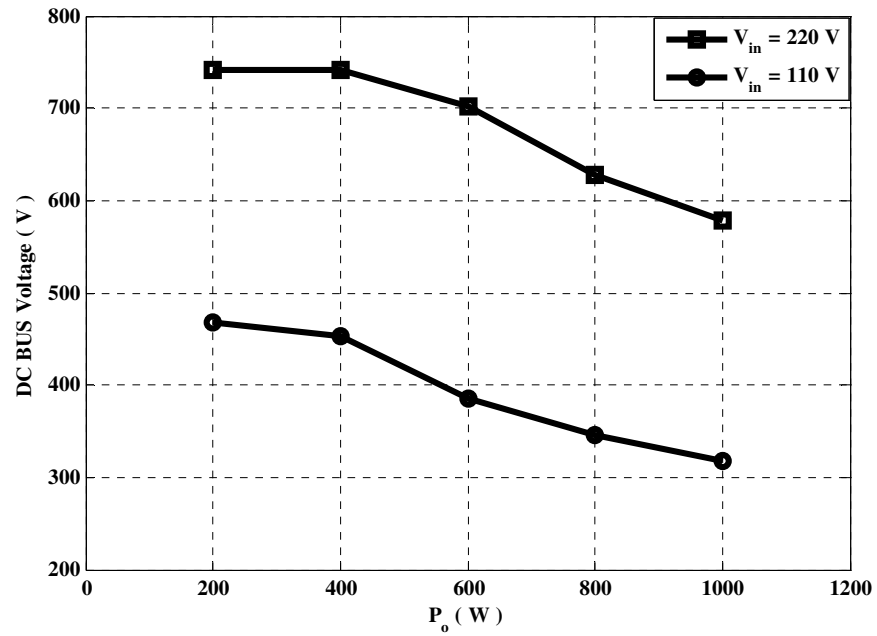
Fig.2.14. Experimental dc bus voltage at different value of output power.
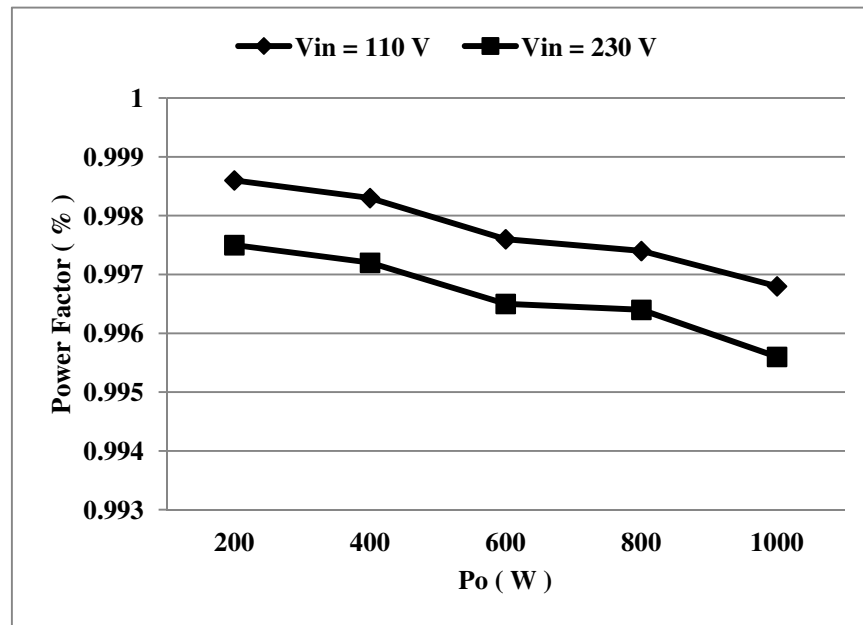
Fig.2.15. Input power factor at different values of output power.
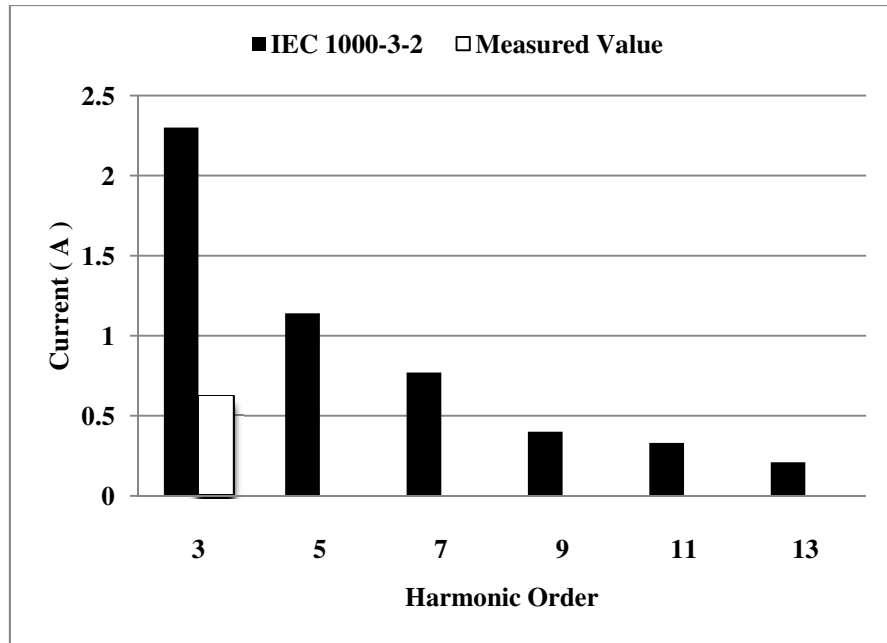
Fig.2.16. Input current harmonic at $V_{in} = 230$ V_{rms} , P_o=1000W compared to IEC1000-3-2 Class A.
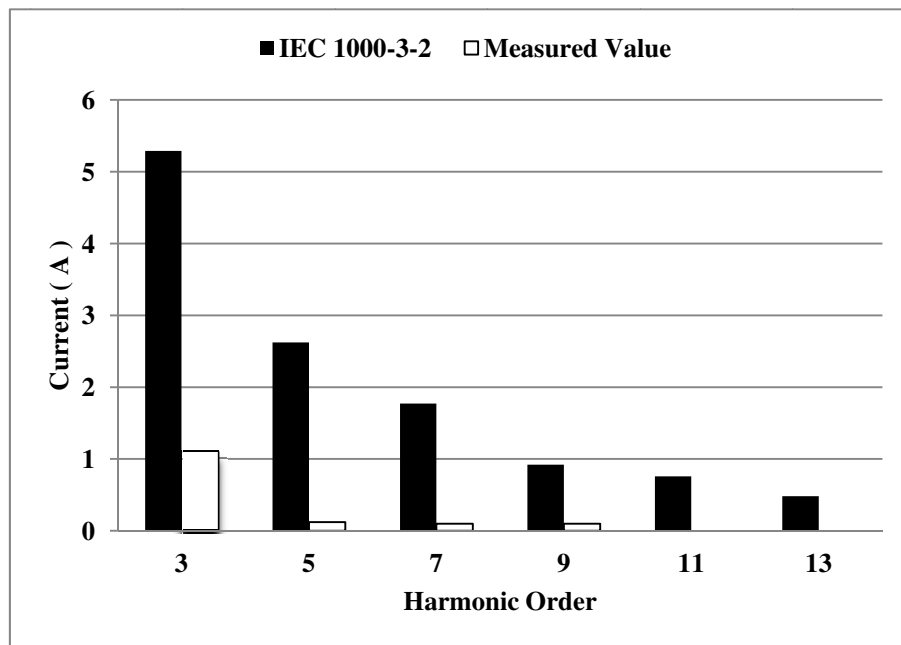
Fig.2.17. Input current harmonic at $V_{in} = 100$ V_{rms} , P_o=1000W compared to IEC1000-3-2 Class A.

2.9.   Conclusion

In this chapter, a new three-level, single-stage single-phase power-factor-corrected (SSPFC) AC-DC PWM converter that operates with a single controller was presented. The proposed converter can operate with universal input voltage (90– 265 Vrms) and with less input current distortion, wider load operating range, and less output inductor current ripple than previously proposed SSPFC converters. The advantageous features of the proposed converter are due to the fact that it is a three-level converter that allows the uncontrolled primary-side dc bus voltage to be higher than what can be allowed for two-level converters so that it does not have the design restrictions that these converters have.

The operation of the new converter was explained in detail and analyzed, its steady-state characteristics were determined by analysis, and a procedure for the design of certain key converter components was developed and demonstrated with an example. Experimental results obtained from a prototype confirmed the feasibility of the new converter and its ability to meet IEC 1000-3-2 standards for electrical equipment.

Chapter 3

3. Modified Single-Phase Single-Stage Three-Level Power Factor Correction AC-DC Converters

3.1. Introduction

Although the converter proposed in Chapter 2 is an improvement over previously proposed SSPFC converters, its performance can be further improved if some modifications are made to its topology. In this chapter, two such modifications are proposed – one to reduce the output inductor current ripple, the other to increase converter efficiency. The operation of each modified converter and the reason for the proposed modification is explained in detail, and experimental results that confirm the effectiveness of the proposed modification are presented.

3.2. A Single-Phase Single-Stage Three-Level Power Factor Correction AC-DC Converter with Auxiliary Circuit

The converter proposed in Chapter 2 can be designed to operate with a continuous output inductor current for load more than 50%, without its components being exposed to excessive peak voltage stresses. Doing so reduces the need for components that can handle high peak currents and the need for additional output filtering to remove the ripple. Although the output characteristics are improved and the output inductor current has less ripple than what is typically found in higher power two-level SSPFCs, this ripple is still considerable and some measure should be taken to reduce it even feature.

In order to reduce ripple at the output current in heavy loads, the converter's output section can be implemented with two output inductors:

- There should be one larger inductor for heavy load conditions to reduce the output inductor current ripple and

- There should be another separate smaller inductor for light load conditions to prevent the dc bus voltage from becoming excessive under these conditions.

This is what is trying to be achieved in the modified converter with a new auxiliary circuit to reduce the amount of output inductor current that can exist when the converter is operating under heavy load conditions. The new auxiliary circuit is simple and is active only when the converter is operating under light load conditions.

3.2.1. Effect of Output Inductor on DC Bus and Output Ripple

As mentioned, the dc bus voltage in SSPFC converters is uncontrolled, as they have only one controller that is used to regulate the output voltage. This voltage is, instead, dependent on the energy equilibrium that must exist at the dc bus capacitor—the amount of energy or charge that is fed into this capacitor must be equal to the amount of energy or charge that is removed from the capacitor during a half line cycle[26]. This energy is dependent on the current that is flowing in and out of the bus capacitor, which is, in turn, dependent on the input and output inductor currents.

The output inductor current of a SSPFC full-bridge converter can be in the continuous conduction mode (CCM), or the discontinuous conduction mode (DCM), depending on the output inductor value and the load. Reference [31] shows that varying the output inductor (but keeping all the other parameters fixed) does not seem to have an effect on the dc bus voltage for higher output loads when the output inductor current is operating in CCM, but does so at lower output loads when the output is in DCM. The same paper also shows that the dc bus voltage rises as load is reduced when the output is in CCM, but remains fixed when the output inductor current is in DCM. Ideally, the output inductor of a SSPFC converter should be large enough for the output current to be in CCM for heavy load and small enough to be in DCM for light loads, but these two criteria cannot be met by a single output inductor. As a result, SSPFC converters are

designed so that their output inductor is small, to ensure that the output current is in DCM for light loads, which prevents the intermediate dc bus voltage from rising to excessive values.

The main drawback to this approach is that the output inductor current has a large ripple when the converter is operating with heavy loads. Although the converter proposed in Chapter 2 can be designed so that its output current has less ripple than other SSPFC converters, the basic issue of conflicting output inductor criteria remains and an alternative approach should be considered.

3.2.2. Operation of The Auxiliary Circuit in SSPFC Three-Level Converter

In order to address the issue of conflicting output inductor criteria, the auxiliary circuit shown in Fig.3.1 is proposed.
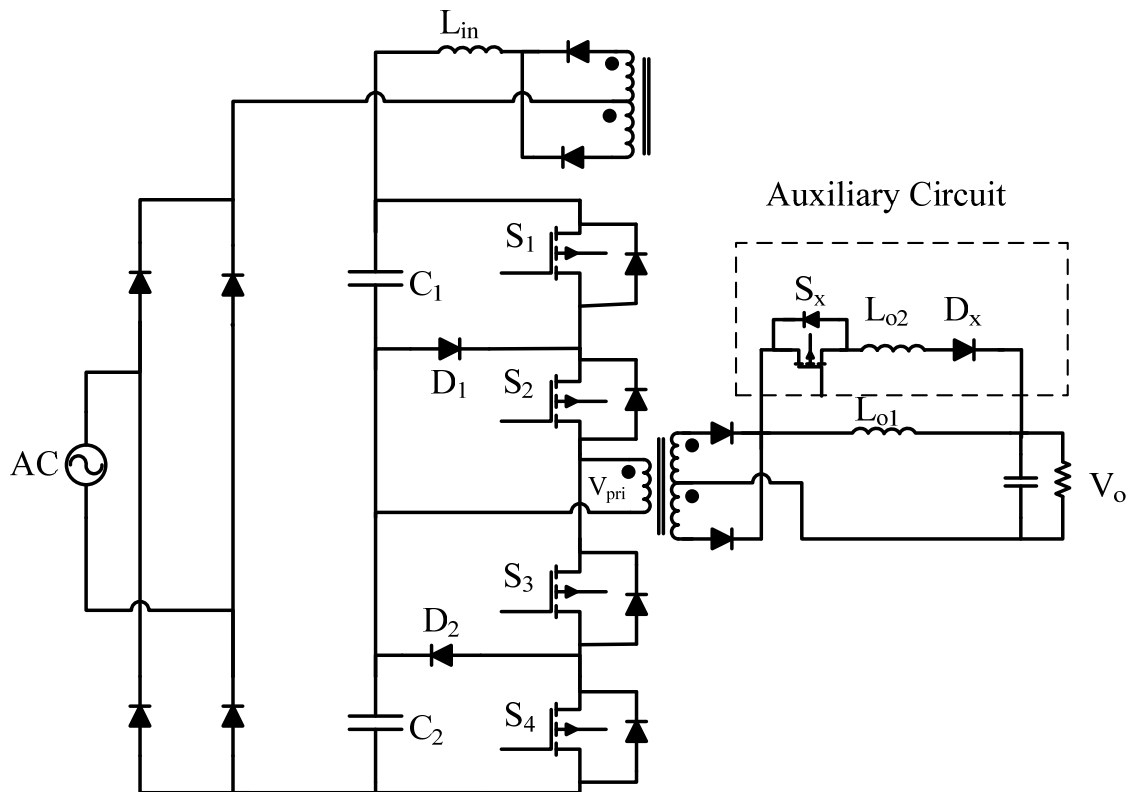
Fig.3.1. Proposed single-stage three-level AC-DC converter.

This auxiliary circuit is attached to the output section of the SSPFC converter, and consists of a MOSFET, a small inductor L_{o2} (much smaller than main inductor L_{o1}) and a blocking diode that blocks the body-diode of the MOSFET. The auxiliary circuit is inactive unless the dc bus voltage tries to exceed a certain preset level. It is then and only then that the auxiliary switch MOSFET is turned ON so that the small auxiliary circuit inductor is placed parallel to L_{o1}.

What this does is that it reduces the net inductance at the output so that most of the output current flows through L_{o2}; this makes the output inductor current discontinuous, which ensures that the dc bus voltage does not rise to an excessive level. If the load is increased at some later time, then (a) there is no need for L_{o2} as the dc bus voltage is unlikely to become excessive and (b) there is need for L_{o1} to be in the converter to avoid high output current ripple. In this case, the auxiliary switch is OFF and all the output current flows through L_{o1}. It should be noted that the S_x switch is a low voltage and a low frequency switch as it is just a "setting" switch (light-load setting or heavy load setting).

The effect of having different output inductor values on the dc bus voltage can be seen from Fig.3.2, which is a graph of dc bus capacitor voltage (half of the dc bus voltage for the converter in Fig.3.1) vs. output inductor value for a converter operating with input voltage V_{in} =265 Vrms, output voltage V_o = 48 V, switching frequency f_{sw} = 50 kHz, L_{in} = 35 µH, a 1:2 auxiliary transformer ratio and a 2.5:1 main transformer ratio is 2.5:1.

It can be seen that (a) it does not matter what the output inductor is if the output current is in CCM; (b) the larger the output inductor is, the larger the dc bus voltage is for light load conditions when the output inductor current is in DCM. Although a 50 µH inductor may be suitable to reduce output current ripple when the converter is operating with heavy loads, it is not suitable when the converter is operating with lighter loads.

If the converter shown in Fig.3.1 is implemented with L_{o1} = 50 µH and L_{o2} = 15 µH and it is desired that the voltage across a dc bus capacitor does not exceed 420 V, then, according to Fig.3.2, auxiliary switch S_x should be turned ON when the load decreases to about 60% of the full-load. Doing so parallels the L_{o2}=15 µH with L_{o1} so that the

equivalent inductor at the output decreases to about 11.5 µH. It should be noted that the values of L_{o1} (= 50 µH) and L_{o1} in parallel with L_{o2} (= 11.5 µH) are considerably higher than the output inductor values that have been reported for other SSPFC full-bridge converters.

It should be noted that control of the auxiliary switch is very simple and based on the hysteresis control to prevent it from turning on and off frequently. This control circuit can be implemented by a Flip-Flop logic circuit.
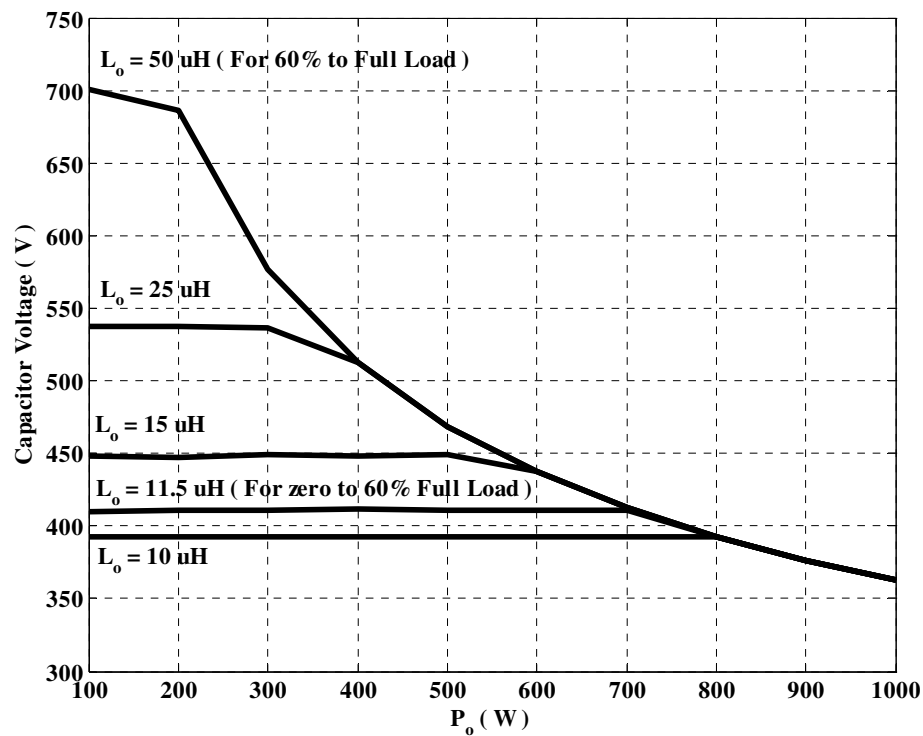
Fig.3.2. Effect of output inductor value L_o on DC bus capacitor voltage.

3.2.3. Experimental Results

A prototype of the proposed converter was built to confirm its feasibility. The prototype was designed according to the following specifications: Input voltage V_{in} = 90-265 Vrms, output voltage V_o = 48 V, maximum output power P_o = 1000 W and the switching frequency f_{sw} = 50 kHz. The main switches were FDL100N50F, and the diodes were UF1006DICT. The components were L_{in} = 35 μH, L_{o1} = 50 μH, L_{o2} = 15 μH and C_1, C_2 = 2200 μF. The auxiliary transformer ratio was 1:2 and the main transformer ratio was 2.5:1. Typical waveforms are shown in Fig.3.3 and 3.4.

Fig.3.3 (a) shows voltage waveforms of the top switches; they show that there is reduced voltage stress across the switches as the voltage is limited to half the dc-bus voltage. Fig.3.3 (b) shows the voltage across the primary side of the main transformer, which is looks like that of a standard full-bridge converter. Fig.3.3 (c) shows the input voltage and input current before filtering; it can be seen that the input current has no deadbands. Figs.3.4 (a) and 3.4 (b) shows the current ripple for heavy load when auxiliary switch is S_x is OFF and light load when S_x is ON. It can be seen that the converter can operate with low current ripple under heavy load conditions.

It should be noted that the operation of the auxiliary circuit under lighter load conditions reduces the efficiency of the converter by 1%-1.5% compared to the converter proposed in Chapter 2 where the converter was implemented with almost the same output inductor, but without the auxiliary circuit. The auxiliary circuit, however, does allow the converter to operate with significantly less output inductor current ripple than is possible without the auxiliary circuit and with improved heavy-load performance, when it is considered that the auxiliary circuit in not active when the converter is operating under heavy load conditions. There is, therefore, a trade-off between light-load and heavy-load performance that should be taken into account when considering implementing the proposed auxiliary circuit to a single-stage converter.

It should be noted that the proposed auxiliary circuit can be used in any SSPFC converter, two-level or three-level.
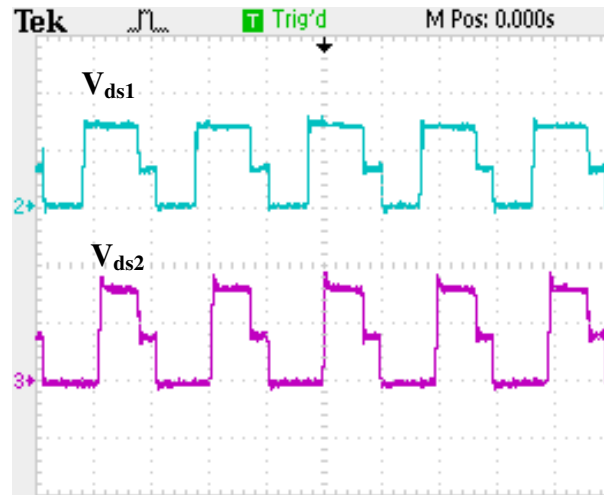
(a) Top switch voltages V_{ds1} and V_{ds2} (V: 100V/div., t: 10 μs/div.)
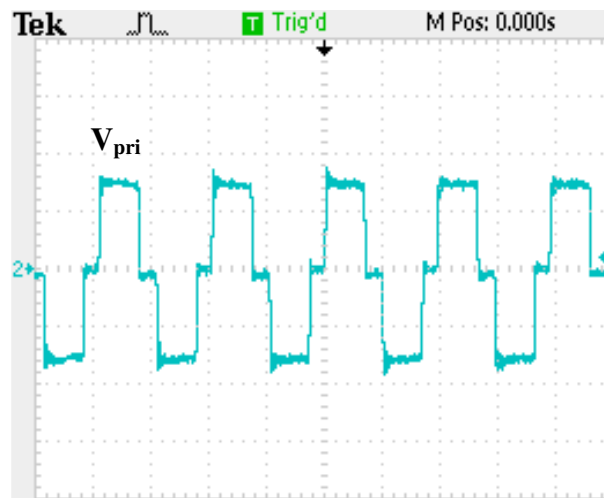
(b) Primary voltage of the main transformer (V: 150V/div., t: 4 μs/div.)
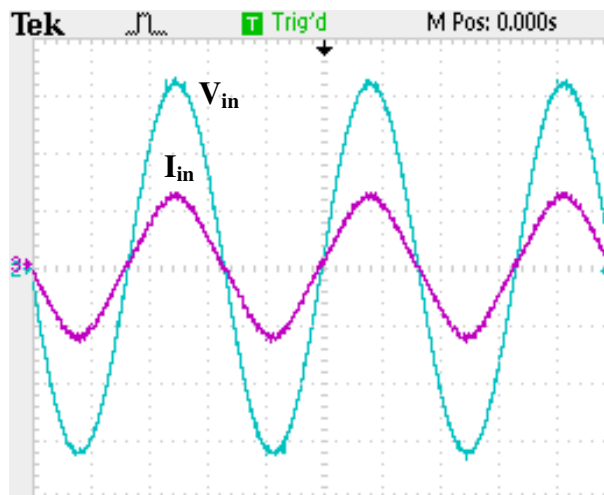
(c) Input current and voltage (V: 50 V/div, I: 10 A/div)

Fig.3.3. Typical experimental waveforms.
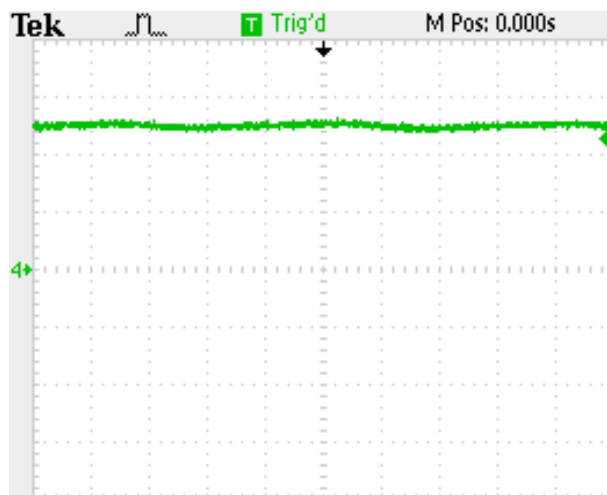
(a) Output inductor current with L_o= 50µH (I: 8A/div., t: 5 µs/div.)
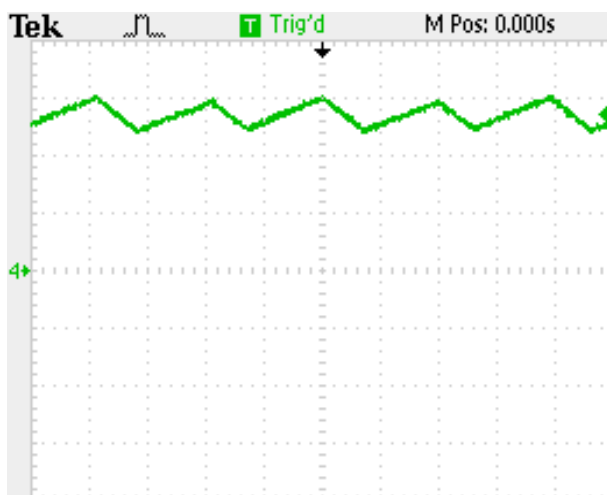
(b) Output inductor current with Lo= 11.5µH (I: 8A/div., t: 5 µs/div.)

Fig.3.4. Typical experimental waveforms

3.3. Single-Phase Single-Stage Three-Level Power Factor Correction AC-DC Converter with Phase-Shift Modulation (PSM)

A new three-level AC-DC single-stage converter that can operate with standard phase-shift PWM is proposed in this section. The operation of the converter is explained and its feasibility is confirmed with experimental results obtained from a prototype converter. Finally, the efficiency of the new converter is compared to a previously proposed converter of the same type and it is shown that the new converter has better efficiency, especially for light-load operation.

3.3.1. Phase-Shift Technique for Three-Level Single-Stage Converters

The proposed converter, shown in Fig.3.5, integrates an AC-DC boost PFC into a three-level DC-DC converter. It is almost the same as the converter proposed in Chapter 2 with a flying capacitor between two clamping diodes.

Typical converter waveforms are shown in Fig.3.6, and equivalent circuit diagrams that show the converter's modes of operation with PSM are shown in Fig. 3.7. The diode rectifier bridge output is replaced by a rectified sinusoidal source and thick lines representing the paths of current conduction.

The converter has the following modes of operation:

**Mode 1 ($t_0 < t < t_1$)(Fig.3.7(a)):**

During this mode, switches S_1 and S_2 are ON and energy from dc bus capacitor C_1 is transferred to the output load. Since the auxiliary winding generates a voltage ($N_{aux} / N_1 = 2$) that is equal to the total dc-link capacitor voltage (sum of C_1 and C_2), the voltage across the input inductor is the rectified supply voltage and thus the input inductor current starts rising.
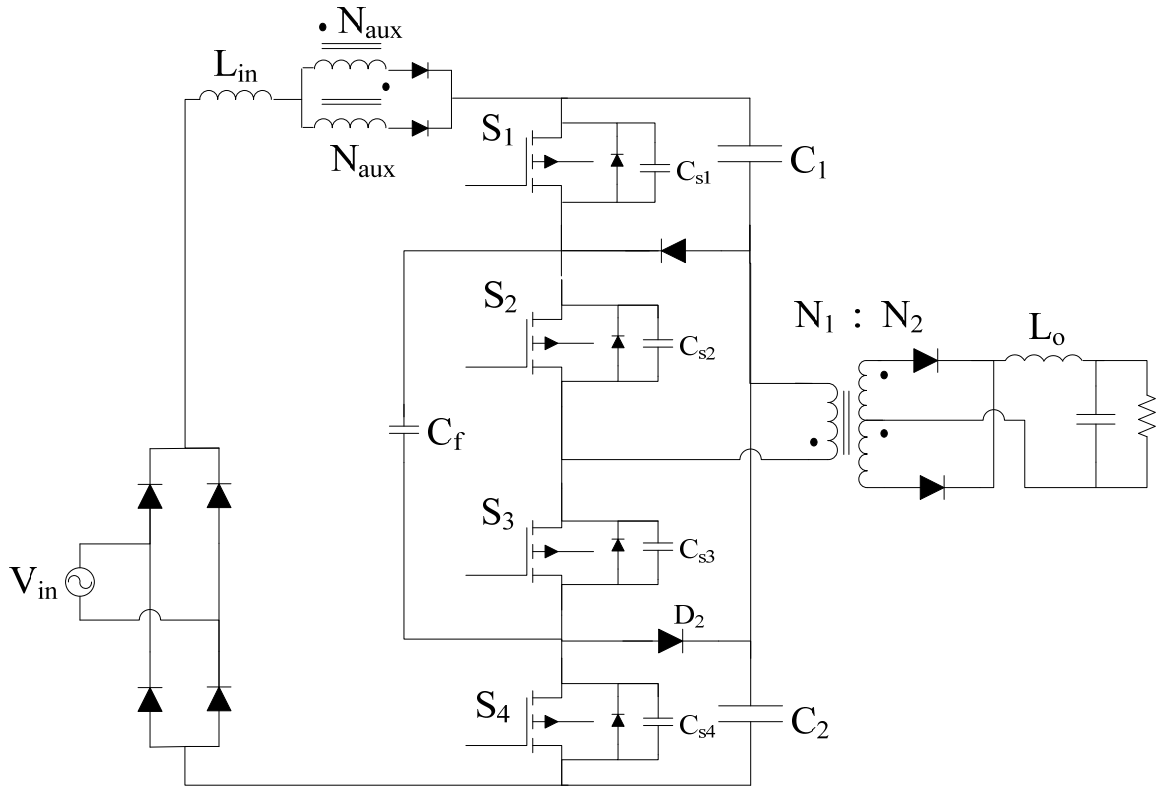
Fig.3.5. Proposed single-stage three-level AC-DC converter
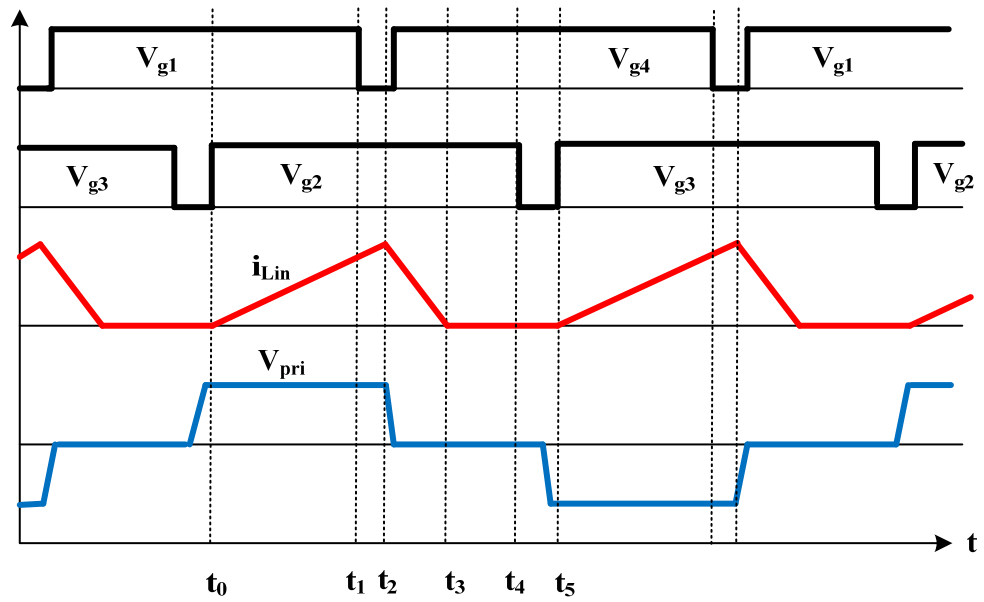
Fig.3.6. Typical waveforms for proposed converter

Mode 2 ($t_1 < t < t_2$)(Fig.3.7(b)):

In this mode, S_1 is OFF and S_2 remains ON. Capacitor C_{s1} charges and capacitor C_{s4} discharges through C_f until C_{s4}, the output capacitance of S_4, clamps to zero. The energy stored in the input inductor during the previous mode starts being transferred into the dc-link capacitors. This mode ends when S_4 turns on with ZVS.

Mode 3 ($t_2 < t < t_3$)(Fig.3.7(c)):

In Mode 3, S_1 is OFF and S_2 remains ON. The energy stored in the input inductor during Mode 1 is completely transferred into the dc-link capacitors. The amount of stored energy in the input inductor depends upon the rectified supply voltage. This mode ends when the input inductor current reaches zero. Also during this mode, the load inductor current freewheels in the secondary of the transformer.

Mode 4 ($t_3 < t < t_4$)(Fig.3.7(d)):

In this mode, S_1 is OFF, the primary current of the main transformer circulates through diode D_1 and S_2 and the load inductor current freewheels in the secondary of the transformer.

Mode 5($t_4 < t < t_5$)(Fig.3.7(e)):

In this mode, S_1 and S_2 are OFF and the current in the transformer primary charges capacitor C_2 through the body diode of S_3 and switch S_4. This mode ends when switches S_3 and S_4 are switched on and a symmetrical period begins. In this mode, the load inductor current continues to transfer energy from input to the output.

It should be noted that the analysis and design of this converter is identical to that presented for converter in Chapter 2. Consequently, the analysis of the new TL single-stage converter is not presented here.

(a) Mode1 ($t_0 < t < t_1$)

(b) Mode2 ($t_1 < t < t_2$)

(c) Mode3 ($t_2 < t < t_3$)

(d) Mode4 ($t_3 < t < t_4$)

(e) Mode5 ($t_4 < t < t_5$)
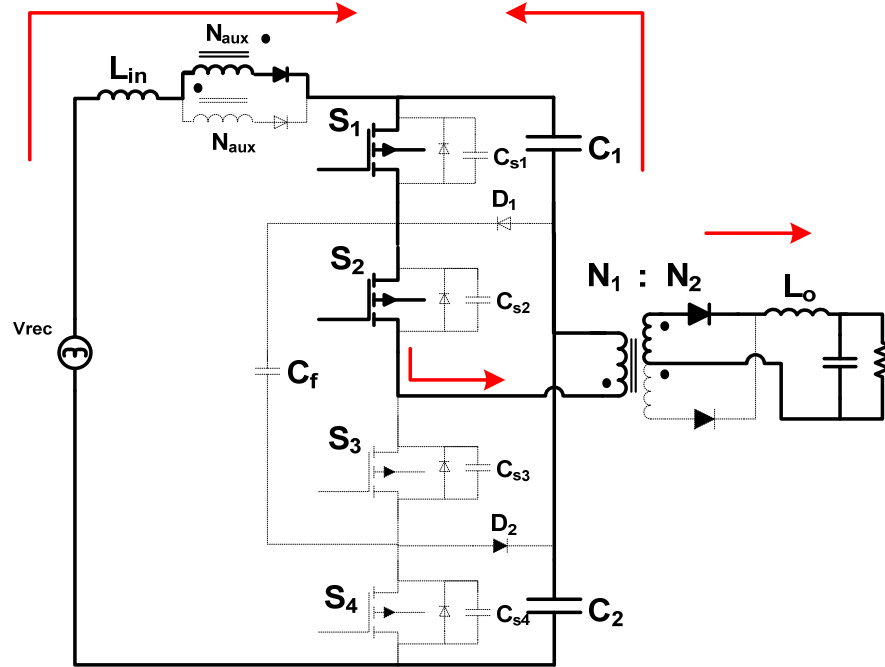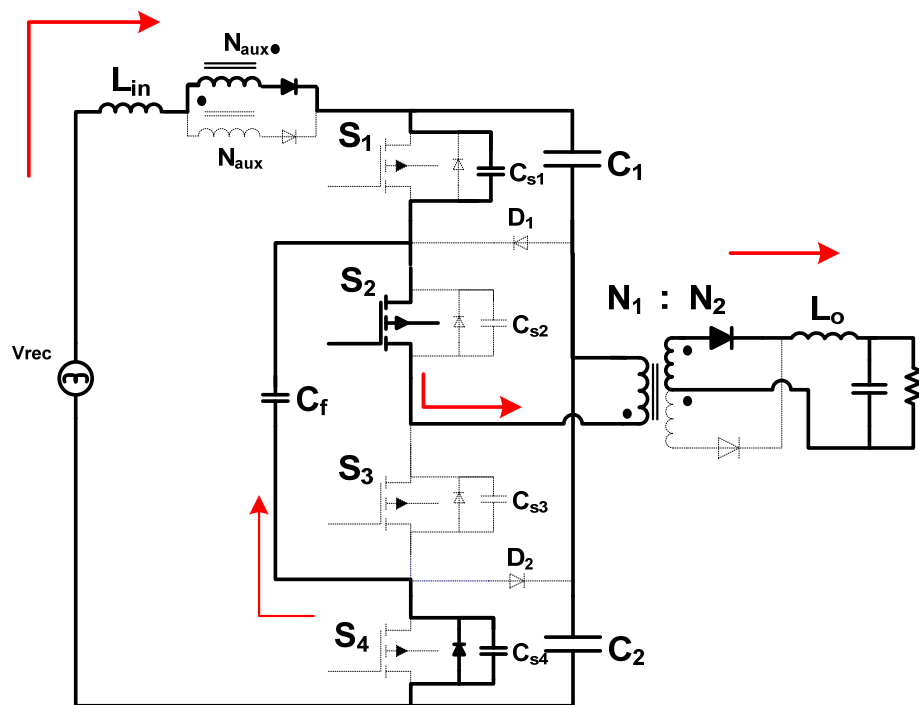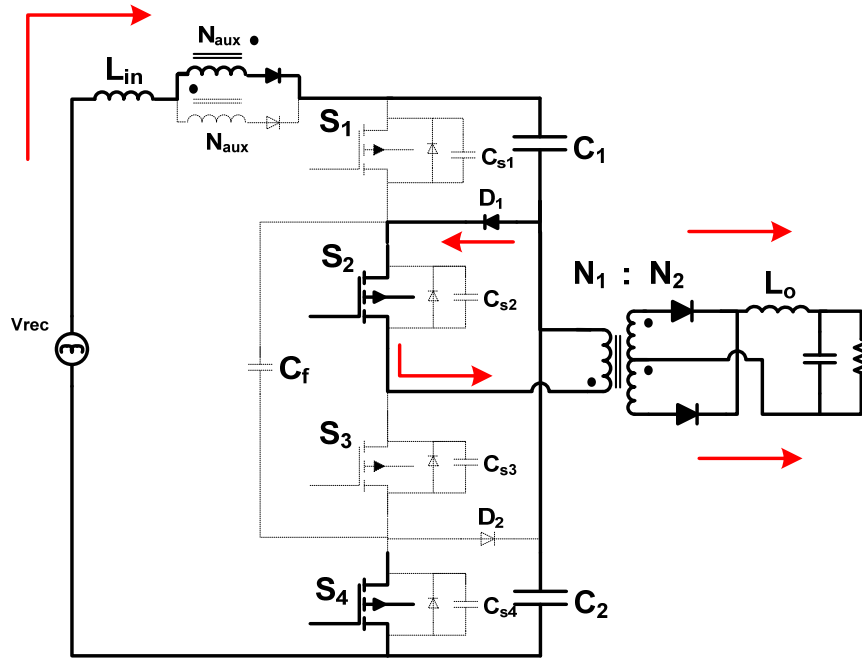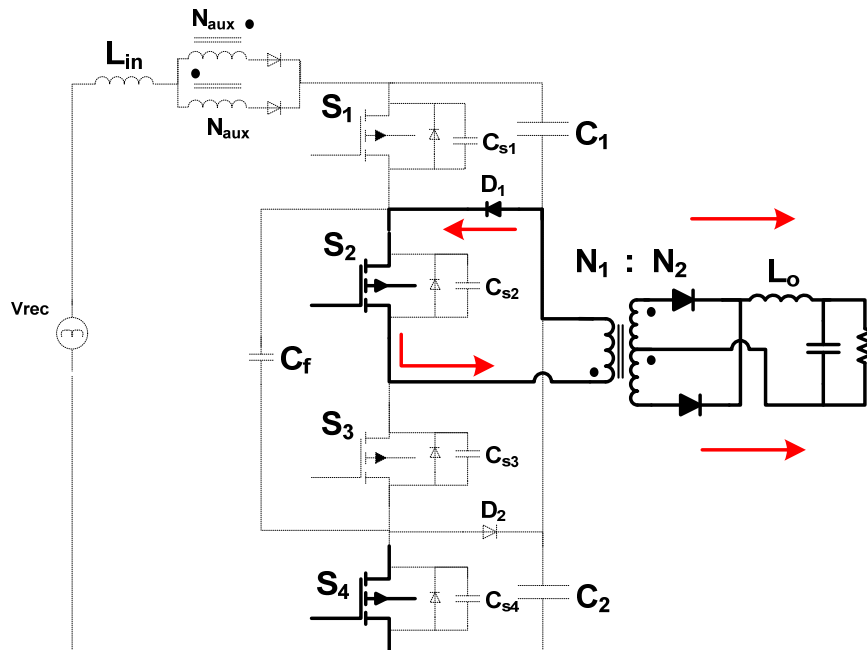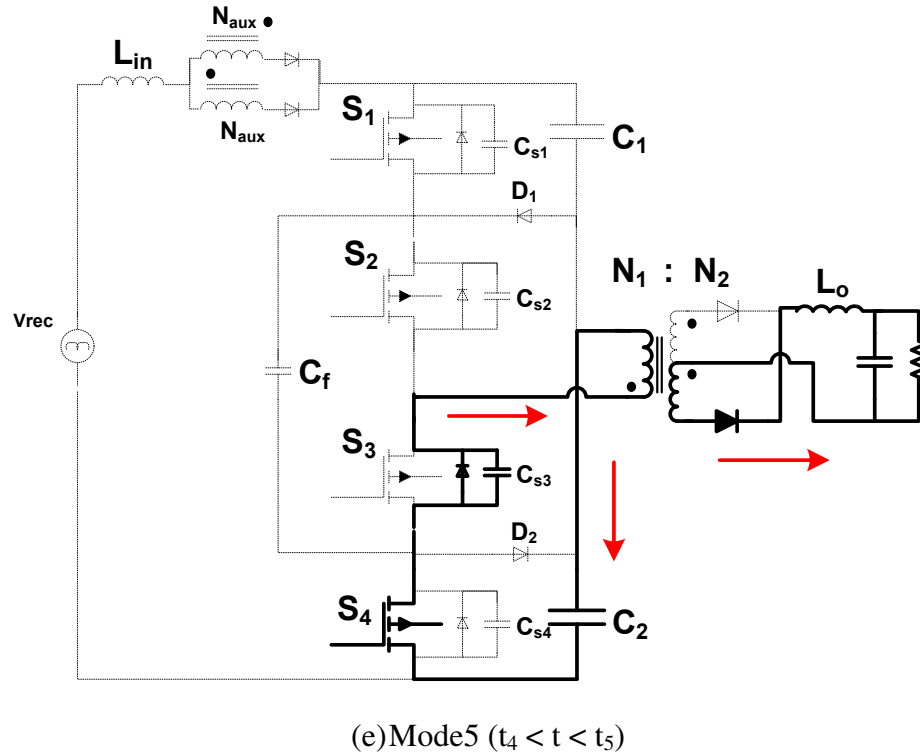
Fig.3.7. Modes of operation.

3.3.2. Experimental Results

A 48Vdc, 50 kHz experimental prototype of the proposed converter was built to confirm its feasibility and to compare its performance to the conventional three-level converter proposed in Chapter 2. It should be noted that the previous proposed converter was implemented with the PWM method and with standard phase-shift modulation PWM (PSM) and no difference in efficiency was found. The new TL single-stage converter was implemented with PSM.

For both converters, the input voltage was V_{in} = 90-265 V_{rms}, the main switches were FDL100N50F, and the diodes were UF1006DICT. The input inductance was L_{in} = 35 µH, L_o = 15 µH and $C_1 = C_2 = 2200$ µF. The value of C_f the new converter was 2200 µF. The main transformer ratio for both converters was 2.5:1. Typical converter waveforms are shown in Fig. 3.8-3.10.
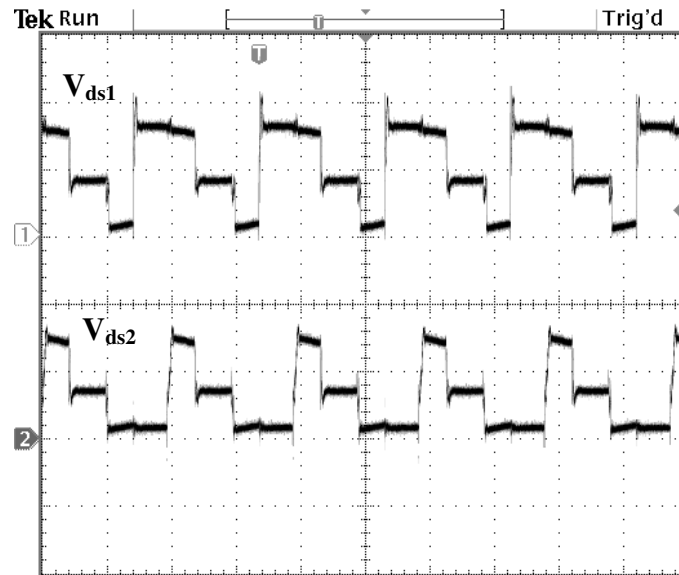
(a) Top switch voltages V_{ds1} and V_{ds2} (V: 100V/div., t:10 µs/div.)
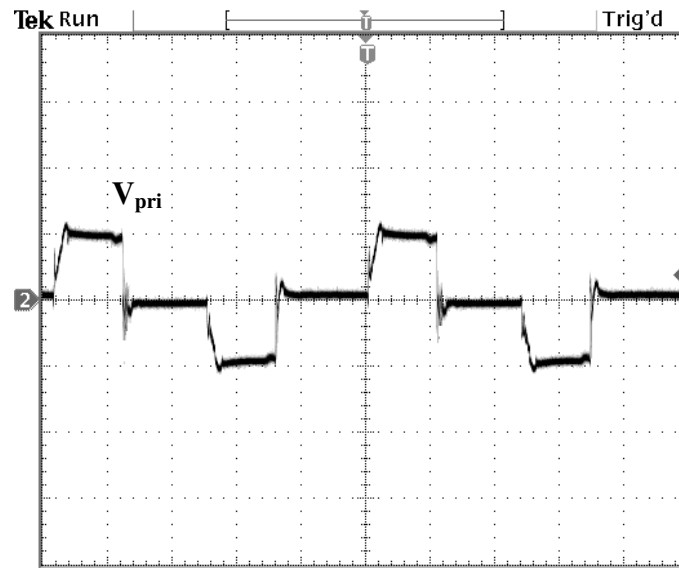
(b)Primary voltage of the transformer (V: 150V/div., t:4 µs/div.)

Fig.3.8. Typical waveforms of a PWM three-level Converter;

Fig. 3.8(a) shows typical voltage waveforms for the top switches S_1 and S_2 and Fig. 3.8(b) shows the voltage across the primary side of the main transformer for the PWM converter. Fig. 3.9(a) shows typical voltage waveforms for the top switches S_1 and S_2, and Fig. 3.9(b) shows the voltage across the primary side of the main transformer of the new converter. Fig.3.9(c) shows the voltage and current of the switch S_1.
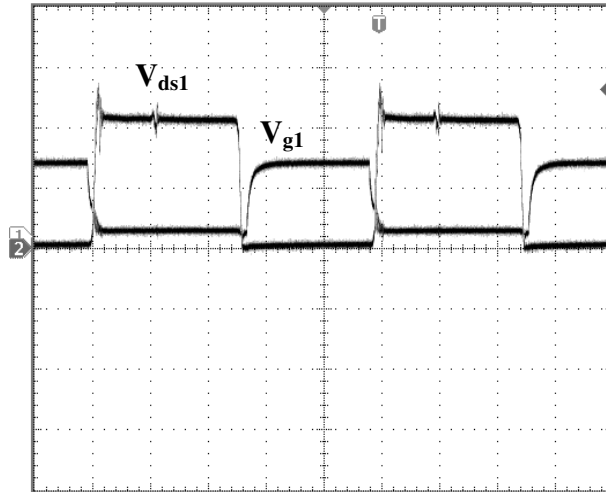
(a)   Gating signal and switch voltages of S_1 (V: 100V/div., t:4 µs/div.)
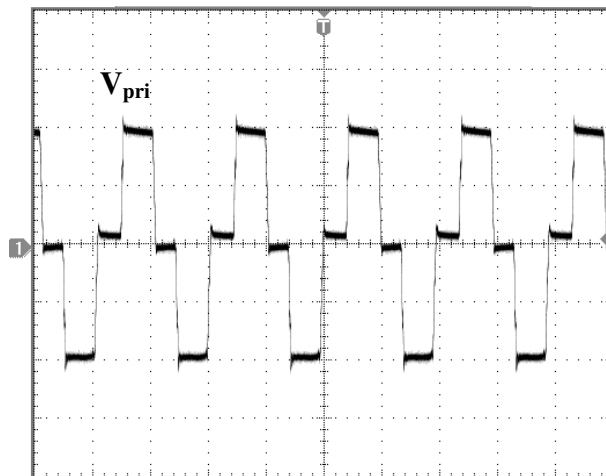
(b) Primary voltage of the transformer (V: 100V/div., t:10 µs/div.)
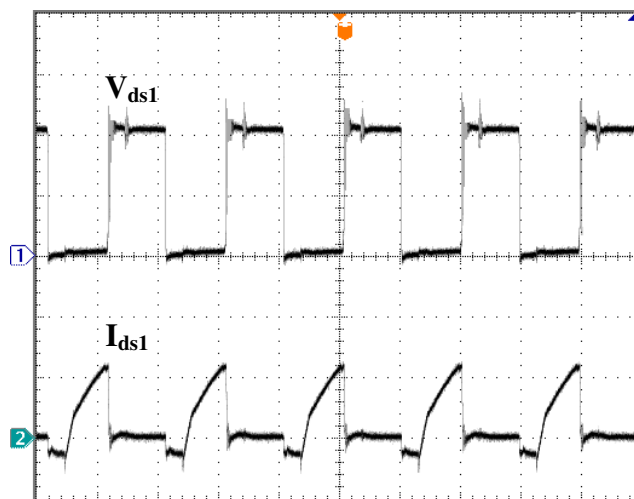
(c) V_{ds} and I_{ds1} current of S_1 (V: 100V/div., I:5A/div, t:10 µs/div.)

Fig.3.9. Typical waveforms of a PSM three-level converter.

Fig.3.10 shows a graph of curves of efficiency vs. output load for the two converters. It can be seen that that new three-level converter has a higher efficiency that the converter proposed in Chapter 2 under light load conditions and that the efficiency of the two converters are almost the same under heavy load conditions. This is because under light load conditions, where there is generally insufficient energy to discharge the switch output capacitances, the new three-level converter using PSM and flying capacitor C_f, can work with ZVS at least for two switches which is not possible for the converter in Chapter 2.
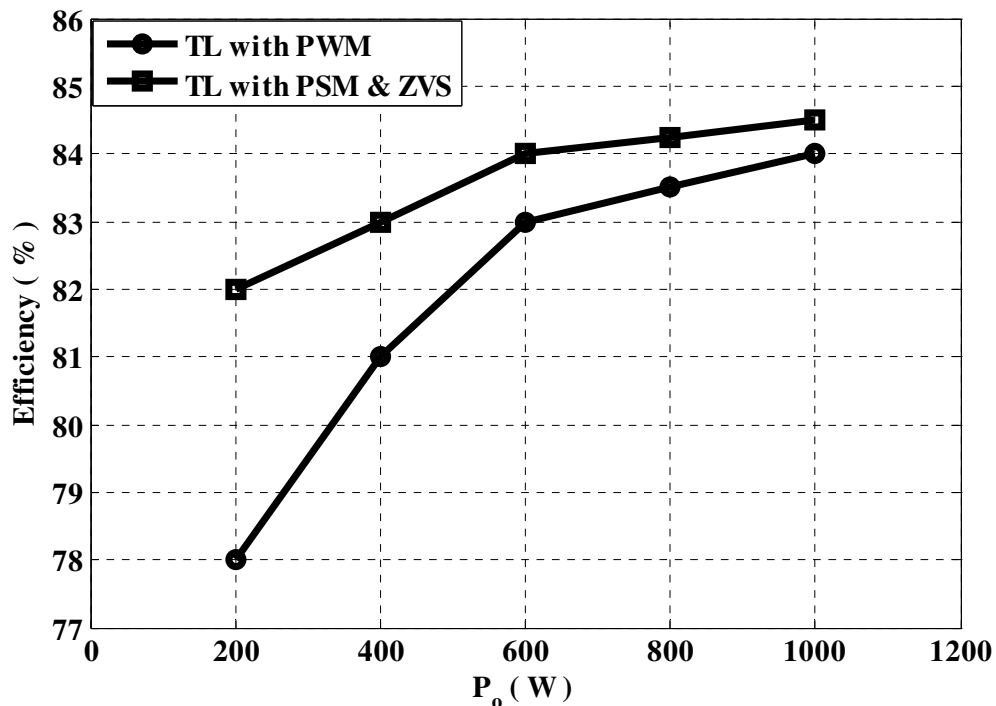
Fig.3.10. Efficiency of PWM and PSM three-level single-stage AC-DC converter.

It should be noted that the proposed converter can still operate with ZVS at 100W output power (10% of full load) and the PWM three-level converter can achieve ZVS up to 400W (30% of full load).

3.4. Conclusion

In this chapter, two modifications to the basic multilevel converter that was introduced in Chapter 2 were proposed. The first modification was the addition of a simple auxiliary circuit to the transformer secondary-side of the converter that is enabled only when the converter operates with light loads. This circuit allows larger output inductors to be used for heavier loads, which reduces output inductor current ripple and thus component peak current stresses and output voltage ripple. Such output inductors cannot be used in the basic topology as it would result in excessive primary-side dc bus voltages. The second modification was to change the basic topology to allow the converter to operate with phase-shift PWM modulation, which is the standard method of operating a full-bridge converter. This allowed the converter to operate with standard, commercially available ICs and with improved light load efficiency. The operation of both modified converters was reviewed and their feasibility was confirmed with results obtained from experimental prototypes.

Chapter 4

4. A Single-Stage Three-Level AC-DC Converter with Two Controllers

4.1. Introduction

The converters proposed in Chapters 2 and 3 were multilevel single-stage converters that were implemented with just a single controller that regulated the output voltage. Single-stage converters are typically implemented with a single controller to save on cost. Since it is standard practice to implement AC-DC converters with two controllers with the additional controller used to regulate the dc bus voltage, the main focus of this chapter is an examination of how a multilevel single-stage converter can be made to operate with two controllers instead of one. The implications of operating the converter in such a manner are discussed and experimental results obtained from a prototype converter are presented to show how the operation of the converter using two controllers differs from single-controller operation.

4.2. Converter Operation

The proposed converter, which is shown in Fig.4.1, integrates an AC-DC boost PFC converter into a three-level DC-DC converter. The AC-DC boost section consists of an input diode bridge, boost inductor L_{in}, boost diode D_{x1} and switch S_4, which is shared by the multilevel DC-DC section. This section is a conventional three-level converter except for diodes D_{x2}, which prevents input current from flowing to the mid-point of capacitors C_1 and C_2, and D_{x3}, which bypasses D_{x2}. Although there is only a single converter, it is operated with two independent controllers. One controller is used to perform PFC and regulate the voltage across the primary-side dc bus capacitors by sending appropriate gating signals to S_4. The other controller is used to regulate the output voltage by sending appropriate gating signals to S_1 to S_4.
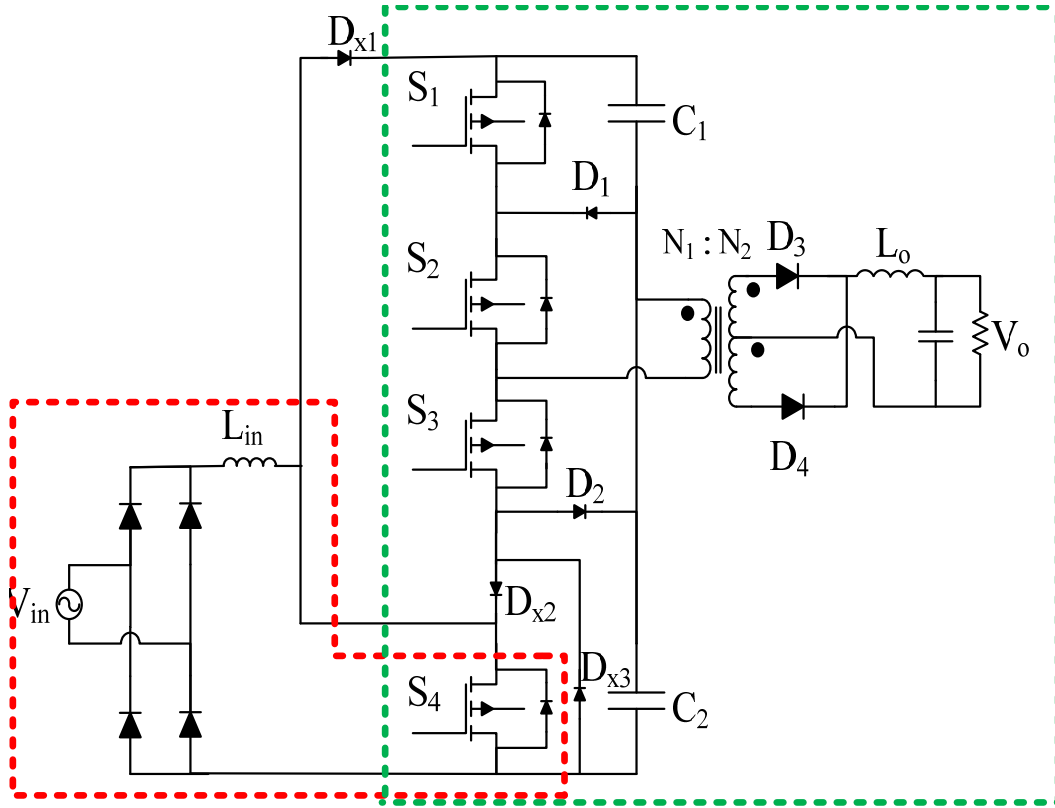
Fig.4.1. Proposed SSPFC converter with two controllers.

It should be noted that the control of the input section is decoupled from the control of the DC-DC section and thus can be designed separately. The gating signal of S_1, however, is dependent on that of S_4, which is the output of the input controller; how this signal is generated is discussed in detail in the next section. The gating signals for S_2 and S_3 are easier to generate as both switches are each ON for half a switching cycle, but are never ON at the same time.

Typical converter waveforms are shown in Fig.4.2, and equivalent circuit diagrams that show the converter's modes of operation are shown in Fig.4.3 with the diode rectifier bridge output replaced by a rectified sinusoidal source. As the input line frequency is much lower than the switching frequency, it is assumed that the supply voltage is constant within a switching cycle.
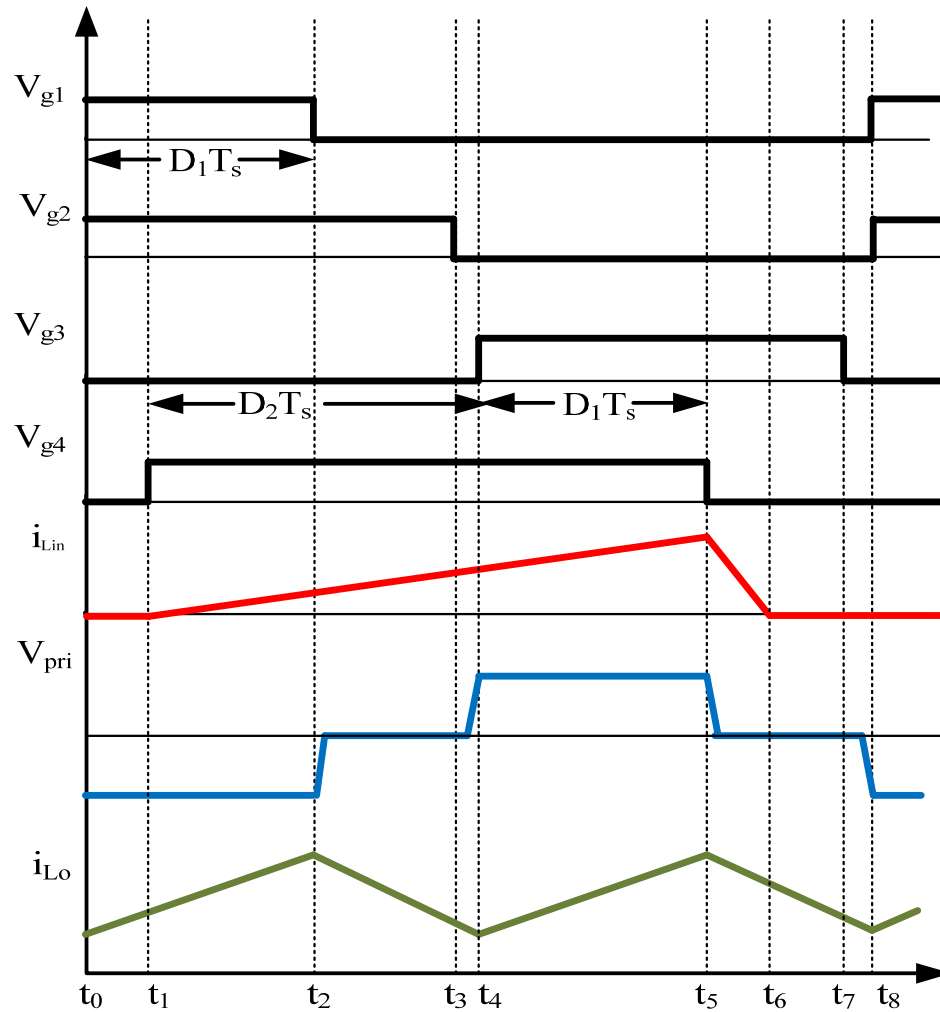
Fig.4.2. Typical waveforms describing the modes of operation.

The converter has the following modes of operation:

Mode 1 ($t_0 < t < t_1$):

During this mode, switches S_1 and S_2 are ON and energy from DC bus capacitor C_1 is transferred to the output load. In the output section, a positive voltage of $(V_{pri}/n)-V_o$ (where n is the ratio of primary to secondary transformer turns) is impressed across L_o and the current through it rises.

Mode 2 ($t_1 < t < t_2$):

In this mode, S_1 and S_2 remain ON and S_3 turns ON. The energy from dc bus capacitor C_1 is transferred to the output load. At the same time, the diode bridge output voltage V_{rec} is impressed across input inductor L_{in} so that the current flowing through this inductor rises.

Mode 3 ($t_2 < t < t_3$):

In this mode, S_1 is off, the primary current of the main transformer circulates through diode D_1 and S_2 and the load inductor current freewheels in the secondary of the transformer. Since, the S_4 is ON and the diode bridge output voltage V_{rec} is impressed across input inductor L_{in} so that the current flowing through this inductor rises.

Mode 4 ($t_3 < t < t_4$):

In this mode, S_1 and S_2 are OFF and S_4 is ON. The current in the primary of the transformer charges capacitor C_2 through the body diode of S_3 and D_{x3}.

Mode 5 ($t_4 < t < t_5$):

In this mode, S_3 and S_4 are ON. Energy flows from capacitor C_2 flows into the load while the current flowing through input inductor L_{in} continues to rise.

Mode 6 ($t_5 < t < t_6$):

In this mode, S_4 turns off. The current in input inductor flows thorough the diode D_{x1} to charge the capacitors C_1 and C_2. The current in the transformer primary flows thorough the S_3 and D_2. This mode ends when the inductor current reaches zero. Also during this mode, the load inductor current freewheels in the secondary of the transformer.

Mode 7 ($t_6 < t < t_7$):

In this mode, the load inductor current freewheels in the secondary of the transformer. This mode ends when the switches S_3 turns off.

Mode 8 ($t_7 < t < t_8$):

In this mode, S_3 is OFF and the current in the primary of the transformer charges capacitor C_1 through the body diodes of S_1 and S_2. Finally, converter reenters Mode 1.

Mode 1 ($t_0 < t < t_1$)

Mode 2 ($t_1 < t < t_2$)

Mode 3($t_2 < t < t_3$)

Mode 4 ($t_3 < t < t_4$)

Mode 5 ($t_4 < t < t_5$)

Mode 6 ($t_5 < t < t_6$)

Mode 7 ($t_6 < t < t_7$)

Mode 8 ($t_7 < t < t_8$)
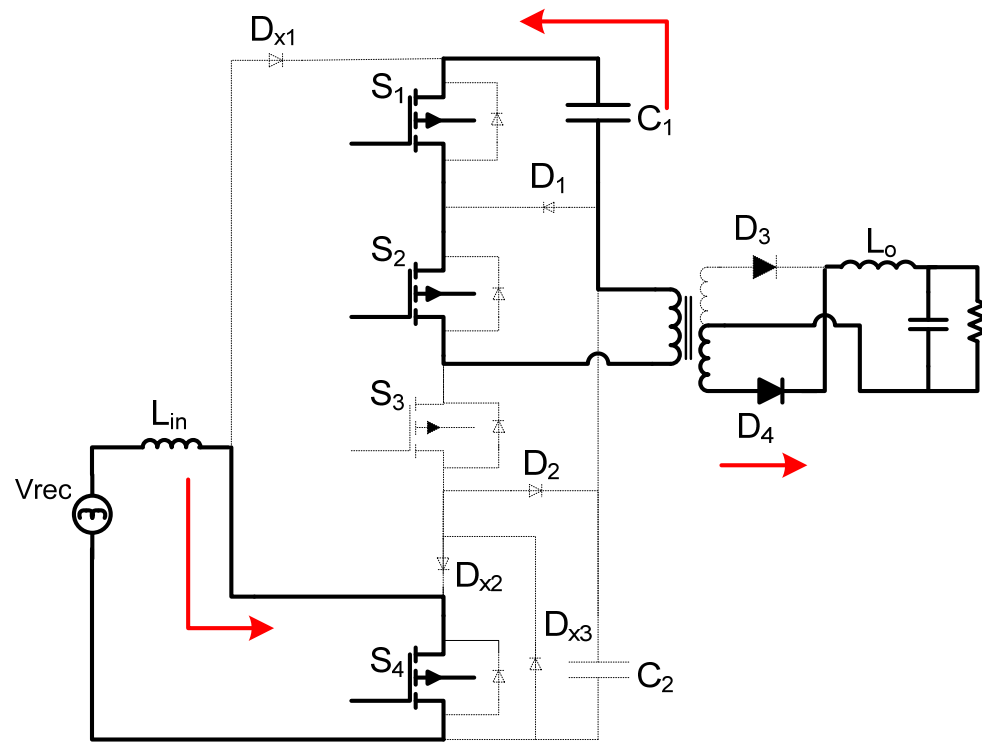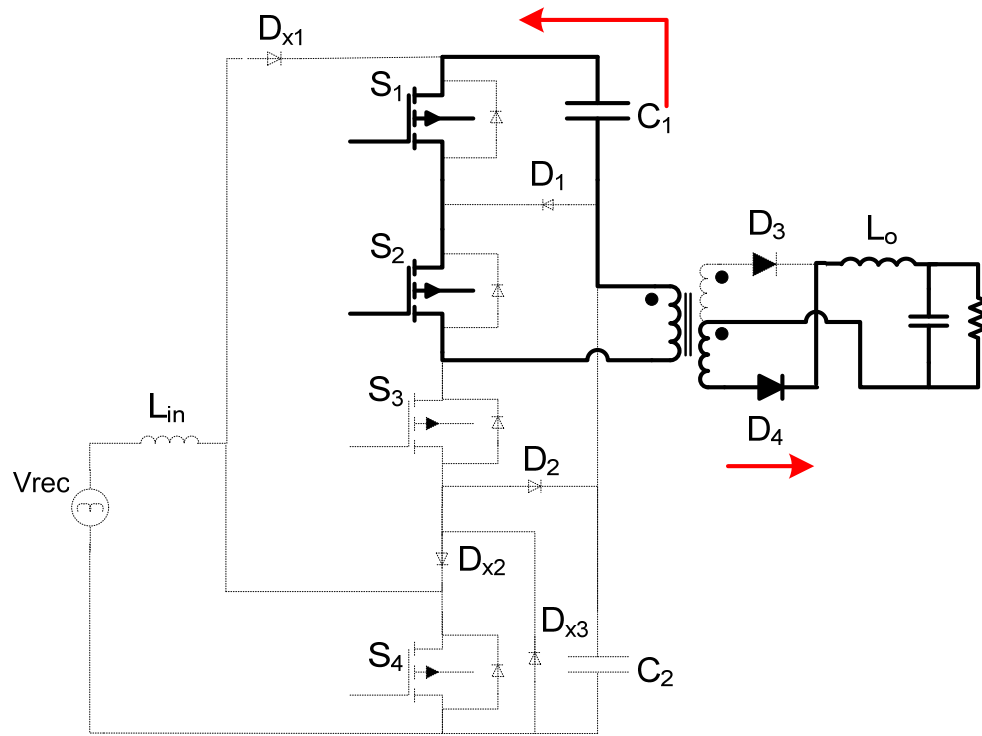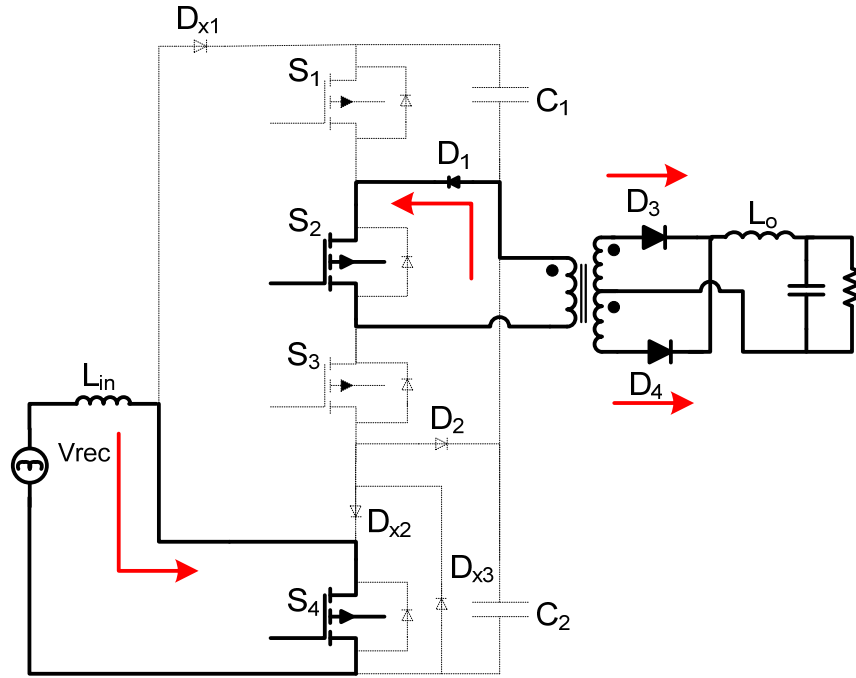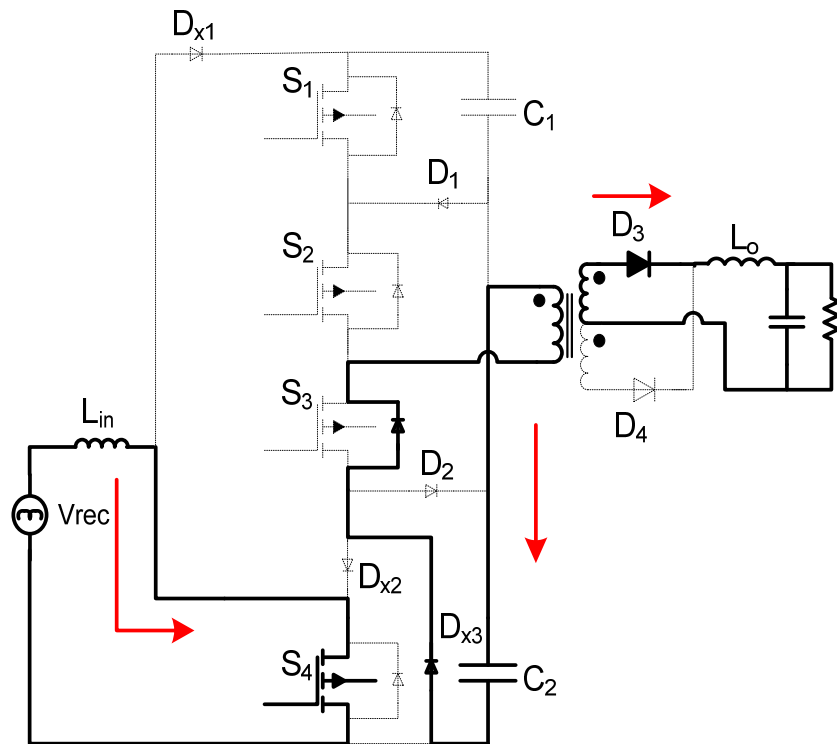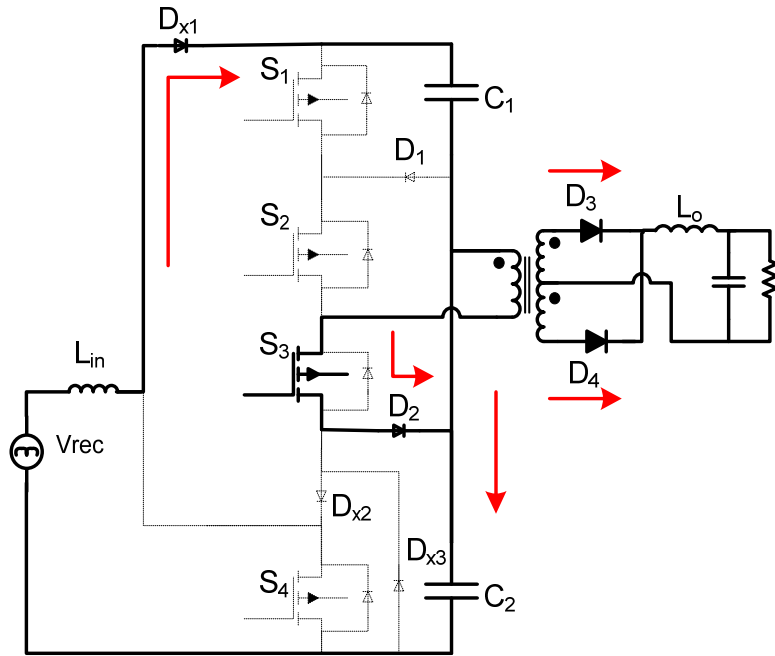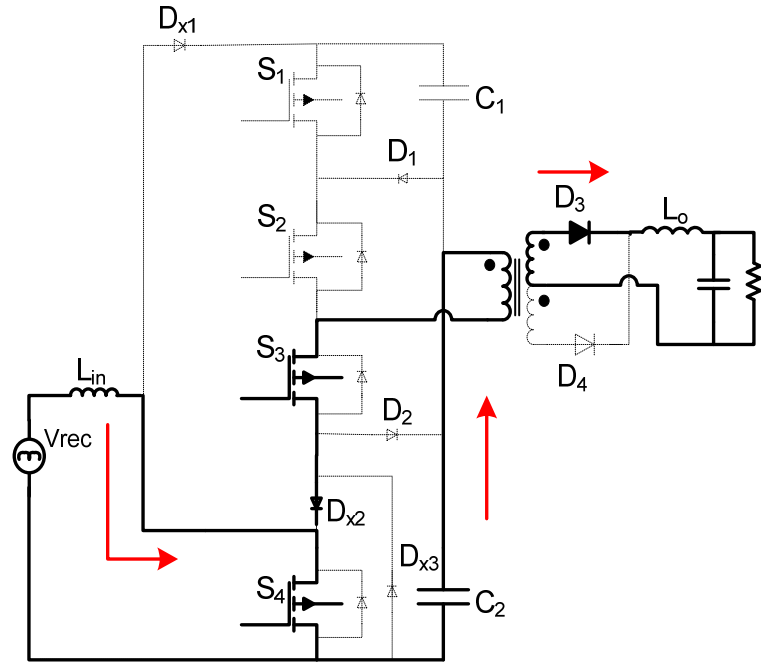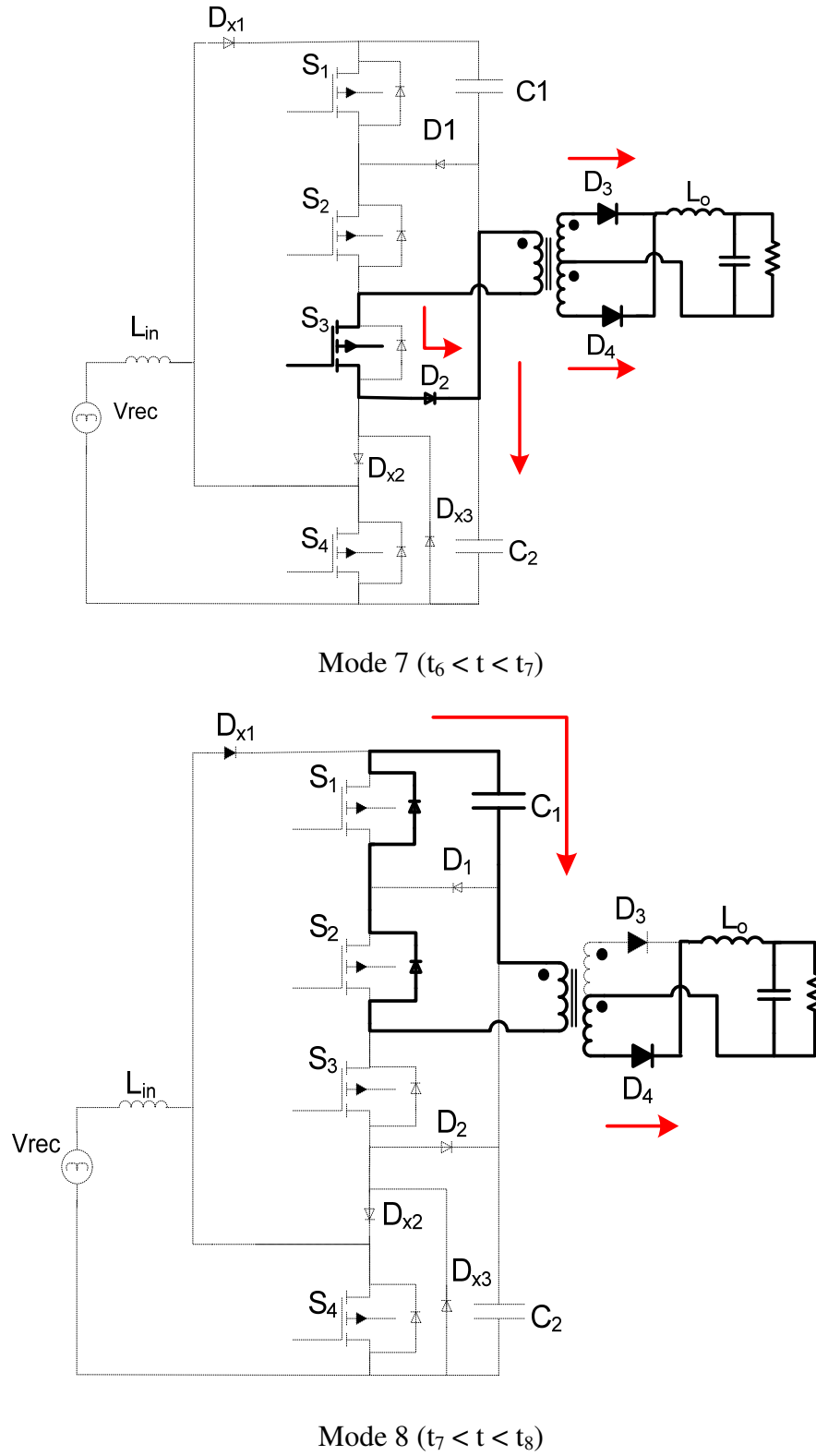
Fig.4.3. Equivalent circuits for each operation stage for the converter.

4.3. Converter Design

A procedure for the design of the converter is presented in this section and is demonstrated with an example. The converter is to be designed with the following parameters for the example:

Input voltage: V_{in} = 90−265 Vrms

Output voltage: V_o = 48 V

Maximum output power: P_o = 1350 W

Switching frequency: $f_{sw} = {}^1/_{T_{sw}}$ = 50 kHz

Input current harmonics: IEC1000-3-2 for Class A electrical equipment.

Step 1: Determine Value for Output Inductor L_o:

The output inductor should be designed so that the output current is made to be continuous under most operating conditions. The minimum value of L_o should be the value of L_o with which the converter's output current will be continuous on the when the converter is operating with maximum input voltage, minimum duty cycle (D_{min}), and at least 50% of maximum load. The minimum value of L_o can therefore be determined to be

$$L_{o,min} \geq \frac{V_0^2}{0.5\ P_{o,max}} \cdot \frac{(1-D_m)}{2} \cdot \frac{T_{sw}}{2} \tag{4.1}$$

Substituting $P_{o,max}$ = 1350 W, V_o = 48 V, T_{sw} = 20 μs, and D_m = 0.45 gives $L_{o,min} \geq$ 9.36 μH and the value of L_o should be larger to provide some margin. It should be noted that such a value is considerably higher than what is typically found in most other single-stage full-bridge converters, which must operate with very low output inductor values to prevent the dc bus voltage from becoming excessive. On the other hand, the value of L_o cannot be too high as the dc bus voltage of the converter will become excessive; a value of L_o = 10 μH, which is just above 9.36 μH is chosen.

Step 2: Determine Value for Turns Ratio of Main Transformer N:

The relation between V_{bus}, D, V_o and N is;

$$V_o = \frac{V_{bus}}{2N}.D \qquad (4.2)$$

The minimum value of N can be found by considering the case when the converter must operate with minimum input line and, thus, minimum primary-side dc bus voltage $V_{bus,min}$ and maximum duty cycle D_{max}. If the converter can produce the required output voltage and can operate with continuous output currents in this case, then it can do so for all cases.

$$N \geq \frac{V_{bus,min}}{2V_o}.D_{max} \qquad (4.3)$$

V_{bus} = 650V and it is achieved by controlling the S_4. Substituting V_o = 48 and D_{max} = 0.75 then the value of N should be equal or more than 5. In this example value of transformer ratio is considered to be equal to N=5.

Step 3: Determine Value for Inductor L_{in}:

The value for L_{in} should be low enough to ensure that the input current is fully discontinuous under all operating conditions, but not so low as to result in excessively high peak current.

For the case where L_{in} is such that the input current remains discontinuous for all operating conditions, the minimum value of L_{in} determine as:

$$L_{in,max} < \frac{(V_{bus,min}{}^2)*D_{max}*(1-D_{max})^2}{2.P_{o,max}.f_{sw}} \qquad (4.4)$$

Where D_{max} = 0.75, $V_{bus,min}$=650V, V , $P_{o,max}$=1.35 kW and f_{sw} = 50KHz The minimum value of L_{in} = 114 µH is found. For this design, L_{in} = 80 µH is used.

It should be noted that two controllers can be designed taking into considerations that their crossover frequencies should be wide apart on the s-plane. This is to ensure that the two controllers do not interact with each other. As mentioned earlier, one controller is used to control dc bus voltage and shape the input current and one controller for control output voltage. The time constant for PFC controller should be faster in compare to output voltage controller.

4.4. Experimental Results

A 48Vdc, 50 kHz experimental prototype of the proposed converter was built to confirm its feasibility. The input voltage V_{in} = 90-265 Vrms, The main switches (S_1, S_2 and S_3) were FDL100N50F and switch S_4 was IXFH20N100P and the diodes were UF1006DICT. The input inductance is L_{in} = 80 μH, L_o = 10 μH and C_1, C_2 = 2200 μF. The main transformer ratio was 5:1.

Typical converter waveforms are shown in Fig.4.4. Fig.4.4 (a) shows typical gating voltage waveforms for the top two switches and Fig.4.4 (b) shows the typical gating voltage waveforms for the bottom switches. Fig.4.4 (c) shows the voltage across the primary side of the main transformer. It can be seen that the proposed converter manages to impress a standard square voltage waveform across the transformer primary. Fig.4.4 (d) shows the input voltage and input current after filtering. It can be seen that the input current has no deadbands like those found in single-stage converter input currents, and thus it has a near unity input power factor. Fig.4.6 shows the experimental efficiency at different values of output power. It should be noted that the DC bus voltage was regulated for 650 V for the experimental results shown in Fig.4.4 and 4.5. Fig.4.6 and Fig.4.7 show the input current harmonic when V_{in} = 100 and 230 V_{rms} respectively; it can be seen from Fig. 4.7 that the converter can meet the IEC1000-3-2 Class A standard for electrical equipment.
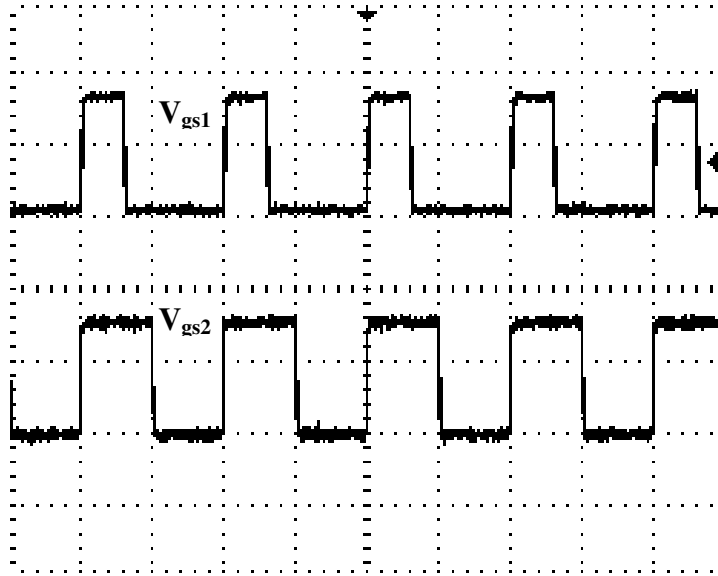
(a)(V: 10V/div., t: 10 µs/div.)
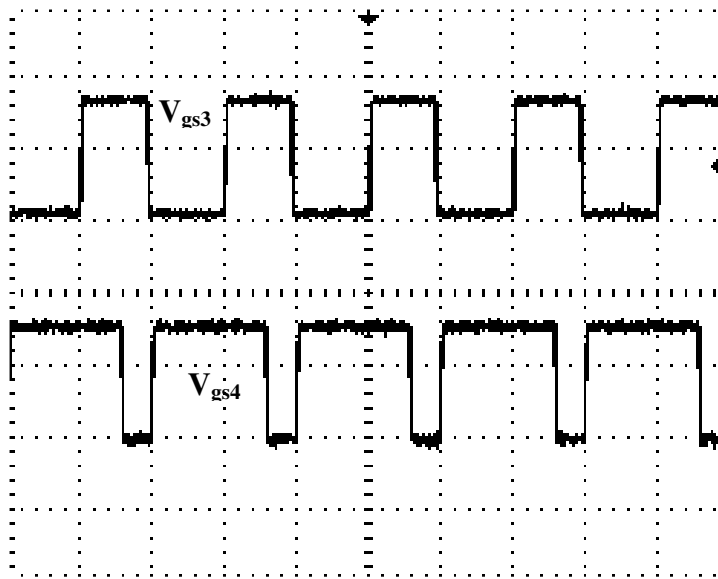
(b)(V: 10V/div., t: 10 µs/div.)
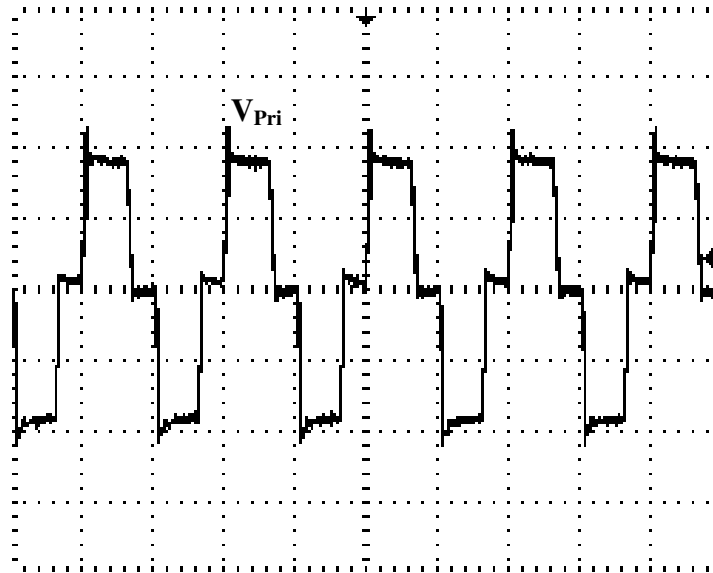
(c)(V: 200V/div., t: 10 µs/div.)
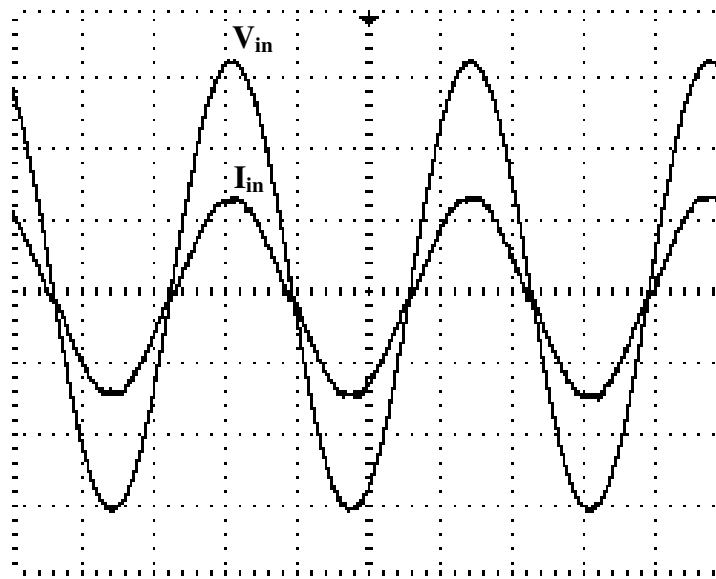
(d) (V: 50V/div., I: 10 A/div.)

Fig.4.4. Typical experimental waveforms. (a) Top switch voltages V_{gs1} and V_{gs2} (b) Bottom switch voltages V_{gs3} and V_{gs4} (c) Primary voltage of the main transformer (d) Input current and voltage.
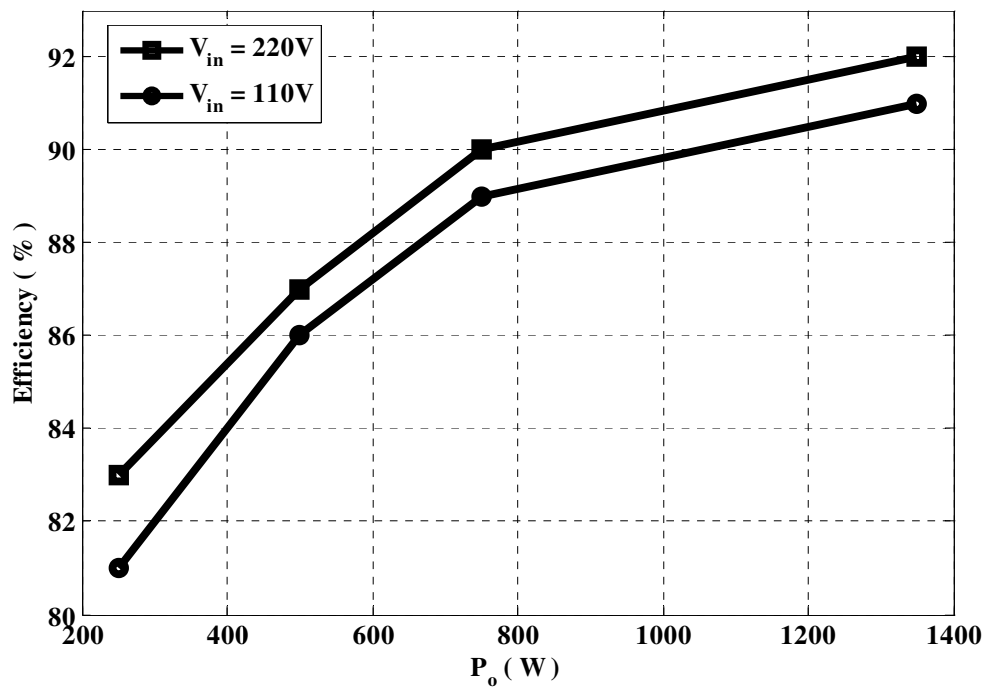
Fig.4.5. Proposed converter efficiency vs. load power
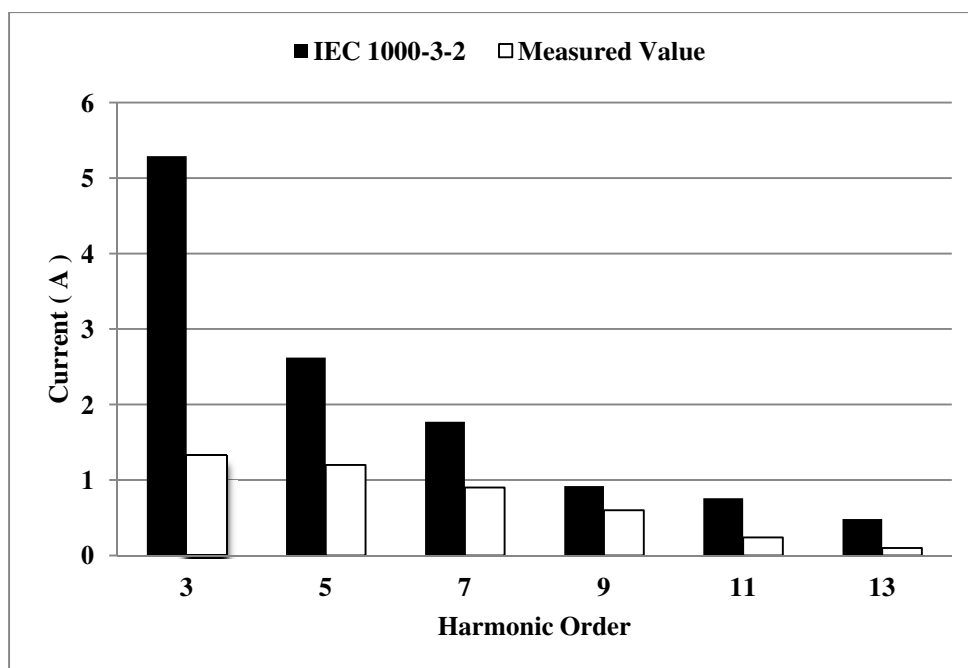
Fig.4.6. Input current harmonics at $V_{in} = 100$ V_{rms} , P_o=1.35kW compared to IEC1000-3-2 Class A standard.
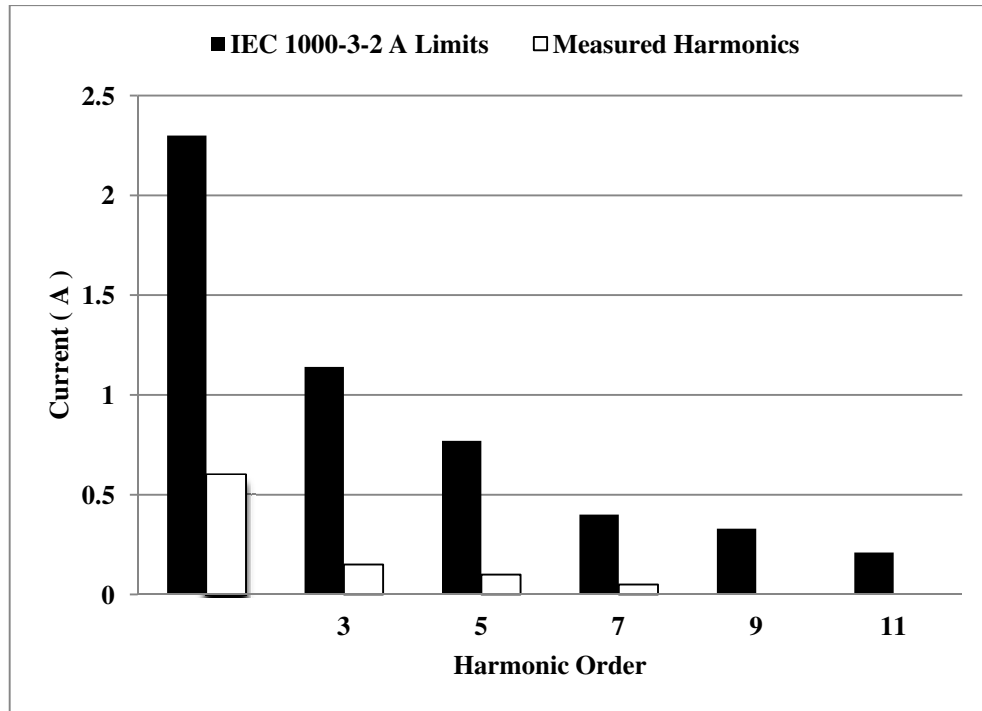
Fig.4.7. Input current harmonics at V_{in} = 230 V_{rms} , P_o=1.35kW compared to IEC1000-3-2 Class A standard.

It should be noted the efficiency of the proposed converter is generally better than the efficiency of the converter proposed in Chapter 2. One reason for this is that the two controller converter does not have the auxiliary winding that the converter proposed in Chapter 2 has so that it does not have the conduction losses that are associated with this winding. Another reason is that at heavy loads, the dc bus voltage of the two controller converter can be controlled to be higher (650V) that that of the converter in Chapter 2 (350V); this results in less current flowing in the primary side of the converter and therefore fewer conduction losses and higher efficiency at heavy loads.

4.5.   Conclusion

In this chapter, the steady-state characteristics and performance of a multilevel single-stage AC-DC converter implemented with a dedicated controller to regulate the primary-side dc bus voltage were examined. The basic principles of the converter

operating in this manner were explained as was its design, and experimental results that confirmed the feasibility of the converter were presented. It was shown that of two-controller operation results in better performance that the single-controller converter proposed in Chapter 2.

Chapter 5

5. Three-Phase Single-Stage Three-Level Power Factor Correction AC-DC Converters

5.1. Introduction

Since the problems associated with three-phase, single-stage power factor correction (SSPFC) converters are similar to those of single-phase SSPFC converters, it would seem that the solutions to these problems would be similar as well. It cannot be assumed, however, that a solution that is suited for a single-phase converter is naturally appropriate for a three-phase converter and vice versa. This is because some proposed single-phase SSPFC are not suited for the heavier loads that three-phase converters are used for, while some three-phase SSPFC topologies make use of the neutral connection of a three-phase source, which is not possible in single-phase converters.

In this chapter, the converter proposed in Chapter 2 is modified by changing its input section from a single-phase to a three-phase input. The steady-state characteristics of the new converter are determined by mathematical analysis and a design example is presented. The feasibility of the new three-phase converter is confirmed with results that were obtained from an experimental prototype.

Based on the new three-phase converter, a second three-phase converter is proposed. This second converter is similar to the first one except that its input is interleaved with two paralleled sections so that its input current can be reduced. In this chapter, the operation of the new three-phase SSPFC converter with interleaved input section and its modes of operation are explained in detail. The steady-state characteristics of the converter are determined by mathematical analysis and are used to develop a procedure for the design of key converter components. The feasibility of the new converter is confirmed with results that were obtained from an experimental prototype.

5.2. New Three-Phase Single-Stage Three-Level Power Factor Correction AC-DC Converters

The basic principle behind the proposed converter shown in Fig.5.1 is that it uses auxiliary windings that are taken from the converter transformer to cancel the dc bus capacitor voltage so that the voltage that appears across the diode bridge output is zero. This voltage cancellation occurs whenever there is voltage across the main transformer winding and current in the input inductors rises when it does. Whenever there is no voltage across the main transformer primary winding, the total voltage across the dc bus capacitors appears at the output of the diode bridge; since this voltage is greater than the input voltage, the input currents falls. If the input currents are discontinuous, they will be naturally sinusoidal and in phase with the input voltages. The typical waveforms are shown in Fig. 5.2.
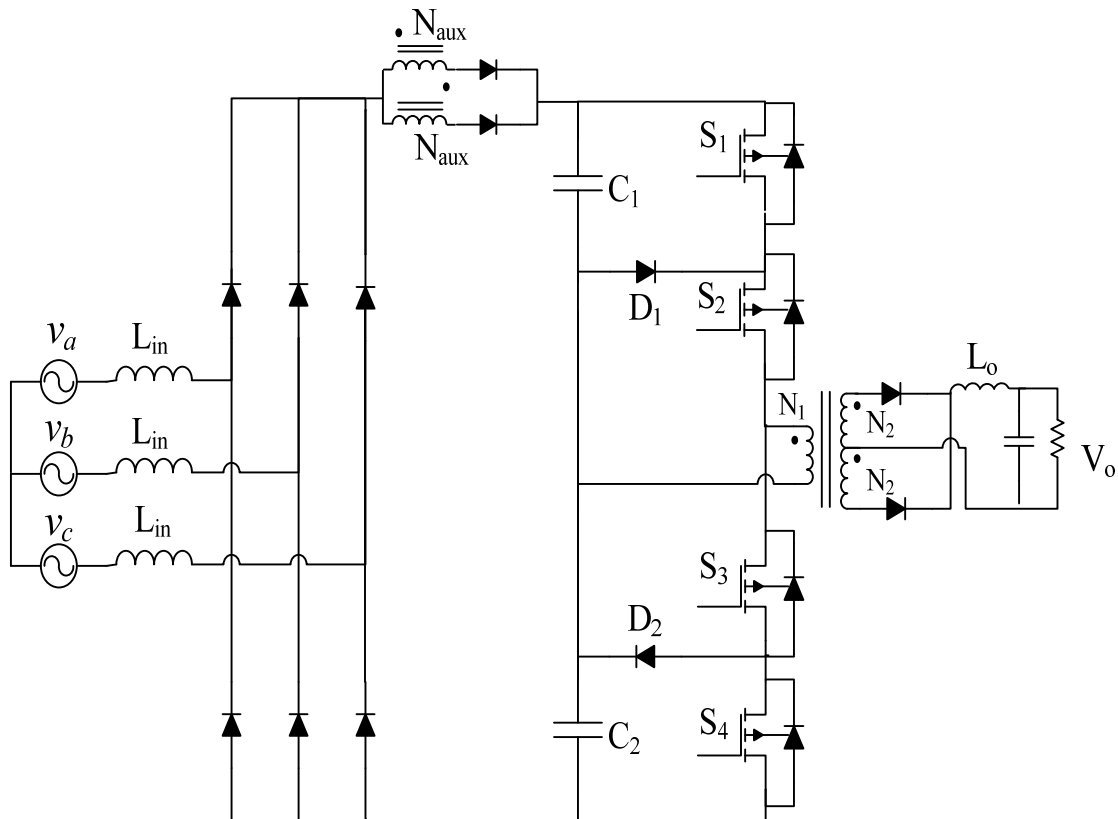
Fig.5.1 Three-phase three-level proposed converter.
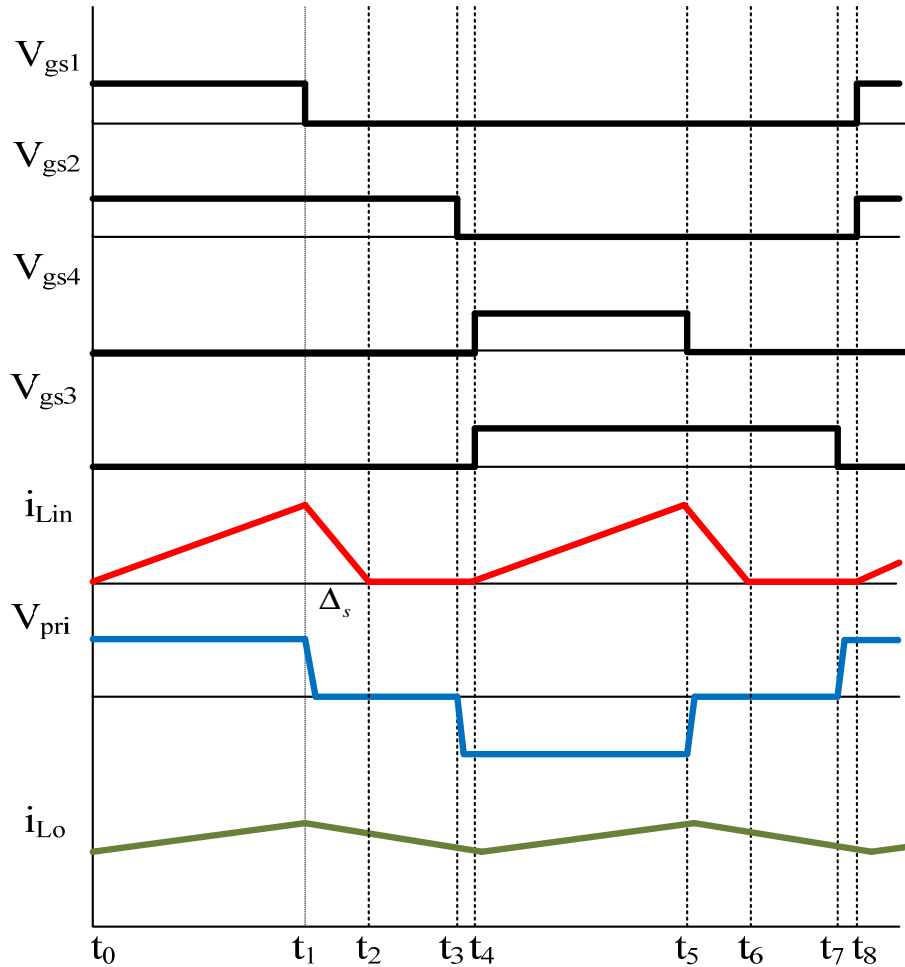
Fig.5.2. Typical waveforms describing the modes of operation.

5.2.1. Converter Operation

To simplify the analysis, the following assumptions are made: (i) The input voltage value can be considered as constant within a switching period as the period of the three-phase voltage supply is much longer than the switching period. (ii) All devices are ideal. (iii) The currents in inductors $L_a = L_b = L_c = L_{in}$ are i_{La}, i_{Lb}, i_{Lc} and have the same amplitude. (iv) The DC bus voltage has no ripple.

The equivalent circuit in each stage is shown in Fig. 5.3-5.6. The converter goes through the following modes of operation in a half switching cycle:

Mode 1 (t₀ < t < t₁) (Fig. 5.3):

During this interval, switches S₁ and S₂ are ON. The switches remain ON for a period given by $\frac{D}{2f_{sw}}$. In this mode, energy from the dc-link capacitor C₁ flows to the output load. Due to magnetic coupling, a voltage appears across one of the auxiliary windings and cancels the total dc bus capacitor voltage; the voltage at the diode bridge output is zero and the input currents rise. Due to the high switching frequency, the supply voltage is assumed constant within a switching cycle. In this mode, the three-phase input current equations are as follows:

$$\begin{cases} v_a = L_a \frac{di_{La}}{dt} \\ v_b = L_b \frac{di_{Lb}}{dt} \\ v_c = L_c \frac{di_{Lc}}{dt} \\ i_{La} + i_{Lb} + i_{Lc} = 0 \\ v_a + v_b + v_c = 0 \end{cases} \tag{5.1}$$
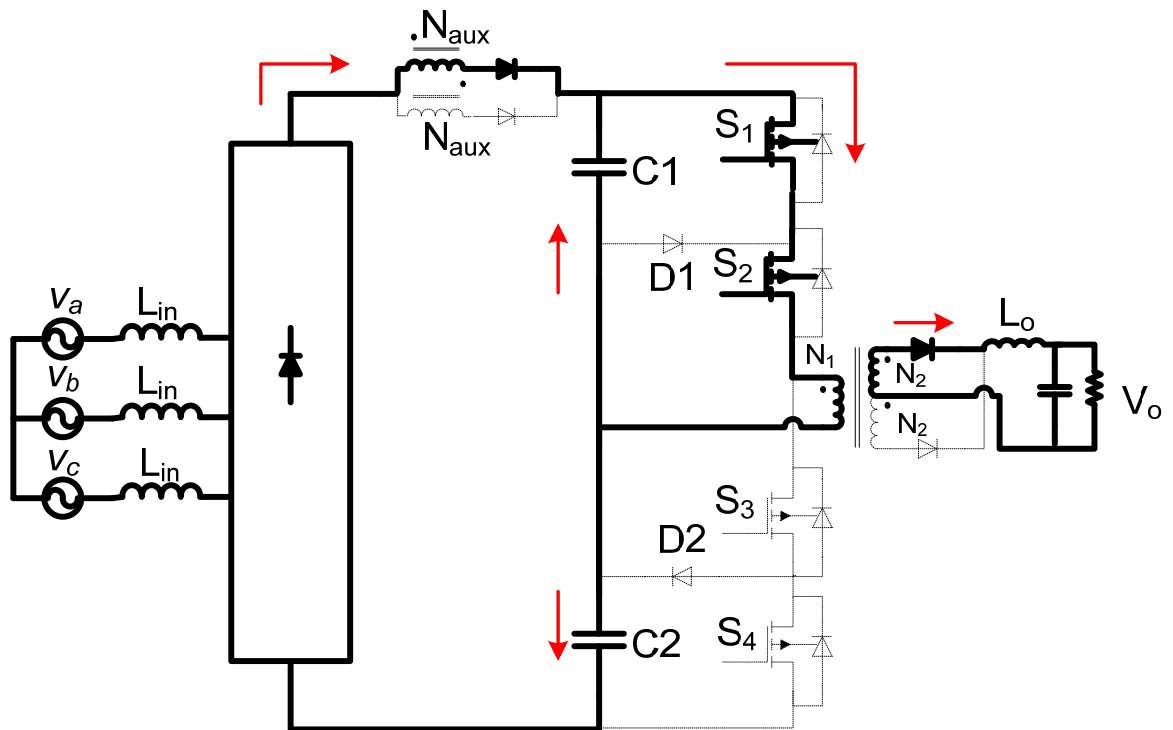
Fig.5.3. Mode 1 (t₀ < t < t₁)

As it can be seen from (5.1), the equations that describe the relation between the current and voltage of input currents i_{La} ,i_{Lb} and i_{Lc} *are* the same, but with different notation. Therefore, instead of using terms with subscripts a, b and c in this paper, a general notation $\overrightarrow{}$ is defined so that only one equation is written instead of three equations. Equation (5.1) can thus be rewritten as

$$\vec{v} = L_{in} \frac{d\overrightarrow{i_{L_{in}}}}{dt} \tag{5.2}$$

The auxiliary inductor current increases during this mode and the following expression can be written:

$$\overrightarrow{i_{L_{in},k}}(t) = \frac{|\overrightarrow{v_k}|}{L_{in}} \cdot t \tag{5.3}$$

at the end of Mode I, the current in the auxiliary inductor L_{in}, during the kth interval is

$$\vec{i}_{L_{in},k,max} = \frac{|\overrightarrow{v_k}|}{L_{in}} \cdot \frac{D}{2f_{sw}} \tag{5.4}$$

where v_k is the average value of the supply voltage in the interval k, D is the duty cycle, and f_{sw} is the switching frequency. Since the converter operates with a steady-state duty cycle D that is constant throughout the line cycle, the peak value of an input inductor current at the end of this mode is dependent only on the supply voltage.

The output inductor current can be expressed as

$$i_{Lo}(t) = \frac{V_{bus}/2N - V_L}{L_o} \cdot t \tag{5.5}$$

where V_{bus} is the average dc-link voltage and V_L is the average load voltage and N is the transformer ratio between input and output ($N = {}^{n_1}/{n_2}$). If it is assumed that the output inductor current is continuous then the following expression for peak-to-peak ripple can be derived;

$$\Delta i_{Lo} = \frac{{}^{V_{bus}}/{2N} - V_L}{L_o} \cdot \frac{D}{2f_{sw}} \tag{5.6}$$

Mode 2 ($t_1 < t < t_2$) (Fig.5.4):

In this mode, S_1 is OFF and S_2 remains ON. The energy stored in the auxiliary inductors during the previous mode is completely transferred into the dc-link capacitor. The amount of stored energy in the auxiliary inductor depends upon the rectified supply voltage. This mode ends when the auxiliary inductor current reaches zero. Also during this mode, the load inductor current freewheels in the secondary of the transformer. The voltage across the auxiliary inductors in Mode II is $\left|\vec{V_k}\right| - V_{bus}$, thus, the auxiliary current expression is as follows:

$$\frac{d\overrightarrow{i_{L_{in}}}}{dt} = \frac{\left|\vec{V_k}\right| - V_{bus}}{L_{in}}$$

$$\vec{i}_{L_{in},k}(t) = i_{L_{in},k,max} - \frac{V_{bus} - \left|\vec{V_k}\right|}{L_{in}} \cdot t \tag{5.7}$$

This mode ends when the auxiliary inductor current reaches zero.

This mode lasts for ${}^{\Delta_{s,k}}/{2f_{sw}}$ amount of time; using (5.4), the following expression can be found:

$$\vec{\Delta}_{s,k} = \frac{\left|\vec{V_k}\right|}{V_{bus} - \left|\vec{V_k}\right|} D \tag{5.8}$$

iod of Mode II.
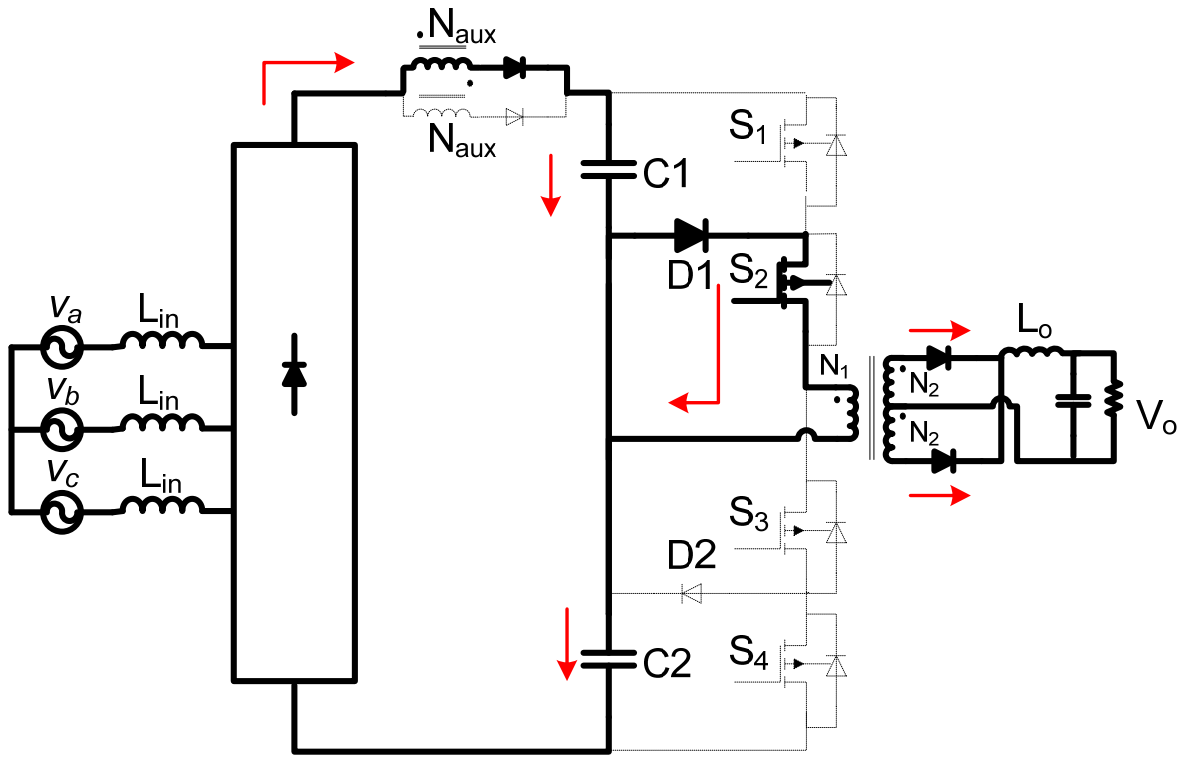
Fig.5.4. Mode 2 ($t_1 < t < t_2$)

Equation (5.8) shows that the duration of this mode is time varying along one ac line period. In order to ensure a discontinuous input current, the normalized period $\Delta_{s,k}$ must satisfy the expression $D + \Delta_{s,k} < 1$ for any interval k and any load conditions. Using (5.8), this constraint can be written as

$$V_{bus} > \frac{|\vec{V_k}|}{1 - D} \tag{5.9}$$

On the other hand, the load inductor current freewheels in the secondary of the transformer, which defines a voltage across the load filter inductor equal to $-V_L$; therefore, the load inductor current is given by

$$i_{Lo}(t) = i_{Lo,max} - \frac{V_L}{L_o}t \tag{5.10}$$

and

$$\Delta i_{Lo} = -\frac{V_L}{L_o}\frac{1-D}{2f_{sw}} \tag{5.11}$$

Consequently, the following expression can be derived from (5.6) and (5.11)

$$V_o = \frac{V_{bus}}{2N}D \tag{5.12}$$

Mode 3 ($t_2 < t < t_3$) (Fig. 5.5):

In this mode, the primary current of the main transformer circulates through D_1 and S_2 and the output inductor current freewheels in the secondary. There is no energy transferred to the dc bus capacitors.

Mode 4 ($t_3 < t < t_4$) (Fig. 5.6):

In this mode, S_1 and S_2 are OFF and the primary current of the transformer charges C_2 through the body diodes of S_3 and S_4. Switches S_3 and S_4 are switched ON at the end of this mode and the half switching cycle ends. For the remainder of the switching cycle, the converter goes through Modes 1 to 4, but with S_3 and S_4 ON instead of S_1 and S_2.

Mode 5 ($t_4 < t < t_5$):

In this mode, S_3 and S_4 are ON a symmetrical period begins. In this mode, energy flows from the capacitor C_2 into the load. The voltage across the auxiliary inductors becomes only the rectified supply voltage of each phase and the current flowing through each inductor increases.
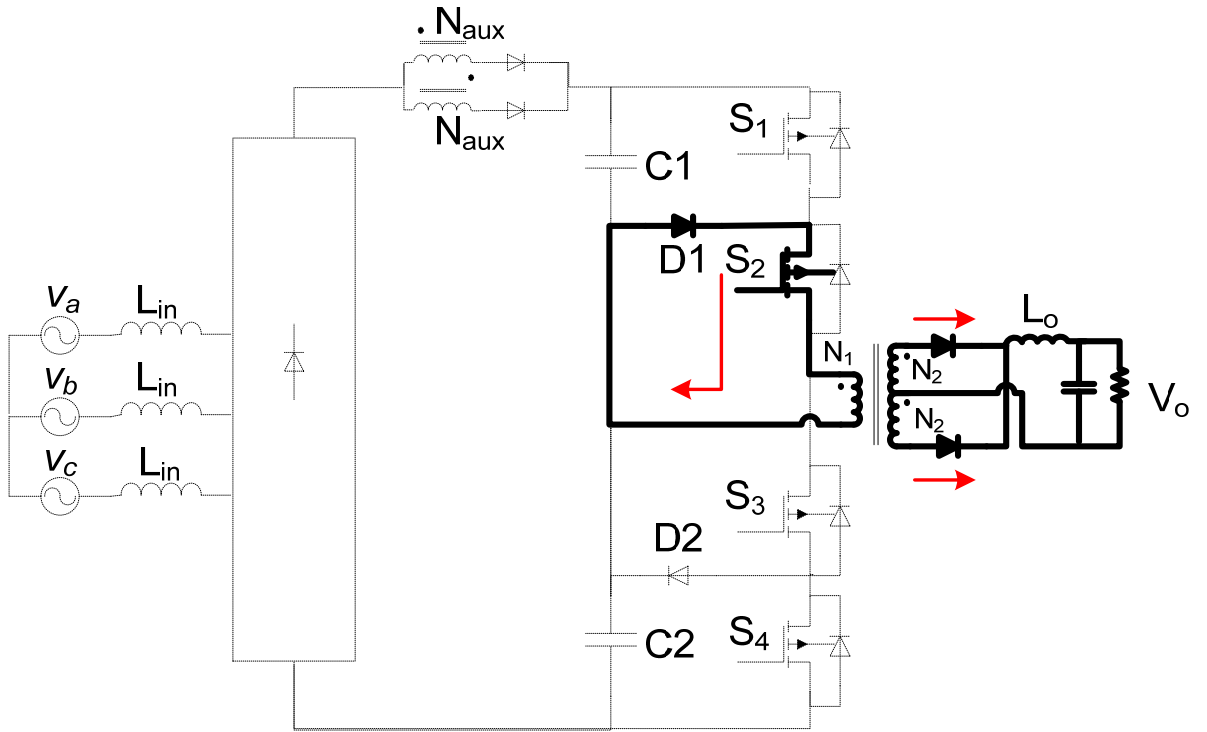
Fig.5.5. Mode 3 ($t_2 < t < t_3$)
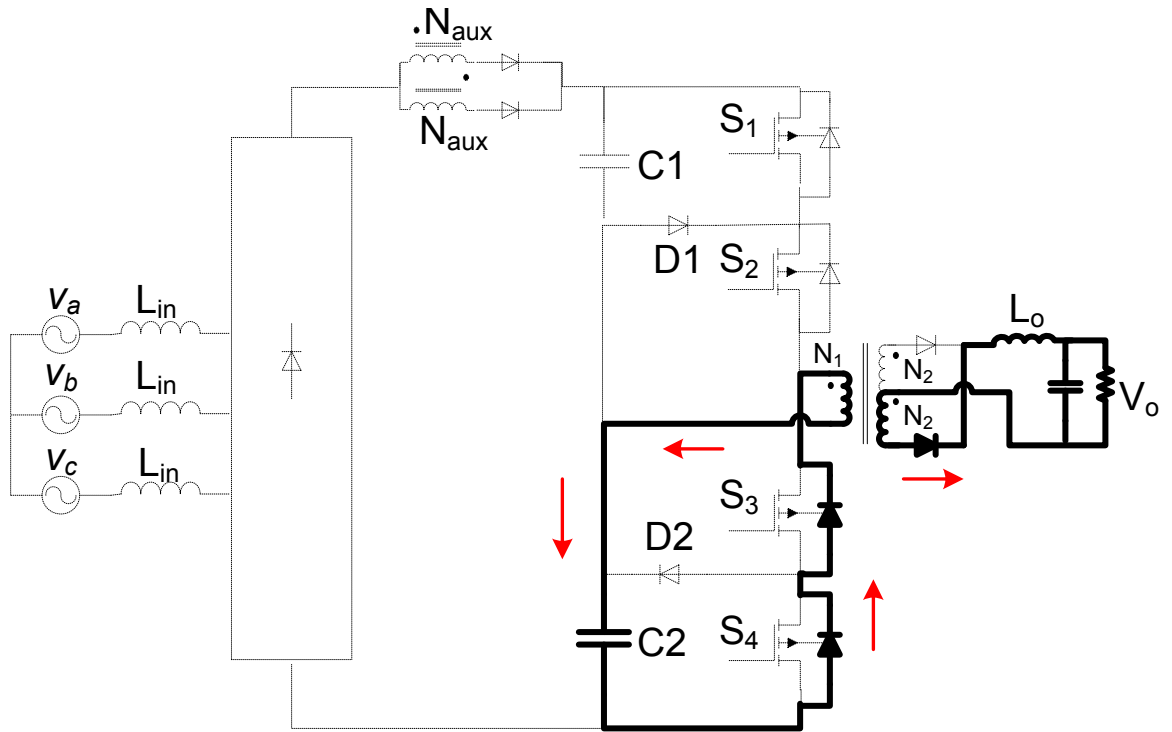
Fig.5.6. Mode 4 ($t_3 < t < t_4$)

Mode 6 (t₅ < t < t₆):

In this mode, S_3 is ON and S_4 is OFF. The energy stored in the auxiliary inductors during the previous mode is completely transferred into the dc-link capacitor.

Mode 7 (t₆ < t < t₇):

In this mode, S_4 is OFF and the primary current of the main transformer circulates through the diode D_2 and S_3. The output inductor current also freewheels in the secondary of the transformer during this mode.

Mode 8 (t₇ < t < t₈):

In this mode, S_3 and S_4 are OFF and the primary current of the transformer charges the capacitor C_1 through the body diodes of S_1 and S_2., Switches S_1 and S_2 are switched on at the end of this mode

Output voltage regulation can be done by standard control methods that control duty cycle D. Duty cycle, D in Eq. (5.4), is defined as the time when S_1 and S_2 are both ON during the first half cycle or when S_3 and S_4 are both ON during the second half cycle. These two cases correspond to energy transfer modes of operation. Any control method that can be used to regulate a two-level full-bridge converter by controlling D can be used to regulate the proposed converter; the only difference is how the gating signals are implemented. For example, the control for the proposed converter can be implemented with a conventional phase-shift PWM controller and some logic can be added to the output of the controller to generate the appropriate gating signals.

5.2.2. Steady State Analysis

In order to develop a procedure that can be used to design the proposed converter, the steady-state operation of the converter must be analyzed to determine its behavior for any given set of specifications (line-to-line input voltage $V_{ll,rms}$, output voltage V_o, output current I_o, and switching frequency f_{sw}) and any given set of component values input

inductors $L_a=L_b=L_c=L_{in}$, duty ratio D, transformer turns ratio $N = n_1/n_2$, output inductor L_o). Important converter characteristics can be determined after the analysis has been performed and then used to develop the design procedure.

Similar analysis that has been done for a single-phase SSPFC converter can be applied for three-phase SSPFCC converter. The key parameter that needs to be determined for the design of the converter is the dc bus capacitor voltage V_{bus}, because it is only then that other parameters such as input current can be determined. Unlike a conventional two-stage converter, a single-stage converter is not solely regulated by the ac-dc boost PFC stage and cannot be purposefully kept constant. This voltage can be derived by noting that energy equilibrium must exist for storage-capacitor when the converter is in steady-state operation.

The energy pumped into the capacitor from the input section must be equal to the energy that provides to the output, so that the net dc current flowing in and out of must be zero during a half-line cycle. However, this cannot be determined by an equation with a closed-form solution due to the various possible combinations of input and output modes of operation, but it must instead be determined using a computer program.

If it is assumed that the converter has ideal semiconductors, and an ideal transformer with no leakage inductance and negligible magnetizing current, then for an operating point with given input voltage V_{in} , output voltage V_L , switching frequency f_{sw}, input inductor L_{in}, output inductor L_o, transformer turns ratio $N = N_{pri}/N_{sec}$, and output current I_o can be determined as follows:

1) Select the set of specifications and components values to be considered. Assume a duty cycle D as an initial "guess"; (i.e., D=0.5) to start the process of determining a corresponding dc bus capacitor voltage V_{bus}.

2) Assume that the output current is continuous; then, use (5.12) to find V_{bus}:

$$V_{bus} = \frac{2V_0 N}{D} \tag{5.13}$$

With this value of V_{bus}, verify that the output current is continuous by seeing that the peak output current ripple does not exceed the average current I_o

$$\frac{1}{2}\frac{\frac{V_{bus}}{2N}-V_o}{L_o}\cdot\frac{D}{2f_{sw}} < I_o \tag{5.14}$$

If this relation is satisfied, then V_{bus} is equal to the value determined in (5.13). If not, then the output current is discontinuous and V_{bus} must be determined using (5.15), which has been derived for DCM;

$$V_{bus} = 2N\frac{V_0 + \sqrt{V_o^2 + \frac{16P_oL_of_{sw}}{D^2}}}{2} \tag{5.15}$$

With V_{bus} known, find the average current that flows out of capacitors during a half-line cycle using either (5.16) for CCM or (5.17) for DCM

$$I_{cb,out-avg} = \frac{I_oD}{2N} \tag{5.16}$$

$$I_{cb,out-avg} = \frac{D^2}{4NL_of_{sw}}\left(\frac{V_{bus}}{2N} - V_o\right) \tag{5.17}$$

3) Determine the average current that is fed from the input to Capacitors during a half-line cycle using (5.17)

$$I_{cb,in-avg} = 3*(2f_{in}\sum_{k=0}^{m}\int_{t^*}^{t_k}\left[\frac{v_{in,k}-V_{bus}}{L_{in}}(t-t^*) + I_{in,k}^*\right]dt) \tag{5.18}$$

Where $I_{in,k}^*$ is the peak input current value during a switching cycle k. If (5.18) is equal to (5.14) or (5.15), then the converter is confirmed to be operating under steady-state conditions and the value of V_{bus} that has been calculated is valid. If not, then the

operating point for which is to be determined is not a valid operating point, and the procedure must be repeated for a different value of D. The flowchart in Fig. 5.7 shows the procedure for the steady-state analysis, which can be implemented in a computer program.
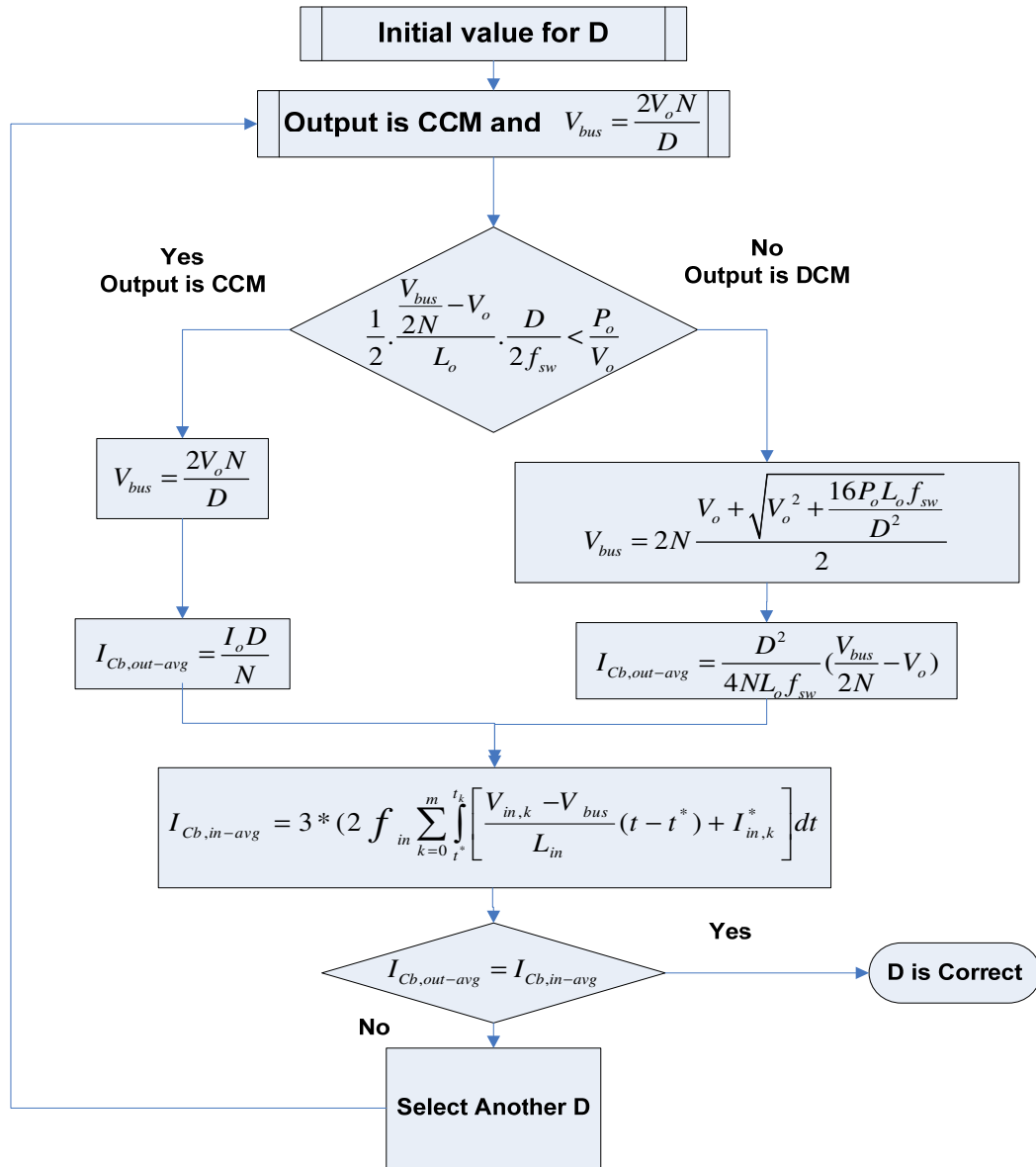
Fig.5.7. The procedure of steady state analysis for determining the dc bus voltage.

The procedure can be repeated to determine V_{bus} (or any other parameter) for other operating points, in order for curves to be generated for analysis and design purposes.

The converter operating characteristics for any given input and output voltage are dependent on three key parameters: transformer turns ratio N, input inductance L_{in} and output L_o. In this section, the effect of each of these parameters is examined with graphs of characteristic curves that have been generated with a computer program based on the procedure described above.

A. *Effect of Output Inductor Value L_o on DC Bus Voltage V_{bus}*

It can be seen from Fig. 5.8 that varying L_o (but keeping all the other parameters fixed) has a slight effect on V_{bus} for higher output loads when the output is operating in CCM, but does so at lower output loads when the output is in DCM. This is because more energy can be transferred from the dc bus capacitor to the output when the output inductor current is discontinuous rather than continuous, for the same amount of average output current.
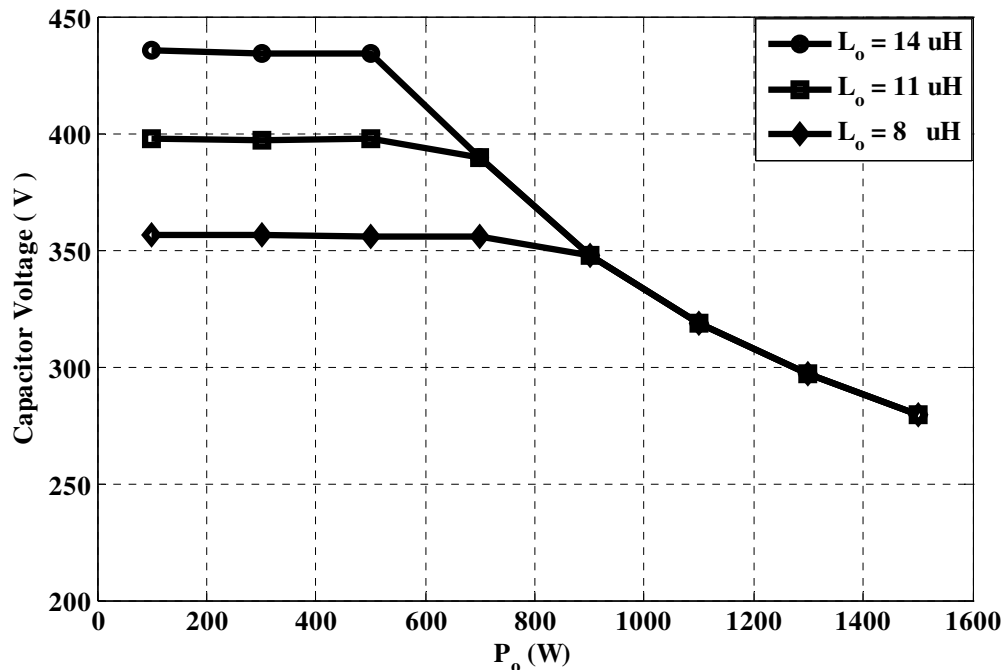
Fig.5.8. Effect of output inductor value L_o on dc bus voltage.
(V_{in}=208V_{rms}, Vo=48V, f_{sw}=50kHz)

B. *Effect of Input Inductor Value L_{in} on DC Bus Voltage V_{bus}*

It can be seen in Fig.5.9 that V_{bus} decreases as L_{in} is increased and all the other parameters are kept constant. Similar to what was stated above for the output inductor, less energy is transferred from the input to the dc bus when the inductor is larger and the current is more likely to approach the boundary of CCM and DCM.
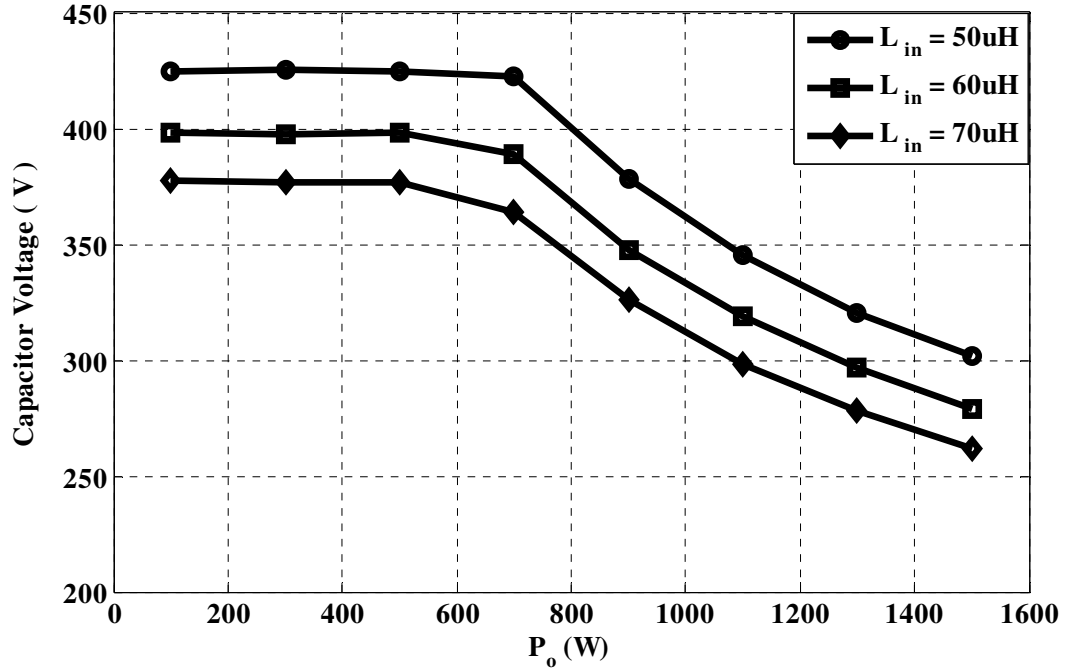
Fig.5.9. Effect of input Inductor value L_{in} on DC Bus Voltage
(V_{in}=208V_{rms}, Vo=48V, f_{sw}=50kHz)

C. *Effect of Transformer Turns Ratio N on DC Bus Voltage*

It can be seen in Fig.5.10 that V_{bus} decreases as the transformer turns ratio N is decreased. This is because as N is lowered, the transformer primary current, which is related to the current flowing out of the energy-storage capacitors, increases for the same amount of load current and so does the amount of energy that is pumped out of C_1 and C_2. If N is very low, then C_1 and C_2 may pump out so much energy that the energy equilibrium at capacitor will result in a very low dc bus voltage that will in turn force the converter to operate with an output voltage that will always be lower than the required

value, especially under heavy load conditions. Likewise, if N is very high, then C_1 and C_2 may pump out so little energy that that the energy equilibrium C_1 and C_2 will result in a very high dc bus voltage that will in turn force the converter to operate with an output voltage that will always be higher than the required value, especially under light load conditions.

Fig.5.10. Effect of transformer ratio value N on dc bus voltage
(V_{in}=208V_{rms}, Vo=48V, f_{sw}=50kHz)

D. Effect of input Voltage V_{in} on DC Bus Voltage V_{bus}

Fig.5.11 shows the effect of input voltage on dc bus voltage. As can be seen, increasing the input voltage increases the dc bus voltage. This is because more energy is pumped into the capacitors when the input voltage is at high line.
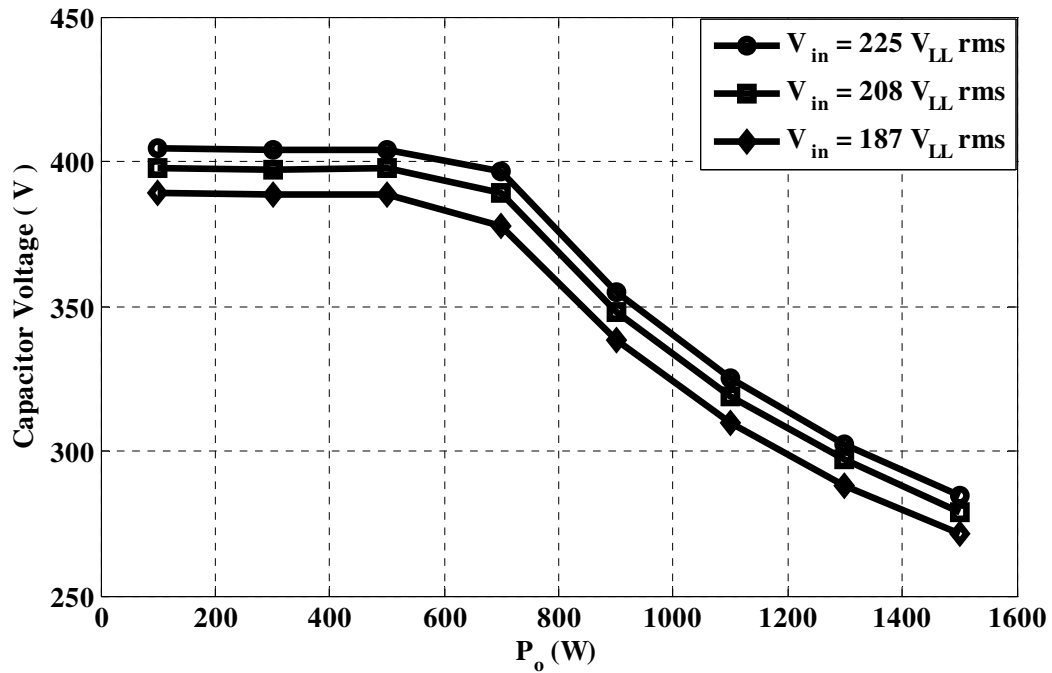
Fig.5.11. Effect of input voltage v_{in} on dc bus voltage
(V_{in}=208V_{rms}, Vo=48V, f_{sw}=50kHz)

5.2.3. Converter Design

A procedure for the design of the converter is presented in this section and is demonstrated with an example. The following criteria should be considered when trying to design the converter:

1) The energy-storage capacitor voltage V_{bus} should not be excessive. The value of V_{bus} should be kept below 800 V if possible so that the use of bulkier and more expensive capacitors can be avoided.

2) Excessive peak output and input currents should be avoided if possible.

3) The input line current must satisfy the necessary regulatory agency requirements of harmonic content such as IEC1000-3-2 Class A.

A design procedure for the selection of converter components based on the characteristic curves presented in the previous sections of this paper is given along with an example to illustrate how the converter can be designed. The converter is to be designed with the following parameters for the example:

Input voltage: $V_{in} = 208 \pm 10\%$ $V_{l\text{-}l, \text{rms}}$

Output voltage: $V_o = 48$ V

Maximum output power: $P_o = 1500$ W

Switching frequency: $f_{sw} = 1/T_{sw} = 50$ kHz

Maximum capacitor voltage: (for each capacitor) 400 V

Input current harmonics: EN61000-3-2 for Class A electrical equipment.

Step 1: Determine Value for Turns Ratio of Main Transformer N

Fig. 5.10 shows that the value of N affects the primary-side dc bus voltage. It determines how much reflected load current is available at the transformer primary to discharge the bus capacitors. If N is low, the primary current may be too high and thus more conduction losses. N should be high enough to reduce the circulating primary current, then the primary current that is available to discharge the dc-link capacitors may be low and thus V_{bus} may become excessive under certain operating conditions (i.e. high line). Equation (5.10) shows the relation between V_{bus}, D, V_o and N. The minimum value of N can be found by considering the case when the converter must operate with minimum input line and thus, minimum primary-side dc bus voltage $V_{bus,min}$ and maximum duty cycle D_{max}. If the converter can produce the required output voltage and can operate with discontinuous input and continuous output currents in this case, then it can do so for all cases.

$$N \geq \frac{V_{bus,min}}{2V_o} \cdot D_{max} \tag{5.19}$$

Finding the proper value of N can be done with a computer program. As described in Section III, V_{bus} is determined by the converter parameters for various values of L_{in} and with fixed values of N. it should be the highest value for which valid operating points exist for the two most extreme line and load conditions: high line, light load and low line, full load. N has been chosen to be 3 for given example.

With a value of N=3, $V_o = 48$, and $D_{max} = 0.75$ the actual value of V_{bus} can now be determined by using computer program which gives $V_{bus,min} = 384$ V.

Step 2: Determine Value for Input Inductor L_{in}

The value for L_{in} should be low enough to ensure that the input current is fully discontinuous under all operating conditions, but not so low as to result in excessively high peak currents. This can be done using the computer program with the following equations, which are based on the descriptions given in Section III .

For the case where L_{in} is such that the input current remains discontinuous for all operating conditions, then the average input power can be expressed as:

$$P_{in} = \frac{3}{\frac{\pi}{2}} * \left(\frac{1}{T_{su}} \int_0^{T_{su}} |v_{s,k}| i_{s,k} d_{w_k} t \right) = \frac{3}{\frac{\pi}{2}} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} |v_{s,k}| i_{s,k} \qquad (5.20)$$

where f_{su} is the input ac frequency and $f_{sn} = \frac{2 f_{sw}}{f_{su}}$ and

$$i_{s,k} = \frac{(D + \Delta_s)}{2} i_{L_{in,max}} = \frac{1}{4} \cdot \frac{D^2}{L_{in} \cdot f_{sw}} \cdot \frac{|v_{s,k}|}{1 - \frac{|v_{s,k}|}{V_{bus}}} \qquad (5.21)$$

By substituting the value of $i_{s,k}$ (21), P_{in} can be expressed as:

$$P_{in} = \frac{3}{\pi/2} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} |v_{s,k}| |i_{s,k}| \tag{5.22}$$

$$= \frac{3 \cdot D^2}{8 \cdot \pi/2 \cdot L_{in} \cdot f_{sw}} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \frac{|v_{s,k}|^2}{1 - \frac{|v_{s,k}|}{V_{bus}}}$$

By assuming the $P_{in} = P_o$, L_{in} can be achieved:

$$L_{in} = \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} |v_{s,k}| |i_{s,k}| \tag{5.23}$$

$$= \frac{D^2}{4 \cdot \pi \ P_o \cdot f_{sw}} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \frac{|v_{s,k}|^2}{1 - \frac{|v_{s,k}|}{V_{bus}}}$$

The worst-case to be considered is the case when the converter operates with minimum input voltage and maximum load since if the input current is discontinuous under these conditions, it will be discontinuous for all other operating conditions and thus an excellent power factor will be achieved. In this case, $V_{in} = 188$ $V_{phase,rms}$ and $V_{bus} = 384$ V as calculated in Step 1 are used to determine L_{in} at the boundary condition for the input section, and $D = D_{max} = 0.75$; assuming the converter to be lossless, $P_{in} = P_o = 1500$ W is used. The value of $L_{in} = 68$ µH is found from the computer program. For this design, $L_{in} = 65$ µH is used.

Step 3: Determine Value for Output Inductor L_o:

The output inductor can be designed in such a way that the output current to be in discontinuous (DCM) or continuous (CCM) or semi-continuous (SCCM) mode. Therefore, there are three options to design output inductor.

3. A) Output inductor for full output DCM

This method is a standard method that has been applied for many converters. The maximum value of L_o should be the value of L_o with which the converter's output current will be on the boundary between being continuous and discontinuous when the converter is operating with minimum input voltage, maximum duty cycle (D_{max}), and full load ($P_{o,max}$). If this condition is met, then the output current will be discontinuous for all other converter's operating conditions. The maximum value of L_o can therefore be determined to be

$$L_{o,max} = \frac{V_0^2}{P_{o,max}} \cdot \frac{(1 - D_{max})}{2} \cdot \frac{T_{sw}}{2} \qquad (5.24)$$

This results in a very high output ripple so that secondary diodes with high peak current ratings and large output capacitors to filter the ripple are needed.

3. B) Output inductor for full output CCM

For having CCM at output, the minimum value of L_o should be the value of L_o with which the converter's output current will be continuous on the when the converter is operating with maximum input voltage, minimum duty cycle (D_{min}), and minimum Load (10% of $P_{o,max}$). If this condition is met, then the output current will be continuous for all other converter's operating conditions. The minimum value of L_o can therefore be determined to be

$$L_{o,min} \geq \frac{V_0^2}{0.1 \cdot P_{o,max}} \cdot \frac{(1 - D_{min})}{2} \cdot \frac{T_{sw}}{2} \qquad (5.25)$$

This results in a low ripple at output and low peak current rating for secondary diodes and consequently lower output capacitor needs to filter the ripple. However, it has a major drawback. Bus voltage V_{bus} is dependent on the current that is flowing in and out of the bus capacitor, which is, in turn, dependent on the output inductor currents. When the

output current is CCM then the dc bus voltage is dependent on the load and it is not constant. This results that the high dc bus voltage at light load condition which needs to use high voltage dc bus capacitor and switches with higher rating. There are two solutions for this problem;

3.B.1) Dc Bus Voltage Control by Changing Auxiliary Winding Turns Ratio

The auxiliary winding turns ratio can be designed in a way that does not completely cancel out the voltage across the dc bus capacitor. This reduces the amount of voltage placed across the input inductor and thus reduces the amount of energy pumped into the input inductor. Consequently, the reduced energy in the input inductor affects the energy equilibrium of the dc bus capacitor and thus reduces the dc bus voltage.

Reducing the number of auxiliary winding turns introduces deadband regions in the zero-crossing sections of the input current waveform. This is because the diode-bridge diodes are reverse biased when the input voltage is low, and current is not allowed to flow in the input inductor as the dc bus voltage is not fully cancelled out by the auxiliary winding [28]. Therefore, there is a trade-off between the input pf and the dc bus voltage reduction. The auxiliary winding turns ratio should be selected to satisfy both the IEC1000-3-2 standards and reduce the dc bus voltage. For example, if choose N_{aux}= 1.7 instead of 2, the bus voltage decreases 50 Volt. Fig. 5.12 shows the variation of power factor versus variation of auxiliary winding turns ratio. (N_x= N_{aux} /2).
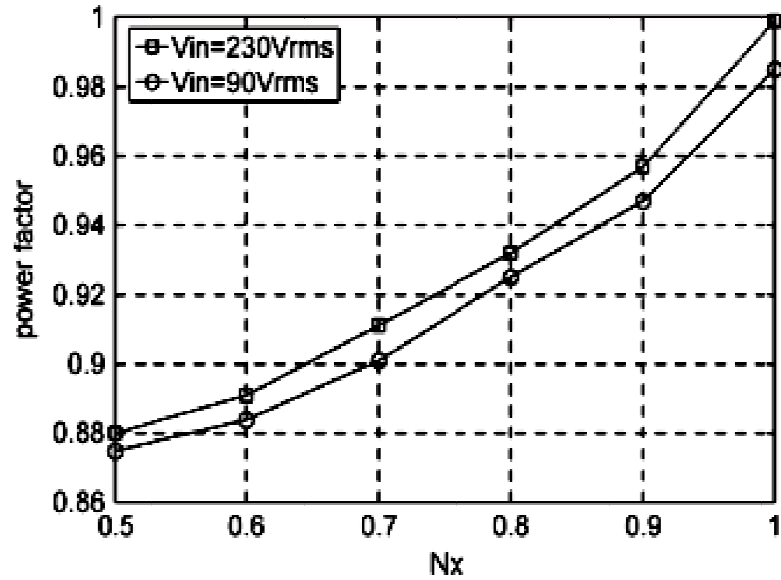
Fig.5.12. Variation of PF for different values of auxiliary winding turns ratio[28].

3. B.2) Output Inductor for Semi-CCM

This method is a compromising solution to have a continuous current at output for almost loads in one hand and preventing high dc bus voltage on the other hand. The output inductor should be designed so that the output current is made to be continuous under most operating conditions. The minimum value of L_o should be the value of L_o with which the converter's output current will be continuous on the when the converter is operating with maximum input voltage, minimum duty cycle (D_{min}), and at least 50% of maximum load. The minimum value of L_o can therefore be determined to be

$$L_{o,min} \geq \frac{V_0^2}{0.5 \ P_{o,max}} \cdot \frac{(1 - D_m)}{2} \cdot \frac{T_{sw}}{2} \tag{5.26}$$

In this paper, Semi-CCM mode for the output current is assumed. Substituting $P_{o,max} = 1500$ W, $V_o = 48$ V, $T_{sw} = 20$ μs, and $D_m = 0.5$ gives $L_{o,min} = 7$ μH and the value of L_o should be larger to provide some margin. The value of L_o should be larger to provide some margin. On the other hand, according to Fig. 5.3, the value of L_o cannot be too high as the dc bus voltage of the converter will become excessive; a value of $L_o = 11$ μH is chosen.

5.2.4. Experimental Results

An experimental prototype of the proposed converter was built to confirm its feasibility. The prototype was designed according to the following specifications:

Input voltage V_{in} = 208±10% Vrms (line-line),

Output voltage V_o = 48 V,

Output power P_o = 1.5kW,

Switching frequency f_{sw} = 50 kHz.

The main switches are FDL100N50F, and diodes are UF1006DICT. The input inductors are L_{abc} = L_{in} = 60 µH, the dc link capacitors are C_1, C_2 = 2200 µF, and the output inductor is L_o =11 µH. The auxiliary transformer ratio is 1:2 and the main transformer ratio is 3:1. Typical converter waveforms are shown in Fig. 5.13, 5.14 and 5.15 for different loads. It can be seen that the proposed converter can operate with no deadband regions, it is a multilevel full-bridge converter, that the switch stress is half the dc bus voltage, and that it can operate with a continuous output current, unlike most other converters of the same type. The lack of deadband regions in the input current waveforms is due to the greater flexibility that is allowed by the proposed converter's multilevel structure – there is less need to distort the input current to try to prevent the dc bus voltage from becoming excessive. It should be noted that, like other previously proposed converters with discontinuous input currents, the high input current ripple is a source of EMI.
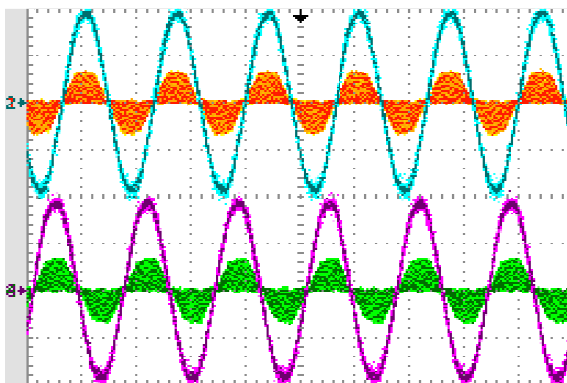
(a) Input current and voltage (for two phases) (V: 100 V/div, I: 15 A/div)
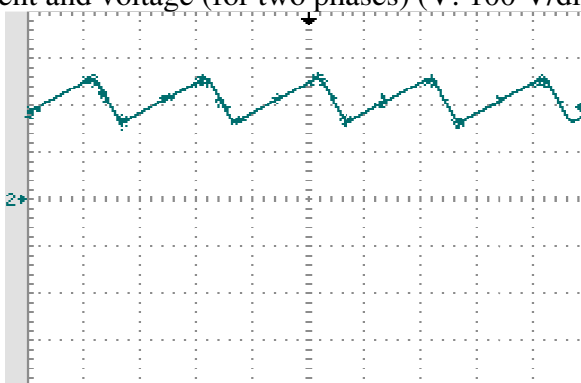
(b) Output inductor current (I:15A/div., t: 5 µs/div.)
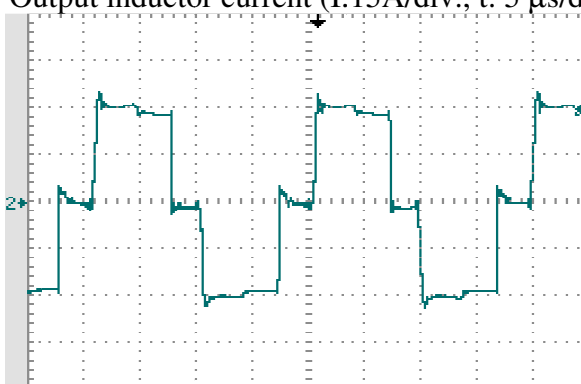
(c)Primary voltage of the main transformer (V: 150V/div., t: 5 µs/div.)
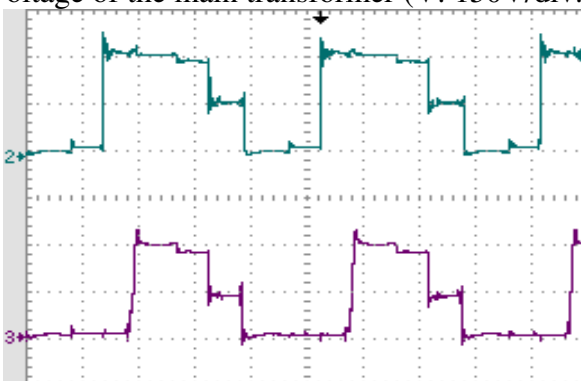
(d)Bottom switch voltages V_{ds4} and V_{ds3} (V: 150V/div., t: 5 µs/div.)

Fig.5.13. Experimental results.
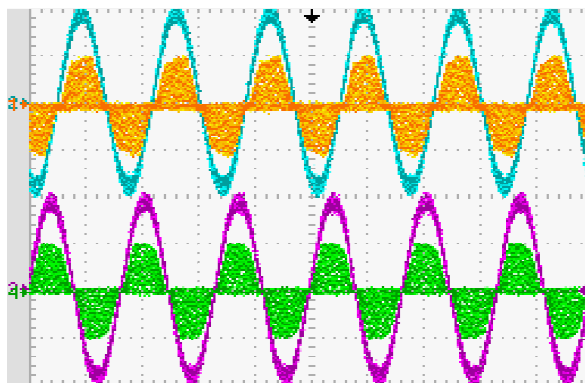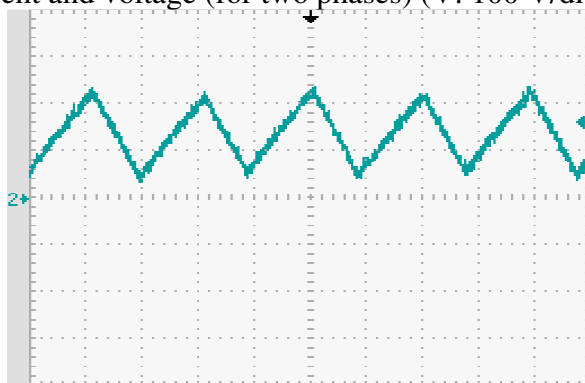
(a) Input current and voltage (for two phases) (V: 100 V/div, I: 10 A/div)

(b) Output inductor current (I:15A/div., t: 5 µs/div.)
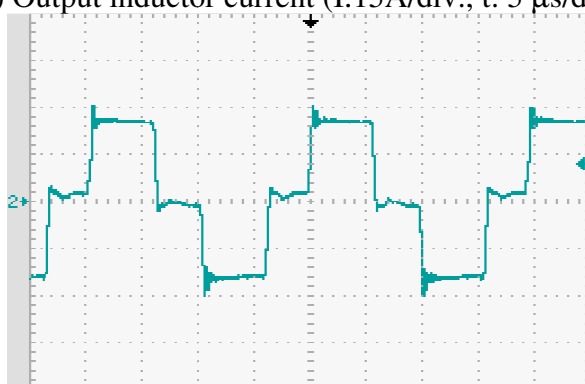
(c)Primary voltage of the main transformer (V: 200V/div., t: 5 µs/div.)
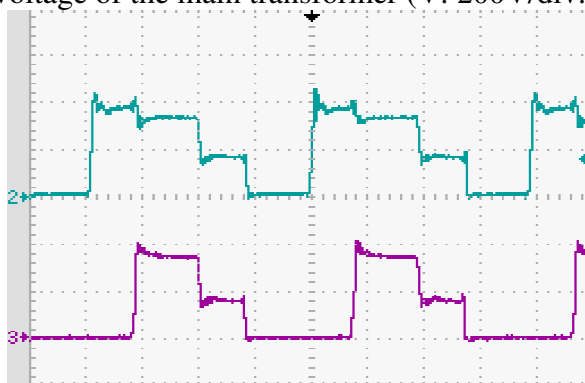
(d)Bottom switch voltages V_{ds4} and V_{ds3} (V: 200V/div., t: 5 µs/div.)

Fig.5.14. Experimental results for 50% of full load.
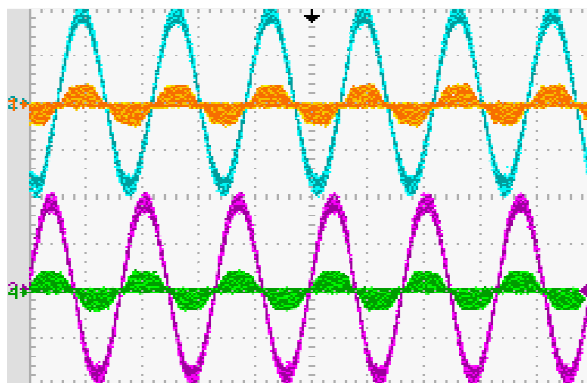
(a) Input current and voltage (for two phases) (V: 100 V/div, I: 10 A/div)
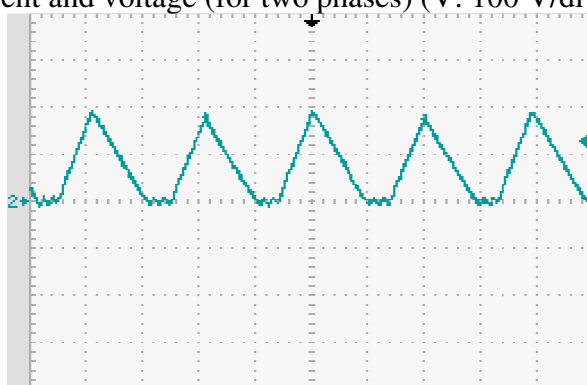
(b) Output inductor current (I:10A/div., t: 5 μs/div.)
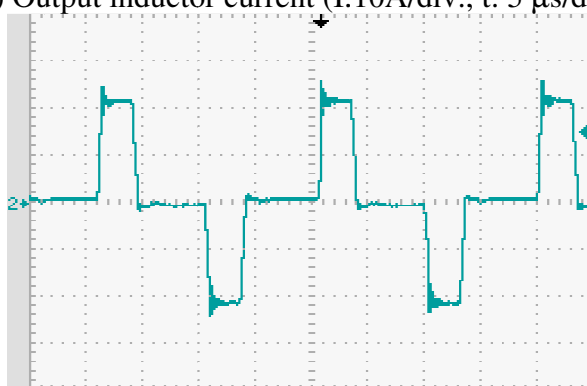
(c)Primary voltage of the main transformer (V: 200V/div., t: 5 μs/div.)
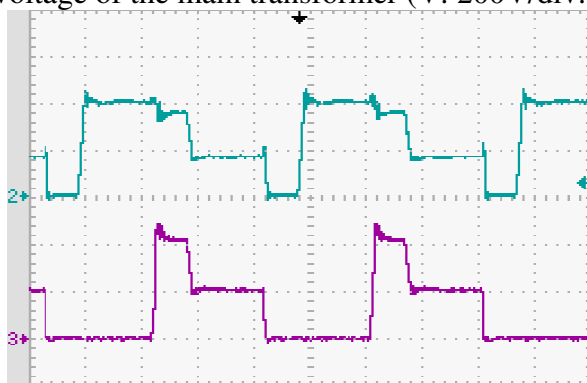
(d) Bottom switch voltages V_{ds4} and V_{ds3} (V: 200V/div., t: 5 μs/div.)

Fig.5.15. Experimental results for 25% of full load.
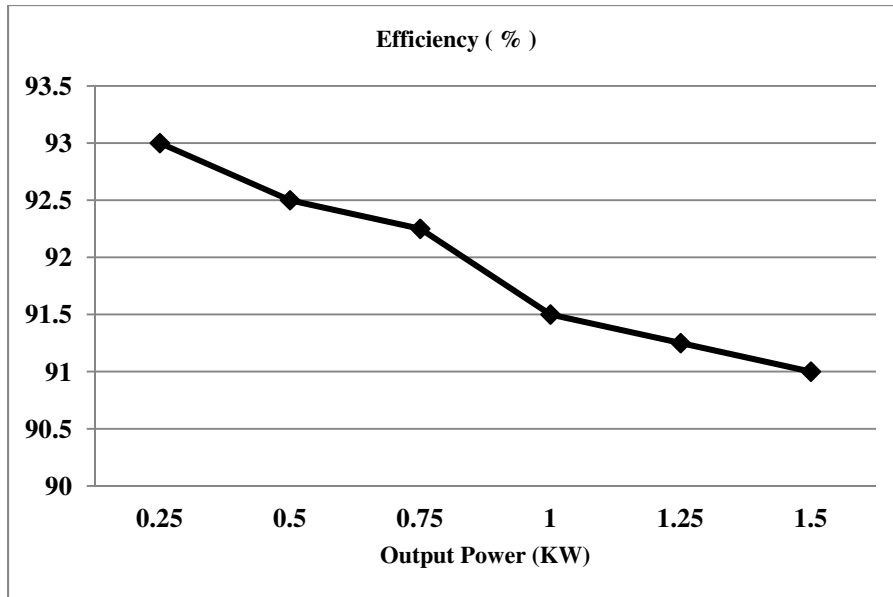
Efficiency (%)

Fig.5.16. Converter efficiency with input voltage $V_{LL\text{-}rms}$ = 220 V.

The efficiency measured from the converter at light load was about 93% and for full load was 91% as shown in Fig.5.16. In multilevel converters such as the proposed converter, the voltage stresses of their power switches are only half of the input voltage and not the full input voltage as is the case for two-level converters. This means that less energy is required to discharge the output capacitances of switch MOSFET devices and thus they can operate with fewer switching losses and a wider load range for ZVS than two-level converters.

Compared to other multilevel converters such as the ones proposed in [51] and [57], the proposed converter is simpler (in terms of topology and in capacitor voltage balancing), has better lighter load efficiency (since its switches are exposed to less voltage and thus it is easier to discharge switch capacitances during switch turn-on with less primary current), and can operate with less output inductor current ripple, even continuous output inductor current at heavier loads. In terms of THD, the proposed converter has low THD, less than 7%, which is similar to the converters in [51] and [57].

Fig. 5.17 and 5.18 show the input current harmonics a P_o =1500 W and P_o =750 W when P_o =1500 W when V_{in} = 220 $V_{l\text{-}lrms}$. It can be seen that the converter's harmonics are below the harmonic levels that are specified by the IEC 1000-3-2 standard.
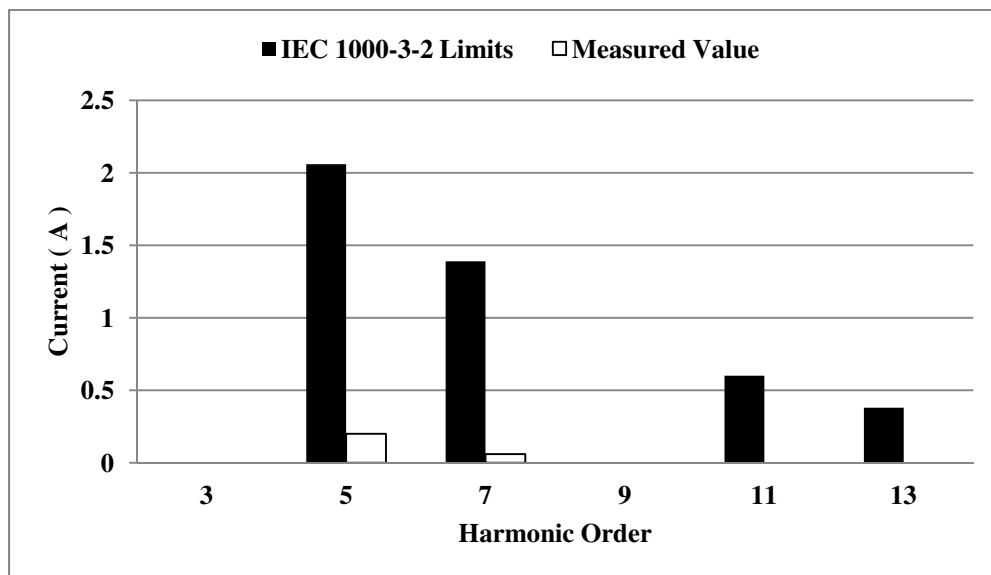
Fig.5.17. Input current harmonic at V_{in} = 220V_{rms}(l-l) , P_o=1.5 KW compared to IEC1000-3-2 Class A standard.
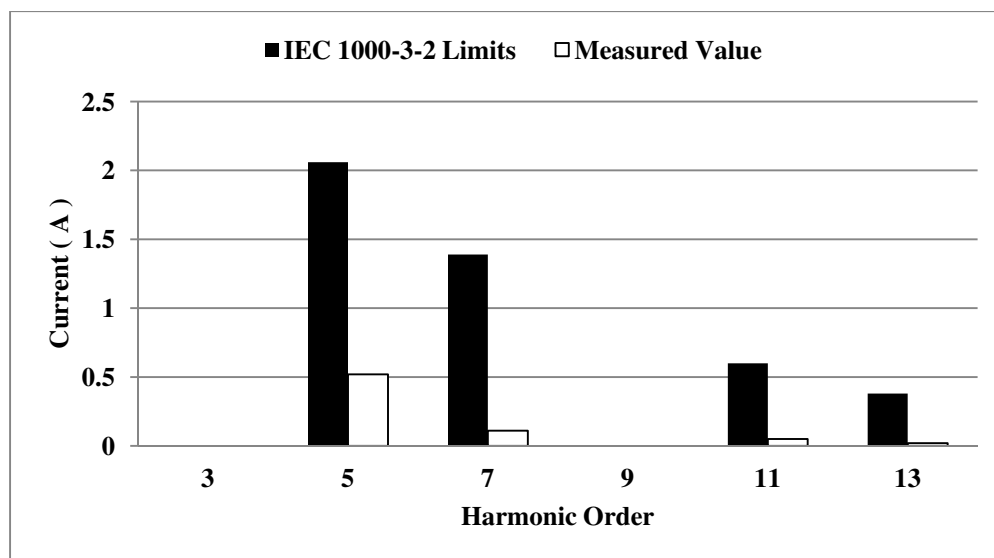
Fig.5.18. Input current harmonic at V_{in} = 220V_{rms}(l-l) , P_o=0.75 KW compared to IEC1000-3-2 Class A standard.

5.3. A New Interleaved Three-Phase Single-Stage Three-Level Power Factor Correction AC-DC Converter

Although the converter described in Section 5.2 represents a significant improvement over other previously proposed three-phase SSPFC converters, like these other converters, it has discontinuous input currents. These discontinuous currents have high current peaks that stress converter components and can introduce large high frequency ripple into the ac source unless filtered out by a large input filter. In order to minimize this high current ripple and reduce the size and cost of the input filter a new topology consisting of interleaved discontinuous conduction mode (DCM) three-phase three-level rectifiers is proposed, as shown in Fig. 5.19.
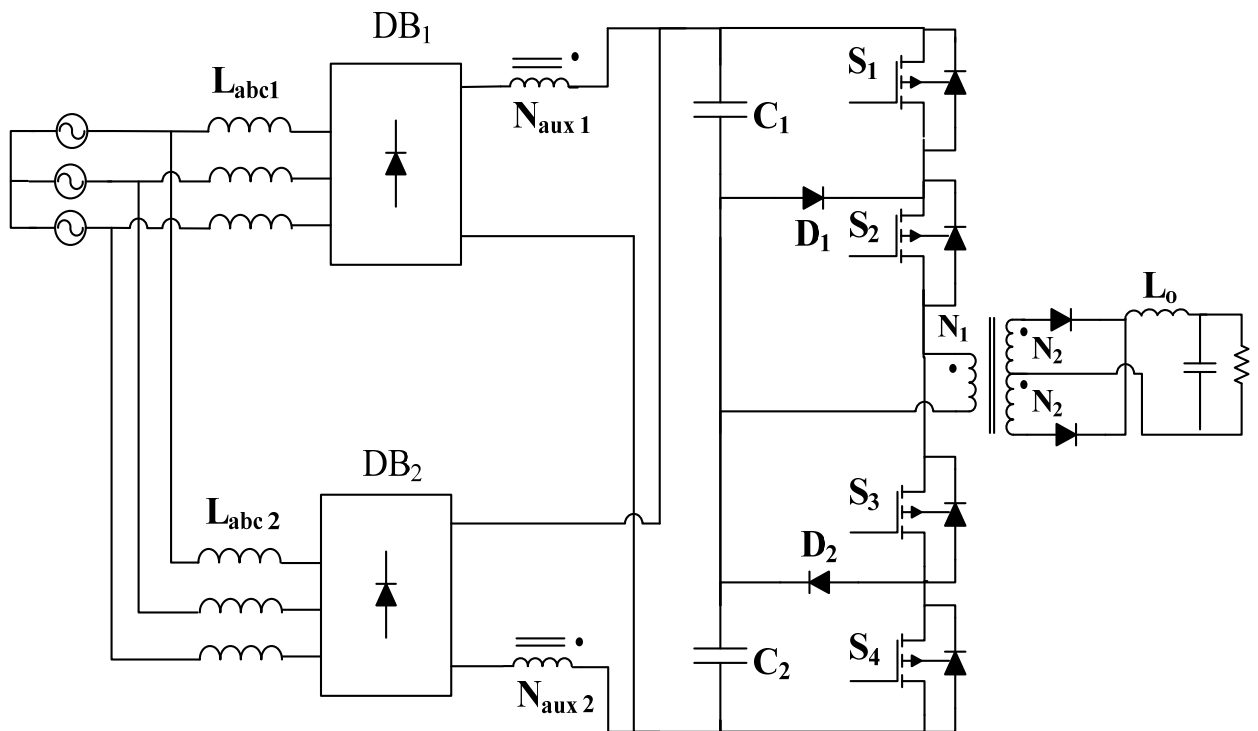
Fig.5.19. Proposed interleaved three-stage three-level converter

In comparison to the converter described in previous section, the proposed converter using interleaved structure does not need to have two high voltage diodes;

output current is continuous for all load ranges, dc bus voltage is less than 450 for all conditions and has much more lower harmonic content at ac side.

5.3.1. Converter Operation

The key waveforms of the proposed converter are the same as described for the converter in section 5.2 and it is shown in Fig.5.20.
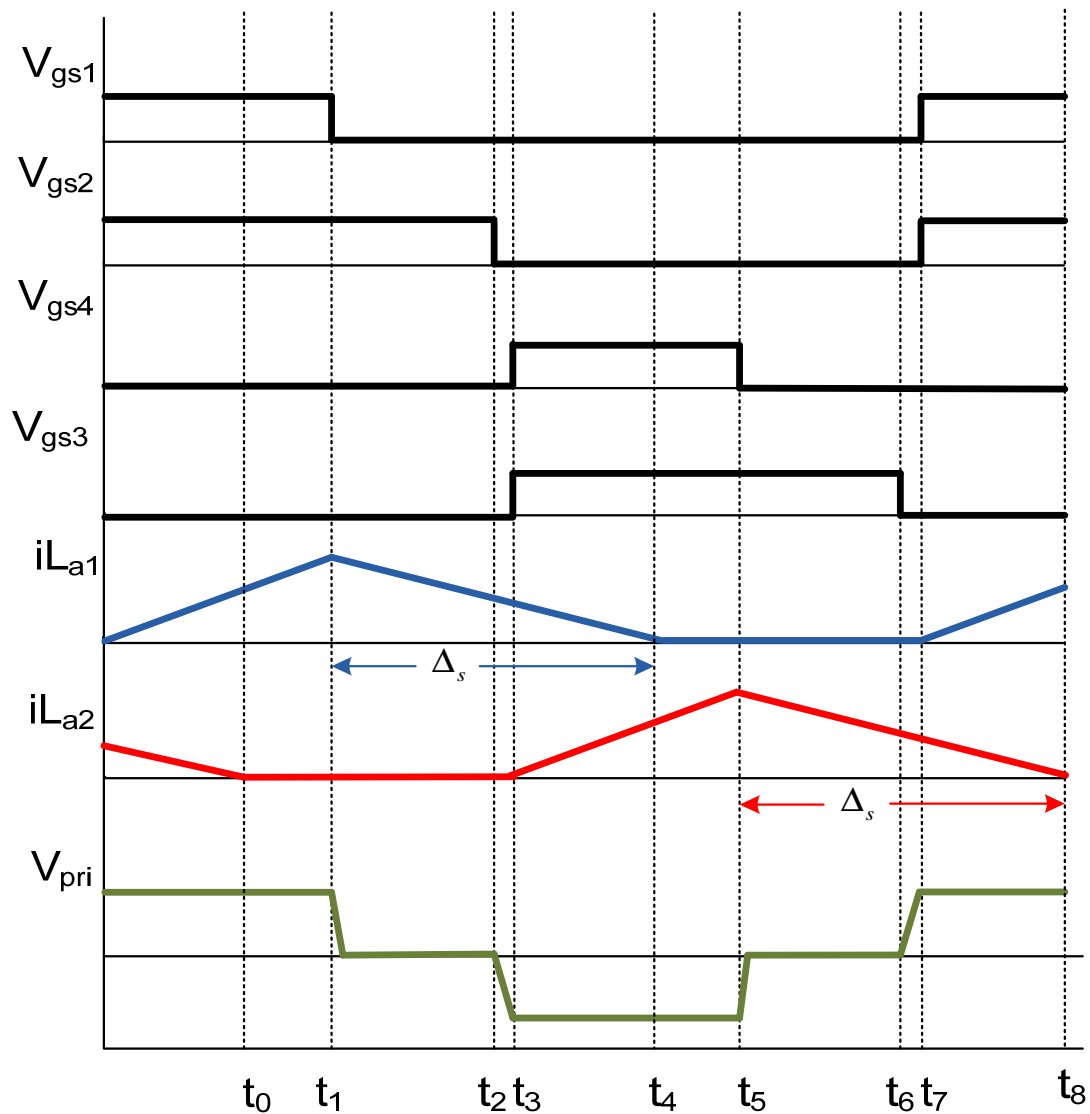
Fig. 5.20. Typical waveforms describing the modes of operation.

The proposed converter uses auxiliary windings that are taken from the converter transformer to act as "magnetic switches" to cancel the dc bus capacitor voltage so that the voltage that appears across the diode bridge output is zero. When the primary voltage of the main transformer is positive, Auxiliary Winding 1 cancels out the dc bus voltage so that the output voltage of Diode Bridge 1 (DB$_1$) is zero and the currents in input inductors L$_{a1}$, L$_{b1}$, and L$_{c1}$ rise. When the primary voltage of the main transformer is negative, Auxiliary Winding 2 cancels out the dc bus voltage so that the output voltage of Diode Bridge 2 (DB$_2$) is zero and the currents in input inductors L$_{a2}$, L$_{b2}$, and L$_{c2}$ rise. When there is no voltage across the main transformer primary winding, the total voltage across the dc bus capacitors appears at the output of the diode bridges and the input currents falls since this voltage is greater than the input voltage. The top two switches represent a converter that produces a discontinuous current in input inductors L$_{a1}$, L$_{b1}$ and L$_{c1}$, the bottom two switches represent a converter that produces a discontinuous current in input inductors L$_{a2}$, L$_{b2}$, L$_{c2}$, so that when the two current of the same phase are added up, then the current ripple is significantly reduced, if not cancelled altogether.

The converters modes of operation are explained in this section. To simplify the analysis, the following assumptions are made: (i) The input voltage value can be considered as constant within a switching period as the period of the three- phase voltage supply is much longer than the switching period. (ii) All devices are ideal. (iii) The currents in inductors $L_{a1} = L_{b1} = L_{c1} = L_{a2} = L_{b2} = L_{c2} = L_1 = L_2 = L$ are i_{La1}, i_{Lb1}, i_{Lc1}, i_{La2}, i_{Lb2}, and i_{Lc2}. (iv) The dc bus voltage has no ripple. (v) The turns ratio of auxiliary windings are N$_{aux1}$=N$_{aux2}$=N$_{aux}$. The equivalent circuit in each stage is shown in Fig. 3.21. The converter goes through the following modes of operation:

Mode 1 ($t_0 < t < t_1$) (Fig. 5.21):

During this interval, switches S$_1$ and S$_2$ are ON. The switches remain ON for a period given by $D/2f_{sw}$. In this mode, energy from dc bus capacitor C$_1$ flows to the output load. Due to magnetic coupling, a voltage appears across Auxiliary Winding 1that cancels the total dc bus capacitor voltage; the voltage at the diode bridge output is zero and the input currents in L$_{a1}$, L$_{b1}$, and L$_{c1}$ rise.
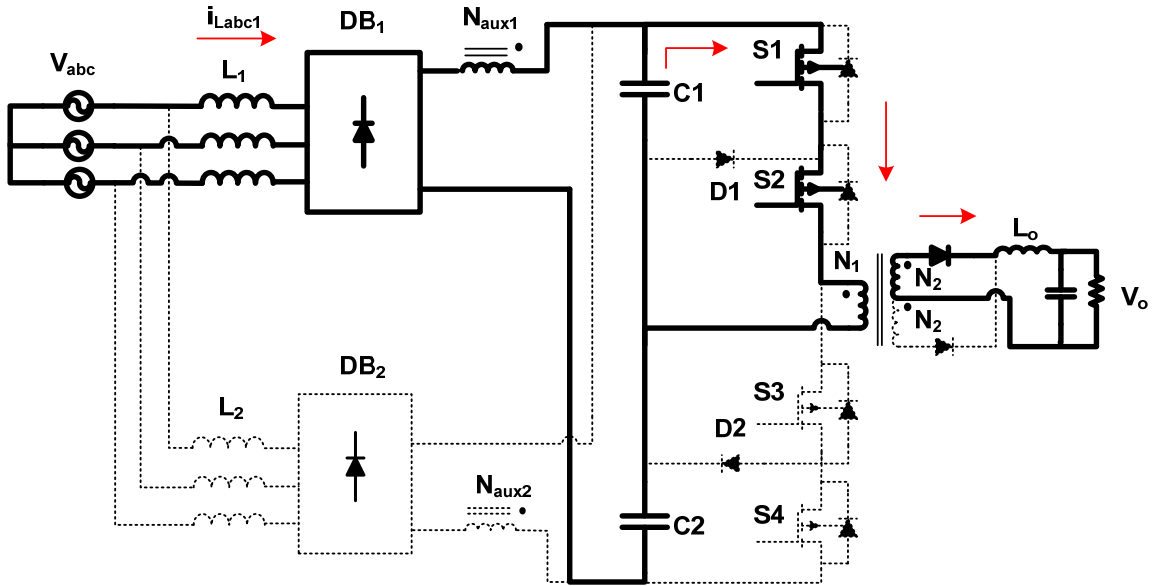
Fig.5.21. Mode 1 ($t_0 < t < t_1$)

Mode 2 ($t_1 < t < t_2$) (Fig. 5.22):

In this mode, S_1 is OFF and S_2 remains ON. The energy stored in L_1 during the previous mode starts to transfer into the dc bus capacitor. The primary current of the main transformer circulates through D_1 and S_2. With respect to the converter's output section, the load inductor current freewheels in the secondary of the transformer, which defines a voltage across the load filter inductor equal to $-V_L$.
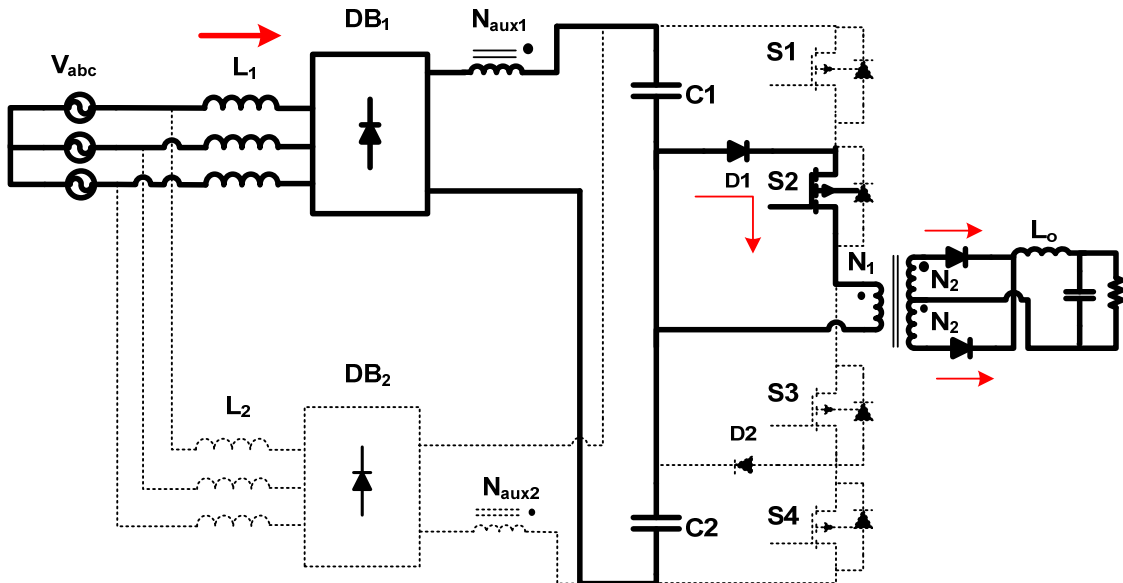
Fig. 5.22. Mode 2 ($t_1 < t < t_2$)

Mode 3 (t₂ < t < t₃) (Fig. 5.23):

In this mode, S_1 and S_2 are OFF. The energy stored in L_1 still is transferring into the dc bus capacitor. The primary current of the transformer charges C_2 through the body diodes of S_3 and S_4. Switches S_3 and S_4 are switched ON at the end of this mode.
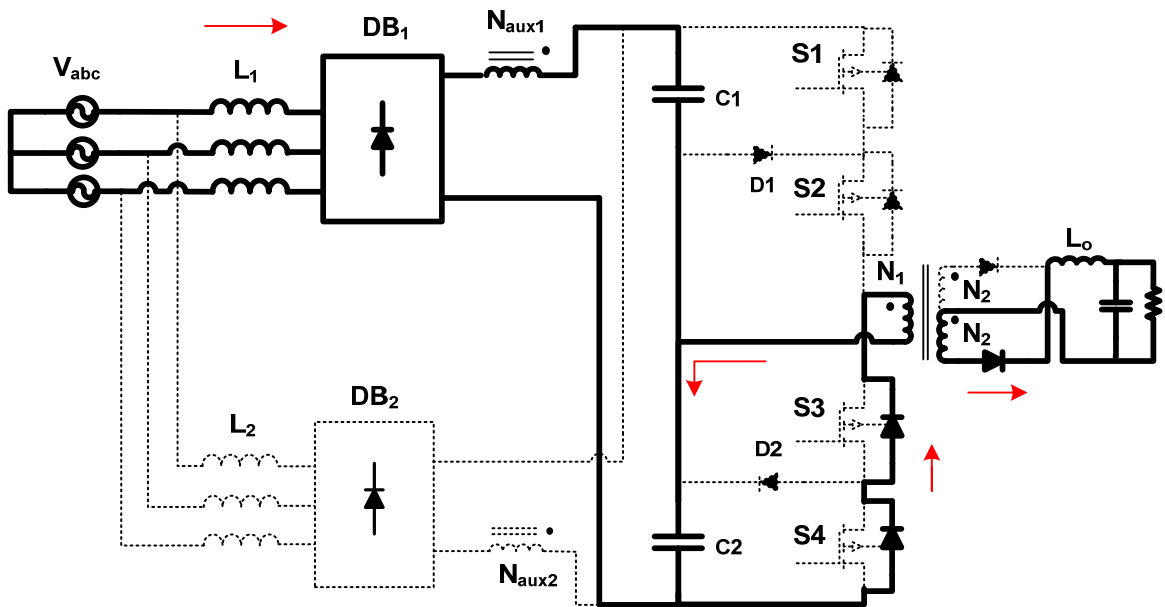
Fig.5.23. Mode 3 ($t_2 < t < t_3$)

Mode 4 (t₃ < t < t₄) (Fig. 5.24):

In this mode, S_3 and S_4 are ON and energy flows from the capacitor C_2 into the load. The magnetic switch cancels out the dc bus voltage and voltage across the auxiliary inductors L_2 becomes only the rectified supply voltage of each phase and the current flowing through each inductor increases. This mode ends when the energy stored in L_1 completely transfers into the dc bus capacitor. For the remainder of the switching cycle, the converter goes through Modes 1 to 4, but with S_3 and S_4 ON instead of S_1 and S_2 and DB_2 instead of DB_1.
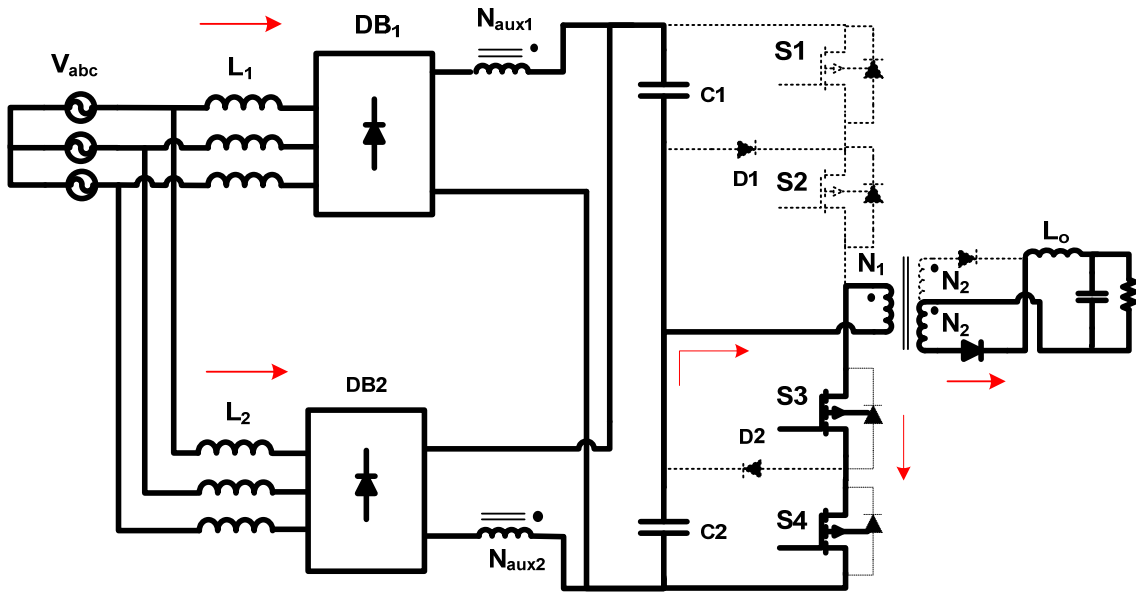
Fig.5.24. Mode 4 ($t_3 < t < t_4$)

Mode 5($t_4 < t < t_5$) (Fig. 5.25):

In this mode, S_3 and S_4 are ON and a symmetrical period begins. In this mode, energy flows from the capacitor C_2 into the load. The voltage across the auxiliary inductors L_2 becomes only the rectified supply voltage of each phase and the current flowing through each inductor increases.
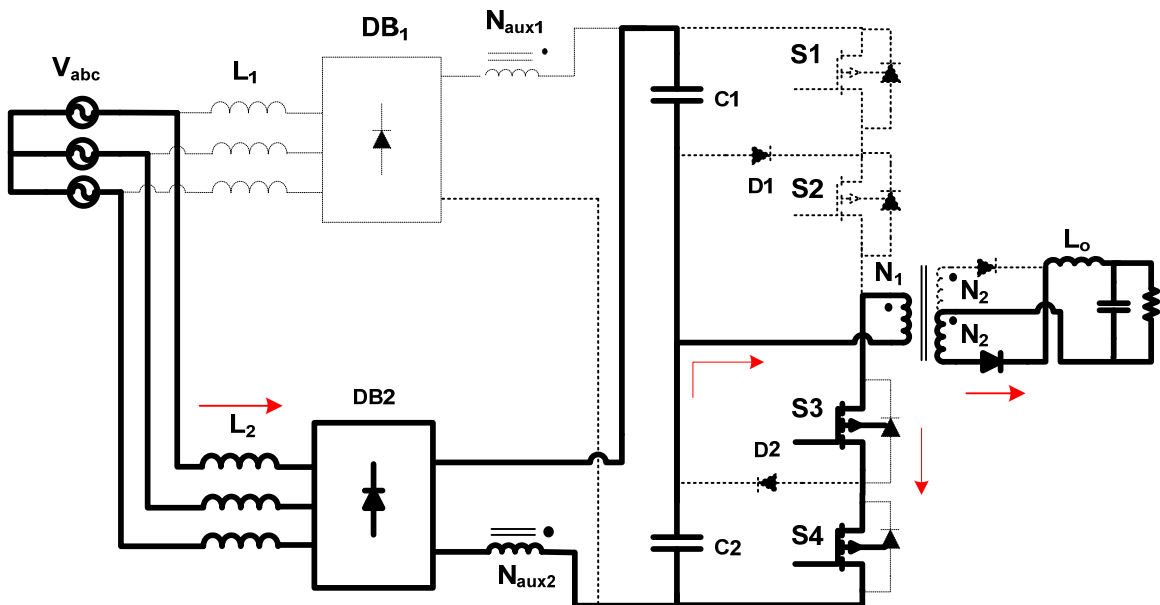
Fig.5.25. Mode 5 ($t_4 < t < t_5$)

Mode 6 (t₅ < t < t₆) (Fig. 5.26):

In this mode, S_3 is ON and S_4 is OFF and the primary current of the main transformer circulates through the diode D_2 and S_3. The energy stored in the auxiliary inductors L_2 during the previous mode starts transferring into the dc bus capacitor. The output inductor current also freewheels in the secondary of the transformer during this mode.
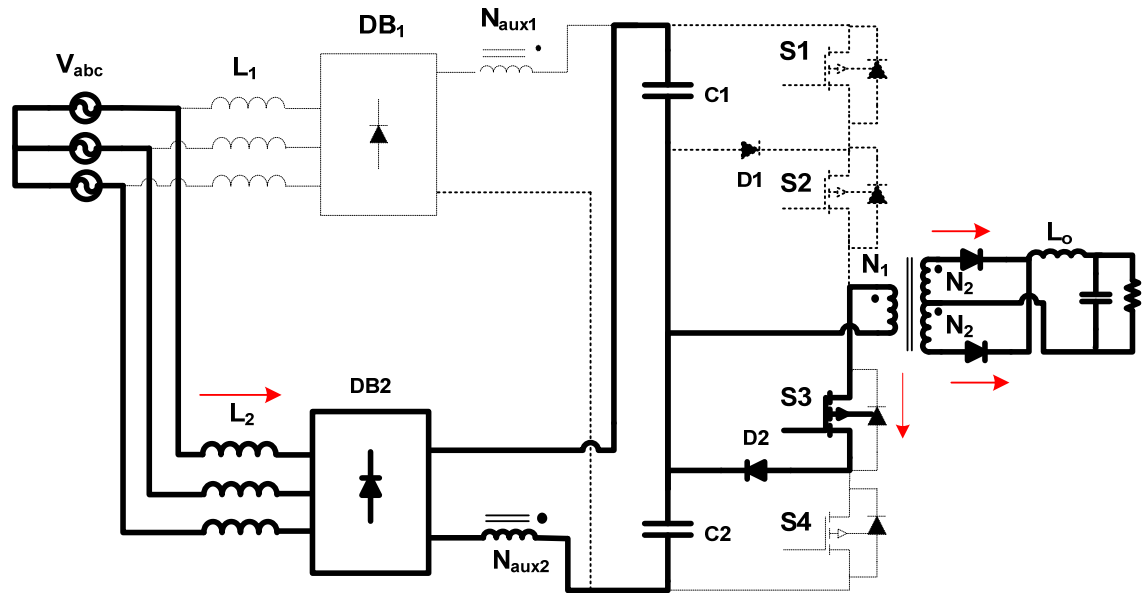
Fig.5.26. Mode 6 ($t_5 < t < t_6$)

Mode 7 (t₆ < t < t₇) (Fig. 5.27):

In this mode, S_3 and S_4 are OFF and the primary current of the transformer charges the capacitor C_1 through the body diodes of S_1 and S_2. The energy stored in the auxiliary inductors L_2 transfers into the dc bus capacitor.

Mode 8 (t₇ < t < t₈) (Fig. 5.28):

In this mode, S_1 and S_2 are ON. In this mode, energy from dc bus capacitor C_1 flows to the output load. This mode ends when energy in inductors L_2 completely transfer into the dc bus. Time t_8 is the end of the switching cycle and another switching cycle begins with the same modes.
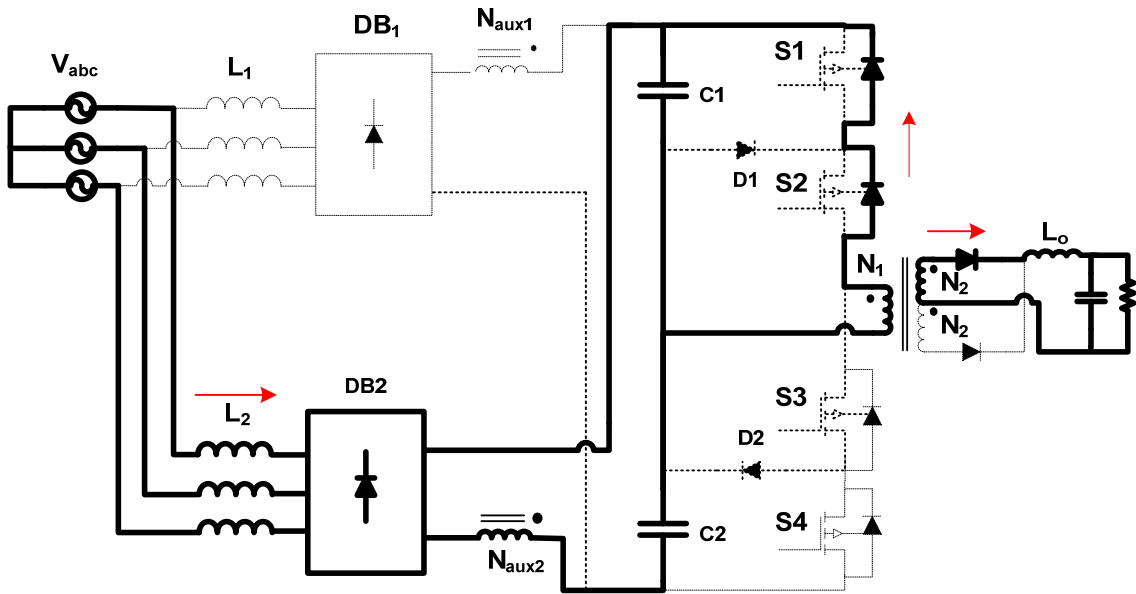
Fig.5.27. Mode 7 ($t_6 < t < t_7$)
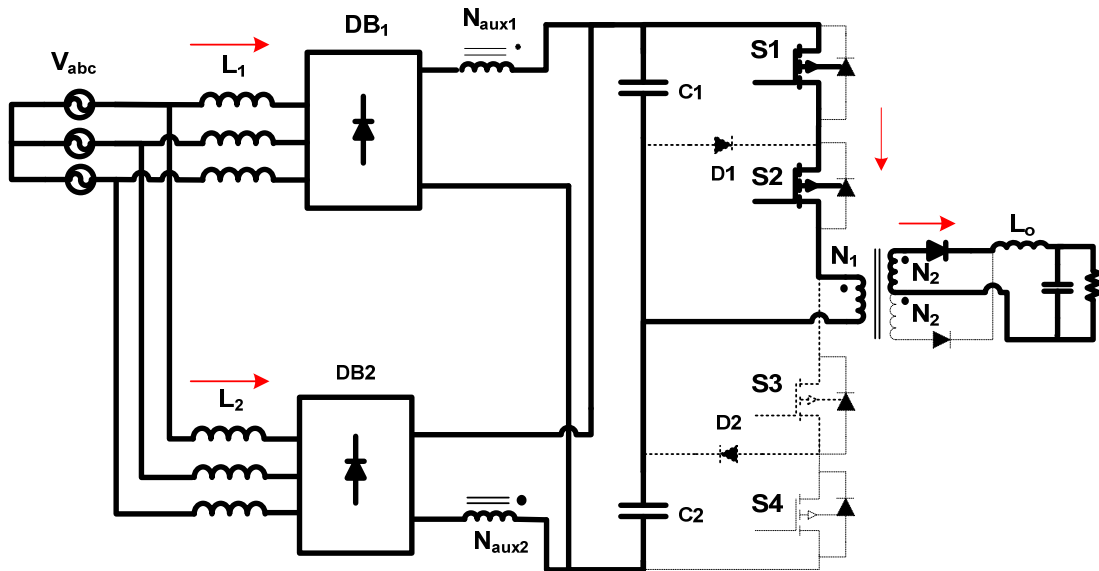
Fig.5.28. Mode 8 ($t_7 < t < t_8$)

It should be noted that input current is summation of inductor currents i_{L1} and i_{L2} which are both discontinuous. However, by selecting appropriate values for L_1 (= L_{a1} = L_{b1} = L_{c1}) and L_2 (= L_{a2} = L_{b2} = L_{c2}) in such a way that two inductor currents such as i_{La1}

and i_{La2} have to overlap each other, the input current can be made continuous as shown in Fig. 5.29; thus reducing the size of input filter significantly. There is a naturally 180° phase difference between the currents in L_1 and the currents in L_2 as one set of currents rises when the transformer primary is impressed with a positive voltage and the other set rises when the transformer primary is impressed with a negative voltage – these two events occur 180° apart during a switching cycle.

$$i_{La} = i_{La1} + i_{La2}$$

i_{La1} i_{La2}
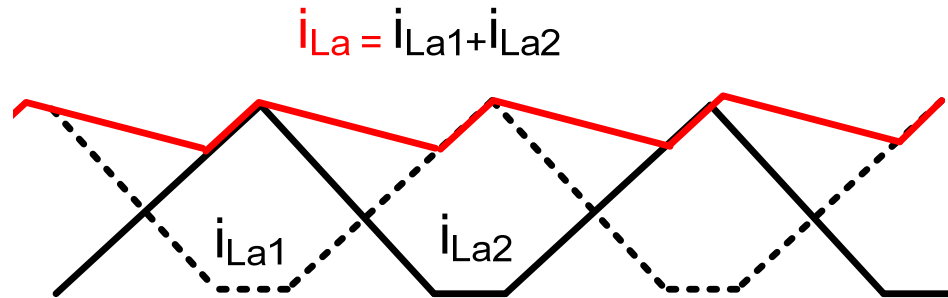
Fig.5.29. Interleaving between two input inductor currents.

5.3.2. Converter Characteristics

The procedure discussed in Section 5.2.2 can be repeated to determine V_{bus} (or any other parameter) for other operating points, in order for curves to be generated for analysis and design purposes. The converter operating characteristics for any given input and output voltage are dependent on three key parameters: transformer turns ratio N, input inductances $L_{1,2}$ and output L_o. In this section, the effect of each of these parameters is examined with graphs of characteristic curves that have been generated with a computer program.

A. Effect of Output Inductor Value L_o on dc Bus Voltage V_{bus}

It can be seen from Fig.5.30 (a) that varying L_o (but keeping all the other parameters fixed) has a slight effect on V_{bus} for higher output loads when the output is operating in CCM, but does so at lower output loads when the output is in DCM. This is because more energy can be transferred from the dc bus capacitor to the output when the

output inductor current is discontinuous rather than continuous, for the same amount of average output current.

B. Effect of Input Inductor Value L_{in} on dc Bus Voltage V_{bus}

It can be seen in Fig.5.30 (b) that V_{bus} decreases as L_{in} is increased and all the other parameters are kept constant. Similar to what was stated above for the output inductor, less energy is transferred from the input to the dc bus when the inductor is larger and the current is more likely to approach the boundary of CCM and DCM.

C. Effect of Transformer Turns Ratio N on dc Bus Voltage

It can be seen in Fig. 5.30 (c) that V_{bus} decreases as the transformer turns ratio N is decreased. This is because as N is lowered, the transformer primary current, which is related to the current flowing out of the energy-storage capacitors, increases for the same amount of load current and so does the amount of energy that is pumped out of C_1 and C_2. If N is very low, then C_1 and C_2 may pump out so much energy that the energy equilibrium at capacitor will result in a very low dc bus voltage that will in turn force the converter to operate with an output voltage that will always be lower than the required value, especially under heavy load conditions. Likewise, if N is very high, then C_1 and C_2 may pump out so little energy that that the energy equilibrium C_1 and C_2 will result in a very high dc bus voltage that will in turn force the converter to operate with an output voltage that will always be higher than the required value, especially under light load conditions.

D. Effect of input Voltage V_{in} on DC Bus Voltage

Fig. 5.23 (d) shows the effect of input voltage on dc bus voltage. As can be seen, increasing the input voltage increases the dc bus voltage. This is because more energy is pumped into the capacitors when the input voltage is at high line.
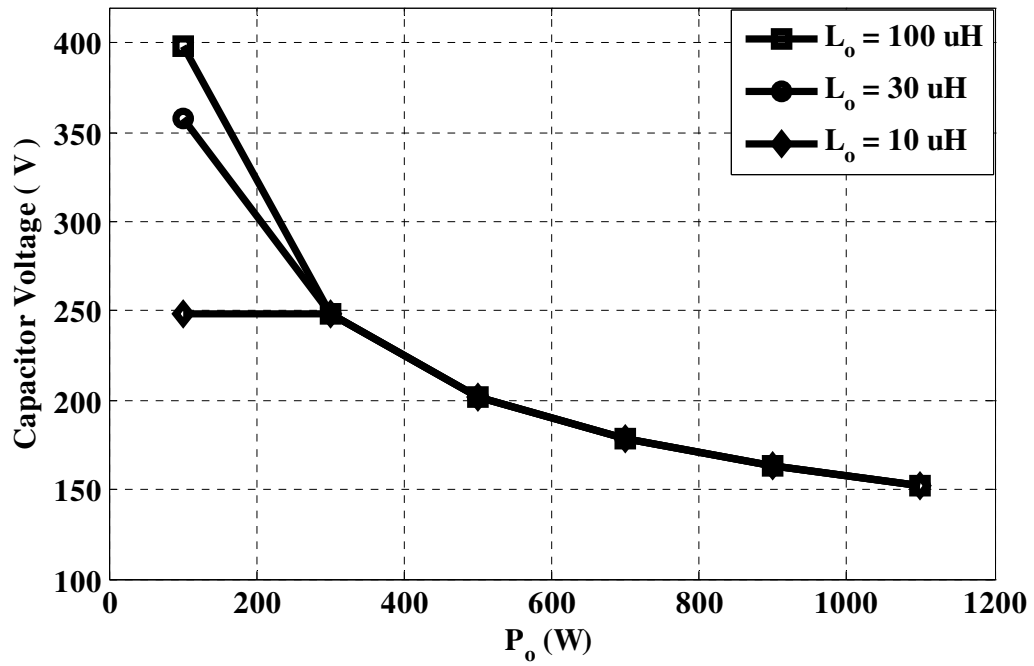
(a) Effect of output inductor value L_o on dc bus voltage
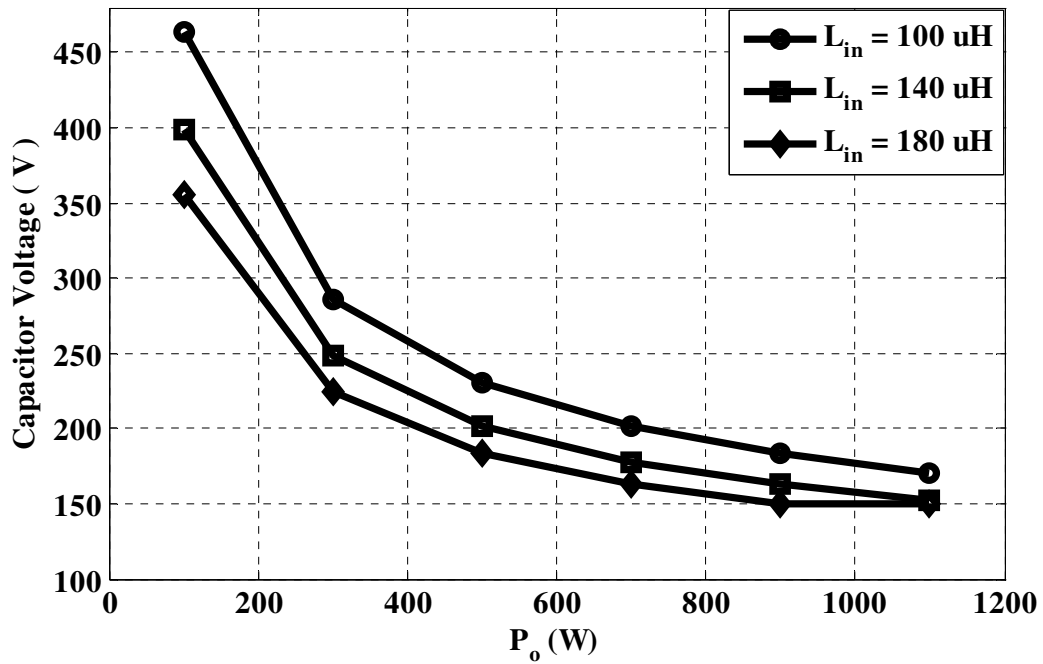
(b) Effect of input Inductor value L_{in} on dc Bus Voltag
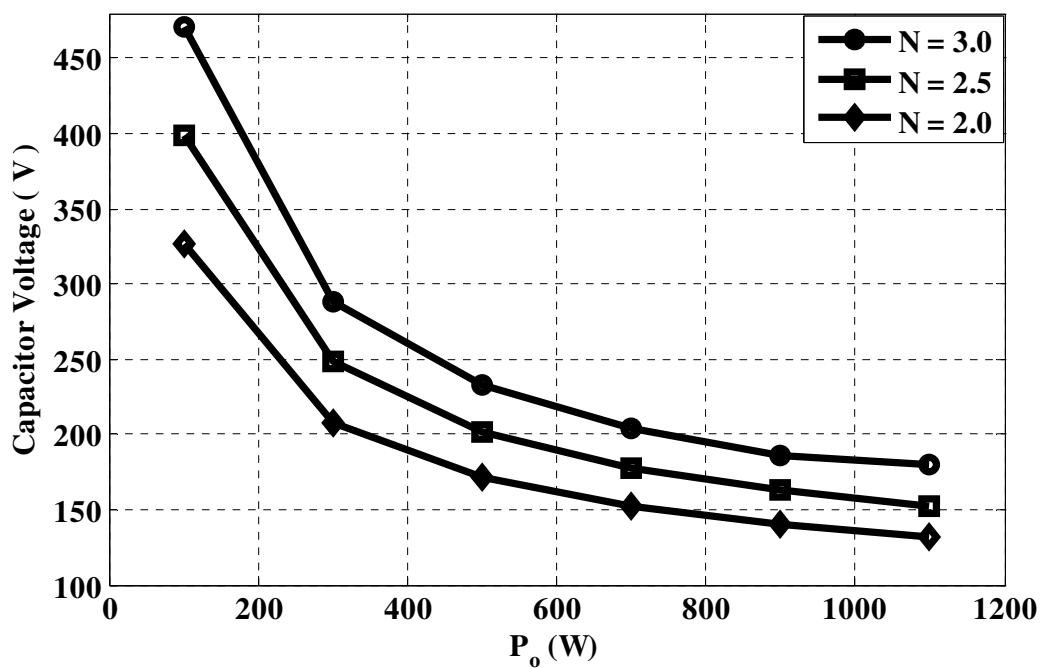
(c) Effect of transformer ratio value N on dc bus voltage
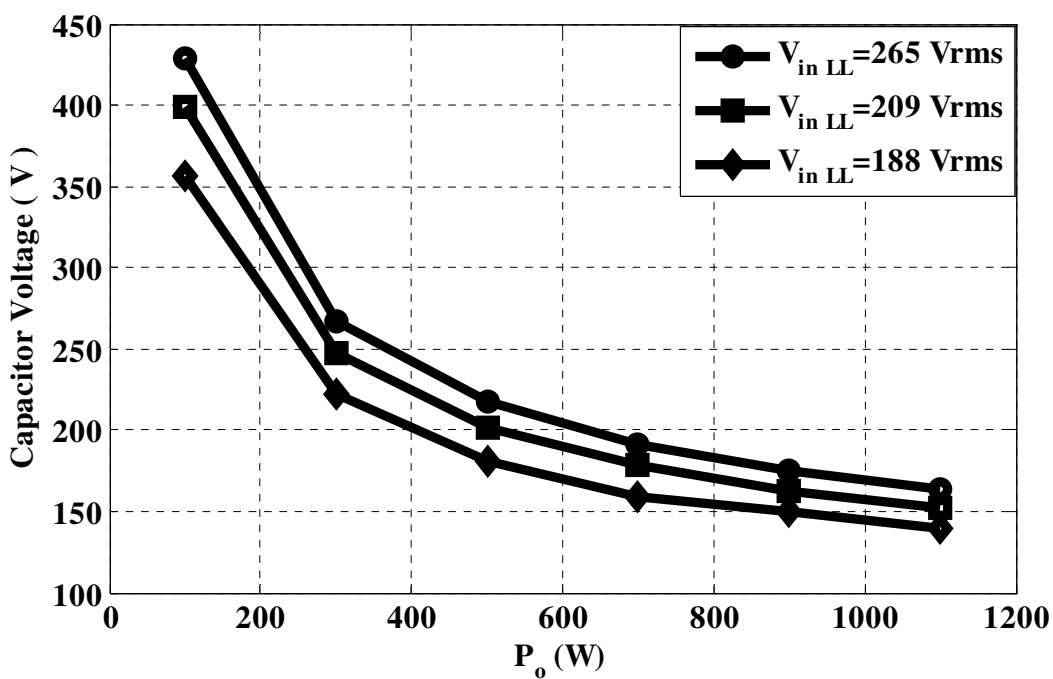
d. Effect of input voltage v_{in} on dc bus voltage

Fig.5.30. Steady-state characteristic curves (V_{in}=208V_{rms}, Vo=48V, f_{sw}=100kHz).

5.3.3. Converter Design

A procedure for the design of the converter is presented in this section and is demonstrated with an example. The following criteria should be considered when trying to design the converter:

i.   The energy-storage capacitor voltage V_{bus} should not be excessive. The value of V_{bus} should be kept to below 800 V if possible so that the use of bulkier, more expensive capacitors can be avoided.

ii.   Excessive peak output and input currents should be avoided.

iii.   The input line current must satisfy the necessary regulatory agency requirements of harmonic content such as IEC1000-3-2 Class A.

A design procedure for the selection of converter components based on the characteristic curves presented in the previous sections of this paper is given along with an example to illustrate how the converter can be designed. The converter is to be designed with the following parameters for the example:

> Input voltage: $V_{in} = 208\pm 10\%$ $V_{l-l,\ rms}$
> Output voltage: $V_o = 48$ V
> Maximum output power: $P_o = 1100$ W
> Switching frequency: $f_{sw} = 1/T_{sw} = 100$ kHz
> Maximum capacitor voltage: (for each capacitor) 400 V
> Input current harmonics: EN61000-3-2 for Class A electrical equipment.

Step1: Determine Value for Turns Ratio of Main Transformer N

N is an important parameter as it affects the amount of reflected load current that is available at the transformer primary to discharge the bus capacitors. Fig. 5.30(c) is an example of how the value of N affects the primary-side dc bus voltage. If N is very high,

then there is little reflected load current available to discharge the bus capacitors, which can result in an extremely high dc bus voltage. If N is low, then the primary current may be very high as there will be a high amount of current circulating in the transformer primary, which will create significant conduction losses. A trade-off between high values of N and low values of N, therefore, must be considered when selecting a value of N.

Selecting a value of N, however, cannot be done with a simple equation and must be done using some other method. One way of doing so is to use the computer program described in the previous section of this paper to examine a wide range of potentially valid combinations of L_o and L_{in} – combinations that allow the converter to work for the two most extreme line and load conditions: high line, light load and low line, full load. For this particular design example, numerous graphs of characteristic curves for different values of N were generated by the authors (not shown here due to space) and based on these graphs, a value of N = 2.5 is selected as an appropriate value.

The relation between V_{bus}, D, V_o and N is similar to (5.12). For the check, the operation of the converter at minimum input line when it operates with minimum primary-side dc bus voltage $V_{bus,min}$ and maximum duty cycle D_{max} should be considered. If the converter can produce the required output voltage and can operate with discontinuous input and continuous output currents in this case, then it can do so for all cases. Substituting $V_{bus,min}$ and maximum duty cycle D_{max} into equation (5.12) gives

$$V_{bus,min} = \frac{2V_o}{D_{max}} \cdot N \tag{5.27}$$

Substituting V_o = 48, N = 2.5, and D_{max} = 0.8 (0.8 has been selected as a conservative D_{max} to provide some margin) gives

$$V_{bus,min} = \frac{2(48)}{0.8} \cdot (2.5) = 300\ V \tag{5.28}$$

It should be noted that the dc bus voltage has not been determined yet. All that has been determined thus far is a value of N that can operate with an acceptable duty cycle for an acceptable minimum dc bus voltage.

Step2: Determine Value for Output Inductor L_o

For having CCM at output, the minimum value of L_o should be the value of L_o with which the converter's output current will be continuous on the when the converter is operating with maximum input voltage, minimum duty cycle (D_{min}), and minimum Load (10% of $P_{o,max}$). If this condition is met, then the output current will be continuous for all other converter's operating conditions. The minimum value of L_o can therefore be determined to be

$$L_{o,min} \geq \frac{V_0^2}{0.1 \cdot P_{o,max}} \cdot \frac{(1 - D_{min})}{2} \cdot \frac{T_{sw}}{2} \qquad (5.29)$$

This results in a low ripple at output and low peak current rating for secondary diodes and consequently lower output capacitor needs to filter the ripple. Substituting V_o = 48, $P_{o,max} = 1100\ W$, $D_{min} = 0.1$ and f_{sw}=100Khz, therefore the value of L_o should be larger than 47 µH. In this case L_o=100 µH is chosen to have less ripple at output and decrease the output capacitance filter.

Step 3: Determine Value for Input Inductor L_{in}

The value for L_1 and L_2 should be low enough to ensure that their currents are fully discontinuous under all operating conditions, but not so low as to result in excessively high peak currents. This can be done using the computer program with the following equations, which are based on the descriptions given in Section III . For the case where $L_1 = L_2 =L$ are such that the i_{L1} and i_{L2} remain discontinuous for all operating conditions, then the average input power can be expressed as;

$$P_{in} = \frac{3}{\frac{\pi}{2}} * \left(\frac{1}{T_{su}} \int_0^{T_{su}} |v_{s,k}| i_{s,k} d_{w_k}\, t \right) = \frac{3}{\frac{\pi}{2}} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} |v_{s,k}| i_{s,k} \qquad (5.30)$$

where f_{su} is the input ac frequency and $f_{sn} = \frac{2 f_{sw}}{f_{su}}$ and

$$i_{s,k} = \frac{(D + \Delta_s)}{2} i_{L_{in,max}} = \frac{1}{4} \cdot \frac{D^2}{L_{in} \cdot f_{sw}} \cdot \frac{|v_{s,k}|}{1 - \frac{|v_{s,k}|}{V_{bus}}} \qquad (5.31)$$

By substituting the value of $i_{s,k}$ (5.31), P_{in} can be expressed as:

$$P_{in} = \frac{3}{\pi/2} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} |v_{s,k}| i_{s,k} = \frac{3 \cdot D^2}{8 \cdot \pi/2 \cdot L_{in} \cdot f_{sw}} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \frac{|v_{s,k}|^2}{1 - \frac{|v_{s,k}|}{V_{bus}}} \qquad (5.32)$$

By assuming the $P_{in} = P_o$, L_{in} can be achieved:

$$L_{in} = \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} |v_{s,k}| i_{s,k} = \frac{D^2}{4 \cdot \pi \cdot P_o \cdot f_{sw}} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \frac{|v_{s,k}|^2}{1 - \frac{|v_{s,k}|}{V_{bus}}} \qquad (5.33)$$

The worst-case to be considered is the case when the converter operates with minimum input voltage and maximum load since if the input current is discontinuous under these conditions, it will be discontinuous for all other operating conditions and thus an excellent power factor will be achieved. In this case, $V_{in} = 188$ $V_{phase,rms}$ and $V_{bus} = 300$ V as calculated in Step 2 are used to determine L_{in} at the boundary condition for the input section, and $D = D_{max} = 0.8$; assuming the converter to be lossless, $P_{in} = P_o = 1100$ W is used. The value of $L_{in} = 180$ μH is found from the computer program. For this design, $L = 140$ μH is used.

5.3.4. Experimental Results and Converter Analysis

An experimental prototype of the proposed converter was built to confirm its feasibility. The prototype was designed according to the following specifications:

Input voltage V_{in} = 208±10% Vrms (line-line),

Output voltage V_o = 48 V,

Output power P_o = 1.1KW,

Switching frequency f_{sw} = 100 kHz.

Typical converter waveforms are shown in Fig. 5.31. It can be seen that the proposed converter can operate with nearly sinusoidal input currents with no deadband regions that it is a multilevel full-bridge converter, that the switch stress is half the dc bus voltage, and that it can operate with a continuous output current, unlike most other converters of the same type.

Experimental results obtained for the proposed converter are compared to the converter proposed in Section 5.2 with same specifications as shown in Tables I and II. The previous converter is a non-interleaved version of the proposed converter with just one set of input inductors instead of two. The output inductor current for the previous converter was designed to be continuous for heavy loads and discontinuous for light loads to keep the dc bus voltage less than 450V. The proposed converter while keeping the same advantages of that converter has continuous current at the output for 10% of full load to full load which makes the output current have less ripple. This is because, the proposed converter has a quite large inductor at the input and therefore the dc bus is small enough that permits to the output inductor to be large enough. It should be noted that no additional input filtering was used for the proposed interleaved converter and the input current waveform shown in Fig. 5.31 (c) is just the summation of an input phase current of Diode Bridge 1 and the corresponding phase current of Diode Bridge 2.
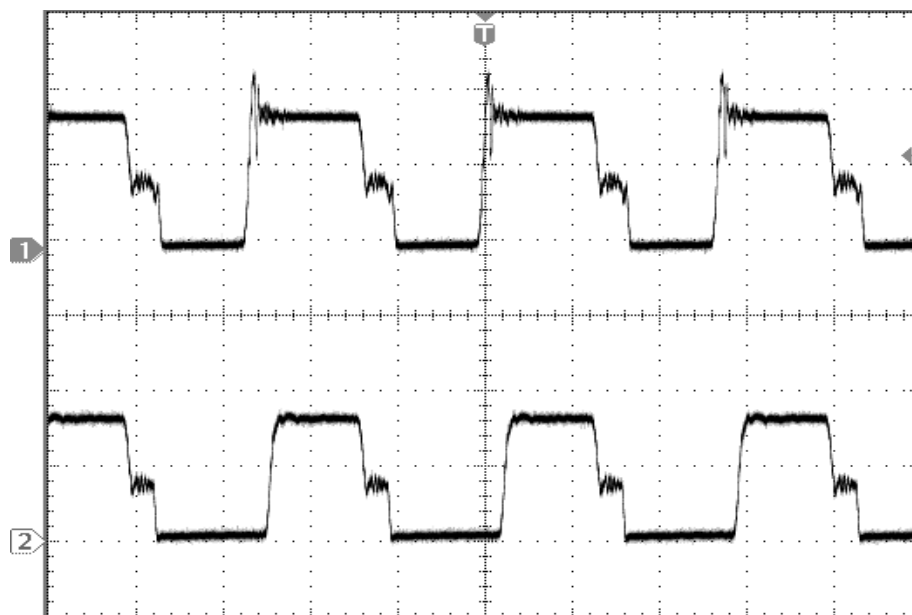
(a)   Top switch voltages V_{ds1} and V_{ds2} (V: 100V/div., t:4 µs/div.)
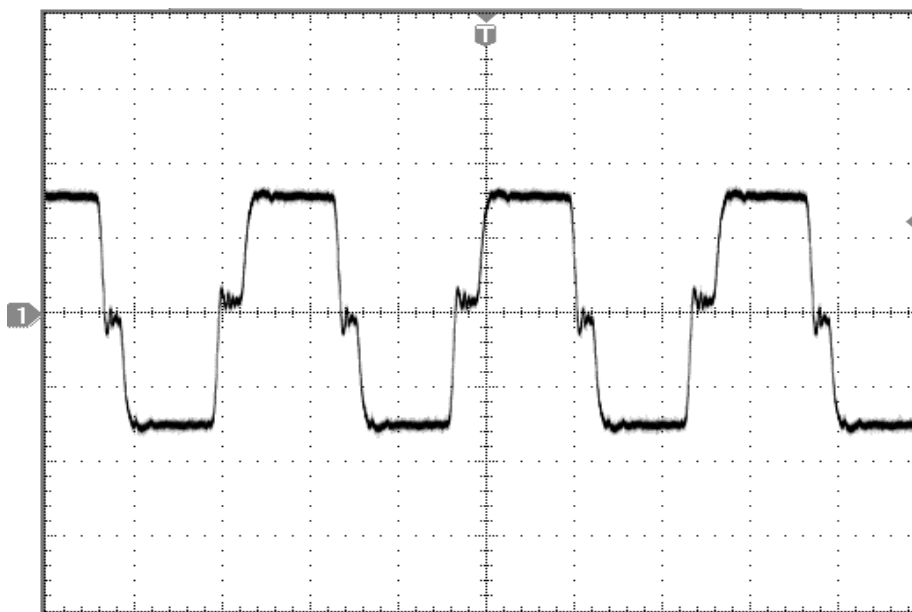
(b) Primary voltage of the main transformer (V:100V/div.,t: 4 µs/div.)
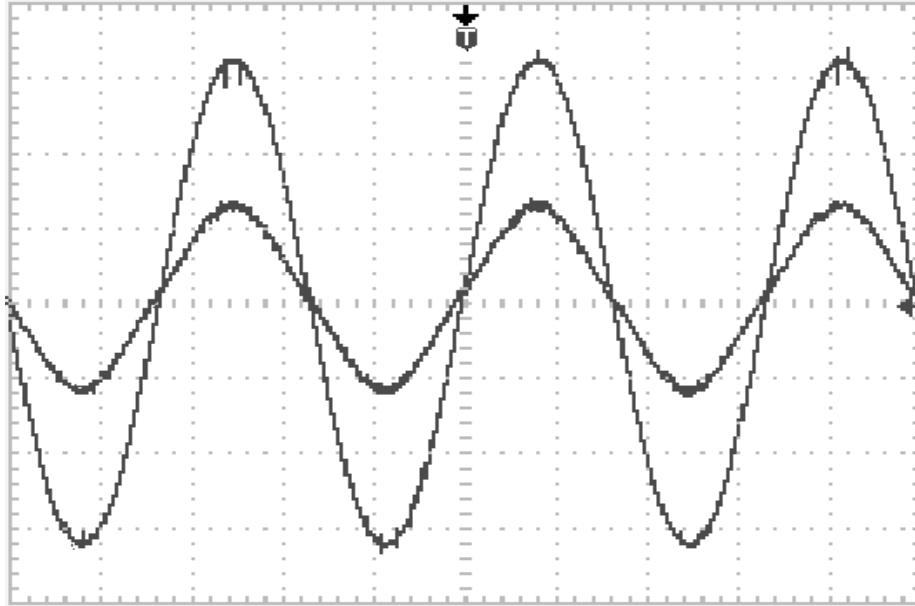
(c) Input current and voltage (V: 100 V/div, I: 4 A/div)
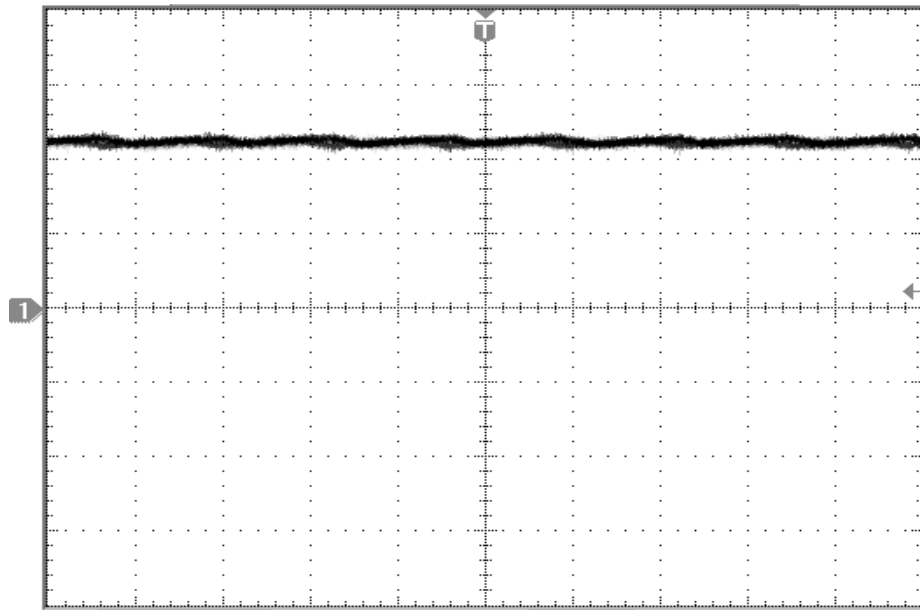
(d) Output inductor current (I:10A/div., t: 4 µs/div.)

Fig.5.31. Experimental results.

Table I: Comparison of elements for non-interleaved and interleaved converters

Components	Coverters	
	Non-interleaved three-level PFC converter	**Interleaved** three-level PFC converter
S_1-S_4	4 * FDL100N50F - 500V	
Clamp diodes	2 * MUR 860	
Rectifier diodes	DSSK60-02A	
Auxiliary rectifier diodes	-	DSI45-16A
Diode bridge	2 * SC50VB80-G	SC50VB80-G
Bus Capacitors	2 * 2200 uF	
Input boost inductor	80 µH	2 * 140 µH
Input filter inductor	3 * 20 µH	-
Input filter capacitor	3 * 1 µF	-
Output filter inductor	15 µH	100 µH
Output filter capacitor	450µF	450µF
Transformer turns ratio	25:10:10	25:10:10

Table II: Comparison of features for non-interleaved and interleaved converters

Parameters	Coverters	
	Non-interleaved three-level PFC converter	**Interleaved** three-level PFC converter
ΔV_o	1.2 V	0.06 V
ΔI_o	7.5 A	0.8 A
D_{max}	0.61	0.77
$V_{bus,max}$	533	302
THD of input current	2.9 %	0.8 %

Fig.5.32 and 5.33 show the input current harmonics at $P_o =1.1KW$ and $P_o =750$ W and Vin = 220 V_{l-lrms} . It can be seen that the converter's harmonics are below the harmonic levels that are specified by the IEC 1000-3-2 standard.
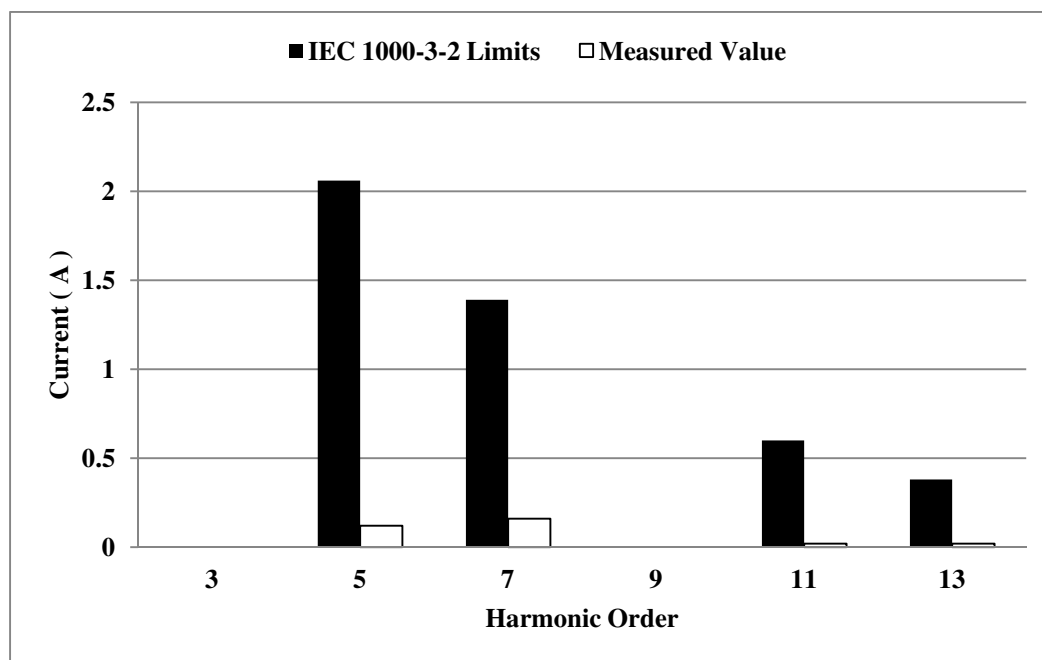
Fig.5.32. Input current harmonic at V_{in} = 220V_{rms}(l-l) , P_o=1.1 KW compared to IEC1000-3-2 standard.
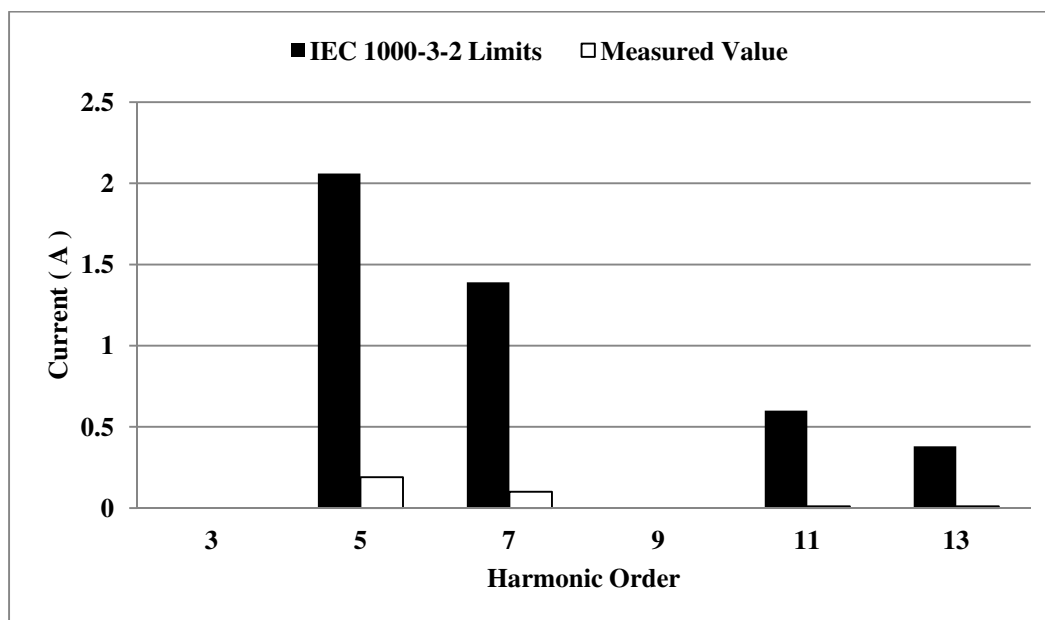
Fig.5.33. Input current harmonic at V_{in} = 220V_{rms}(l-l) , P_o=0.575 KW compared to IEC1000-3-2 standard.

Fig.5.34 shows efficiency of the proposed converter at various output power.
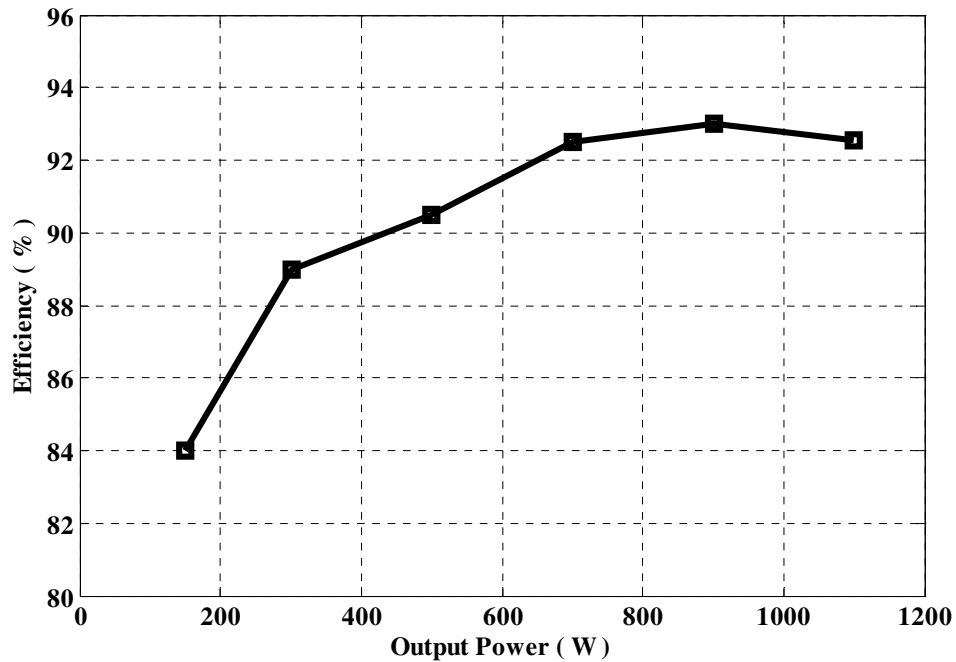
Fig.5.34. Efficiency of the proposed converter at various output power

5.4. Conclusion

In this chapter, the single-phase three-level SSPFC converter proposed in Chapter 2 was modified by changing its input section from a single-phase to a three-phase input. This was done to examine whether the principles behind the single-phase converter could be extended to a three-phase converter – something that is not possible for many previously proposed single-stage SSPFC converters. The steady-state characteristics of the new three-phase converter were determined by mathematical analysis and a design example was presented. It was confirmed that the new three-phase converter was feasible based on results that were obtained from an experimental prototype.

Based on the new three-phase converter, a second three-phase converter was proposed. This second converter was similar to the first one except that its input was interleaved with two paralleled sections so that its input current can be reduced. The

operation of the new three-phase SSPFC converter with interleaved input section and its modes of operation were explained in detail. The steady-state characteristics of the converter were determined by mathematical analysis and used to develop a procedure for the design of key converter components. The feasibility of the new converter was confirmed with results that were obtained from an experimental prototype.

Chapter 6

6. Multilevel DC-DC Converter

6.1.   Introduction

The focus of the work that was done for this thesis was on single-phase and three-phase multilevel SSPFC converters. Based on the work that was done, it was determined that multilevel converters offer several advantages over two-stage single-phase and three-phase SSPFC converters. As a result of this conclusion, it was decided to investigate the use of multilevel converter principles to improve the performance of DC-DC full-bridge converters – specifically its efficiency, especially under light-load conditions.

In this chapter, a new multilevel DC-DC converter is proposed. The basic operation of the converter is explained as are the various modes of operation that the converter goes through during a switching cycle. The steady-state characteristics of the converter are determined by mathematical analysis and are used to develop a procedure for the design of key converter components. The feasibility of the new converter is confirmed with results that were obtained from an experimental prototype.

6.2.   Three-Level DC-DC Converters for Switch-Mode Power Supplies

A new approach to improve light load converter efficiency in DC-DC full-bridge converters is based on using the conventional three-level DC-DC converter (Fig.6.1) in a novel manner. Three-level DC-DC converters are typically used in applications where the input voltage is very high. For example, in high power three-phase AC-DC converters systems where the output of an AC-DC front-end converter is fed to the input of a downstream DC-DC converter, the output voltage of the front-end converter is typically around 800-1000V. In order to avoid peak voltage stresses of 800-1000 V on the DC-DC

converter switches or use devices with lower peak voltage rating that are cheaper, more available and have better switching characteristics, three-level converters are used as the peak voltage rating of the switches in the converter is half of the input DC bus voltage.
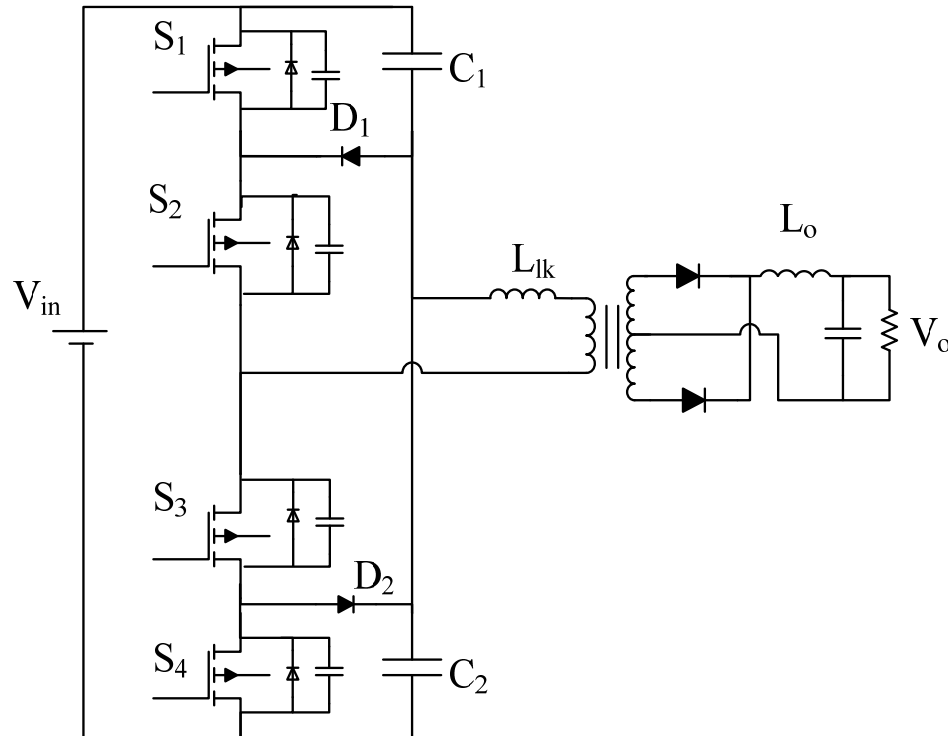
Fig.6.1. Three-level DC-DC converter for low input voltage applications.

Since three-level DC-DC converters have been limited to be used in high voltage and high power applications, they have not been considered for use in lower voltage, lower power applications such as in switch-mode power supplies. As a result, the advantages of three-level converters in lower voltage and lower power switch-mode power supplies have not been considered and power electronics personnel who work on these converters are, therefore, not familiar with three-level converters. The operation of a three-level dc-dc converter is briefly reviewed in the next section for their benefit.

6.2.1. Modes of Operation

Equivalent circuit diagrams that show the modes of operation for a half-switching cycle for the three-level converter in Fig. 6.1 are shown in Fig. 6.2. Typical gating signals for the four converter switches are shown in Fig. 6.3.

Mode 1: During this mode, switches S_1 and S_2 are on, half the dc bus voltage $V_{in}/2$ is impressed across the transformer primary, and energy is transferred to the output.

Mode 2: During this mode, switch S_1 is turned off and the voltage of C_{S1} increases from zero to $V_{in}/2$ while the voltage of $(C_{S3}+C_{S4})$ decreases from V_{in} to $V_{in}/2$ and voltages cross the switches S_3 and S_4 are exposed to $V_{in}/4$.

Mode 3: During this mode, the converter is in a freewheeling mode of operation as current freewheels through S_2 and D_1. It should be noted that the voltage across S_1 during this mode is $V_{in}/2$.

Mode 4: The converter enters Mode 4 when S_2 is turned off. The transformer primary current discharges the output capacitances of switches S_3 and S_4 so that current flows through the body diodes of these devices. The mode ends when S_3 and S_4 are turned on and the converter enters Mode 1 but with S_3 and S_4 on instead of S_1 and S_2.
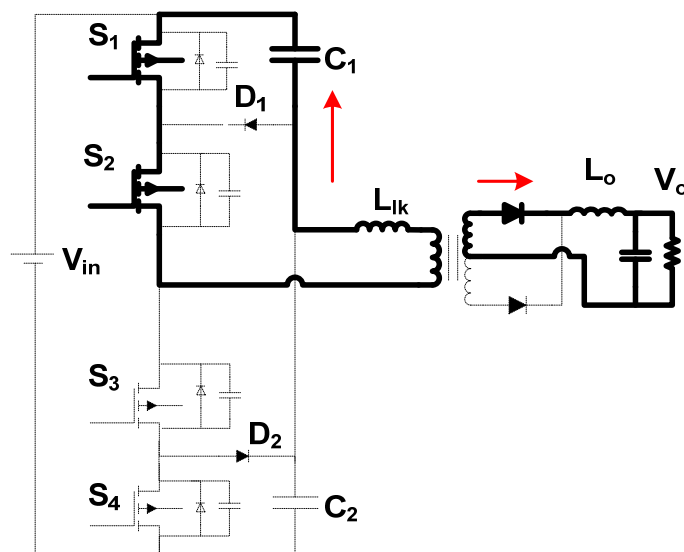
(a) Mode1

(b) Mode2

(c) Mode3

(d) Mode4
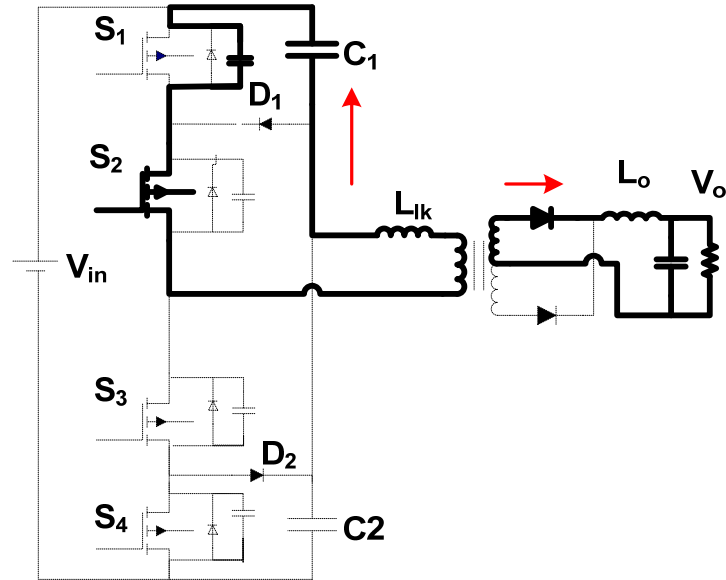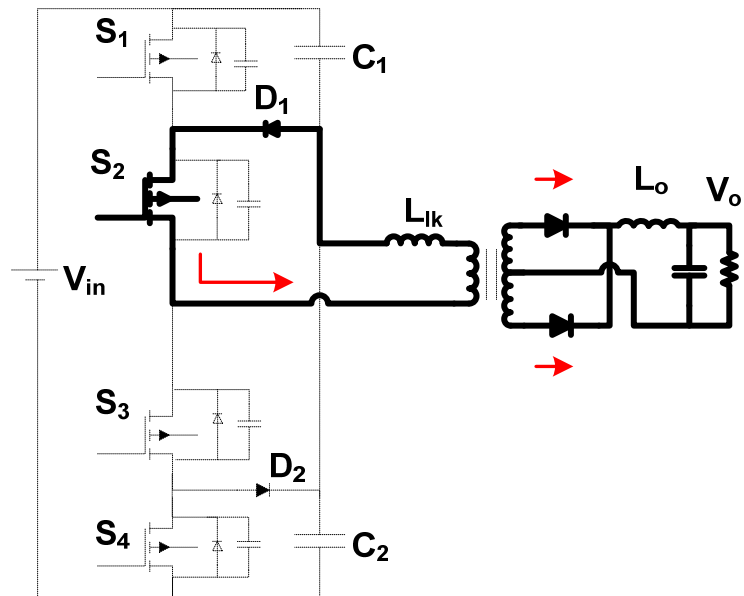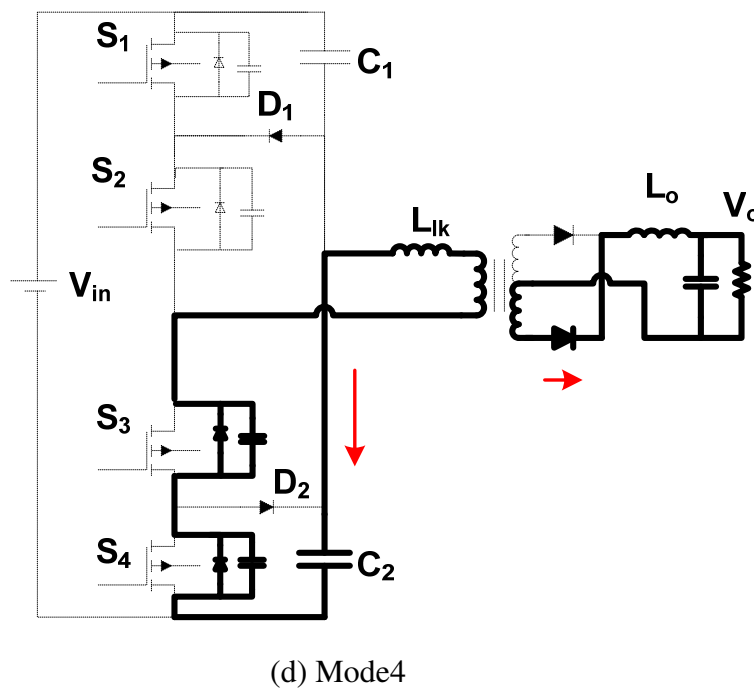
Fig.6.2. Modes of operation.
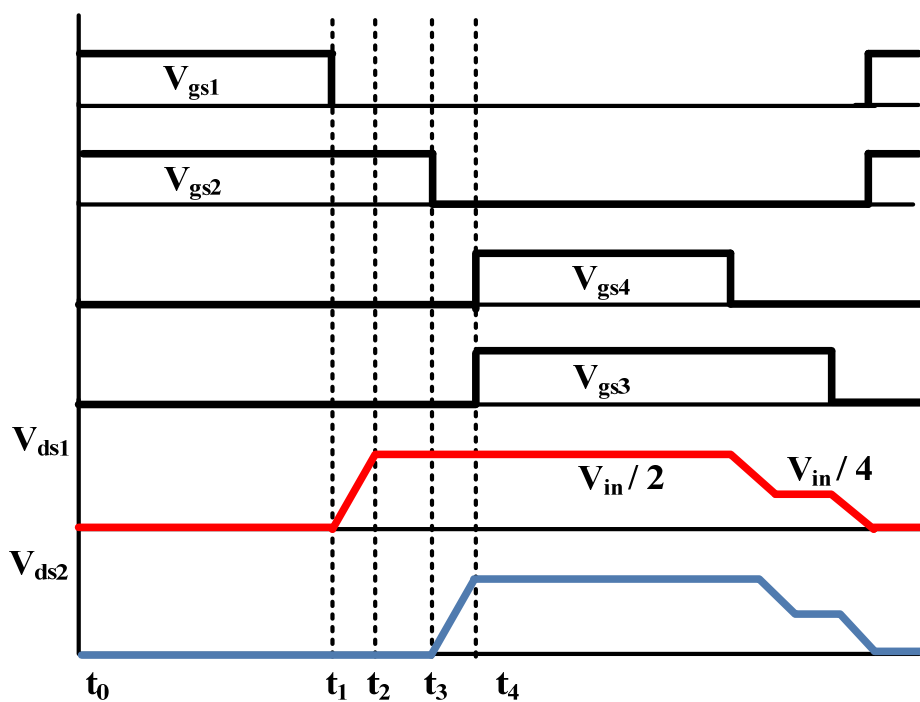
Fig.6.3. Typical waveforms of a three-level converter.

It should be noted that the switches in three-level DC-DC converters are exposed to only half of the dc bus voltage can be taken advantage to improve light-load efficiency in lower voltage and lower power applications. For example, if a three-level DC-DC converter is implemented in an application where the dc bus voltage is 400 V instead of > 600 V, which is a typical input voltage seen by a two-level converter, then the voltage across the converter switches will only be 100 V before turning on, as can be seen in Fig.6.3. If the turn-on loss of a MOSFET switch is proportional to ½ CV^2 where C is the capacitance across the device and V is the voltage across the switch, then there will be an automatic significant reduction in switching losses without the need to use any active auxiliary circuit.

6.2.2. Comparison of Two-Level and Three-Level DC-DC Converter

A ccomparison between a two-level DC-DC converter and a three-level DC-DC converter based on experimental results obtained from prototype converters will be made in the next section.

With respect to the converter switches, the switches of the three-level converter have a peak voltage stress that is half that of the switches of the two-level converter, but must conduct approximately twice as much current. This would seem to mean that the switches in the three-level converter have fewer turn-on switching losses due to ½ CV^2, but more conduction losses due to the product of I^2 and R_{ds}(on), where I is the rms current flowing through the device, typically a MOSFET, and R_{ds}(on) is MOSFET on-state resistance. Switch turn-off losses would seem to be the same given that switch voltage and current are inversely proportional when comparing these parameters with respect to the two converters.

Lower voltage rated switch MOSFET devices, however, tend to have lower values of on-state resistance R_{ds}(on) than higher voltage rated MOSFET devices. A higher voltage rated MOSFET device with a low R_{ds}(on) value is relatively expensive compared to comparable device with a higher R_{ds}(on) value and a lower voltage rated MOSFET with a low R_{ds}(on) value. As a result, when considering a comparison between two-level

and three-level converter, a key consideration that should be taken into account is whether the lower voltage rated MOSFET has a sufficiently low R_{ds}(on) value that can offset the higher conduction losses that exist when it is implemented in a three-level converter.

Switch turn-off losses would seem to be the same for both converters given that switch voltage and current are inversely proportional and turn-off losses can be calculated based on $\frac{1}{2} I_D V_D t_{off}$. However, lower voltage rated switches have lower values of t_{off} than higher voltage rated switches (the switches selected for the three-level converter in this letter have a t_{off} value that is less than half the value of that for the switches selected for the two-level converter) so that the turn-off losses in three-level converters can be less than those in two-level converters, depending on the switches that are selected.

The two-level and three-level converter prototypes were designed with the following specifications: Input voltage V_i = 400 V, output voltage V_o = 48 V, maximum output power $P_{o,max}$ = 700 W, and switching frequency f_{sw} = 50 kHz. Since the design of the conventional two-level and three-level PWM full-bridge converters is very well-known, only certain key design considerations are presented here and readers are referred to papers such as [80] for more design details.

In order to try to keep the design of the two converters similar, an attempt was made to keep the cost of the components of both converters to be the same. As a result, since lower voltage rated switches are less expensive than higher voltage rated switches and diodes are significantly less expensive than switches, it is possible for the cost of the three-level converter to be the same or even less than the two-level converter even though it has more components. Moreover, both converters were designed with the same maximum effective duty cycle (duty cycle minus duty cycle loss), D_{eff} = 0.6 and the resonant inductor L_r (defined as the sum of the primary transformer leakage inductance and an inductor placed in series with the main power transformer to extend the load range over which the converter can operate with zero-voltage switching) was chosen to have a maximum 20% reduction in primary duty cycle as per [80]. The resonant inductor L_r contributes to a loss in effective duty cycle as it causes a finite slope of rising and falling

primary current edges to appear in the transformer primary current, which delays the time when the primary voltage can be reflected to the secondary voltage (thus causing duty cycle loss).

With a maximum effective duty cycle of D_{eff} = 0.6 and a maximum 20% reduction in primary duty cycle, the maximum primary duty cycle can be expressed as

$$D = 0.6 + 0.2D \tag{6.1}$$

Solving (6.1) results in D = 0.75. The value of the resonant inductor that will result in a 20% reduction in primary duty cycle can be determined according to the following equation from [10]

$$L_r = \frac{0.2DnV_{in}}{8f_{sw}\,I_o} \tag{6.2}$$

where

$$\frac{nV_o}{V_{in}/_2} = Deff = 0.6 \tag{6.3}$$

Substituting (6.3) into (6.2) gives n= 2.5 and L_r= 25µH. Based on these values and following the design procedure shown in [80], IPD600N25N3G MOSFET devices were selected for the main full-bridge switches. These devices have an output capacitance C = 100pF and an R_{ds}(on) value of 60mΩ.

In order to have ZVS, it is necessary to have enough energy available from L_r to discharge the output capacitances of the switches before they are turned on. The following expression from [80] can be used to determine the minimum primary current needed to achieve ZVS, with V_{in} = 400, C = 100 pF and L_r= 25µH from (6.2):

$$I_{pr,min} = \frac{V_{in}}{2}\sqrt{\frac{1.5C}{L_r}} = 0.49 \tag{6.4}$$

This primary current corresponds to 1.225 A load current, which is 8% of the full load current.

A similar procedure can be done for the two-level converter. Like the three-level converter above, the two-level converter was designed for a maximum D_{eff} = 0.6, a maximum 20% reduction in primary duty cycle as per [80]. Using equations (6.2) (but with V_{in} instead of $V_{in}/2$) and (6.3)), values of n=5 and L_r= 102µH can be obtained. This value of L_r is comparable to what has been used in the literature for specifications that are like the one used for this letter. Based on these values and following the design procedure shown in [80], FDP18N50 MOSFET devices were selected for the main full-bridge switches. These devices have an output capacitance C = 350pF and an R_{ds}(on) value of 265 mΩ.

Equation (6.4) can be used to determine the minimum primary current needed to achieve ZVS for the two-level converter. Substituting V_{in} = 400, C = 100 pF and L_r= 102µH into (6.4) gives

$$I_{pr,min} = V_{in}\sqrt{\frac{1.5C}{L_r}} = 0.9 \tag{6.5}$$

This primary current corresponds to 4.5 A load current, which is 30% of the full load current. If this current is compared to the value of $I_{pr,min}$ obtained for the three-level converter, it can be concluded that for two converters of comparable cost, the ZVS range for the three-level converter is significantly greater than that of for two-level converter.

When both the three-level and two-level converters are operating with heavy loads, the conduction losses in their switches become more dominant as more current flows through them. These losses are due to the R_{ds}(on) value of the switches; therefore, less R_{ds}(on) results in fewer conduction losses and ultimately improved converter efficiency at heavy loads. Three-level converters can have fewer conduction losses than two-level converters operating with the same input voltage and load even though the transformer primary current is twice as much as the current in two-level converters. This is because switches with half the voltage rating of those used in two-level converters have considerably smaller R_{ds}(on) values and are cheaper as well. For example, the switches that were selected for the three-level converter (IPD600N25N3G) have R_{ds}(on)=60 mΩ

and the switches for two-level converter (FDP18N50) have R_{ds}(on)=265 mΩ. As a result, the three-level converter may have the same amount of conduction losses or even fewer losses than the two-level converter.

6.2.3. Experimental Results

In order to compare the performance of the conventional two-level ZVS-FB converter shown in Fig.1.9 and the conventional three-level DC-DC converter shown in Fig.6.1 for lower voltage, lower power applications, two prototypes were designed and built with the component shown in Tables I.

Table I. Converter Components

Components	Converters	
	Two-Level	Three-Level
S_1-S_4	FDP18N50 $R_{DS(on) =}$ 265 mΩ Coss=330 pF	IPD600N25N3G $R_{DS(on) =}$ 60m Ω Coss=130 pF
D_1-D_2	BYV29 (Clamping diode)	BYV29
Rectifier diodes	DSSK60-02A	DSSK60-02A
Transformer turns ratio	5:1:1	2.5:1:1
L_r	102 µH	25 µH

It should be noted in order to minimize converter voltage ringing on both the primary and secondary sides of the transformer for two-level full bridge DC-DC converter, two clamping diodes, as can be seen in Fig.6.4, added to the primary side. Inductor L_r stores extra energy to extend the soft-switching range and reduce the reverse recovery current of the secondary-side rectifier diodes, while the clamping circuit minimizes converter voltage ringing on both the primary and secondary sides of the transformer.
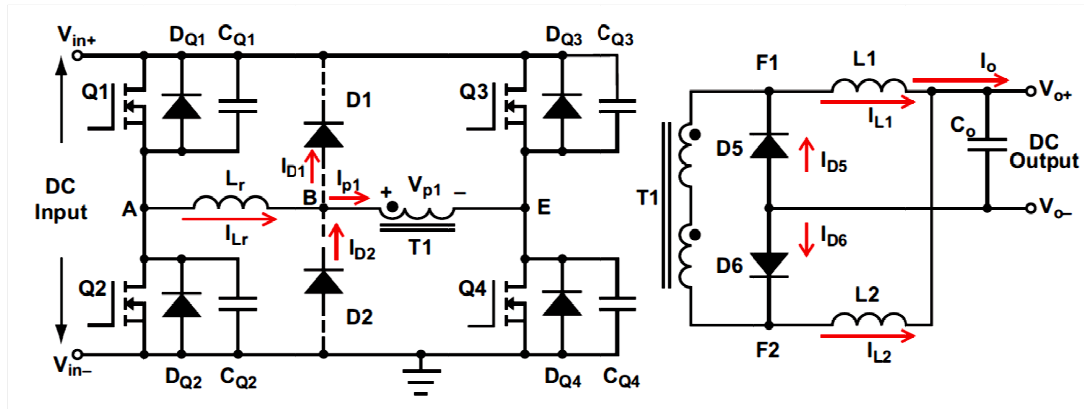
Fig.6.4. A phase-shifted, full-bridge DC-DC converter with clamping diodes [20].

Fig. 6.5(a) and 6.5(b) show typical switch voltage and transformer primary voltage waveforms for the three-level converter. It can be seen that the voltage across the switch is half the dc bus voltage and that the transformer primary voltage has the same shape as that found in a conventional two-level converter.

Fig. 6.6 shows a graph of curves of efficiency vs. output load for the two converters. It can be seen that that three-level converter has a much higher efficiency that the two-level converter under light load conditions and that the efficiency of the two converters are almost the same under heavy load conditions. This is because under light load conditions where there is generally insufficient energy to discharge the switch output capacitances, the three-level converter has more transformer energy available to discharge less capacitance energy as (a) only $V_{in}/4$ is placed across each switch instead of V_{in} (described in Mode 2) and (b) the three-level converter transformer has an input to output turns ratio that about half that of the two-level converter since $V_{in}/2$ is placed across the primary so that there is more reflected current in the primary.
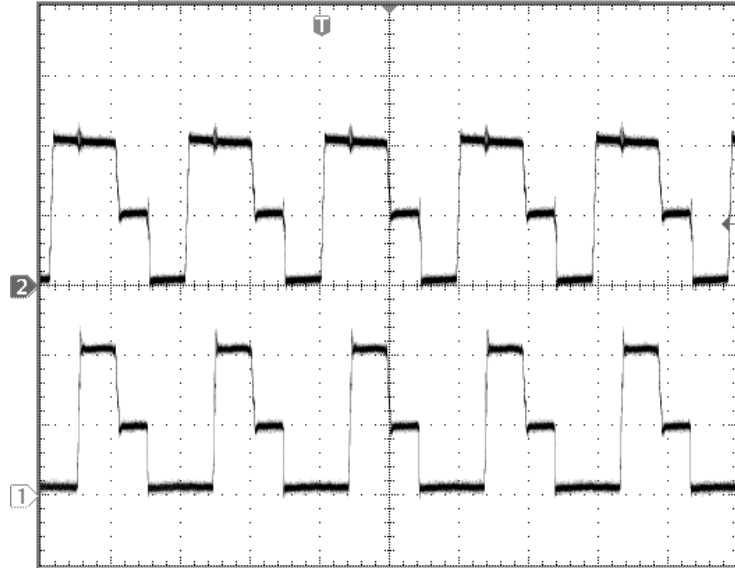
(a) Top switch voltages V_{ds1} and V_{ds2} a three-level converter (V: 100V/div., t:10 μs/div.)
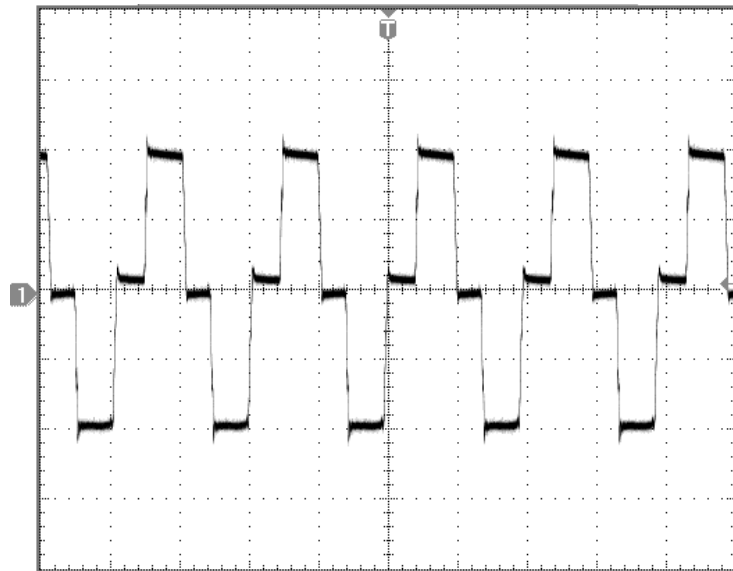
(b) Primary voltage of a three-level converter (V: 100V/div., t:10 μs/div.)

Fig.6.5. Typical waveforms of a three-level converter ($V_{in} = 400$ V)
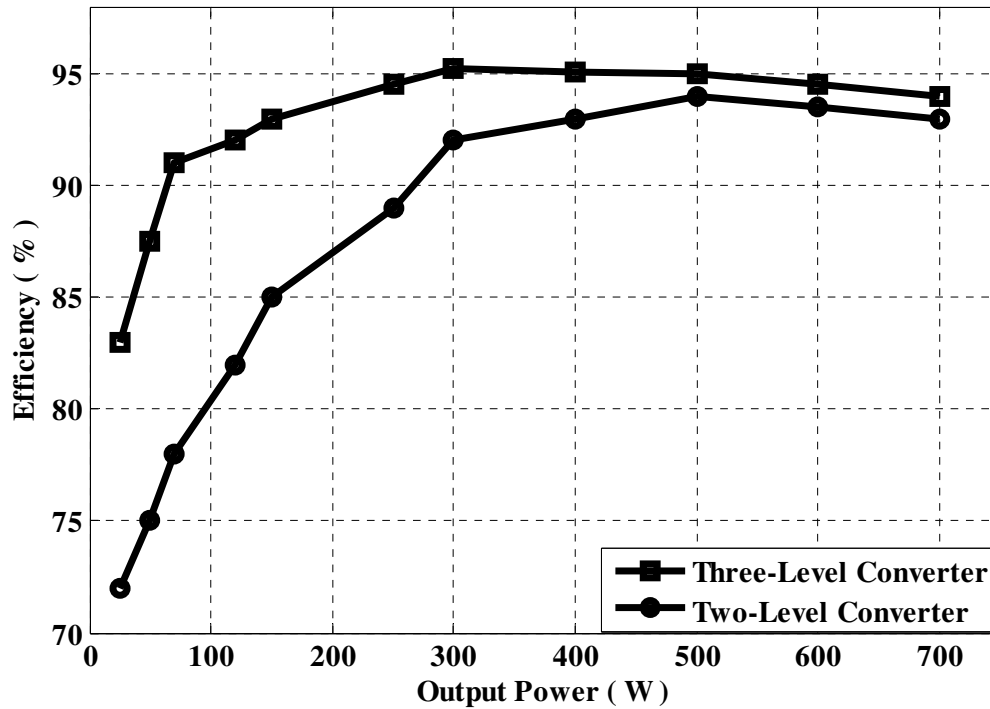
Fig. 6.6. Efficiency of ZVS full-bridge and three-level converter

Since the three-level converter has more circulating current than the two-level converter, the savings in switching losses begin to be offset by an increase in conduction losses as the load is increased. However, the switches are selected for three-level converter have smaller $R_{DS(on)}$, so that the efficiency of the three-level converter is almost the same as the two-level converter at heavier loads.

When compared to the standard two-level converter, the three-level converter has the same number of components except that it has some additional diodes for switch voltage clamping. These components can be considered to be like an auxiliary circuit that is typically found in ZVS-PWM boost converters. In other words, just as power electronics personnel typically use active auxiliary circuits to improve heavy load efficiency in ZVS-PWM boost converters, so too can an auxiliary circuit be used to improve light load efficiency. However, in the case of the three-level converter, the "auxiliary circuit" is simple, passive, and does not affect heavy load efficiency.

It should be noted that there are seemingly an infinite number of types of MOSFETs and that their cost can vary considerably over time. As a result, the decisions that power electronic designers may make in the design of DC-DC converters may be considerably different than what has been done for this thesis. Nonetheless, there may be cases where the use of three-level DC-DC converters is recommended over two-level converters, but this is a design strategy that has not been reported in the literature. The main objective of this part of the thesis has been to make power electronics designers aware of the possibilities of three-level converters.

6.3. A New DC-DC Converter with Wide-Range ZVS and Zero Circulating Current

Although the converter shown in Fig. 6.1 has better light load efficiency than the ZVS-PWM-FB converter, the trade-off of ZVS range vs. circulating current described in Section 6.1 must still be considered. A converter that can operate with ZVS under extremely light load conditions with increasing primary circulating current, which would compromise heavy load efficiency, would be very attractive.

One of the key issues related to primary circulating current is that when the two-level ZVS-PWM-FB is in a freewheeling mode of operation (when there is no voltage impressed across the transformer and thus no energy transfer from primary to secondary), this current just flows in the circuit and does nothing but contribute to power losses. Circulating current and ZVS capability are inversely related as more circulating current means a wider load range for ZVS operation as there is more energy available to discharge the switch output capacitances. This results in fewer switching losses, but more conduction losses.

It is, therefore, standard practice for ZVS-PWM-FB converter designs that the range of ZVS operation be limited to loads greater than 25%-50% full-load so that conduction losses caused by circulating current do not become excessive. But regardless

of whatever compromise is made between circulating current and ZVS range, there are two main weaknesses for the ZVS-PWM-FB topology for high-voltage applications; one of them is its poor light load efficiency and another one is the voltage stress across the switches.

Attempts have been made to increase the efficiency of full-bridge DC-DC converters by addressing this issue of circulating current vs. ZVS range, but most of these attempts have been flawed in some way. For example, converters that use zero-voltage-zero-current methods to eliminate the freewheeling mode circulating current [60]-[64] or use passive auxiliary circuits to extend the ZVS range [65]-[70] offer modest improvement over the ZVS-PWM-FB converter for light loads.

Three-level DC-DC converters have been presented in [72]-[77], [81]-[83] to reduce the voltage stress across the switches. The voltage stresses of their power switches are only half of the input voltage and not the full input voltage as is the case for two-level converters. This means that less energy is required to discharge the output capacitances of switch MOSFET devices and thus they can operate with fewer switching losses and a wider load range for ZVS than two-level converters. The circulating current in three-level converters, however, can be twice as much as that found in comparable two-level converters so that they have more conduction losses. These conduction losses can offset the gain in efficiency that are made with the extension of the load range for ZVS.

This part of the thesis proposes a new DC-DC converter that tries to take advantage of the lower switch voltage stress of three-level converters, but with minimal circulating current so that excellent converter efficiency can be achieved. In the following sections, the new converter is introduced, its basic operating principles are explained, and its modes of operation and its characteristics are discussed. The feasibility of the proposed converter is confirmed with experimental results obtained from a prototype converter.

6.3.1. Basic Principles

The main principle of the proposed converter is based on half-bridge (HB) DC-DC converters as shown in Fig. 6.7. Operating the converter with the gating signals of the switches set at 50% of the duty cycle is the most attractive way to operate a half-bridge converter. This is because the converter has no circulating current when operating with such gating signals and each capacitor has approximately the same voltage across it. Moreover, the HB converter works with soft-switching over a wide load range without using snubber circuits.
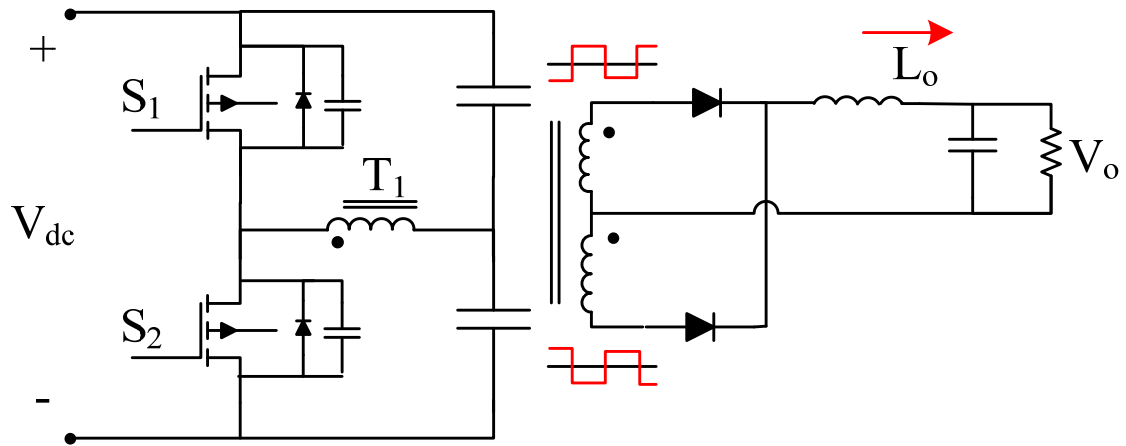
Fig. 6.7. Half-bridge converter.

The HB converter can be modified to have the topology shown in Fig. 6.8. This converter consists of a half-bridge inverter and a full-wave rectification circuit and a current-doubler output. This converter has the same advantages of the HB converter while the converter's secondary acts as two interleaved forward converter outputs connected in parallel and 180º phase offset between the two outputs. The power transformer and the output inductors operate in such a way that switches can maintain ZVS over a wide load range.
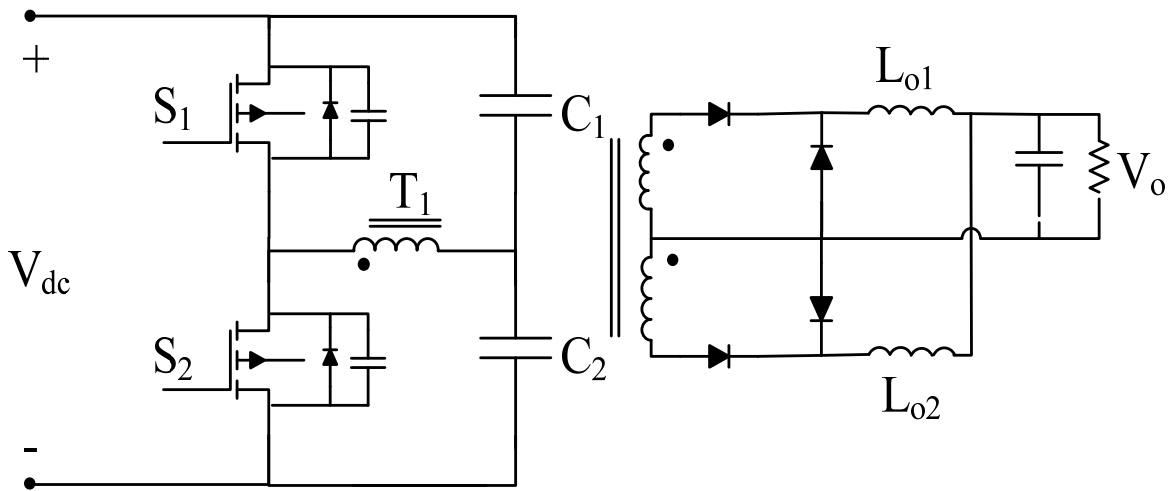
Fig.6.8. Modified half-bridge converter.

Although it is advantageous to operate a HB converter with its switches operating with 50% duty cycle, fixing the duty cycle means that the converter cannot regulate its output voltage. Several converters that combine two HB converters in their topologies and regulate the output voltage by some other means have been proposed in the literature to take advantage of the benefits of operating a HB converter with 50% duty cycle [84]-[88]. The topology proposed in [84] and [85] uses two HB converters in series at the input and in series at the output with an interleaved phase shift strategy. This converter has some advantages such as a wide load range ZVS for its switches and a voltage stress for each switch that is half of the dc bus voltage; however, this converter has the same issues that ZVS-PWM-FB converters have related to circulating current when it is in a freewheeling mode so that it suffers from conduction losses under heavy load conditions.

The converter proposed in [86] is a two stage converter that combines a buck converter stage with a HB converter. The first stage is the buck converter stage, which is used to regulate the input of the HB converter, which is made to operate with a 50% duty cycle. The buck converter stage can regulate the output and the voltage stress of the converter switches is half of the dc bus voltage; however, the switches of buck converters turn on without ZVS, which affects converter efficiency.

Another topology proposed in [87] combines two of the modified HB converters shown in Fig.6.8 by connecting them in parallel at the input and output. This converter can operate with ZVS over a wide load range and does not have any circulating current due to freewheeling modes of operation. The voltage stress of each switch, however, is equal to the dc bus voltage so that the same amount of energy is required to discharge the output switch capacitances as for the output capacitances in two-level converters, which means that the light load efficiency is still not good.

A new DC-DC converter, proposed in this section, has HB converters connected to the input together in series as shown in Fig. 6.9, with (a) one converter stacked on top of the other, (b) a PWM technique that phase-shifts the transformer voltage of one of the half-bridges with respect to the other, and (c) the secondary outputs of the two converters superimposed on a common output filter. The overall DC-DC converter can operate with the ZVS advantages and zero circulating current of a half-bridge converter, but with output voltage regulation. Moreover, the proposed converter arrangement reduces the voltage ratings of the switches so that it can operate with improved light load efficiency.
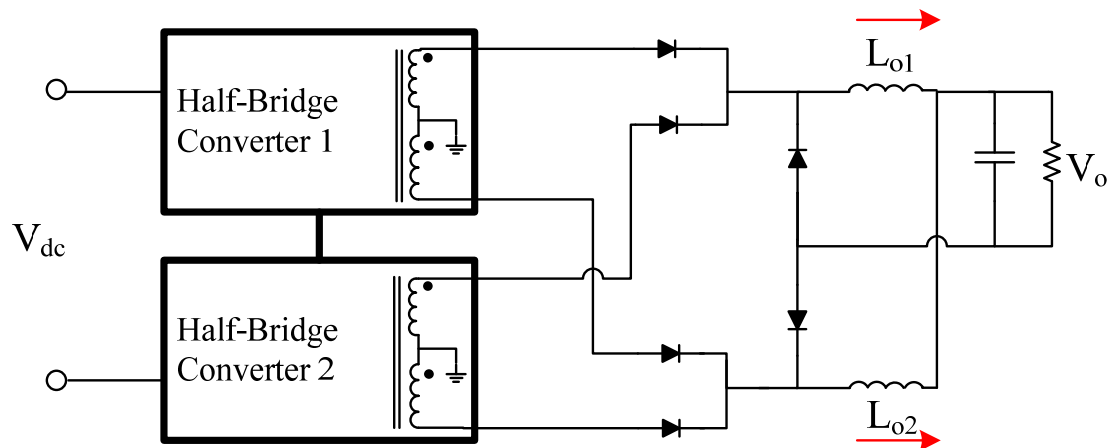
(a) The block diagram of the proposed converter
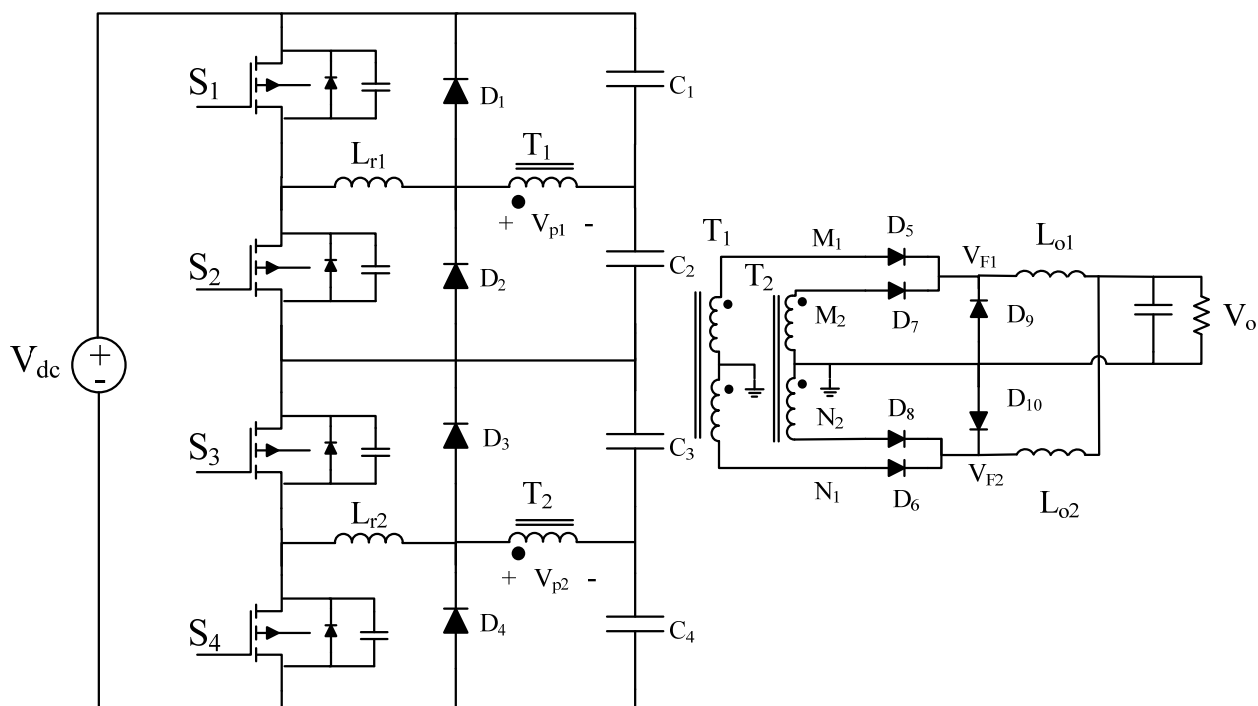
(b) Schematic of the proposed DC-DC converter.

Fig.6.9. Proposed converter.

6.3.2. Converter Operation

The proposed DC-DC converter, shown in Fig. 6.9, is made up of two half-bridge converters stacked one on top of the other. Each half-bridge has an inductor ($L_r = L_{r1} = L_{r2}$) and two clamping diodes that are added to the basic half-bridge topology. The inductor stores extra energy to extend the ZVS range while the clamping diodes minimize any voltage ringing that may appear on either side of the transformer.

As stated in the previous section, each half-bridge is operated with a 50% duty cycle and can be phase-shifted from 0° to 180° with respect to the other. This phase-shifting affects the voltage that is delivered to the current doubler filter input nodes F_1 and F_2, V_{F1} and V_{F2}. When the phase-shift is 0°, Fig.6.10, there is no overlap between V_{F1} and V_{F2}, the converter's duty cycle is 50%, and the net output voltage, V_o, is at its minimum. When the phase-shift is 180°, Fig.6.11, there is complete overlap between V_{F1} and V_{F2}, the converter's duty cycle is 100%, and V_o is at its maximum.

The output voltage can be regulated by phase-shifting the two half-bridges from full load to very light load conditions, Fig.6.12 and 6.13.
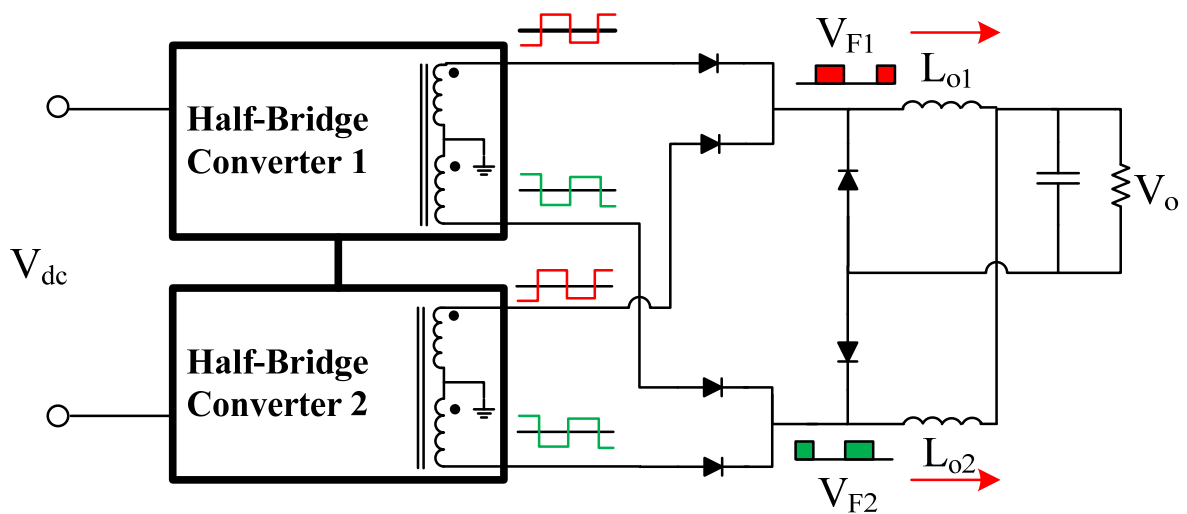
Fig.6.10. Proposed converter with zero degree phase shift.
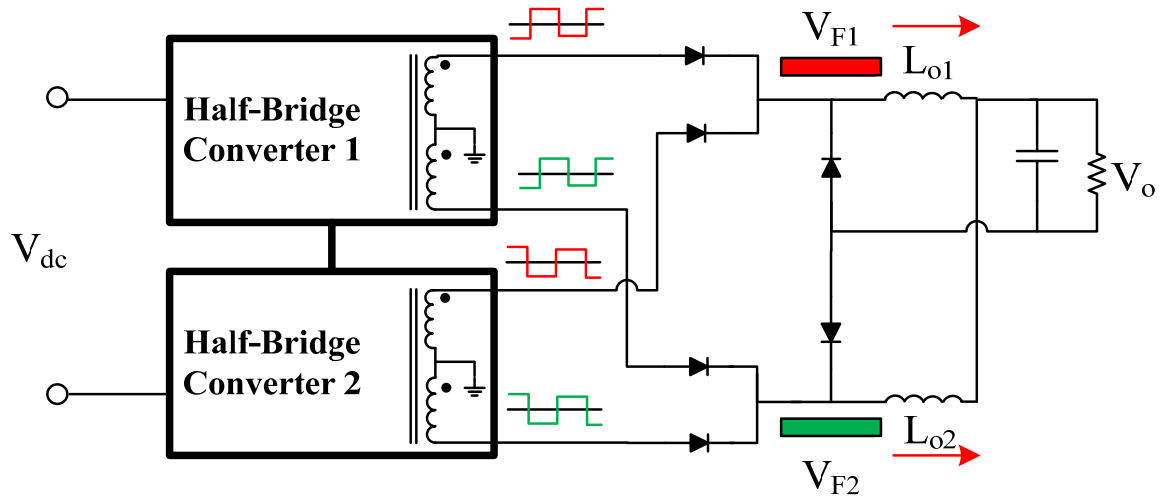
Fig.6.11. Proposed converter with 180 degree phase shift.
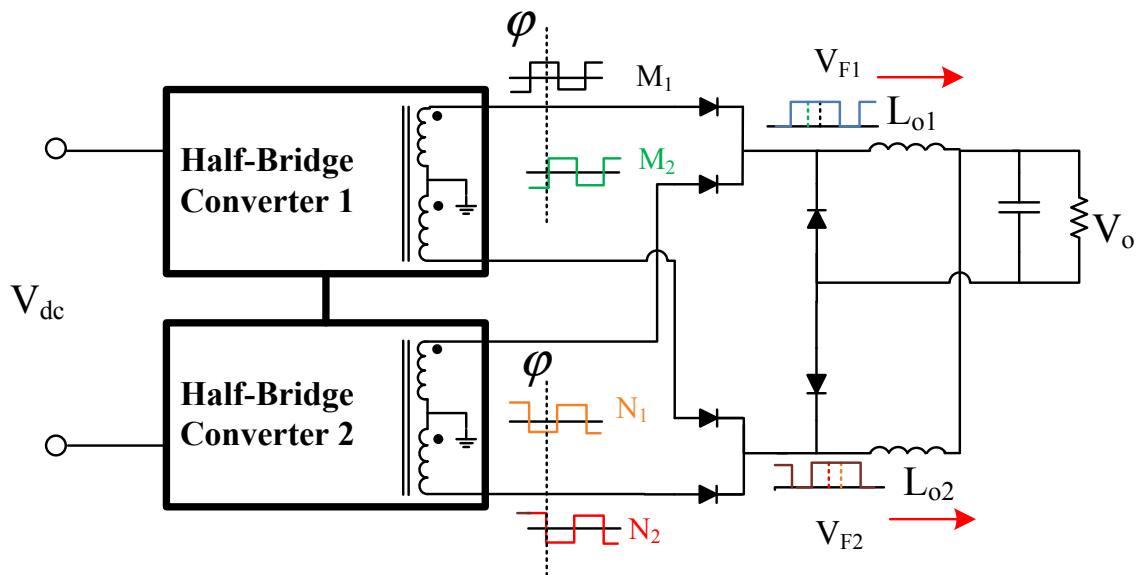
Fig.6.12. Proposed converter with φ degree phase shift.
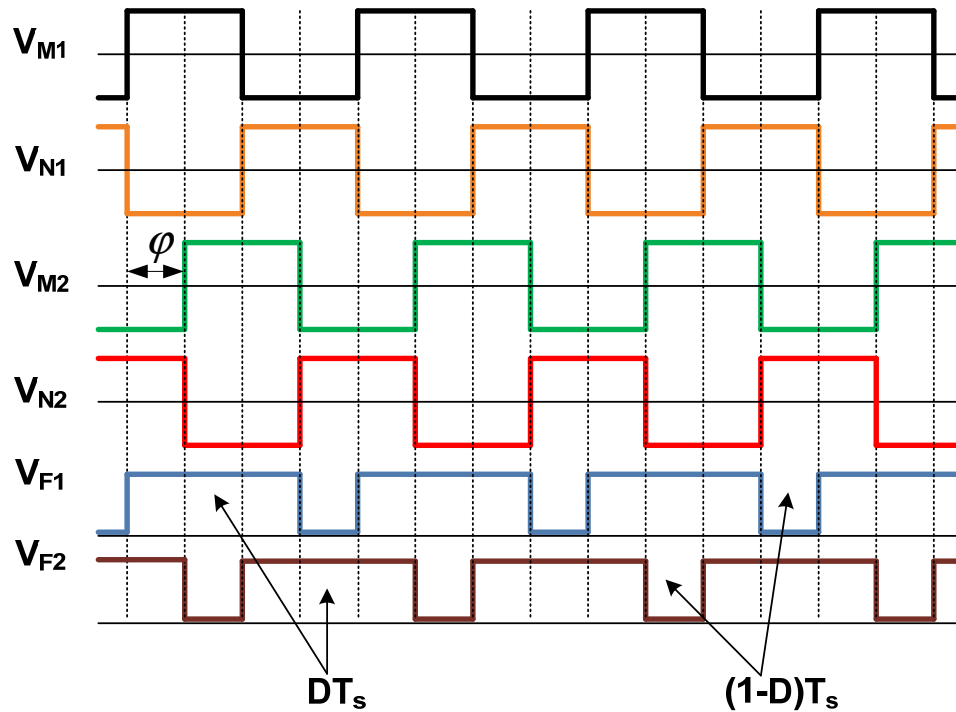
Fig.6.13. Waveforms with phase-shift control.

If the power transformer's turn radio is N:1:1, the converter input and output voltage relationship is described as:

$$V_o = \frac{V_{dc}}{4} * \left(\frac{0.5 + \varphi/360}{N}\right) \qquad (6.6)$$

and the converter's duty cycle is,

$$D = 0.5 + \varphi/360 \qquad (6.7)$$

It should be noted that this converter actually transfers power from the primary to the secondary during both D and 1-D periods. It is because of the fact that the converter has two half-bridge converters in such a way that they always transfer energy from input to the output.

The converter has the following modes of operation. It is assumed that $L_{o1}=L_{o2}$, $C_1=C_2=C_3=C_4$, turns-ratio of T_1= turns ratio of $T_2=N$ and lower half-bridge has a phase-shift, φ, respect to the upper half-bridge. The key waveforms and the equivalent circuit for each mode of operation are shown in Fig. 6.14.
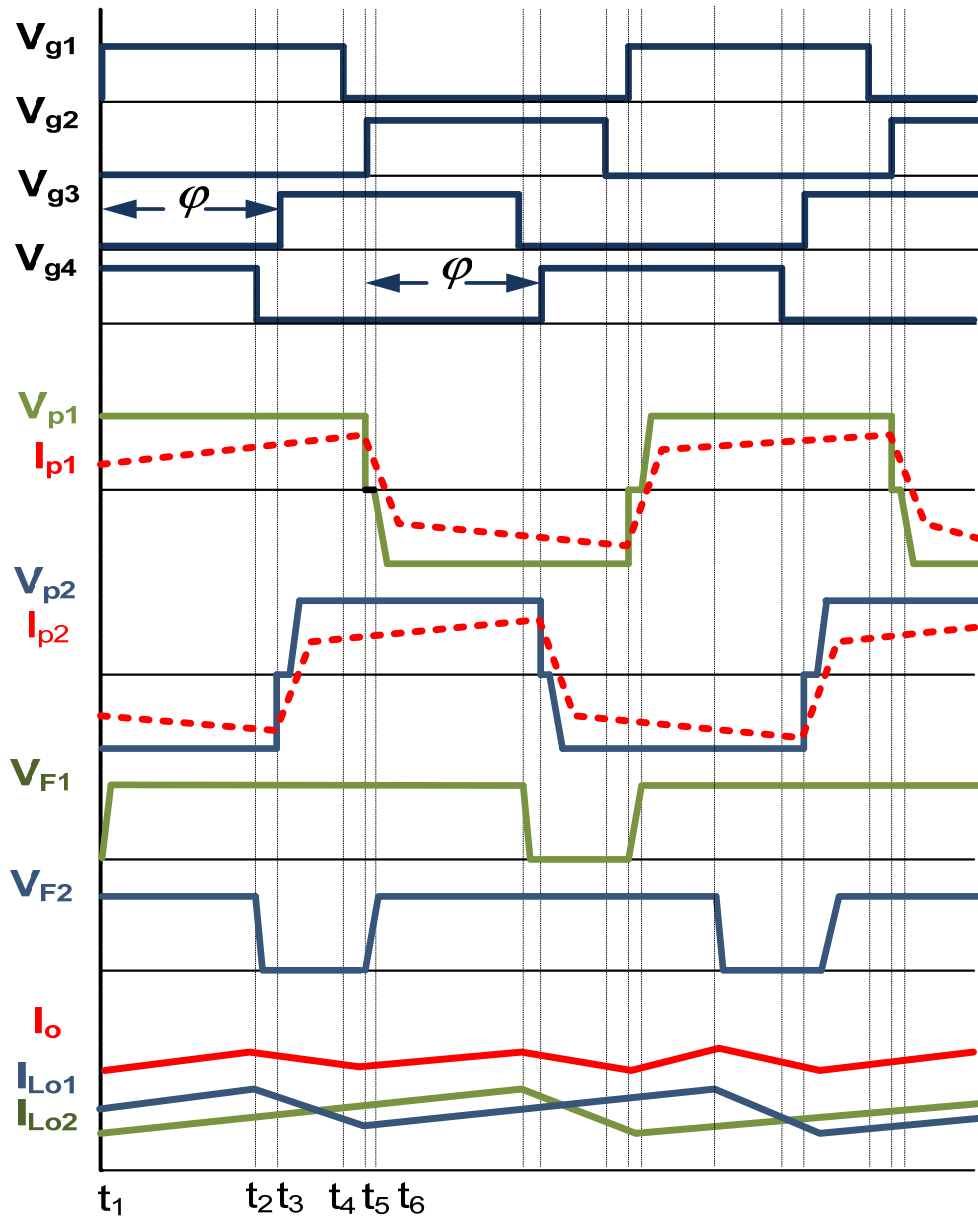
Fig. 6.14. Typical waveforms describing modes of operation.

Mode 1 (t₁ < t < t₂) (Separate Power Transferring for each HB):

During this mode, shown in Fig.6.15, switches S_1 and S_4 are ON. The voltage across the primary of T_1 is positive and the voltage across the primary of T_2 is negative and diodes D_5 and D_8 conduct. Energy is transferred from the primary side to the secondary side of both T_1 and T_2. In this mode, each HB separately transfers energy to the output. The voltage across the output inductors L_{o1} and L_{o2} are the same and equal to $V_{dc}/_{4N} - V_o$ and inductor currents i_{Lo1} and i_{Lo2} are increasing. The duration of this mode depends on the phase-shift degree φ .
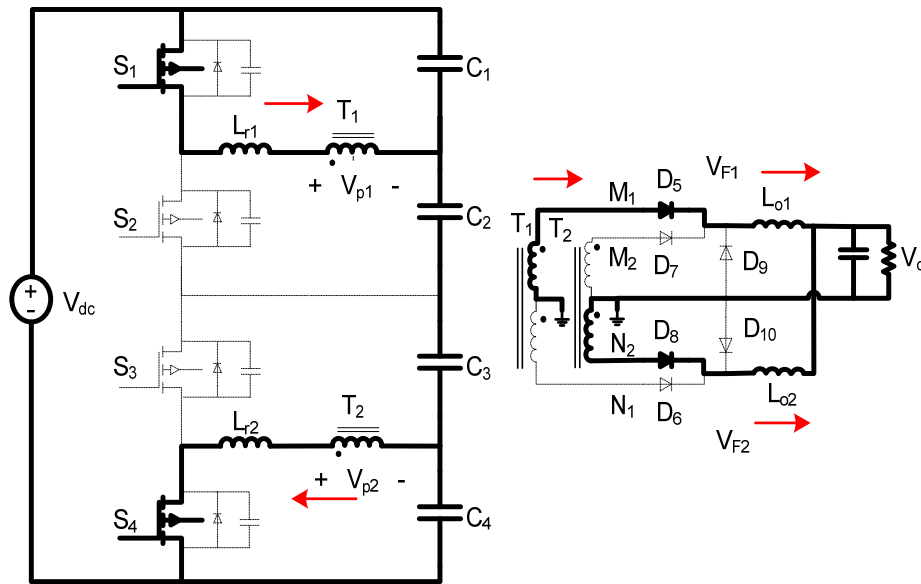
Fig.6.15. Mode 1 ($t_1 < t < t_2$)

Mode 2 (t₂ < t < t₃) (Lower HB Transition):

At t_2, S_4 is turned OFF and capacitor C_{S4} is charged and C_{S3} is discharged in resonant fashion. The primary current of T_2 also starts resonating down to zero. (Fig.6.16)
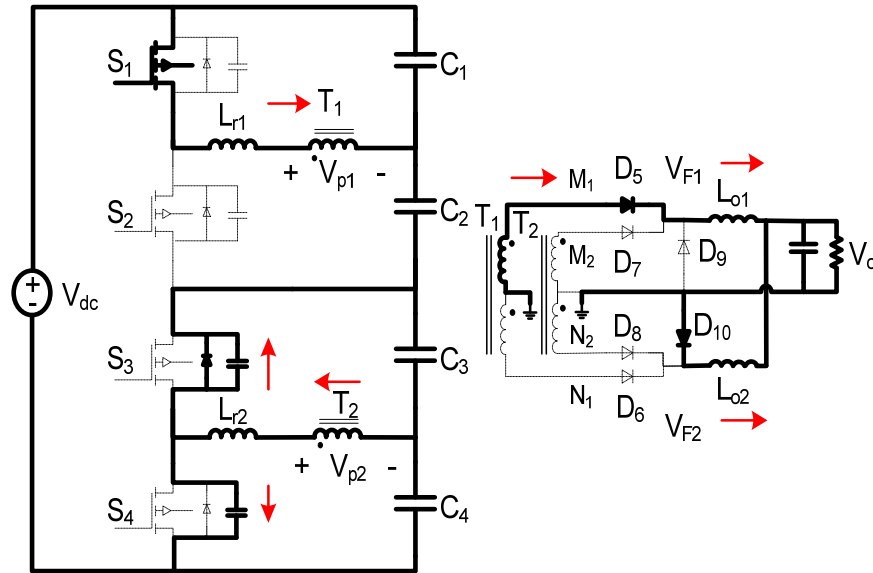
Fig.6.16. Mode 2 ($t_2 < t < t_3$)

To be able to achieve ZVS during this transition, the resonant peak of the capacitor C_{S4} has to be higher than $V_{dc}/2$. The equations describe this mode are

$$i_{Lr2} = (C_{S3} + C_{S4}) \frac{dV_{s4}}{dt} \tag{6.8}$$

$$L_{r2} \frac{d_{i_{Lr2}}}{dt} + V_{s4} = 0$$

therefore

$$i_{Lr2}(t) = I_p \cos(\omega_r t) \tag{6.9}$$

$$v_{s4}(t) = Z_r I_p \sin(\omega_r t)$$

where

$$\omega_r = \frac{1}{\sqrt{(L_{r2} \times (C_{S3} + C_{S4}))}} \tag{6.10}$$

$$Z_r = \sqrt{\frac{L_{r2}}{C_{S3} + C_{S4}}}$$

In order to achieve ZVS for S_3, it needs to have a delay time (t_d) before S_3 turns on, for the primary current of T_2 to discharge completely the body capacitor of S_3 and conduct the body diode of S_3. According to (6.9) and (6.10) t_d can be expressed by

$$t_d = \frac{1}{\omega_r}\sin^{-1}(\frac{V_{dc}}{2 \times I_p \times Z_r}) \tag{6.11}$$

$$t_d \le \frac{\pi}{2\omega_r}$$

During this mode, the primary voltage across T_2 reverses its polarity and becomes positive, which causes diode D_{10} to conduct and take over current i_{Lo2} from D_8. The top half-bridge maintains it's previous state and continues to apply a voltage to F_1 through diode D_5.

Mode 3 ($t_3 < t < t_4$) (Power Sharing):

This mode starts when S_3 turns on with ZVS. The polarity of T_1 and T_2 are both positive and diodes D_5 and D_7 both conduct and share output current, i_{Lo1} since the two transformer outputs, V_{M1} and V_{M2}, have almost the same voltage. In the meantime, D_{10} continues to conduct current i_{Lo2} and i_{Lo2} starts to decrease as -V_o is applied to L_{o2}. The decrease of i_{Lo2} and the increase of i_{Lo1} leads to current ripple cancellation and output current ripple minimization. (Fig. 6.17)

Mode 4 ($t_4 < t < t_5$) (Upper HB Transition):

At t_4, S_1 is turned off and C_{S2} is discharged and C_{S1} is charged in resonant fashion. The primary current of T_1 also starts resonating down to zero. (Fig. 6.18)
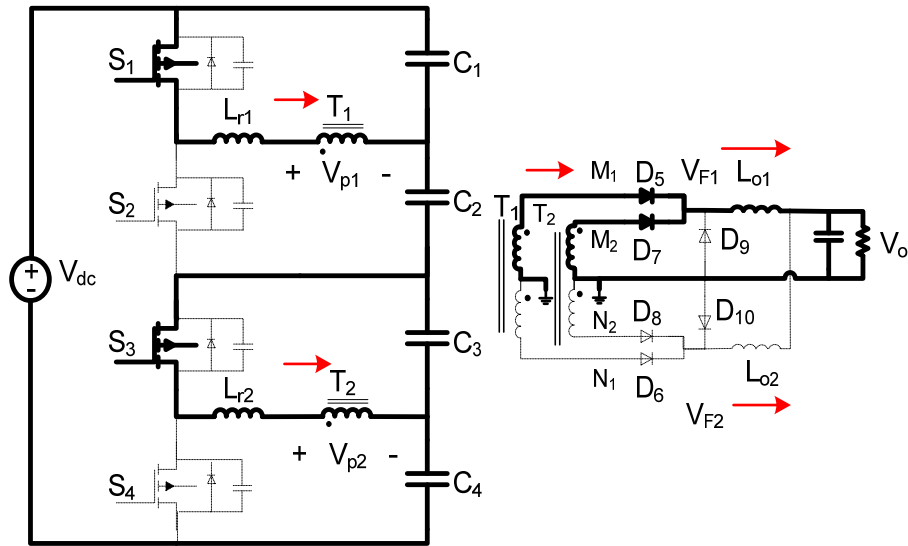
Fig.6.17. Mode 3 ($t_3 < t < t_4$)
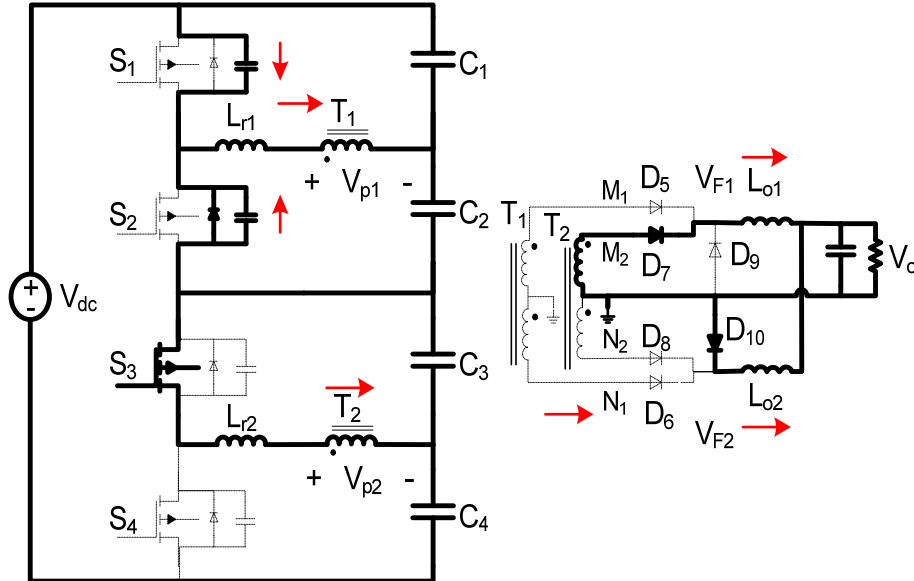
Fig.6.18. Mode 4 ($t_4 < t < t_5$)

To be able to achieve ZVS during this transition, the resonant peak of the capacitor C_{S1} has to be higher than $V_{dc}/2$. In this mode, the delay time should be the same as that for Mode 2,

$$t_d = \frac{1}{\omega_r} \sin^{-1}\left(\frac{V_{dc}}{2 \times I_p \times Z_r}\right) \tag{6.12}$$

$$t_d \leq \frac{\pi}{2\omega_r}$$

where I_p is the maximum transformer current and

$$\omega_r = \frac{1}{\sqrt{(L_{r1} \times (C_{S1} + C_{S2}))}} \tag{6.13}$$

$$Z_r = \sqrt{\frac{L_{r1}}{C_{S1} + C_{S2}}}$$

to achieve ZVS for S_2. The body-diode of S_1 starts to conduct and continues. The voltage across T_1 starts to decrease and eventually reverses its polarity. Output inductor current i_{Lo2} still continues to flow through D_{10} until D_6 starts to conduct.

Mode 5($t_5 < t < t_6$) (Separate Power Transferring for each HB):

After S_2 is turned on with ZVS at t_5, inductor current i_{Lr2} decreases to zero quickly and then starts to build up in the opposite direction. When the i_{Lr2} current reflected to the secondary becomes greater than i_{Lo2} then current is transferred from D_{10} to D_6. In this mode, each HB separately transfers energy to the output. The voltage across the output inductors L_{o1} and L_{o2} are the same and equal to $V_{dc}/4N - V_o$ and inductor currents i_{Lo1} and i_{Lo2} are increasing. (Fig. 6.19)
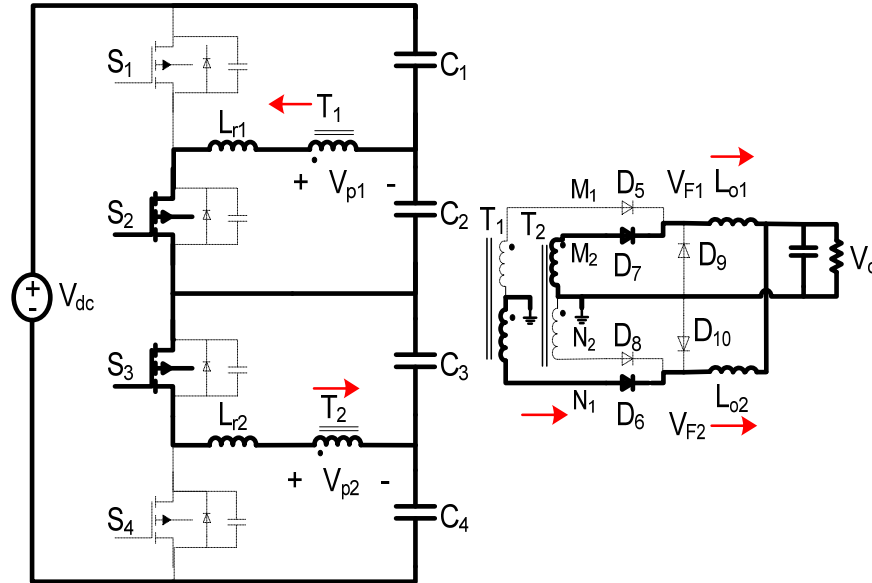
Fig.6.19. Mode 5 ($t_5 < t < t_6$)

Time t_6 is the end of the half switching cycle and another half-switching cycle begins with the same modes, but with complimentary devices conducting current. Each switching cycle has two such half switching cycles.

The proposed converter has the following features:

- It can operate with ZVS from full-load to near no-load conditions. This is because each converter switch is part of a HB converter that operates with 50% duty cycle. Since a HB converter with 50% duty cycle does not operate with any freewheeling modes of operation as does a full-bridge converter, there will always be sufficient energy to discharge the output witch capacitances.

- In addition to the fact that each converter switch is in a HB converter, it is exposed to only half the input voltage as the converter has two HB converter arranged in a multilevel structure. As a result, less energy is

needed to discharge the output capacitor of each converter switch, which further extends the load range over which the converter can operate with ZVS to near no-load conditions.

- Since the converter consists of two HB converters, which do not have freewheeling modes of operation, the converter has near zero circulating current as it transfers energy to the load during all modes of operation. This is another source of efficiency improvement.

6.3.3. Design Procedure

A design procedure for the proposed converter is given along with an example to demonstrate how the converter can be designed. The converter is to be designed with the following parameters for the example:

Input voltage: V_{dc} = 550V

Output voltage: V_o = 48 V

Maximum output power: P_o = 1.2 kW

Switching frequency: $f_{sw} = {}^1\!/_{T_{sw}}$ = 50 kHz

A. *Transformers turn-ratio and resonant inductor*

The transformer turns ratio should be chosen with potential duty-cycle reduction in mind. Duty-cycle reduction is due to the presence of inductors ($L_r = L_{r1} = L_{r2}$) that are in series with each transformer leakage inductance. As was stated at the beginning of Section III, each half-bridge has an inductor ($L_r = L_{r1} = L_{r2}$) and two clamping diodes that are added to the basic half-bridge topology. The inductor stores extra energy to extend the ZVS range while the clamping diodes minimize any voltage ringing that may appear on either side of the transformer.

The L_{r1} and L_{r2} resonant inductors cause a finite slope of rising and falling primary current edges that impact the secondary voltage as shown in Fig.6.20 [89]. Based on Fig.6.20, the duty cycle reduction can be expressed as;

$$\Delta V = L_r \frac{\Delta I}{\Delta t} \tag{6.14}$$

and;

$$\frac{V_{dc}}{2} = L_r \frac{2I_o}{\Delta D_l \, {}^{T_{sw}}\!/_2} \tag{6.15}$$

therefore

$$D_l = \frac{8 L_r I_o}{N V_{dc} T_{sw}} \tag{6.16}$$
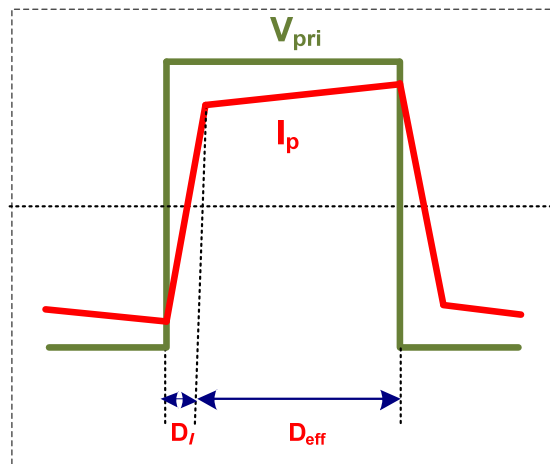
Fig.6.20. Effect of series inductor on duty cycle.

where $L_r = L_{r1} = L_{r2}$ is the resonant inductor and I_o is the maximum output load current, N is the transformer turns ratio, V_{dc} is the dc bus voltage and T_{sw} is the switching period. The effective duty cycle can be expressed as:

$$D_{eff} = D - D_l \tag{6.17}$$

By substituting (6.7) and (6.16) in (6.17)

$$D_{eff} = 0.5 + \varphi/360 - \frac{8L_r I_o}{NV_{dc}T_{sw}} \tag{6.18}$$

Fig.6.21 shows the relation between the effective duty cycle and the resonant inductance value, for $\varphi = 180°$. Fig.6.21 shows that when the value of inductor increases the effect duty cycle will decrease.
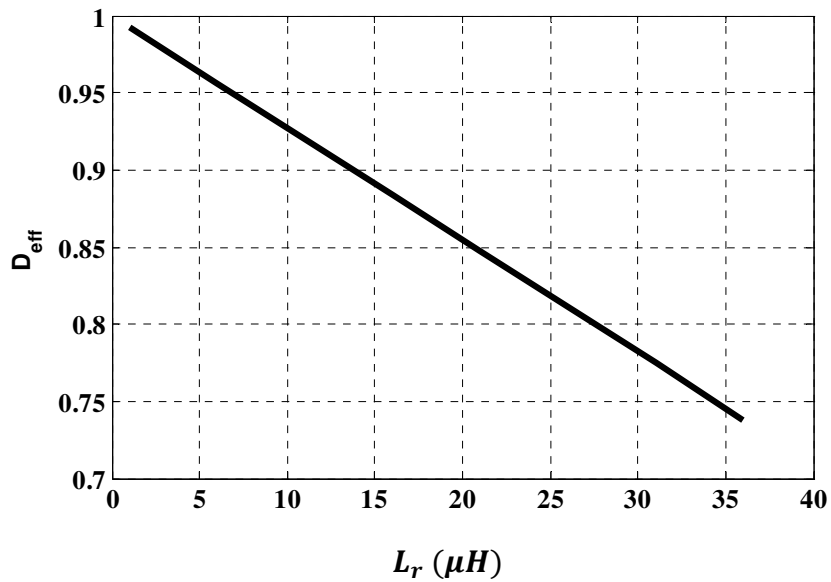
Fig.6.21. Effective duty cycle versus resonant inductance.

By substituting (6.18) in (6.6)

$$V_o = \frac{V_{dc}}{4} * \left(\frac{D_{eff}}{N}\right) \tag{6.19}$$

$$V_o = \frac{V_{dc}}{4N} * \left(0.5 + \varphi/360 - \frac{8L_r I_o}{NV_{dc}T_{sw}}\right)$$

Based on (6.19), the transformer turns ratio N can be obtained as (6.20);

$$N = \frac{V_{dc}D + \sqrt{(V_{dc}D)^2 - 128V_o f_s L_r I_o}}{8V_o} \tag{6.20}$$

Fig.6.22 shows the relation between the transformers turns ratio and the resonant inductance of the transformers for V_{dc} = 550 V, V_o = 48V, f_s=50 kHz, P_o= 1.2 kW. As it can be seen in Fig.6.22, when the value of inductor increases the transformer turns ratio should be decreased. Based on Fig.6.21 and 6.22, the desired value for N and L_r can be determined. For this example, N=2.5 and $L_r=L_{r1} = L_{r2}$ =15 µH are chosen.
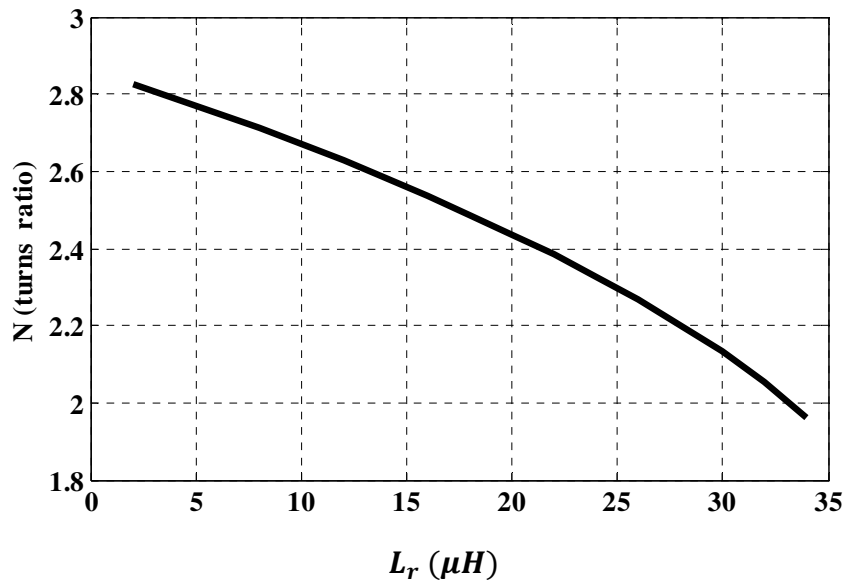
Fig.6.22. Transformers turns ratio versus resonant inductance.

B. Delay time for ZVS

Based on equation (6.11), to have ZVS the delay time, which is the amount of time between the turning off of one half-bridge switch and the turning on of another in the same half-bridge is

$$t_{d1} < \frac{\pi}{2}\sqrt{L_r(C_{s1} + C_{s2})} \tag{6.21}$$

$$t_{d2} < \frac{\pi}{2}\sqrt{L_r(C_{s3} + C_{s4})} \tag{6.22}$$

This is based on a quarter of the resonant cycle interaction between L_r and the output capacitances of the switches.

C. Input Capacitors

Assuming that the four input capacitors each have the same voltage, the high frequency voltage ripple across the capacitors can be calculated by considering the current through the capacitors in a switching cycle. The maximum peak-peak ripple of an input capacitor can be approximated by considering that at most, half of the maximum reflected load current can charge or discharge the capacitor over 50% of the switching cycle. This can be stated as

$$\Delta V_{Cin} = \frac{I_o T_s}{4NC_{in}} \tag{6.23}$$

The value of each input capacitor can be obtained by rearranging (4.23) to give

$$C_{in} = \frac{I_o T_s}{4N\Delta V_{Cin}} \tag{6.24}$$

If $\Delta V_{Cin} = 0.2V$, then the value for each capacitor should be 208uF. For this example, the the value for $C_1 = C_2 = C_3 = C_4$ is chosen to be 220uF.

If there is any voltage difference between the two secondary windings of the two transformers in parallel, the converter works the same as it does for all the modes of operation shown in Fig.6.13 except for Mode 3. In this mode, there are two cases:

Case 1: V_{M1} is larger than V_{M2}. In this case, D5 continues to conduct current as it does in previous modes. D_7 cannot conduct current until the end of this mode, when the polarity

of the V_{M1} changes. This means that only the half-bridge converter with T_1 delivers power to the output during Mode 3.

Case 2: V_{M2} is larger than V_{M1}. In this case, D_5 conducts current at the start of Mode 3, but current is transferred from D_5 to D_7 during this Mode. This means that only the half-bridge converter with T_2 delivers power to the output during Mode 3.

As a result, one converter delivers more power to the output than the other if there is any voltage difference between the two secondary windings of the two transformers. The amount of power difference depends on the amount of phase shifting between the two half-bridge converters. For example, the phase shift varies from 20° to 110° for the converter design in this paper, which can result in one half-bridge converter delivering as much as $\frac{(110-20)}{360}\%$ $= 25\%$ more power to the output than the other.

6.3.4. Experimental Results

A 1.2 kW, 550V/48V, 50 kHz DC-DC prototype was built to confirm the feasibility of the converter. The converter was implemented with the following component values:

Power MOSFETs: IRFP460

Rectifier Diodes: V20300C

Freewheel Diodes: V20100

Resonant inductor: 10µH

Output Inductor: 25µH

Power Transformer: Turn Ratio = 25:10:10

Half bridge capacitors: 4 x 220 µF

Typical converter waveforms are shown in Fig. 6.23-6.26. Fig. 6.23 shows typical gating and drain-source voltage waveforms of a switch. It shows that even at near zero load, the converter switches work with ZVS as the drain-source voltage of a switch can

be forced down to zero before the switch is turned on. Fig. 6.24 shows the primary voltage and current of the T_1 transformer for light load (5% of the full load). It shows that the half-bridge switches operate with 50% duty cycle and there is no circulating current in the circuit, even for light load. Fig. 6.25 shows voltage V_{M1} and V_{M2}; it can be seen that the two voltages are phase-shifted relative to teach other. Fig. 6.26 shows that there is no ringing at the output rectifiers. This is due to the presence of the clamping diodes at the primaries of both transformers.

Fig. 6.27 shows the efficiency of the proposed converter compared to other previously proposed three-level DC-DC converters operating at 50 kHz. The most important characteristic to note is the "flatness" of the efficiency curve of the proposed converter; the proposed converter can operate with an excellent efficiency even under light load conditions while other converter have a significantly lower light load efficiency. This is because of the lack of freewheeling circulating current in the transformer primary and the fact that the converter can operate with ZVS over almost the full load range (except for the very lightest of loads).
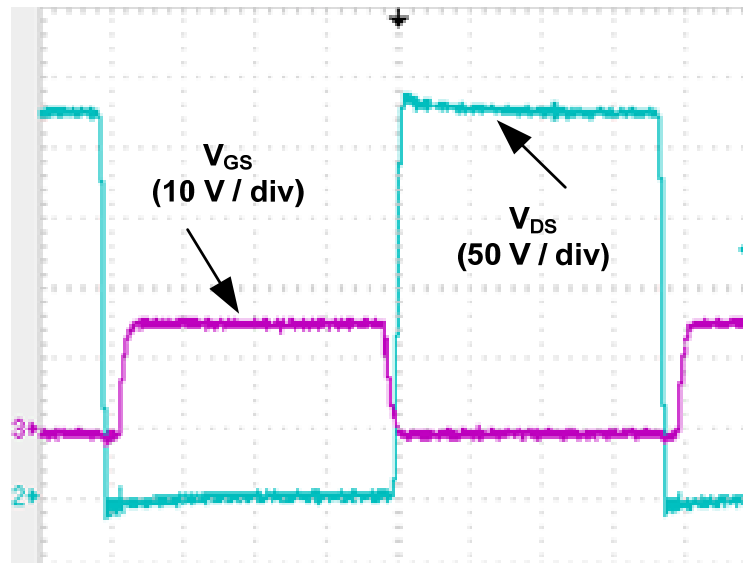
Fig.6.23. Gate and drain-source waveforms for P_o=60W.
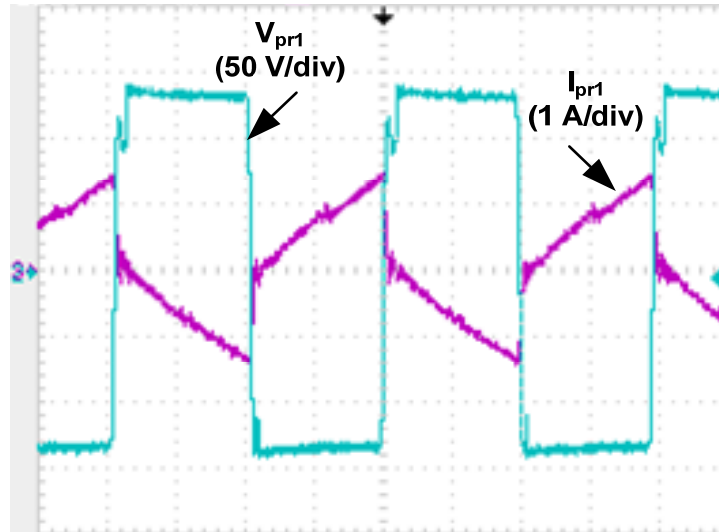
Fig.6.24. Transformer primary voltage and current waveforms (P_o=60W).
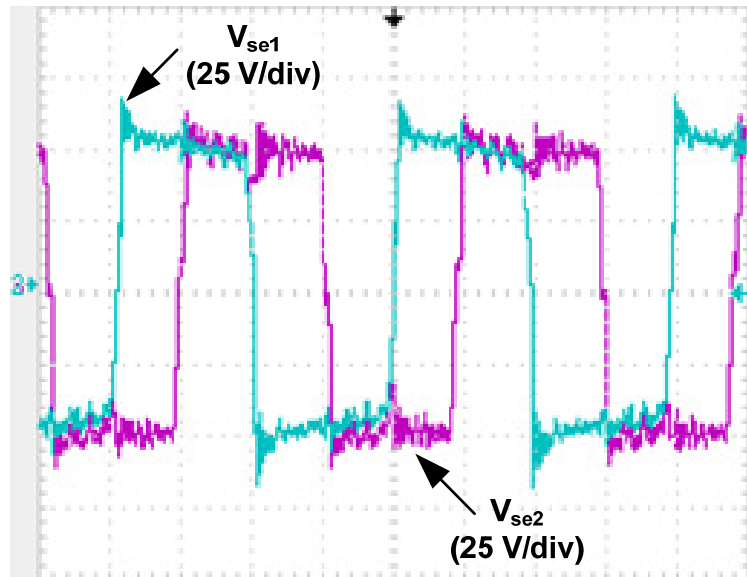
Fig.6.25. Transformer secondary voltage waveforms (P_o=900W).
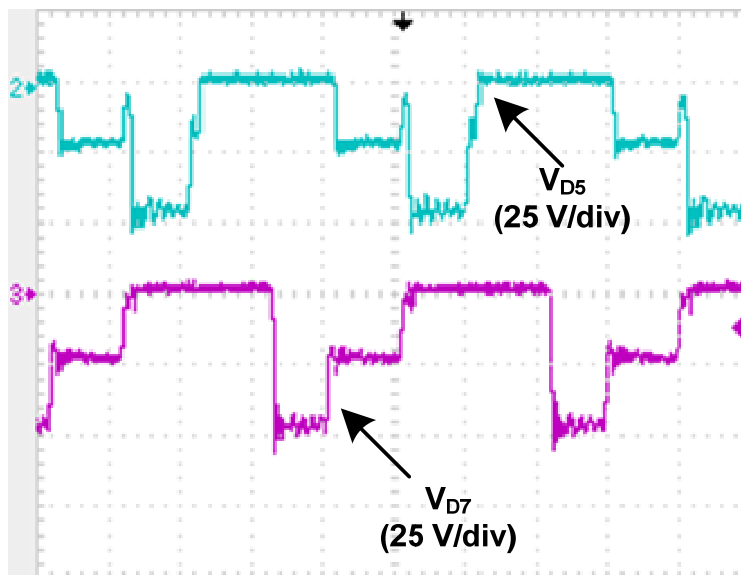
Fig.6.26. Voltages of rectifier diodes (P_o=900W).
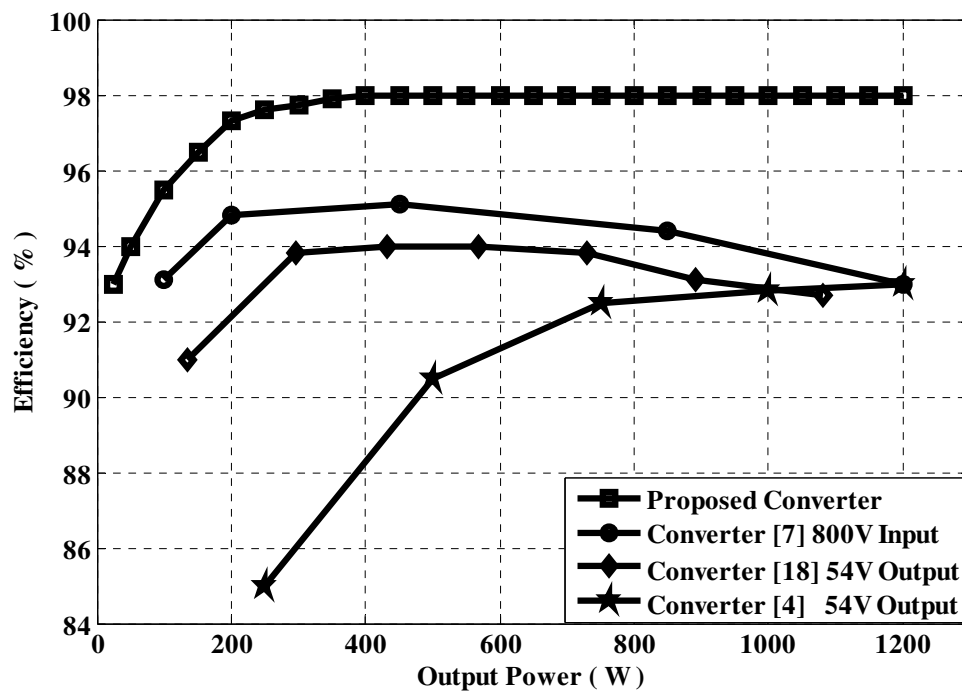
Fig.6.27. Efficiency of the proposed converter at different output power.

It should be noted that none of the diodes in the converter have any reverse recovery issues. In the case of the primary side diodes, there is no reverse recovery because the diodes turn on and off softly due to the presence of inductances in the converter. For example, two primary side diodes are connected to a common node with the cathode of one connected to the anode of another. At this node, there is a connection for the main power transformer and a resonant inductor. Any rise or fall of current in the primary diodes is therefore constrained by inductances and thus there is no reverse recovery current in these diodes.

As for the secondary diodes, there is no reverse recovery because the commutation of the current from a conducting diode to another diode is affected by the leakage inductances of the transformer and by the lack of sufficient voltage to force the commutation. Fig. 6.28 and 6.29 show the rectifier diode current and freewheeling diode current respectively without reverse recovery current.
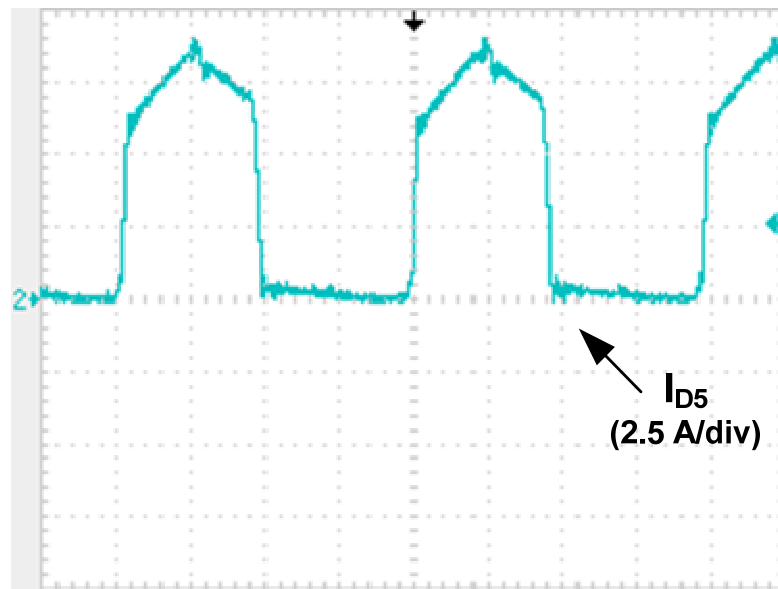
Fig.6.28 Current of a rectifier diode (P_o=1200W).
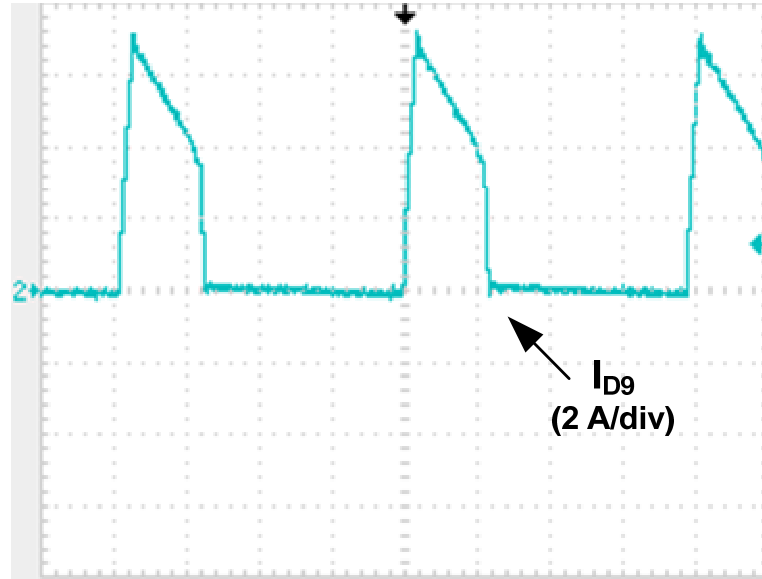
Fig.6.29 Current of a freewheeling diode (P_o=1200W).

6.4.   Conclusion

A new three-level DC-DC converter was proposed in this chapter. The outstanding feature of this converter is that it can operate with ZVS from full-load to near no-load conditions with hardly any circulating freewheeling primary current due to its novel structure. This structure is based on the stacking of two half-bridge converters that operate with 50% duty cycle on top of each other, with voltage regulation performed by phase-shifting one half-bridge with respect to the other. Since such half-bridge converters do not have freewheeling modes of operation and since the converter switches are exposed to only half the input voltage, the converter can have high efficiency even under light load conditions. In the chapter, the basic operation of the converter was explained, its features were stated, and its design was discussed. The feasibility of the converter was experimentally confirmed with results obtained from a prototype.

Chapter 7

7. Summary and Conclusion

7.1. Summary

AC-DC and DC-DC converters are widely used for electrical power conversion in many industrial applications such as for telecom equipment, information technology equipment, conventional and electric vehicles, space power systems and power systems based on renewable energy resources. This thesis has focused on the use of multilevel, three-level converter circuit structures (topologies) to improve the performance of AC-DC and DC-DC switch-mode power supply converters.

Chapter 1 presented a literature survey of what can be considered to be the state of the art for AC-DC and DC-DC converters. In this chapter, the drawbacks of previous proposed converters were reviewed and the thesis objectives and outline were stated.

In Chapter 2, a new three-level, single-stage single-phase power-factor-corrected (SSPFC) AC-DC PWM converter that operates with a single controller was presented. The proposed converter operates with universal input voltage (90– 265 Vrms) and with a better efficiency, less distorted input current, wider load operating range, and less output inductor current ripple than previously proposed SSPFC converters. The advantageous features of the proposed converter are due to the fact that it is a three-level converter, which allows the uncontrolled primary-side dc bus voltage to be higher than what can be allowed for two-level converters; therefore it does not have the design restrictions that two-level converters have. The operation of the new converter was explained in detail and analyzed, and its steady-state characteristics were determined. The converter's design was discussed and a design procedure was established and demonstrated with an example. Experimental results obtained from a prototype confirmed the feasibility of the new converter and its ability to meet IEC 1000-3-2 standards for electrical equipment.

In Chapter 3, two modifications to the SSPFC converter introduced in Chapter 2 were proposed. The first modification was the addition of a simple auxiliary circuit that is active only when the converter is operating under light load conditions. This auxiliary circuit allows the converter to operate with significantly reduced output inductor current ripple under heavy load conditions. As a result, secondary-side component peak current stresses and the output voltage ripple are significantly reduced without making the light load primary-side dc bus voltage excessive. The second modification was to make a small change to the SSPFC converter presented in Chapter 2 to allow it to operate phase-shift pulse-width modulation (PWM) instead of the conventional PWM method for three-level converters. Doing so increased the efficiency of the converter, especially for light load operation. The two modifications were briefly discussed and their effectiveness in improving converter performance was confirmed with experimental results.

A new multilevel single-stage AC-DC converter was proposed in Chapter 4. This converter was operated with two controllers – one controller that performed input PFC and a second controller that regulated the output voltage. The outstanding feature of this converter is that it can operate with a performance that is comparable to that of two-stage converters, but at a lower cost as it has a single-stage converter topology. The basic operating principles and modes of operation of the converter were explained in the chapter and its design was discussed. The feasibility of the converter was confirmed with experimental results that were obtained from a prototype converter.

In Chapter 5, the SSPFC single-controller converter that was proposed in Chapter 2 was modified for three-phase operation to see how well it could operate with a three-phase input and with higher power levels. It was confirmed that this three-phase SSPFC converter can operate with the advantageous features of the single-phase converter under these conditions. Based on the new three-phase, three-level SSPFC converter, a new three-phase, three-level SSPFC converter with interleaved input was derived and proposed. The proposed interleaved converter has the advantageous features of the new three-phase SSPFC converter, but with reduced input current ripple, which reduces input section component stresses and EMI noise and filtering. The operation of the proposed interleaved converter was explained in detail and analyzed, its steady-state characteristics

were determined, and its design was discussed. The feasibility of the converter was confirmed with experimental results obtained from a prototype converter.

Since it was determined that multilevel converter concepts can be used to improve the performance of AC-DC switch-mode power supply converters, therefore, an effort was made to investigate whether multilevel converter concepts can be used to improve the performance of DC-DC converters. As a result, a new three-level DC-DC converter was derived and this converter was proposed in Chapter 6. The outstanding features of this converter are that it operates with zero-voltage switching (ZVS) from full-load to near no-load conditions with hardly any circulating freewheeling primary current due to its novel structure. This structure is based on stacking two half-bridge converters that operate with 50% duty cycle on top of each other and voltage regulation is performed by phase-shifting one half-bridge with respect to the other. Since such half-bridge converters do not have freewheeling modes of operation and since the converter switches are exposed to only half the input voltage, the converter has high efficiency even under light load conditions; 95% for 10% of full load. The basic operation of the converter was explained, its features were stated, and its design was discussed. The feasibility of the converter has been experimentally confirmed with results obtained from a prototype.

7.2. Conclusions

Based on the research that was performed, the following can be considered to be the most significant conclusions of the thesis:

- It was determined in Chapter 2 that applying multilevel converter concepts to single-phase, single-stage converters can result in a greater load operating range and less input current distortion and output ripple than what can be achieved with previously proposed single-stage PFC converters.

- It was determined in Chapter 3 that a SSPFC converter can be implemented with a simple auxiliary circuit at its output that can help reduce output inductor

current and output voltage ripple, without making the light load primary DC bus voltage excessive.

- It was determined in Chapter 3 that making a modification to the multilevel SSPFC converter proposed in Chapter 2 and operating it with the conventional phase-shift PWM technique can result in increased power conversion efficiency.

- It was determined in Chapter 4 that converter proposed in Chapter 2 can be successfully implemented with two controllers instead of just one to improve the performance of the converter.

- It was determined in Chapter 5 that the multilevel SSPFC converter proposed in Chapter 2 can be adapted for three-phase inputs, resulting in less input current distortion and less output ripple that other previously proposed three-phase SSPFC converters.

- It was determined in Chapter 5 that an interleaved input section can be successfully integrated into the three-phase SSPFC multilevel converter to produce an input current with significantly reduced input current ripple.

- It was determined in Chapter 6 that a multilevel DC-DC converter can operate with high efficiency and a nearly flat efficiency vs. load curve for a wide load range due to certain inherent properties of multilevel topologies.

7.3. Contributions

The following are the most significant contributions of the thesis:

- A new single-phase single-stage three-level PFC AC-DC PWM converter was proposed. The proposed converter operates with universal input voltage (90–265 V_{rms}) and with a better efficiency, less distorted input current, wider load operating range and less output inductor current ripple than similar, previously proposed converters of the same type.

- A new, simple auxiliary circuit was proposed to reduce the output voltage ripple of single-stage PFC converters while avoiding excessive primary-side dc bus voltages. This auxiliary circuit can be used for single-phase or three-phase, two-level or three-level SSPFC converters.

- A new single-phase single-stage three-level PFC AC-DC phase shift modulation (PSM) converter was proposed. This converter can operate with standard and readily available commercial ICs and with greater light load efficiency than similar converters based on multilevel topologies.

- A new AC-DC single–stage three-level converter with two controllers was proposed. The proposed converter has the merits of the multilevel SSPFC converter, and but can regulate the dc bus voltage like a two-stage converter.

- A new three-phase single-stage three-level PFC AC-DC PWM converter was proposed. The proposed converter operates with a better efficiency, less distorted input current, wider load operating range, and less output inductor current ripple than similar converters of the same type.

- A new interleaved three-phase, single-stage three-level PFC AC-DC PWM converter was proposed. The proposed converter can reduce the input ripple current and therefore can reduce the size value of input filtering significantly.

- A new multilevel DC-DC converter that can operate with zero-voltage switching (ZVS) from almost no-load to full-load conditions and with reduced circulating current was proposed. The efficiency curve of the proposed converter shows a significant improvement over that of more conventional two-stage converters.

- Procedures for the design of these converters were established, thus enabling power electronics personnel to implement these converters.

- The feasibility of all the new converters proposed in the thesis was confirmed with results obtained from experimental, proof-of-concept, and laboratory prototypes.

7.4. Suggested Future Work

The following suggestions for future work can be made as a continuation of the research that was performed in this thesis:

- The single-stage AC-DC converters proposed in the thesis operate with hard switching. No attempt was made to maximize converter efficiency by using any zero-voltage switching or zero-current switching techniques to reduce switching losses. Research can be done to investigate the use of such techniques to improve converter efficiency – to see how effective these techniques are and to see which techniques are the most effective.

- The DC-DC multilevel converter proposed in Chapter 6 was operated with a maximum load of 1.2 kW. Unlike conventional two-level converters, the efficiency vs. load curve did not begin to dip before this load was reached. Research can be performed to determine how the converter operates at heavier loads and when the efficiency vs. load curve begins to dip.

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Appendix A

MATLAB Programs

A.1. Characteristic of a three-level single-phase single-stage ac-dc Converter

```
clear all
clc
fsu=60;
fsw=50000;
fsn=2*fsw/fsu;
Tsw=1/fsw;
nn=1;
vinmin=220;
N=2.5;
Lo= 15e-6;
Laux=30e-6;

%************* Calculating D and Vbus ************************
for po=100:100:1000
   jj=1;
   for D=0.05:0.001:0.85
     vbus=2*vo*N/D;

     status= (po/vo)-(1/2)*(((vbus/(2*N))-vo)/Lo)*(D/(2*fsw));
     if status >=0
       vbus=2*vo*N/D; %CCM
```

```
      Icboutave=(po/vo)*D/(2*N);
   else
      vbus = 2*N *(vo+sqrt(vo^2+(16*po*Lo/(Tsw*D^2))))/2; %DCM
      Icboutave=(D^2/(4*N*Lo*fsw))*(vbus/(2*N)-vo);
   end


   fsn=round(fsn);
   Icbinave1=0;


   for kk=1:fsn
      vsk = vinmin*sqrt(2)*abs(sin(2*pi*kk/fsn));
      K1  = ((D^2)/(4*Laux*fsw))*(vsk*vsk)/(1-vsk/vbus);


      Icbinave2=Icbinave1+K1;
      Icbinave1=Icbinave2;
   end


   pin=Icbinave2/(2*fsn);
   error(jj)=abs(po - pin);
   jj=jj+1;
end

[x I]=min(error);
D=(1/1000)*(I-1)+0.05;
DD(nn)=D;

vbus=2*vo*N/D;
status= (po/vo)-(1/2)*(((vbus/(2*N))-vo)/Lo)*(D/(2*fsw));

if status >=0
   vbus=2*vo*N/D; %CCM
```

```
    else
        vbus = 2*N *(vo+sqrt(vo^2+(16*po*Lo/(Tsw*D^2))))/2; %DCM
    end


    VBUS(nn)=vbus/2;
    RESULT=[VBUS ; DD*0.5]
    nn=nn+1;
end

po=100:100:1000;
RESULT=[VBUS ; DD*0.5]
Plot(po,VBUS)
```

A.2. Design on Inductor for a three-level single-phase single-stage ac-dc Converter

```
clear all
clc

vo=48;
po=1000;
fsu=60;
Tsu=1/fsu;
fsw=50000;
Tsw=1/fsw;
Dmax=0.75;
fsn=2*fsw/fsu;

vinmin=90;
vbusmin=300;

for k=0:fsn-1

    vsk(k+1)=vinmin*sqrt(2)*abs(sin(2*pi*k/fsn));
    K1(k+1)=(vsk(k+1)*vsk(k+1))/(1-(vsk(k+1)/vbusmin));

end

K=mean(K1);
L= ((Dmax^2)/(4*po*fsw))*K
```

A.3. Characteristic of a three-level three-phase single-stage ac-dc Converter

```
clear all
clc
vo=48;
fsu=60;
fsw=50000;
fsn=2*fsw/fsu;
Tsw=1/fsw;
nn=1;
vinmin=220/sqrt(3);


N=3;
Lo= 11e-6;
Laux=60e-6;


%************* Calculating D and Vbus ************************
for po=100:200:300

  jj=1;
  for D=0.1:0.001:0.7
        vbus=2*vo*N/D;

    status= (po/vo)-(1/2)*(((vbus/(2*N))-vo)/Lo)*(D/(2*fsw));

    if status >=0

      vbus=2*vo*N/D; %CCM
      Icboutave=(po/vo)*D/N;
    else
```

```matlab
    vbus = 2*N *(vo+sqrt(vo^2+(16*po*Lo/(Tsw*D^2))))/2; %DCM
    Icboutave=(D^2/(4*N*Lo*fsw))*(vbus/(2*N)-vo);
  end


  fsn=round(fsn);
  Icbinave1=0;


  for kk=1:fsn
    vska =vinmin*sqrt(2)*abs(sin(2*pi*kk/fsn));
    vskb =vinmin*sqrt(2)*abs(sin(2*pi*kk/fsn-2*pi/3));
    vskc =vinmin*sqrt(2)*abs(sin(2*pi*kk/fsn+2*pi/3));



    K1=(D^2/(4*Laux*fsw*sqrt(3)))*((vska*vska)/(1- vska/vbus))
    +(D^2/(4*Laux*fsw*sqrt(3)))*((vskb*vskb)/(1-vskb/vbus))
    +(D^2/(4*Laux*fsw*sqrt(3)))*((vskc*vskc)/(1-vskc/vbus));


    Icbinave2=Icbinave1+K1;
    Icbinave1=Icbinave2;
  end


  Icbinave=Icbinave1/fsn;
   error(jj)=abs((po-2*Icbinave));


   jj=jj+1;
end
[x I]=min(error);
D=(1/1000)*(I-1)+0.1;
DD(nn)=D;


vbus=2*vo*N/D;
```

```
    status= (po/vo)-(1/2)*(((vbus/(2*N))-vo)/Lo)*(D/(2*fsw));


    if status >=0
        vbus=2*vo*N/D; %CCM
    else
        vbus = 2*N *(vo+sqrt(vo^2+(16*po*Lo/(Tsw*D^2))))/2; %DCM
    end


    VBUS(nn)=vbus/2;
    RESULT=[VBUS ; DD]
    nn=nn+1;
end


tt=100:200:1500;
plot(tt,VBUS)
```

A.4. Design on Inductor for a three-level three-phase single-stage ac-dc Converter

```
clear all
clc

vo=48;
po=1500;
fsu=60;
Tsu=1/fsu;
fsw=50000;
Tsw=1/fsw;
Dmax=0.75;
 fsn=2*fsw/fsu;
 vinmin=128;
vbus=520;

Icbinave1=0;
 for kk=1:fsn
   vska =vinmin*sqrt(2)*abs(sin(2*pi*kk/fsn));
   vskb =vinmin*sqrt(2)*abs(sin(2*pi*kk/fsn-2*pi/3));
   vskc =vinmin*sqrt(2)*abs(sin(2*pi*kk/fsn+2*pi/3));

   K1=(Dmax^2/(4*fsw))*((vska*vska)/(1-
vska/vbus))+(Dmax^2/(4*fsw))*((vskb*vskb)/(1-
vskb/vbus))+(Dmax^2/(4*fsw))*((vskc*vskc)/(1-vskc/vbus));
   Icbinave2=Icbinave1+K1;
   Icbinave1=Icbinave2;
end

L=Icbinave1/(fsn*po*sqrt(3))
```

Curriculum Vitae

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Post-secondary   Isfahan University of Technology
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                       Isfahan University of Technology
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                       1999-2001 M.Sc.

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Publications:

1. **M. Narimani**, G. Moschopoulos, "A New Single-Phase Single-Stage Three-Level Power Factor Correction AC-DC Converter", *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2888-2899, 2012.

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4. **M. Narimani**, G. Moschopoulos, "A New DC-DC Converter with Wide-Range ZVS and Reduced Circulating Current", Early Access in *IEEE Transactions on Power Electronics,* 2012.

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