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Investigation on the Benefits of Safety Margin Improvement in CANDU Nuclear Power Plant Using an FPGA-based Shutdown System

Jingke She
The University of Western Ontario

Supervisor
Dr. Jin Jiang
The University of Western Ontario

Graduate Program in Electrical and Computer Engineering
A thesis submitted in partial fulfillment of the requirements for the degree in Doctor of Philosophy

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By

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School of Graduate and Postdoctoral Studies
The University of Western Ontario
London, Ontario

THE UNIVERSITY OF WESTERN ONTARIO
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_____

Dr. Jin Jiang

Advisory Committee

_____

Dr. Arash Reyhani-Masoleh

_____

Dr. Robert Sobot

Examining Board

_____

Dr. Mark Lawford

_____

Dr. Robert E. Webber

_____

Dr. Xianbin Wang

_____

Dr. Robert Sobot

The thesis by

Jingke She

Entitled

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ABSTRACT

The relationship between response time and safety margin of CANadian Deuterium Uranium (CANDU) nuclear power plant (NPP) is investigated in this thesis. Implementation of safety shutdown system using Field Programmable Gate Array (FPGA) is explored. The fast data processing capability of FPGAs shortens the response time of CANDU shutdown systems (SDS) such that the impact of accident transient can be reduced. The safety margin, which is closely related to the reactor behavior in the event of an accident, is improved as a result of such a faster shutdown process.

Theoretical analysis based on neutron dynamic theory is carried out to establish the fact that a faster shutdown process can mitigate accidental consequences. To provide more realistic test cases from a thermalhydraulic perspective, an industry grade simulation tool known as CATHENA is used to generate comparable accident-shutdown transients for different SDS response times. Results from both verification methods explicitly prove the feasibility of improving the safety margin via faster shutdown process.

To demonstrate this concept, a prototype of the proposed faster SDS is constructed. The trip logic of CANDU shutdown system No.1 (SDS1) is converted into a digital hardware design and implemented within chosen FPGA platform. The functionality of the FPGA-based SDS1 is implemented, and the response times are tested and compared to those of the existing CANDU SDS1. The achieved 10.5 *ms* response time of the FPGA-based SDS1 is again applied to the CATHENA simulation process to quantitatively present the 26.98% improvement in the safety margin.

To investigate potential improvement in safety margin by using FPGA technology, hardware-in-the-loop (HIL) simulation is performed by connecting the FPGA-based SDS1 to an NPP training simulator. The 6.26% improvement in safety margin has been verified, based on which a 10% potential power upgrade is discussed as another benefit of applying FPGA technology to CANDU NPPs.

Keywords: FPGA, safety margin, CANDU, response time, SDS1, HIL, power upgrade.

Learning is like rowing upstream,

not to advance is to drop back.

学如逆水行舟，

不进则退。

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ABBREVIATIONS AND NOMENCLATURE

Abbreviations

2oo3	Two-out-of-three voting
A/D	Analog to Digital
AECB	Atomic Energy Control Board
AECL	Atomic Energy Canada Ltd.
ALARA	As Low As Reasonable Achievable
AOO	Anticipated Operational Occurrence
ASIC	Application Specific Integrated Circuit
BWR	Boiling Water Reactor
CANDU	CANadian Deuterium Uranium
CATHENA	Canadian Algorithm for THEermalyhraulic Network Analysis
CNSC	Canadian Nuclear Safety Commission
CSA	Conservative Safety Analysis
DBA	Design Based Accident
DCC	Digital Control Computer
DSP	Digital Signal Processing
EDA	Electronic Design Automation
EdF	Electricite de France
E/E/PE	Electrical, Electronic, and Programmable Electronic systems
EMI	Electromagnetic Interference
EPZ	Elektriciteits Produktiemaatschappij Zuid-Nederland
FPGA	Field Programmable Gate Array
HIL	Hardware-In-the-Loop
HTS	Heat Transport System
I&C	Instrumentation and Control
I/O	Input and Output

IAEA	International Atomic Energy Agency
IEC	International Electrotechnical Commission
LOCA	Loss of Coolant Accident
LOFA	Loss of Flow Accident
NI	National Instruments
NPP	Nuclear Power Plant
PCB	Printed Circuit Board
PDC	Programmable Digital Comparator
PHT	Primary Heat Transport
PJA	Prompt Jump Approximation
PLD	Programmable Logic Device
PROM	Programmable Read-Only Memory
PWR	Pressurized Water Reactor
R/D	Research and Development
RIH	Reactor Inlet Header
ROH	Reactor Outlet Header
ROPT	Reactor Overpower Trip
RRS	Reactor Regulating System
SDS	Shutdown System
SDS1	Shutdown System No. 1
SDS2	Shutdown System No. 2
SG	Steam Generator
SIL	Safety Integrity Level
SUT	System Under Test
U.S. NRC	United States Nuclear Regulatory Commission
V&V	Verification and Validation
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

Nomenclature

a	reactivity insertion rate
A	reactivity feedback coefficient
B	reactivity feedback coefficient
β	faction of the single group delay neutrons in the total neutrons
β_i	fractions of one of the six delay neutron groups
c_i	concentration of one of the six delay neutron groups
e_E	relative error of the mean
E	mean of measured response time samples
γ	a / β
Δk	added reactivity by the change of the density or the temperature
K_{eff}	effective reactor multiplication constant
l	lifetime of the single group delay neutrons
l_i	lifetime of one of the six delay neutron groups
$\boldsymbol{L}$	$\gamma - t_{k1}$
λ	decay constant of the single group delay neutrons
λ_i	decay constant of one of the six delay neutron groups
ρ	reactivity
σ	standard deviation of the measured response time samples
σ_E	standard deviation of the mean
n_0	initial neutron flux density
n_j	maximum of neutron flux density in process j
n_k	maximum of neutron flux density in process k
$n(t)$	neutron flux density
$n(t)_{\max}$	maximum of the neutron flux density
$n_1(t)$	neutron flux density in time range ($0 \le t \le t_1$)
$n_2(t)$	neutron flux density in time range ($t_1 \le t \le 2t_1$)

P_{peak}	peak of the power surge
SP_V	voltage value of the setpoint
SP_b	binary value of the setpoint
Δt	$t_{k1} - t_{j1}$
t_1	shutdown initiation time
t_d	decision-making time of SDS1
t_{j1}	shutdown initiation time of process j
t_{jd}	decision-making time of SDS1in process j
t_{k1}	shutdown initiation time of process k
t_{kd}	decision-making time of SDS1in process k
t_r	time for an accident transient to reach the setpoint
$\boldsymbol{x}$	the appropriate variable (coolant density or temperature)

1 INTRODUCTION

A nuclear power plant (NPP) is a complicated system which utilizes nuclear fission energy to generate electricity. It has been proved to be an effective and clean way to provide energy to human society. However, both the fuel and the fission products are radioactive and could harm human health, if handled inappropriately. Thus, safety is always the top priority during the design, construction, and operation of an NPP. Nowadays, more and more technologies have the potential of improving NPP safety. This thesis focuses on improving the safety margins of NPPs using Field Programmable Gate Arrays (FPGAs). A brief introduction is given in this chapter to illustrate NPP safety issues, CANadian Deuterium Uranium (CANDU) NPPs, safety systems in CANDU NPPs, FPGA technology, and the motivations, objectives, as well as the research approaches taken in this thesis.

1.1 Safety issues in NPPs

Nuclear safety refers to managing the operational risk such that the probability of releasing radioactive materials or other hazards is kept at an acceptable level. It is always the top priority of NPPs since the results of nuclear accidents can cause severe public hazards and massive economic loss. More specifically, operational limits and safety requirements have to be established with the objective of keeping the risk associated with plant operation within the limits prescribed by government appointed independent nuclear safety regulators. Satisfaction of these limits and requirements demands reliable

and effective safety systems that are capable of ensuring safe operation, preventing severe accidents, and alleviating the accident consequences. Technical specifications are also declared for NPP systems and operation status such that the plant operation does comply with all the necessary limits and requirements.

1.1.1 Safety objectives and requirements in NPPs

According to the documentations released by the International Atomic Energy Agency (IAEA), all the requirements for minimizing the risks associated with NPPs are derived based upon three fundamental safety objectives [1]:

(1) **General nuclear safety objective:** To protect individuals, society and the environment from harm by establishing and maintaining in nuclear installations effective defences against radiological hazards;

(2) **Radiation protection objective**: To ensure that in all operational states radiation exposure within the installation or due to any planned release of radioactive material from the installation is kept below prescribed limits and as low as reasonably achievable, and to ensure mitigation of the radiological consequences of any accidents; and

(3) **Technical safety objective**: To take all reasonably practicable measures to prevent accidents in nuclear installations and to mitigate their consequences should they occur; to ensure with a high level of confidence that, for all possible accidents taken into account in the design of the installation, including those of very low probability, any radiological consequences would

be minor and below prescribed limits; and to ensure that the likelihood of accidents with serious radiological consequences is extremely low.

The latter two objectives are indeed complementary support to the general one, which indicate specific goals from two different aspects. Measures, like reactor regulating system (RRS) and digital control computers (DCCs), are taken to guarantee that these objectives are achievable at any of the plant's operational states. Although the NPP design is required to cut down the likelihood of plant states that could lead to radioactive releases, it has to be clearly indicated that the probability of an accident does exist. In the case of an accident, further measures, such as deployment of safety systems and post-accident systems, are necessary to keep the level of radioactive exposure as low as possible and mitigate subsequent radiological consequences.

To achieve the above three fundamental objectives, safety requirements are issued and applied to every lifecycle stage and every operational state of an NPP. These safety requirements cover design, operation, and decommission of an NPP. They are specified for each lifecycle stage from risk management, safety defence, principle technology, to human factors. These requirements are mandatory and documented as regulations for the nuclear industry.

At the design stage of a new NPP, comprehensive safety analysis is required to identify all the possible sources and evaluate the effects that radiation doses could bring to on-site workers, the public, and the environment. The design organization is required to ensure that the NPP is designed to comply with all the necessary safety regulations. The accomplished design should also pass an independent safety assessment before it can be

delivered for fabrication/construction. During the design process, a requirement so called "defence in depth" [2] shall be incorporated such that the NPP can maintain the integrity of physical barriers of radioactive materials. The defence in depth concept includes a series of levels of protection with a consideration of both accident and failure of certain barrier. It offers NPPs graded safety protection against various possibilities of transients, anticipated operational occurrences (AOOs), and accidents. Following such a concept, the design is required to be carried out through safety classification, general plant design, plant system design, equipment qualification, human factor evaluation, etc. Safety systems of NPPs, due to their importance to plant safety, are highly considered with more specific requirements. The operating organization, on the other hand, is also required to prescribe proper operating procedures and assure their execution.

1.1.2 Operation limits and safety margins

With the purpose of meeting the safety requirements, a comprehensive description of NPP operating status is provided by defining operational limits. These operational limits categorize the plant behavior into several domains and margins. As an example, the limits and margins used in CANDU NPPs are illustrated in Figure 1.1 [3]:

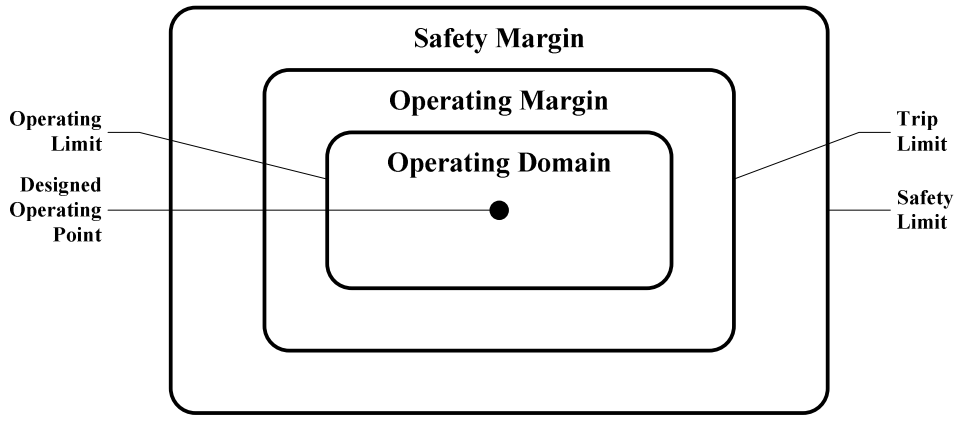


Figure 1.1 –Limits and margins of CANDU NPPs

As can be seen, the normal operation of a CANDU NPP is restricted within the "operating domain" by the trip limit (trip setpoint). While safety limit indicates the regulatory acceptance criteria. Violation of the safety limit can lead to severe accident such as fuel channel dryout, which may cause catastrophic consequences, say, core meltdown. In case of an accident, parameters representing reactor behavior, such as reactor power and temperature, will drift out of the operating domain and violate the trip limit. NPP safety systems then step in to execute reactor trip functions, preventing the safety limit of the reactor from being exceeded. With the consideration that it takes time to accomplish the trip process, the trip limit is defined lower than the safety limit. Two quantities, margin to trip and margin to dryout, are discussed in [4], giving a clear illustration of their relationship.

According to the official IAEA definition, safety margin is "the difference or ratio in physical units between the limiting value of an assigned parameter the surpassing of which leads to the failure of a system or component, and the actual value of that parameter in the plant" [5]. It plays an important role of transient buffer between the operating value and the regulatory acceptance criteria. Because it takes time for the accidental transients of operating parameters to overcome this buffer, the existence of safety margin allows safety systems to detect accidents, stop the dangerous progress, and mitigate major threatening consequences.

Variables within the reactor can change dramatically in the event of an accident. For example, in a large loss of coolant accident (LOCA) in CANDU, the positive reactivity, as a result of quick voiding of the primary heat transport (PHT) system, can be as high as +4.3 *mk* at 0.9 second into the accident [6]. As a consequence, the temperature and the

reactor power can elevate at an expeditious rate, which poses a serious threat to the reactor safety. Various accident analyses have been done to show how CANDU reactors mitigate severe accidents within the safety limits [7-11]. Safety margins buffer these accident transients and keep the plant safety under such undesired accident conditions. Due to its importance to the plant safety, safety margin is often utilized in NPPs for modifications and performance improvement [12].

1.1.3 NPP safety systems

It is strictly required that NPPs must be equipped with safety systems such that the plant safety is preserved even when an accident happens. Major functionality of the safety systems is to prevent the damage of physical barriers and the releasing of radioactive substances. Moreover, NPP safety systems have to mitigate the post-accident consequences such that the damage or harm caused by the accident is reduced to a level as low as possible.

No matter which reactor type is adopted in an NPP, its safety systems are normally categorized into reactor protection system, emergency core cooling system, and containment system with respect to their functions. The reactor protection system has the responsibility of shutting down the reactor once the reactor is threatened by abnormal transients, e.g. rapid increase of reactor power. Methods of shutting down the reactor include insertion of control/shutoff rods and injection of neutron poison. Either of them introduces rapid neutron absorption that leads to reactor shutdown. The emergency core cooling system provides extra coolant supply for both the core and the containment in case of undesired loss of coolant. The temperature is then kept at an acceptable level to prevent damage such as core melt. Failure of such safety systems can lead to severe

consequences, such as what happened in Fukushima NPP, Japan [13]. The containment system, including the fuel cladding, reactor vessel, and primary containment, is a group of physical barriers that prevent radioactive materials from being released to the environment. The containment system also possesses depressurization and exhausting equipments to strengthen the seal function.

1.2 Safety systems in CANDU NPPs

CANDU is a unique reactor type that were designed and developed by Atomic Energy Canada Limited (AECL) and Ontario Hydro since the early 1950s [14]. Its unique features, such as heavy water moderator, horizontal calandria, and on-line refueling, make it one of the most successful reactor types for commercial production of electricity [15]. Safety systems of CANDU are capable of detecting accident situations and mitigating the relevant consequences.

1.2.1 General information

Safety systems are deployed in CANDU NPPs to prevent catastrophic consequences resulting from accidents. Accident scenarios are detected and the reactor is shut down in a timely fashion. They are also in charge of dealing with the post-accident situation such as removing residual heat, refilling the fuel channel with coolant, preventing release of hazardous radioactive particles, etc.

Four fundamental safety functions are considered in CANDU NPP safety systems, which are consistent with international reactor safety design principles and Canadian safety requirements [16]. They are:

(1) To shutdown the reactor and maintain it in a safe shutdown condition;

(2) To remove decay heat from the fuel effectively;

(3) To maintain a barrier to limit radioactive release to the public and plant personnel; and

(4) To supply information necessary for the operator to monitor the status of the plant.

In order to achieve the above functions effectively, CANDU safety systems are categorized as shutdown systems, post-shutdown safety systems, and safety support systems.

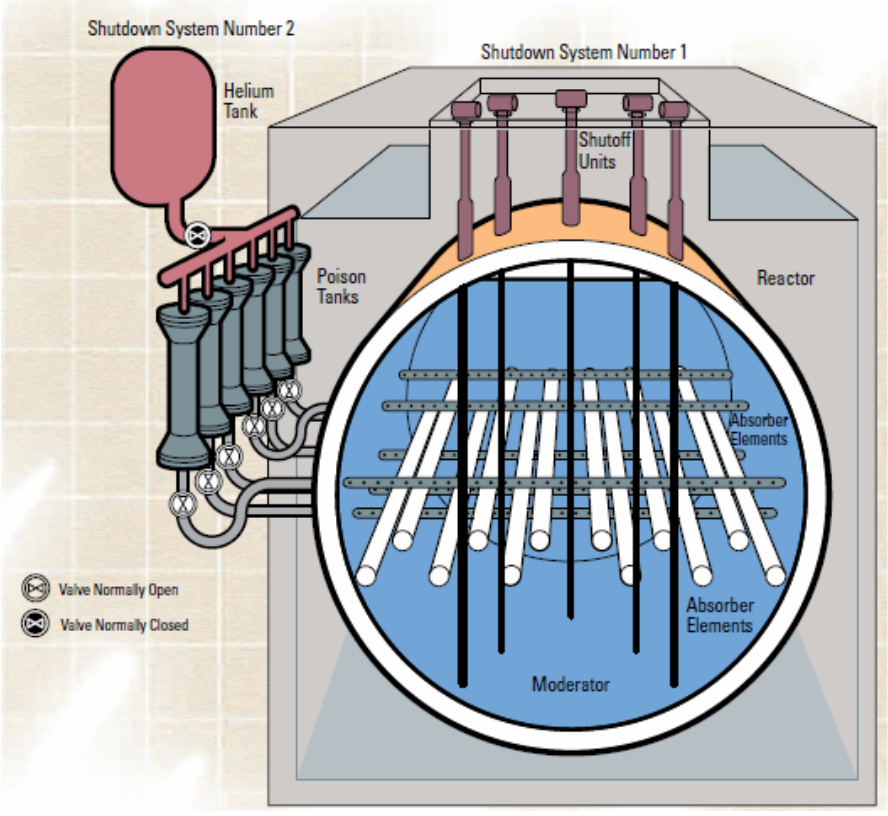


Figure 1.2 – CANDU SDS1 and SDS2

Shutdown systems are used to, as indicated by their names, shutdown the reactor before an accident causes serious damage to the plant. Figure 1.2 [17], describes the CANDU shutdown system No. 1 (SDS1) and shutdown system No. 2 (SDS2), respectively. SDS1 shuts the reactor down by inserting 28 shutoff rods from the top of the calandria, while SDS2 performs the shutdown action in a manner of rapid poison injection. When the reactor is shutdown, it is the responsibility of the post-shutdown systems to alleviate the consequences that has been caused by the accident, such as decay heat removal. The safety support system, which provides power and monitoring information for shutdown and post-shutdown purposes, works together with the above mentioned safety systems to assure a successful shut down process.

1.2.2 SDS1

All CANDU NPPs are required to be equipped with two independent and diverse shutdown systems, SDS1 and SDS2. Each shall be able to shutdown the reactor and keep the reactor subcritical such that any fuel failure mechanism shall not result in a loss of primary heat transport system integrity.

In CANDU 6 SDS1, there are totally 28 shutoff rods arranged in two banks with 14 rods each. They are located right above the top of the reactor so that gravity can be the driving force when a drop-down action is required.

As one of the safety systems in CANDU NPP, SDS1 has to meet strict requirements that are stipulated for these safety systems [18]:

(1) shutdown the reactor and keep it subcritical whenever necessary;

(2) have high availability;

(3) have online testing ability;

(4) have enough redundancy and independency; and

(5) perform its function on time whenever necessary.

According to the requirements documented by regulators, the unavailability of CANDU SDS1 is required to be less than 10^{-3} years per year, which means the fraction of time for which SDS1 is not available per year shall be demonstrated to be less than 10^{-3} years. The online testing ability is required to ensure the availability of SDS1 such that the testing of SDS1 can be carried out without a reduction in the effectiveness of the system. Sufficient redundancy and independency allow the SDS1 to remain functional when a failure of any single component in the SDS1 happens. On-time actuation of SDS1 is critical to plant safety since the consequence could be much worse with a delayed shutdown in an accident with rapid transient. The response time of SDS1 is the key factor that affects the shutdown speed. The shorter the response time is, the faster the SDS1 can shutdown the reactor, resulting in a lower power surge. Thus shortening the response time could help improve the safety features in the plant.

To obtain the mentioned qualifications, the SDS1 control is designed to be a triplicate, relay logic applied system [19]. There are a total of three trip channels (D, E, and F) with completely independent and physically separated power supplies, trip parameter sensors, instrumentation trip logic and annunciation. Each trip channel has exactly the same functionality. The reliability and availability criteria are met with the triple redundancy

while the online testing ability is allowed by the independence between each channel. Meanwhile spurious trips are also effectively prevented through a two out of three (2oo3) vote of the three outputs of the triple redundant trip channels. This majority voting logic permits the reactor trip signal to be released only when at least two trip channels are on trip status, which reduces the probability of a false trip decision.

SDS1 is one of the most important safety systems in CANDU NPPs since it provides an effective and reversible shutdown process. Due to its importance to the plant safety, there have been many efforts for SDS1 improvement, which leads to three evolutions [20]. With a purpose of enhancing plant safety, the current thesis work also focuses on improving SDS1 using digital hardware technology.

1.3 Research motivations

The motivations of using FPGA technology to improve CANDU SDS1 and further the NPP safety margin lie in several technical aspects: potential benefits of an improved safety margin, the problems that an existing CANDU SDS1 is facing, and FPGA advantages for SDS1 improvement. This thesis work is stimulated when FPGA has shown its superiority in some non-safety applications of nuclear industry [21]. At the same time, conventional safety system in existing CANDU NPPs are facing problems ranging from obsolescence resistance to regulatory approval difficulties. Preliminary investigations show that applying FPGA technology to CANDU SDS1 not only solve current technical problems, but also can lead to safer operation and even performance enhancement of the plant.

1.3.1 Safety margin improvement

Safety margin is a buffer between the normal operation and unacceptable system failure caused by an accident. A more conservative safety margin ensures higher tolerance to accident consequences. If SDS1 reacts to the accident with a shorter response time, the trip process will be initiated earlier and the transient surge of reactor parameters will be lower. Moreover, process variables such as temperature and pressure progress rapidly during accidents. Hence, the earlier the reactor is shutdown, the lighter the impact of the accident would be. For example, less heat is generated when the chain reaction is stopped earlier, which alleviates the post-accident recovery. Considering the fact that FPGA systems have the potential of faster processing speed than software-based ones for a given algorithm/logic, the safety margin improvement can be realized by a faster shutdown process via an FPGA-based shutdown system. Detailed validation of such a concept will be discussed in detail in Chapter 2 based on neutron dynamics analysis.

A further idea regarding to a faster shutdown is that the operating power of the plant can be upgraded without endangering the plant safety. Since the surge peak of an accident transient with a faster shutdown process is lower, power upgrade is allowed as long as the accidental surge peak remains within acceptable criteria. If the safety margin improvement with faster shutdown is validated, then there is a possible chance for the power upgrade. However, power upgrade not only depends on the realization of faster shutdown process, but also regulatory approval and other engineering considerations on related systems.

1.3.2 SDS1 performance

As one of the most important safety systems in CANDU NPPs, SDS1 takes critical responsibility of protecting the reactor. Since it is the first safety system that reacts to an NPP accident, there is a direct relationship between SDS1 performance and the NPP safety margin. Regulators require SDS1 to have the highest safety integrity level (SIL). Its performance is hence one of the key issues of NPP safety.

SDS1 is a standby system waiting to be called upon to shutdown the reactor. Therefore, 1) it should have high reliability when waiting for the call of duty; 2) it should react to the upset condition quickly and properly to mitigate the post-accident consequences; and 3) it should have firm obsolescence resistance since an NPP is built to be in service for decades. The software-based SDS1, however, is facing problems at meeting these requirements because of its inherent failure modes, serial processing pattern, and unavoidable reprogramming process for alternative platforms.

Inherent failure modes and difficulties of algorithm validation have burdened the regulatory approval process for software reliability and availability. In a microprocessor-based platform, task-distribution process and the serial processing pattern limit the overall processing speed. The obsolescence problem becomes more and more serious with microprocessor-based systems under rapid technology progress. These problems are offering a margin for SDS1 performance improvement. For this reason, SDS1 is chosen as the research topic of this thesis work to investigate how its performance can be improved and how the plant safety margins can be improved with a faster speed of response of the SDS1.

1.3.3 Advantages of using FPGAs

FPGAs have been widely utilized in applications where flexible and low cost digital hardware implementations are needed. This programmable semiconductor device contains a matrix of high density configurable logic blocks connected via programmable interconnects. Resorting to computer-based design tools, the logic design for FPGAs is essentially circuit-independent [22]. This unique feature enables a design to be transferred from one FPGA platform to another without going through redesign [23], which leads to potential enhancement of the obsolescence resistance of a system. A schematic view of an FPGA chip structure is shown in Figure 1.3.

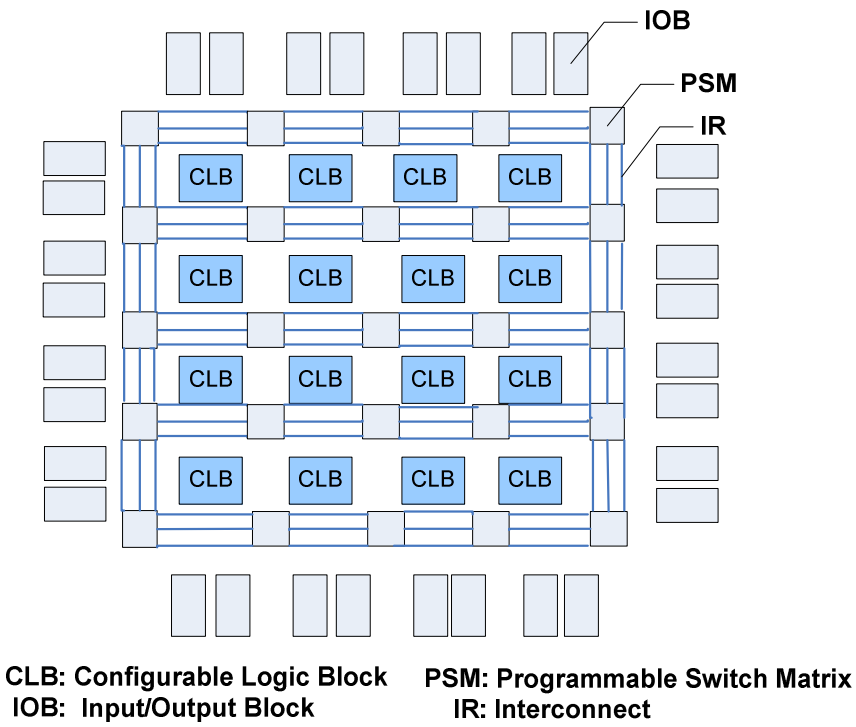


Figure 1.3 – Schematic view of an FPGA chip

It is important to point out that, in the design and implementation phase of any FPGA systems, Electronic Design Automation (EDA) tool kits which are operating system driven are involved. However, once the design and implementation phase is complete, the

final implemented product is a pure hardware system. It does not include software failure modes so that the regulatory approval process becomes less complex.

With the help of parallel processing and pure hardware implementation, FPGAs have the potential to achieve faster processing speed than software-based systems. Development of modern semiconductor technology has allowed the amount of logic elements in one FPGA chip to reach a million-gate level. This feature offers abundant resource for realizing parallel processing for all the similar logic steps, say, thousands of value range checking. Propagation delay and queuing time consumed in a serial processing system are eliminated and, hence a faster processing speed can be obtained. In a pure hardware implementation, no operating system exists. Even the memory access is not necessary if there are no complicated calculations. Logics that are to be processed then can be distributed to corresponding elements directly through pre-configured routes. Therefore, the results can be obtained at the output quickly. In previous applications of FPGAs, it was found the processing speed of FPGAs can be two to three orders of magnitude faster than pure software implementation for the same problem [24].

Having the capability of higher obsolescence resistance, easier regulatory approval, and faster processing speed, FPGAs have shown great potential for improving current NPP safety systems that are computer-based. How to realize an FPGA-based safety system and how the NPP safety features can be improved by this method are the main motivations for this thesis.

FPGA itself is not a brand new technology but has become more and more powerful for implementation of customized systems. Its logic elements capacity and processing speed

have been improved by several magnitude orders since it was invented in 1985, which now makes it possible for the replacement of software-based systems such as the existing SDS1.

As what have been introduced, FPGA has obvious advantages over software-based systems such as improved obsolescence resistance, easier approval procedure, and faster processing speed. Replacing those existing software-based systems, even safety-related systems in NPPs, with FPGA-based platform, can have these advantages fully utilized. As a consequence, the whole plant can benefit from these advantages to achieve a safer NPP.

1.4 Objectives, methodologies, and scope of research

Current thesis work focuses on: 1) exploring the speed of the shutdown systems and its impact on plant safety; 2) validating the concept of improving safety margin with faster shutdown process; 3) realizing the SDS1 trip logic that is currently implemented within a software-based system; 4) verifying and validating its performance; and 5) evaluating the improvement that can be realized. To accomplish the listed objectives, research methodologies are defined as well as the research scope.

1.4.1 Research objectives

Objectives of the work are defined for three major stages of the research procedure: 1) analysis for the plant accident behavior and the impact of faster shutdown process; 2) implementation of an FPGA-based SDS1; and 3) evaluation of the FPGA-based SDS1 and the safety margin improvement.

The analysis work concentrates on the accident scenarios and the related plant response. Analytical attempts are used to explore in detail the accidental transients within different shutdown processes. The objectives for the analysis work are defined below:

(1) Accident scenarios are to be set up as analysis objects; and

(2) The concept that the safety feature can be improved via a faster SDS1 is to be validated and verified based on the predefined accident scenarios;

For the FPGA implementation work, the focus is on: 1) the feasibility of a pure hardware implementation of the SDS1 trip logic; and 2) the effective utilization of FPGA advantages for the SDS1 implementation. Then the objectives are defined as follows:

(1) An FPGA-based SDS1 trip channel is to be implemented. The related Input/Output (I/O) ports are defined and connected to a simulation environment for performance evaluation;

(2) The functionalities of the designed FPGA-based SDS1 trip channel are validated under normal and accident conditions;

(3) A methodology for comparison of the speed of responses is established; and

(4) Comparisons are carried out under different NPP operating conditions.

For the evaluation of the safety margin improvement, expected outputs are an illustration of the benefits that a faster SDS1 can offer to the plant and a practical implementation that can show the proved improvement under certain accident scenarios. More specifically, the following issues are to be addressed:

(1) The benefits of shortening response time of the shutdown systems is to be validated quantitatively in terms of the safety margins of a CANDU NPP;

(2) A diverse FPGA implementation to achieve shortened response time and to validate the safety margin improvements in a simulation environment is to be demonstrated; and

(3) Other benefits as a result of shorten response time, more specifically, the potential power upgrade, while maintaining the improved safety margins is to be explored quantitatively.

1.4.2 Research approaches

To obtain the above objectives, suitable research approaches are determined through literature survey, assessment, and selection. Specific techniques are targeted to certain procedures for cost-effective results.

To validate the concept of safety margin improvement, thermalhydraulic analysis for accident transients is necessary. The analysis of transients based on distinct response time is capable of showing the improvement in a faster shutdown process against the slower one. With selected accident scenarios, an industry standard code, CATHENA [25], is used for such kind of analysis. A simplified reactor model and the accident scenarios are created for the thermalhydraulic simulation.

A standard FPGA development procedure is applied for the SDS1 implementation. A systematic design is drafted based on current SDS1 trip logic. Hardware coding,

simulation, synthesis, and configuration are performed by using industry standard development kit [26].

Hardware-in-the-loop (HIL) simulation [27] is chosen for the functionality and performance validation of the FGPA-based SDS1. With an industry grade NPP simulator available, the FPGA-based SDS1 can be tested by being connected to the simulator and acting as a trip channel that reacts to the simulated accidents. Real-time monitoring of variables and trip signals is then enabled. The functionality evaluation is then straightforward when the captured responses from the FPGA system are analyzed.

To statistically estimate the response speed of such an FPGA-based SDS1, Monte Carlo simulation [28] is selected. This is because the timing is not a fixed value due to measurement noise and equipment uncertainties. Applying this simulation method allows a more comprehensive description of the timing performance of the FPGA system, which is of importance to the safety margin improvement objective.

The thermalhydraulic simulations are utilized further to analyze the improvement based on evaluated timing performance of the FPGA-based SDS1. Transients of a worst-case accident are simulated using different response time of SDS1 to generate comparable results.

With the purpose of further verifying the effectiveness of the shortened response time and validating the safety margin improvement in a real-time environment, HIL simulation is again applied. Unlike the off-line CATHENA simulation, HIL simulation performs on-line performance evaluation and the performance of the tested system can be monitored in real time.

In summary, the research approaches adopted in this work are listed as following:

(1) Establish thermalhydraulic models for CATHENA simulations with specified accident scenarios that represent a typical worst case accident;

(2) Analyze the simulated transients to verify the "faster shutdown" concept and validate the performance improvement;

(3) Analyze the CANDU SDS1 trip logics and translate them into a suitable form for FPGA implementation;

(4) Use a simulator to validate the results of the implemented FPGA system;

(5) Use both deterministic and statistical methods to evaluate the performance of the FPGA-based implementation of SDS1 against its software-based implementations in PLCs;

(6) Perform the thermalhydraulic simulation for the worst case scenario again using the evaluated FPGA response time;

(7) Analyze transients of critical system variables based on the results of the thermalhydraulic simulation as a function of different shutdown response time to establish the baseline for evaluating the FPGA implementation;

(8) Compare the simulation results with different response times so that the characteristics of transients are identified as a function of response time;

(9) Describe how the safety margins can be improved with a faster decision-making process, as well as how this can be utilized for potential power upgrade; and

(10) Demonstrate the feasibility of this approach using an HIL simulation with an industry grade CANDU NPP simulator and to provide further verification and validation.

1.4.3 Research scope

Although safety margin improvement covers a wide range of considerations, the current thesis mainly focuses on the CANDU safety margin improvement via improved SDS1 resorting to FPGA technology. Necessary bounds are defined such that the research is under explicit direction and the accomplished work is oriented to specific results.

First of all, the research objectives are defined within CANDU NPPs. Both the safety margin and the SDS1 trip logic are analyzed based on existing CANDU technical information. Although other NPPs or even non-nuclear industry share the safety margin concept as well, such kinds of safety margins are not considered in this work.

Secondly, the improvement of SDS1 is focused on the shortening of its response time using digital hardware implementation. After being in service for decades, SDS1 can be potentially improved in many ways. However, this work exams only the shortening of response time as an objective, to which research effort is mainly paid.

Choosing an FPGA as the implementation platform is based on its verified advantages, especially the fast processing that can potentially increase the SDS1 response speed.

Focus of this part is only to evaluate the response time of an FPGA-based SDS1prototype. There is no plan to qualify such a prototype work for regulatory approval, including the software design tools used for FPGA design and implementation.

Some of the FPGA advantages indicated in this work are derived from comparison against current software-based system. The comparison is based on a survey of previously accomplished work. There is no intention to evaluate software-based system here to provide a performance comparison.

Current study does not have all the SDS1 trip parameters implemented since one process trip parameter is enough for functionality validation and response time comparison against software-based system. Proper responses of other parameter implementation are only redundant supports and do not account more for the research objectives. However, data cross verifications between multiple channels will not be considered.

Finally, the accident scenarios applied for safety margin analysis are obtained from previous CANDU safety analysis work. The CATHENA simulation is mainly based on a selected worst case scenario which is enough to show the safety margin improvement. It has to be pointed out that the overall evaluation of the plant safety margin needs thorough study for different accident scenarios. However, this will be beyond the scope.

1.5 Main contributions

Within the prescribed research scope, this thesis uses SDS1 as an example to show how FPGA-based safety-critical system can improve the safety margin of CANDU NPPs as

well as the feasibility for potential power upgrade. The main contributions of this thesis can be summarized as:

(1) A valuable reference for FPGA applications in NPP safety systems has been presented in the "Top-Down" design flow with special design techniques involved;

(2) Performance illustration of FPGA-based SDS1 has been given by the timing evaluation, which proves the advantages of applying FPGAs to NPP safety systems;

(3) Quantitative description of the safety margin improvement with faster shutdown process has been obtained through thermalhydraulic simulations;

(4) Analytical relationships between the response time and the critical transient parameters are derived as an evaluation of the response time effects;

(5) Potential power upgrade has been validated with thermalhydraulic simulations; and

(6) The safety margin improvement has been validated by on-line HIL simulations using an NPP simulator.

1.6 Organization of the thesis

The remainder of this thesis is structured as follows: Chapter 2 presents analytical discussion for safety margin improvement, FPGA applications in NPPs, and relevant literature reviews. Chapter 3 covers the thermalhydraulic analysis for the validation of

safety margin improvement. The SDS1 trip logic and its FPGA implementation process are discussed in Chapter 4. The main content of Chapter 5 is the evaluation of both the FPGA-based SDS1 and the potential safety margin improvement. The HIL simulation work is introduced in Chapter 6 to demonstrate the safety margin improvement within a realistic NPP environment, followed by Chapter 7 where the conclusions are drawn and future research directions are suggested.

2 NUCLEAR SAFETY AND FPGA APPLICATIONS IN NPPS

The objective of the current research work deals with safety issues in NPPs due to their significance to both the plants and public safety. This chapter covers the essentials of nuclear safety and relevant FPGA applications, including safety regulations and standards, safety margins, safety systems, why and how FPGA-based system can be and has been applied to NPPs, etc. Detailed literature review is also presented on these aspects.

2.1 Nuclear safety

The safety assurance of an NPP is to protect the on-site operating staff, the public, and the environment from the hazards of the radioactive substances. To achieve such a goal, both natural and engineered radiation barriers are deployed. The design, operation, and analysis of an NPP have to comply with strictly prescribed safety regulations and standards issued by regulators such that the nuclear safety objectives are achieved. Safety margin is defined for a plant parameter as a buffer between the operating value and the tolerance of the barriers. These crucial barriers can then survive in accidents to prevent release of radiological hazards. Safety analysis methods are developed and utilized to evaluate the plant behavior and safety margins. Safety systems are designed and installed in order to detect the initiating conditions of undesired abnormal situations and mitigate the consequences.

2.1.1 Regulations and standards

Significant efforts have been invested in designing reliable NPP safety systems to achieve the goal of safe and effective energy production. To satisfy the NPP safety demands, regulators and other national/international organizations, such as International Electrotechnical Commission (IEC) and IAEA, have developed guidelines and standards for the entire procedure of design, installation, and operation according to experiences and knowledge accumulated in decades.

(1) IEC standards

Among these organizations, IEC is well known for their meticulously developed IEC standards. For safety systems such as SDS1, where computer systems are involved, the standard named IEC-61508 provides corresponding requirements for their functional safety.

IEC-61508 is specifically developed to provide requirements and guidance for electrical, electronic, and programmable electronic (E/E/PE) systems that are used to carry out safety-related functions [29, 30]. It provides detailed lifecycle requirements for the system itself and its software along with the precise definitions, safety integrity requirement, and technique overview. In its general requirements, an overall framework of the lifecycle of safety-related systems is described using a flow chart. Each step of the lifecycle, such as risk analysis and system realization, is depicted with objective, scope, requirements, inputs, and desired outputs. Following the general requirements are the requirements for E/E/PE systems and software, respectively. Definitions and abbreviations are also indicated for the whole standard to obtain consistency.

Conformance to this standard is now an essential requirement by the regulators to the NPP research and development (R/D) procedure.

In addition to the IEC-61508 standard, there are two standards that are documented specially for NPPs: IEC-61513 and IEC-62138. IEC-61513 provides general requirements for NPP instrumentation and control (I&C) system important to safety [31], where both conventional hard-wired equipment and computer-based systems are considered. Requirements and recommendations for safety-related I&C systems are listed from overall architecture to each component. IEC-62138 focuses on the software aspects of computer-based systems that perform functional safety in NPPs [32].

Because of the popularity and effectiveness of IEC standards in NPP safety system R/D processes, they are considered as the minimum requirement for safety systems in NPPs. Each country develops its own regulations and guidance for nuclear safety based on related IEC standards.

(2) IAEA safety series

IAEA takes the responsibility of guiding the peaceful nuclear power utilization, including the NPPs and medical isotopes. To explicitly define, describe, and enforce the appropriate use of nuclear energy, IAEA publishes its safety series covering all the aspects of nuclear safety. For instance, safety standards for NPPs are developed and published for the reference of all the countries that have nuclear energy utilization purposes [33].

As for I&C systems in NPPs, including the shutdown systems, IAEA publishes relevant standards and guidance. Especially with the rapid development of digital systems, IAEA issues its specifications of requirements for NPP I&C systems [34] as well as the requirements for safety related NPP systems [35]. The development work for NPP safety systems follows a strict life-cycle process such that the proper functionality and acceptable quality are ensured. FPGA-based systems, as one of the digital systems that are being utilized for NPP I&C applications, have to follow these standards as well.

(3) Canadian classification of NPP safety requirements

Starting from 1946, Canada established its own nuclear safety regulator at the outset of its nuclear development plan. This regulator, Atomic Energy Control Board (AECB), had been working for decades to provide surveillance and administration for Canada's nuclear industry until it was replaced by a new government-organized one, Canadian Nuclear Safety Commission (CNSC). With the evolution of CANDU reactors, safety requirements are developed to provide clearly defined safety objectives and the approaches. Presently, there are complete and mature safety guidelines and requirements for entire CANDU lifecycle, such as the "General Nuclear Safety and Control Regulations" and "Requirements for Shutdown Systems for CANDU NPPs". These regulations set the standards how CANDU reactors should be designed, operated, maintained, and protected. For example, requirements for SDS1 define what criteria an SDS1 should meet to achieve the safety [36]:

(1) Seismic qualification;

(2) Environmental qualification including against jets crash and other dynamic loads;

(3) Unavailability of less than 10^{-3} years per reactor year;

(4) Fail-safe operation;

(5) On-line testing without impairing the normal operation;

(6) Manual initiation from the control room;

(7) Separation and independence of safety system channels from each other and from process systems; and

(8) Requirements applicable to safety support equipment.

Safety analysis criteria are also available to guide licensees in a proper manner of performing the required safety analysis of a nuclear facility [37]. Only with the satisfaction of such criteria can CNSC accept the analysis results when considering a licensing process. One thing that needs to be clarified is that CNSC evaluates the compliance of safety criteria also in association with other international standards, such as those from IAEA and IEC. Safety analysis in this thesis work takes these requirements into priority consideration.

2.1.2 Defence in depth

In fact, all the CANDU NPPs have extensive conventional safety programs which are much more stringent than that in other industrial facilities. The philosophy against hazards in NPP is to reduce the hazard levels to As Low As Reasonably Achievable (ALARA). Achievement in this aspect so far in Canada is that the radiation dose received by CANDU NPP onsite workers has been reduced by about a factor of 10 over the 40-50 years of plant operation [38]. With the rules listed as power control, fuel cooling, and

radioactivity containment, CANDU established its “Defence in Depth” safety concept. This concept assumes possible design flaws, equipment failures, as well as human errors. It then sets up a safety model to protect the plant from these threats using multiple barriers, reliable process systems, reliable safety systems, competent operating and maintenance staff, and failure detection/correction techniques.

To achieve the “Defence in Depth” goal and ensure safe and normal operation, NPPs require high reliability and availability of both process systems and safety systems. Several principles are followed during design and operation to meet the high reliability and availability requirements.

The first one is redundancy. Additional components are installed to the system to avoid whole system failure when one of the components is down. The redundant components increase the reliability and availability by providing a backup at possible single component failure. For example, both SDS1 and SDS2 have three redundant trip channels. By this means, the shutdown system maintains its function even when one or two of its trip channels are out of operation.

Another principle for NPP system design is independence, which means physical separation of systems or components. Independence prevents the failure happened in one system/component from affecting the others. As for the shutdown systems, all the three trip channels are independent from each other. This also helps online maintenance by allowing one channel to be tested without affecting the other two.

Diversity is also important to system reliability and availability. This attempt provides more than one way to realize a specific system function. Normally, the diversity systems

are even designed by different teams to avoid potential duplicated defects. CANDU NPPs have two shutdown systems which can shutdown the reactor using two different methods. Therefore, even when an unexpected situation stops SDS1 from functioning, SDS2 is still able to shutdown the reactor since it monitors the similar trip parameters and trips the reactor in a totally different way.

Periodic testing increases the reliability and availability by detecting failures that exist in standby system, e.g. shutdown system. A failure in the shutdown system will not be noticed until it is called for its function. The consequence of an unavailable shutdown system due to undetected failure is absolutely unacceptable by the NPP safety requirements. Thus, the periodic testing is of importance to avoid this kind of undesired scenario.

To gather information of the NPP systems for safety concern, operational surveillance is applied to provide continuous monitoring and ability of detecting potential problems. A flaw can then be detected and corrected before it becomes real threat to plant safety.

Fail safe operation is a critical feature of safety systems in NPPs. It leaves the system in a safe state after failure happens. Thus, the safety is not jeopardized when the system faces a failure. A good example is the clutches that hold the shutoff rods in SDS1. The shutoff rods are released not only by the trip signal but also by a failure of the clutch power supply. The reactor is then shutdown to conservatively protect the plant in such a case.

Preventive maintenance and predictive maintenance are methods that are taken in advance to prevent system failure in the NPPs. Reliability data and other related information are collected as estimation inputs of the maintenance judgment. It offers NPP

systems an opportunity to correct the problem through maintenance rather than suffers a system failure.

All the above mentioned principles and techniques are applied together to achieve NPP safety objective. Due to its importance to the plant safety, shutdown systems, as what have been introduced and discussed previously, have adopted most of these features to ensure the plant is not endangered at accident scenarios.

2.2 Safety margins

2.2.1 An overview

As introduced previously, safety margin plays an important role of transient buffer between the operating value and the regulatory acceptance criteria. Because it takes time for the accidental transients of operating parameters to overcome this buffer, the existence of safety margin allows safety systems to react to accidents, stop the dangerous progress, and mitigate major threatening consequences. Figure 2.1 [5] shows a brief illustration of such a concept with two estimation methods: conservative calculation and best estimate calculation plus uncertainty bound.

Most important safety margins relate to physical barriers against release of radioactive substances, such as fuel matrix and fuel cladding. Regulators always confirm safety margin to be an indispensable issue of NPP safety [39-41]. It should be clearly indicated that the safety margin is not exclusive to nuclear industry. It has been applied to wherever risks are involved. Therefore, experience and knowledge from other industries about safety margin are worth considering.

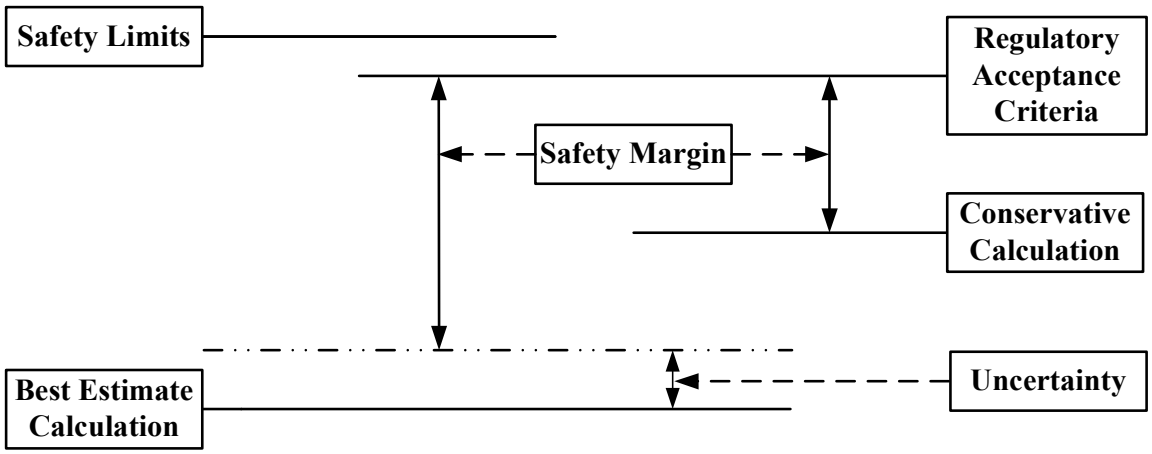


Figure 2.1 –Concept of safety margins and uncertainties

By definition, the safety margin is determined by the gap between the operating value and the acceptance criteria. However, the actual value is difficult to determine in many practical cases. That is why uncertainty exists within the best estimate calculation method and the conservative calculation has to take the highest possible uncertainty into account. Hence, the precise safety margin cannot be confirmed easily. Practically, safety margin is usually considered as the difference in physical units between the regulatory acceptance criteria and the calculated value of the relevant parameter [5].

2.2.2 Safety margin improvement through faster shutdown process

The safety margin can be improved by a faster shutdown process in a manner of shortening the response of safety systems. The principle of the investigated technique lies in the relationship between the accidental transients and the shutdown speed, which is illustrated using neutron dynamics theory and relevant analysis.

(1) Neutron dynamics basics

In a nuclear fission reactor, the chain reaction is sustained by generating the same number of neutrons as those that have been absorbed, leaked, and utilized for current fission. The

production of neutrons can be described using a factor so called effective reactor multiplication constant K_{eff} , which is defined as:

$$K_{eff} \equiv \frac{Total \quad Number \quad of \quad Current \quad Generation \quad Neutrons}{Total \quad Number \quad of \quad Last \quad Generation \quad Neutrons} \tag{2.1}$$

When K_{eff} is less than 1, the reactor is subcritical, which means the amount of the neutrons in the reactor is decreasing and the fission will eventually stop. When K_{eff} is greater than 1, the reactor is supercritical, which means more neutrons are produced than lost and the reactor power rises. Only when K_{eff} is equal to 1 will the reactor remain at a critical state.

In reactor physics, a quantity that is closely related to K_{eff} is used more often. It is called reactivity and defined as:

$$\rho \equiv \frac{K_{eff} - 1}{K_{eff}} \tag{2.2}$$

It is the relative net neutron production between two generations, which can indicate the reactor criticality status more intuitively since it is of opposite sign of subcritical and supercritical:

$$\rho < 0 : subcritical; \quad \rho = 0 : critical; \quad \rho > 0 : supercritical.$$

During fission reactions, some neutrons are released immediately, which are called prompt neutrons. Others are released shortly after the fission when the fission products decay and are called delayed neutrons. These fission products are named precursors and

normally categorized into six delay groups according to their decay time. Their decay constants, fractions of their delay neutrons, lifetime, and concentration are denoted as λ_i, β_i, l_i, and c_i.

One approximation commonly utilized in neutron dynamic analysis is to treat all delay neutrons as one group. In such an approximation, quantities describing the original six groups are simplified to only describe the single group.

The faction of the single group delay neutrons in the total neutrons is annotated as β:

$$\beta = \sum_{i=1}^{6} \beta_i \tag{2.3}$$

The average lifetime of all the precursors is a weighted average value:

$$l = \sum_{i=1}^{6} \beta_i l_i / \beta \tag{2.4}$$

The decay constant of precursors in a single delay neutron group approximation is then:

$$\lambda = \beta / (\sum_{i=1}^{6} \beta_i l_i) \tag{2.5}$$

(2) Neutron density transient as a function of reactivity changes

When positive reactivity is introduced into a reactor that is at the steady-state, the reactor is forced to produce a transient which is described in [42] with simplified consideration of a point kinetic reactor model and single delay neutron group:

$$n(t) = \frac{n_0}{\beta - \rho}\left[\beta \exp(\frac{\lambda\rho}{\beta - \rho}t) - \rho \exp(-\frac{\beta - \rho}{l}t)\right] \tag{2.6}$$

where,

$n(t)$ is the neutron flux density, which is proportional to the reactor power;

n_0 is the initial neutron flux density;

β is the delay neutron fraction;

ρ is the introduced step reactivity;

λ is the decay constant of the delayed neutron group; and

l is the neutron lifetime.

Equation (2.6) illustrates the transient of neutron density after the introduction of extra reactivity. The second term in the right side decreases rapidly after the start of the transient since it is related to the prompt neutrons. The first term then becomes dominant. This gives an exponential increase in reactor power after the step reactivity increase. The bigger the step reactivity is, the more expeditiously the transient will rise. Hence, in a LOCA of CANDU, the void-introduced positive reactivity can cause the reactor power to elevate exponentially.

In an NPP, when the quickly rising transients of critical parameters exceed the predefined trip thresholds, safety systems take action to shutdown the reactor by means of injecting a large amount of negative reactivity. Up to 80 *mk* of negative reactivity can be inserted to the CANDU reactor core by SDS1in order to neutralize the effect of introduced positive reactivity. The inserted negative reactivity is so large that its earlier insertion can effectively stop the exponential increase in neutron flux density and significantly mitigate

the transient. Typically, the faster the shutdown action is, the sooner the rising trend of transient will be slowed down and the lower the surge peak will be. As a result, the gap between the safety limit and the surge peak is widened, which translates into a higher safety margin. Implementing a faster shutdown process then turns out to be an effective method for safety margin improvement.

To analytically describe an accident-shutdown process, Equation (2.6) is not applicable any more. The reasons are: 1) there are two reactivity insertion processes; 2) reactivity inserted into the core by either process is relatively large; and 3) the inserted reactivity is a function of time and cannot be adequately approximated by a step change.

(3) Accident-shutdown analysis using PJA

To analyze the accident-shutdown process, an available method is the prompt jump approximation (PJA), which has been widely used for approximated reactor calculations [43-45]. In such an approximation, the transient caused by the reactivity interference within a very short time interval is considered as a "prompt change". It assumes that, within an extremely short interval, the reactor has instant response to the inserted reactivity. It is an ideal assumption in mathematical consideration but does provide an accurate approximation to the neutron transient. As a matter of fact, the response time of neutron flux density is in the order of 10^{-4} second, which can be approximated to 0, i.e. a prompt response.

PJA is utilized here to analyze the accident-shutdown scenario such that the difference between shutdown processes, especially the difference between surge peaks, can be

analytically described. Since it is only a concept demonstration, reasonable assumptions are adopted to simplify the analysis.

First of all, the overall reactivity transient, including all potential reactivity feedback, is considered as a linear function in both accident and shutdown processes. It is reasonable because these two processes are all accomplished very quickly such that linear functions are capable of well approximating these non-linear reactivity insertions in a short period.

Secondly, for the convenience of solving neutron dynamic equations, the two linear reactivity insertion processes are set to have the same slope, i.e. the rate of reactivity increasing in the accident is identical to that of reactivity decreasing in the shutdown. This is again due to the concept validation purpose. The curve that describes the reactivity transient of such a case is presented in Figure 2.2 in which the accident is set to happen at $t = 0\ s$.

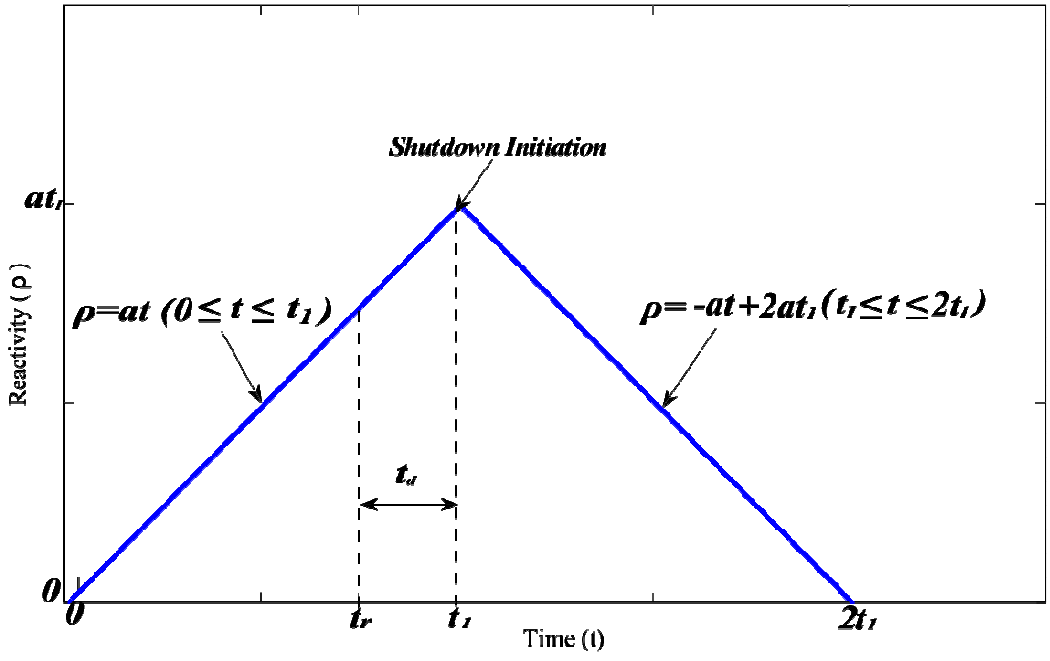


Figure 2.2 – Reactivity insertion in accident-shutdown process

Once the shutdown process starts, a large amount of negative reactivity is introduced into the reactor such that the overall reactivity begins to drop. Thus in the current study, t_1 in Figure 2.2 is considered as the initiation time of the shutdown process, which in turn is taken as the shutdown system response time since the accident is assumed to start at $t = 0\,s$.

As what is illustrated in Figure 2.2, the accident introduced reactivity rises at a rate of a. At time t_1 the shutdown process is initiated and the reactivity decreases at the same rate. The reactivity, as a function of time, is presented below in Equation (2.7).

$$\rho(t) = \begin{cases} at & (0 \le t \le t_1) \\ \\ a(2t_1 - t) & (t_1 \le t \le 2t_1) \end{cases} \tag{2.7}$$

The shutdown response time t_1 is the time needed by the shutdown system before initiating negative reactivity insertion. It consists of two parts: the rising time t_r for the reactor parameter, such as neutron power, to reach predefined shutdown threshold and the decision-making time t_d of the trip logic. Both of them are shown in Figure 2.2 as well.

In 1985, Ott and Neuhold had derived the neutron flux density equations based on such a scenario using point kinetics reactor model and single delay neutron group [46], which is listed in Equations (2.8) and (2.9).

$$n_1(t) = \frac{n_0 \beta}{\beta - at} \exp\left\{-\lambda\left[t + \frac{\beta}{a}\ln(1 - \frac{a}{\beta}t)\right]\right\} \qquad (0 \le t \le t_1) \tag{2.8}$$

$$n_2(t) = \frac{n_0\beta}{\beta - a(2t_1 - t)} \exp\left\{-2\lambda\left[t_1 + \frac{\beta}{a}\ln(1 - \frac{a}{\beta}t_1)\right] + \lambda\left[(2t_1 - t) + \frac{\beta}{a}\ln(1 - 2\frac{a}{\beta}t_1 + \frac{a}{\beta}t)\right]\right\} \qquad (t_1 \le t \le 2t_1) \tag{2.9}$$

where $n_1(t)$ and $n_2(t)$ are neutron flux density for different time range, and $n_1(t_1) = n_2(t_1)$.

Equation (2.8) provides a method to determine the rising time t_r since the negative reactivity insertion starts after the trip threshold is reached. Assuming the reactor is in full power when the accident happens at $t = 0$ s and the predefined trip threshold is 110% full power, t_r can then be decided by solving Equation (2.10) below.

$$110\%n_0 = \frac{n_0\beta}{\beta - at_r} \exp\left\{-\lambda\left[t_r + \frac{\beta}{a}\ln(1 - \frac{a}{\beta}t_r)\right]\right\} \qquad (0 \le t_r \le t_1) \tag{2.10}$$

Equation (2.10) turns to be

$$\frac{a\lambda t_r}{a + \lambda\beta} + \ln\left(1 - \frac{a}{\beta}t_r\right) + \frac{a\ln(1.1)}{a + \lambda\beta} = 0 \tag{2.11}$$

Taylor series indicate that

$$\ln(1 + x) = \sum_{i=1}^{\infty} \frac{(-1)^{i+1}}{i} x^i \qquad \forall x \in (-1,\ 1]$$

Terms in which $i \ge 2$ are negligible when $0 < x \ll 1$.

Since $0 < \frac{a}{\beta}t_r \ll 1$, Equation (2.11) turns to be

$$\frac{a\lambda t_r}{a+\lambda\beta} - \frac{a}{\beta} t_r + \frac{a \ln(1.1)}{a+\lambda\beta} = 0 \tag{2.12}$$

The solution of (2.12) is

$$t_r = \frac{\beta}{a} \ln 1.1 \tag{2.13}$$

As for the power surge peak decision, both Equations (2.8) and (2.9) are investigated.

Let the exponential term in Equation (2.8) be $E_1(t)$, then for $(0 < t \le t_1)$

$$\frac{dn_1}{dt} = n_0 \beta \frac{\frac{dE_1(t)}{dt}(\beta - at) - (-a)E_1(t)}{(\beta - at)^2}$$

where

$$\frac{dE_1(t)}{dt} = E_1(t)\left[-\lambda\left(1 + \frac{\beta}{a}\frac{-\frac{a}{\beta}}{1-\frac{a}{\beta}t}\right)\right] = E_1(t)\left(\frac{\lambda\beta}{\beta - at} - \lambda\right)$$

Thus

$$\frac{dn_1}{dt} = n_0 a\beta \frac{\lambda t + 1}{(\beta - at)^2} E_1(t) > 0 \quad (0 < t \le t_1) \tag{2.14}$$

Equation (2.14) shows that $n_1(t)$ is a monotonic increasing function with its maximum appears at $n_1(t_1)$.

Let the exponential term in Equation (2.9) be $E_2(t)$, then

$$\frac{dn_2}{dt} = n_0\beta \frac{\frac{dE_2}{dt}(at - 2at_1 + \beta) - aE_2(t)}{(at - 2at_1 + \beta)^2} \qquad (t_1 \le t \le 2t_1)$$

where

$$\frac{dE_2}{dt} = \lambda E_2(t)(-1 + \frac{\beta}{a}\frac{\frac{a}{\beta}}{1 - 2\frac{a}{\beta}t_1 + \frac{a}{\beta}t}) = E_2(t)(\frac{\lambda\beta}{at - 2at_1 + \beta} - \lambda)$$

Thus,

$$\frac{dn_2}{dt} = -n_0 a\beta \frac{(\lambda t - 2\lambda t_1 + 1)}{(at - 2at_1 + \beta)^2} E_2(t) \tag{2.15}$$

Since $t \ge t_1$, it follows that

$$\lambda t - 2\lambda t_1 + 1 \ge \lambda t_1 - 2\lambda t_1 + 1 = 1 - \lambda t_1 > 0 \quad (\lambda > 0, \quad 0 < t_1 < 1)$$
$$\Rightarrow \frac{dn_2}{dt} < 0 \quad (t_1 \le t \le 2t_1)$$

which means $n_2(t)$ is a monotonic decreasing function and have its maximum appears at $n_2(t_1)$.

It is now proved that $t = t_1$ is the peaking moment and the maximum of $n(t)$ is:

$$n(t)_{\max} = n_1(t_1) = n_2(t_1) = \frac{n_0\beta}{\beta - at_1}\exp\left\{-\lambda\left[t_1 + \frac{\beta}{a}\ln\left(1 - \frac{a}{\beta}t_1\right)\right]\right\} \tag{2.16}$$

Equation (2.16) indicates that for PJA method, the surge peak appears when the negative reactivity is inserted at the shutdown initiation. This is an approximate description using the single delayed neutron group PJA method. Although the six delayed neutron groups PJA gives more realistic results, Equation (2.16) is accurate enough to be used in the current conceptual validation purpose.

To mitigate the post-accident consequences, i.e. to reduce the extra heat generation after the accident, one can insert the negative reactivity either quickly after the shutdown initiation or earlier after the trip threshold is reached. The former implies a greater reactivity insertion rate a at $t \geq t_1$, which cannot be reasonably approximated by the PJA method discussed previously. The latter means faster response of the shutdown system, which is also the objective of current study.

To compare two shutdown processes, j and k, that have different shutdown decision-making time t_{jd} and t_{kd} $\left(t_{jd} < t_{kd}\right)$, transient peak values of these two neutron flux densities (n_j and n_k) are calculated and compared. The peaking time t_{j1} and t_{k1} are expressed as:

$$t_{j1} = t_r + t_{jd}; \qquad t_{k1} = t_r + t_{kd}$$

The two peak values are now:

$$n_j = \frac{n_0 \beta}{\beta - a t_{j1}} \exp\left\{-\lambda\left[t_{j1} + \frac{\beta}{a}\ln\left(1 - \frac{a}{\beta} t_{j1}\right)\right]\right\} \tag{2.17}$$

and

$$n_k = \frac{n_0\beta}{\beta - at_{k1}} \exp\left\{-\lambda\left[t_{k1} + \frac{\beta}{a}\ln\left(1 - \frac{a}{\beta}t_{k1}\right)\right]\right\} \tag{2.18}$$

According to the SDS1 specifications of CANDU NPP [47], the maximum allowed decision-making time of SDS1 is 0.1 *s*, which is part of a standard SDS1 response time. By assigning t_{k1} the maximum allowed response time, it is then possible to investigate the advantage of a shutdown process that has shorter decision-making time than 0.1 *s*. Let $t_{kd} = 0.1\ s$ and the peak time of process *k* is then illustrated by applying Equation (2.13):

$$t_{k1} = t_r + t_{kd} = \frac{\beta}{a}\ln 1.1 + 0.1 \tag{2.19}$$

The ratio between the two peak value n_j and n_k is now

$$\frac{n_j}{n_k} = \frac{\dfrac{n_0\beta}{\beta - at_{j1}} \exp\left\{-\lambda\left[t_{j1} + \dfrac{\beta}{a}\ln\left(1 - \dfrac{a}{\beta}t_{j1}\right)\right]\right\}}{\dfrac{n_0\beta}{\beta - at_{k1}} \exp\left\{-\lambda\left[t_{k1} + \dfrac{\beta}{a}\ln\left(1 - \dfrac{a}{\beta}t_{k1}\right)\right]\right\}}$$

$$= \frac{\beta - at_{k1}}{\beta - at_{j1}} \exp\left\{\lambda\left[t_{k1} - t_{j1} + \frac{\beta}{a}\ln\left(\frac{1 - \dfrac{a}{\beta}t_{k1}}{1 - \dfrac{a}{\beta}t_{j1}}\right)\right]\right\} \tag{2.20}$$

$$\left(\frac{\beta}{a}\ln 1.1 < t_{j1} < t_{k1} = \frac{\beta}{a}\ln 1.1 + 0.1\right)$$

It is clear that

$$\frac{\beta - at_{k1}}{\beta - at_{j1}} < 1, \quad (t_{j1} < t_{k1}) \tag{2.21}$$

As for the exponential part, let

$$g = t_{k1} - t_{j1} + \frac{\beta}{a}\ln\left(\frac{1-\frac{a}{\beta}t_{k1}}{1-\frac{a}{\beta}t_{j1}}\right)$$

and

$$t_{k1} - t_{j1} = \Delta t, \quad \beta/a = \gamma > 0, \quad (0 < \Delta t < 0.1)$$

Then

$$g(\Delta t) = \Delta t + \gamma \ln\left[\frac{1-\frac{1}{\gamma}t_{k1}}{1-\frac{1}{\gamma}\left(t_{k1}-\Delta t\right)}\right] = \Delta t + \gamma \ln\left(\frac{\gamma - t_{k1}}{\gamma - t_{k1} + \Delta t}\right) \quad (0 < \Delta t < 0.1) \qquad (2.22)$$

It is easy to verify that Equation (2.22) is a monotonic decreasing function with an initial value 0:

$$g(0) = 0 + \gamma \ln\left(\frac{\gamma - t_{k1}}{\gamma - t_{k1} + 0}\right) = 0 + \gamma \ln 1 = 0$$

$$g'(\Delta t) = 1 + \gamma \frac{1}{\frac{\gamma - t_{k1}}{\gamma - t_{k1} + \Delta t}} \cdot \frac{-(\gamma - t_{k1})}{\left(\gamma - t_{k1} + \Delta t\right)^2} = 1 - \frac{\gamma}{\gamma - t_{k1} + \Delta t}$$

$$\because \quad t_{k1} = t_{j1} + \Delta t > \Delta t$$
$$\therefore \quad -t_{k1} + \Delta t < 0$$
$$\Rightarrow \gamma - t_{k1} + \Delta t < \gamma$$

$$\Rightarrow \frac{\gamma}{\gamma - t_{k1} + \Delta t} > 1$$

$$\Rightarrow g'(\Delta t) = 1 - \frac{\gamma}{\gamma - t_{k1} + \Delta t} < 0$$

Since $g(\Delta t)$ is a monotonic decreasing function with an initial value 0,

$$g(\Delta t) < 0 \quad (0 < \Delta t < 0.1) \tag{2.23}$$

Equation (2.23) proves that the index of the exponential part in (2.20) is less than 0 since λ is positive as the decay constant of the precursor group. Thus, substituting Equation (2.21) and Equation (2.23) back to Equation (2.20) yields

$$\begin{aligned} &\frac{n_j}{n_k} < 1, \quad \left(\frac{\beta}{a} \ln 1.1 < t_{j1} < t_{k1} = \frac{\beta}{a} \ln 1.1 + 0.1 \right) \\ &\Rightarrow n_j < n_k \end{aligned} \tag{2.24}$$

From a neutron dynamics perspective, (2.24) analytically proves that for the given response time t_{j1} and t_{k1}, $(\frac{\beta}{a} \ln 1.1 < t_{j1} < t_{k1})$, the transient surge peak of a faster shutdown process is lower. That is to say, it is feasible to have a larger safety margin by shortening the response time of SDS1.

A specific example, i.e. a large LOCA, can be used to intuitively illustrate the concept.

Let

$$L = \gamma - t_{k1},$$

then

$$g(\Delta t) = \Delta t + \gamma \ln \left(\frac{L}{L + \Delta t} \right)$$

β of U-235 is 0.0065 [42]. For the specific large LOCA in CANDU, value of a can also be approximately estimated:

$$a = 0.0043 / 0.9 \cong 0.0048 \quad k / s \text{ [6]},$$

which leads to $L = 1.1251 \quad s / k$.

Thus

$$g(\Delta t) = \Delta t + \gamma \ln\left(\frac{L}{L+\Delta t}\right) = \Delta t + \frac{0.0065}{0.0048}\ln\left(\frac{1.1251}{1.1251+\Delta t}\right) = \Delta t + 1.3542\ln\left(\frac{1.1251}{1.1251+\Delta t}\right) \quad (2.25)$$

Plotting Equation (2.20) with substituted Equation (2.25) gives Figure 2.3.

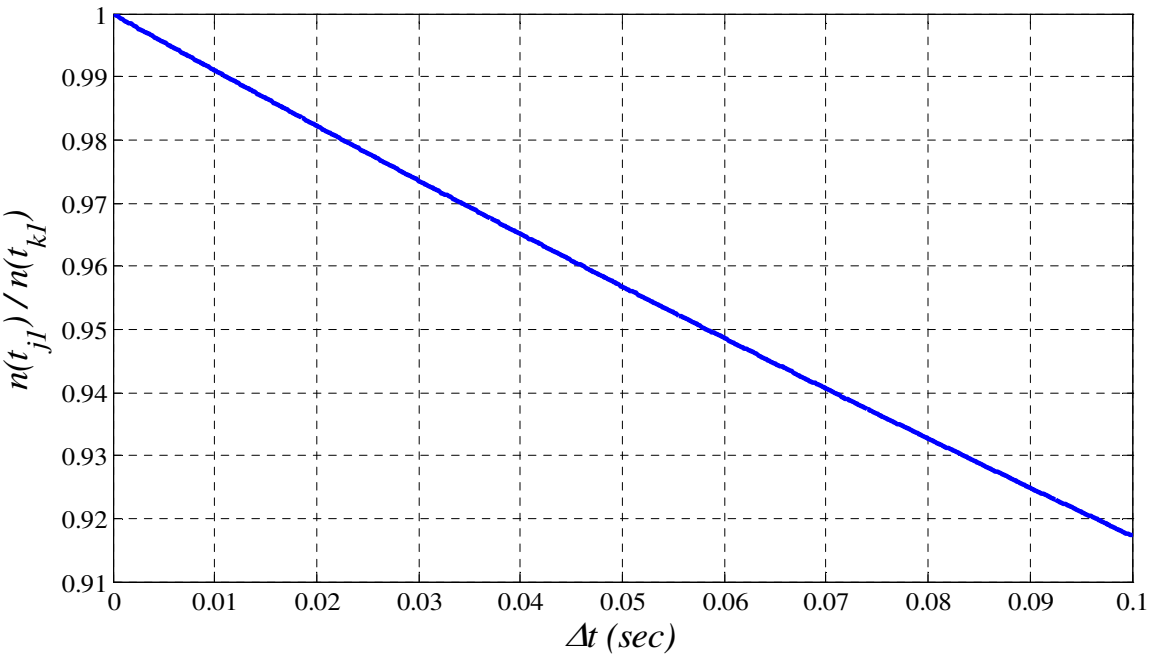


Figure 2.3 – Surge peak ratio of LOCA transients (PJA)

Figure 2.3 quantitatively illustrates how the peak ratio in a postulated LOCA varies with the difference between two shutdown processes. Increasing Δt represents faster response in shutdown process *j*. As it can be seen, if the decision-making time of process *j* can be

shortened to be 0.03 s, i.e. $\Delta t = 0.07\,s$, the peak value can be reduced to be about 94% of that of process k. A 6% safety margin improvement is then realized, which can contribute to the enhancement of the plant safety in postulated accident scenarios.

To explore how the reactivity insertion rate a affects the peak value ratio, different values of a are assigned to Equation (2.22), which gives corresponding parameters listed in Table 2.1:

Table 2.1 Relevant parameter values based on *a*

***a* (k/s)**	**γ (s/k)**	**t_{k1}(s)**	***L*(s/k)**
0.006	1.0833	0.2032	0.8801
0.003	2.1667	0.3065	1.8602
0.001	6.5	0.7195	5.7805

* For U-235: $\beta = 0.0065;\ \ \lambda = 0.078\ \ s^{-1}$

Based on the parameters in Table 2.1, the surge peak ratios decided by Equation (2.20) are plotted in Figure 2.4. The plotted data illustrates the sensitivity of the surge peak ratio to the reactivity insertion rate a. As what can be seen, the faster the reactivity is inserted, the faster the ratio changes with Δt. It means the difference between the two surge peaks is more notable in the fast reactivity change scenario. One can then predict that the surge peak difference is more obvious for a more severe accident in which the reactivity changes dramatically.

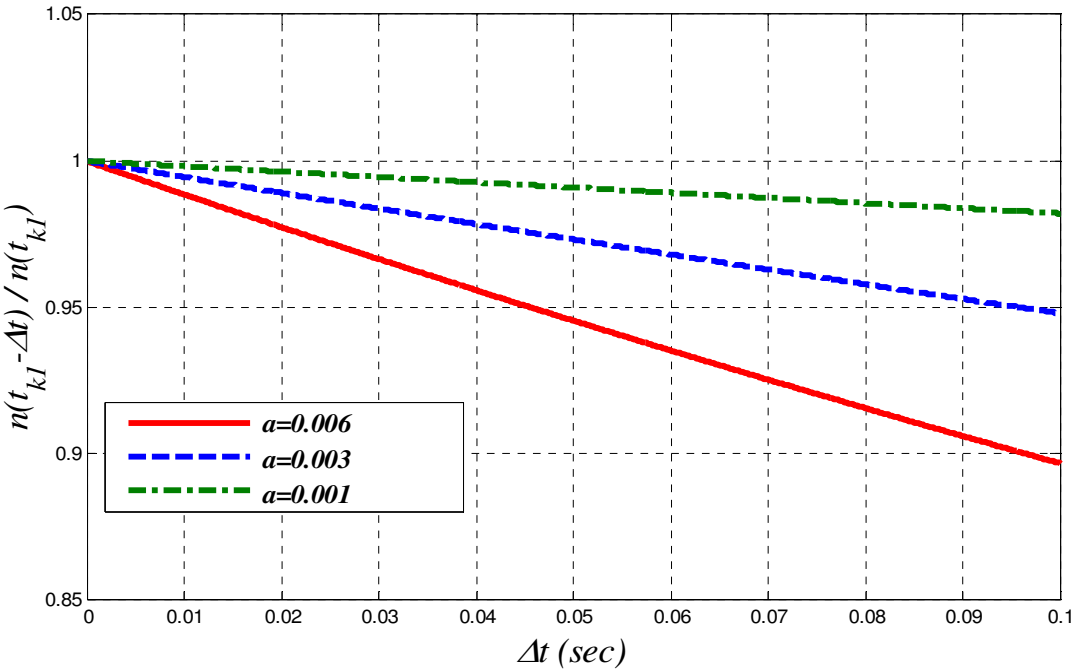


Figure 2.4 – Surge peak ratios on different *a*

Improvement of safety margins with faster shutdown system also provides opportunities for potential power upgrade of the operating NPPs. Since the safety margin of the system is directly related to the speed of the shutdown action, a faster shutdown system can potentially limit the peak of the accidental surge below the safety limit when the operating power is upgraded. Power upgrade is a cost-effective method for NPPs to increase their MW rates, which has been realized in U.S. successfully [48]. However, most of the accomplished power upgrade projects are based on license renewal, uncertainty reduction, equipments capacity enhancement, etc [49]. These methods are either based on complicated license re-evaluation or investment to upgrade equipment. With the availability of mature FPGA technology, the faster shutdown process can indeed be realized with easier regulatory approval, strong obsolescence resistance, and relatively lower cost.

2.3 CANDU SDS1

In this work, CANDU SDS1 is used as an example to investigate the feasibility of realizing faster shutdown with FPGA technology. Research work here is focused on shortening the response time such that SDS1 can react faster.

2.3.1 Evolutions

In the early 1950s, the shutdown systems in CANDU reactors used very simple design. The prototypes of CANDU reactors, Nuclear Power Demonstration and Douglas Point, used a "dump tank" which drains the heavy water moderator and pumps it back to the PHT loop to provide negative reactivity [50]. The design of the gravity-drop mechanical shutoff rods (the prototype of the current SDS1) was first added into shutdown system in Pickering-A design [51]. The trip logic of SDS1 was firstly based on relay circuit and analog comparators [52]. After being in service for decades, all these designs are facing aging and digitization challenges. In the early 1980s, CANDU NPPs started replacing their conventional relay logic and analog devices in safety systems with digital computers [53]. The software-driven shutdown system in Canada was first developed and deployed in Darlington NPP [54]. The SDS1 trip logic was turned into digital computer based design (PDCs) in the CANDU 6 model (started in Pt. Lepreau and Gentilly-II in 1982) [55]. Recently, PLCs are also used to serve as shutdown system controller in a CANDU NPP refurbishment project [56]. All of these are a natural evolution with rapid development of computer technology and do bring performance enhancement to CANDU NPPs.

Whilst CANDU NPPs are now having fully computerized SDS1, digital computers are used mainly in two components of the system: trip logic processing unit and the display/monitoring unit [55]. The monitoring computer is a passive component not involved in the shutdown process. Thus, the trip computer, which executes the trip logic using software, is the only component that can be replaced by faster FPGA implementation to speed up SDS1.

2.3.2 Issues in software-based SDS1

When global computerization tide appeared, there was increasing ubiquity of computer systems in both everyday life and industries. CANDU was among the first reactors, in the early 1980s, to use digital computers for shutdown logic implementation. However, difficulties were encountered after these software-based safety systems had been deployed in NPPs for years.

The process of approving the license becomes difficult and time consuming, especially for software-based systems with complex control logic and algorithms. The reasons of this strait lie in the nature of software itself, such as discrete processing manner and inherent design faults [57].

When the control algorithms become more and more complex to adapt the increasing safety and function demands, system specifications are getting miscellaneous. It is basically impossible to demonstrate that the design of a software-based system for realistic control purpose is correct and that failure mechanisms are completely eliminated [58]. The reliability of software-based system is also argued due to the large number of discrete states without the repetitive structure found in computers. Problems can arise in

the use of software-based systems when their discrete nature is accompanied by great complexity which is a source of error and unreliability [57]. Canadian industry has put efforts to improving this aspect through learned lessons in NPP safety critical software applications [59]. It is also very difficult to provide realistic test conditions for the software-based system. Actual operating conditions often differ from test conditions. However, the software simulation process at the verification and validation (V&V) stage has to be performed based on assumptions and there is no way to guarantee that the simulation is accurate enough [60].

Due to above mentioned reasons, regulators are facing difficulties when approving a software-based system for safety application in NPPs [61]. When the system is about to be applied as safety critical components in an NPP, the approval work load can be burdened even further. Then the question arises for how one can take advantage of the digital system without suffering the burden of regulatory approval process, especially for safety critical systems. One option is given by advanced digital hardware platforms, e.g. FPGAs, which are pure hardware once implemented but capable of processing complex logic as software-based system do.

2.3.3 Speed of response of CANDU SDS1

Figure 2.5 shows the brief structure of one of the three CANDU SDS1 channels, which is composed of sensors for system variable measurement, trip computer for trip logic processing, relay logic for 2oo3 voting, and the shutoff rods for reactor trip [52].

Since this is basically a serial structure, the time consumed by a shutdown process is the summation of the time needed for each section. Theoretically, the shutdown process can

be speeded up by reducing the consumed time of any of these parts. However, the significance of these attempts can be totally different since the time spent by each section holds different portion of the total shutdown time. For instance, it takes up to two seconds for the shutoff rods to be fully inserted into the core while the maximum time consumed by the trip computer is 100 *ms* [47]. Furthermore, there has to be available techniques that are capable of effectively reducing the consumed time. Although SDS1 is equipped with compressed springs to provide extra driving force for shutoff rods insertion [16], the insertion still occupies the most length of the entire shutdown process. The decision-making time consumed in the trip computer is to be studied in this work since the trip logic is what to be implemented using an FPGA.

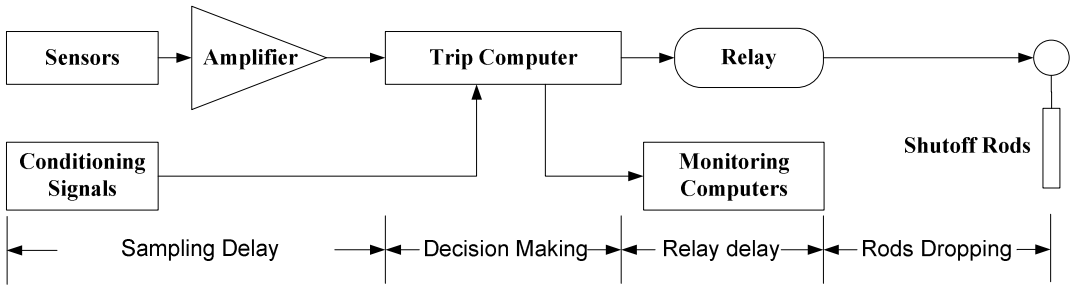


Figure 2.5 – Signal path of SDS1

The speed of response of CANDU SDS1 has been followed with interest and explored by developer and utility of CANDU, such as AECL and OPG. Through a plant test of SDS1 in Bruce-A NPP, AECL has proved that the faster insertion rate of shutoff rods can produce lower neutron flux transient during the shutdown process [62]. Shutdown system tests performed by OPG in Unit 8 of Pickering-B NPP indicate that it took 800 *ms* for reactor neutron power to start decreasing after the initiation of shutoff rods dropping [63], which implies that the speed of the shutdown system has to be fast enough to assure plant safety. It has to be pointed out that in both of the above two cases the shutdown process

was initiated from a normal operating status. Hence, during an accident in which the reactor safety is facing serious threat, a timely and fast shutdown process is of even greater significance.

Regulators take speed of response as a critical factor of achieving NPP safety. It is clearly stated in the CNSC regulations that the shutdown speed and the shutdown margin should be effective enough such that the predefined limits are not exceeded [41]. In the design of the computer-based CANDU SDS1, AECL gives a specification that the logic processing time for the trip computer should not exceed 100 *ms*. This is ensured by a system watchdog which issues a channel trip signal if it has not received any response from the trip computer after 100 *ms* [47]. Both the regulatory requirement and the design specification are to ensure an effective shutdown speed such that the plant safety is reserved even at the appearance of undesired accidents.

With a consideration of the safety significance that the shutdown speed means to NPPs, the emphasis of the current thesis is put on realizing faster speed of response of SDS1 and FPGA, with its demonstrated fast processing advantage, is chosen as an ideal platform for this purpose. Although what this approach shortens is only the decision-making time of the trip logic, which is not a significant portion of the entire shutdown process delay, it does prove the feasibility and advantage of fastening SDS1 speed by FPGA technology.

2.4 FPGA applications for NPP I&C systems

The FPGA utilization for signal processing and control logic execution has been approved to be feasible and cost-effective in many industries. When the demands for

more reliable performance and higher obsolescence resistance arise in nuclear industries, FPGA platform becomes a focus of advanced I&C systems. FPGAs are taken as an ideal option for the replacement of existing obsolescent systems due to its unique configurable hardware characteristics and application experience in other industries. However, challenges do exist for applying FPGA technology to NPP I&C systems since the nuclear industry has its own specific circumstances and unique life cycle requirements. Furthermore, during the FPGA design and implementation process, extra attention is needed to maximally utilize and realize its excellence in enhancing system performance.

2.4.1 Why FPGA

FPGA is not the only option for the update of NPP I&C systems but it does have attractive features to compete with other technologies. The superiority derived from the comparison against others highlights the feasibility of applying FPGAs for the purpose of updating NPP I&C system.

When comparing to old analog systems, an FPGA, as a digital system, shows its outstanding capabilities of better energy resolution, higher signal throughput, stronger obsolescence resistance, and smaller physical size. Less analog components are used in an FPGA since the propagating electrical signals are digitized, which improves the noise immunity and temperature stability. At a very high sampling rate, the incoming signals could encounter pulse overlap, i.e. the pileup. The system performance is then downgraded with a decreased system throughput. Within an FPGA-based system, the digital processing manner has more efficient pileup rejection, which leads to higher throughput. As for the obsolescence resistance feature, the standard development process of an FPGA-based system reserves the effectiveness of the verified and validated FPGA

design and guarantees the functionality of a new FPGA-based system when transplanting the design from the obsolete hardware platform. Finally, due to the higher density and lower supply voltage, FPGA-based systems reduce the size and improve the portability. Cables and cabinets used in the old analog systems can be greatly reduced.

Being a digital hardware platform, an FPGA-based system reveals its merits against software-based digital systems. With no operating system involved, the task distribution is realized directly by distributing signals into pre-configured integrated circuits. The waiting time consumed in a task queue is eliminated. The hardware components that execute the task in a software-based system, e.g. the microprocessor, data bus, and the memory, have to wait for the instructions from the operating system before moving to the next processing stage. In FPGA-based systems, task processing is arranged by building specific circuits for specific processing stages, which increases the processing speed by converting the task processing into signal propagation from input ports to output ports. Due to inherent failure modes, the V&V process of software-based systems cannot cover all the possible cases that could trigger system failure. It is then hard to categorize which inputs, of the ones that have not been executed yet, would produce a failure at execution [57]. Hence, software-based systems could lose its functionality at the appearance of unpredictable system collapse. While for an FPGA-based system, the failure modes only exist in the components of the hardware structure, which are relatively few and can be dependably predicted. Thus, as long as both the design and hardware platforms have been verified and validated, the FPGA platform configured with the design maintains its desired functionality.

FPGAs are competitive even against other modern state-of-the-art digital hardware technologies. Application specific integrated circuit (ASIC), which is most widely utilized for hardware implementation [64], has the potential of being considered as an option for NPP I&C systems. However, it requires large production volume of one ASIC design to make it profitable. On the other hand, only a few chips are needed for a specific I&C application in an NPP even with the consideration of backup and redundancy. Moreover, ASICs are not as flexible as FPGAs. In the case of system specification modification, FPGAs can be reconfigured with a revised design while the only way for an ASIC-based system is to redo the design and manufacture procedure.

In general, FPGAs have demonstrated advantages and superiorities over analog systems, software-based digital systems, and other hardware-based digital system for NPP I&C applications. These potential advantages for NPP performance improvement have attracted great interest of nuclear industry all around the world. Scientists and engineers in nuclear industry have paid a lot attention to this technology and made extraordinary progress, which will be discussed later in the review section.

2.4.2 Performance enhancement through FPGA applications

With the truth that most existing NPPs are using antiquated technologies for I&C systems, FPGAs are optimistically anticipated to enhance plant performance in NPPs. Since FPGAs have strengths in logic processing and signal processing, performance enhancement is mostly expected where signal sampling and algorithm execution are required.

Detectors and sensors are pivotal NPP instruments that provide the measurements of system variables. Accuracy and timeliness are of importance for achieving reliable performance. High throughput and resolution that can be achieved by FPGAs make the performance enhancement possible for processing of the sensor signals. As a matter of fact, most FPGA vendors now provide digital signal processing (DSP) modules within the FPGA chip such that users can realize demanded signal processing by simply specifying the configuration of these modules [65].

I&C systems that are responsible for logic/algorithm execution act as central brain of an NPP. The accuracy and timing of their performance directly affect the productivity and safety of the entire plant. For those safety-related I&C systems, enhanced performance can realize faster and stronger protection for the plant and the environment. Safety systems based on FPGA technology can utilize the fast processing feature to realize such an objective, which is the major investigation of current work and make it one of the major contributions.

Applying FPGA technology to NPP I&C system also enhances the system reliability and availability with fewer inherent failure modes. As an example, considerable progress has been made in reliability and availability by FPGA-based safety-related control and communication functions in accordance with the experience gained in Ukraine NPPs [66]. The deployed FPGA-based systems in Ukraine NPPs are qualified for complex solutions for nuclear installations of different types. They are proved to be a useful tool for retrofit and modernization of existing NPPs. Meanwhile the financial expenses in these NPPs are reduced without affecting the licensing processes.

2.5 Previous work review

The focus of the review is on topics that are relevant to current study such as safety margin, CANDU SDS1, and the FPGA applications in NPPs.

2.5.1 Work on safety margin

Since safety margin is a crucial to NPP safety, both academic and industry have paid enormous attention and efforts to this subject. Regulators such as the CNSC also take the compliance of the safety margin requirement as a necessity of licensing [67]. The accomplished research work about safety margin can be generally categorized into two major areas: precise estimation and improvement techniques.

Since uncertainties exist in the current safety margin estimation as shown in Figure 2.2, lots of research efforts are paid in seeking techniques for more precise results. As what has been surveyed and discussed in [5], traditionally the safety margin estimation is mostly based on conservative evaluation model calculations. Thus, the derived safety margin has high conservatism which reflects untrue operating situation and limits potential enhancement of the plant performance. New estimation methods are then proposed and investigated. For defence-in-depth principle, both deterministic and probabilistic assessments are applied for such kind of safety margin estimation. The deterministic method still includes conservative method but with best estimate method as a complement for different analysis objectives and issues [68, 69]; while the probabilistic methods, which includes best estimate plus uncertainties, are increasingly being used [70-72]. All these efforts concentrate on finding a more accurate way to quantify safety margins and their uncertainties. During a safety margin assessment of an NPP, both

conservative safety analysis (CSA) and probabilistic safety analysis (PSA) may be utilized together to present a complementary assessment to the regulators [73]. Furthermore, the estimation of the confidence of safety margin has special meaning to regulators for their confirmation of the safety satisfactory of a nuclear facility. Various attempts are developed for this safety mandatory goal [74, 75].

Since the current work has limited the scope on investigation of accidental transients of critical reactor parameters, the methods of determining the safety margin are not taken into consideration. However, research work carried out in this thesis does depend on what have been explored. For instance, the interaction between trip limit and safety limit determines the emphasis of the simulation work. The trip limit, which is of considerable significance to safety margin, is determined based on design based accidents (DBAs). In a CANDU NPP, there are total 10 trip parameters associated with the critical system variables. They are high reactor neutron power, high log rate neutron power, heat transport high pressure, heat transport low flow, reactor building high pressure, pressurizer low level, SG low level, moderator high temperature, heat transport low pressure, and SG feed-line low pressure. Any of these parameters across the predefined thresholds (even if temporarily in a transient) is considered to be a potential accident scenario. However, the trip decisions are made based on 2oo3 logics to reduce probability of spurious trips. To meet the acceptance criterion for a specific DBA, the trip limit is set such that the DBA does not pose any safety concerns to the plant system and operators. To ensure this, the trip limit is always set conservatively so that the safety limits are not jeopardized even in the worst case DBA. Significant amount of work has been done to determine those limits under specific operating conditions and postulated accident

scenarios. Two design parameters, margin to trip and margin to dryout, are discussed in [4], which provides a clear relationship between the trip limits and the safety limits. It is also critical to emphasize that an NPP is a complex dynamic system. Even after the trip action is initiated, surges in the system variables are still expected due to thermal inertia associated with the system. Compliance of safety limits at the instant of shutdown system initiation does not necessarily guarantee that the safety limits will not be violated in subsequent period. For this reason, a similar concept known as "shutdown margin" in the unit of reactivity is proposed [76], where the role within the framework of the reactor safety is also described as a reference to the current work. According to [5], the safety margins can either be 1) deterministic, or 2) probabilistic. For current work, only deterministic safety margins are considered, more specifically, in terms of the transient thermal power level.

Keeping adequate safety margin or even improving it has important implication to NPP maintenance and life extension projects [77]. It is intuitively understandable that one can increase the safety margins by lowering the corresponding trip thresholds or enhancing the safety limits. It has been shown in [4] that the probability of power surge exceeding the safety limit during an accident will decrease if the safety margin is increased by means of lowering the trip thresholds. One of the drawbacks associated with lowering the trip thresholds is that the reduced operating range of the reactor, e.g. lower temperature/pressure, resulting in an operating power de-rating. Thus, lowering power output leads to undesirable economical consequences. As for the safety limit enhancement, higher damage resistance of reactor components is required, for which large amount of extra expense on technology renovation cannot be avoided. Although

extra safety margin can be obtained in NPPs by investigating increased confidence on the toughness upper limits of physical barriers with further and appropriate approaches [78], it is still a way of confirming more accurate safety limit instead of enhancing the physical tolerances of the NPP hazard barriers.

Safety margin estimated by best estimate plus uncertainty is presented in an "improved" approach as compared to conservative calculation. This is again a more precise determination to approach the true value rather than expanding the original safety margin.

Safety margin improvement is also followed with interest by other industries. Most of them are still in a form of addressing the uncertainty more rigorously [79]. In [80] and [81], dynamic safety margin is applied to improve the control of safety-critical systems. The technique of enhancing upper limit is adopted in mechanics inventions to widen the existing safety margin [82]. Even modification of reactor design has become a way of safety margin improvement [83]. However, none of these open publications have touched the area of controlling the post-accident transients for safety margin improvement.

2.5.2 Discussions on existing NPP safety systems

CANDU industry has paid attention and efforts to performance improvement of SDS1 trip computers [84]. The usage of software-based systems for safety-critical systems has been debated from early 1980s to present [60, 85]. Nevertheless, these products of the 1980s are facing more and more challenges from state-of-the-art technologies such as advanced FPGAs today. As the central control unit of SDS1, the trip unit should have high reliability, fast response, and strong obsolescence resistance. Easier regulatory approval would also be important. Unfortunately, nowadays bottlenecks of satisfying

these requirements have been encountered by software-based trip computers. It has been pointed out that extremely large amount of efforts and evidences are needed for assessing the reliability of software deployed in safety-critical systems [86]. CANDU industry itself has a tough and long-waiting licensing experience during the 1980s for their first software-based digital shutdown system [87]. Swedish regulatory body also stated their comments on licensing software-based safety systems [88] while the controversies on software-based safety systems between Korean nuclear facilities and regulators are shared in [89]. All these documented opinions and experiences expose the connate drawbacks of software-based safety systems.

2.5.3 FPGA applications in NPPs

FPGAs and similar programmable logic devices (PLD) are not new to nuclear industries. Numerous research projects and engineering applications were initiated decades ago. These projects focused on FPGA solutions that can increase the reliability and serviceability with the original functionality and specifications still accommodated. These projects covered from nuclear medical applications and reactor instrumentations to radiation detection and NPPs. Since the 1990s, nuclear industry has greeted a blooming era of FPGA applications.

In the 1980s, the Canadian nuclear industry launched several research projects to apply PLDs to CANDU NPPs. Distinct applications have been developed for process control systems such as the CANDU fuel-handling machine and the NPP powerhouse emergency venting system [21]. Among these NPP projects, FPGAs show the ability of dealing with large number of I/O pins and complex logic functions as well as other economical and flexible features. An outstanding advantage approved among these NPP projects is that

the interconnected gates of logic provide independent parallel paths for the various logic circuits that are implemented. The transfer function connecting an output to any number of determining inputs operates independent of the other circuits within the chip, barring total failure of the device. Moreover, the pin-to-pin transitions are proved to be on the order of nanoseconds, and circuits can be modeled to precise timing characteristics with timing delays designed into the circuit.

Besides the above fully implemented and qualified applications, AECL also paid attention to the FPGA application for safety-critical systems. Various prototype-approaches were investigated to make FPGA the alternate of those aged relays in safety systems such that the conditioning interlocks and more complex control logic can be implemented [90-92]. Unfortunately, these inspiring projects were not able to become on-site applications. The immaturity of PLDs at that time, such as low density of logic elements and weak immunity to electromagnetic interference (EMI), constraint them to be widely used for safety related applications. The confidence of digital computers was relatively higher over that of the "newborn" PLDs, which led to the computerized SDS1 in CANDU NPPs.

Nevertheless, PLDs such as FPGA never left the sight of nuclear engineers. After the development of more than one decade, FPGAs became very popular in other industries and made remarkable contributions since the beginning of the century. Their powerful abilities are reflected in data acquisition, signal processing, and logic implementation. More and more FPGA applications then started to appear in nuclear fields such as reactor instrumentation and nuclear imaging [93-95]. These kinds of research work mostly

utilized FPGA's features of signal processing and flexibility because they mainly involve data acquisition functions.

In existing NPPs, as long as current systems satisfy the safety and operating requirements, there is no immediate demand of replacing them with new technology unless enough confidence is built upon convincing verification and validation. Fortunately, both regulators and nuclear power industry became aware of the potential of FPGAs and started both feasibility investigation and prototype attempts. Starting from 2008, IAEA has held four annual international workshops for FPGA applications in NPPs. Many other conferences of nuclear engineering also take FPGA as a striking topic with growing interest. Numerous topics have been presented. With respect to the scope of this thesis, the survey of the accomplished work is briefly categorized as safety-related and non safety-related.

Non safety-related topics mainly concentrate on instrumentation/monitoring and supporting functions of NPP systems [96-98]. These FPGA applications are similar to those data-oriented ones. Data acquisition and processing are their main functionality, which can be helped by the signal processing capacity and flexibility features of FPGAs. On the side of safety-related systems, the high qualifications can still meet the specified requirements by fully utilizing FPGAs advanced features. To specifically and effectively guide the FPGA-based safety development for NPPs, regulators and other related entities have issued different guidelines and standards [23, 99, 100]. Following these guidelines as well as the original requirements of safety systems, FPGA-based safety applications are carried out worldwide.

Electricite de France (EDF), a French power utility, developed several FPGA-based projects for their NPPs. These projects include upgrading the control rod positioning system and pump speed control systems. Significant benefits are summarized as simplified design and safety justification, focused upgrade of existing I&C systems, and application portability on technologies [101]. In Japan, FPGA technology is utilized for radiation monitoring safety system from 2004 to 2007 [102]. A safety-critical FPGA system is developed in Korea based on an existing safety PLC and replaced this PLC to carry safety functions [103]. FPGA-based shutdown system is designed and implemented in Ukrainian and Bulgarian NPPs where the design load is reduced while the performance was upgraded [104]. An interesting example is documented in [105] that it took U.S. NRC only two years to complete the approval process, which is much shorter than a software-based implementation that can last over 10 years. Canadian nuclear industry did not fall behind. FPGA platform is investigated to improve the reactor trip methodology and the digital control computers in NPPs [106, 107].

The above surveyed FPGA work in nuclear industry provides a review of the preliminary but rapid progressing attempts of applying FPGA technology into both non safety-related systems and safety-related ones. As it can be seen, the flexibility feature enables FPGAs to accommodate different specifications of various projects. Its standard implementation process realizes simplified design and transportability of applications. Most importantly, its high reliability and serviceability make FPGA one of the best options for safety-related system development.

In addition to the inherent characteristics that lead to fast processing of FPGAs, tremendous effort has been continuously invested to develop techniques that enhance the

processing speed of FPGAs. The delay within FPGA interconnections and routing architecture can be potentially shortened to further increase the response speed [108, 109]. Improving the logic block architecture is also applied to the processing speed of FPGAs [110, 111]. To improve the arithmetic processing capability of FPGAs, specifically designed algorithm is proposed [112].

There have been many non-nuclear applications that utilize the fast processing speed of FPGAs to achieve better performance. Real-time image processing uses the high-speed FPGAs to improve data arrangement through dynamic reconfiguration [113]. High-speed network flow processing is achieved using FPGA-based system [114]. Utilization of FPGA-based controller helps the motion control system obtain high-speed and high-accuracy performance [115]. Such fast processing ability is also applied to many other projects, such as high-speed communication interface [116], rapid prototyping platform for variable-speed drives [117], and high-speed edge and corner detection in image processing [118].

However, as noticed, the fast processing advantage has not been fully explored and applied for nuclear safety applications, even there is already successful work in other nuclear application domains [119, 120]. Since building a high-speed controller using FPGA technology has been demonstrated [121], current work proposes that implementing CANDU SDS1 using an FPGA is a way of realizing faster shutdown process for safety margin improvement.

2.6 Summary

This chapter presents necessary background for the proposed research. Several key topics are introduced and discussed with detailed review of previously works.

After the introduction of some nuclear safety basics, the concept of the safety margin is explored. Using neutron dynamic theory, it is demonstrated analytically that faster shutdown process is an effective way to reduce the jeopardizing effect of an accidental transient. It is then chosen as the topic of research in this thesis for safety margin improvement.

FPGA applications in NPPs have been followed closely worldwide since the early 1980s. For both non safety-related and safety-related applications, FPGAs have successfully proved their superiorities as compared with other methods. Accomplished projects utilized distinct FPGA features to achieve desired specifications. But the fast processing speed of FPGAs has not been fully utilized to improve NPP safety. This direction with an objective of an FPGA-based fast-reacting SDS1 is explicitly investigated in this thesis.

To summarize, this thesis brings forward an idea for safety margin improvement through faster shutdown process by using an FPGA-based SDS1. Based on the related work, the research details, results, and foreseeable benefits are presented and discussed in the following chapters.

3 INVESTIGATIONS ON ACCIDENTS IN CANDU NPPS

The thermalhydraulic investigations on specific accidents have to be carried out from practical perspective to test the proposed safety margin improvement concept. The main focus is whether or not a shortened shutdown process is able to improve the NPP safety margins. In this chapter, the thermalhydraulic investigations are performed using an industry grade code specifically for CANDU reactors called CATHENA.

The procedure for thermalhydraulic studies can be divided into following steps: 1) constructing simulation models; 2) defining the test scenarios and simulation environments; 3) carrying out the simulations; 4) collecting and analyzing the simulation results; and 5) drawing the conclusions

3.1 CANDU thermalhydraulic basics

The reasons of using thermalhydraulic analysis for V&V of the accident scenario are: 1) Reactor variables that have close relationship to NPP safety mostly involve thermalhydraulic transients, such as thermal power, temperature, and pressure; 2) Transients of these thermalhydraulic-related variables are very intuitive and, hence, can clearly demonstrate their impacts to the safety margins; 3) Catastrophic consequences caused by severe accidents can threaten NPP safety through accidental transients of these variables. Therefore, accidental impacts on NPP safety can be described and analyzed by a proper thermalhydraulic analysis.

3.1.1 Chosen thermalhydraulic loop

Power reactors use coolant to bring out the heat generated by fission reactions in the core. Most reactors use light water. A CANDU reactor is designed to cool the core using heavy water but recently light water is being considered [122]. No matter what kind of coolant, efficient circulation of the coolant is of extreme importance. Coolant is pumped through a pipe network from which the heat in the core is exchanged to the secondary side for electricity generation. The coolant, after passing through the steam generator (SG), is circulated back to the core to repeat the heat transfer function. A closed-loop circulation is formed. Failure of the circulation, such as loss of flow (stagnation) and loss of coolant, is considered as a severe accident since it leads to the halt of the heat removal process. As a result, the temperature can then increase at an exponential rate and pose a serious threat to the reactor core and the nuclear fuel inside the core.

A CANDU reactor has its unique circulation loop, the PHT system. Unlike the designs of pressurized water reactor (PWR) or boiling water reactor (BWR) in which the core is fully submerged in the lighter water, CANDU reactors have the moderator and coolant separated. In a CANDU 6 reactor, a horizontal calandria houses both the pressurized fuel channels and the moderator. Coolant is distributed into 380 pressurized fuel channels to deliver the heat to the four SGs. The circulation of the coolant in a CANDU 6 reactor can be divided into two independent loops, each of which contains half of the fuel channels. The loop is arranged in a “Figure of 8” with the coolant making two passes in opposite directions, so is the coolant in two adjacent fuel channels. Each loop has its own SGs and other auxiliary equipments such as pumps, valves, pressurizer, reactor inlet header (RIH), and reactor outlet header (ROH). An illustrative diagram is presented in Figure 3.1.

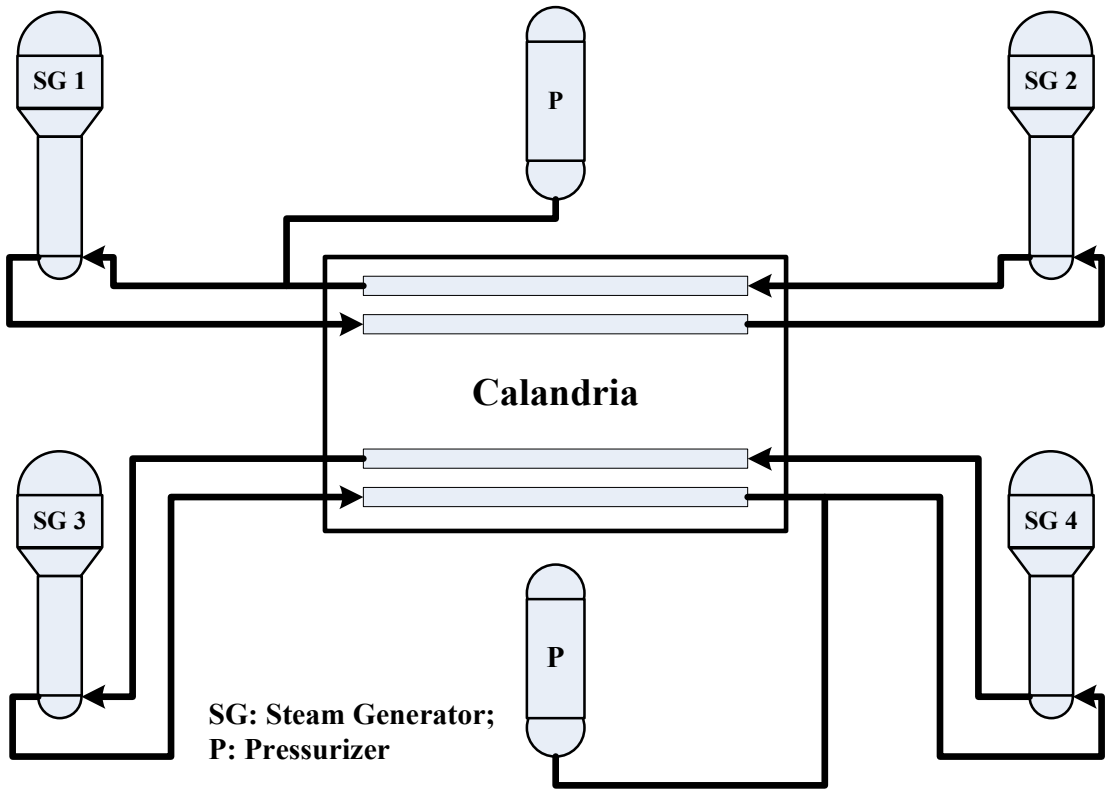


Figure 3.1 – CANDU PHT loops

Most of CANDU thermalhydraulic analysis work is associated with the PHT system, where many phenomena with safety concern occur [123, 124]. LOCA, which always is the safety focus, is one type of the postulated accidents in the PHT system during simulation and analysis. The fuel channel, which is the source of thermal power, is another component that is worthy of investigation [125, 126]. One DBA that could happen in a fuel channel is a loss of flow accident (LOFA). Thermalhydraulic investigation of a channel-based LOFA helps reveal the channel behavior during such undesired conditions.

Thermalhydraulic analysis in this thesis investigates the reactor behavior during a channel LOFA and a PHT LOCA. Structures and parameters of both PHT and a fuel

channel are used for construction of CATHENA simulation models. Transients of critical variables, such as thermal power and sheath temperature, are recorded and analyzed for the postulated accidents.

3.1.2 CATHENA basics in accident simulations

CATHENA stands for Canadian Algorithm for THEermalyhraulic Network Analysis. It is developed by AECL as an industry tool for postulated accident analysis in CANDU reactors [25]. It uses a transient, one-dimensional two-fluid representation of two-phase flow in the piping networks. Under a two-phase condition, liquid and vapor may have different temperature, pressure, and velocity. Thus, each phase has independent conservation equations of mass, energy, and momentum. CATHENA simulation/analysis is based on solving such six partial differential equations.

In addition to the two-fluid thermalhydraulic model, CATHENA provides a generalized heat transfer package as well as the reactor control system modeling. Therefore, it is possible to simulate the transient thermal behavior of the core as a function of actions in control/safety systems, e.g. an accident and its related shutdown process. The description of the accident are defined in CATHENA with details of the accident and shutdown process, such as the flow rate change at LOCA or how fast the negative reactivity is injected during a shutdown process.

A component package in CATHENA is available for constructing desired system models. The components include the model of pipes, valves, T-junctions, volumes, reservoirs, etc. The envisaged reactor model or simulation loop can easily be built using different combinations and connections of these models. Some of these models can even be used

as boundary conditions in the simulated network. Users have to specify the characteristic parameters of each component, such as length, fluid direction, and material properties. One can use tables to enter process information so that CATHENA can select appropriate dynamics within the simulated process.

The constructed model and gathered information are integrated to generate an input file for CATHENA. Edit of the input file has to follow certain format predefined in the CATHENA manual. Simulation parameters such as print interval and output file name should also be specified. Initial conditions are required in the input file.

In a simulated accident scenario, the accident takes place when the system is at steady-state. Hence, the steady-state behavior of the system has to be simulated first. The yielded results are used as the initial conditions for the transient simulation. In the steady-state simulation, there is no interference introduced into the system. As long as the initial conditions are within reasonable range, the simulation results represent a steady-state system.

3.1.3 Description and justification of the postulated accidents

As what have been introduced, the LOFA and LOCA are the two accidents that threaten the integrity of physical barriers for radioactive substances. This study chooses these two accident scenarios for analysis with a consideration of strengthening the safety margin improvement concept by validating it under severe accident cases.

The LOFA might involve one fuel channel as a result of a flow blockage or the whole PHT because of loss of forced circulation such as a pump trip. There are then large increase in the mass of the exit flow and overpressure within PHT system/channel. One

of the undesired consequences is the flow/power mismatch, i.e. more power is being generated in the fuel channel than that can be removed by the coolant flow. If the reactor cannot be shut down at this time, fuel channel can potentially encounter dryout and fuel bundle rupture with the accumulated heat. Since SDS1 monitors the PHT flow as a trip parameter, the serious consequences can be prevented by shutting down the reactor right after the occurrence of this accident. Because the positive reactivity introduced is slow at the beginning of LOFA when quick voiding has not occurred, a timely shutdown will effectively prevent sharp surges in PHT pressure and power. Thus the response time of the SDS1 is of critical significance to the plant safety during such an accident.

The large LOCA, which is often postulated to happen in the PHT, brings much faster positive reactivity in the core than LOFA. Void fraction increases because of not only the coolant outflow but also the quick boiling of coolant following the channel depressurization. This can be a fast developing process and leave very short time for the plant to react. The exponentially increase in power transient offers the worst case scenario for the safety margin analysis than other cases, especially when the SDS1 response time is of the main interest.

The justifications of choosing both LOFA and LOCA for the thermalhydraulic investigations are: 1) they are typical severe accidents concerned as threat to the plant SIL; 2) their occurrence involves dramatic transients of the reactor thermalhydraulic variables, such as power, temperature, and pressure; and 3) their responses could be different for different SDS1 response speed, which provides a clear picture on the benefits of response time reduction of the shutdown system.

3.2 CATHENA simulation for the postulated accidents

To support the current investigation, simplified CANDU 6 fuel channel model and reactor core model are constructed without considering details of the fuel assembly, and associated control systems, since the current work focuses only on the transients of critical system variables after a major accident. The fuel channel model is constructed with a simplification of boundary conditions and fuel bundles. It uses standard 37-element CANDU 6 fuel channel attributes. The reactor core model includes reactor core, RIH, ROH, feeder pipes that connect the core to both RIH and ROH, and the two header boundary conditions at both ends of the core model.

Since LOFA is one of the severe DBAs that can cause fuel overheating during reactor operation [127], it is selected first to analyze the local transient behavior under different shutdown processes. Furthermore, a large LOCA of 35% break at RIH in the PHT system is chosen as the worst-case accident scenario for the core-wide transients analysis since this kind of accidents has been categorized as one of the most severe accidents that can occur in a CANDU reactor.

During simulation studies, a steady-state condition is reached first; subsequently the selected accident scenarios are initiated. The simulation studies are performed under different response time of the SDS1. The data for both the fuel channel model and the core model are collected, which reflect transients in both local and global points of view, respectively.

3.2.1 Construction of simulation models

To investigate the impacts resulted from accidents, this thesis puts the emphasis on some critical in-core variables such as the reactor thermal power and sheath temperature of the fuel bundles. The simulation is then limited to the transients taking place within the core. Model construction work also mainly specifies details of the CANDU 6 core. Two simulation models are constructed for the thermalhydraulic simulations. One is a fuel channel model for the LOFA analysis while another is a reactor core model for the selected large LOCA.

A typical CANDU 6 reactor core consists of 380 horizontal pressurized channels. Each holds 12 fuel bundles. All these fuel channels are located inside a calandria filled with heavy water moderator. Heavy water is also used as coolant that passes through pressure tubes to remove the heat generated in the core. Coolant goes through the RIH where it is further distributed to each channel through feeder pipes. The ROH collects heated coolant from the channels before transporting the thermal energy to the PHT system for steam generation. On the top of the calandria, there are 28 SDS1 shutoff rods that can be inserted into the core to stop the chain reaction when activated by the SDS1 trip signal. A reactor face view with a bank of shutoff rods on top is shown in Figure 3.2.

The geometry parameters of the fuel channel, which is needed for CATHENA simulation, are listed in Table 3.1. As what is stated in Table 3.1, there are totally 21 simulation nodes defined within a standard CANDU 6 fuel channel. Fuel bundles within the channel are also standard 37-element ones.

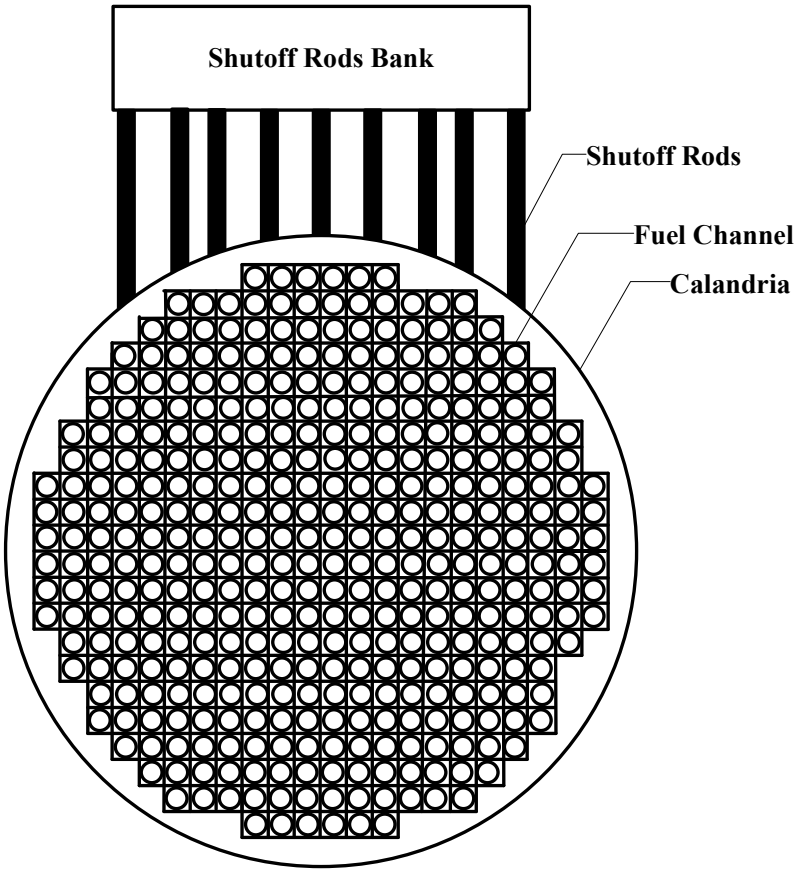


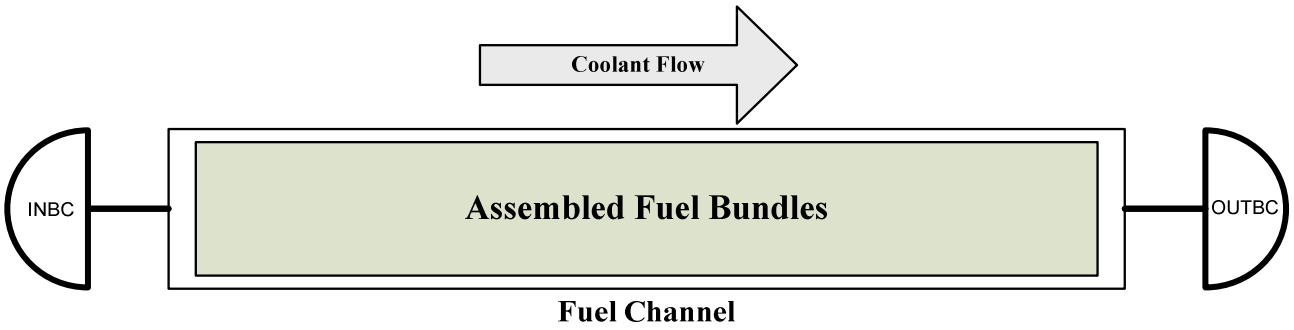
Figure 3.2 – CANDU 6 face view with SDS1 shutoff rods

Table 3.1 Fuel channel attributes for CATHENA simulation

Length (m)	Flow Area (m^2)	Hydraulic Diameter (m)	No. of Bundles	Fuel Bundle	No. of Nodes
5.9436	3.40694E-3	7.37629E-3	12	37-element	21

(1) Fuel channel model

The fuel channel model for the LOFA simulation is based on parameters listed in Table 3.1. An illustration of this fuel channel model is shown in Figure 3.3:



INBC：Inlet Boundary Conditions
OUTBC: Outlet Boundary Conditions

Figure 3.3 – Fuel channel model

Purpose of such a model is to explore the local transients during a LOFA. The INBC and OUTBC are two reservoirs used as boundary conditions. The part of "assembled fuel bundles" is a simplification of the 12-bundle pattern. The channel power, which is 5481.58KW, is selected from one of the 380 fuel channels.

As it can be seen, the fuel channel model concentrates on the transient of a severe DBA within a single fuel channel. Since the transient surge appears within a short period after the accident happens, auxiliary components of the fuel channel are not included.

(2) Reactor core model

As for the reactor core model, the core partitioning method is applied. Operation experience and research results have shown that CANDU has flat neutron flux mapping which causes relatively uniform power distribution [128, 129]. It can be mentioned that there is no large difference in thermal power between nearby fuel channels. Hence, it is reasonable to use a model of assembled fuel channel to represent part of the reactors, as displayed in Figure 3.4.

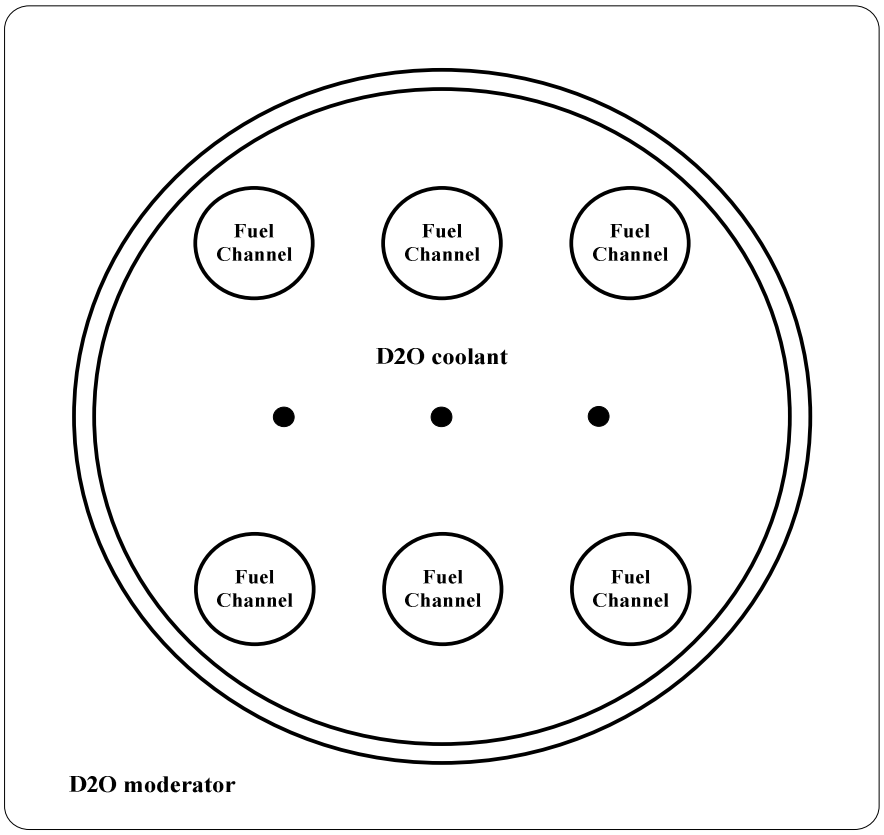


Figure 3.4 – Postulated region assembly

Moreover, due to relative large physical size of CANDU 6 core, one usually divides it into fourteen virtual zones for control system design and implementation [130, 131]. However, any single fuel channel from an inlet to an outlet covers two zones. Since the current study focuses on the global thermalhydraulic behavior, the model should cover the core from the flow inlet to the outlet. Hence, a 7-regional partition of the core is used. Each of these seven regions is formed by merging two zones adjacent in horizontal direction of the mentioned 14-zone partition, which is similar as the model used in [132]. This simplified model is used for the study of the core thermal power distribution in each of the seven regions and their associated safety margins. Trip decision for the postulated

accident is initiated with consideration of regional signals in each of the seven regions, such as regional neutronic signals and power signals. The 7-regional core model used in the current study is shown in Figure 3.5.

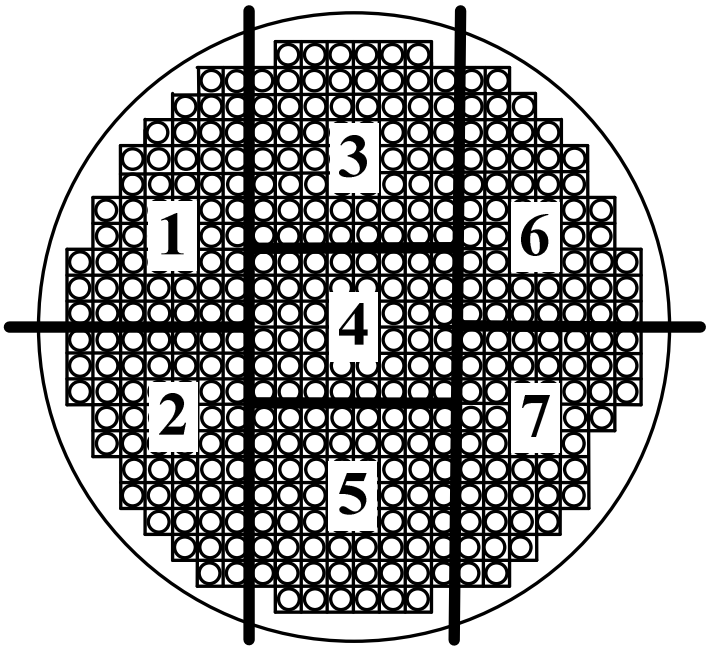


Figure 3.5 – Core partitioning for simulation studies

Table 3.2 Region characteristics

Region	No. of channels	Power (MW)	LHGR (MW/m)	Region PPF
Region 1	52	265.833	0.8601	0.9424
Region 2	52	264.288	0.8551	0.9370
Region 3	62	346.352	0.9399	1.0300
Region 4	48	306.073	1.0728	1.1755
Region 5	62	348.210	0.9449	1.0354
Region 6	52	265.905	0.8603	0.9427
Region 7	52	264.560	0.8560	0.9379
Total	380	2061.221	0.9126	N/A

*LHGR: Linear Heat Generating Rate; PPF: Power Peaking Factor

The effects of neutronics and Xenon are also taken into consideration in the modeling process. The characteristics of the seven regions are listed in Table 3.2.

After the geometry configuration of the core model is determined, a point kinetic model is chosen for each region to count for neutronic effects in the reactor core. Kinetics coefficients are determined by the effective density and temperature that are obtained from steady-state simulations results. The simulated core is assumed to be at an equilibrium condition, before any fault is initiated. Decay power and Xenon effects are both taken into account using CATHENA internal system models. Reactivity feedback from both coolant density and the temperature is also considered in accordance with the CATHENA simulation requirements, in which it is described in a quadratic form listed in Equation (3.1) [133]:

$$\Delta k = A \times (\Delta x)^2 + B \times \Delta x \tag{3.1}$$

where,

Δk is the added reactivity by the change of the density or the temperature;

x represents the appropriate variable (density or temperature); and

both A and B are the related coefficients.

For the simulated CANDU reactor, coefficients used in Equation (3.1) are listed in Table 3.3 according to the CATHENA input reference manual.

Table 3.3 Coefficients of reactivity change caused by void fraction and temperature

	A	*B*
Density	0	-0.0118
Fuel Temperature	3.747E-6	-0.006

The RIH and ROH are modeled using available components from the CATHENA component base. Basically these two headers are modeled as branches of connected pipes with volumes. The actual layouts of these two header models are shown in Figure 3.6 and Figure 3.7.

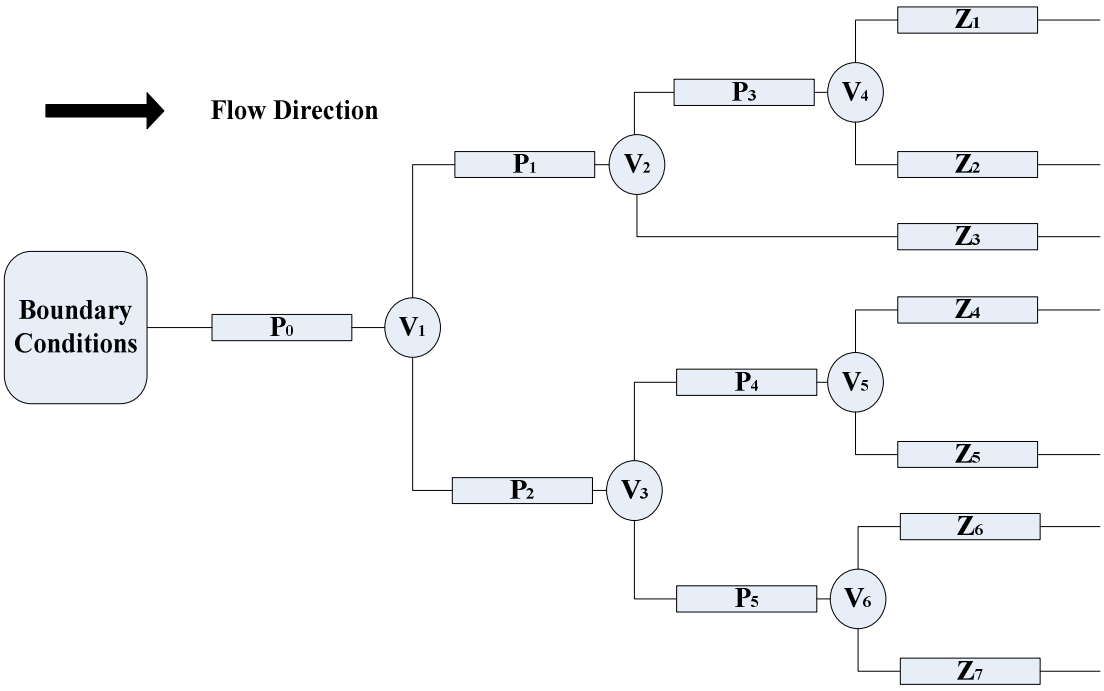


Figure 3.6 – Layout of the RIH model

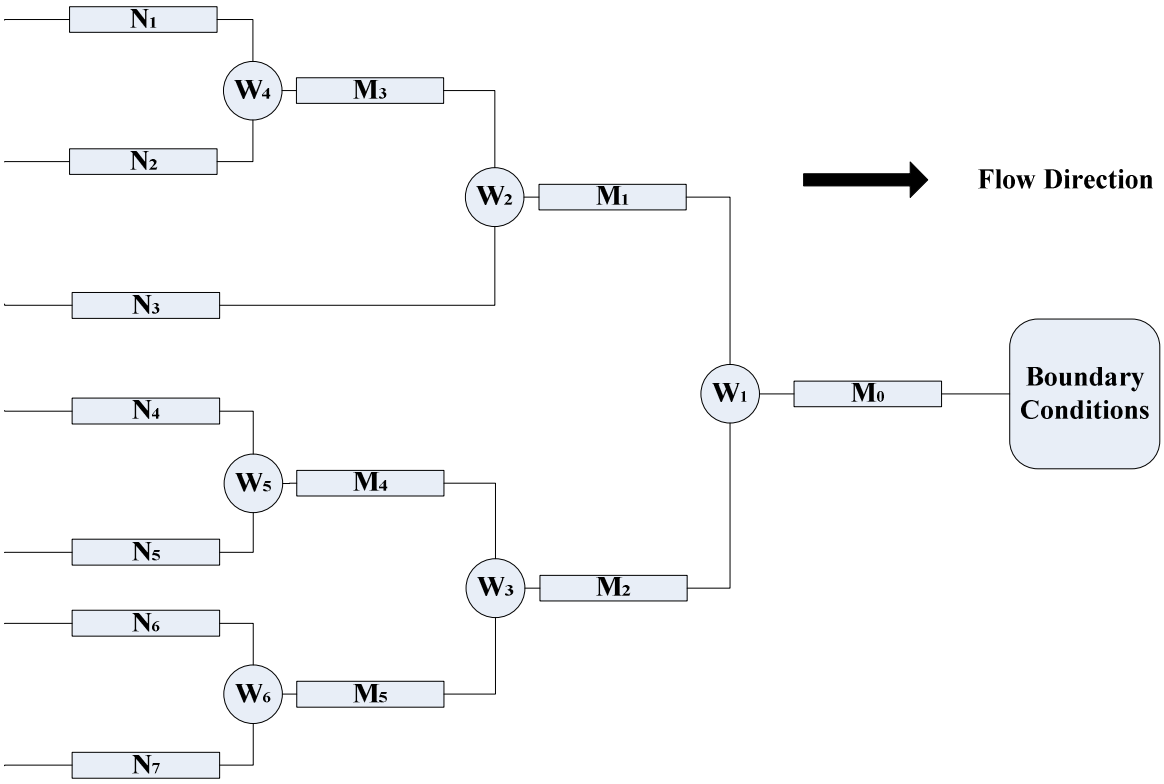


Figure 3.7 – Layout of the ROH model

With the models of core, RIH, and ROH are prepared, they are connected to the feeder pipes and two boundary conditions at both ends to form the CATHENA simulation model. Due to the relatively short transient interval of an "accident-shutdown" process, the model has been simplified such that not all the components in the PHT system are included. The transients of other PHT components have been omitted because they do not affect the in-core parameters instantly.

The pipe set Z(*i*) in the RIH model and N(*i*) in the ROH model are connected to corresponding regions, e.g. Z(1) is connected to Region 1 at the inlet side while N(1) is connected to the outlet side. The geometry parameters of these pipe sets are indicated in Table 3.4. Only parameters for P(*i*) and Z(*i*) are presented because P(*i*) set and Z(*i*) set are identical to M(*i*) set and N(*i*) set, respectively.

Table 3.4 Pipe attributes in RIH and ROH

Pipe No.	Length (m)	Flow Area (m^2)	Hydraulic Diameter (m)	Simulation Node
P0	0.1	1.2946	1.2839	1
P1	0.1	5.6555E-1	8.4858E-1	1
P2	0.1	7.2909E-1	9.6348E-1	1
P3	0.1	3.5432E-1	6.7167E-1	1
P4	0.1	3.7476E-1	6.9077E-1	1
P5	0.1	3.5432E-1	6.7167E-1	1
Z1	0.1	1.7716E-1	4.7494E-1	1
Z2	0.1	1.7716E-1	4.7494E-1	1
Z3	0.1	2.1123E-1	5.1860E-1	1
Z4	0.1	1.6353E-1	4.5631E-1	1
Z5	0.1	2.1123E-1	5.1860E-1	1
Z6	0.1	1.7716E-1	4.7494E-1	1
Z7	0.1	1.7716E-1	4.7494E-1	1

In reality, CANDU 6 has two independent loops, each of which has its own RIH and ROH. However, for the purpose of examining the global thermal behavior of the reactor under a large LOCA scenario, these two loops are aggregated to form a single loop model as shown in Figure 3.8.

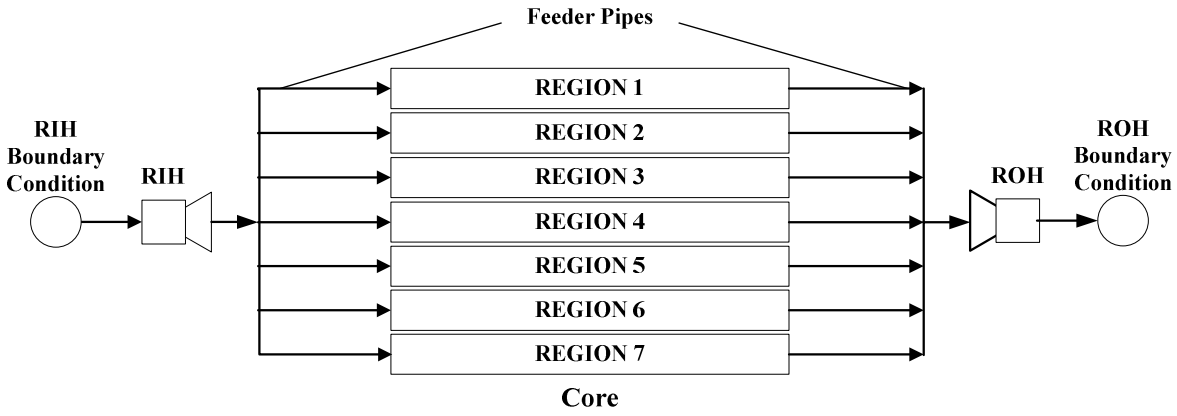


Figure 3.8 – CATHENA simulation model for large LOCA studies

Again, this is a simplified reactor core model because, for the current study, 10 seconds simulation runs after the LOCA are sufficient. The effects of other unmodeled system components are relatively small and can be neglected. As far as power transients are considered, only a period of 1-3 seconds is needed for the safety margin analysis [134].

3.2.2 The simulation cases

As this is a safety-related analysis, accident cases should be selected for the CATHENA simulation. It is then possible to observe how the reactor responds to the accident and how the proposed technique help improving the safety features. A LOFA case is simulated first with the fuel channel model to investigate the local transient of a typical DBA. Since the results are more persuasive if the worst case scenario is considered, simulation of a large LOCA is then carried out. The improvement on system safety under the worst case accident will be applicable to other less severe cases.

(1) LOFA

A LOFA is an accident in which the coolant flow rate of the PHT system encounters decrease or even stagnation. Such an accident is caused by some undesired events, such as loss of off-site power, pump failure, heat exchanger blockage, pipe blockage, or valve closure, etc. At an onset of a LOFA, the coolant heat transfer coefficient is reduced and the reactor core is subject to overheating. Fuel integrity faces severe threat [127].

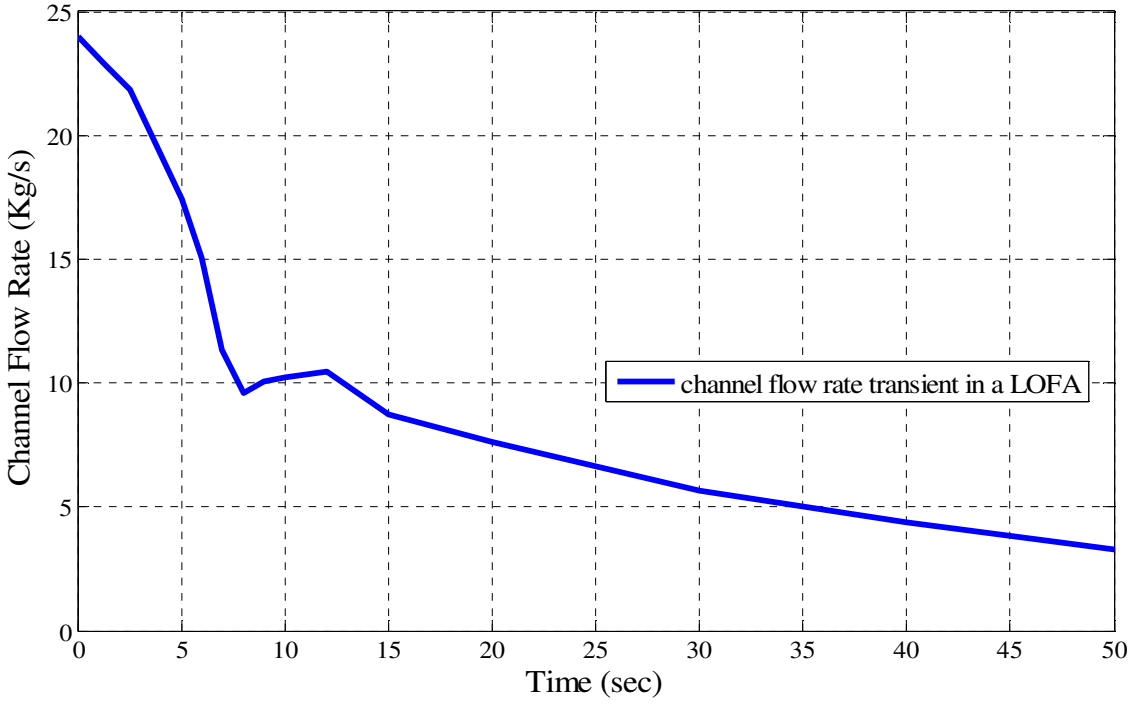


Figure 3.9 – Flow rate transient in a LOFA

On November 25, 1993, Unit 4 of Darlington NPP in Ontario Canada, encountered a LOFA due to the loss of plant power supply [135]. The PHT pumps were tripped, leading to significant reduction of the in-core coolant flow. The resulting increased PHT pressure, PHT temperature, and the reactor thermal power lead to both the SDS1 and SDS2 trip. The plant data of the flow rate during this accident is adopted for the LOFA case

simulation in this work. Figure 3.9 shows the LOFA flow rate transient in the fuel channel model [135].

(2) Large LOCA

Large LOCA scenario is chosen as a core wide simulated accident since it is one of the most severe accidents that could occur in a CANDU NPP. There have been plenty investigations from the 1980s [136], the 1990s [137], to present [138, 139] for such LOCA scenario. The large LOCA, which is mostly postulated to happen in the PHT system, causes decrease in coolant mass and increase in the void fraction. Decreasing coolant deteriorates the heat removal capability of PHT system, which leads to a fuel overheat stage. While the increase in void fraction brings linearly increased positive reactivity [140] followed by a dramatically elevated thermal power. Impacts of these two consequences can jeopardize the safety of the plant. For such a severe accident, it becomes more evident for the proposed techniques to alleviate the post-accident scenario. It is also relatively easy to describe this accident scenario in LOCA using just the break size and the rate of flow change. Furthermore, there are both power and temperature surges in the "accident-shutdown" transients, which are the main considerations for safety margin analysis in the current work.

LOCA accidents can be categorized by different accident scenarios, such as break size and break location. Following the worst-case principle, the worst case LOCA has to be selected by specifying the break size and location. The way to define the "worst" is based on the severe consequences that the accident can cause.

There are several key locations in the PHT system where large LOCA can occur, such as RIH, ROH, pump suction pipe, etc. In this work, the selected simulation case is RIH break LOCA. More specifically, 35% break at RIH is chosen for large LOCA simulation. The justifications for such choice are given below.

RIH is the location where the coolant is distributed to all 380 fuel channels in CANDU 6. Each CANDU 6 fuel channel has a flow rate of 24 *kg/s*, which means that the RIH flow rate can reach as high as 9120 *kg/s*. Under an operating pressure of 11 *MPa*, a break appears at this critical point can cause rapid lost of the coolant. Due to the selected LOCA consequences, the plant safety can be seriously jeopardized. Investigation of the RIH break LOCA helps gain knowledge of the post-blowdown scenario as well.

At a certain location, breaks of different sizes can have distinctive impacts to the system behavior. However, a larger break does not mean a worse consequence. Large break yields fast lost of the coolant but not the long stagnation of the coolant. When stagnation happens, the flow rate is reduced to around 0 *kg/s*. The halt of heat removal results in rapid heat accumulation. On the other hand, the loop depressurization from the break dramatically lowers the boiling point of the coolant. With the accumulated heat and lowered boiling point, the coolant starts vaporization quickly, which increases the void fraction even further. The result is then a vicious circle: increasing void fraction causes higher power and temperature with positive reactivity. The accumulated heat in turn increases the void fraction. Thus, the longer the stagnation is, the worse the situation will be. CANDU research work has pointed out the 35% break at the RIH to potentially be the worst large LOCA case since it causes the longest stagnation during the post-accident period [141, 142]. Engineering experiments conducted at AECL provides even more

detailed information on the RIH breaks [143]. In Figure 3.10 and Figure 3.11 [143], the recorded data have shown the flow rate and sheath temperature during LOCA for different break sizes. 35% RIH break turns out to have the longest stagnation and results in the highest sheath temperature, which confirms it as the worst case of RIH break accidents. In the planned CATHENA LOCA simulation work, 35% RIH break is then used to analyze the safety features. In the simulation process, the 35% RIH break is realized by setting a change of flow rate at the first pipe of RIH where the largest flow rate appears.

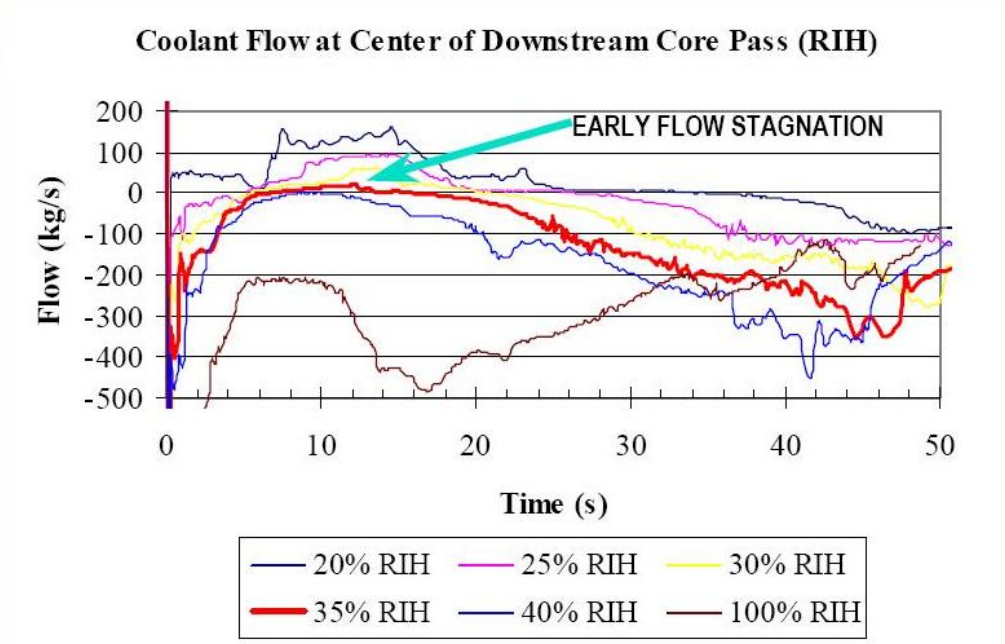


Figure 3.10 – RIH flow rate at different break sizes [143]

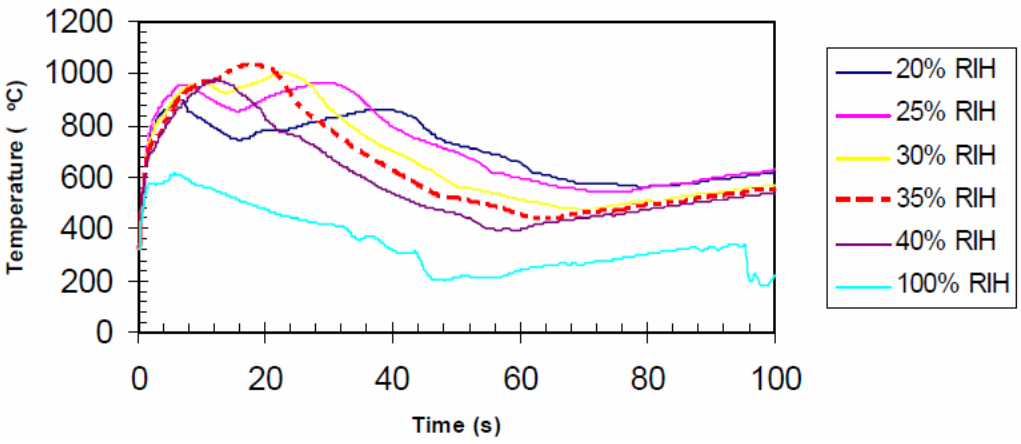


Figure 3.11 – Sheath temperature at central channel during RIH breaks [143]

3.2.3 Simulation for steady-state conditions

Steady-state simulation is used to establish the initial conditions before performing the accident simulation. Thus, it is necessary to run a steady-state simulation. The initial conditions for accident simulation is obtained for both the fuel channel model and the reactor core model as listed in Table 3.5 and Table 3.6.

Table 3.5 Steady-state conditions for LOFA

Location	Flow Rate (kg/s)*	Power (KW)	Sheath Temp. (℃)*	Pressure (MPa)*
Fuel Channel	24	5431.579	345	10.025327

*Sheath temperatures are sampled at the hottest point of sheath's innermost layer.
*Flow rates and pressures are sampled at the first node.

Table 3.6 Steady-state conditions for large LOCA

Location	Flow Rate (kg/s)*	Power (MW)	Sheath Temp. (℃)*	Pressure (MPa)*
RIH	9120.0002	N/A	N/A	10.602951
Region 1	1226.7261	265.833	328	10.465877
Region 2	1227.0570	264.288	327	10.465866
Region 3	1646.6269	346.352	333	10.501979
Region 4	1088.6030	306.073	336	10.473398
Region 5	1459.8117	348.210	334	10.471931
Region 6	1235.4499	265.905	328	10.469471
Region 7	1235.7260	264.560	327	10.469462
ROH	9119.4647	N/A	N/A	10.000005

*Sheath temperatures are sampled at the hottest point of sheath's innermost layer.
*Flow rates and pressures are sampled at the first node of each component.

Since the objective of this work is to investigate the improvement of the safety margin by comparing the accident transients under different response time of SDS1, each accident simulation is performed with different SDS1 response times. 200 *ms* and 10 *ms* are chosen for the LOFA simulation. For the large LOCA case, three response time values, 100 *ms*, 50 *ms*, and 20 *ms* are used.

Furthermore, the starting time of the LOFA is set to be $t = 0$ *s*, while the large LOCA is assumed to occur at $t = 1$ *s*. Trip setpoint of LOFA is set at 80% of PHT flow according to CANDU 6 SDS1 design specifications [36].

The entire LOFA and LOCA simulation covers a 9-second interval. Beyond 9 seconds, the boundary conditions of these two simplified open-loop models can no longer satisfy the saturated steam enthalpy requirements to provide meaningful results. Typically, the reactor thermal power surge occurs within the first 1-3 seconds after the initiation of accidents. These thermal power surges are used for safety margin studies.

3.3 Simulation results

Simulation results for critical system variables, such as thermal power and sheath temperature, are collected and compared for the validation purpose. The advantage of a faster shutdown is demonstrated in terms of improvement on safety margin.

3.3.1 Results for the LOFA case

The reactor power transients and sheath temperature transients in the LOFA under different SDS1 response times are plotted in Figure 3.12 and Figure 3.13, respectively.

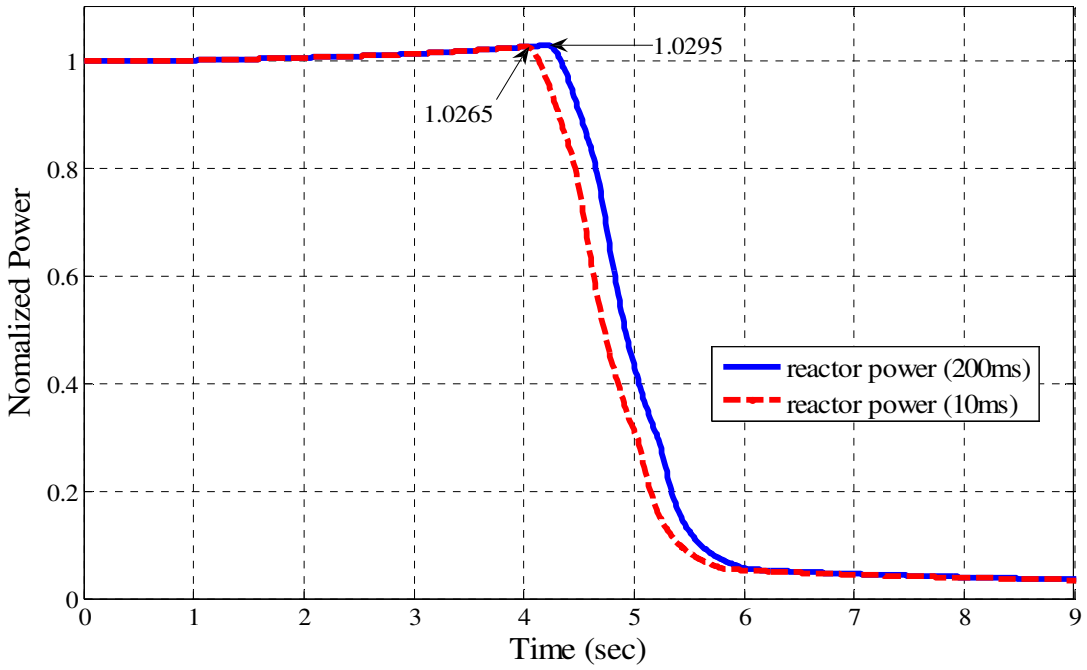


Figure 3.12 – Comparison of power transients in LOFA

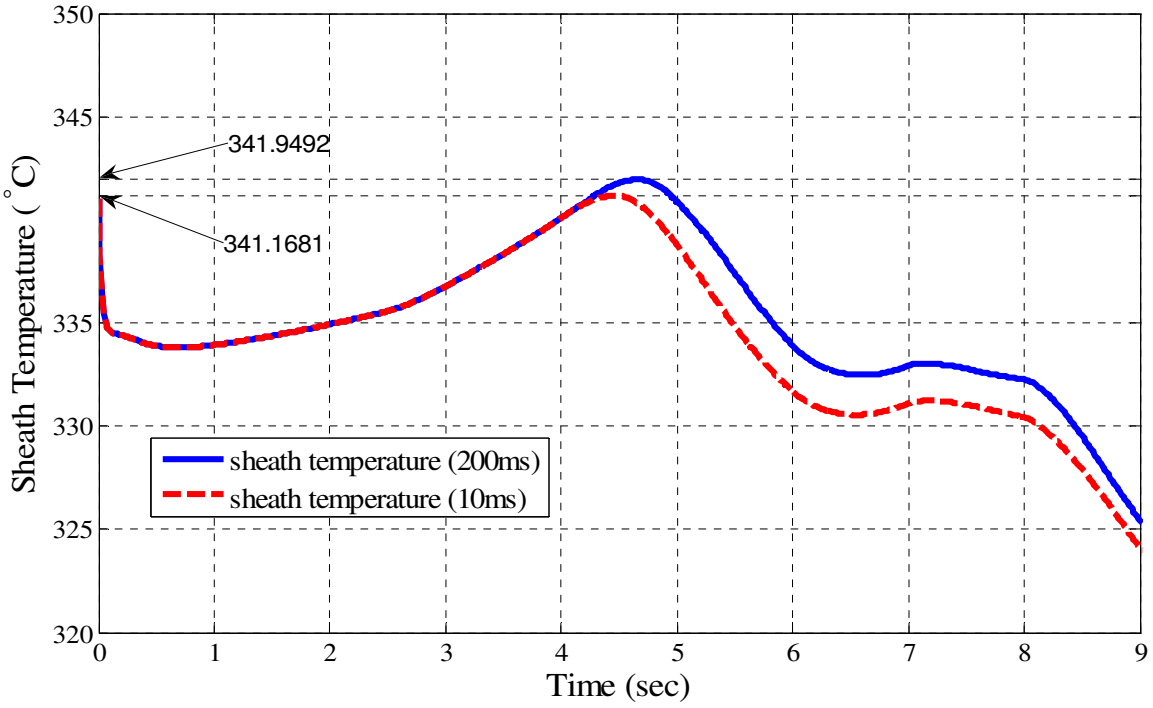


Figure 3.13 – Comparison of sheath temperature transients in LOFA

As can be seen, the differences between the two power surges or the two temperature transients are relatively small. The reason lies in the small reactivity change during the chosen LOFA. Decreasing in the coolant flow, unlike the LOCA, only reduces the heat transfer coefficient at the initial stage. Voiding appears when accumulation of the fuel-generated heat reaches a certain level, which is then capable of increasing the in-core thermal power and sheath temperature. The gradual rising of temperature is a reflection of such phenomenon. The LOFA simulation results also confirm what has been plotted and discussed in Figure 2.4. Accident transients in which there is no dramatic reactivity change show less dependency on the response time of the shutdown systems.

Although there is no significant reduction of the peak power surge by using faster shutdown process, the LOFA simulation results do confirm the feasibility of lowering the

peak of power surge with an increase of shutdown speed. The LOFA simulation also yields a clear indication that safety margin improvement may not be significant for accident cases with slow reactivity increase.

3.3.2 Results for the Large LOCA case

Simulations for 35% RIH break accident present reactor power and sheath temperature transients with respect to three SDS1 response times. Figure 3.14 and 3.15 show these transients and the comparison result is indicated by the labeled surge peak values.

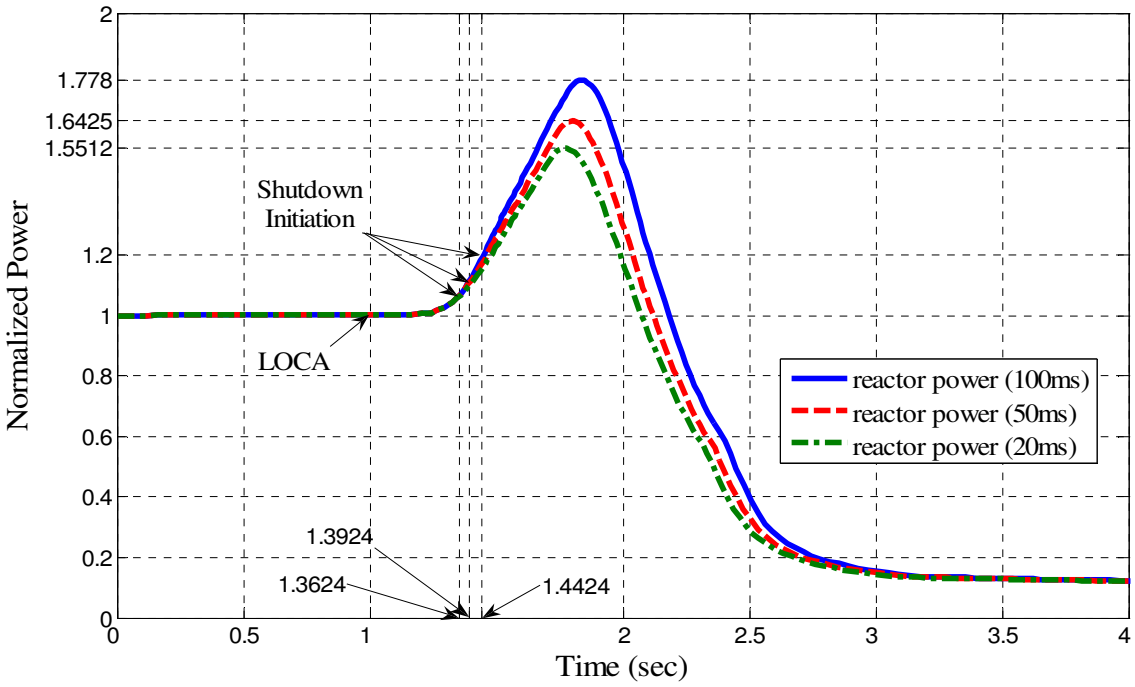


Figure 3.14 – Comparison of power transients in large LOCA

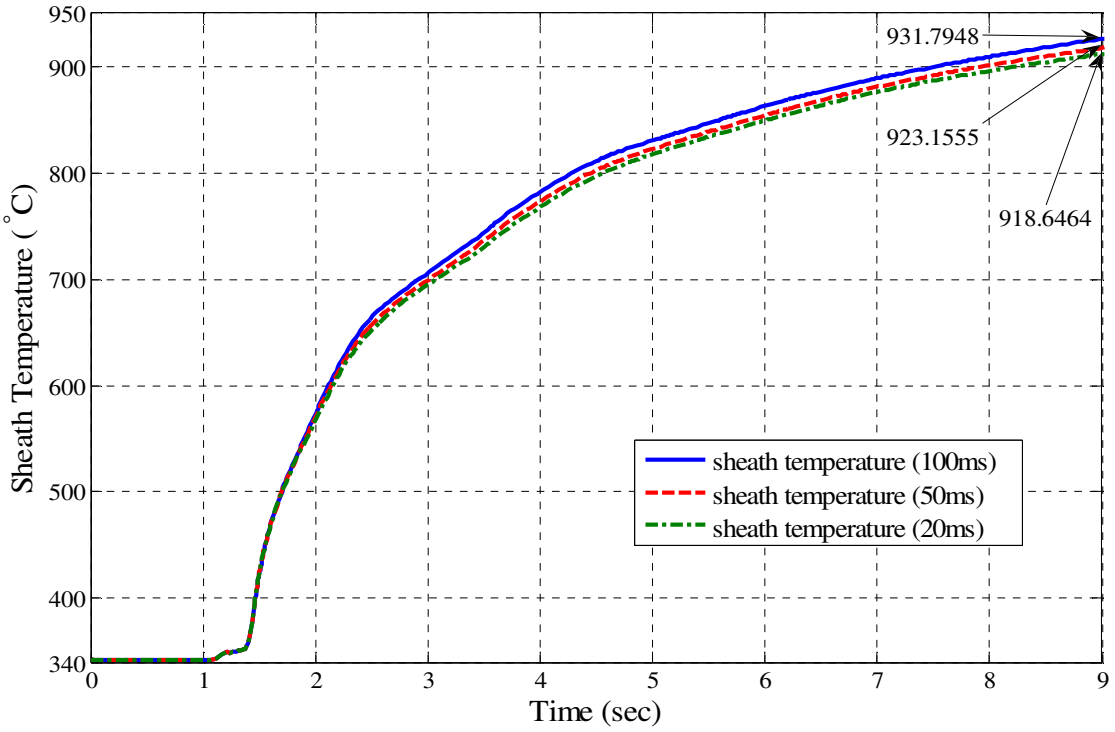


Figure 3.15 – Comparison of sheath temperature transients in large LOCA

It should be pointed out that the sheath temperature has not reached the peak value since there is no ECCS included in this simulation. It takes more than 9 seconds, which is the valid simulation interval for current simulation model, for the temperature transient to reach the peak. However, the simulated transients still present the trend of the increasing sheath temperature can be alleviated by faster shutdown process.

Due to the large and quick positive reactivity introduction in a large LOCA, reactor power rises at expeditious rate. In such a circumstance, the faster shutdown process can have significant influence on the safety margin. Power surges caused by LOCA are reduced clearly in the 50 *ms* and 20 *ms* cases as compared to the 100 *ms* case. As a result, the faster the shutdown process is, the more the margin can be saved.

3.4 Summary

This chapter mainly focuses on the research approaches adopted for thermalhydraulic investigations, including the thermalhydraulic model construction, selection of the accident scenarios, and CATHENA simulation. Purpose of these research approaches is to validate the concept of improving the safety margin via faster shutdown.

The thermalhydraulic simulation model is constructed based on both CANDU characteristics and CATHENA requirements. Simplifications are applied such that the investigations concentrate only on in-core transients. A LOFA that happens in a single fuel channel and a 35% RIH break event, as the worst-case of an RIH break LOCA, are selected as the simulation scenarios. Steady-state conditions are chosen to be the initial conditions for the simulated accidents.

Results of the CATHENA simulation for both cases have demonstrated the correctness and feasibility of the proposed concept. Comparison between the two simulated cases has also shown that this concept can improve the safety of the reactor under accident conditions.

4 SDS1 TRIP LOGIC AND ITS FPGA IMPLEMENTATION

The concept of safety margin improvement has been validated using both analytical method in Chapter 2 and thermalhydraulic simulation method in Chapter 3. An FPGA-based SDS1 has to be designed and implemented to demonstrate practical feasibility of this concept. The SDS1 in a typical CANDU 6 is selected for this purpose. The trip logic within the trip computer is translated into a digital hardware design and implemented on an FPGA system. Following the standard FPGA development procedure, this implementation involves coding, simulation, synthesis, and hardware configuration.

4.1 SDS1 trip logic

The SDS1 trip logic in a CANDU 6 is executed within trip computers called PDCs [55]. Different trip parameters correspond to different safety-critical process variables. Safety-critical variables are measured on-line in real-time and compared against predefined threshold within PDCs. Trip decisions are then passed to the downstream of SDS1 for execution. The trip logic units contains signal conditioning of the inputs, the trip threshold, comparison between the measured system variables and the thresholds, decision of the extensive conditions, and the generation of output trip signals.

4.1.1 PDCs in a CANDU 6 unit

PDC-based SDS1 in CANDU 6 plants is the first computer-based shutdown system in CANDU NPPs. Two PDCs are deployed to deal with seven process-based trip parameters. The other three parameters (neutron power, neutron log rate power, and reactor building

pressure) still rely on analog circuits for trip functions. Hence, CANDU 6 NPPs use both conventional analog logic and computers in their SDS1.

The reasons why CANDU chooses digital computers for the shutdown systems are [55]:

(1) Safety features and production availability can be improved by replacing the obsolescent analog circuit with digital computers ;

(2) The testing loads of the operators can be reduced by using digital computers ;

(3) Digital computers have greater flexibility than analog circuits in logic design; and

(4) Digital computers bring reduced construction and commissioning cost.

Since PDCs were not a part of the initial CANDU 6 design, it had to be retrofitted into the system where most of the setups were designed for relay or analog systems. This integration problem was solved by means of supplementing or replacing some components in the analog design such that the requirements for a new digital system can be satisfied. Therefore, the SDS1 is a system with the trip unit replaced by digital computers but the rest remains as conventional. An overview of a PDC-based trip channel in a CANDU 6 SDS1 is illustrated in Figure 4.1.

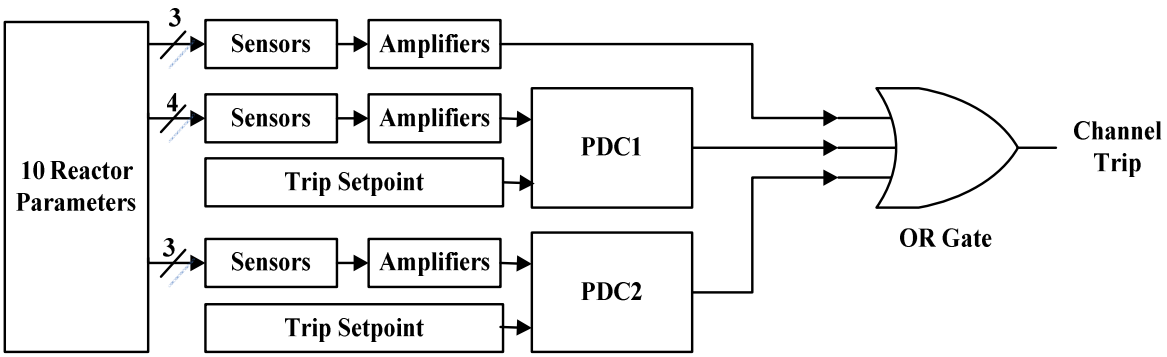


Figure 4.1 – Overview of SDS1 trip channel

As the control unit in SDS1, PDCs acquire trip parameters and make decisions by comparing them against the trip thresholds. For those thresholds dependent to reactor operating conditions, PDCs also calculates appropriate thresholds. Under some special circumstances, it is also necessary for PDCs to consider additional conditions for trip decision. The inputs of PDCs are the sampled and amplified sensor values while the output is normally the trip decision. Since there are two PDCs in a single trip channel, trip decisions from both of them, along with the three analog trip decisions, are combined to form a selection logic (mostly just an OR gate). Output of this selection logic is the channel trip decision. Trip decisions from all three channels are processed by a 2oo3 voting logic to generate the final SDS1 trip signal. This final decision is the signal passed to the clutches for shutoff rods release.

In the revised design of the PDCs, a surveillance unit called “Watchdog” is added [55]. It monitors the update of PDCs. If a PDC does not update its watchdogs for more than 100 *ms*, the watchdog declares a failure of its associated PDC. The watchdog then trips and puts its associated channel in a safe state. PDCs also have a self-testing circuit with the test vectors stored in a programmable read-only memory (PROM). When the self-testing

mode is activated, the inputs of PDCs are switched from the sensor signal paths to the PROM. Test vectors are then read by PDCs and the decision outputs are compared to expected terms from the design specifications. All the trip parameters have corresponding test vectors, thus it is possible to test the PDCs ability for all the trip parameters. This automatic test feature makes the maintenance more cost-effective. Since PDCs have brought proven benefits to CANDU NPPs and the operating experience has verified their adaptability and reliability, the Canadian nuclear industry has further developed a fully computerized shutdown systems that integrate PDCs and other computer-based components in the Darlington NPP [51, 104]. It has been confirmed that adoption of digital computers did enhance the plant safety and performance. But challenges appear with the increasing demand for system safety [144]. After nearly two decades of infield service, these systems are facing additional new challenges such as obsolescence problems and availability of alternative technologies.

As mentioned in Chapter 3, there are a total of ten trip parameters in the CANDU 6 SDS1 trip logic. Seven of them are process-based and processed by PDCs, while the other three use conventional analog circuits. The trip parameters such selected that they can cover most of process failure scenarios. The SDS1 Trip parameters, setpoints, and protective coverage are summarized in Table 4.1 [36].

Table 4.1 SDS1 Trip Parameters and Setpoints

	TRIP PARAMETERS	DETECTOR TYPE	SETPOINT	CONDITIONING PARAMETERS
1	High Neutron Power	Vertical in-core detectors	ROPT-HSP-1 122% ROPT-HSP-2 109.3% ROPT-HSP-3 83.3%	Setpoints adjusted by handswitches
2	Rate Log High Neutron Power	Ion chambers	10% per second	N/A
3	Reactor Building High Pressure	ΔP transmitters	3.45kPa	N/A
4	Primary Heat Transport Low Flow (PDC1)	ΔP transmitters	80% of nominal flow at FP in instrument	Channels 1. Conditioned out when ionization chamber $\Phi_{LOG} < 0.1\% FP$ 2. Trip setpoint modified by pump mode handswitch
5	Moderator High Temperature (PDC1)	RTDs	$87°C$	N/A
6	Pressurizer Low Level (PDC1)	ΔP transmitters	Function of the reactor power	1. Trip setpoint modified by pump mode handswitch. 2. Setpoint determined by flux detector signals Φ_{AVEC} 3. Conditioned out when: a. $\Phi_{LOG} < 1\% FP$, and b. $\Phi_{AVEC} < 10\% FP$
7	SG Low Level (PDC1)	ΔP transmitters	Function of the reactor power	1. Setpoint determined by flux detector signals Φ_{AVEC} 2. Conditioned out when a. $\Phi_{LOG} < 1\% FP$, and b. $\Phi_{AVEC} < 10\% FP$

8	HTS High Pressure (PDC2)	Pressure transmitters	Relief valves – 10.24MPa (g) Immediate trip – 10.45MPa (g) Delayed trip – 10.24MPa (g) 3 s delay	1.Immediate trip setpoints modified by pump mode handswwitch 2. Delayed trip conditioned out when shading corrected ion chamber line signal $\Phi_{LINC} < 70\%$
9	HTS Low Pressure (PDC2)	Pressure transmitters	Function of reactor power	1. Conditioned out when $\Phi_{LOG} < 0.1\% FP$ 2. Setpoint is function of Φ_{LINC} 3. Trip setpoints modified by pump mode handswitch
10	SG Feedline Low Pressure (PDC2)	Pressure transmitters	3.9MPa (g)	1. conditioned out when $\Phi_{LOG} < 9\% FP$
11	Manual Trip	N/A	N/A	N/A
12	Start-up Count Rate	N/A	N/A	N/A

* ROPT—Reactor Overpower Trip; FP—Full Power; Φ_{LINC}: Ion chamber line signal (neutron flux); Φ_{AVEC}: Ion chamber signal average (neutron flux); Φ_{LOG}: Ion chamber signal log rate (neutron flux); HTS: Heat Transport System.

Distribution of trip parameters in PDC1 and PDC2 is illustrated by logic structures in Figure 4.2 and 4.3 respectively. Manual trip signals are not shown because they are mandatory commands issued by the operators. Multiplexers are used as a signal selector such that the extensive conditions can determine the validity of the trip signal.

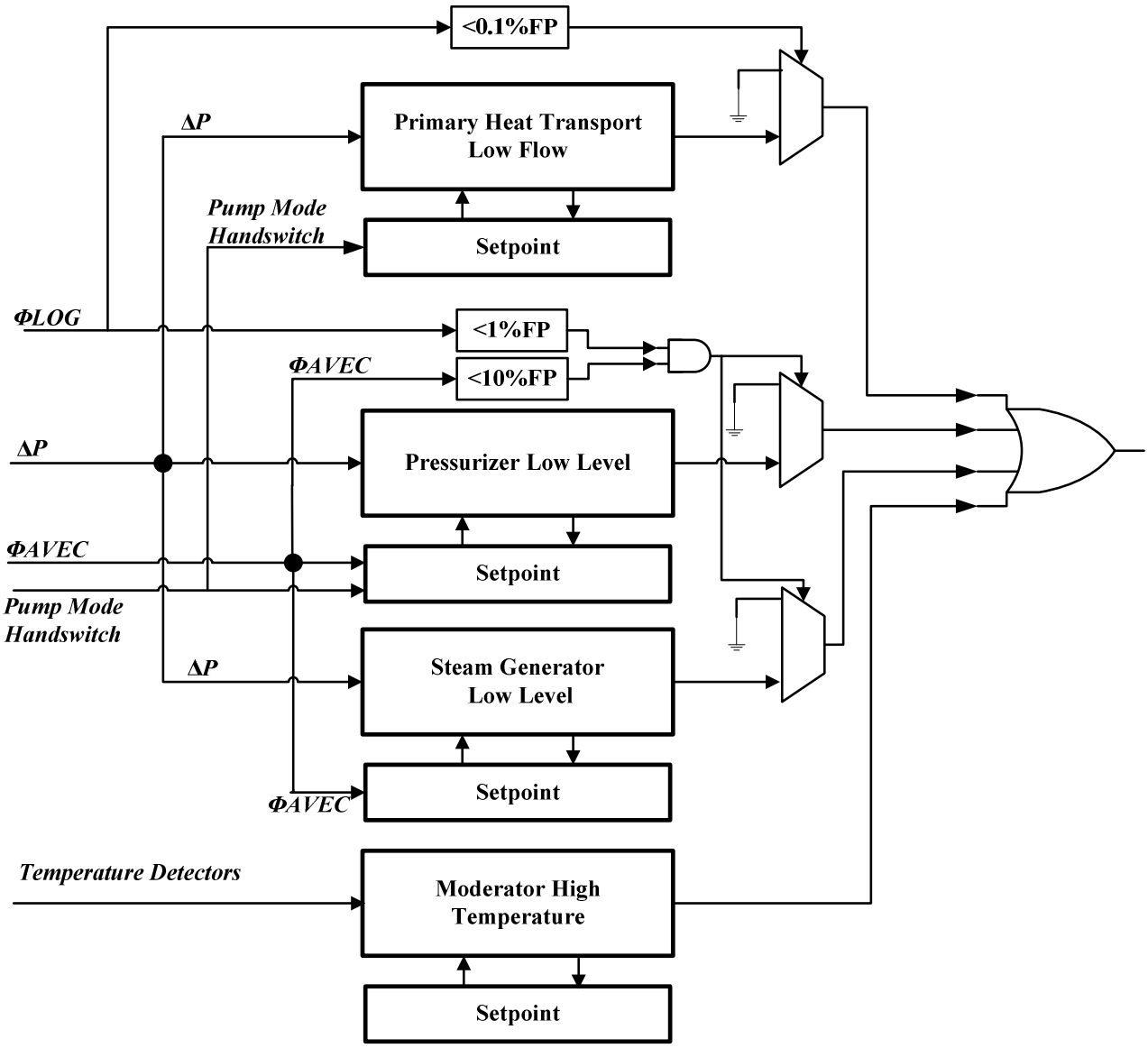


Figure 4.2 – Trip logic structure in PDC1

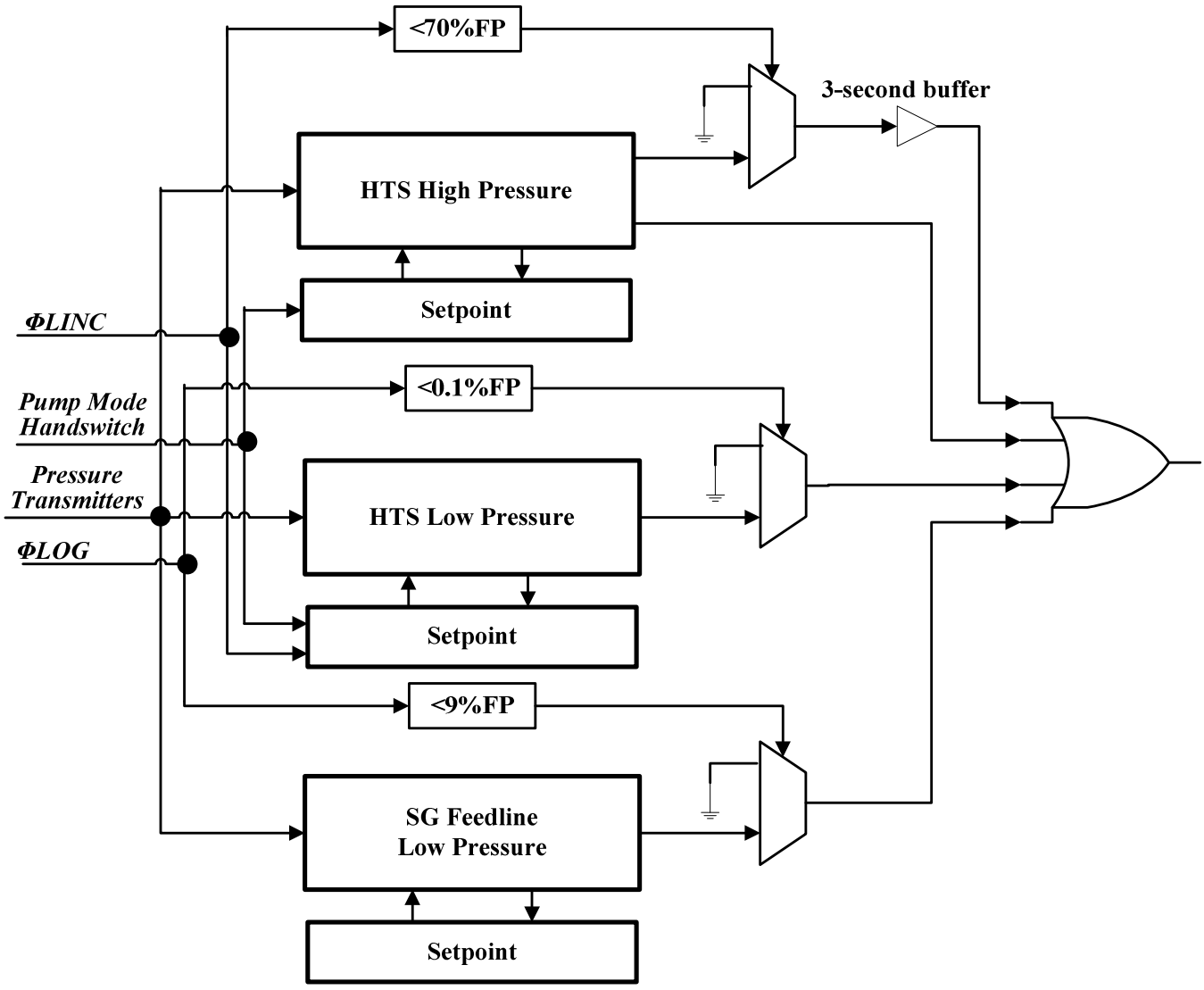


Figure 4.3 – Trip logic structure in PDC2

The logic structures provide a systematic description of PDCs, in which the logic flow and component connections are clearly illustrated. Since the connection of this logic flow has been validated by infield experiments and operations in NPPs, it will be used as the reference for the FPGA system design in this thesis. Function blocks and interactions of the FPGA system are defined and specified based on the PDC specifications such that the SDS1 functionalities can be preserved.

4.1.2 Trip logics

The essential trip logic in the SDS1 consists of two major steps: acquiring critical plant variables in real-time and comparing them against the setpoints, which themselves can be functions of other system variables (e.g. reactor power). A trip decision is made depending on the results of the comparison. It is important to emphasize that, as the information propagates through the logic, some data processing procedures are required. For example, the sensor data may need to be preprocessed before they can be used for logic operation. The pre-processing also takes time. In a software-based implementation involved with operating systems, several computer instruction cycles have to be used to complete a single operation. A trip function may be composed of several internal CPU operations. When the functions are realized on an FPGA platform, some of the processing can be carried out in parallel, hence, to shorten the decision-making time.

In practice, many accident or incident conditions can lead to a forced trip of an NPP. In this study, the “SG low level” scenario has been selected for the functionality evaluation of the current FPGA-based SDS1 implementation. The reasons to choose this scenario are: 1) the signals to indicate “SG low level” pass through PDC1 which will be replaced by the FPGA based implementation; 2) “SG low level” is one of the commonly reported

incidents in existing NPPs; and 3) the results are very intuitive when the SG levels are being observed on the simulator. The trip parameters for the "SG low level" scenario involve more than just SG levels. In fact, because the level depends on the reactor power, the setpoint is also a function of the reactor power. The setpoint determination involves sorting and range checking calculations. These operations do take time when implemented in a digital computer, such as PDC1.

The actual shutdown logic in the "SG low level" scenario is illustrated in Figure 4.4:

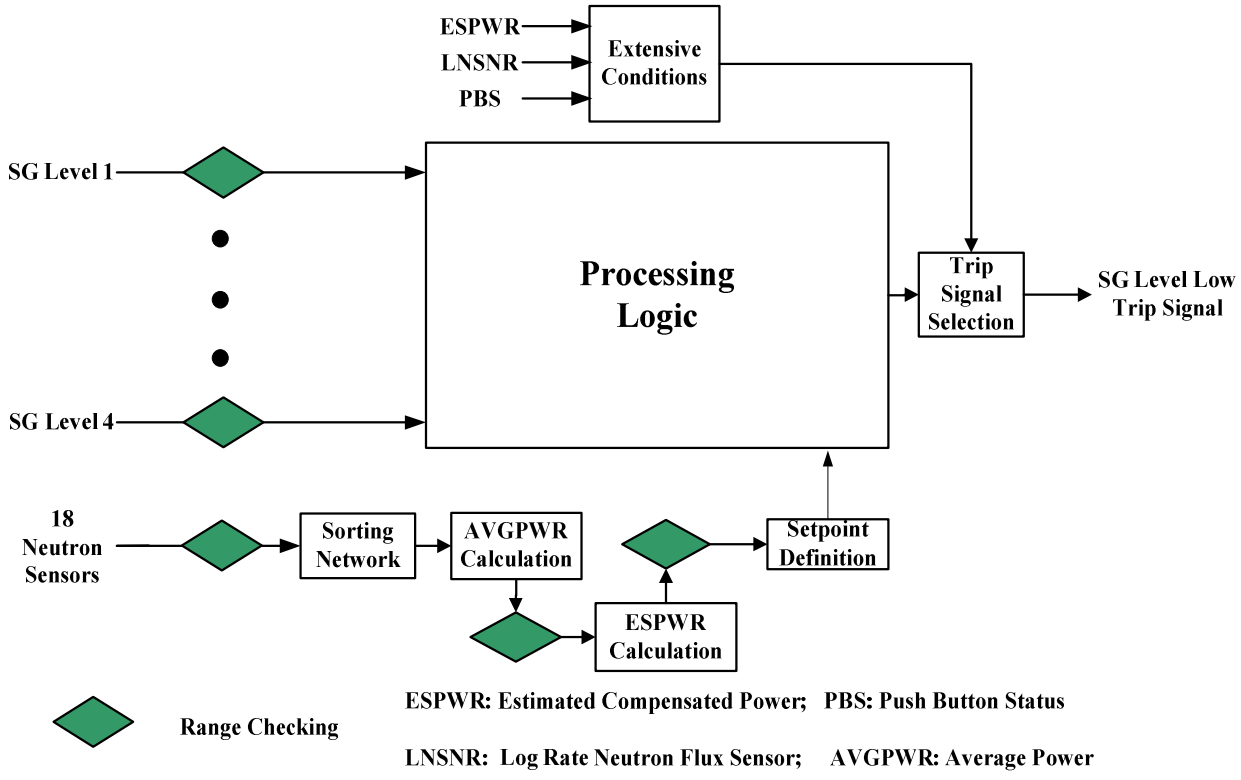


Figure 4.4 – SG low level trip logic

As can be seen from Figure 4.4, in the PDC1 logic structure, the "SG low level" trip logic can be divided into several major function blocks:

(1) input signal processing including range checking and sensor value sorting;

(2) setpoint conditioning since the setpoint depends on the reactor power;

(3) processing logic where the trip decision is made;

(4) extensive conditions that validate the trip decision; and

(5) the trip signal selection in which the final trip decision is made.

The FPGA design has to take these function blocks into consideration in order to implement the functionalities and satisfy SDS1 requirements. Only in such a premise can the FPGA design introduce advanced techniques such as parallel processing to the implementation. One thing needs to be clarified is that, even though the input signals appear to be in a parallel pattern in Figure 4.4, the actual processing within the PDC is still serial in nature because the algorithm is executed by a microprocessor-based system, so is the sorting of the 18 neutron sensor values. The FPGA design can handle such kind of issues using parallel processing techniques.

4.2 Implementation of SDS1 trip logic on an FPGA platform

The “SG low level” trip logic is used as an example for the FPGA design. The process to implement FPGA-based “SG low level” trip logic” can be divided into four major steps: 1) system design; 2) hardware programming; 3) functionality validation; and 4) final implementation on FPGA chips.

The system design starts with a sketch of the system overview, which is a function block diagram. Each function block in the sketch is complemented with detailed specifications. How the FPGA design takes advantage of parallel and hardware processing is described in detail.

After the functionality of each component is specified, VHDL programming environment is used to synthesize the desired functions. VHDL stands for VHSIC (Very High Speed Integrated Circuits) Hardware Description Language. It is used to code text models that describe logic circuits [145]. The synthesis process translates high level algorithmic operations into register-level or gate-level specifications, i.e. specifications at a circuit level.

Once the synthesis part is complete, the function simulation can be carried out by applying test vectors to the inputs and verifying whether the outputs match the expected ones. The entire verification step is performed within the software design environment. This verification process can detect design flaws in the function specification, data path, and logic control within the simulation coverage, so that corrections can be made.

Once all the logic is validated, the system design is considered complete. At this stage, the designed system can be downloaded to an FPGA chip according to the selected register maps. An EDA tool can be used for selection of routing of signal paths and placement of logic elements. Once this step is accomplished, the implementation of FPGA-based system is considered to be completed. In practice, extensive testing will have to be performed to valid the performance of the system. This is, however, not the focus of this thesis.

4.2.1 System design

An overview sketch for the main functionalities of SDS1is drawn based on the PDC logic structures. The sketch contains the same major function blocks as discussed in Section 4.1.2. In this first step, the digital system architecture of PDC logics, sub-systems, functionalities of each subsystem, and the relationships among them have to be designed. In this case, the overall system architecture is shown in Figure 4.5:

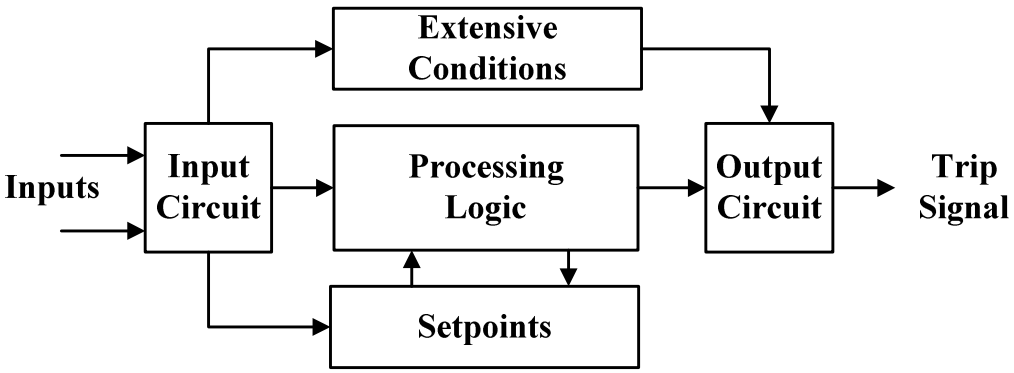


Figure 4.5 – System architecture of the FPGA-based SDS1

When applied to "SG low level" logic, the specific functionalities of each functional block in Figure 4.5 can be summarized as follows:

(1) The input circuit is responsible for pre-processing of the measured input signals. All signals are synchronized to the on-board system clock. Measurements from the 18 neutron detector are also sorted at this stage. Data range of all the inputs is also checked to ensure that they are valid.

(2) The desired trip thresholds are stored in the setpoint registers. For different trip parameters, the trip thresholds are distinctive. In the current work, since the algorithm for both the average power and the estimated power is not

available, the trip thresholds are assumed to be pre-determined and stored in the registers. The design process then is simplified as follows: once the sorting process is complete, an "enable signal" is passed to the threshold registers in the next step. The stored threshold values are then fetched for comparison purpose.

(3) Once the SG levels and the trip thresholds are established, the processing logic then is in the decision-making unit for trip decisions. Four inputs of the SG levels are compared to the stored thresholds by the processing logic. If the trip condition is established, the trip signal is then issued to the output circuit for trip execution.

(4) The "Extensive Conditions" block is another decision-making unit that determines whether or not an extensive condition is effective for the trip status confirmation. The reason for this part is because the reactor does have certain special operating status. For example, when the neutron flux log rate is less than that of 1% full power and the average neutron flux is less than that of 10% full power, the "SG low level" condition is considered as an unnecessary trip parameter.

(5) The output circuit consists of a multiplexer that is controlled by the extensive condition unit. If the extensive conditions stand, no matter what status the sensor trip signal is, the final trip decision will be overwritten. Another signal that controls the output circuit is the manual push button signal. When the

push button signal is received by the output circuit, the trip signal will definitely be issued regardless the outcomes of other decision-making units.

Remark: Due to I/O port limitations of the FPGA platform used in this prototype work, 18 neutron sensor values are stored in registers. They become available to the system once the SG level measurements reach the input circuit. The extensive condition part is also simplified since neither the estimated power nor the log rate neutron sensor signals is available for this work. This simplification has virtually no effects on logic complexity. The overall logic is still more complex than that is implemented in [146]. The system description of the designated FPGA system based on above specifications can be illustrated in Figure 4.6.

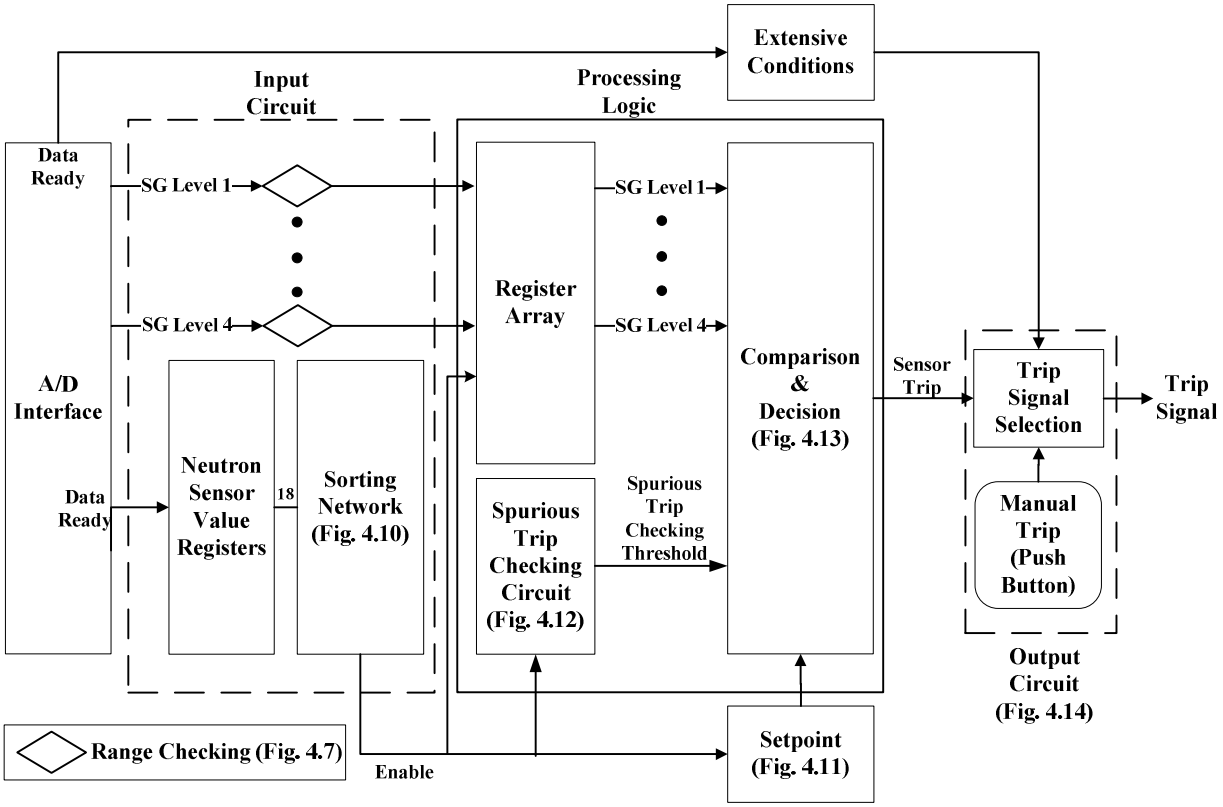


Figure 4.6 – System description of the FPGA-based "SG low level" trip channel

An analog to digital (A/D) chip is used as an interface between the test signal source and the FPGA system. Detailed description of each block used in the FPGA implementation is elaborated next.

4.2.2 Input circuit

The input circuit is used for pre-processing of the input signals. Pre-processing is absolutely necessary to maintain the correctness of the subsequent logic processing. Input signals have to be validated for their proper ranges before being passed to the rest of the system. Sometime sorting of input signals is also required for calculating the parameter-related setpoint. In the "SG low level" logic, both "range checking" of the input values and sorting of values from 18 neutron detectors are required. The input circuit is designed for these two functionalities.

(1) Range checking

The range checking is performed by comparing the input value against its upper and lower limits defined in the regulations. Only when the value is within these limits, the value is treated as a valid measurement. In the current design, a parallel processing algorithm is utilized.

In total, there are four SG level signals and 18 neutron sensor measurements. 22 range checking circuits are implemented such that each signal has its own circuit to eliminate waiting time at this stage. All these 22 range checking circuits perform the checking simultaneously once the data arrive. Although in the current design the 18 neutron values are pre-stored in a register array, the range checking is still performed when the "data ready" signal reaches the input circuit. Secondly, for each range checking circuit, the

value is compared against its upper and lower limits again in a parallel manner. Two comparators, one for each limit, are implemented. Thus, two comparison steps are executed simultaneously. The result of one limit checking is a Boolean value. As long as the input value is between the upper and lower limits, an enable signal will be sent to the register to release the values to the subsequent logics. Figure 4.7 provides the details of such a parallel range checking circuit.

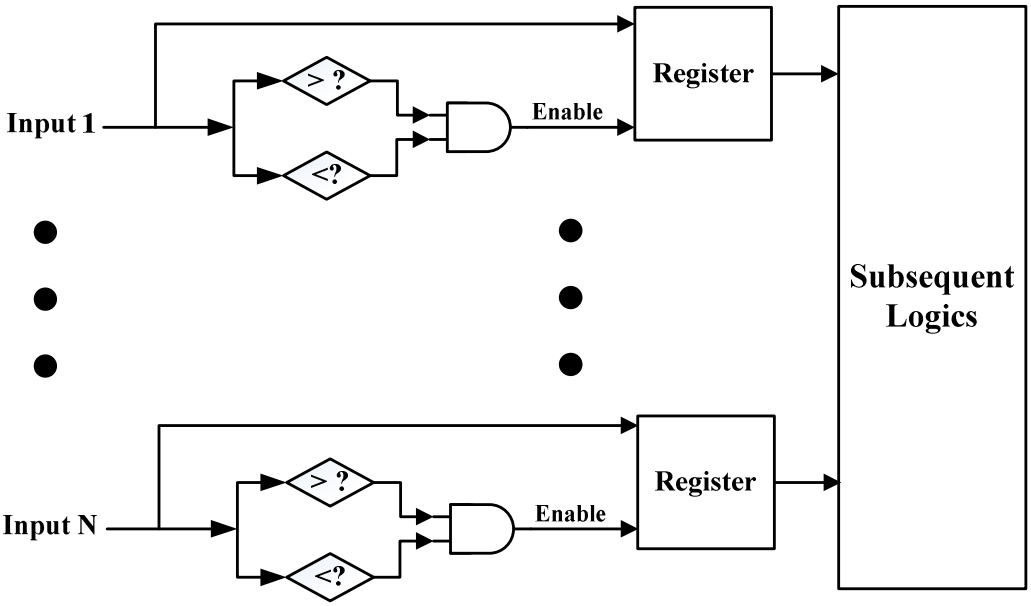


Figure 4.7 – Parallel range checking circuit

By processing data in parallel, waiting time is eliminated and the efficiency is enhanced. Comparing to a serial processing, such design can shorten the processing time. The price to pay is to use additional hardware resource for implementing the identical circuits. Fortunately, today's FPGAs have high density of logic elements and the increase in hardware resource requirement is not a concerned issue.

(2) Sorting network

In additional to range checking, sorting is also needed for the 18 neutron sensor measurements. This is because the threshold for the "SG low level" trip logic is a function of the reactor power. The 16 highest neutron sensor values from the 18 detectors have to be selected for setpoint calculations. Due to the fact that the specific setpoint calculation algorithm is not considered in this work, a predefined setpoint is stored in the register arrays. It is available to the processing logic once an "enable" signal representing sorting completion is issued from the sorting network.

To sort the values from 18 neutron detectors using a parallel processing scheme, the Batcher-Merge sorting algorithm is utilized [147]. Although this algorithm was developed originally for parallel processing system using multiple microprocessors, its sorting structure is ideal for hardware implementation. An illustrative diagram for an 8-element Batcher-Merge sorting network is presented in Figure 4.8.

The sorting algorithm can be decomposed into several simpler units with which 2 input values (a1 and a2) are to be sorted. Each unit is nothing but a comparator. A bottom-up sorting unit assigns the larger value to b2 and the smaller value to b1. This is opposite in a top-down sorting unit. The sorting in Figure 4.8 can be divided into three steps: 2-element sorting (which corresponds to the four sorting units in the left column), 4-element sorting (which is the top left and bottom left partitions), and the 8-element sorting (which is the rest of the network). Sorted elements are merged into the next stage. Sorting operations in the same process are carried on simultaneously in parallel fashion. This is shown at the first column that all the 2-element sorting operations are done at the

same time. A signal representing completion is sent by each stage to enable the next stage such that the pipeline processing is ensured.

To clearly show how the sorting is processed, an unsorted array, (7, 4, 3, 5, 8, 1, 2, 6), is fed to the inputs of the sorting network in Figure 4.8. Each sorting unit relocates the input values to its corresponding outputs. For example, in the bottom-up sorting unit at the top-left corner, the input 7 is relocated to the pin of b2 since 7 is bigger than 4. Following such a processing principle, the output of the entire sorting network is a sorted array (1, 2, 3, 4, 5, 6, 7, 8).

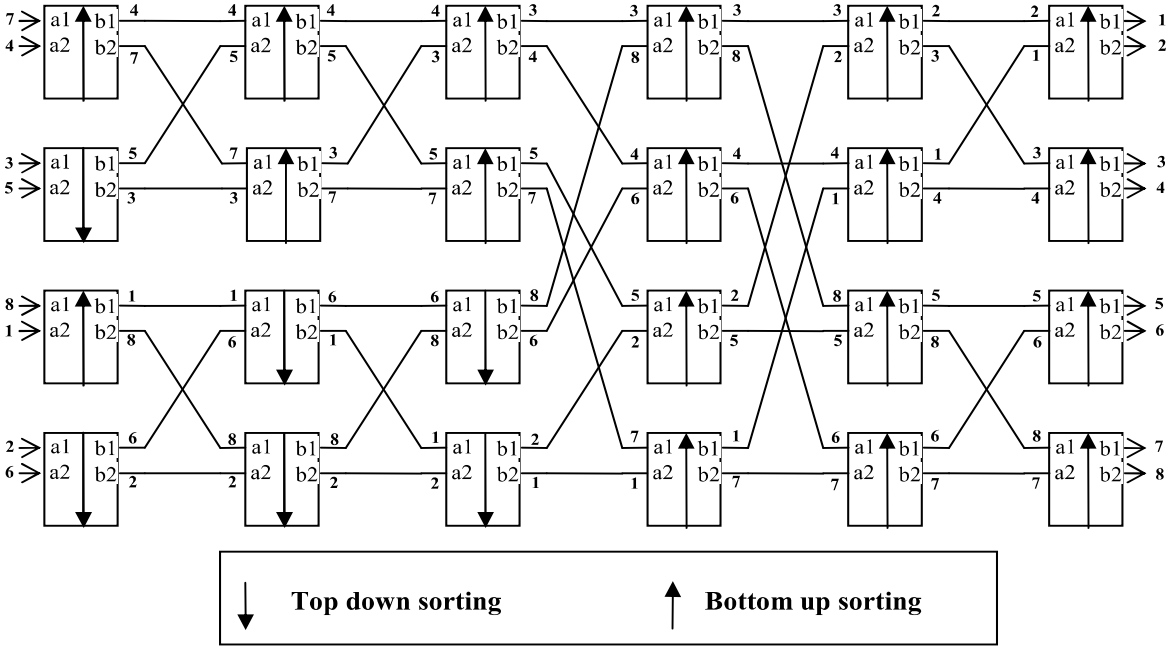


Figure 4.8 – An illustrative diagram for Batcher-Merge sorting network

The entire sorting network consists of six stages (columns). Because the dataflow goes from the inputs (left) to the outputs (right) stage by stage and every stage executes the processing simultaneously, such a layout of the sorting network allows for pipeline implementation to increase the processing speed. Six stages are illustrated in Figure 4.8,

which forms a six-step pipeline. This is the one of the primary reasons why FPGA implementation can speed up the logic processing process. Such a sorting scheme does not need any memory storage, and no operating systems are involved. The sorting units can be implemented by using integrated circuit elements on an FPGA platform. Moreover, in the case of pipeline implementation, each stage of the sorting network is controlled by a clock signal. Therefore, one can attain different processing speed by using different clock frequency.

Based on the sorting algorithm in Figure 4.8, this thesis work develops the 16-element sorting network for the "SG low level" trip logic. Slight revisions are made such that the element integration and the VHDL coding are simplified. The 16-element sorting network is indicated in Figure 4.9. Comparing units are the same as those in Figure 4.8.

There is an issue for the sorting network that needs extra attention. This network is only suitable for an input set that has 2^n (n=1, 2 …) elements; but there are 18 neutron values in the "SG low level" trip logic. The solution for this problem is: 1) 16 of the 18 neutron values are sorted first; 2) the sorted smallest value (O16) is then compared to one of the two unsorted values to pick up the bigger one which can be add it to the sorted set; 3) steps 1) and 2) are repeated for the last unsorted value. Thus the 18 values have to go through two 16-element sorting networks and two comparators. At last a set of 16 biggest values out of an 18-value set is generated. This is then what the trip logic needs for setpoint generation. One should be aware that the final 16 outputs are not necessarily sorted since what the system needs are only 16 biggest values out of the 18 inputs. The described "16 of 18" solution is presented in Figure 4.10.

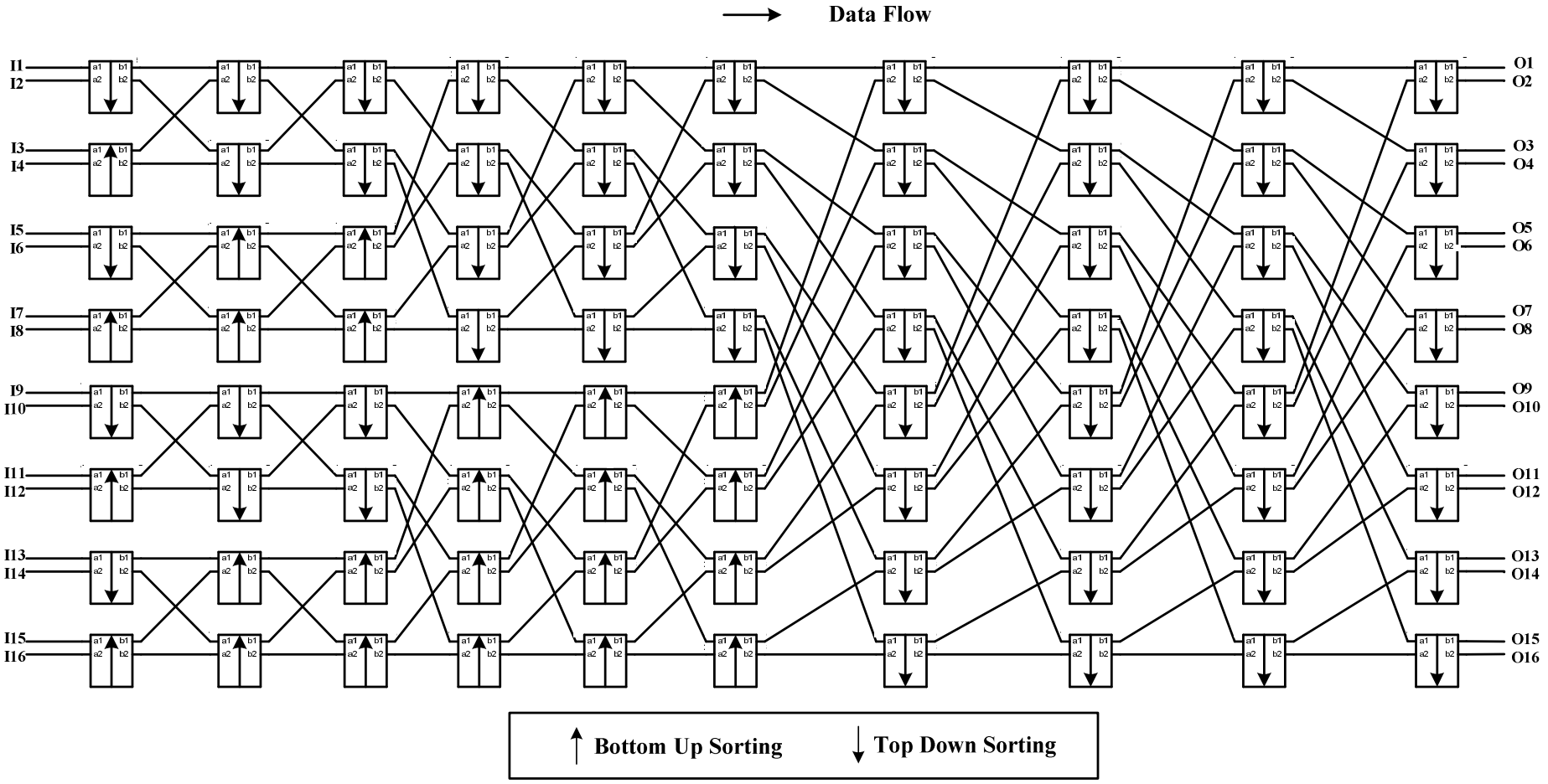


Figure 4.9 – 16-element sorting network

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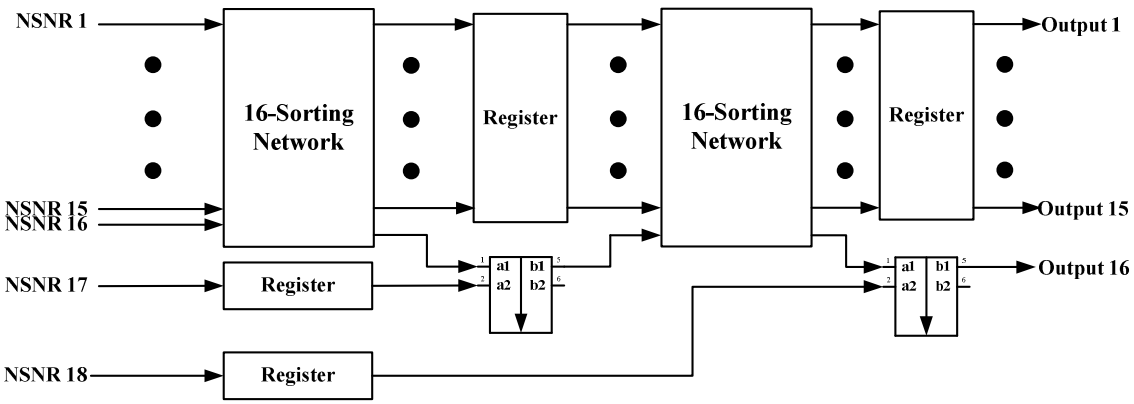

Figure 4.10 – The "16 out of 18" method

4.2.3 Setpoint register

The water level setpoint for the "SG low level" trip logic is set to be 2.00 *m* within a 0-6 meters full level range [146] for two reasons: 1) Presently there is no enough knowledge for the setpoint calculation algorithm; and 2) it is set so for the convenience of applying the industry grade NPP simulator to the HIL simulation. In such a setup, any SG level lower than 2.00 *m* will trigger the SDS1 to issue a reactor trip signal.

As for the binary representation of the setpoint, it is scaled according to the binary value of the input SG level converted by the A/D converter. The A/D interface converts the input analog voltage signals into 12-bit digital signals. It uses 1 *V* and 5 *V* as the low and high references, respectively. Thus, the signal with a magnitude of 1 *V* comes from the simulator represents 0.00 *m* of the SG level while 5 *V* signal is for the 6.00 *m*, i.e. the highest level. For the 2.00 *m* setpoint, the corresponding voltage is

$$SP_V = \frac{2}{6-0} \times (5-1) + 1 = 2.33V \tag{4.1}$$

Since 5 V is the highest input voltage, it corresponds to the biggest 12-bit binary value $(1111,1111,1111)_2$. The binary value of the setpoint that should be stored in the register is then determined as:

$$SP_b = \frac{SP_V - 1}{5 - 1} \times (1111,1111,1111)_2 = (0101,0101,0101)_2 \tag{4.2}$$

This binary value is then stored in a register array as illustrated in Figure 4.11, where each register holds one bit. Once the "enable" signal arrives, the stored value is made available to the processing logic.

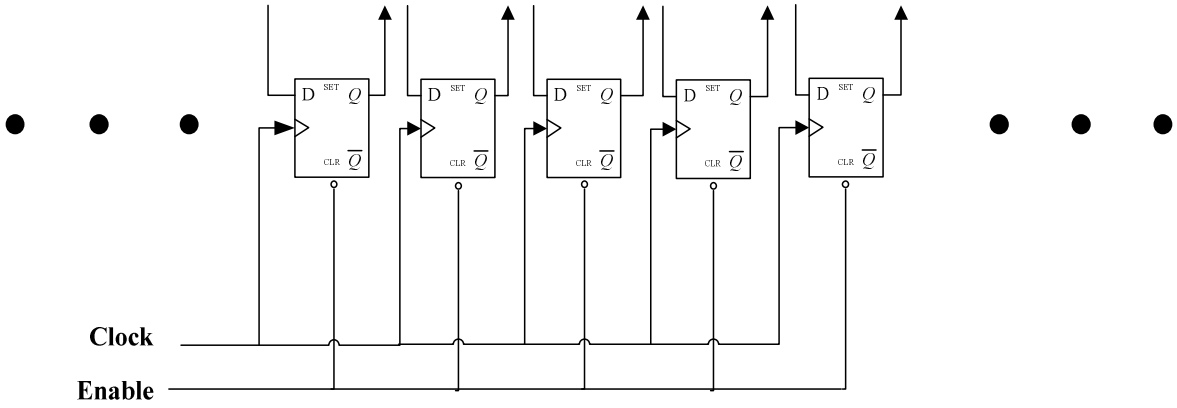

Figure 4.11 – Register array for setpoint storage

4.2.4 Extensive conditions

According to Table 4.1, there are two extensive conditions for the "SG low level" trip logic. In practical NPPs, when both the neutron log rate signal and the average neutron signal are lower than the prescribed limits, the reactor is operating at low power level. This could happen such as the reactor is at a start-up state. In this case, the decision from the processing logic should be bypassed since the SG level is not used in the trip decision.

However, in this work it has technical difficulty to extract the two neutron-related signals from the simulator; hence this part has not been realized. The extensive condition block in the system design is then simplified as a selection signal generator activated by the "data ready" signal from the A/D interface. The Boolean value of the selection can be changed by a switch on the FPGA development board. It is an alternative way to simulate extensive conditions under the current circumstances.

4.2.5 Processing logic

The processing logic is the central unit of the trip logic, where the sensor trip decisions are made. A parallel processing scheme is again utilized to process all the four input SG levels. Four subgroups of identical processing logic are developed thus each SG level input uses its own. It not only shortens the processing time, but also prevents whole system failure if a single circuit is used. The faults, defects, or even failures occurred in one subgroup are isolated, which ensures that the system is able to perform its most functionalities in the presence of single circuit failure.

As for the processing logic, it contains simple comparators in the current design as in both the relay design and the microcomputer design [55]. However, during the simulation work, there was signal oscillation in both the signal source and the FPGA chip. The reason has been traced to the background noise and the device output uncertainties. The input value oscillation near the trip threshold can easily confuse the processing logic, which leads to frequent jitters at the output trip signal. As a result, the system always generates spurious trip signals. The reliability level becomes unacceptable since the system does not give authentic reflection of the actual scenarios.

To solve the trip signal jitter problem, the oscillation issues have to be resolved. It is found that a single trip threshold divides the signal transient into only two stages: trip and not trip. When oscillation happens around this single trip threshold, the trip signal flips with the oscillation.

The solution is given by adding one more threshold as the trip decision reference. The processing logic is programmed as a state machine that makes trip decision with consideration of both thresholds. The extra reference threshold is set to be higher than the actual trip threshold. The transient of the oscillation is now divided into three stages (top, middle, and bottom) by the two thresholds. Top stage is safe and a trip signal is unnecessary. The bottom stage means the SG level has go below the trip limit and the trip signal has to be issued. At the middle stage, the system considers “not trip” if the transient comes from the top stage while “trip” if the transient is from the bottom stage. Only when a transient from the bottom stage goes beyond the reference threshold will the trip signal be eliminated. The design principle is illustrated in Figure 4.12. The system now judges the trip status with one more concern and the jitters of the trip signal are eliminated. With the reference threshold, the processing logic can be more aware of the approaching accident scenario such that the probability of successful accident detection is increased. Moreover, the reference threshold provides double confirmation for trip signal elimination, which prevents possible missed detection of the trip status.

The added threshold is stored in a register array as well. Both the reference threshold and the trip threshold are made available for the processing logic by the “enable” signal from the sorting network.

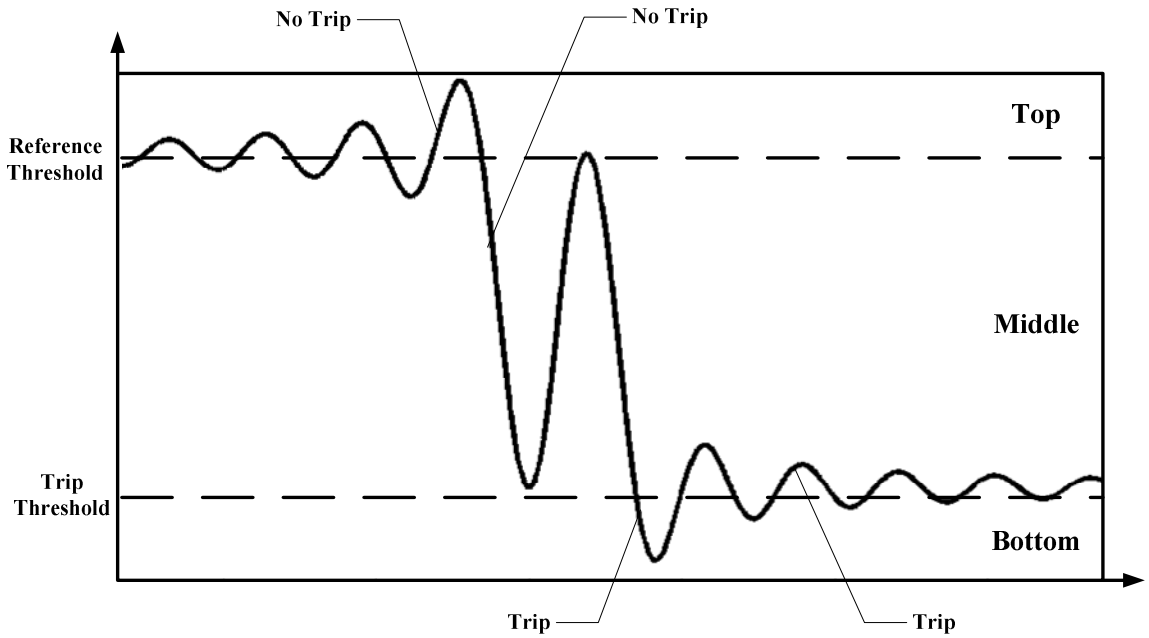

Figure 4.12 – The two-threshold design

The state machine for the two-threshold scheme is specified as following:

(1) There are totally four states: Idle, Top, Middle, and Bottom;

(2) The Idle state corresponds to the system reset signal, i.e. the system is forced to Idle state by the reset signal no matter which state it currently resides;

(3) The other three states are based on the stage of the current signal; and

(4) The change in the transient stage activates a state transition and related signals will be issued.

The detailed state diagram is shown in Figure 4.13.

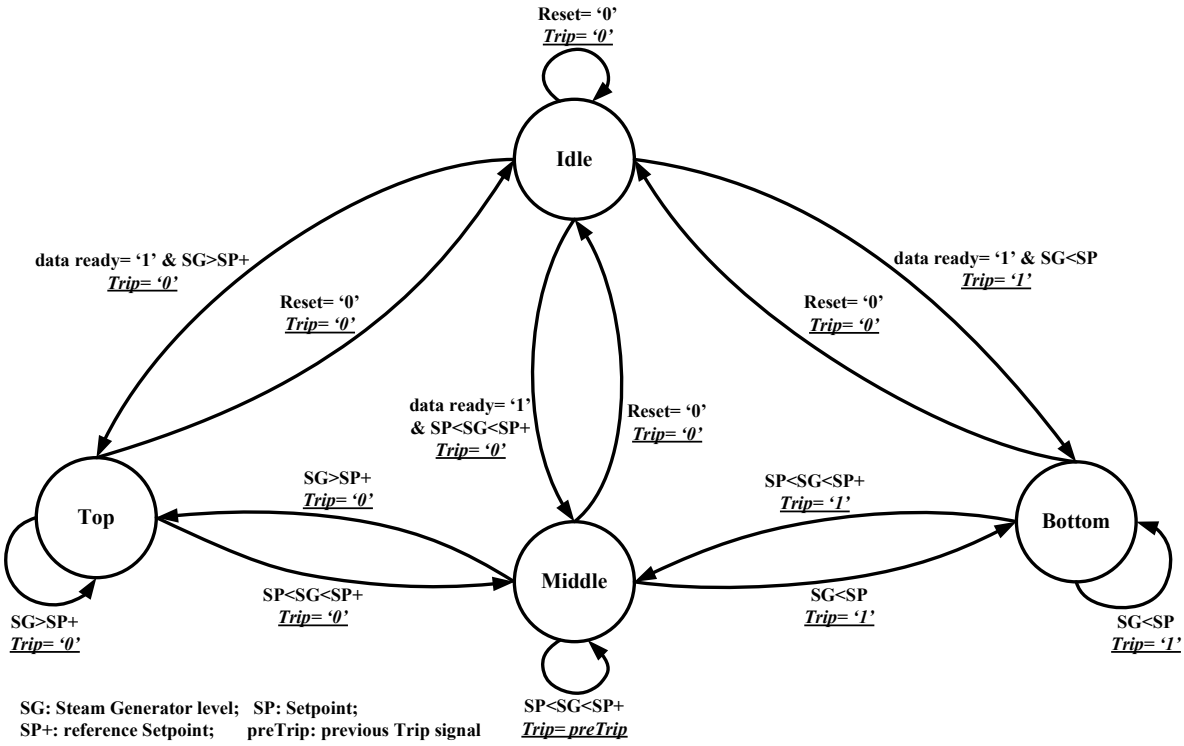

Figure 4.13 – State diagram of the processing logic

Since the decision logic is simple, the reset signal and the clock are both selected as system-global. As a result, the implementation of pipeline processing is straight forward and the signal communication is synchronous. Within a highly synchronous system, extra components are not necessary to coordinate communications between different clock domains. Consequently, the performance of the system is highly effective.

4.2.6 Output circuit

The first part of the output circuit acts as a multiplexer in which the output is determined by a selection signal. The selection signal, as previously mentioned, comes from the extensive conditions. In the current work, the system is simplified and there are only two inputs to the multiplexer: sensor trip from the processing logic and a grounded pin. If the extensive conditions are established, the grounded pin is selected as the output to bypass

the sensor trip decision. But the extensive conditions have lower priority than an operator-issued manual trip. Therefore, following the multiplexer, an OR gate is used to connect both the selected output and the manual trip signal. In a practical NPP, the manual trip signal is connected to the output of a 2oo3 voting logic such that it has the highest priority to bypass all the trip decisions from SDS1. Figure 4.14 shows structure of such an output circuit.

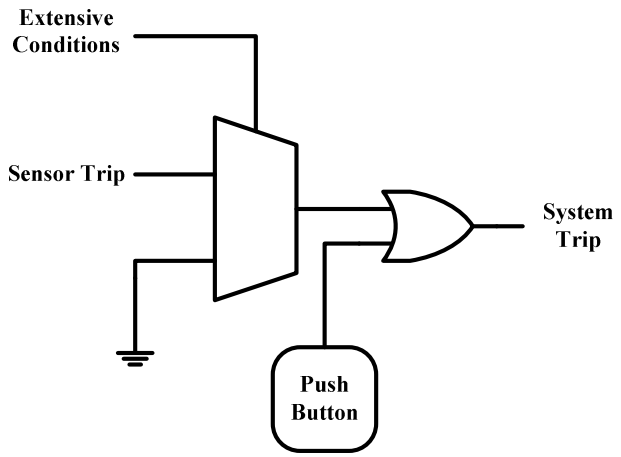

Figure 4.14 – The structure of the output circuit

4.2.7 Implementation details

After all the detailed designs are complete, the implementation process is initiated.

First of all, VHDL coding is carried out based on the component specifications. Components only need to be coded once. For multiple uses of one component, such as the sorting units in the sorting network, duplicated instances can be generated. Each coded component is tested through function simulation using the design tool to ensure specifications are met.

Schematic programming is available in the current design tool, Altera Quartus II, which allows top level system construction via connection of all the necessary components. A snapshot of a part of the EDA development environment is shown in Figure 4.15, where function blocks are connected by data buses and signal paths to form a logic processing subsystem for one of the four input SG level signals.

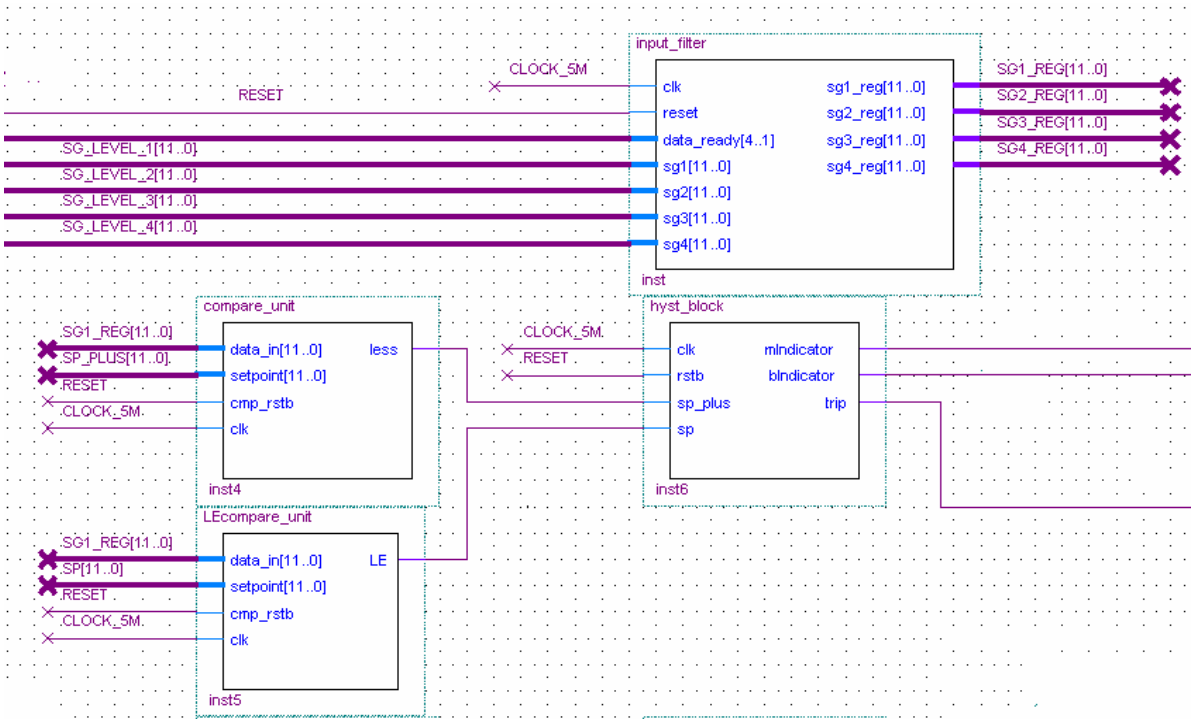

Figure 4.15 – Snapshot of the EDA development environment

Compilation is performed after the whole schematic design is verified through function simulation. The outcome of the compilation is a bitstream file that contains specific circuit description and routing instructions. Configuration of the actual FPGA platform is done by downloading this bitstream file to an Altera Stratix FPGA chip.

To establish connections between the implemented FPGA platform and the simulation environment for evaluation purposes, it is necessary to have an A/D interface. Four A/D

chips are mounted onto a printed circuit board (PCB) board to form such an interface. Incoming 4-20mA signals from the simulation environment are converted by the interface into digital signals that can be processed by the FPGA platform.

The configured FPGA platform along with the connected A/D interface is shown in Figure 4.16.

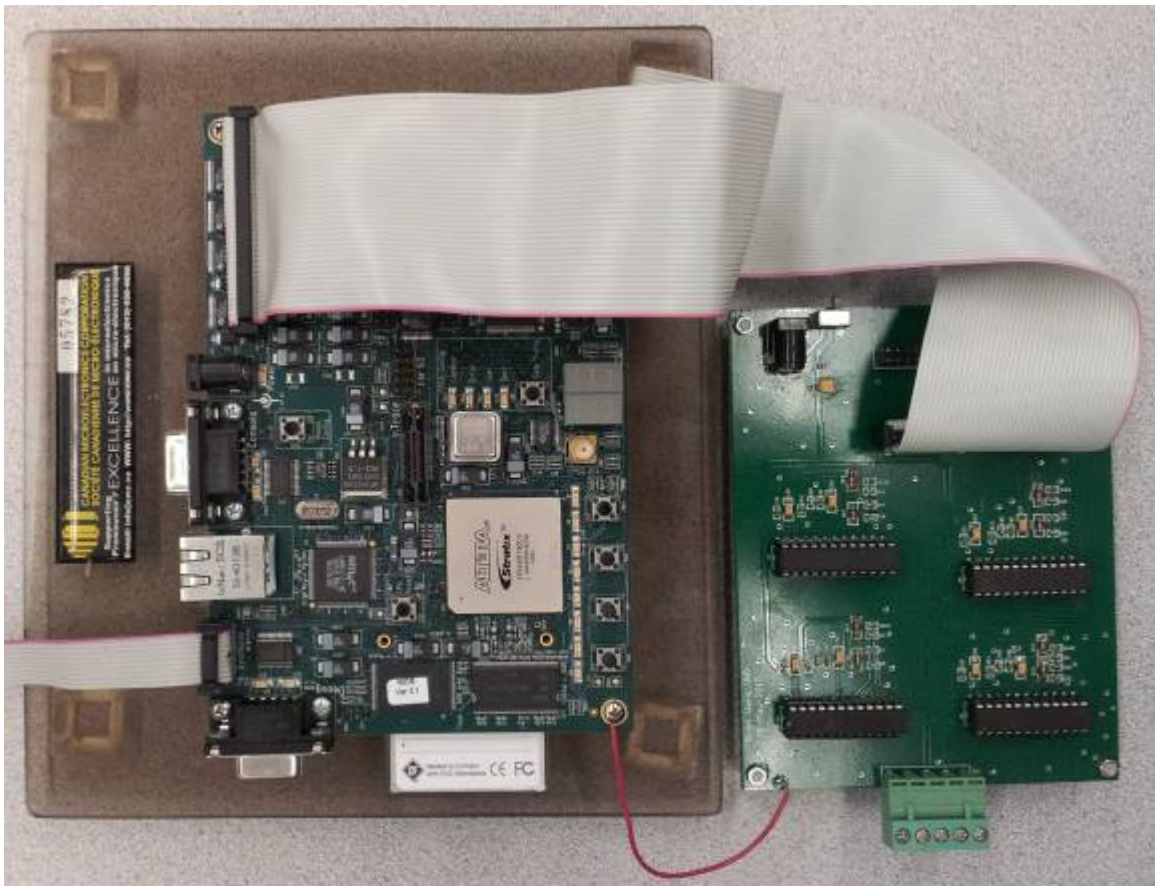

Figure 4.16 – FPGA platform and the A/D interface

4.2.8 Discussions for the implemented FPGA platform

During the design and implementation process, techniques that fully utilize the advantages of an FPGA platform are deployed whenever possible. Waiting time in a task queue, which is unavoidable in software-based processing, is reduced by using parallel

implementation, e.g. the range checking and variable sorting. Pipeline processing is applied to tasks that can be divided into *N* stages (*N*=1, 2 …) such that different stages of these *N* tasks can be processed simultaneously. The total clock cycles in such an implementation are less than 100. Furthermore, a configured FPGA chip is independent from the software-based design tool. The processing delay in such a pure hardware system is only the signal propagation latency in the circuit. Therefore, the processing speed of a certain algorithm or logic is increased significantly. As a matter of fact, in a previous work [146], it has proved that for an identical logic, the FPGA platform can have a processing speed 13 times faster than that of an industry standard PLC.

Despite the advantages in increased processing speed, bottleneck problems that limit full exploration of NPP FPGA applications do exist in the current study. Since the access to the plant data and SDS1 technical information is limited, current implementation work has to be based on some assumptions. Although the implemented platform is capable of demonstrating the processing speed advantage, it is not possible to conduct performance comparison against SDS1 in use. Meanwhile, there is yet no specific guideline for FPGA applications in CANDU NPPs, which makes it harder for current implementation to comply with specific CANDU NPP requirements. Finally, the total trip-related I/O ports in a CANDU 6 SDS1 are 133 [148]. It requires special hardware interface to implement the full system. However, this work can only use products available in our research lab, which is another reason for focusing on one of the ten trip parameters for implementation and evaluation.

Comparing to other systems that have been utilized in NPPs for safety functions, FPGAs do have some disadvantages. The most widely used FPGAs are SRAM-based ones,

which are configured through on-board SRAMs. The weakness of SRAM-based FPGAs is that they are vulnerable to radiation. The configured interconnection between CLBs can be affected by radiation such as neutron flux within the NPP containment, which may cause malfunctions of the system and is completely unacceptable. Previous research work has explored such a problem and concluded that FPGAs may have difficulties of surviving radiation environment [149]. Moreover, reliability of CMOS-based devices can be weakened by the CMOS scaling since the soft error rate increases along with the density of on-chip transistors [150]. In the foreseeable future, much higher density of transistors is expected in CMOS technology, design and implementation of a reliable device will be seriously challenged by variability and degradation [151]. Fortunately, efforts and measures have been investigated to alleviate such disadvantage of future FPGA applications [152, 153].

4.3 Summary

The "SG low level" trip logic is used as an example for FPGA implementation in this research. The trip logic is translated from a PDC logic structure into a digital hardware system design. Each function block in this digital hardware system is then coded in VHDL with parallel and pipeline schemes. Due to limited access to industry information and data, some parts of the design are simplified but desired functionalities are kept. To accommodate the simulation environment, extra logic and components are added.

All the coded components are debugged and tested with function simulations, after which the system integration (still in VHDL) and synthesis are performed. All of these steps are

executed using an EDA tools called Quartus II from Altera since an Altera Stratix FPGA is used. Synthesized FPGA design is compiled to a bitstream that can be downloaded to the FPGA chip for configuration. When the configuration is done, the FPGA implementation of the “SG low level” trip logic is considered to be finished. The next step will be performance test.

5 PERFORMANCE EVALUATION OF THE FPGA-BASED SDS1

To evaluate the performance of the implemented FPGA-based SDS1 trip channel, special test environments and cases are arranged for both the functionality verification and performance evaluation. The evaluated response time of such trip channel is then applied to the large LOCA CATHENA simulation to generate comparable results against those derived from an existing SDS1.

5.1 Methodology, experimental setup, and test cases

The purpose of evaluating the implemented FPGA-based SDS1 trip channel is: 1) to confirm that it does satisfy the function specifications of a standard SDS1; 2) to investigate whether or not it can processes the trip logic faster than an existing SDS1.

5.1.1 Methodologies for performance evaluation

For the designed FPGA-based SDS1, both functionalities and response time are examined in comparison with a software-based safety PLC. The functionality evaluations are performed by connecting this FPGA trip channel to an HIL simulation environment using an NPP simulator, while the response time is evaluated by simultaneously applying a sinusoidal input to both FPGA trip channel and the safety PLC as used in [146]. The difference in response times is captured and analyzed.

5.1.2 Experimental setups

For functionality evaluations, an HIL simulation environment has been set up. It consists of an NPP training simulator, a data acquisition system, an A/D converter interface, and

the implemented FPGA-based SDS1. A block diagram of the experimental setup is illustrated in Figure 5.1, in which the data formats in this HIL simulation are also shown.

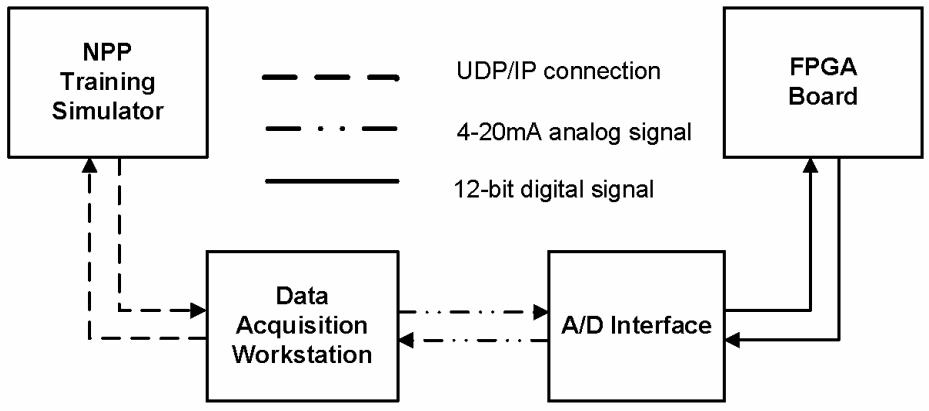

Figure 5.1 – HIL simulation environment for functionality evaluation

As shown in Figure 5.2, channel E of the SDS1 in the simulator is replaced by the FPGA trip channel. The simulation data generated by the simulator is applied to the FPGA board through data acquisition workstation and a UDP/IP Ethernet connection. The outputs from the FPGA board are sent over to the simulator in a similar manner.

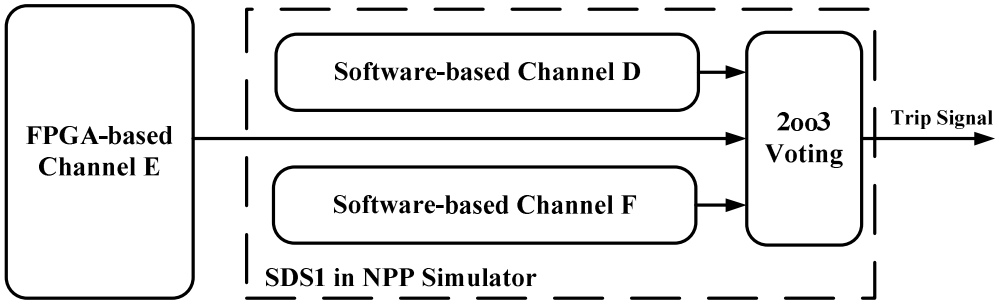

Figure 5.2 – Channels representation of the HIL simulation

The above HIL set up is not used for evaluating the response time, because the simulator is running at a 200 *ms* time step (5 *Hz*) which is much slower than the clock frequency of the FPGA board (5M *Hz*). A separated test environment is constructed as shown in

Figure 5.3. A sinusoidal signal is applied to the FPGA board, and the responses are recorded on an oscilloscope for off-line processing.

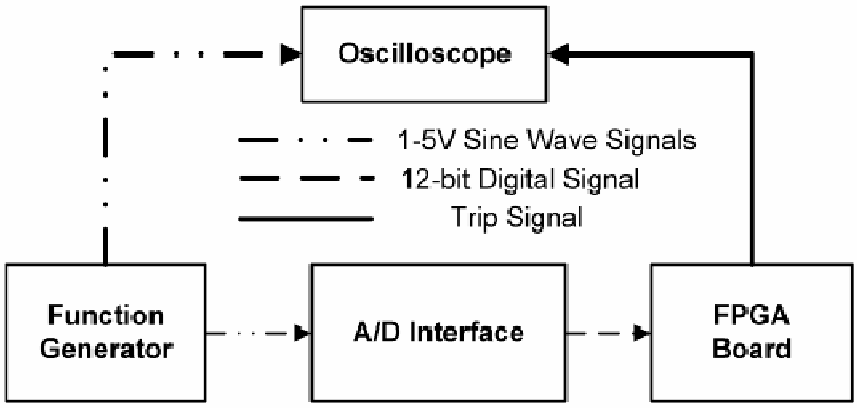

Figure 5.3 – Setup for evaluation response time of the FPGA implementation

5.1.3 Simulation approaches and test cases

The functionalities and response time are evaluated using the experimental setups. The operating frequency of the FPGA channel is set at 5M *Hz* with due consideration of background noise in the simulation environment. In the functionality evaluation, the following accident scenario is used:

A fault is introduced deliberately to close a feed water valve on one SG. As a result, the SG level begins to decrease. To evaluate the behavior of channel E only, positive biases have been added to the setpoints in channel D and channel F, so that the responses from these two channels are always after that of channel E. The manual trip on channel D is initiated at an early stage of the simulation to fulfill the 2oo3 logics when the trip signal from channel E is registered. Under this arrangement, the reactor trip event solely depends on the trip signal from the FPGA-based channel E. The evaluations have been

repeated with the manual trip signal issued at different time instance to show that the effectiveness of FPGA-based channel E is insensitive to the time of manual trips.

The response time is assessed by applying an upper shifted sinusoidal signal (1 –5*V*) to the FPGA system input. The response from the "SG low level" trip channel is captured and recorded on an oscilloscope. Because of the experimental uncertainties and measurement noise, the measured response time varies with each realization. Thus statistical analysis, based on Monte Carlo methods, has been carried out to estimate the response time of the FPGA implementation. The input frequencies are randomly selected within the range of 0.1 *Hz* to 10 *Hz* based on a uniform distribution. For each input frequency, the response time is measured. It is found that 120 samples are sufficient to produce an acceptable 1% relative error in the mean. Therefore, the Monte Carlo simulation is performed with 120 randomly selected input frequencies.

5.2 Experimental results and analysis

Experimental results are captured and analyzed. The analysis results are compared against the performance of an existing SDS1 to give verification of the system correctness and the timing performance.

5.2.1 Functionality simulation

The feed water valve is deliberately closed to initiate the accident at time 0. The channel D manual trip is also issued. As the water level decreases below the preselected setpoint for FPGA channel (channel E), the 2oo3 logic is fulfilled. Shutoff rods are inserted into

the reactor and the thermal power of the reactor reduces dramatically. For clarity, the results from one simulation run are shown in Figure 5.4.

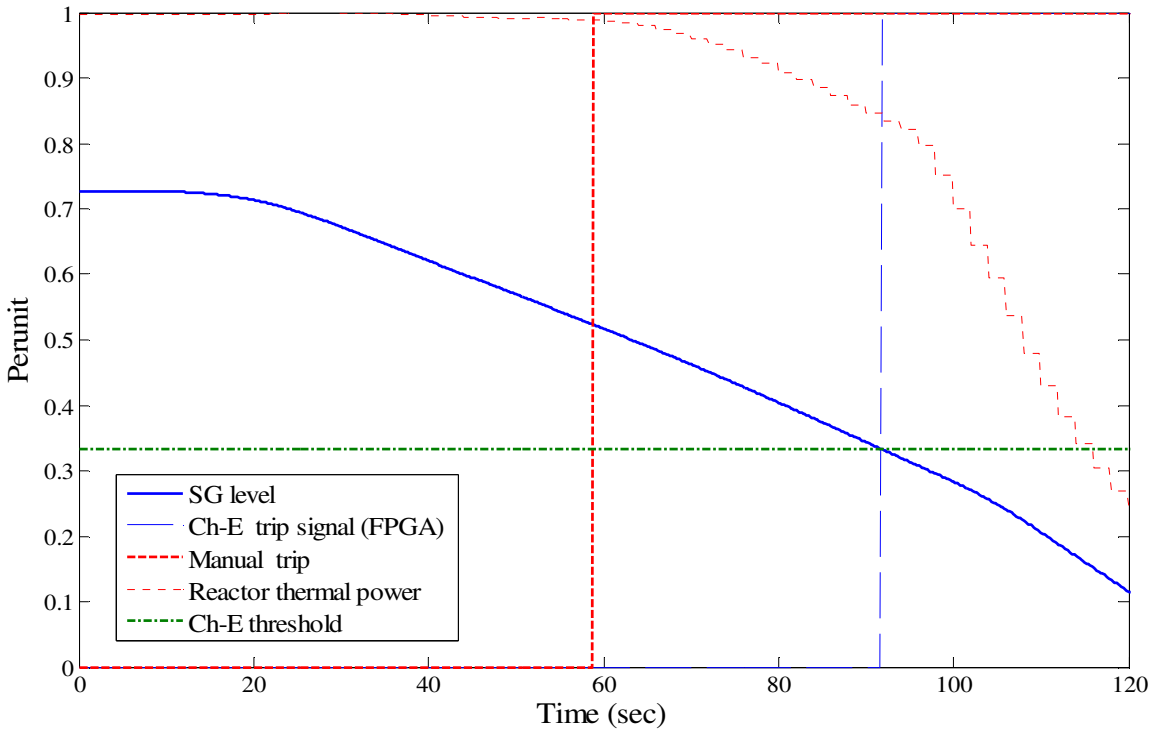

Figure 5.4 – Functionality evaluation of FPGA-based SDS1

5.2.2 Response time evaluation

A sample data captured by the oscilloscope is shown in Figure 5.5. In this particular case, it is shown that the response time of the FPGA channel is measured to be 10.12 *ms*. This is one of the 120 Monte Carlo simulation cases and only provides an intuitive view for the timing performance. The distribution of the recoded response time under 120 samples is illustrated in Figure 5.6 and the results of the statistic analysis are listed in Table 5.1.

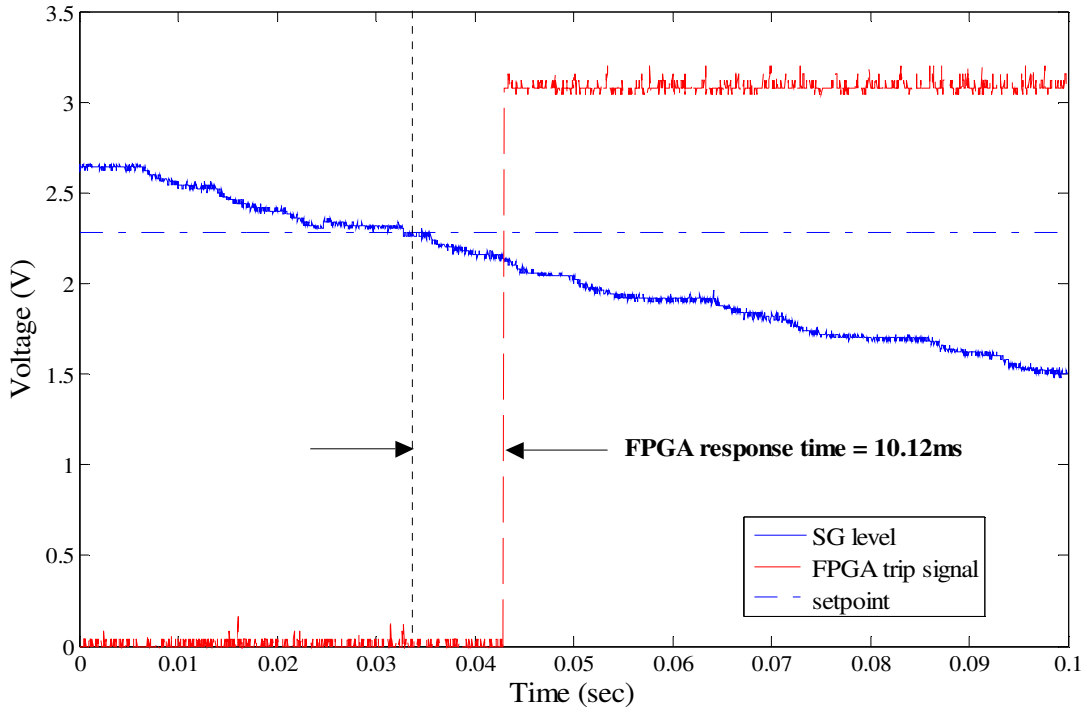

Figure 5.5 – Result of a response time test of the FPGA-based SDS1

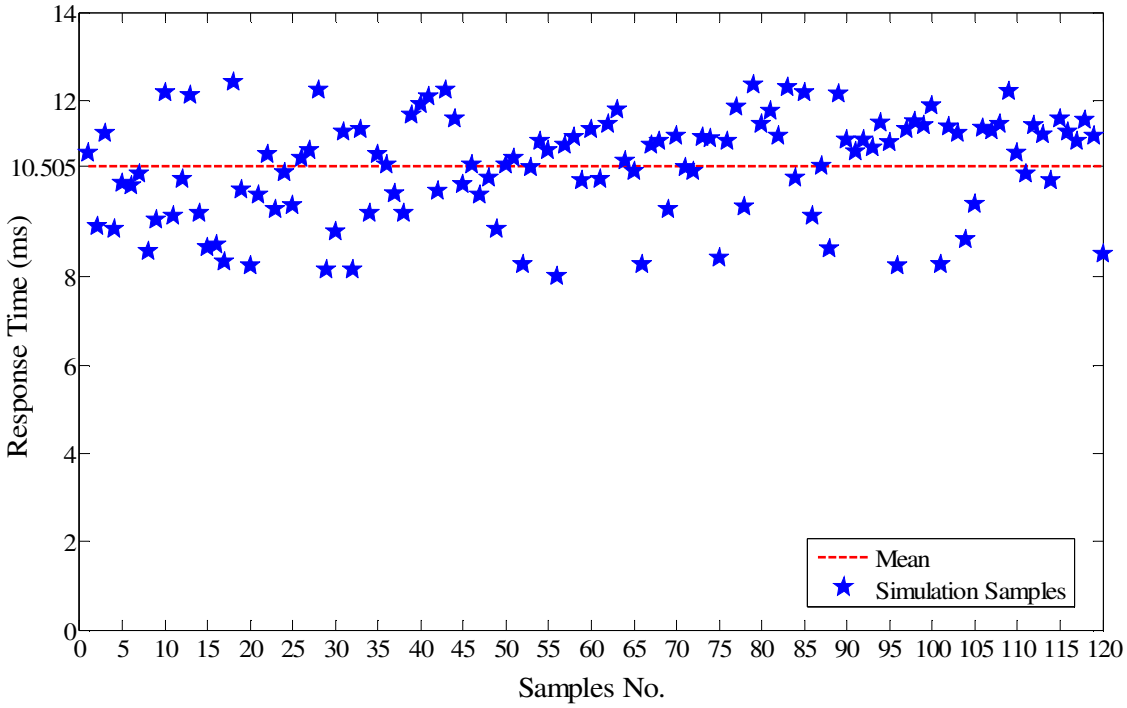

Figure 5.6 – Distribution of the timing simulation samples

Table 5.1 Statistical measures of the response time tests

Statistic measures	Results
Mean	
$E = \frac{1}{120} \cdot \sum_{i=1}^{120} x_i$	$E = 10.5\ ms$
Standard deviation of the samples	
$\sigma = \sqrt{\frac{1}{120} \sum_{i=1}^{120} (x_i - 10.5)^2}$	$\sigma = 1.160722$
Standard deviation of the mean	
$\sigma_E = \frac{\sigma}{\sqrt{120}}$	$\sigma_E = 0.105969$
Relative error of the mean	
$e_E = \frac{\sigma_E}{E} \times 100\%$	$e_E = 1.0087\%$

5.2.3 Analysis of the test results

The FPGA-based trip channel has been extensively evaluated under different trip conditions. A sample of the simulation results in Figure 5.4 has clearly shown that the FPGA-based trip channel can successfully provide correct trip signals.

The statistic analysis of the timing simulation indicates that the average response time of the FPGA trip channel is 10.50 *ms*. Although there exist several samples that have relative large variance from the mean, this 10.5 *ms* value is considered as rational result with acceptable relative error. This response time is considerably shorter than that of a software-based PLC system (78.69 *ms*) [146] under the identical HIL environment (i.e. the same SG low level scenario on the same simulator and the same data acquisition unit).

The reduced delay, 78.69 - 10.5 = 68.19 *ms*, is a significant improvement of the SDS1 decision-making time. Percentage wise, the FPGA implementation is 86.66% faster as shown in Figure 5.7.

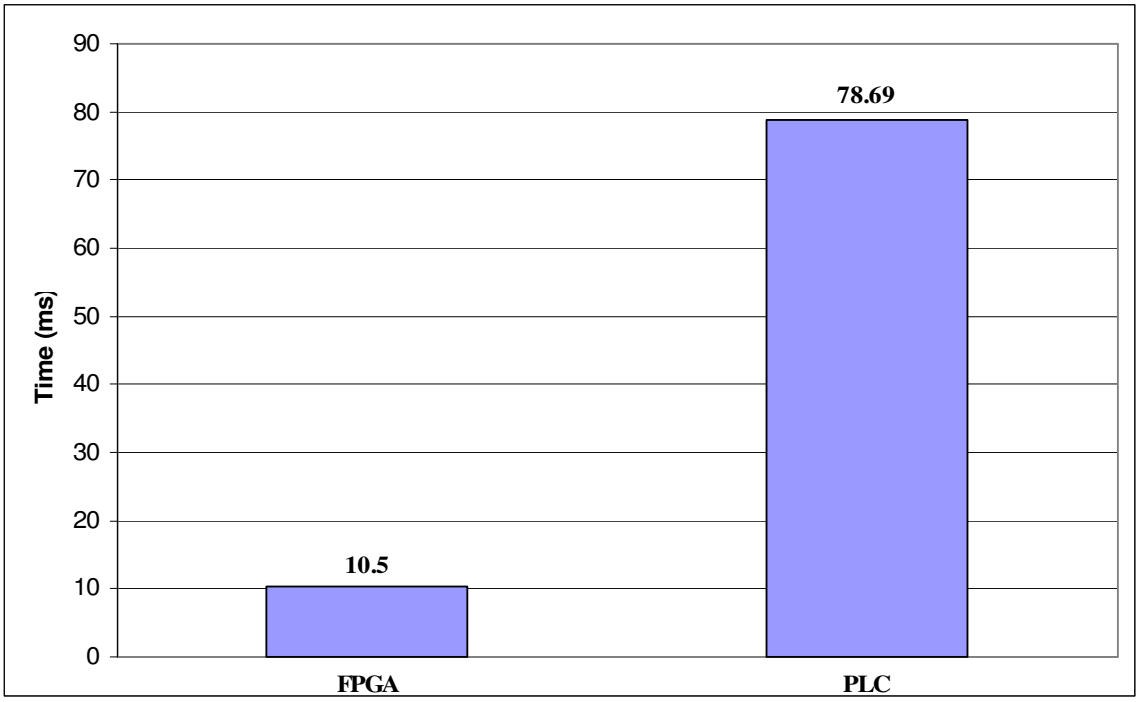

Figure 5.7 – Comparison of response time between FPGA and PLC

There are several factors that can potentially affect the response time of the FPGA trip channel. First, the algorithm complexity of the trip logic is a dominant one. For a certain trip parameter implemented with the same FPGA design technique, the simpler the trip logic is, the faster the trip decision can be made. Within the FPGA chip itself, the clock frequency also has significant influence on the response time. A faster clock can certainly produce a shorter response time. However, one should always consider the sensor dynamics and the noise effect when choosing the suitable clock frequency. Finally, the speed of data acquisition systems, in particular, A/D converter time, has to be considered.

In the current work, the A/D conversion time is $20\mu s$ according to the datasheet [154], which is negligibly small as compared to the channel response time. Thus, it has minimal effect on the response time of the FPGA and allows the measured time to represent directly the performance of the FPGA-based SDS1.

As for the comparison between FPGA and PLC implementations, it should be mentioned that the Tricon v9 PLC tested in [146] is a matured industrial product which is already utilized in CANDU NPP [56]. It also has been approved by U.S. NRC as acceptable for safety-related use in NPPs [155]. Such a Tricon v9 PLC system has many additional features that the FPGA platform does not have. For instance, the PLC itself is a triple redundant controller while the FPGA channel in this work has no redundancy. All the inputs of the Tricon v9 system are made triplicate for validation purpose before feeding to the three main processors. A voter is deployed for the results from the three main processors such that the probability of incorrect output can be reduced [155]. Such triple redundancy enhances the system reliability and qualifies its compliance to the regulation requirements. The tradeoff, however, is the extra time consumed at both the input and output ends for the inputs validation and result voting. Although the Tricon v9 PLC performs the trip logic slower than the FPGA channel, it is capable of performing many other complicated control functionalities. Furthermore, the A/D conversion time is common to all implementations whether an FPGA or a PLC is used. The sole objective to use this PLC as a benchmark example is to show that FPGA-based implementation can carry out what a traditional operating system driven software-based system can do, and can do it faster.

5.3 CATHENA simulation using evaluated response time

The large LOCA scenario in Chapter 3 is simulated again with the obtained FPGA response time. 100.0 *ms* is selected in the first simulation case, since it is considered by industry as the maximum allowed response time for CANDU SDS1[47]. According to the evaluation work reported previously, 10.5 *ms* is used as the improved response time to generate simulation results for comparison. Although the largest measured response time (12.4 *ms*) should be used for CATHENA simulation with the "worst case concern", the simulation results are identical for both 10.5 *ms* and 12.4 *ms* due to the calculation accuracy of CATHENA code. Moreover, 12.4 *ms* is not guaranteed to be the worst case with limited samples, but 10.5 *ms* is a statistically evaluated value with acceptable relative error. Therefore, 10.5 *ms* is used in this study for the result analysis work.

5.3.1 Simulation results

The simulation results are analyzed for the verification of the safety margin improvement. The relationship between the response time and transient parameters is obtained from the simulation results analysis.

Simulation results with 100.0 *ms* response time are shown in Figure 5.8 and Figure 5.9, including the region power transients (Figure 5.8) and the region temperature transients (Figure 5.9). To illustrate the importance of the shutdown process, the power transient when no shutdown action is taken is shown in Figure 5.10 along with the core power transient for 100.0 *ms* response time (peaking at 1.778).

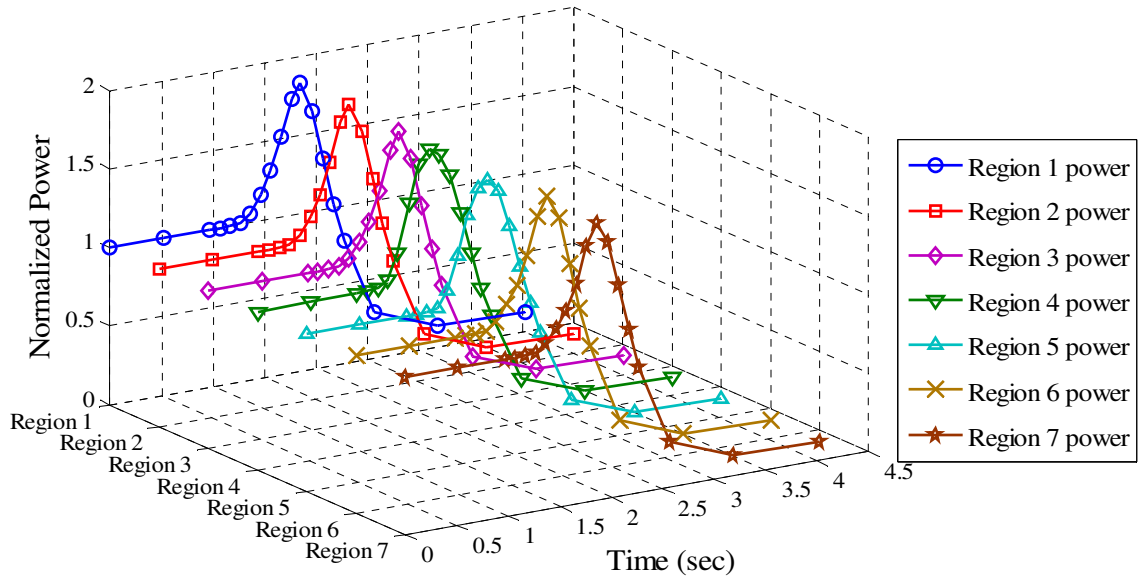

Figure 5.8 – Region power transients with 100.0 *ms* response time

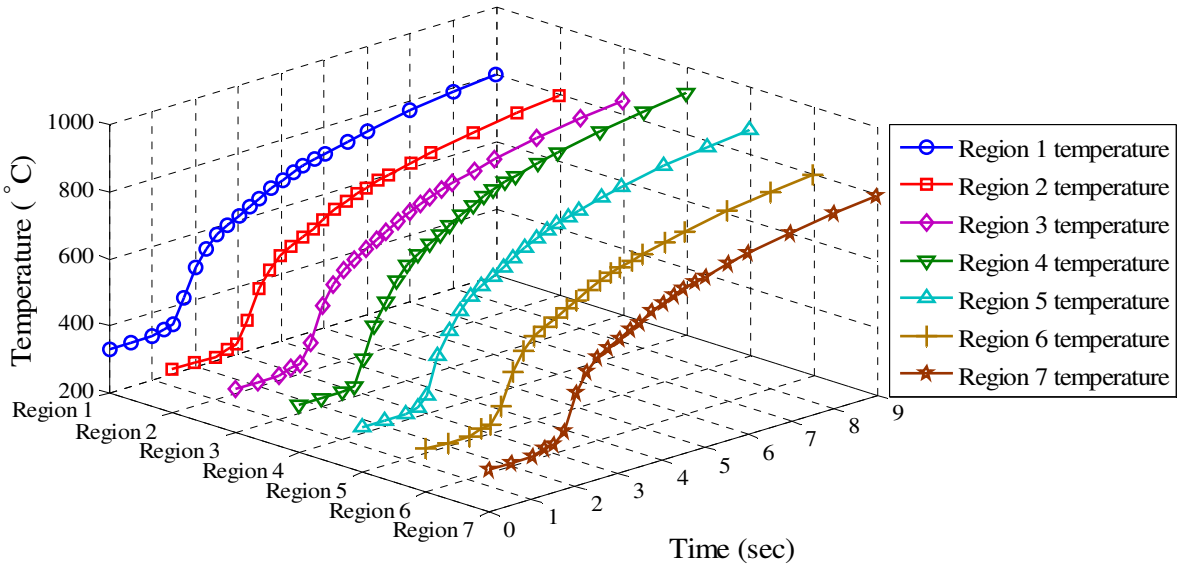

Figure 5.9 – Region temperature transients with 100.0 *ms* response time

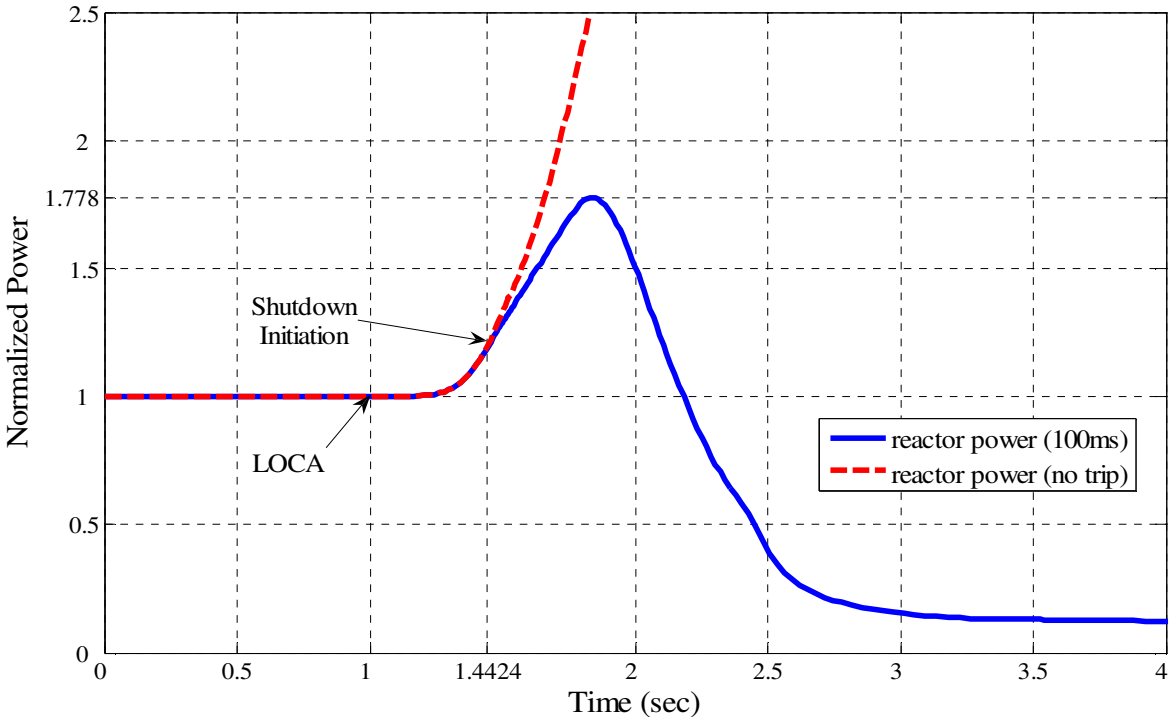

Figure 5.10 – Core power transients with and without shutdown action

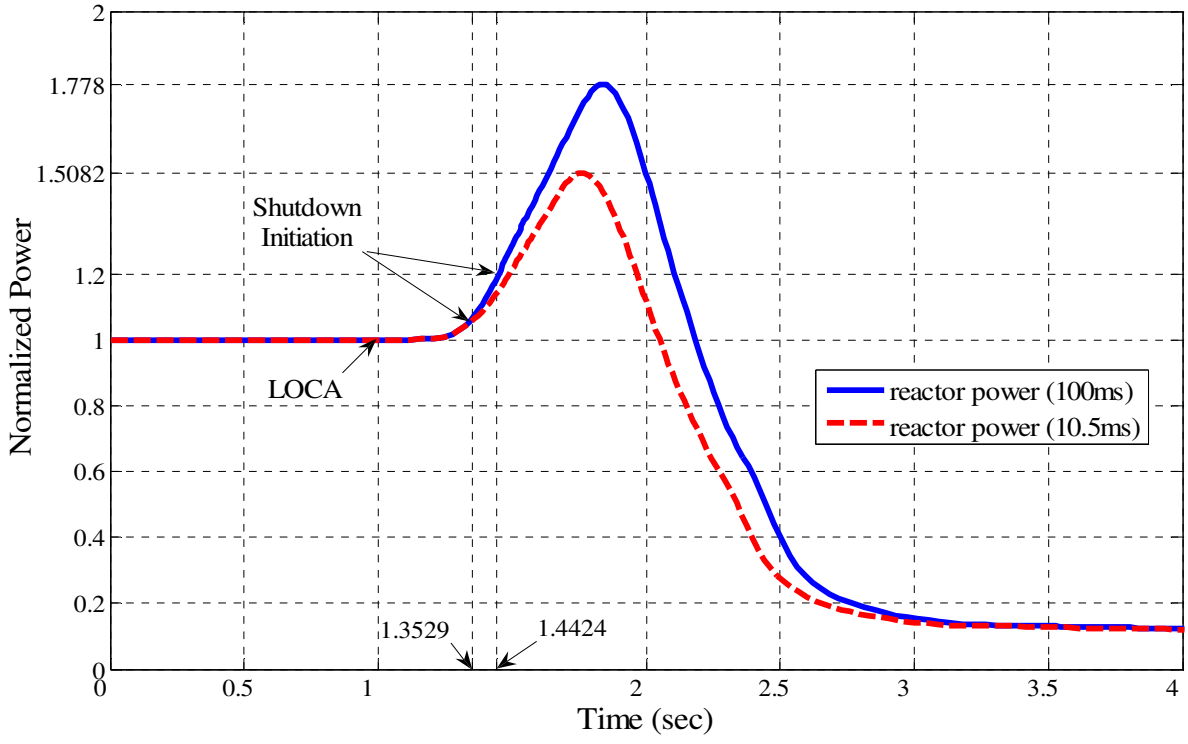

Figure 5.11 – Comparison of power transients under two different response times

The identical large LOCA scenarios have also been examined with both response times of 10.5 *ms* and 100.0 *ms*. The peak for the power surge is recorded at 1.5082 for 10.5 *ms* and 1.778 for 100.0 *ms*. The results under both response times are compared in Figure 5.11.

5.3.2 Analysis of simulation results

As the simulation results indicate, a large LOCA can cause dramatic increase in reactor power and temperature. The positive reactivity brought by rapid voiding of PHT system destroys the thermal balance within the core. The shutdown system reacts to this situation and inserts sufficient amount of negative reactivity (-80 *mk*) to stop the chain reaction. That is why the power transient starts to drop quickly soon after the shutoff rods insertion. Thus, the sooner the SDS1 is activated, the smaller the power peaks will be.

By comparing the slopes of the transient curves, one can also note that the rate at which the transient rises for 10.5 *ms* shutdown time is much smaller than that of 100.0 *ms* response time. Slower power increasing produces a lower peak in the transient. The difference between the two peaks, as described in Figure 5.11, is 1.778-1.5082 = 0.2698. In other words, it represents 27% reduction in the power surge peak, which means that 555.15 MJ less amount of heat has to be removed from the core eventually according to Table 5.2. Without getting into specifics of the safety limit in an operating reactor, it is evident that lower power peaks will be beneficial to safety margins.

Although the sheath temperature does not reach the peak value within this simulation time range, the temperature transient in 10.5 *ms* case does show improvement according to the simulation results. Moreover, within the 9-second simulation process the amount of

heat generated in 10.5 *ms* case is 6,649.04 *MJ*. It is 555.15 *MJ* less than the 7,204.19 *MJ* of 100.0 *ms* case. Comparison of these two cases is summarized in Table 5.2.

Table 5.2 Comparison of key parameters under two shutdown cases

Case	Delay Time (ms)	Power Peaks	Temp. Peaks (℃)	Heat (MJ)	Time to Peak (s)
1	100.0	1.778	931.79	7, 204.19	0.839
2	10.5	1.5082	909.05	6, 649.04	0.757
Δ	89.5	0.2698	22.74	555.15	0.082

Although it has been shown that shorter response time produces lower peaks in power surges, how the variation of the response time affects the peak of surge is yet to be investigated. Further analysis on the relationship between the decision-making response time and the peak of the power surge under a large LOCA has been carried out. Simulations under different response time varying from 10.5 *ms* to 200.0 *ms* are performed. Based on the simulation results, the relationship between the response time and the power peak can be approximated by the following linear equation (5.1):

$$P_{peak} = 0.003t_d + 1.4765 \tag{5.1}$$

where

P_{peak} is the peak value (in normalized power) of the thermal power transient as result of a LOCA; t_d is the decision-making time (in the unit of millisecond) needed by the trip channel, known as the response time.

Since the power surge peaking time is also of importance to the safety analysis, a formula to predict the surge peak time is also established based on the simulation results as follows (5.2):

$$T_{peak} = 0.0008 t_d + 0.7547 \tag{5.2}$$

where

T_{peak} is the time (in the unit of second) that the thermal power transient reaches its peak after the LOCA is initiated; t_d is the decision-making time (in the unit of millisecond) needed by the trip channel, known as the response time.

The sampled data and the curve fitting results for these two relationships are illustrated in Figure 5.12.

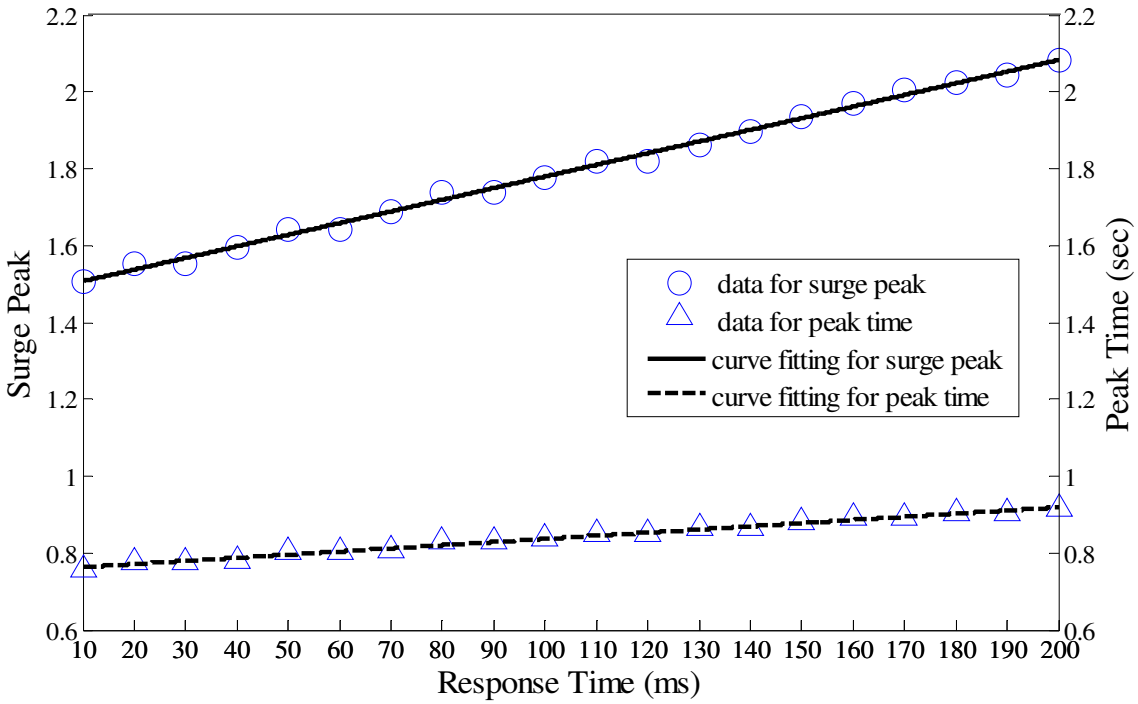

Figure 5.12 – Power surge (peak and time) vs. the response time

These two linear relationships clearly illustrate why shortening the response time of a shutdown system can be beneficial to mitigate the impact of an accident and to contribute to the NPP safety. In other words, by shutting down the chain reaction faster, less decay heat will be generated, which effectively increase the operational safety margin. Since, by definition, the safety margin of a particular system variable is defined as the difference between the operating values of this variable and its safety limit, the safety margin of reactor power is directly related to the operating power level. One can potentially increase the power level without scarifying the safety margins, i.e. maintain the same level of power surge, if the response time of the shutdown system can be shortened.

5.4 Summary

In this chapter, the test environment and test cases used in this work are described to show the evaluation methodologies.

The simulated results, for both the functionality and timing performance, are presented along with the analysis. The FPGA-based trip channel responds properly to the postulated "SG low level" scenario by issuing the expected trip signal. The reactor is then tripped at the moment when SG level goes below the predefined setpoint. The statistical analysis of the timing performance has highlighted the advantage of an FPGA-based trip channel as compared to an SDS1 controller utilized in an existing CANDU NPP.

On the basis of the timing evaluation, CATHENA simulation is carried out to quantify the safety margin improvement. Relationship between the response time and critical parameters, i.e. peak power surge, is established through data analysis.

6 VALIDATION OF FPGA-BASED SDS1 IN AN HIL SIMULATION

To demonstrate the feasibility of the proposed safety margin improvement scheme from more practical point of view, HIL simulations have been carried out in this chapter. The HIL platform, as described in [27], consists of a CANDU NPP simulator, an industry grade FPGA development system, and associated interface devices. In this study, a large LOCA similar to what has been discussed in Chapter 3 is created in the NPP simulator. One channel of the safety shutdown system of SDS1 within the simulator is replaced by a National Instruments (NI) FPGA implementation. Trip signal issued by the FPGA-based trip channel is used by the simulator to form the simulator trip signals.

6.1 Advantages of HIL simulations

The HIL simulation studies are conducted under a large LOCA scenario similar to those used in the CATHENA analysis. This experimental platform enables us not only to validate the results from CATHENA directly, but also to examine the practical aspects of a diverse FPGA implementation in real-time, such as signal interface, and the real-time response of the NPP operating parameters. More importantly, it further demonstrates the feasibility and benefits of this concept.

The in situ performance of the FPGA implementation is evaluated. Both the decision-making process of the FPGA-based SDS1 and the behavior of the simulator under large LOCA conditions can be examined in parallel. Moreover, power transients generated by

the simulator provide powerful validation of the safety margin improvement from a practical NPP environment.

6.2 HIL simulation setup

HIL simulation is selected due to explained reasons and advantages. The simulation loop is constructed similar to that of Chapter 5. However, the FPGA platform used in this chapter is an industry grade equipment from NI. The HIL simulation interface is also upgraded to provide sufficient I/O ports for the current HIL simulation.

6.2.1 HIL simulation platform

HIL simulations are utilized to further verify the effectiveness of shortening the response time on improvement of safety margin in a real-time environment and to demonstrate the technical feasibility of FPGA-based implementation. An HIL simulation platform similar to that in Chapter 5 has been built up for validation and verification of NPP safety systems in [27]. In the current study, the entire HIL simulation platform operates in real-time to respond to the LOCA instead of the "SG low level" scenario described in Chapter 4. Since industry grade NPP simulator is used in the HIL platform, the evaluation of the developed FPGA system can be carried in an integrated and more realistic environment by considering the entire plant operating environments.

The main justifications for using HIL simulations are: 1) to provide a quasi-practical environment for verification and validation of the safety shutdown systems in real-time; 2) to examine the practical signal interfaces and their effects on the FPGA-based decision-making system; 3) to allow for real-time monitoring of relevant variables in the simulated

plant coherently; and 4) to study the trip channel performance in comparison with other forms of shutdown system implementation. These features associated with an HIL platform cannot simply be done in an off-line CATHENA simulation.

The entire HIL simulation platform discussed in [27] is exploited here except that the system under test (SUT) now is an FPGA system instead of the PLC. The simulator acts as the virtual NPP where the postulated accident is simulated and the plant responses to the shutdown process are captured and displayed. A microcontroller-based interface, as shown in Figure 6.1, replaces the PC-based data acquisition workstation used in Chapter 4 to provide more efficient data transmission and processing. In addition to one UDP/IP input port, there are eight voltage I/Os, eight current I/Os, and eight digital I/Os on this interface. The programmed microcontroller transfers the UDP/IP packages into corresponding 4-20 *mA* industry grade signals that are taken as the inputs of the NI FPGA system.

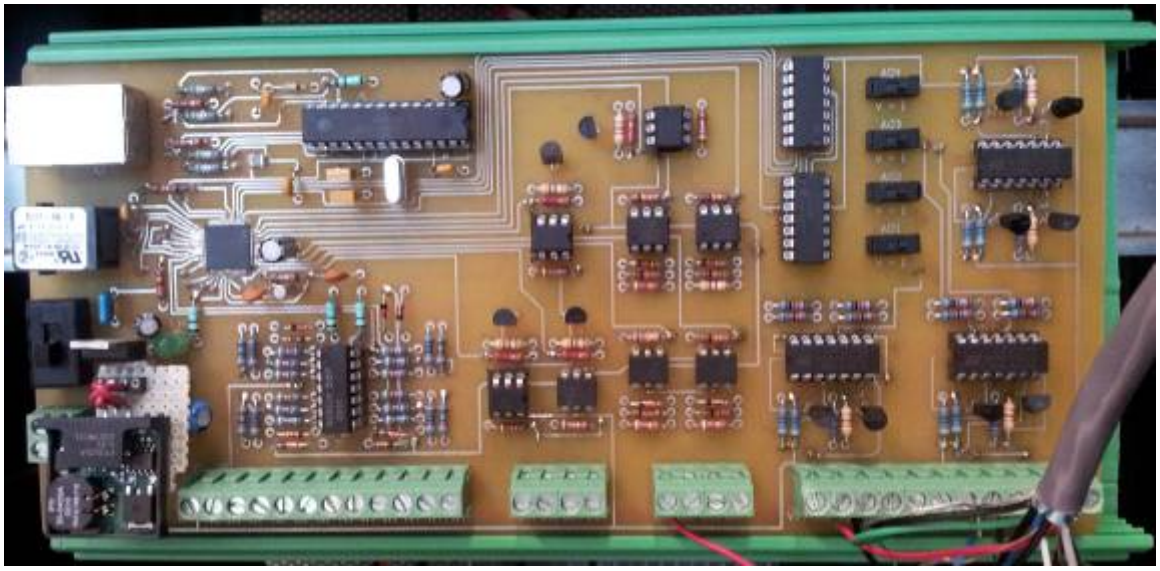

Figure 6.1 – Microprocessor-based HIL interface board

The FPGA system used here, as shown in Figure 6.2, is an NI PXI-7811R system from NI with an onboard Virtex-II 1M-gate FPGA device. It is programmed through LabVIEW FPGA module, which enables custom onboard decision-making that executes with hardware-timed speed and reliability [156]. The FPGA programming module, running in the PC-based controller board of the PXI platform, is the design tool for the FPGA device. The trip logic under a LOCA condition is decomposed into function blocks and coded via the programming module. An apparent advantage of this NI PXI FPGA system is that it has expansion chassis to house extra I/O ports if needed [157]. Two chassis are used with four I/O modules in each. One expansion chassis along with its plug-in I/O modules, which are capable of converting FPGA digital ports into multifunction ports, are shown in Figure 6.3.

Figure 6.2 – National Instruments PXI-7811R FPGA platform

Figure 6.3 – National Instruments expansion chassis and I/O modules

The assembly of the entire PXI FPGA system is illustrated by a schematic diagram in Figure 6.4.

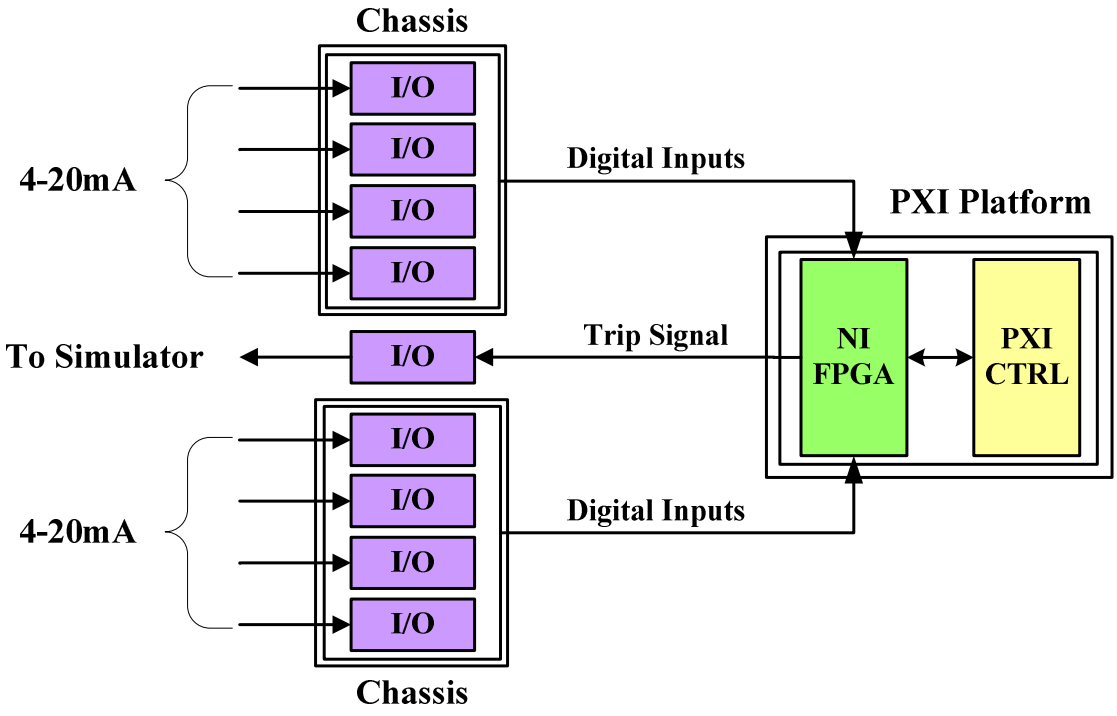

Figure 6.4 – Assembly of the PXI FPGA system

6.2.2 Implementation of the trip logic

In the implemented trip logic, the neutron overpower is used as the trip parameter since it is a key parameter associated with the LOCA conditions. The process variables being monitored are obtained from the neutron detectors. The simulated LOCA causes transients in the neutron flux.

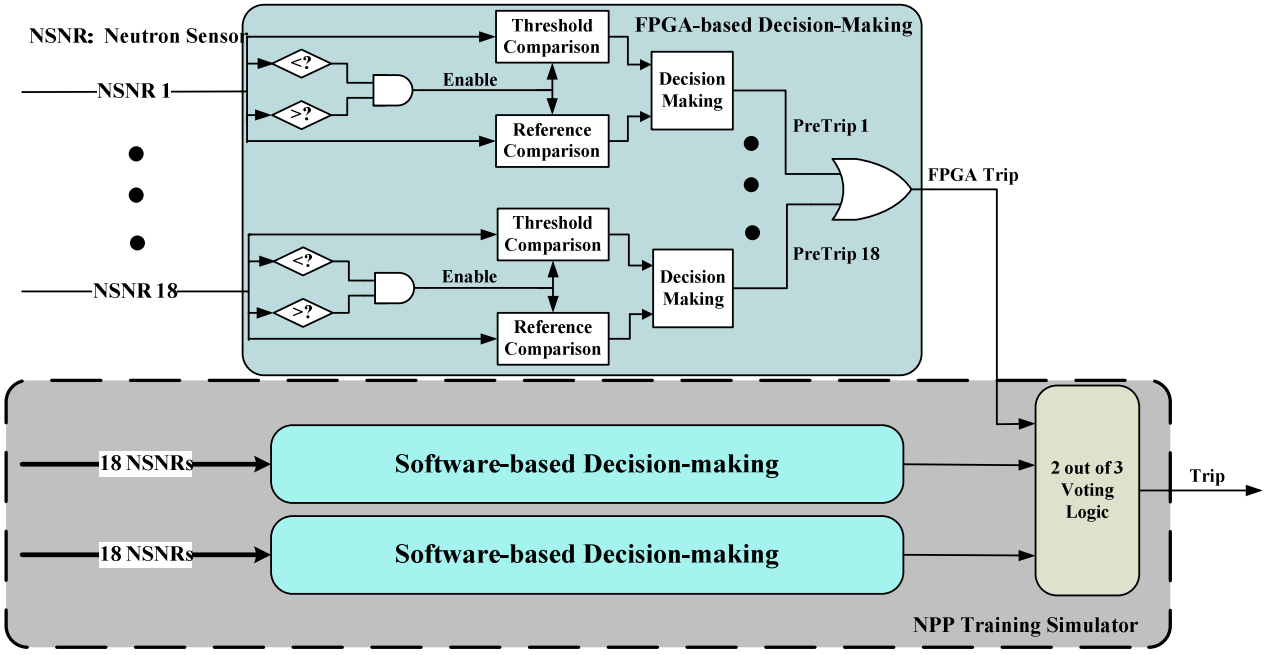

Figure 6.5 – Logic process of neutron overpower trip process

The logic for neutron overpower trip consists of a comparison between the measured neutron flux and the predefined trip thresholds. The measured values from the sensors are validated by range checking circuit. To prevent spurious trips, an additional comparison channel is used to provide decision reference for the trip logic in this work. This is identical to the technique used in Chapter 4 to prevent spurious trip signals and jitters. There are totally 18 neutron detectors in SDS1 of a CANDU NPP. The trip decision is issued if any of these 18 values exceeds the trip threshold. Both the FPGA-based trip

channel and the software-based ones in the simulator are shown in an illustrative diagram, Figure 6.5, to describe the logic process of the HIL simulation.

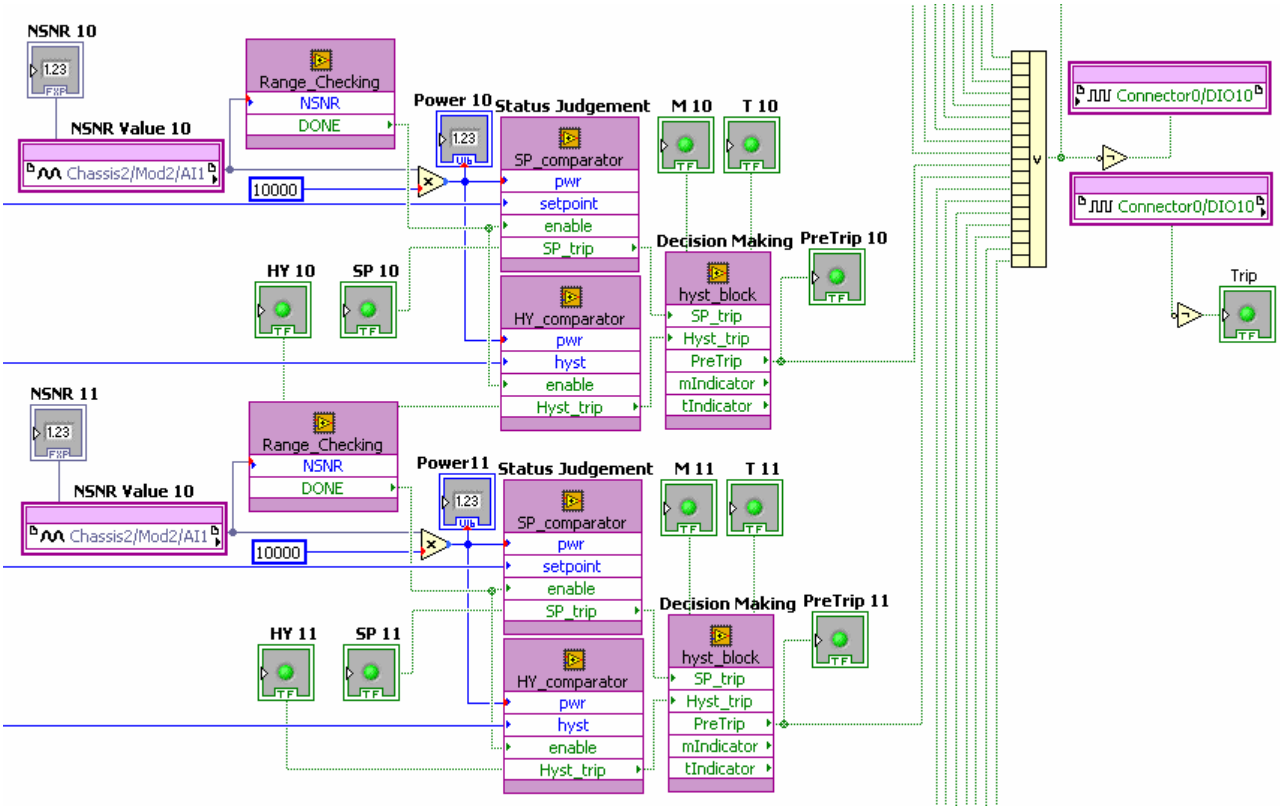

Figure 6.6 – Programmed neutron overpower trip logic

A portion of the actual programmed block diagram within the design environment is shown in Figure 6.6. The signal sources in Figure 6.6 are the I/O ports from the chassis-hold modules. The 4-20 *mA* industry grade signals are converted by these modules into digital signals for FPGA processing. Input signals to the FPGA are fed to the decision-making unit after passing the range checking. Trip decisions of all the 18 paths are pre-trip signals, which are merged into an OR gate to generate the final channel trip signal. Indicators are distributed into different intermediate signal paths for on-line monitoring

purpose. As an outcome of the FPGA-based trip logic, the channel trip signal is wired to a different I/O module such that the HIL interface can fetch it once it is available and pass it to the simulator as an indication of the simulated accident.

The real-time monitoring feature is easily realized in the LabVIEW programming environment. Indicators connected to the signal paths are assembled to generate a graphic interface that displays the ongoing transients on monitored parameters. A screenshot of such an interface is presented in Figure 6.7.

Figure 6.7 – Real-time monitoring interface

The FPGA implementation process of the above trip logic comprises of several steps, which is similar to what have been done in Chapter 4: 1) systematic design, 2) coding the logic in VHDL, 3) synthesis and function simulation, and 4) configuration of the FPGA device. The systematic design specifies a map of function blocks for the shutdown logic. HDL coding provides logic illustration for each function block. The digital circuit specification is translated from all the algorithmic operations by a synthesis process. After successfully passing the verification process using function simulations, the design can then be compiled into a bitstream file and downloaded to the FPGA hardware system for execution.

6.2.3 Setup of experiments

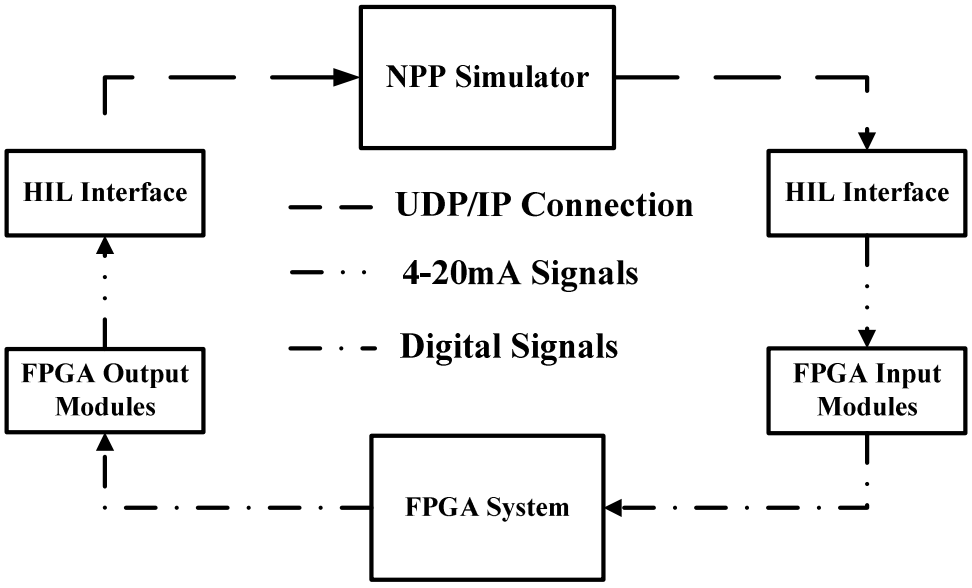

Figure 6.8 – HIL simulation setup with FPGA-based shutdown channel

Once the design and implementation of the FPGA-based CANDU trip channel are completed, the system is connected to the NPP simulator through proper interface to form the HIL simulation environment. Process variables of the simulated scenario are fetched

from the simulator and available to outside access through UDP/IP connections. The interface board translates these UDP/IP signals from the simulator into 4-20 *mA* industry standard analog signals that are connected to the FPGA system. Trip signal generated by FPGA system is then sent to the simulator to perform shutdown actions. An illustrative diagram of the experimental setup can be described in Figure 6.8.

The actual experimental setup is shown in Figure 6.9.

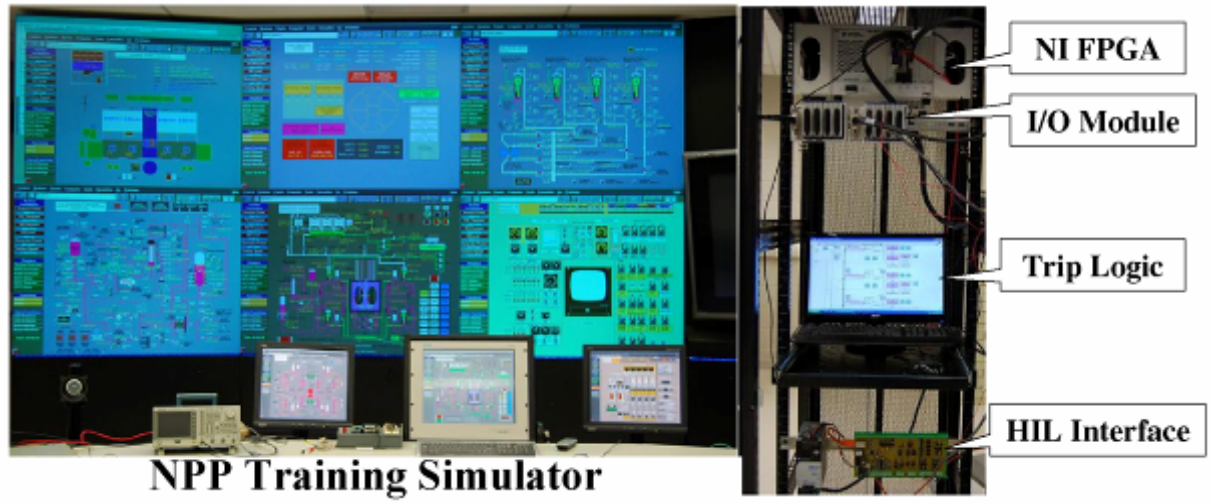

Figure 6.9 – Experimental setup with FPGA-based shutdown channel

It is important to point out that the HIL simulation is different from off-line simulation such as CATHENA. In off-line simulations, the accident scenarios are examined by solving thermalhydraulic equations. The simulation is entirely performed in terms of mathematical formulations. The trip process is based on a predefined function. Hence, neither on-line monitoring nor trip performance evaluation can be easily carried out.

In an HIL simulation, the FPGA system acts as one of the trip channels to interact with the rest of simulator dynamics on-line in real-time. Its performance can be conveniently

compared against other two trip channels within the NPP simulator to demonstrate their effects on system safety margins. HIL simulations allow on-line monitoring of changes in the plant parameters/signals in real-time. Without doubt, an HIL simulation provides a more realistic view of the safety control systems in an NPP. It is a useful platform to evaluate safety control system hardware and software. It plays an excellent complementary role to the thermalhydraulic-based safety analysis tools, such as CATHENA.

6.2.4 Selection of simulation case

Through HIL simulation, a large LOCA accident in the form of 20% break at two RIHs is configured to take place in the simulator at time $t = 0\ s$. The FPGA-based trip channel monitors the variation of all the neutron detectors and makes the trip decision once the preset conditions are met. It should be mentioned that the scenarios used in the HIL simulation is slightly different from what was done in the CATHENA simulations. The main reasons for the discrepancy are as follows:

(1) Since 10.5 *ms* used by CATHENA simulation is based on a statistical analysis performed in Chapter 5, it would be difficult to reproduce exact response time in the HIL simulation for the conditions of the postulated accident;

(2) The power output of the NPP simulator used in the HIL simulation is higher than that of a CANDU 6. Its full electric power level is at 900 *MW* with an LHGR of 0.9941, while CANDU 6 has an electric power output of 600 *MW* with an LHGR of 0.9126;

(3) Due to the discrepancies in power levels, the trip set-point of the NPP simulator is also slightly different from that used in CATHENA simulation for CANDU 6;

(4) The trip logic channels in the simulator are software-based trip logic; and

(5) The trip logic implemented in CATHENA is limited due to insufficient technical information while the NPP simulator is designed to produce complete plant responses.

6.3 HIL simulation results

Even though it is unfortunate that one cannot provide a direct comparison between the results of the HIL simulation and the CATHENA simulation, one can still draw many qualitative conclusions. With full understanding of the limitations of the HIL simulation platform and the power level difference between CANDU 6 and the simulator, adjustments have been made accordingly to accommodate the above discrepancies to ensure the validity of the simulation results.

Since there are three independent trip channels in the SDS1, one of the channels in the simulator is replaced by the implemented FPGA-based shutdown system. Subsequently, the speed of trip logic response of the FPGA-based system can be compared against that of the standard software-based trip logic within the simulator. The simulations have been carried out and the results are shown in Figure 6.10.

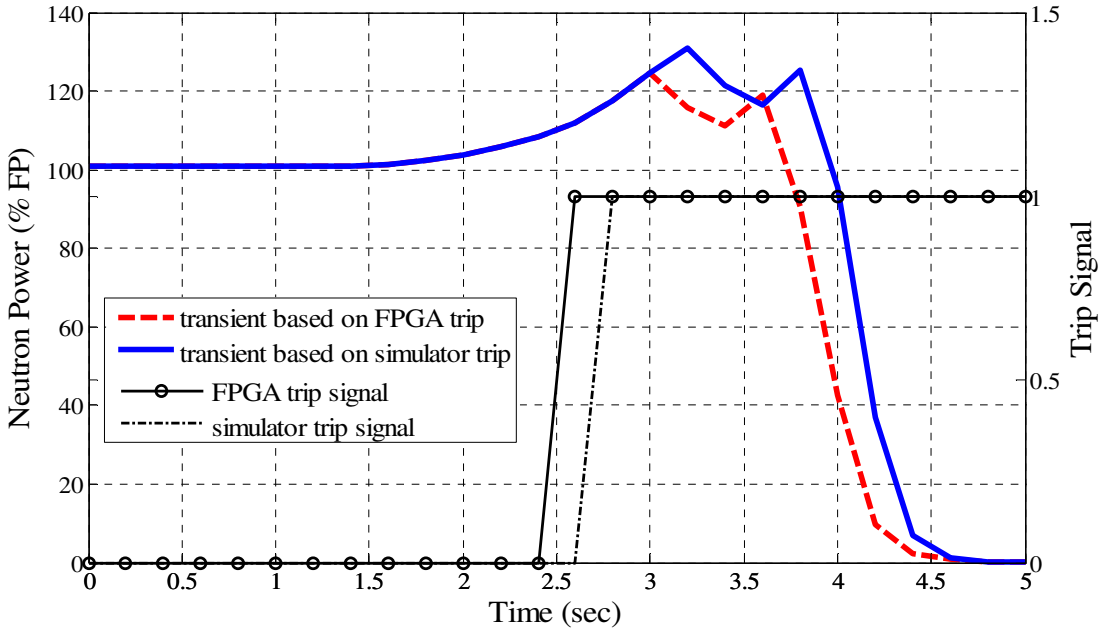

Figure 6.10 – Power comparison between FPGA trip and simulator trip channels

As can be seen, the neutron power starts rising at exponential rate after the initiation of the large LOCA. Because the FPGA-based trip channel responds to the accident scenario more quickly than the software-based simulator trip channel does, trip signal from the FPGA-based trip channel is issued earlier. As a consequence, the reactor is shut down earlier with the FPGA-based trip channel and the neutron power transient is forced to a 6.26% lower peak than that of the simulator-based shutdown transient.

6.4 Discussions

By observing the response times of the shutdown system channels, clearly, the FPGA-based channel provides significant improvement in the speed of response as compared to the software-based trip channel. As a result, the peak value of the power excursion is lower if the trip is initiated by the FPGA-based system.

Although the shape of the power transients are different from what has been obtained in CATHENA simulations due to reasons as explained earlier, the corresponding curves do demonstrate the concept of improving safety margin with a faster shutdown system response time. This HIL simulation results further validate the concept of safety margin improvement when a faster shutdown system is used.

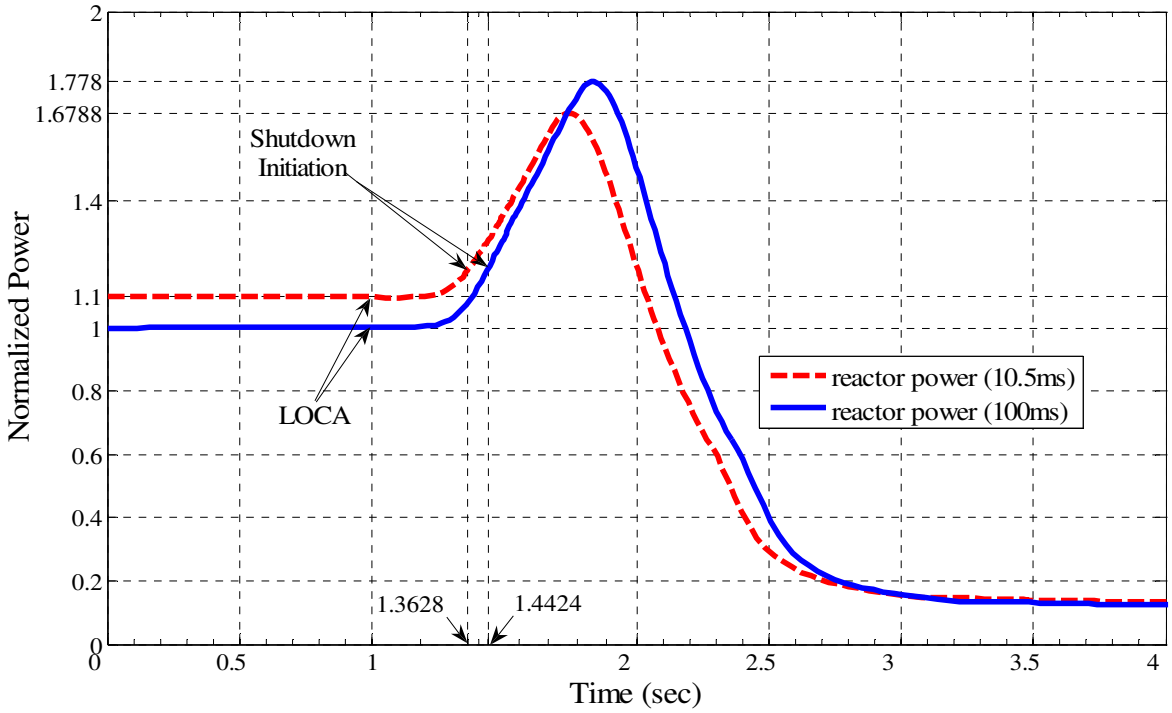

Figure 6.11 – Potential power upgrade with a faster SDS1

It is interesting to point out that with a faster shutdown system, one can effectively upgrade the steady-state operating power of the reactor without jeopardizing the safety margins. To further demonstrate this concept, a series experiments have been conducted by varying the speed of shutdown systems in CATHENA. These simulations use the same model and LOCA case as in Chapter 3. The results for two shutdown system response times (10.5 *ms* and 100.0 *ms*) are shown in Figure 6.11, where the transient of the 10.5 *ms* case is based on 10% enhanced operating power. As shown, the safety

margin improvement can be maintained as 1.778-1.6788 = 9.92%, with even lower power surge in this case, when a 10% operating power upgrade is to be implemented.

It is important to point out that power upgrade in practice involves much more than simply increasing the speed of shutdown systems. Speed of response of shutdown systems will ensure that there is no further increase in power peak surges in the event of an accident. However, if operating at a higher power output under the normal operating conditions, many plant systems have to be subjected to higher temperature and pressure, impacts of a power upgrade on other system components have to be fully investigated and approved by regulatory bodies. This will be beyond the scope of the investigations in the current thesis.

6.5 Summary

This chapter mainly focuses on validation of the designed FPGA-based SDS1 via HIL simulation. The accident scenario is similar as what has been considered in CATHENA simulations except that a more realistic simulation environment is involved. Moreover, an industry grade FPGA platform, with more I/Os than the prototype in Chapter 4, is used. The logic implementation is more concrete with actual input signals rather than restoring values within the registers.

To further verify the improvement shown in CATHENA off-line simulation, the real-time HIL simulation is utilized by realizing the similar LOCA scenario in an FPGA-based trip channel. The industry grade NPP simulator is connected to provide on-line monitoring

and trip action. Trip logic for the LOCA is implemented and the experimental environment for data monitoring and analysis are developed.

Results from the HIL simulations have been presented and analyzed. It has been demonstrated that FPGA-based trip logic can provide faster shutdown reaction to accident scenario, providing a 6.26% lower power surge than that of the simulator-based transient.

Based on the proven improvement, potential power upgrade is discussed and illustrated. It has been shown that the safety margin improvement can still be reserved as 9.92% after a 10% upgrade in the operating power has been realized.

7 CONCLUSIONS AND FUTURE WORK

Conclusions as well as suggestions for future work are presented in this chapter. The conclusions are drawn with reference to the research objectives and the obtained research results. However, limitations do exist in the current work, which leave margins for future investigation, based on which the future directions for this line of research are also discussed.

7.1 Conclusions of this research

This thesis started with a purpose of investigating possible improvement of CANDU NPP safety features by use of FPGA technology. As stated by the objectives of this work, the concept of safety margin improvement via faster shutdown process has to be validated and both the implementation and evaluation of an FPGA-based SDS1 have to be accomplished and followed by verifications of achievable benefits.

During the verification process, theoretical investigation is carried out first to obtain analytical approval of the concept. Furthermore, thermalhydraulic models to describe a LOFA and a large LOCA have been established for a CANDU reactor. Using an industrial grade simulation program, CATHENA, the accident transients are simulated based on different response times of SDS1. Conclusions of the investigation are summarized as follows:

(1) The peak values of the transient responses of the critical reactor variables are a function of the response time of the shutdown systems. The sooner the

shutdown action takes place, the smaller these peak values will be, which corresponds to a bigger safety margin; and

(2) The safety margin improvement for accidents with slow reactivity introduction, such as a LOFA, is not significant due to gradually power increase.

To validate this concept, an FPGA-based SDS1 has been implemented based on the existing SDS1 trip logic. The overall system design matches the PDC logic structure such that the implemented system satisfies the function specifications of SDS1. The design flows from the top level system down to the details of function blocks. Special techniques such as parallel and pipeline structures have been adopted wherever possible to improve the system performance. The entire design process is performed under the VHDL coding, which is absolutely circuit independent. The implemented system has been evaluated with appropriate experimental setup. Following the response time evaluation, the CATHENA simulation for a large LOCA is carried out again to confirm the safety margin improvement offered by such an FPGA-based SDS. Quantitative description of the safety margin improvement has been obtained by analytical estimation of the relationship between the critical transient parameters and the response time.

Conclusions for the implementation work can be drawn as following:

(1) According to the FPGA implementation process, it has been concluded that FPGA application for the SDS1 trip logic is feasible and circuit independent;

(2) The functionality tests have concluded that the implemented SDS1 trip channel can perform successfully under the "SG low level" condition.

(3) It has been concluded in the current work that one of the main advantages of using FPGA-based SDS1 is the fast shutdown speed. The evaluated 10.5 *ms* response time has conduced that the FPGA implementation can shorten the response time of software-based SDS implementation by as much as 86.66%;

(4) According to the CATHENA simulation based on the evaluated response time, 26.98% improvement of the safety margin has been obtained via the FPGA-based SDS1 under a large LOCA condition; and

(5) The analytical relationship between the response time of SDS1 and critical transient variables, which turns out to be linear for both cases, has been derived and illustrated in Equation (5.1) and Equation (5.2).

To further validate the benefit obtained from the off-line CATHENA simulation, an on-line HIL simulation has been performed with an industry grade FPGA system and improved simulation interface. The simulated accident is also a large LOCA except the circumstances are different to CATHENA simulations due to different reactor types. Possibility of power upgrade under faster shutdown process is also explored and discussed. The accomplished work can be concluded as follows:

(1) The safety margin improvement, which is 6.26% in normalized power, and the faster shutdown process of FPGA trip channel have been validated again in a more realistic on-line HIL simulation involving an NPP simulator, and

(2) Based on the result of the analysis work, one can potentially increase 10% of the nominal operating power of the reactor, while retaining a 9.92% safety margin improvement simply by using a faster shutdown system.

7.2 Limitations and suggestions for future work

In a thesis work, limitations do exist for the research scope. The limitations in current work are discussed below while suggestions for the future work are given as potential research directions.

7.2.1 Limitations of the current work

The scope of this thesis has been set as investigation of CANDU NPP safety margin improvement with an FPGA-based SDS1. The research relied on the fast processing speed of the FPGA platform and related benefit analysis. Within this scope, the FPGA-based SDS1 trip channel is implemented for processing speed evaluation. The evaluated timing performance is then utilized in a thermalhydraulic simulation to verify the safety margin improvement and potential power upgrade. All the objectives defined within the research scope have been achieved. However, FPGAs are powerful digital systems that can be applied to many other control applications in NPPs. Since distinctive requirements and specifications exist in each application, unique methodology is often needed during the investigations.

Although a particular FPGA-based SDS1 trip channel has been implemented, challenges and difficulties do appear during the research process. One of them is the limited access to some necessary information such as the full SDS1 trip logic. The implemented digital

system has to be simplified to make it functional. Thus, attempts of highlighting the fast processing speed can only succeed by comparing the performance of the simplified logic implemented in an FPGA and a PLC. Without implementing the full shutdown logic, this work is unable to compare the in situ performance of an FPGA-based system and the onsite SDS1 in existing NPPs.

It is eventually a prototype research work, where the available resource is not as complete as an industry project. The two FPGA platforms, the Altera Stratix FPGA development kit and the National Instruments PXI FPGA system, are of limited capability. Either the lack of enough I/O pins or the communication deficiency of the HIL interface constrains the investigation.

As for the use of CATHENA, only two postulated accident scenarios are simulated to verify the transient differences between two shutdown processes. Practically, CATHENA is capable of doing more than this. Besides simulating an accidental scenario, CATHENA also provides capability to integrate with other programs to realize more complicated functionality. Its remote access control model enables communication between CATHENA and other area-specific codes. The accessible variables in CATHENA can be fetched as inputs for calculations being performed in another program. This actually extends the functionality of CATHENA as a sole thermalhydraulic code. For example, the reactor models developed in [128] and [130] have the potential to be appropriately connected to CATHENA for on-line simulation studies.

It should be noticed that only response time has been considered in this work as a factor of the accidental transient. Without doubt, a detailed exploration for effects of other parameters will make the current work more comprehensive.

7.2.2 Suggestions for future work

Suggestions for future work are given by referring to identified limitations. Only potential research topics or approaches are discussed with respect to the CANDU safety issues.

The suggestions are listed as following:

(1) Investigation of FPGA applications for other I&C systems in CANDU NPP is needed since FPGAs offer obvious advantages over software-based solutions;

(2) It is worth implementing a full SDS1 (or even SDS2) trip logic in an FPGA system such that the in-situ performance of FPGA-based SDS1 can be thoroughly examined;

(3) If possible, it is of extreme importance to implement and evaluate an FPGA-based system that is fully capable of realizing all the I/O functions in SDS1;

(4) Achieving an on-line simulation through cooperation between CATHENA and another program allows exhaustive investigation on both thermalhydraulics and reactor physics;

(5) It would be interesting to consider other trip parameters in the accident transients with FPGA-based SDS implementation.

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APPENDIX A

CATHENA Simulation Input File

The following input file is for the CATHENA simulation of 35% RIH break case with 100 *ms* SDS1 decision-making time.

```
' CANDU 6 RIH 35% LOCA',
'UWO-CIES JINGKE SHE'/
'CONTROL PARAMETERS'/
'SOLUTION CONTROL'/
0.0, 10.0, , 0.0001, 0.0001, 0.01/
'* START TIME IS 0.0'/
'* END TIME IS 10'/
'* INNITIAL TIME STEP IS 0.0001'/
'* MINIMUM TIME STEP IS 0.0001'/
'* MAXIMUM TIME STEP IS 0.01'/
'PRINT CONTROL'/
0.01, 0.01, 0.01, , , ,.TRUE.,'A'/
'RESTART CONTROL'/
,'CORERIH35.rst', 0.01, ,.FALSE.,'C','C',/
'END'/ OF CONTROL PARAMETERS GROUP
'COMPONENTS'/
'INBC',,,,,,,,,'D2O'/
'P0',    0.1000, 0.000, 1.2946372,     1.28389,     , , 'CIRC',    1, 'D2O'/
'P1',    0.1000, 0.000, 5.6555204E-1,  8.485772E-1, , , 'CIRC',    1, 'D2O'/
'P2',    0.1000, 0.000, 7.2908516E-1,  9.634833E-1, , , 'CIRC',    1, 'D2O'/
'P3',    0.1000, 0.000, 3.5432176E-1,  6.716670E-1, , , 'CIRC',    1, 'D2O'/
'P4',    0.1000, 0.000, 3.7476340E-1,  6.907703E-1, , , 'CIRC',    1, 'D2O'/
'P5',    0.1000, 0.000, 3.5432176E-1,  6.716670E-1, , , 'CIRC',    1, 'D2O'/
'V1', , , , , , ,'VOLMC', ,D2O, , 0.0001/
'V2', , , , , , ,'VOLMC', ,D2O, , 0.0001/
'V3', , , , , , ,'VOLMC', ,D2O, , 0.0001/
'V4', , , , , , ,'VOLMC', ,D2O, , 0.0001/
'V5', , , , , , ,'VOLMC', ,D2O, , 0.0001/
'V6', , , , , , ,'VOLMC', ,D2O, , 0.0001/
'Z1', 0.1000, 0.000, 1.7716088E-1, 4.7494E-1, , , 'CIRC',1,'D2O'/
```

'Z2', 0.1000, 0.000, 1.7716088E-1, 4.7494E-1, , , 'CIRC',1,'D2O'/
'Z3', 0.1000, 0.000, 2.1123028E-1, 5.1860E-1, , , 'CIRC',1,'D2O'/
'Z4', 0.1000, 0.000, 1.6353312E-1, 4.5631E-1, , , 'CIRC',1,'D2O'/
'Z5', 0.1000, 0.000, 2.1123028E-1, 5.1860E-1, , , 'CIRC',1,'D2O'/
'Z6', 0.1000, 0.000, 1.7716088E-1, 4.7494E-1, , , 'CIRC',1,'D2O'/
'Z7', 0.1000, 0.000, 1.7716088E-1, 4.7494E-1, , , 'CIRC',1,'D2O'/
'ZONE1', 5.9436, 0.000, 3.40694E-3, 7.37629E-3, , , '37ELMT', 21,'D2O',52/
'ZONE2', 5.9436, 0.000, 3.40694E-3, 7.37629E-3, , , '37ELMT', 21,'D2O',52/
'ZONE3', 5.9436, 0.000, 3.40694E-3, 7.37629E-3, , , '37ELMT', 21,'D2O',62/
'ZONE4', 5.9436, 0.000, 3.40694E-3, 7.37629E-3, , , '37ELMT', 21,'D2O',48/
'ZONE5', 5.9436, 0.000, 3.40694E-3, 7.37629E-3, , , '37ELMT', 21,'D2O',62/
'ZONE6', 5.9436, 0.000, 3.40694E-3, 7.37629E-3, , , '37ELMT', 21,'D2O',52/
'ZONE7', 5.9436, 0.000, 3.40694E-3, 7.37629E-3, , , '37ELMT', 21,'D2O',52/
'N1', 0.1000, 0.000, 1.7716088E-1, 4.7494E-1, , , 'CIRC',1,'D2O'/
'N2', 0.1000, 0.000, 1.7716088E-1, 4.7494E-1, , , 'CIRC',1,'D2O'/
'N3', 0.1000, 0.000, 2.1123028E-1, 5.1860E-1, , , 'CIRC',1,'D2O'/
'N4', 0.1000, 0.000, 1.6353312E-1, 4.5631E-1, , , 'CIRC',1,'D2O'/
'N5', 0.1000, 0.000, 2.1123028E-1, 5.1860E-1, , , 'CIRC',1,'D2O'/
'N6', 0.1000, 0.000, 1.7716088E-1, 4.7494E-1, , , 'CIRC',1,'D2O'/
'N7', 0.1000, 0.000, 1.7716088E-1, 4.7494E-1, , , 'CIRC',1,'D2O'/
'W1', , , , , , ,'VOLMC', ,D2O, , 0.0001/
'W2', , , , , , ,'VOLMC', ,D2O, , 0.0001/
'W3', , , , , , ,'VOLMC', ,D2O, , 0.0001/
'W4', , , , , , ,'VOLMC', ,D2O, , 0.0001/
'W5', , , , , , ,'VOLMC', ,D2O, , 0.0001/
'W6', , , , , , ,'VOLMC', ,D2O, , 0.0001/
'M0', 0.1000, 0.000, 1.2946372, 1.28389, , , 'CIRC', 1, 'D2O'/
'M1', 0.1000, 0.000, 5.6555204E-1, 8.485772E-1, , , 'CIRC', 1, 'D2O'/
'M2', 0.1000, 0.000, 7.2908516E-1, 9.634833E-1, , , 'CIRC', 1, 'D2O'/
'M3', 0.1000, 0.000, 3.5432176E-1, 6.716670E-1, , , 'CIRC', 1, 'D2O'/
'M4', 0.1000, 0.000, 3.7476340E-1, 6.907703E-1, , , 'CIRC', 1, 'D2O'/
'M5', 0.1000, 0.000, 3.5432176E-1, 6.716670E-1, , , 'CIRC', 1, 'D2O'/
'OUTBC',,,,,,,,'D2O'/
'END'/ OF COMPONENTS GROUP
'CONNECTIONS'/ OF COMPONENTS
'INBC','L-P0'/
'R-P0','V1'/
'V1','L-P1'/
'V1','L-P2'/
'R-P1','V2'/
'V2','L-P3'/
'V2','L-Z3'/

'R-Z3','L-ZONE3'/
'R-P2','V3'/
'V3','L-P4'/
'V3','L-P5'/
'R-P3','V4'/
'V4','L-Z1'/
'V4','L-Z2'/
'R-Z1','L-ZONE1'/
'R-Z2','L-ZONE2'/
'R-P4','V5'/
'V5','L-Z4'/
'V5','L-Z5'/
'R-Z4','L-ZONE4'/
'R-Z5','L-ZONE5'/
'R-P5','V6'/
'V6','L-Z6'/
'V6','L-Z7'/
'R-Z6','L-ZONE6'/
'R-Z7','L-ZONE7'/
'R-ZONE1','L-N1'/
'R-ZONE2','L-N2'/
'R-N1','W4'/
'R-N2','W4'/
'W4','L-M3'/
'R-ZONE4','L-N4'/
'R-ZONE5','L-N5'/
'R-N4','W5'/
'R-N5','W5'/
'W5','L-M4'/
'R-ZONE6','L-N6'/
'R-ZONE7','L-N7'/
'R-N6','W6'/
'R-N7','W6'/
'W6','L-M5'/
'R-ZONE3','L-N3'/
'R-M3','W2'/
'R-N3','W2'/
'W2','L-M1'/
'R-M4','W3'/
'R-M5','W3'/
'W3','L-M2'/
'R-M1','W1'/

```
'R-M2','W1'/
'W1','L-M0'/
'R-M0','OUTBC'/
'END' /OF CONNECTIONS
'BOUNDARY CONDITIONS'/
'RESERVOIR B.C.', 'RIH'/
'INBC'/
11.75E6, , 2.65E2, 0, 'HG-BY-SAT', 'HF-BY-TEMP'/
'RESERVOIR B.C.', 'ROH'/
'OUTBC'/
10.0E6, , 3.1E2, 0, 'HG-BY-SAT', 'HF-BY-TEMP'/
'FLOW B.C.','FWFLOW'/
'INBC','L-P0'/
9120/
'END'/OF BOUNDARY CONDITIONS
'SYSTEM MODELS'/
'KINETICS', 'RPOWER1'/
1, 21, 'SIM_PK', 'DEN_VOID'/
0.001, 'EQUILIBRIUM', 'CANDU', '.FALSE.'/
/
'FUELCHL1'/ GENHTP model label
'QUADRATIC', 'DIF'/ fluid density coefficient
0.0, -0.0118/
'QUADRATIC', 'DIF'/ fuel temperature coefficient
3.747E-6, -0.006/
'QUADRATIC', 'DIF'/ fluid temperature coefficient
0.0,0.0/
'KINETICS', 'RPOWER2'/
1, 21, 'SIM_PK', 'DEN_VOID'/
0.001, 'EQUILIBRIUM', 'CANDU', '.FALSE.'/
/
'FUELCHL2'/ GENHTP model label
'QUADRATIC', 'DIF'/ fluid density coefficient
0.0, -0.0118/
'QUADRATIC', 'DIF'/ fuel temperature coefficient
3.747E-6, -0.006/
'QUADRATIC', 'DIF'/ fluid temperature coefficient
0.0,0.0/
'KINETICS', 'RPOWER3'/
1, 21, 'SIM_PK', 'DEN_VOID'/
0.001, 'EQUILIBRIUM', 'CANDU', '.FALSE.'/
/
```

```
'FUELCHL3'/ GENHTP model label
'QUADRATIC', 'DIF'/ fluid density coefficient
0.0, -0.0118/
'QUADRATIC', 'DIF'/ fuel temperature coefficient
3.747E-6, -0.006/
'QUADRATIC', 'DIF'/ fluid temperature coefficient
0.0,0.0/
'KINETICS', 'RPOWER4'/
1, 21, 'SIM_PK', 'DEN_VOID'/
0.001, 'EQUILIBRIUM', 'CANDU', '.FALSE.'/
/
'FUELCHL4'/ GENHTP model label
'QUADRATIC', 'DIF'/ fluid density coefficient
0.0, -0.0118/
'QUADRATIC', 'DIF'/ fuel temperature coefficient
3.747E-6, -0.006/
'QUADRATIC', 'DIF'/ fluid temperature coefficient
0.0,0.0/
'KINETICS', 'RPOWER5'/
1, 21, 'SIM_PK', 'DEN_VOID'/
0.001, 'EQUILIBRIUM', 'CANDU', '.FALSE.'/
/
'FUELCHL5'/ GENHTP model label
'QUADRATIC', 'DIF'/ fluid density coefficient
0.0, -0.0118/
'QUADRATIC', 'DIF'/ fuel temperature coefficient
3.747E-6, -0.006/
'QUADRATIC', 'DIF'/ fluid temperature coefficient
0.0,0.0/
'KINETICS', 'RPOWER6'/
1, 21, 'SIM_PK', 'DEN_VOID'/
0.001, 'EQUILIBRIUM', 'CANDU', '.FALSE.'/
/
'FUELCHL6'/ GENHTP model label
'QUADRATIC', 'DIF'/ fluid density coefficient
0.0, -0.0118/
'QUADRATIC', 'DIF'/ fuel temperature coefficient
3.747E-6, -0.006/
'QUADRATIC', 'DIF'/ fluid temperature coefficient
0.0,0.0/
'KINETICS', 'RPOWER7'/
1, 21, 'SIM_PK', 'DEN_VOID'/
```

```
0.001, 'EQUILIBRIUM', 'CANDU', '.FALSE.'/
/
'FUELCHL7'/ GENHTP model label
'QUADRATIC', 'DIF'/ fluid density coefficient
0.0, -0.0118/
'QUADRATIC', 'DIF'/ fuel temperature coefficient
3.747E-6, -0.006/
'QUADRATIC', 'DIF'/ fluid temperature coefficient
0.0,0.0/
'END'/ of system models
'SYSTEM CONTROL'/
'CALCULATE','NOMPWR','.FALSE.'/
'PROGRAM'/
C     CALCULATE THE NOMALIZED POWER
C
      DATA S1 /2.65833E8/, S2 /2.64288E8/, S3 /3.46352E8/
      DATA S4 /3.06073E8/,S5 /3.4821E8/,S6 /2.65905E8/,S7 /2.6456E8/
      R1="THER_PWR:RPOWER1"*S1
      R2="THER_PWR:RPOWER2"*S2
      R3="THER_PWR:RPOWER3"*S3
      R4="THER_PWR:RPOWER4"*S4
      R5="THER_PWR:RPOWER5"*S5
      R6="THER_PWR:RPOWER6"*S6
      R7="THER_PWR:RPOWER7"*S7
      NOMPWR=(R1+R2+R3+R4+R5+R6+R7)/2.061221E9
C
      END
/
'INPUT TABLE','FLOWTAB'/
1,15/
'TIME','FFLOW'/
0.0, 9192/
0.3, -640.008/
0.4, -705.996/
0.5, -773.373/
0.6, -840.02/
0.7, -656.67/
0.8, -473.32/
0.9, -289.97/
1.0, -353.33/
1.1, -416.68/
1.25,-479.97/
```

```
1.7, -310.01/
2.2, -290.03/
2.6, -304/
4.0, -69.63/
'TIME VAR.','FEEDFLOW'/
'FLOWTAB','FFLOW'/
1.0/
'FWFLOW','MFLO','.FALSE.'/
/
'INPUT TABLE','SDSRVT'/
1,9/
'TIME','DREACT'/
0.0, 0.0/
0.4, -2.0/
0.6, -5.46/*-1.0
0.8, -9.10/*-2.73
1.0, -13.64/*-4.55
1.2, -30.28/*-6.82
1.4, -47.36/*-25.0
1.6, -64.24/*-43.18
1.8, -80/*-48.62
'TIME VAR.','REACTV'/
'SDSRVT','DREACT'/
/
'RPOWER1','DK_ADD'/ application point is region 1 power
'RPOWER2','DK_ADD'/ application point is region 2 power
'RPOWER3','DK_ADD'/ application point is region 3 power
'RPOWER4','DK_ADD'/ application point is region 4 power
'RPOWER5','DK_ADD'/ application point is region 5 power
'RPOWER6','DK_ADD'/ application point is region 6 power
'RPOWER7','DK_ADD'/ application point is region 7 power
/
'TRIP','HIGHPWR'/
'COMPARE'/
'NOMPWR',1.0,0.01/  measurement time constant of 0.01s
/
'GT'/
'CONSTANT(1.05)'/ neutron overpower trip setpoint
/
/
/
'TRIP','HIGHRAT'/
```

```
'COMPARE'/
'FIS_LG_I:RPOWER4',1.0,0.25/
/
'GT'/
'CONSTANT(0.1)'/ log rate trip setpoint
/
/
/
'TRIP', 'TRIPPWR'/
'OR'/
'HIGHPWR'/
'HIGHRAT'/
/
0.0, 0.1/ TDWAIT,TDELAY (SDS1 decision-making time)
'REACTV'/ application point
/
'OUTPUT','OUT0'/
1,'CPOWER.OUT','(1X,F13.6,1X,F10.4)',0,0.01/ output file of core power transient
'NOMPWR'/
/
'OUTPUT','PWROUT1'/
1,'Z1PWR.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'THER_PWR:RPOWER1'/
/
'OUTPUT','PWROUT2'/
1,'Z2PWR.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'THER_PWR:RPOWER2'/
/
'OUTPUT','PWROUT3'/
1,'Z3PWR.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'THER_PWR:RPOWER3'/
/
'OUTPUT','PWROUT4'/
1,'Z4PWR.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'THER_PWR:RPOWER4'/
/
'OUTPUT','PWROUT5'/
1,'Z5PWR.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'THER_PWR:RPOWER5'/
/
'OUTPUT','PWROUT6'/
1,'Z6PWR.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
```

```
'THER_PWR:RPOWER6'/
/
'OUTPUT','PWROUT7'/
1,'Z7PWR.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'THER_PWR:RPOWER7'/
/
'OUTPUT','TEMP1'/
1,'Z1TEMPF35.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'TWALL:FUELCHL1(11,21,1,1)'/
/
'OUTPUT','TEMP2'/
1,'Z2TEMPF35.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'TWALL:FUELCHL2(11,21,1,1)'/
/
'OUTPUT','TEMP3'/
1,'Z3TEMPF35.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'TWALL:FUELCHL3(11,21,1,1)'/
/
'OUTPUT','TEMP4'/
1,'Z4TEMPF35.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'TWALL:FUELCHL4(11,21,1,1)'/
/
'OUTPUT','TEMP5'/
1,'Z5TEMPF35.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'TWALL:FUELCHL5(11,21,1,1)'/
/
'OUTPUT','TEMP6'/
1,'Z6TEMPF35.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'TWALL:FUELCHL6(11,21,1,1)'/
/
'OUTPUT','TEMP7'/
1,'Z7TEMPF35.OUT','(1X,F13.6,1X,F10.4)',0,0.01/
'TWALL:FUELCHL7(11,21,1,1)'/
/
'OUTPUT','OUT3'/
1,'CFLOW.OUT','(1X,F13.6,1X,F10.4)',,0.01/
'MFLO:INBC>L-P0'/
/
'OUTPUT', 'OUT4'/
1,'CTEMPC.OUT','(1X,F13.6,1X,F10.4)',,0.01/
'TEMPF:ZONE4(11)'/
/
```

'END'/ of system control
'HEAT TRANSFER PACKAGE'/
'MODEL:(FUELCHL1)'/
'RADIAL:(3,0.00,20,.61214E-02,2,.61214E-02,10,.65405E-02)',
'AXIAL:(5.9436,21)-EQUAL-SEGMENT', 'SECTOR:(1,1)',
'CYLINDER:(1,1924)',
'HEATED LENGTH:(5.770485)'/
'BOUNDARY CONDITIONS:(0,1)'/
'OUTSIDE HYDRAULIC:(ZONE1)'/
'37-ROD-1', 'HT-CRIT-(2*0,2*2,2*2)','HT-CORR-DEFAULT',,,
'WALL-INTERFACE-HEAT-TRANSFER:(6*5,1)','CORRECTION FACTOR:(,,,,,,,,0.97,)'/
'UO2'/
'GAP:(10000.,0.00,0.00)'/ GAP CONDUCTANCE, conservatively using 37-element bundle
'ZIRCALOY'/ SHEATH
'HQ-TIME:(265833000,RPOWER1)'/
'R-UNIFORM','S-UNIFORM','A-USER','C-UNIFORM'/
0.0056,0.0166,0.0273,0.0374,0.0466,0.0548,0.0617,0.0673,0.0714,0.0739,0.0747,0.0739,
0.0714,0.0673,0.0617,0.0548,0.0466,0.0374,0.0273,0.0166,0.0056/ Axial power distribution
'HQ-NIL'/ GAP
'HQ-NIL'/ SHEATH
'TEMP-4D'/
308 308 308 307 307 306 305 304 302 301 299 297 295 293 291 288 285 282 279 276
269 269 269 268 268 268 268 267 267 267/
400 399 398 397 395 392 389 385 380 375 369 363 357 349 342 334 325 316 307 297
275 274 274 273 273 272 271 271 270 270/
502 501 499 496 492 487 481 474 465 456 446 435 423 410 396 382 367 351 335 318
282 281 280 279 278 277 276 275 274 273/
611 610 607 603 597 589 579 568 555 541 526 509 491 472 452 430 408 386 362 339
290 289 287 286 284 283 282 280 279 278/
723 722 718 711 703 692 679 663 646 626 605 582 558 532 505 477 448 418 388 357
297 295 293 292 290 288 287 285 283 281/
835 833 828 820 809 794 777 757 735 710 683 654 623 590 556 521 486 449 412 375
304 302 300 298 296 294 292 290 288 286/
940 937 931 921 907 889 868 844 817 786 753 718 681 642 602 561 519 476 433 391
310 308 306 304 301 299 297 295 292 290/
1032 1029 1022 1010 994 973 949 921 889 854 815 775 732 688 642 595 548 500 452 404
316 314 311 309 306 304 302 299 297 294/
1106 1103 1095 1081 1063 1040 1013 981 946 907 864 820 773 724 673 622 570 518 466 415
322 319 316 314 311 309 306 304 301 299/
1156 1152 1143 1129 1110 1085 1056 1022 984 942 897 850 800 748 694 640 586 531 476 422
326 324 321 318 315 313 310 308 305 302/
1176 1172 1163 1149 1129 1104 1074 1039 1000 958 912 863 812 759 704 649 593 537 482 427

330 327 324 322 319 316 314 311 308 306/
1168 1164 1156 1141 1122 1097 1068 1033 995 953 908 860 809 757 703 648 593 538 483 429
332 330 327 324 322 319 317 314 311 309/
1131 1127 1119 1105 1087 1063 1036 1003 967 927 885 839 791 741 690 638 585 532 479 427
334 331 329 326 324 321 319 316 314 311/
1067 1064 1056 1044 1027 1006 981 952 919 883 844 803 759 713 666 618 569 520 471 422
335 332 330 327 325 322 320 318 315 313/
982 979 973 962 948 930 908 883 855 823 789 753 715 675 633 590 547 503 459 414
334 332 330 327 325 323 321 319 316 314/
883 881 876 867 855 840 823 802 778 752 724 694 661 628 592 556 519 481 442 404
333 331 329 327 325 323 321 319 317 315/
774 772 768 762 753 741 727 711 693 672 650 626 601 573 545 516 485 454 423 391
330 328 327 325 323 322 320 318 317 315/
663 662 659 654 647 639 629 617 604 589 573 555 536 516 494 472 449 425 400 375
326 325 324 322 321 320 318 317 316 314/
553 552 550 547 543 537 531 523 514 504 493 482 469 455 441 425 409 393 376 358
322 321 320 319 318 317 316 315 314 313/
448 448 447 445 443 440 436 432 427 422 416 410 402 395 387 378 369 359 349 339
317 316 316 315 315 314 313 313 312 312/
353 353 353 352 352 351 350 348 347 345 344 342 339 337 334 332 329 326 322 319
312 312 311 311 311 311 311 310 310 310/
'PRINT:(33008)','CALCULATE STATISTICS'/
'MODEL:(FUELCHL2)'/
'RADIAL:(3,0.00,20,.61214E-02,2,.61214E-02,10,.65405E-02)',
'AXIAL:(5.9436,21)-EQUAL-SEGMENT', 'SECTOR:(1,1)',
'CYLINDER:(1,1924)',
'HEATED LENGTH:(5.770485)'/
'BOUNDARY CONDITIONS:(0,1)'/
'OUTSIDE HYDRAULIC:(ZONE2)'/
'37-ROD-1', 'HT-CRIT-(2*0,2*2,2*2)','HT-CORR-DEFAULT',,,
'WALL-INTERFACE-HEAT-TRANSFER:(6*5,1)','CORRECTION FACTOR:(,,,,,,,,0.97,)'/
'UO2'/
'GAP:(10000.,0.00,0.00)'/ GAP CONDUCTANCE, conservatively using 37-element bundle
'ZIRCALOY'/ SHEATH
'HQ-TIME:(264288000,RPOWER2)'/
'R-UNIFORM','S-UNIFORM','A-USER','C-UNIFORM'/
0.0056,0.0166,0.0273,0.0374,0.0466,0.0548,0.0617,0.0673,0.0714,0.0739,0.0747,0.0739,
0.0714,0.0673,0.0617,0.0548,0.0466,0.0374,0.0273,0.0166,0.0056/ Axial power distribution
'HQ-NIL'/ GAP
'HQ-NIL'/ SHEATH
'TEMP-4D'/
308 308 308 307 306 306 305 304 302 301 299 297 295 293 290 288 285 282 279 276

```
269 269 269 268 268 268 268 267 267 267/
399 398 397 396 394 391 388 384 379 374 369 363 356 349 341 333 325 316 306 296
275 274 274 273 273 272 271 271 270 270/
500 499 497 495 491 486 479 472 464 455 445 434 422 409 395 381 366 350 334 318
282 281 280 279 278 277 276 275 274 273/
609 607 605 600 594 586 577 566 553 539 524 507 489 470 450 429 407 385 362 338
290 288 287 286 284 283 281 280 279 277/
719 718 714 708 699 688 675 660 643 623 602 580 556 530 503 475 447 417 387 357
297 295 293 291 290 288 286 285 283 281/
830 828 823 815 804 790 773 753 731 706 679 650 620 588 554 519 484 448 411 374
304 302 300 298 296 294 292 290 288 286/
933 931 925 915 901 884 863 839 812 782 749 715 678 639 600 559 517 475 432 390
310 308 306 303 301 299 297 294 292 290/
1025 1022 1015 1003 987 967 943 915 883 848 811 771 728 684 639 593 545 498 450 403
316 314 311 309 306 304 301 299 297 294/
1098 1095 1087 1074 1056 1033 1006 975 940 901 859 815 768 720 670 619 568 516 465 414
321 319 316 314 311 308 306 303 301 298/
1147 1143 1135 1121 1101 1077 1048 1015 977 936 892 845 795 744 691 637 583 529 475 421
326 323 320 318 315 312 310 307 305 302/
1167 1163 1155 1140 1121 1096 1066 1032 994 951 906 858 807 755 701 646 591 535 480 426
329 327 324 321 319 316 313 311 308 305/
1159 1156 1147 1133 1114 1089 1060 1026 988 947 902 854 804 753 699 645 591 536 481 428
332 329 327 324 321 319 316 314 311 308/
1122 1119 1110 1097 1079 1056 1028 997 961 922 879 834 787 737 687 635 583 530 478 426
334 331 328 326 323 321 318 316 313 311/
1059 1056 1049 1037 1020 999 975 946 913 878 839 798 755 710 663 615 567 518 470 421
334 332 329 327 325 322 320 317 315 313/
975 973 966 956 942 924 902 878 850 819 785 749 711 671 630 588 545 501 457 413
334 331 329 327 325 323 320 318 316 314/
878 875 870 862 850 835 818 797 774 748 720 690 658 625 590 554 517 479 441 403
332 330 328 326 324 322 320 318 317 315/
770 768 764 758 749 737 724 708 689 669 647 623 598 571 543 514 484 453 422 390
330 328 326 324 323 321 320 318 316 315/
660 658 656 651 644 636 626 615 601 586 570 553 534 514 493 470 448 424 399 374
326 325 323 322 321 319 318 317 315 314/
551 550 548 545 541 535 529 521 512 503 492 480 467 454 439 424 408 392 375 357
322 321 320 319 318 317 316 315 314 313/
447 447 446 444 442 439 435 431 426 421 415 409 402 394 386 377 368 359 349 338
317 316 316 315 314 314 313 313 312 311/
353 353 352 352 351 350 349 348 346 345 343 341 339 337 334 331 328 325 322 319
311 311 311 311 311 310 310 310 310 310/
'PRINT:(33008)','CALCULATE STATISTICS'/
```

'MODEL:(FUELCHL3)'/
'RADIAL:(3,0.00,20,.61214E-02,2,.61214E-02,10,.65405E-02)',
'AXIAL:(5.9436,21)-EQUAL-SEGMENT', 'SECTOR:(1,1)',
'CYLINDER:(1,2294)',
'HEATED LENGTH:(5.770485)'/
'BOUNDARY CONDITIONS:(0,1)'/
'OUTSIDE HYDRAULIC:(ZONE3)'/
'37-ROD-1', 'HT-CRIT-(2*0,2*2,2*2)','HT-CORR-DEFAULT',,,
'WALL-INTERFACE-HEAT-TRANSFER:(6*5,1)','CORRECTION FACTOR:(,,,,,,,,0.97,)'/
'UO2'/
'GAP:(10000.,0.00,0.00)'/ GAP CONDUCTANCE, conservatively using 37-element bundle
'ZIRCALOY'/ SHEATH
'HQ-TIME:(346352000,RPOWER3)'/
'R-UNIFORM','S-UNIFORM','A-USER','C-UNIFORM'/
0.0056,0.0166,0.0273,0.0374,0.0466,0.0548,0.0617,0.0673,0.0714,0.0739,0.0747,0.0739,
0.0714,0.0673,0.0617,0.0548,0.0466,0.0374,0.0273,0.0166,0.0056/ Axial power distribution
'HQ-NIL'/ GAP
'HQ-NIL'/ SHEATH
'TEMP-4D'/
311 311 311 311 310 309 308 307 305 303 302 300 297 295 292 290 287 284 280 277
269 269 269 268 268 268 268 267 267 267/
410 410 409 407 405 402 398 394 389 384 377 371 364 356 347 339 329 319 309 299
275 275 274 273 273 272 271 271 270 269/
522 521 519 516 511 506 499 491 482 472 460 448 435 421 406 390 374 357 339 321
283 282 281 280 278 277 276 275 274 273/
642 641 638 633 626 617 607 594 580 565 548 529 509 488 466 443 419 394 369 343
291 289 287 286 285 283 282 280 279 277/
767 765 760 753 744 731 717 699 680 658 635 609 582 554 524 493 461 429 396 363
297 296 294 292 290 288 286 285 283 281/
892 889 884 874 862 846 826 804 778 751 720 688 653 617 580 541 502 462 422 381
305 302 300 298 296 294 292 289 287 285/
1009 1006 999 987 972 952 928 900 870 835 799 759 718 674 630 584 538 491 444 397
311 309 306 304 301 299 297 294 292 289/
1113 1110 1102 1088 1070 1046 1018 986 950 910 867 822 774 724 673 621 568 516 463 411
317 314 312 309 306 304 301 299 296 294/
1197 1193 1183 1168 1148 1121 1090 1054 1014 969 922 871 818 763 707 650 593 535 478 422
322 320 317 314 311 308 306 303 300 297/
1252 1248 1238 1222 1200 1172 1138 1099 1056 1009 958 904 848 789 730 670 609 549 489 430
327 324 321 318 315 312 310 307 304 301/
1275 1270 1260 1244 1221 1192 1158 1118 1074 1026 973 918 861 801 740 679 617 555 495 435
330 327 324 322 319 316 313 310 307 304/
1265 1261 1251 1234 1212 1184 1150 1111 1067 1020 968 914 857 798 738 678 617 556 495 436

```
333  330  327  324  321  318  316  313  310  307/
1221 1217 1208 1192 1171 1145 1113 1076 1035  990  942  890  836  781  724  666  607  549  491  434
334  331  329  326  323  320  318  315  312  310/
1148 1145 1136 1122 1103 1079 1051 1018  981  940  896  849  800  749  697  644  590  536  482  429
335  332  329  327  324  322  319  316  314  311/
1051 1048 1041 1029 1013  993  968  940  908  872  834  794  751  706  660  613  565  517  468  420
334  331  329  327  324  322  320  317  315  313/
940  937  931  922  908  892  871  848  822  793  761  727  691  654  615  575  534  493  451  409
332  330  328  326  324  322  319  317  315  313/
817  815  811  803  793  780  765  747  726  704  679  652  624  594  563  531  498  464  429  395
329  328  326  324  322  320  319  317  315  313/
693  692  689  683  676  667  656  643  628  612  593  574  553  531  507  483  458  432  405  378
326  324  323  321  320  318  317  316  314  313/
572  571  569  565  561  555  548  539  529  519  507  494  480  465  449  433  415  397  379  359
321  320  319  318  317  316  315  314  313  312/
458  457  456  454  452  449  445  440  435  429  423  416  408  400  391  381  371  361  350  339
316  315  314  314  313  312  312  311  311  310/
355  355  354  354  353  352  351  350  348  346  344  342  340  337  335  332  328  325  322  318
310  310  310  309  309  309  309  309  308  308/
'PRINT:(33008)','CALCULATE STATISTICS'/
'MODEL:(FUELCHL4)'/
'RADIAL:(3,0.00,20,.61214E-02,2,.61214E-02,10,.65405E-02)',
'AXIAL:(5.9436,21)-EQUAL-SEGMENT', 'SECTOR:(1,1)',
'CYLINDER:(1,1776)',
'HEATED LENGTH:(5.770485)'/
'BOUNDARY CONDITIONS:(0,1)'/
'OUTSIDE HYDRAULIC:(ZONE4)'/
'37-ROD-1', 'HT-CRIT-(2*0,2*2,2*2)','HT-CORR-DEFAULT',,,
'WALL-INTERFACE-HEAT-TRANSFER:(6*5,1)','CORRECTION FACTOR:(,,,,,,,,0.97,)'/
'UO2'/
'GAP:(10000.,0.00,0.00)'/ GAP CONDUCTANCE, conservatively using 37-element bundle
'ZIRCALOY'/ SHEATH
'HQ-TIME:(281040000,RPOWER4)'/
'R-UNIFORM','S-UNIFORM','A-USER','C-UNIFORM'/
0.0056,0.0166,0.0273,0.0374,0.0466,0.0548,0.0617,0.0673,0.0714,0.0739,0.0747,0.0739,
0.0714,0.0673,0.0617,0.0548,0.0466,0.0374,0.0273,0.0166,0.0056/  Axial power distribution
'HQ-NIL'/ GAP
'HQ-NIL'/ SHEATH
'TEMP-4D'/
316  316  316  315  314  313  312  311  309  307  305  303  301  298  295  292  289  285  282  278
269  269  269  269  268  268  268  267  267  267/
427  427  425  423  421  418  413  409  403  397  390  383  375  366  357  347  337  326  314  303
```

```
277  276  276  275  274  273  273  272  271  271/
554  553  550  547  542  535  528  518  508  497  484  470  455  439  423  405  387  368  348  328
286  285  283  282  281  280  279  278  276  275/
692  690  687  681  673  663  651  637  621  603  583  562  539  515  490  464  437  409  381  352
295  293  291  290  288  286  285  283  282  280/
837  835  830  822  811  796  779  759  736  711  684  655  623  591  557  522  486  449  412  375
303  301  299  297  295  293  291  289  287  285/
986  983  976  965  950  931  908  882  852  819  784  746  706  664  621  577  532  487  441  396
312  309  307  304  302  300  297  295  293  290/
1126 1122 1114 1100 1081 1058 1029  997  960  919  876  830  781  731  679  626  573  520  467  414
319  317  314  311  309  306  304  301  298  296/
1252 1248 1238 1222 1199 1171 1138 1099 1056 1009  958  904  847  789  730  669  609  548  489  430
327  324  321  318  315  312  309  307  304  301/
1353 1349 1337 1319 1294 1262 1225 1181 1133 1080 1023  963  900  835  770  703  637  571  506  443
333  330  327  324  321  318  315  312  309  306/
1421 1416 1404 1384 1358 1324 1283 1237 1185 1128 1067 1002  936  867  797  727  656  587  519  452
338  335  332  329  326  323  320  317  314  310/
1449 1444 1432 1411 1384 1349 1308 1260 1207 1148 1086 1020  951  881  809  737  666  595  525  458
343  340  336  333  330  327  324  321  318  315/
1437 1432 1420 1400 1373 1339 1298 1251 1199 1141 1080 1015  947  878  807  736  665  595  526  459
346  342  339  336  333  330  327  324  321  318/
1384 1379 1368 1349 1324 1292 1253 1209 1160 1106 1048  986  922  857  790  722  654  587  521  457
347  344  341  338  335  332  329  326  323  320/
1296 1291 1281 1264 1242 1213 1178 1139 1094 1045  993  938  880  820  758  696  634  572  511  451
347  344  341  339  336  333  330  327  325  322/
1179 1176 1167 1153 1133 1109 1079 1045 1007  965  920  872  822  769  716  661  606  550  495  441
346  344  341  338  336  333  331  328  326  323/
1045 1042 1035 1024 1008  988  964  936  905  871  834  794  752  709  663  617  570  523  475  428
344  342  339  337  335  332  330  328  326  323/
900  898  892  884  872  857  838  817  793  767  738  707  674  640  604  567  529  490  451  412
341  339  337  335  333  331  329  327  325  323/
754  752  749  742  734  723  710  695  678  659  638  616  592  566  540  512  483  454  424  393
336  334  333  331  329  328  326  325  323  322/
612  611  609  605  600  593  585  575  564  552  538  523  507  491  473  454  434  414  393  372
330  329  327  326  325  324  323  322  321  319/
482  481  480  478  475  471  467  462  456  449  442  434  425  416  406  396  385  373  361  348
323  322  321  321  320  319  319  318  317  317/
365  365  365  364  364  362  361  360  358  356  354  351  349  346  343  340  336  333  329  325
316  316  315  315  315  315  314  314  314  314/
'PRINT:(33008)','CALCULATE STATISTICS'/
'MODEL:(FUELCHL5)'/
'RADIAL:(3,0.00,20,.61214E-02,2,.61214E-02,10,.65405E-02)',
```

'AXIAL:(5.9436,21)-EQUAL-SEGMENT', 'SECTOR:(1,1)',
'CYLINDER:(1,2294)',
'HEATED LENGTH:(5.770485)'/
'BOUNDARY CONDITIONS:(0,1)'/
'OUTSIDE HYDRAULIC:(ZONE5)'/
'37-ROD-1', 'HT-CRIT-(2*0,2*2,2*2)','HT-CORR-DEFAULT',,,
'WALL-INTERFACE-HEAT-TRANSFER:(6*5,1)','CORRECTION FACTOR:(,,,,,,,,0.97,)'/
'UO2'/
'GAP:(10000.,0.00,0.00)'/ GAP CONDUCTANCE, conservatively using 37-element bundle
'ZIRCALOY'/ SHEATH
'HQ-TIME:(348210000,RPOWER5)'/
'R-UNIFORM','S-UNIFORM','A-USER','C-UNIFORM'/
0.0056,0.0166,0.0273,0.0374,0.0466,0.0548,0.0617,0.0673,0.0714,0.0739,0.0747,0.0739,
0.0714,0.0673,0.0617,0.0548,0.0466,0.0374,0.0273,0.0166,0.0056/ Axial power distribution
'HQ-NIL'/ GAP
'HQ-NIL'/ SHEATH
'TEMP-4D'/
312 312 312 311 311 310 309 307 306 304 302 300 298 296 293 290 287 284 281 277
269 269 269 269 268 268 268 268 267 267/
414 414 413 411 408 405 402 397 392 387 380 374 366 358 350 341 331 321 311 300
276 275 275 274 273 273 272 271 271 270/
529 528 526 523 518 512 505 497 488 477 466 453 440 425 410 394 377 360 342 323
284 283 282 281 280 278 277 276 275 274/
653 652 649 644 637 628 617 604 589 573 556 537 516 494 472 448 423 398 372 346
292 291 289 288 286 285 283 282 280 279/
782 780 776 769 759 746 731 713 693 670 646 620 592 563 532 500 468 434 401 366
300 298 296 294 292 290 289 287 285 283/
912 910 904 894 881 865 845 821 795 766 735 701 666 628 590 550 510 469 427 386
308 305 303 301 299 297 294 292 290 288/
1035 1032 1024 1012 996 976 951 922 890 855 816 776 733 688 642 595 547 499 451 403
315 312 310 307 305 302 300 297 295 293/
1144 1141 1132 1118 1099 1074 1045 1012 974 933 888 841 791 740 687 633 579 525 471 417
321 319 316 313 310 308 305 303 300 297/
1232 1228 1218 1202 1181 1153 1121 1083 1041 995 945 893 838 781 723 664 604 545 487 429
327 324 321 319 316 313 310 307 305 302/
1291 1286 1276 1259 1236 1206 1171 1131 1086 1037 984 928 869 809 747 685 622 560 498 438
332 329 326 323 320 317 314 312 309 306/
1315 1310 1299 1282 1258 1228 1193 1151 1105 1055 1000 943 883 821 758 694 630 567 504 443
336 333 330 327 324 321 318 315 312 310/
1305 1301 1290 1273 1250 1220 1185 1144 1099 1049 996 939 880 819 757 694 630 567 505 444
339 336 333 330 327 324 321 319 316 313/
1260 1256 1246 1230 1208 1180 1147 1108 1066 1019 968 915 859 801 741 681 621 561 501 442

340 338 335 332 329 326 324 321 318 315/
1184 1180 1171 1156 1137 1112 1082 1047 1009 966 921 872 821 768 714 659 603 547 492 437
341 338 335 333 330 328 325 322 320 317/
1083 1079 1072 1060 1043 1021 996 966 933 896 856 814 770 723 676 627 577 527 478 428
340 338 335 333 330 328 325 323 321 318/
966 964 957 947 934 916 895 871 844 813 781 746 708 670 629 588 546 503 460 416
338 336 334 332 330 327 325 323 321 319/
839 837 832 825 814 801 785 766 745 721 696 668 639 608 576 542 508 473 438 402
335 333 332 330 328 326 324 323 321 319/
711 709 706 701 693 683 672 658 643 626 607 587 565 542 518 493 467 440 413 385
332 330 329 327 326 324 323 321 320 318/
585 584 582 578 574 567 560 551 541 530 518 505 490 475 458 441 423 405 386 366
327 326 325 324 323 321 320 319 318 317/
467 467 466 464 461 458 454 449 444 438 431 424 416 408 398 389 379 368 357 345
321 321 320 319 319 318 317 317 316 316/
362 361 361 360 360 359 358 356 355 353 351 349 346 344 341 338 334 331 327 324
316 315 315 315 315 315 314 314 314 314/
'PRINT:(33008)','CALCULATE STATISTICS'/
'MODEL:(FUELCHL6)'/
'RADIAL:(3,0.00,20,.61214E-02,2,.61214E-02,10,.65405E-02)',
'AXIAL:(5.9436,21)-EQUAL-SEGMENT', 'SECTOR:(1,1)',
'CYLINDER:(1,1924)',
'HEATED LENGTH:(5.770485)'/
'BOUNDARY CONDITIONS:(0,1)'/
'OUTSIDE HYDRAULIC:(ZONE6)'/
'37-ROD-1', 'HT-CRIT-(2*0,2*2,2*2)','HT-CORR-DEFAULT',,,
'WALL-INTERFACE-HEAT-TRANSFER:(6*5,1)','CORRECTION FACTOR:(,,,,,,,0.97,)'/
'UO2'/
'GAP:(10000.,0.00,0.00)'/ GAP CONDUCTANCE, conservatively using 37-element bundle
'ZIRCALOY'/ SHEATH
'HQ-TIME:(265905000,RPOWER6)'/
'R-UNIFORM','S-UNIFORM','A-USER','C-UNIFORM'/
0.0056,0.0166,0.0273,0.0374,0.0466,0.0548,0.0617,0.0673,0.0714,0.0739,0.0747,0.0739,
0.0714,0.0673,0.0617,0.0548,0.0466,0.0374,0.0273,0.0166,0.0056/ Axial power distribution
'HQ-NIL'/ GAP
'HQ-NIL'/ SHEATH
'TEMP-4D'/
308 308 308 307 307 306 305 304 302 301 299 297 295 293 291 288 285 282 279 276
269 269 269 268 268 268 268 267 267 267/
399 399 398 397 394 392 388 384 380 375 369 363 357 349 342 334 325 316 306 297
275 274 274 273 273 272 271 271 270 270/
501 501 499 496 492 487 481 474 465 456 446 435 423 410 396 382 367 351 335 318

282 281 280 279 278 277 276 275 274 273/
611 610 607 603 596 588 579 568 555 541 525 509 491 471 451 430 408 386 362 338
290 288 287 286 284 283 282 280 279 277/
723 721 717 711 702 691 678 663 645 626 605 582 557 532 505 477 448 418 388 357
297 295 293 291 290 288 286 285 283 281/
835 832 827 819 808 794 777 757 734 709 682 653 622 590 556 521 485 449 412 375
304 302 300 298 296 294 292 290 288 286/
939 936 930 920 906 888 867 843 816 786 753 718 681 642 602 561 518 476 433 390
310 308 306 303 301 299 297 294 292 290/
1031 1028 1021 1009 993 972 948 920 888 853 815 774 732 687 641 595 547 499 451 404
316 314 311 309 306 304 301 299 297 294/
1105 1101 1093 1080 1062 1039 1012 980 945 906 864 819 772 723 673 621 570 518 466 414
321 319 316 314 311 308 306 303 301 298/
1154 1150 1142 1128 1108 1084 1055 1021 983 941 896 849 799 747 694 640 585 530 476 422
326 323 321 318 315 313 310 307 305 302/
1175 1171 1162 1147 1128 1103 1073 1038 999 957 911 862 811 758 704 648 593 537 481 427
330 327 324 321 319 316 313 311 308 305/
1167 1163 1154 1140 1120 1096 1066 1032 994 952 907 859 808 756 702 648 593 537 482 428
332 329 327 324 321 319 316 314 311 308/
1129 1125 1117 1104 1085 1062 1034 1002 966 926 884 838 790 740 689 637 584 532 479 427
334 331 329 326 323 321 318 316 313 311/
1065 1062 1055 1043 1026 1005 980 951 918 882 843 802 758 712 666 617 569 520 471 422
334 332 329 327 325 322 320 317 315 313/
981 978 972 961 947 929 907 882 854 822 788 752 714 674 632 590 546 502 458 414
334 331 329 327 325 323 320 318 316 314/
882 880 875 866 854 839 822 801 777 751 723 693 661 627 592 555 518 480 442 403
332 330 328 326 324 322 320 318 317 315/
773 772 768 761 752 740 726 710 692 672 649 625 600 573 545 515 485 454 422 390
330 328 326 325 323 321 320 318 316 315/
662 661 658 653 647 638 628 617 603 588 572 554 535 515 494 471 448 424 400 375
326 325 323 322 321 319 318 317 315 314/
552 551 549 546 542 537 530 522 514 504 493 481 468 455 440 425 409 392 375 357
322 321 320 319 318 317 316 315 314 313/
448 447 446 445 442 440 436 432 427 422 416 409 402 394 386 378 368 359 349 338
317 316 316 315 314 314 313 313 312 311/
353 353 352 352 351 350 349 348 347 345 343 341 339 337 334 331 328 325 322 319
311 311 311 311 311 310 310 310 310 310/
'PRINT:(33008)','CALCULATE STATISTICS'/
'MODEL:(FUELCHL7)'/
'RADIAL:(3,0.00,20,.61214E-02,2,.61214E-02,10,.65405E-02)',
'AXIAL:(5.9436,21)-EQUAL-SEGMENT', 'SECTOR:(1,1)',
'CYLINDER:(1,1924)',

'HEATED LENGTH:(5.770485)'/
'BOUNDARY CONDITIONS:(0,1)'/
'OUTSIDE HYDRAULIC:(ZONE7)'/
'37-ROD-1', 'HT-CRIT-(2*0,2*2,2*2)','HT-CORR-DEFAULT',,,
'WALL-INTERFACE-HEAT-TRANSFER:(6*5,1)','CORRECTION FACTOR:(,,,,,,,0.97,)'/
'UO2'/
'GAP:(10000.,0.00,0.00)'/ GAP CONDUCTANCE, conservatively using 37-element bundle
'ZIRCALOY'/ SHEATH
'HQ-TIME:(264560000,RPOWER7)'/
'R-UNIFORM','S-UNIFORM','A-USER','C-UNIFORM'/
0.0056,0.0166,0.0273,0.0374,0.0466,0.0548,0.0617,0.0673,0.0714,0.0739,0.0747,0.0739,
0.0714,0.0673,0.0617,0.0548,0.0466,0.0374,0.0273,0.0166,0.0056/ Axial power distribution
'HQ-NIL'/ GAP
'HQ-NIL'/ SHEATH
'TEMP-4D'/
308 308 308 307 306 306 305 304 302 301 299 297 295 293 290 288 285 282 279 276
269 269 268 268 268 268 268 267 267 267/
399 398 397 396 394 391 388 384 379 374 369 363 356 349 341 333 325 316 306 296
275 274 274 273 272 272 271 271 270 269/
500 499 497 495 491 486 479 472 464 455 445 434 422 409 395 381 366 350 334 318
282 281 280 279 278 277 276 275 274 273/
609 607 605 600 594 586 577 566 553 539 524 507 489 470 450 429 407 385 362 338
290 288 287 286 284 283 281 280 279 277/
719 718 714 708 699 688 675 660 643 623 602 580 556 530 503 475 447 417 387 357
297 295 293 291 290 288 286 285 283 281/
830 828 823 815 804 790 773 753 731 706 679 650 620 588 554 519 484 448 411 374
303 301 299 297 295 293 291 290 288 286/
933 931 925 915 901 884 863 839 812 782 749 715 678 639 600 559 517 475 432 390
310 308 305 303 301 299 296 294 292 290/
1025 1022 1015 1003 987 967 943 915 883 848 811 771 728 684 639 592 545 498 450 403
316 313 311 308 306 304 301 299 296 294/
1098 1095 1087 1074 1056 1033 1006 975 939 901 859 815 768 720 670 619 568 516 465 413
321 319 316 313 311 308 306 303 301 298/
1147 1143 1135 1121 1101 1077 1048 1015 977 936 892 845 795 744 691 637 583 529 475 421
326 323 320 318 315 312 310 307 304 302/
1167 1163 1155 1140 1121 1096 1066 1032 993 951 906 858 807 754 701 646 590 535 480 426
329 326 324 321 318 316 313 310 308 305/
1159 1156 1147 1133 1113 1089 1060 1026 988 947 902 854 804 753 699 645 590 536 481 427
332 329 326 324 321 319 316 313 311 308/
1122 1119 1110 1097 1079 1056 1028 996 961 921 879 834 786 737 686 635 582 530 478 426
333 331 328 326 323 321 318 316 313 311/
1059 1056 1048 1037 1020 999 974 946 913 878 839 798 755 709 663 615 567 518 469 421

334 331 329 327 324 322 319 317 315 312/
975 972 966 956 942 924 902 877 849 818 785 749 711 671 630 588 545 501 457 413
333 331 329 327 325 322 320 318 316 314/
877 875 870 862 850 835 818 797 774 748 720 690 658 625 590 554 517 479 441 403
332 330 328 326 324 322 320 318 316 314/
770 768 764 757 748 737 723 707 689 669 647 623 598 571 543 514 484 453 421 390
329 328 326 324 323 321 319 318 316 314/
659 658 655 651 644 636 626 614 601 586 570 552 534 513 492 470 447 424 399 374
326 325 323 322 320 319 318 317 315 314/
550 550 548 545 540 535 528 521 512 502 492 480 467 454 439 424 408 392 375 357
322 321 320 319 318 317 316 315 314 313/
447 446 445 444 441 439 435 431 426 421 415 408 401 394 386 377 368 358 348 338
316 316 315 315 314 313 313 312 312 311/
352 352 352 351 351 350 349 348 346 345 343 341 339 336 334 331 328 325 322 318
311 311 311 311 310 310 310 310 310 309/
'PRINT:(33008)','CALCULATE STATISTICS'/
'END'/ of heat transfer package
'INITIAL CONDITIONS'/
'INBC','L-P0'/
9120/
'R-P0','V1'/
9120/
'V1','L-P1'/
4090.9090/
'V1','L-P2'/
5029.0910/
'R-P1','V2'/
4090.9090/
'V2','L-P3'/
2448.1285/
'V2','L-Z3'/
1642.7804/
'R-Z3','L-ZONE3'/
1642.7804/
'R-P2','V3'/
5029.0910/
'V3','L-P4'/
2562.7517/
'V3','L-P5'/
2466.3393/
'R-P3','V4'/
2448.1285/

'V4','L-Z1'/
1223.8985/
'V4','L-Z2'/
1224.2301/
'R-Z1','L-ZONE1'/
1223.8985/
'R-Z2','L-ZONE2'/
1224.2300/
'R-P4','V5'/
2562.7516/
'V5','L-Z4'/
1104.4797/
'V5','L-Z5'/
1458.2719/
'R-Z4','L-ZONE4'/
1104.4797/
'R-Z5','L-ZONE5'/
1458.2719/
'R-P5','V6'/
2466.3393/
'V6','L-Z6'/
1233.0314/
'V6','L-Z7'/
1233.3079/
'R-Z6','L-ZONE6'/
1233.0314/
'R-Z7','L-ZONE7'/
1233.3079/
'P0', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.600646E+06, 1.118E+06, 265, .00000E+00, 8.1355, 8.1355/
'P1', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.556869E+06, 1.118E+06, 265, .00000E+00, 8.3545, 8.3545/
'P2', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.558240E+06, 1.118E+06, 265, .00000E+00, 7.9668, 7.9668/
'P3', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.512847E+06, 1.118E+06, 265, .00000E+00, 7.9807, 7.9807/
'P4', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.517243E+06, 1.118E+06, 265, .00000E+00, 7.8986, 7.8986/
'P5', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.516754E+06, 1.118E+06, 265, .00000E+00, 8.0400, 8.0400/
'V1', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.571986E+06, 1.118E+06, 265, .00000E+00, 9120/

'V2', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.526644E+06, 1.118E+06, 265, .00000E+00, 4090.9090/
'V3', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.530757E+06, 1.118E+06, 265, .00000E+00, 5029.0910/
'V4', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.485266E+06, 1.118E+06, 265, .00000E+00, 2448.1285/
'V5', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.490226E+06, 1.118E+06, 265, .00000E+00, 2562.7516/
'V6', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.488761E+06, 1.118E+06, 265, .00000E+00, 2466.3393/
'Z1', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.471466E+06, 1.118E+06, 265, .00000E+00, 7.9802, 7.9802/
'Z2', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.471459E+06, 1.118E+06, 265, .00000E+00, 7.9823, 7.9823/
'Z3', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.509159E+06, 1.118E+06, 265, .00000E+00, 8.9832, 8.9832/
'Z4', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.477035E+06, 1.118E+06, 265, .00000E+00, 7.8016, 7.8016/
'Z5', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.476447E+06, 1.118E+06, 265, .00000E+00, 7.9747, 7.9747/
'Z6', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.474755E+06, 1.118E+06, 265, .00000E+00, 8.0397, 8.0397/
'Z7', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.474748E+06, 1.118E+06, 265, .00000E+00, 8.0415, 8.0415/
'ZONE1','BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.464067E+06, 1.119E+06, 265, .00000E+00, 7.9848, 7.9848/
10.449291E+06, 1.123E+06, 266, .00000E+00, 7.9985, 7.9985/
10.434477E+06, 1.129E+06, 267, .00000E+00, 8.0212, 8.0212/
10.419614E+06, 1.137E+06, 269, .00000E+00, 8.0526, 8.0526/
10.404692E+06, 1.147E+06, 271, .00000E+00, 8.0925, 8.0925/
10.389700E+06, 1.160E+06, 274, .00000E+00, 8.1403, 8.1403/
10.374629E+06, 1.173E+06, 277, .00000E+00, 8.1957, 8.1957/
10.359470E+06, 1.188E+06, 280, .00000E+00, 8.2578, 8.2578/
10.344215E+06, 1.204E+06, 283, .00000E+00, 8.3259, 8.3259/
10.328855E+06, 1.221E+06, 286, .00000E+00, 8.3989, 8.3989/
10.313387E+06, 1.237E+06, 289, .00000E+00, 8.4755, 8.4755/
10.297806E+06, 1.254E+06, 293, .00000E+00, 8.5542, 8.5542/
10.282112E+06, 1.270E+06, 296, .00000E+00, 8.6330, 8.6330/
10.266308E+06, 1.285E+06, 298, .00000E+00, 8.7102, 8.7102/
10.250399E+06, 1.299E+06, 301, .00000E+00, 8.7835, 8.7835/
10.234396E+06, 1.310E+06, 303, .00000E+00, 8.8509, 8.8509/
10.218310E+06, 1.321E+06, 305, .00000E+00, 8.9100, 8.9100/

10.202161E+06, 1.329E+06, 307, .00000E+00, 8.9588, 8.9588/
10.185967E+06, 1.336E+06, 308, .00000E+00, 8.9952, 8.9952/
10.169752E+06, 1.339E+06, 308, .00000E+00, 9.0178, 9.0178/
10.153540E+06, 1.340E+06, 308, .00000E+00, 9.0258, 9.0258/
'ZONE2','BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.464056E+06, 1.119E+06, 265, .00000E+00, 7.9870, 7.9870/
10.449273E+06, 1.123E+06, 266, .00000E+00, 8.0006, 8.0006/
10.434452E+06, 1.129E+06, 267, .00000E+00, 8.0231, 8.0231/
10.419582E+06, 1.137E+06, 269, .00000E+00, 8.0543, 8.0543/
10.404654E+06, 1.147E+06, 271, .00000E+00, 8.0939, 8.0939/
10.389656E+06, 1.159E+06, 274, .00000E+00, 8.1414, 8.1414/
10.374580E+06, 1.173E+06, 276, .00000E+00, 8.1963, 8.1963/
10.359417E+06, 1.188E+06, 279, .00000E+00, 8.2580, 8.2580/
10.344158E+06, 1.203E+06, 283, .00000E+00, 8.3256, 8.3256/
10.328795E+06, 1.220E+06, 286, .00000E+00, 8.3981, 8.3981/
10.313325E+06, 1.236E+06, 289, .00000E+00, 8.4740, 8.4740/
10.297743E+06, 1.253E+06, 292, .00000E+00, 8.5520, 8.5520/
10.282049E+06, 1.268E+06, 295, .00000E+00, 8.6302, 8.6302/
10.266246E+06, 1.283E+06, 298, .00000E+00, 8.7067, 8.7067/
10.250340E+06, 1.297E+06, 301, .00000E+00, 8.7793, 8.7793/
10.234340E+06, 1.309E+06, 303, .00000E+00, 8.8460, 8.8460/
10.218259E+06, 1.319E+06, 305, .00000E+00, 8.9045, 8.9045/
10.202115E+06, 1.327E+06, 306, .00000E+00, 8.9528, 8.9528/
10.185927E+06, 1.333E+06, 307, .00000E+00, 8.9888, 8.9888/
10.169718E+06, 1.337E+06, 308, .00000E+00, 9.0112, 9.0112/
10.153512E+06, 1.338E+06, 308, .00000E+00, 9.0191, 9.0191/
'ZONE3','BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.500004E+06, 1.119E+06, 265, .00000E+00, 8.9882, 8.9882/
10.481718E+06, 1.122E+06, 266, .00000E+00, 9.0030, 9.0030/
10.463385E+06, 1.128E+06, 267, .00000E+00, 9.0275, 9.0275/
10.444993E+06, 1.136E+06, 269, .00000E+00, 9.0613, 9.0613/
10.426530E+06, 1.146E+06, 271, .00000E+00, 9.1041, 9.1041/
10.407985E+06, 1.158E+06, 273, .00000E+00, 9.1555, 9.1555/
10.389345E+06, 1.171E+06, 276, .00000E+00, 9.2148, 9.2148/
10.370602E+06, 1.185E+06, 279, .00000E+00, 9.2814, 9.2814/
10.351745E+06, 1.200E+06, 282, .00000E+00, 9.3542, 9.3542/
10.332766E+06, 1.216E+06, 285, .00000E+00, 9.4321, 9.4321/
10.313659E+06, 1.232E+06, 288, .00000E+00, 9.5137, 9.5137/
10.294421E+06, 1.248E+06, 291, .00000E+00, 9.5973, 9.5973/
10.275052E+06, 1.263E+06, 294, .00000E+00, 9.6811, 9.6811/
10.255555E+06, 1.277E+06, 297, .00000E+00, 9.7628, 9.7628/
10.235938E+06, 1.291E+06, 299, .00000E+00, 9.8404, 9.8404/

10.216213E+06, 1.302E+06, 302, .00000E+00, 9.9115, 9.9115/
10.196395E+06, 1.312E+06, 303, .00000E+00, 9.9738, 9.9738/
10.176503E+06, 1.320E+06, 305, .00000E+00, 10.0251, 10.0251/
10.159563E+06, 1.326E+06, 306, .00000E+00, 10.0634, 10.0634/
10.136599E+06, 1.329E+06, 306, .00000E+00, 10.0873, 10.0873/
10.116640E+06, 1.331E+06, 307, .00000E+00, 10.0958, 10.0958/
'ZONE4','BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.469929E+06, 1.119E+06, 265, .00000E+00, 7.8065, 7.8065/
10.455762E+06, 1.124E+06, 266, .00000E+00, 7.8223, 7.8223/
10.441533E+06, 1.131E+06, 268, .00000E+00, 7.8485, 7.8485/
10.427248E+06, 1.141E+06, 270, .00000E+00, 7.8849, 7.8849/
10.412896E+06, 1.153E+06, 272, .00000E+00, 7.9312, 7.9312/
10.398464E+06, 1.167E+06, 275, .00000E+00, 7.9871, 7.9871/
10.383940E+06, 1.183E+06, 279, .00000E+00, 8.0520, 8.0520/
10.369314E+06, 1.201E+06, 282, .00000E+00, 8.1254, 8.1254/
10.354573E+06, 1.220E+06, 286, .00000E+00, 8.2064, 8.2064/
10.339709E+06, 1.239E+06, 290, .00000E+00, 8.2938, 8.2938/
10.324712E+06, 1.259E+06, 294, .00000E+00, 8.3861, 8.3861/
10.309579E+06, 1.278E+06, 297, .00000E+00, 8.4817, 8.4817/
10.294306E+06, 1.297E+06, 301, .00000E+00, 8.5785, 8.5785/
10.278894E+06, 1.315E+06, 304, .00000E+00, 8.6740, 8.6740/
10.263351E+06, 1.331E+06, 307, .00000E+00, 8.7657, 8.7657/
10.247685E+06, 1.345E+06, 309, .00000E+00, 9.3398, 8.8507/
10.231985E+06, 2.525E+06, 311, .01198E+00, 9.5670, 9.0164/
10.215744E+06, 2.525E+06, 313, .03100E+00, 9.7855, 9.2275/
10.199223E+06, 2.526E+06, 313, .07205E+00, 10.1871, 9.6138/
10.181687E+06, 2.526E+06, 313, .11929E+00, 10.6534, 10.0678/
10.163305E+06, 2.526E+06, 312, .15333E+00, 10.9313, 10.4112/
'ZONE5','BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.469062E+06, 1.119E+06, 265, .00000E+00, 7.9802, 7.9802/
10.454300E+06, 1.123E+06, 266, .00000E+00, 7.9952, 7.9952/
10.439498E+06, 1.130E+06, 268, .00000E+00, 8.0200, 8.0200/
10.424643E+06, 1.139E+06, 269, .00000E+00, 8.0546, 8.0546/
10.409722E+06, 1.150E+06, 272, .00000E+00, 8.0984, 8.0984/
10.394725E+06, 1.164E+06, 275, .00000E+00, 8.1513, 8.1513/
10.379639E+06, 1.179E+06, 278, .00000E+00, 8.2125, 8.2125/
10.364456E+06, 1.195E+06, 281, .00000E+00, 8.2815, 8.2815/
10.349164E+06, 1.213E+06, 284, .00000E+00, 8.3574, 8.3574/
10.333755E+06, 1.231E+06, 288, .00000E+00, 8.4391, 8.4391/
10.318222E+06, 1.249E+06, 292, .00000E+00, 8.5251, 8.5251/
10.302561E+06, 1.267E+06, 295, .00000E+00, 8.6138, 8.6138/
10.286770E+06, 1.285E+06, 298, .00000E+00, 8.7032, 8.7032/

10.270851E+06, 1.301E+06, 301, .00000E+00, 8.7911, 8.7911/
10.254811E+06, 1.316E+06, 304, .00000E+00, 8.8750, 8.8750/
10.238659E+06, 1.330E+06, 307, .00000E+00, 8.9525, 8.9525/
10.222411E+06, 1.341E+06, 309, .00000E+00, 9.0208, 9.0208/
10.206087E+06, 1.350E+06, 310, .00000E+00, 9.4878, 9.0773/
10.189696E+06, 2.526E+06, 311, .00355E+00, 9.6475, 9.1470/
10.173143E+06, 2.526E+06, 312, .00598E+00, 9.7378, 9.1922/
10.156601E+06, 2.526E+06, 312, .00852E+00, 9.7340, 9.2213/
'ZONE6','BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.467256E+06, 1.119E+06, 265, .00000E+00, 8.0443, 8.0443/
10.452281E+06, 1.123E+06, 266, .00000E+00, 8.0580, 8.0580/
10.437268E+06, 1.129E+06, 267, .00000E+00, 8.0807, 8.0807/
10.422206E+06, 1.137E+06, 269, .00000E+00, 8.1121, 8.1121/
10.407083E+06, 1.147E+06, 271, .00000E+00, 8.1519, 8.1519/
10.391891E+06, 1.159E+06, 274, .00000E+00, 8.1997, 8.1997/
10.376620E+06, 1.173E+06, 276, .00000E+00, 8.2549, 8.2549/
10.361260E+06, 1.188E+06, 279, .00000E+00, 8.3170, 8.3170/
10.345803E+06, 1.204E+06, 283, .00000E+00, 8.3849, 8.3849/
10.330242E+06, 1.220E+06, 286, .00000E+00, 8.4578, 8.4578/
10.314572E+06, 1.236E+06, 289, .00000E+00, 8.5341, 8.5341/
10.298789E+06, 1.253E+06, 292, .00000E+00, 8.6125, 8.6125/
10.282893E+06, 1.269E+06, 295, .00000E+00, 8.6912, 8.6912/
10.266886E+06, 1.283E+06, 298, .00000E+00, 8.7680, 8.7680/
10.250775E+06, 1.297E+06, 301, .00000E+00, 8.8411, 8.8411/
10.234569E+06, 1.309E+06, 303, .00000E+00, 8.9081, 8.9081/
10.218282E+06, 1.319E+06, 305, .00000E+00, 8.9669, 8.9669/
10.201930E+06, 1.328E+06, 306, .00000E+00, 9.0154, 9.0154/
10.185535E+06, 1.334E+06, 307, .00000E+00, 9.0517, 9.0517/
10.169118E+06, 1.337E+06, 308, .00000E+00, 9.0742, 9.0742/
10.152704E+06, 1.339E+06, 308, .00000E+00, 9.0821, 9.0821/
'ZONE7','BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.467247E+06, 1.119E+06, 265, .00000E+00, 8.0461, 8.0461/
10.452266E+06, 1.123E+06, 266, .00000E+00, 8.0597, 8.0597/
10.437247E+06, 1.129E+06, 267, .00000E+00, 8.0823, 8.0823/
10.422179E+06, 1.137E+06, 269, .00000E+00, 8.1135, 8.1135/
10.407051E+06, 1.147E+06, 271, .00000E+00, 8.1530, 8.1530/
10.391855E+06, 1.159E+06, 274, .00000E+00, 8.2006, 8.2006/
10.376579E+06, 1.173E+06, 276, .00000E+00, 8.2555, 8.2555/
10.361215E+06, 1.187E+06, 279, .00000E+00, 8.3171, 8.3171/
10.345755E+06, 1.203E+06, 283, .00000E+00, 8.3847, 8.3847/
10.330192E+06, 1.219E+06, 286, .00000E+00, 8.4571, 8.4571/
10.314520E+06, 1.236E+06, 289, .00000E+00, 8.5329, 8.5329/

10.298736E+06, 1.252E+06, 292, .00000E+00, 8.6107, 8.6107/
10.282840E+06, 1.268E+06, 295, .00000E+00, 8.6888, 8.6888/
10.266835E+06, 1.282E+06, 298, .00000E+00, 8.7651, 8.7651/
10.250726E+06, 1.296E+06, 300, .00000E+00, 8.8375, 8.8375/
10.234523E+06, 1.308E+06, 303, .00000E+00, 8.9040, 8.9040/
10.218239E+06, 1.318E+06, 305, .00000E+00, 8.9623, 8.9623/
10.201892E+06, 1.327E+06, 306, .00000E+00, 9.0104, 9.0104/
10.185501E+06, 1.333E+06, 307, .00000E+00, 9.0463, 9.0463/
10.169089E+06, 1.336E+06, 308, .00000E+00, 9.0687, 9.0687/
10.152680E+06, 1.337E+06, 308, .00000E+00, 9.0765, 9.0765/
'N1', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.145426E+06, 1.340E+06, 307, .00000E+00, 9.0256, 9.0256/
'N2', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.145401E+06, 1.339E+06, 308, .00000E+00, 9.0197, 9.0197/
'N3', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.106654E+06, 1.331E+06, 307, .00000E+00, 10.0998, 10.0998/
'N4', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.154589E+06, 2.526E+06, 312, .16830E+00, 10.6411, 10.5778/
'N5', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.148292E+06, 2.526E+06, 312, .00992E+00, 9.2865, 9.2328/
'N6', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.144489E+06, 1.339E+06, 308, .00000E+00, 9.0821, 9.0821/
'N7', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.144468E+06, 1.337E+06, 308, .00000E+00, 9.0772, 9.0772/
'W1', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.016686E+06, 2.528E+06, 309, .002765E+00, 9120.0391/
'W2', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.067423E+06, 1.336E+06, 308, .00000E+00, 4090.9122/
'W3', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.066126E+06, 2.527E+06, 310, .04875E+00, 5029.1249/
'W4', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.114225E+06, 1.340E+06, 308, .00000E+00, 2448.1312/
'W5', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.117391E+06, 2.526E+06, 312, .08480E+00, 2562.7811/
'W6', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.112862E+06, 1.338E+06, 308, .00000E+00, 2466.3420/
'M0', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.000006E+06, 2.529E+06, 310, .02765E+00, 9.5140, 9.4830/
'M1', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.050371E+06, 1.338E+06, 308, .00000E+00, 9.4775, 9.4373/
'M2', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.049745E+06, 2.528E+06, 310, .04881E+00, 9.5238, 9.4859/

'M3', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.098624E+06, 1.339E+06, 308, .00000E+00, 9.0209, 9.0209/
'M4', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.100619E+06, 2.527E+06, 312, .09083E+00, 9.9140, 9.8682/
'M5', 'BY-NODE','HG-BY-SAT','HF-BY-TEMP'/
10.097052E+06, 1.340E+06, 308, .00000E+00, 9.1360, 9.0908/
'R-M1','W1'/
4090.9123/
'R-M2','W1'/
5029.1269/
'W1','L-M0'/
9120.0391/
'R-ZONE3','L-N3'/
1642.7809/
'R-M3','W2'/
2448.1313/
'R-N3','W2'/
1642.7809/
'W2','L-M1'/
4090.9122/
'R-M4','W3'/
2562.7828/
'R-M5','W3'/
2466.3421/
'W3','L-M2'/
5029.1249/
'R-ZONE1','L-N1'/
1223.8998/
'R-ZONE2','L-N2'/
1224.2313/
'R-N1','W4'/
1223.8998/
'R-N2','W4'/
1224.2314/
'W4','L-M3'/
2448.1312/
'R-ZONE4','L-N4'/
1104.4395/
'R-ZONE5','L-N5'/
1458.3400/
'R-N4','W5'/
1104.4408/

```
'R-N5','W5'/
1458.3403/
'W5','L-M4'/
2562.7811/
'R-ZONE6','L-N6'/
1233.0327/
'R-ZONE7','L-N7'/
1233.3092/
'R-N6','W6'/
1233.0328/
'R-N7','W6'/
1233.3092/
'W6','L-M5'/
2466.3420/
'R-M0','OUTBC'/
9120.0412/
'END'/  of INITIAL CONDITIONS
```

APPENDIX B

Altera Stratix FPGA Platform
&
National Instruments PXI-7811R FPGA Platform

Two FPGA platforms have been utilized in the current work for platform diversity. The Altera Stratix FPGA platform is used to implement the "SG low level" trip logic and evaluate the system response time. The National Instruments PXI-7811R FPGA platform, with neutron overpower trip logic implemented, is connected to the HIL simulation environment to verify the safety margin improvement in a large LOCA case.

Altera Stratix FPGA Platform

The Altera Stratix FPGA platform is originally designed as an embedded system development board. It features an onboard Stratix EP1S40F780C5 FPGA chip with supporting I/O ports, interacting switches, and LED displays. The layout of all the components on the development board is shown in Figure B.1. A block diagram showing the interaction between the Stratix FPGA chip and other onboard components is presented in Figure B.2. Detailed features of the Stratix FPGA chip are listed in Table B.1 below.

The configuration of the onboard Stratix FPGA is through an EDA tool from Altera called Quartus II running on a host computer. Quartus II is capable of hardware coding, function simulation, and onboard signal monitoring. The synthesized design is also compiled and downloaded to the Stratix FPGA by Quartus II through a data cable connecting the board and the host computer.

Table B.1 Stratix FPGA features

Logic Elements	41,250
M512 RAM blocks (32 x 18 bits)	384
M4K RAM blocks (128 x 36 bits)	183
M-RAM blocks (4K x 144 bits)	4
Total RAM bits	3,423,744
DSP blocks	14
Embedded multipliers	112
PLLs	12
Maximum user I/O pins	822

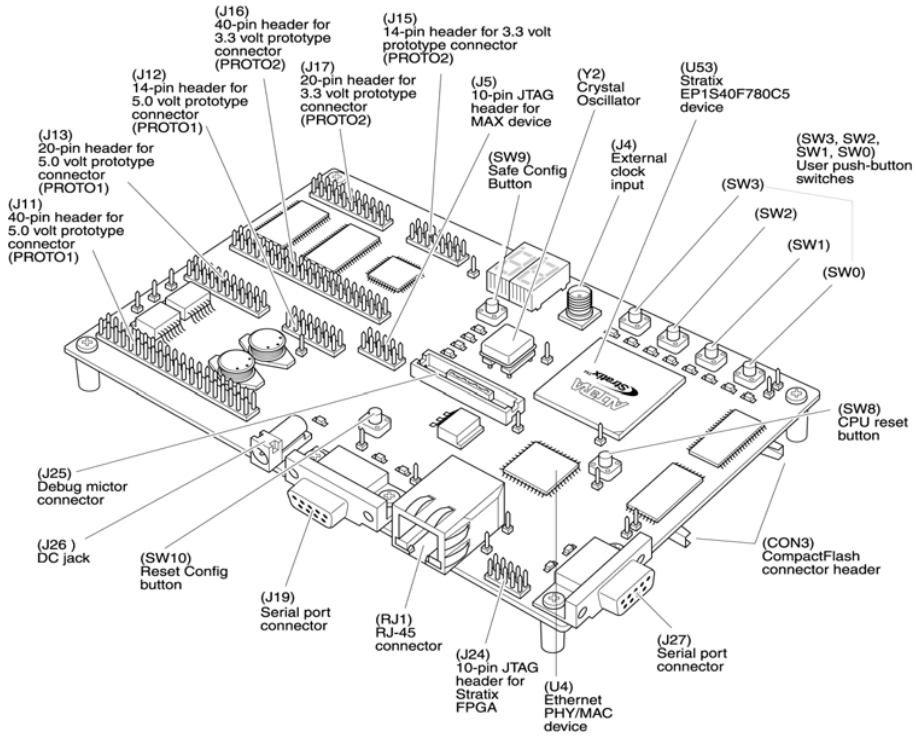

Figure B.1 – Component layout of the Stratix FPGA development board

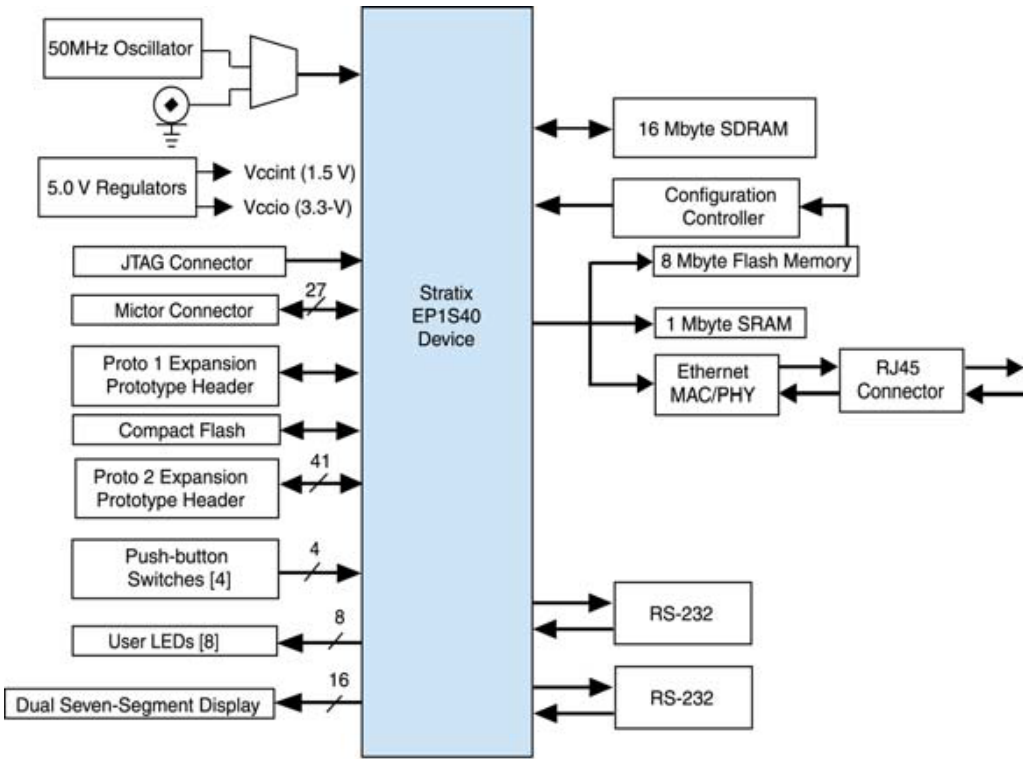

Figure B.2 – Block diagram of Stratix FPGA development board

The input and output signals are directed to the onboard prototype connectors as illustrated in Figure B.1. More specifically, J11 and J16 are used to take the four incoming 12-bit SG level signals while J15 is responsible for pass the trip signal issued by FPGA to the simulation environment.

The schematic overview of the implemented “SG low level” logic is shown in Figure B.3.

Although the Stratix FPGA board is capable of realizing the “SG low level” trip logic, its insufficient I/O pins limit the application for systems that have more I/O request. Therefore, to explore FPGA application for CANDU SDS1 with more I/O requests, the National Instruments PXI-based FPGA platform is applied for the investigation of FPGA performance in the HIL simulation environment.

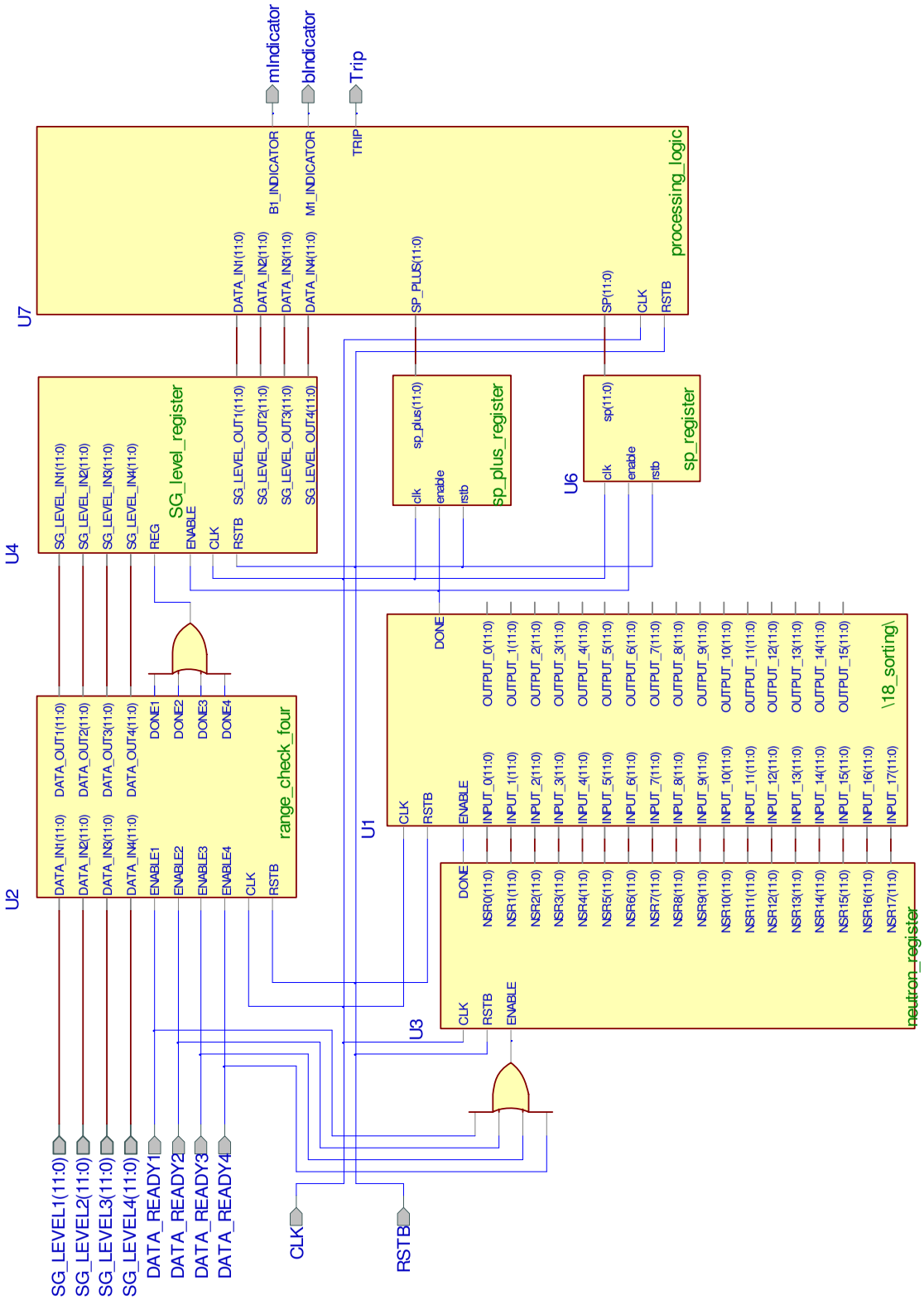

Figure B.3 – Schematic overview of the FPGA-based "SG low level" trip logic

VHDL source code for the top-level design shown in Figure B.3

```
----------------------------------------------------------------------------------------------------
--
-- Title       : SDS1 Steam Generator Low Level  Trip Logic
-- Design      : SDS1_SG_LL_trip
-- Author      : Jingke She
-- Company     : UWO
--
-- Design unit header --------------------------------------------------------------------------

library IEEE;
use IEEE.std_logic_1164.all;

entity SG_LL_TRIP is
  port(
      CLK : in STD_LOGIC;
      DATA_READY1 : in STD_LOGIC;
      DATA_READY2 : in STD_LOGIC;
      DATA_READY3 : in STD_LOGIC;
      DATA_READY4 : in STD_LOGIC;
      RSTB : in STD_LOGIC;
      SG_LEVEL1 : in STD_LOGIC_VECTOR(11 downto 0);
      SG_LEVEL2 : in STD_LOGIC_VECTOR(11 downto 0);
      SG_LEVEL3 : in STD_LOGIC_VECTOR(11 downto 0);
      SG_LEVEL4 : in STD_LOGIC_VECTOR(11 downto 0);
      Trip : out STD_LOGIC;
      bIndicator : out STD_LOGIC;
      mIndicator : out STD_LOGIC
  );
end SG_LL_TRIP;

architecture structure of SG_LL_TRIP is
---- Component declarations -----
component neutron_register
  port (
      CLK : in STD_LOGIC;
      ENABLE : in STD_LOGIC;
      RSTB : in STD_LOGIC;
      DONE : out STD_LOGIC;
      NSR0 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR1 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR10 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR11 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR12 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR13 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR14 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR15 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR16 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR17 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR2 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR3 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR4 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR5 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR6 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR7 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR8 : out STD_LOGIC_VECTOR(11 downto 0);
      NSR9 : out STD_LOGIC_VECTOR(11 downto 0)
  );
end component;
component processing_logic
```

```
  port (
      CLK : in STD_LOGIC;
      DATA_IN1 : in STD_LOGIC_VECTOR(11 downto 0);
      DATA_IN2 : in STD_LOGIC_VECTOR(11 downto 0);
      DATA_IN3 : in STD_LOGIC_VECTOR(11 downto 0);
      DATA_IN4 : in STD_LOGIC_VECTOR(11 downto 0);
      RSTB : in STD_LOGIC;
      SP : in STD_LOGIC_VECTOR(11 downto 0);
      SP_PLUS : in STD_LOGIC_VECTOR(11 downto 0);
      B1_INDICATOR : out STD_LOGIC;
      M1_INDICATOR : out STD_LOGIC;
      TRIP : out STD_LOGIC
  );
end component;
component range_check_four
  port (
      CLK : in STD_LOGIC;
      DATA_IN1 : in STD_LOGIC_VECTOR(11 downto 0);
      DATA_IN2 : in STD_LOGIC_VECTOR(11 downto 0);
      DATA_IN3 : in STD_LOGIC_VECTOR(11 downto 0);
      DATA_IN4 : in STD_LOGIC_VECTOR(11 downto 0);
      ENABLE1 : in STD_LOGIC;
      ENABLE2 : in STD_LOGIC;
      ENABLE3 : in STD_LOGIC;
      ENABLE4 : in STD_LOGIC;
      RSTB : in STD_LOGIC;
      DATA_OUT1 : out STD_LOGIC_VECTOR(11 downto 0);
      DATA_OUT2 : out STD_LOGIC_VECTOR(11 downto 0);
      DATA_OUT3 : out STD_LOGIC_VECTOR(11 downto 0);
      DATA_OUT4 : out STD_LOGIC_VECTOR(11 downto 0);
      DONE1 : out STD_LOGIC;
      DONE2 : out STD_LOGIC;
      DONE3 : out STD_LOGIC;
      DONE4 : out STD_LOGIC
  );
end component;
component SG_level_register
  port (
      CLK : in STD_LOGIC;
      ENABLE : in STD_LOGIC;
      REG : in STD_LOGIC;
      RSTB : in STD_LOGIC;
      SG_LEVEL_IN1 : in STD_LOGIC_VECTOR(11 downto 0);
      SG_LEVEL_IN2 : in STD_LOGIC_VECTOR(11 downto 0);
      SG_LEVEL_IN3 : in STD_LOGIC_VECTOR(11 downto 0);
      SG_LEVEL_IN4 : in STD_LOGIC_VECTOR(11 downto 0);
      SG_LEVEL_OUT1 : out STD_LOGIC_VECTOR(11 downto 0);
      SG_LEVEL_OUT2 : out STD_LOGIC_VECTOR(11 downto 0);
      SG_LEVEL_OUT3 : out STD_LOGIC_VECTOR(11 downto 0);
      SG_LEVEL_OUT4 : out STD_LOGIC_VECTOR(11 downto 0)
  );
end component;
component sp_plus_register
  port (
      clk : in STD_LOGIC;
      enable : in STD_LOGIC;
      rstb : in STD_LOGIC;
      sp_plus : out STD_LOGIC_VECTOR(11 downto 0)
  );
end component;
component sp_register
  port (
```

```
      clk : in STD_LOGIC;
      enable : in STD_LOGIC;
      rstb : in STD_LOGIC;
      sp : out STD_LOGIC_VECTOR(11 downto 0)
  );
end component;
component \18_sorting\
  port (
      CLK : in STD_LOGIC;
      ENABLE : in STD_LOGIC;
      INPUT_0 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_1 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_10 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_11 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_12 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_13 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_14 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_15 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_16 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_17 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_2 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_3 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_4 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_5 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_6 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_7 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_8 : in STD_LOGIC_VECTOR(11 downto 0);
      INPUT_9 : in STD_LOGIC_VECTOR(11 downto 0);
      RSTB : in STD_LOGIC;
      DONE : out STD_LOGIC;
      OUTPUT_0 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_1 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_10 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_11 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_12 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_13 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_14 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_15 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_2 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_3 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_4 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_5 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_6 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_7 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_8 : out STD_LOGIC_VECTOR(11 downto 0);
      OUTPUT_9 : out STD_LOGIC_VECTOR(11 downto 0)
  );
end component;

---- Signal declarations used on the diagram ----
signal NET174 : STD_LOGIC;
signal NET2748 : STD_LOGIC;
signal NET2754 : STD_LOGIC;
signal NET2758 : STD_LOGIC;
signal NET2762 : STD_LOGIC;
signal NET3590 : STD_LOGIC;
signal NET4878 : STD_LOGIC;
signal NET4938 : STD_LOGIC;
signal BUS134 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS138 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS142 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS146 : STD_LOGIC_VECTOR (11 downto 0);
```

```
signal BUS150 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS154 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS158 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS162 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS166 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS170 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS178 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS182 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS186 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS190 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS194 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS198 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS202 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS206 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS210 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS214 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS218 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS222 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS226 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS230 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS234 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS238 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS242 : STD_LOGIC_VECTOR (11 downto 0);
signal BUS4820 : STD_LOGIC_VECTOR (11 downto 0);

begin
----  Component instantiations  ----
U1 : \18_sorting\
  port map(
      CLK => CLK,
      DONE => NET4878,
      ENABLE => NET174,
      INPUT_0 => BUS170,
      INPUT_1 => BUS178,
      INPUT_10 => BUS182,
      INPUT_11 => BUS186,
      INPUT_12 => BUS190,
      INPUT_13 => BUS194,
      INPUT_14 => BUS198,
      INPUT_15 => BUS202,
      INPUT_16 => BUS206,
      INPUT_17 => BUS210,
      INPUT_2 => BUS214,
      INPUT_3 => BUS218,
      INPUT_4 => BUS222,
      INPUT_5 => BUS226,
      INPUT_6 => BUS230,
      INPUT_7 => BUS234,
      INPUT_8 => BUS238,
      INPUT_9 => BUS242,
      RSTB => RSTB
  );
U2 : range_check_four
  port map(
      CLK => CLK,
      DATA_IN1 => SG_LEVEL1,
      DATA_IN2 => SG_LEVEL2,
      DATA_IN3 => SG_LEVEL3,
      DATA_IN4 => SG_LEVEL4,
      DATA_OUT1 => BUS4820,
      DATA_OUT2 => BUS134,
      DATA_OUT3 => BUS138,
```

```
      DATA_OUT4 => BUS142,
      DONE1 => NET2748,
      DONE2 => NET2762,
      DONE3 => NET2758,
      DONE4 => NET2754,
      ENABLE1 => DATA_READY1,
      ENABLE2 => DATA_READY2,
      ENABLE3 => DATA_READY3,
      ENABLE4 => DATA_READY4,
      RSTB => RSTB
  );
U3 : neutron_register
  port map(
      CLK => CLK,
      DONE => NET174,
      ENABLE => NET3590,
      NSR0 => BUS170,
      NSR1 => BUS178,
      NSR10 => BUS182,
      NSR11 => BUS186,
      NSR12 => BUS190,
      NSR13 => BUS194,
      NSR14 => BUS198,
      NSR15 => BUS202,
      NSR16 => BUS206,
      NSR17 => BUS210,
      NSR2 => BUS214,
      NSR3 => BUS218,
      NSR4 => BUS222,
      NSR5 => BUS226,
      NSR6 => BUS230,
      NSR7 => BUS234,
      NSR8 => BUS238,
      NSR9 => BUS242,
      RSTB => RSTB
  );
U4 : SG_level_register
  port map(
      CLK => CLK,
      ENABLE => NET4878,
      REG => NET4938,
      RSTB => RSTB,
      SG_LEVEL_IN1 => BUS4820,
      SG_LEVEL_IN2 => BUS134,
      SG_LEVEL_IN3 => BUS138,
      SG_LEVEL_IN4 => BUS142,
      SG_LEVEL_OUT1 => BUS146,
      SG_LEVEL_OUT2 => BUS150,
      SG_LEVEL_OUT3 => BUS154,
      SG_LEVEL_OUT4 => BUS158
  );
U5 : sp_plus_register
  port map(
      clk => CLK,
      enable => NET4878,
      rstb => RSTB,
      sp_plus => BUS162
  );
U6 : sp_register
  port map(
      clk => CLK,
      enable => NET4878,
```

```
      rstb => RSTB,
      sp => BUS166
  );
U7 : processing_logic
  port map(
      B1_INDICATOR => mIndicator,
      CLK => CLK,
      DATA_IN1 => BUS146,
      DATA_IN2 => BUS150,
      DATA_IN3 => BUS154,
      DATA_IN4 => BUS158,
      M1_INDICATOR => bIndicator,
      RSTB => RSTB,
      SP => BUS166,
      SP_PLUS => BUS162,
      TRIP => Trip
  );
NET4938 <= NET2754 or NET2758 or NET2762 or NET2748;

NET3590 <= DATA_READY4 or DATA_READY3 or DATA_READY2 or DATA_READY1;

end structure;
```

National Instruments PXI-7811R FPGA platform

The National Instruments PXI-7811R FPGA platform enables custom logic design with a Vertex-II FPGA chip and LabVIEW graphical development tools. It has expansion chassis that can be used to increase the analog inputs to as many as 64 ports, which is capable of implementing applications that require large number of I/O. The LabVIEW FPGA module is a powerful programming tool which enables both graphic development and VHDL coding for specific function blocks. These features make it possible to easily transfer other VHDL coded design to the LabVIEW development environment.

The entire platform, as introduced in Chapter 6, consists of the PXI-FPGA, the expansion chassis, and the I/O modules housed in the chassis. Detailed technical specifications of these devices are presented in Table B.2, Table B.3, and Table B.4.

Table B.2 NI 7811R FPGA features

FPGA Type	Virtex-II V1000
No. of flip-flops	10,240
No. of 4-input LUTs	10240
No. of 18 x 18 multipliers	40
Power requirement for +3.3V rail	500 mA
Power requirement for +5V rail	5 mA
Max clock rate	40 MHz
Bidirectional digital channels	160
Resolution	64 bits
Minimum input pulse width	12.5 ns
Embedded block RAM	720 Kb

Table B.3 NI 9151 expansion chassis features

No. of slots	4
Resolution	25 ns
Max sampling rate	40 MS/s

Table B.4 NI 9203 analog current input module features

Measurement type	Current
Signal conditioning	0-20 mA
Channels	8
Resolution	16 bits
Sample rate	200 KS/s
Maximum current range	-20 mA, 20 mA
Maximum current range accuracy	0.049 mA
Minimum current range	0 mA, 20 mA
Minimum current range accuracy	0.049 mA

APPENDIX C

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CURRICULUM VITAE

Name: Jingke She

Place of Birth: Huaihua, Hunan Province, China

Year of Birth: 1977

Post-secondary Education and Degrees:

Bachelor of Engineering
Tsinghua University
Beijing, China
1996 - 2000

Master of Applied Science
Memorial University of Newfoundland
St. John's, Newfoundland, Canada
2004 – 2006

Doctor of Philosophy
The University of Western Ontario
London, Ontario, Canada
2006-2012

Honors and Awards:

Scholarship of Excellence, 2nd grade
Tsinghua University, 1998

Best Overall Performance Award
Memorial University of Newfoundland, 2005

Publications:

1. Jingke She, "Power upgrading of nuclear power plant by improving shutdown system No.1 with FPGA technology", *31st Canadian Nuclear Society Annual Conference*, St. John, NB, Canada, 2007.

2. J. Drew Rankin, Jingke She, and Jin Jiang, "Evaluation of safety PLCs and FPGAs for shutdown systems in CANDU nuclear power plants", *International Symposium on Future I&C for Nuclear Power Plants*, Harbin, China, Sep. 8-10, 2008.

3. Jingke She and Jin Jiang, “FPGA application for CANDU shutdown system No.1”, *NPIC&HMIT 2009*, Knoxville, Tennessee, American Nuclear Society, 2009.

4. Jingke She and Jin Jiang, “On the speed of response of an FPGA-based shutdown system in CANDU nuclear power plants”, *Nuclear Engineering and Design*, Vol. 241, pp.2280-2287, 2011.

5. Jingke She and Jin Jiang, “Potential improvement of CANDU NPP safety margins by shortening the response time of shutdown systems using FPGA-based implementation”, *Nuclear Engineering and Design*, Vol. 244, pp. 43-51, 2012.