DC/DC Converter 3D Assembly for Autonomous Sensor Nodes

Thierry Hilt[(1)], Hervé Boutry[(1)], Rémi Franiatte[(1)], Frédéric Rothan[(1)], Nicolas Sillon[(1)]
Frank Stam[(2)], Alan Mathewson[(2)],Ningning Wang[(2)], Cian O'Mathuna[(2)] Kenneth Rodgers[(2)]
[(1)]CEA-LETI, MINATEC
17 rue des Martyrs, 38054 Grenoble, Cedex 9, France
[(2)]TYNDALL NATIONAL INSTITUTE
Prospect Row, Cork, Ireland

Abstract

This paper reports on the design and the manufacturing of an integrated DCDC converter, which respects the specificity of sensor node network: compactness, high efficiency in acquisition and transmission modes, and compatibility with miniature Lithium batteries.

A novel integrated circuit (ASIC) has been designed and manufactured to provide regulated Voltage to the sensor node from miniaturized, thin film Lithium batteries. Then, a 3D integration technique has been used to integrate this ASIC in a 3 layers stack with high efficiency passives components, mixing the wafer level technologies from two different research institutions.

Electrical results have demonstrated the feasibility of this integrated system and experiments have shown significant improvements in the case of oscillations in regulated voltage. However, stability of this output voltage toward the input voltage has still to be improved.

Introduction

Autonomous sensor node networks are promising approaches for monitoring specific data in various applications, such as automotive tire pressure monitoring, mechanical reliability in aeroplane bodies, and health monitoring. Further applications also arise in the prospective field of space exploration. These applications have all been studied in the European funded project e-CUBES. The main challenge for these sensor nodes lies in size and form factor reduction and both antenna and power supply are components which take up a considerable amount of the available space.

The power supply system

A sensor node power supply consists of an eventual energy scavenger that provides power from an external environment (i.e. vibration, shock) to a mean of storage (i.e. batteries, capacitor) from which a DC/DC converter provide regulated voltage to the sensor node.

Energy storage needs to have very small, dimensions and almost no self discharging. This leads us to renounce the regular rechargeable battery and capacitor solutions and choose specific thin film Lithium metal batteries with a 5x5mm² footprint. However, while this solution is very suitable for low consumption, it shows a non negligible internal resistance when relatively high current is needed. This has to be taken into account for this application.

Indeed, the main characteristic of such sensor node network is that the system is either on sleeping mode during mostly all the time, consuming very little power, or collecting data and transmitting them, requiring high current for a short period of time, and both in a optimized efficient way. This requires to develop a specific DC/DC converter, with a novel power management ASIC that can switch from a voltage conversion mean to another depending of the duty cycle.

The power management chip

The power management unit (PMU) must provide a stable 3.3 V output voltage to the load, independently from the input battery voltage and from the load current. Indeed, the battery voltage may vary over time as the battery is discharged. The maximum battery voltage is 5 V, but drops when it provides a high output current (up to 10 mA) due to its internal resistance. Hence, a voltage down-converter must be implemented in the power management unit.

The load current depends on the operating mode of the sensor node, which is operated with a low duty cycle to reduce the mean dissipated power. In standby mode, only a few blocks (real time clock, watchdogs, wake-up circuitry) must be powered. The typical required current in this phase is only 1 µA. In transmission mode, the RF module as well as the sensors and the data processing blocks are powered. During this second phase, the maximum required current is 10 mA..

There exist two main power supply topologies, based on two different principles: These are inductive switched mode power supplies (SMPS) and low drop-out linear regulators (LDO). Capacitive voltage regulators will not be presented here, because the output voltage regulation and output power of such regulators are not well suited to our application.

A switching converter contains a power input and control input ports, and a power output port. The raw input power (delivered by a battery or other power sources) is processed by the power filter as specified by the control input, as shown in Figure 1.

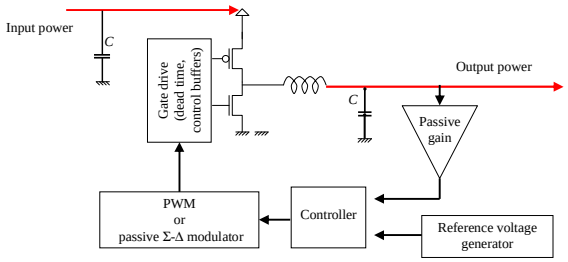

Figure 1 Standard step-down switching inductive DCDC converter schematic

A controller block provides a feedback between the output and the power filter, producing a well-regulated output. The

regulator loop compares the output voltage to a reference voltage, and adjusts the duty cycle of the control signal of the switches, so as to provide a constant output whatever the input voltage or the load current are. Duty cycle control can be performed with a Pulse Width Modulator (PWM) working at a constant frequency or a delta-sigma modulator (either active or passive).

A key component of this system is the power filter. It contains integrated CMOS devices (MOS and/or diodes) and passive components, such as inductors and capacitors either off chip or integrated on chip. This must be carefully designed in order to ensure high efficiency and small output ripple.

The efficiency of such a circuit is defined as $\eta = \frac{\text{Power at the output}}{\text{Power at the input}} = \frac{P_{out}}{P_{in}} = 1 - \frac{P_{loss}}{P_{in}}$ where P_{loss} is the power lost when transferring energy from the source to the inductor and from the inductor to the load. Power is mainly dissipated in two ways.

The first one is the Joule effect in the series resistances of the switches and the inductor. This power depends significantly on the load current, but it also depends on the current ripple. The root mean square (rms) current is high compared to the mean current when the ripple is large. In a first approximation, the current ripple is inversely proportional to the product $L*F_s$, where L is the inductance and F_s the switching frequency. It is all the more important becasue the inductance is low. Unfortunately, integrated passives can only provide low values for these two components.

The second source of power loss is the power dissipated in driving the MOS switches. Indeed, in order to reduce the Joule effect, the Ron of these transistors must be low (typically 1 Ohm or less). As a counterpart, they are very wide (the typical width lies between 1000 and 10000 times the gate length) and the gate capacitance is high (typically several pF). The switching power loss can be expressed as

$$P_{switch} = F_s * C_{gg} * V_{gg}^2$$

where F_s is the sampling frequency (10 to 20 MHz), C_{gg} is the total gate capacitance of all transistor switches and V_{gg} is the driving voltage.

For low output powers, the efficiency is poor because a lot of power is wasted in switching the transistors, whereas only a small amount of energy is delivered to the load. On the contrary, when the output current becomes high, the main sources of power loss are resistive losses. In theses conditions, the efficiency can reach 80 %..

In conclusion, low values of inductance must be compensated by increasing the switching frequency to avoid large voltage and current ripple. Nevertheless, the rms current can be high compared to the mean current provided to the load. This implies that the Joule effect dissipation is high. Moreover, high switching frequencies lead to more power dissipation in driving the switches.

A trade-off has to be found between the switching frenquency, the size of the MOS switches and the inductance in order to maximise the power efficiency.

On the other hand, low drop-out linear regulators (LDO) are small, easy to understand, and easy to design thanks to easy to follow design rules. A typical schematic of such a regulator is shown on Figure 2.

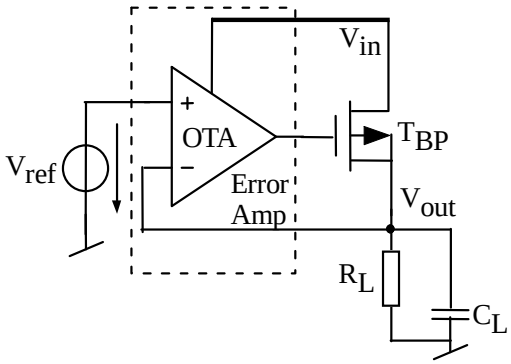

Figure 2 Typical Linear regulator schematic

The integrated area is dominated by the bypass transistor, by dropout voltage and rated load current. Unfortunately, the efficiency is poor (the maximum efficiency is $\eta = \frac{\text{Power at the output}}{\text{Power at the input}} = \frac{V_{out}}{V_{in}}$), unless it is operating near dropout.

In order to fullfill the requirements of the power management system, a dual mode PWM/LDO converter has been implemented. It features an inductive SMPS in parallel with a linear regulator (see Fig. 3). The SMPS is used in transmission mode, when the ouptut power demand is high, while the LDO is used in standby mode, when the output current is low. Each type of regulator is thus used in its best working range, providing a high global efficiency. An external control signal Enable_SMPS allows the user to switch from one mode to the other.

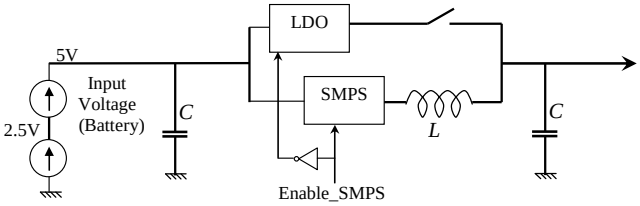

Figure 3 Dual mode converter schematic

Three external passive components are needed: an inductor and two capacitors at the input and the output. The input capacitor is used as a current buffer to reduce the spikes on the output current flowing from the battery in transmission mode.

Both regulators share the same low power voltage reference, based on a sub-bandgap circuit [1] with only 1 µA static consumption under 5 V.

The LDO error amplifier is biased in weak inversion to minimize power loss, and consumes only a few tens of nanowatts.

In order to enhance the SMPS efficiency, the input NMOS power transistor and the analog feedback controller are biased under 2.5 V only. Level shifters are then used to provide the correct levels to the PMOS switch of the power filter. This technique reduces the switch driving power by a factor of 4.

To further improve the efficiency, the SMPS makes use of an asynchronous passive delta-sigma modulator to generate the variable duty cycle clocks that drives the power filter [2]. This innovative Pulse Density Modulation (PDM) is used for its ease of implementation (2 RC filters as integrators and 3 inverters) and very low power consumption. Moreover, it does not need an additional oscillator. However, due to its working principle, this type of oscillator does not provide a fixed switching frequency. That results in a spread output noise spectrum. The mean switching frequency has been adjusted to 15 MHz in order to reduce the current ripple with an integrated inductance of 1 µH. In this case, the output capacitor can be as low as 100 nF to provide an output voltage ripple of less than 4 mV.

The characterisation results obtained from this system are summarised in next table.

CMOS technology	AMS 0.35 µm
Chip size (core)	1350 µm * 620 µm
Nominal inductance	1 µH to 4 µH
Nominal capacitance	100 nF
SMPS efficiency @ 10 mA output current – Fs = 15 Mhz	> 65 %
LDO efficiency @ 1 µA output current	66 %

The mean output voltage is higher than expected, because the reference voltage generated on chip is slightly higher than expected (830 mV instead of 800 mV).

Integrated Inductor

One of the main difficulties in the miniaturization of power conversion circuits is the reduction of the size of the energy storage and transfer devices, i.e. inductors and transformers, which are essential in the circuit but normally occupy a significant fraction of the volume of the power converters. The miniaturization of magnetic components is becoming increasing important when there is a space constraint for the circuit. A similar CMOS compatible process as in [3] has been used in this work to realize an integrated inductor on silicon substrate. **Figure 4** shows a typical cross-section of such type inductors.

Although the CMOS compatibility of the process allows monolithic solution for power converters, the fabricated inductor was firstly co-packaged and demonstrated electrically with the converter IC in this work. A detailed description of the technology used to fabricate the inductors has been given previously [3]. The essential details which are required in order to understand the design process are briefly described here. The substrate is a silicon wafer with a layer of insulation (SiO2, approximately 1µm thick). A seed layer of Ti/Cu is deposited by sputtering on the insulation. A layer of magnetic material (Ni45Fe55) is electroplated and patterned (layer 1) on top of the seed layer. This layer is further insulated by a patterned layer of BCB (layer 2). The Cu-windings are then deposited using electroplated copper on top of a Ti/Cu seed layer (layer 3). These windings are covered by a layer of SU8 (epoxy type photoresist) to isolate them from the top magnetic layer (layer 4). Finally, the top magnetic layer is electroplated (layer 5) to obtain a closed magnetic path.

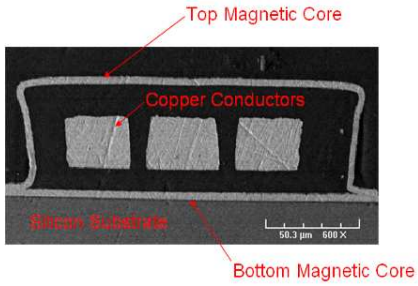

Figure 4 Cross section of a micro-fabricated inductor

The entire process consists of 5 mask layers. This racetrack inductor construction has been chosen over other inductor constructions (such as a toroïdal approach) because of its relatively simple construction, which requires just a single layer of conductors, thus avoiding the use of vias. The direction of flux travel in the device is in a single direction, perpendicular to the long axis of the core, which allows for the exploitation of anisotropy in the material, to reduce core losses. When electroplating all the magnetic layers, a magnetic field was applied to control the anisotropy direction of the NiFe films. The easy axis is induced parallel with the core long axis and the hard axis of the magnetic layers was aligned perpendicular to the racetrack shaped copper windings, so that during inductor operation the flux travel is along the hard axis. In the hard axis, magnetization takes place by domain rotation as opposed to domain growth, hence to minimize the core loss. The fabricated inductor was fully characterised and its inductance and DC resistance are 1.05µH, and 0.88Ohm, respectively.

3D integration

The components to be integrated to build the DC/DC converter are the energy management ASIC, two 100nF capacitors and one 1µH inductor. In order to use the smallest integrated device, we use NXP PICs Capacitors [4] and Tyndall's integrated inductor technology both chosen for their high density. Given the size of the chosen components, it appears that the size of the inductor is rather equal to the sum of the footprints of the other components and thus, a 3D integration would significantly reduce the overall size of the assembly which is critical for the application presented in this paper. Moreover, electrical performances can be expected to be improved thanks to 3D integration as the ASIC runs at 15MHz.

Regarding the Die to Wafer, 3D integration technology choice, we've taken into account the fact that the components to be assembled are heterogeneous and thus the process

temperature has to be minimized to avoid residual stress. Moreover, due to the difficulty of supplying components at wafer scale, we choose to use thermo compression on Ni micro bumps (Micro inserts technology) for face-to-face interconnection of the ASIC and the capacitors, as it enables us to avoid processing the dies prior to their attachment. Also, due to the low density of intra stratum interconnections (8 contacts for a 7x7mm² devices) Through Silicon Vias (TSV) technology won't be economically relevant, and thus we've focused on a Chip-in-Polymer process. As the trenched Capacitors devices cannot be thinned down to 90µm without affecting the reliability, high height copper pillar (100µm) technology have been chosen: ViaBelt™ Technology [5]. The scheme of the 3D integrated device is shown in **Figure 5**.

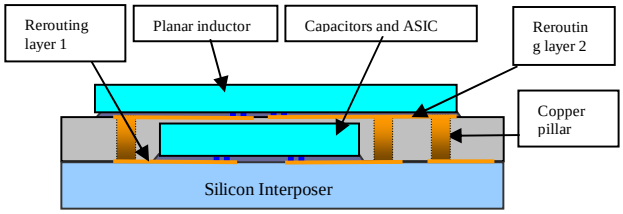

Figure 5 Schematic of the DC/DC 3D integration.

LETI's ViaBelt™ Process has been applied as described below:

a) Continuous Ti/Cu seed layer deposition,.

b) Growth of Nickel micro-inserts on the pre-determined host pads, as shown below in **Figure 6**.

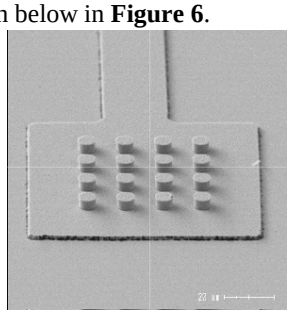

Figure 6 Array of Ni micro inserts on host pad.

c) Rerouting in the base layer. The patterns of this level have been specifically designed for all the host pads of the pillars to be connected to one another.

d) The copper pillars are electroplated by means of a photo-patternable dry thick film, as shown below in **Figure 7**.

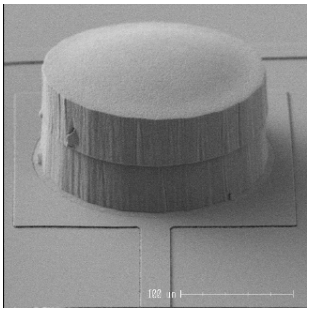

Figure 7 100µm Copper pillar.

e) Dies are flip-chipped with a DATACON 2200 APM+ machine. First a drop of epoxy glue is deposited on the base wafer, and the die is then aligned and positioned face-down, as shown in **Figure 8**. After all the dies have been placed, a collective thermo-compression stage is implemented to promote adhesion and Al-Ni connection between the dies and wafer.

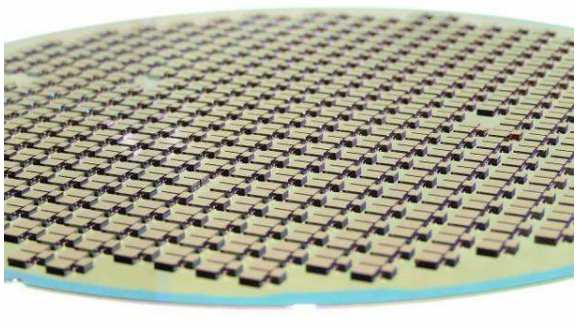

Figure 8 ViaBelt™ Dies to Wafer assembly.

f) After die attachment a specific polymer is spun to embed the chips and pillars.

g) To obtain again a surface on which a metal layer can be deposited, the polymer embedding layer is grinded until the copper pillars appear. Finally, a polymer layer is deposited to insulate dies bottom faces and opened on top of the Copper pillars, as shown in **Figure 9**.

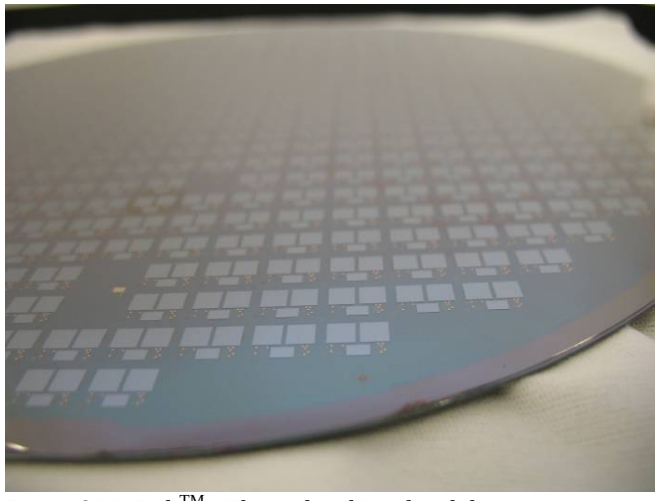

Figure 9 ViaBelt™ : Thinned and Insulated dies.

Inductor Attachment

It is envisaged that the final system would have the inductor fabricated using the process described earlier directly on the surface of the ViaBelt™ assembly. However to allow the initial electrical testing it was required that the integrated conductor and the ViaBelt™ assembled devices be electrically connected. As the copper pillars of the ViaBelt™ assembly need to be connected to the copper bond pads of the silicon integrated inductor, two standard interconnection methods (wire bonding and solder flip chip) were selected to allow this initial testing.

The wire bonding method consisted of attaching both the ViaBelt™ assembly and the silicon integrated inductor to a silicon sub mount using an ablestik 84-LMI-SR4 silver filled epoxy which is then temperature cured. 30 micron gold wire ball/wedge bonding was used to connect the copper pillars to the inductor bond pads.

The second method selected for the electrical connection was to use solder flip chip assembly. This was achieved by the use of commercially available 300µm SAC305 solder spheres. These spheres are a lead free Sn96.5Ag3.0Cu0.5 alloy with an approximate melting point of 220°C. The assembly process for this technique consists of solder ball placement on the two inductor bond pads. A further two solder balls are placed on the opposite corners of the inductor silicon to balance the silicon device during flip chip. These solder balls are then reflowed to a peak temperature of 240°C to attach them to the inductor. A no clean flux is used to aid this adhesion process. A Finetech flip-chip aligner bonder is then used to align and mount the device onto the ViaBelt™ assembly. Again the solder balls are reflowed to a peak temperature of 240°C with the aid of a no clean flux. Figure 10 below shows the silicon integrated inductor flip chip bonded to the ViaBelt™ assembly Figure 11 shows the cross section of one of the solder balls attaching the copper pillar to the inductor bond pad

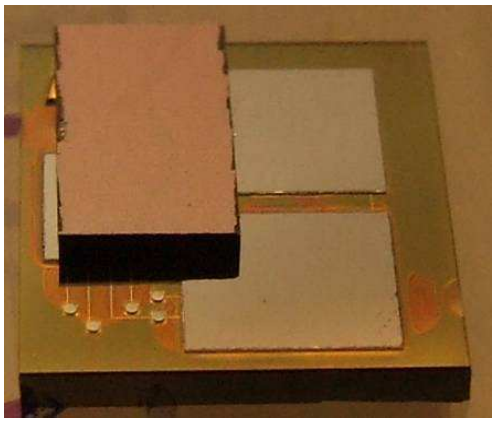

Figure 10 Global view of the 3D assembly

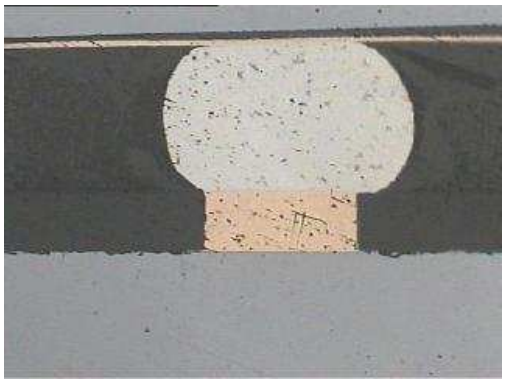

Figure 11 Solder ball attachment of pillar to inductor.

To provide further mechanical strength to the assembly the inductor chip is underfilled with a loctite underfill – Ablestik 8828 and cured in a convection oven. Figure 12 shows the cross section of the underfill of the inductor silicon.

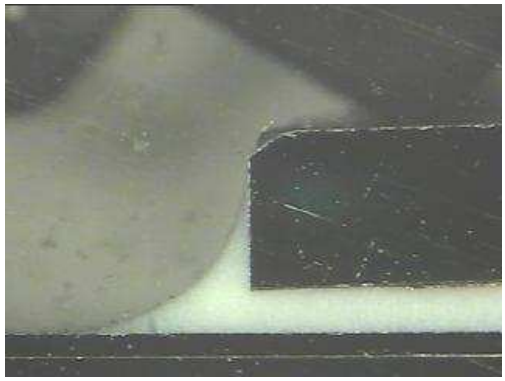

Figure 12 Inductor underfill.

Figure 13 shows the cross section of the whole device after all the assembly steps are completed. From this the inductor chip, inductor metal, ASIC chip and a copper pillar are visible.

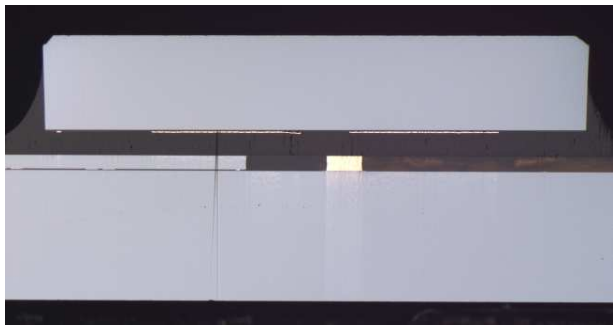

Figure 13 Micro sectioning of the 3D assembly.

Electrical Results

Electrical measurements were performed on two devices which have the inductor connected with gold wire bonds to the rest of the system. They have highlighted a significant reduction of the oscillations previously observed on Energy Management IC when tested with discrete passives: these oscillations can be hardly been seen whereas they were predominant previously. However, DC/DC converter efficiency and stability toward input voltage (linked to battery charge) was not as good as previously tested with discrete passives on the devices tested. This issue is still under investigation.

Conclusion

As a result, a 3D integration of a DC/DC converter for miniature sensor node network has been achieved. This is a key achievement for this application, solving one of its key issues and weighing in the spreading of autonomous sensors node networks. Moreover, the work presented in this paper demonstrates the successful mixing of processes from two European Integration Platforms.

Future work will consist of the full wafer scale integration of the inductor.

Acknowledgement

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