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Design and simulation of a new QCA-based low-power universal gate

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Quantum-dot Cellular Automata (QCA) is recognized in electronics for its low power consumption and high-density capabilities, emerging as a potential substitute for CMOS technology. GDI (Gate Diffusion Input) technology is featured as an innovative approach for enhancing power efficiency and spatial optimization in digital circuits. This study introduces an advanced four-input Improved Gate Diffusion Input (IGDI) design specifically for QCA technology as a universal gate. A key feature of the proposed 10-cell block is the absence of cross-wiring, which significantly enhances the circuit's operational efficiency. Its universal cell nature allows for the carrying out of various logical gates by merely altering input values, without necessitating any structural redesign. The proposed design showcases notable advancements over prior models, including a reduced cell count by 17%, a 29% decrease in total energy usage, and a 44% reduction in average energy loss. This innovative IGDI design efficiently executes 21 combinational and various sequential functions. Simulations in 18 nm technology, accompanied by energy consumption analyses, demonstrate this design's superior performance compared to existing models in key areas such as multiplexers, comparators, and memory circuits, alongside a significant reduction in cell count.

KEYWORDS

improved gate diffusion input, quantum-dot cellular automata, polarization, QCADesigner, low-power

1 Introduction

The enhancement of system capabilities and the trend toward reduced hardware sizes have brought to light significant challenges in complementary metal-oxide-semiconductor (CMOS) technology, particularly with the shift toward nanoscale circuitry. This development has prompted an increased need for alternative technological solutions, focusing on enhancing power efficiency and reducing the size of circuits (Sadrarhami et al., 2018).

Quantum-dot Cellular Automata (QCA) has garnered interest as a potential alternative to CMOS technology, primarily due to its high circuit density (approximately 1,012 cells/cm^2) and swift switching frequency (around 1 THz) (Naz et al., 2021). QCA technology uniquely integrates Boolean logic operations with quantum dot functionalities, leveraging the advanced physical simulation of both automata and quantum dot cells (Wang and Xie, 2018). This integration signifies a substantial advancement, aiming to enhance the efficiency and scalability

of semiconductor technologies. A Quantum cell contains four quantum dots and two mobile electrons. The arrangement of these electrons along one of the two primary diagonals determines the logical value of the cell, either zero or one. This configuration relies on the Coulombic interactions among the electrons, not only with adjacent neighbors but also with cells in diagonal positions and those in different layers. Thus, the logical state of any given cell depends on the states of surrounding cells, highlighting the importance of a comprehensive evaluation of neighboring cell states for accurate charge determination (Mohammadi and Navi, 2018; Wang and Xie, 2018). Thus, the logical charge assigned to any given cell is linked to the charges of its surrounding cells, necessitating a comprehensive assessment of neighboring cell states to ascertain each cell's charge (Wang and Xie, 2018) accurately. Figure 1 depicts a quantum cell in two polarization states of 0 and 1.

As illustrated in Figure 2, the architecture within QCA is segmented into four distinct clock zones, labeled 0, 1, 2, and 3. Each zone is characterized by a unique sequence of four clock phases: switch, hold, release, and relax (Sadeghi et al., 2020).at the switch phase, the cell's polarization state is established. Following this, the hold phase maintains this specified polarization without alteration. Progressing to the release phase, there is a gradual diminishment in the cell's polarization, leading to the relax phase where the cell's polarization is entirely neutralized. This cycle ensures precise control over the cell's energy state and data flow, highlighting the intricate design and operational efficacy inherent in QCA technology (Abutaleb, 2018).

In the realm of dynamic circuit analysis, the evaluation of energy levels and the determination of cell polarization are crucial. This is achieved through simulations conducted with a correlation vector engine. Specifically, the kink energy concept is pivotal, reflecting the energy differential between cells a and b when they exhibit opposing polarizations. This energy differential is quantifiable through the electrostatic interactions analysis among the charges present

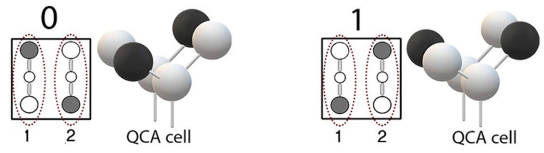

FIGURE 1
Two different polarization states of a QCA cell.

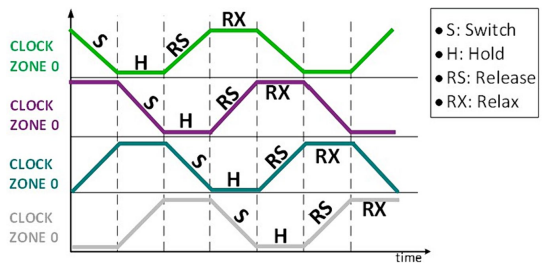

FIGURE 2
Four different phases in each clock zone (Sadeghi et al., 2020).

(Cardenas-Barrera et al., 2002). The method involves a detailed computation of electrostatic interactions between disparate points within the same cell, guided by equation (1), wherein the proportionality constant, known as Coulomb's constant, plays a fundamental role. The process to ascertain the kink energy entails an initial calculation of energy for cells exhibiting opposing polarities, followed by a similar computation for cells of identical polarity. The subtraction of these values yields the kink energy (Chen et al., 2019).

$$W_{a,b} = K\frac{q_a q_b}{[\gamma_b - \gamma_a]} \tag{1}$$

$$K = \frac{1}{4\pi\varepsilon_0\varepsilon_\gamma}$$

Circuit design errors in QCA technology encompass manufacturing, design, and clocking errors (Khan et al., 2023). Manufacturing errors, disrupt cell function due to chemical imperfections like single-electron defects (Bhat et al., 2023). The design errors affect both reversible and conventional circuits. Reversible design exhibits greater error resistance, maintaining functionality despite flaws and ensuring no data loss during computation. Although reversible design struggles with multiple lost or extra cell defects (Ahmadpour et al., 2023), common errors like cell displacement and wire crossing impact circuit function (Khan et al., 2023). Techniques such as the Friedkin gate, GDI gate, and tile design method have been utilized to mitigate these errors (Tougaw et al., 2021; Khan et al., 2023; Safaiezadeh et al., 2023). The tile in QCA technology, crucial for circuit design, provides higher error resistance than basic gates but may elevate circuit complexity. Optimal cell spacing for improved output ranges between 2 and 3 nanometers (Huang and Ottavi, 2005). In conventional design, QCA cells, majority gates, inverters, and wires form essential components, with errors in these elements leading to circuit flaws (Khan et al., 2023). Cell rotation is a notable error, particularly affecting curved QCA wires, with inverters exhibiting the least tolerance. Complex circuits are sensitive to rotation failures, but reliability can be enhanced by adding extra cells in the majority gate design. Cell misalignment poses additional challenges (Tougaw et al., 2021). The third type of fault is clocking errors. Accurate clocking, using appropriate methods, is vital for effectiveness. In QCA technology, clocking errors present a significant challenge that can affect the overall performance and reliability of computational circuits. Clocking in QCA is vital for controlling the information flow through the cells, ensuring that data moves in a precise and orderly manner (Khan et al., 2023). An error in the clocking sequence can disrupt this flow, leading to incorrect data processing and output. Such errors might occur due to synchronization issues, where the timing between different parts of the circuit becomes misaligned (Liu et al., 2014). Moreover, variations in fabrication processes can lead to inconsistencies in cell behavior under clocking signals, further exacerbating the problem. To mitigate clocking errors, designers employ rigorous simulation and testing methodologies, focusing on synchronization mechanisms and enhancing the robustness of the clocking architecture. This involves careful layout planning and the incorporation of error detection and correction mechanisms that can identify and compensate for clocking

discrepancies, thereby ensuring that the circuit maintains its intended functionality even in the presence of potential clocking inaccuracies (Liu et al., 2014).

GDI as an innovative approach for digital circuits is primarily attributed to minimalist transistor requirement and its ability to minimize power dissipation compared to traditional CMOS technology (Sadrarhami et al., 2018). A basic GDI configuration involves the integration of one PMOS and one NMOS transistor (Ghorbani et al., 2022). The superiority of GDI over CMOS is evident through its reduced transistor count, accelerated operational speed, diminished power consumption, and the simplification of Boolean function implementations. Additionally, the strategic interconnection of multiple GDI cells facilitates the creation of complex multi-input gates. The basic structure of a GDI gate is shown in Figure 3. Table 1 illustrates different Boolean functions that can be generated using this block (Abiri et al., 2019). The GDI presents a notable approach for designing low-power and compact digital circuits, particularly useful in digital logic and microprocessor design. Despite its advantages in reducing power consumption, GDI faces challenges. The GDI technique might introduce challenges in achieving high-speed performance for certain applications, as the propagation delays inherent in GDI circuits could impact operational speed. Overcoming these challenges requires innovative design strategies and the integration of GDI with other technology such as QCA technology to balance power efficiency with performance and noise resilience (Abiri et al., 2019).

The typical approach to circuit design in QCA technology involves combining the majority gates and inverters, which tends to enlarge the circuit footprint. Additionally, establishing communication between different gates increases circuit latency. Introducing universal gates, particularly for complex circuitry, can reduce circuit size, latency, and power consumption (Riyaz et al., 2024).

Universal gates, offering a wider functionality spectrum compared to standard majority and inverter gates, hold promise for minimizing circuit size, power usage, and latency (Hayati and Rezaei, 2019). Optimization techniques often borrow from successful strategies in other technologies. Therefore, in addressing the design challenge in QCA technology, this paper proposes a versatile gate utilizing GDI optimized in QCA to perform various fundamental functions. This GDI's application in QCA not only tackles GDI-related issues like high-speed performance, noise margins, and propagation delays but also resolves a fundamental challenge in QCA circuit design, namely the reliance on basic gates.

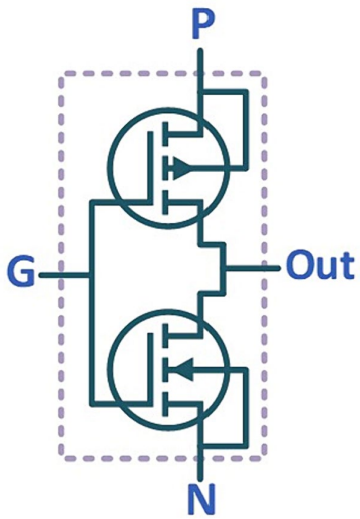

FIGURE 3
Gate diffusion input (Abiri et al., 2019).

For instance, in reference (Ghorbani et al., 2022), a dynamic XOR cell and full adder design using a combination of GDI and dynamic logic, termed D-GDI, is proposed. This design reduces the area, Power Delay Product (PDP), and parasitic capacitances at the output node and intermediate nodes. The D-GDI full adder also shows a 20% reduction in power consumption compared to the best existing designs. An improved version of this cell in reference (Abiri et al., 2014) reduces the chip area for pull-up and pull-down networks by about 80 and 50%, respectively, compared to the basic GDI cell, while also improving the PDP.

However, GDI-based digital integrated circuits, while advantageous in terms of power efficiency and simplicity of design, face a limitation in achieving full-swing capability. To overcome this problem, dynamic logic has been integrated with GDI to enable full-swing functionality.

In Abiri et al. (2019), a GDI unit is proposed for QCA technology, inspired by the circuit detailed in Abiri et al. (2014). This unit, constructed with 16 QCA cells, executes seven functions within an area of 0.02 μm^2 and experiences a delay of 2 clock pulses. By employing the QCA-GDI cell, multiplexer (MUX) circuits featuring two and four inputs were crafted and simulated, consisting of 16 and 30 cells, respectively, with an average energy consumption of 29.66 μeV. Furthermore, a two-input XOR gate was developed, comprising 39 cells, a 2-phase delay, and consuming 44.48 μeV of energy, and a full-wave rectifier (FWR) consisting of 30 cells with a 2-phase delay. Despite the unit's higher cell count and larger footprint, its minimal delay and accessible input/output cells offer advantages.

Mandai and Chakrabarty (2017) presents a Universal Logic Gate (ULG) in QCA technology, capable of implementing AND, OR, and XOR functions. With 11 cells, this planar gate covers an area of 0.01 μm^2 and operates within a single clock phase. Despite its reduced cell count, small area, and minimal delay, the gate's low robustness and limited functionality are drawbacks.

A 30-cell universal gate with 6 input cells is introduced in Hayati and Rezaei (2019). This three-layered design implements 13 standard universal gate functions and covers an area of 0.11 μm^2, indicating a large cell number. However, its 1-phase delay and accessible input/output cells are beneficial.

TABLE 1 Various logic functions for different input combinations of GDI cell (Abiri et al., 2019).

N	P	G	D	Functions
0	B	A	A'B	F1
B	1	A	A' + B	F2
1	B	A	A + B	OR
B	0	A	A.B	AND
C	B	A	A'B + AC	Mux
0	1	A	A'	NOT

In Tripathi et al. (2020), following the approach in Gupta and Wairya (2016), the design of basic circuits, adders, and comparators in QCA technology is discussed. An XOR gate with 11 cells, a 2-phase delay, an area of 0.012 μm^2, and a MUX gate with 19 cells and an area of 0.02 μm^2 are designed. Also, a 73-cell adder with an area of 0.08 μm^2 and a 25-cell single-bit comparator with an area of 0.03 μm^2 are presented. The primary advantage of this method is the low delay in the designed circuits. However, using various structures, large cell numbers, and higher areas are disadvantages.

In Riyaz et al. (2024), a universal and reversible gate is presented. This gate is designed and simulated using 39 cells and works in one clock phase. This gate with an area of 0.029 μm^2 can perform 13 different functions.

In Sadrarhami et al. (2018), a GDI block based on QCA technology using 11 cells is proposed. The block, covering an area of 0.01 μm^2, operates with a delay of one clock phase. It is based on the majority function as per equation (2), executing nine basic functions.

$$\begin{aligned} Output &= Maj\left(Maj\left(G',P,0\right),Maj\left(G,N,0\right),1\right) \\ &= Maj\left(G'P,GN,1\right) = G'P + GN \end{aligned} \tag{2}$$

Using the GDI method in designing a universal gate in QCA technology can reduce power consumption and smaller circuit areas by eliminating the need for basic gates. Hence, this article aims to propose a new QCA-based IGDI block as a standard design unit for implementing various digital circuits' basic functions.

The organization of this edition is as follows: First, in Section 2, we discuss how to design, test, and evaluate the QCA-IGDI block. Section 3 covers developing various types of circuits using the IGDI-QCA block. In Section 4, a comprehensive comparison is made between the proposed works and previous works, and finally, it ends with the conclusion in Section 5 of the article.

2 Proposed IGDI-QCA block

To solve the circuit design challenge with basic gates in QCA technology, in this paper, a universal gate is designed and simulated using the improved GDI technique. By changing the structure of GDI, an IGDI with four input cells is proposed. Then this plan is simulated in QCA technology. The operating principle of the IGDI-QCA block is encapsulated in equation (3), which is derived from the corresponding Karnaugh map and its subsequent simplification. The proposed IGDI-QCA block consists of 10 cells, which include four input terminals labeled P, G, N, and H along with one output cell.

$$\begin{aligned} &Output = GH^{'}PN^{'} + G'HPN^{'} + G'H'P'N + GHP^{'}N \\ &+G'H'PN + GH^{'}PN + G'HPN + GHPN \\ &\multimap\!\otimes\!\multimap = PN + G'H'N + G'HP + GH^{'}P + GHN \end{aligned} \tag{3}$$

Figure 4 displays the configuration of the proposed block, along with an examination of its functionality, encompassing output statuses for diverse inputs across different clock phases, and a depiction of energy consumption distribution.

The area of the proposed block is 0.011 μm^2. The scheme is designed in a single layer and lacks cross-coupling methods. Using one clock phase reduces the delay in the proposed gate. As shown in Table 2, the proposed block enables the implementation of a wide range of basic functions. By simply changing the input values in the proposed block unit structure, various basic operations such as AND, OR, NOT, BUFFER, XOR, XNOR, Multiplexer (MUX), majority logic, and a three-input exclusive OR can be performed.

It should be noted that to simulate the proposed block and all the circuits designed using the proposed block, QCADesigner-E software in 18 nm technology using default simulation parameters according to Table 3 and using dual vector simulator engines and coherence vector has been done. Also, to determine the amount of energy consumed and draw its distribution map, the QCAPro simulator has been used. The energy utilization of the proposed block, under three different energy levels, is meticulously detailed and tabulated in Table 3.

Table 4 provides the consumed energy of the proposed block at three energy levels, calculated and presented according to the method proposed in Timler and Lent (2002). The static energy stemming from leakage power is significantly lower than the dynamic energy arising from switching, displaying a similar state to circuits of CMOS technology. The average energy dissipation of the circuit, represented by Ebath_total, is estimated as the sum (Ebath) for each clock pulse cycle by each cell in the design, aiming to illustrate the overall wasted energy. In the following, several complex circuits are designed and simulated using the proposed block IGDI-QCA.

3 Designed combinational and sequential circuits using the proposed IGDI-QCA block

This part of the paper focuses on demonstrating the effectiveness of the proposed IGDI-QCA block by designing and simulating a range of commonly used logic and computational circuits. In addition to the mentioned basic gates, connecting multiple proposed blocks, more complex combinational and sequential circuits can be designed. An example of this application is the design of a single-bit comparator circuit using the IGDI-QCA block. The comparator is a crucial component in the decision-making processes of complex computing circuits. Its detailed structure, circuit design, simulation outcomes, and energy consumption metrics are comprehensively depicted in Figure 5. Optimizing the comparator circuit improves other circuits that use this gate.

Similarly, the application of the proposed IGDI-QCA block is further exemplified through the design of a four-bit parity generator circuit, as showcased in Figure 6. The four-bit parity generator is used in error detection in digital storage and communication systems. Producing a parity bit ensures the data integrity by checking whether the number of set bits is odd or even.

The importance of memory circuits in modern computing cannot be overstated, as they are crucial for data storage and retrieval, directly impacting the speed and efficiency of computational processes. QCA plays a pivotal role in the development of high-speed memory circuits. This article introduces a novel three-layer reversible memory structure in QCA, utilizing the advanced IGDI block. The memory design

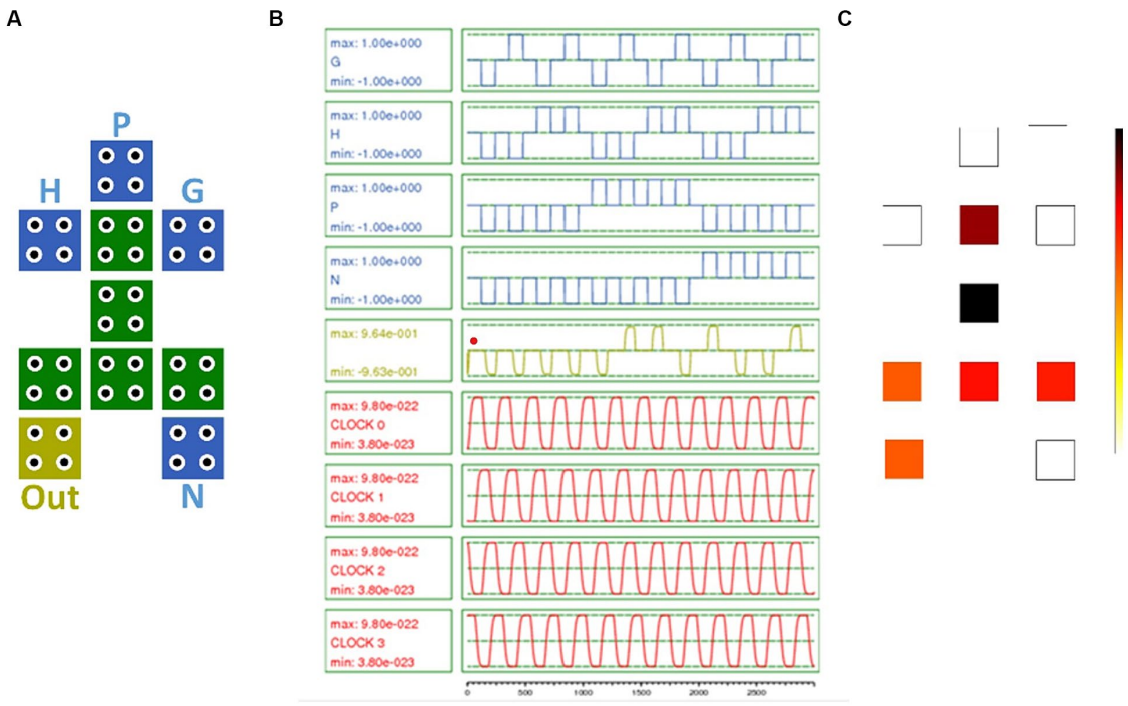

FIGURE 4
(A) Proposed gate simulation **(B)** Simulation results and **(C)** Energy dissipation map with.

TABLE 2 Logic functions implemented by the proposed MGDI cell.

H	N	P	G	OUT	H	N	P	G	OUT
0	0	B	A	AND (A, B)	0	B	A	1	A
1	B	0	A		1	B	A	0	
B	A	0	1		1	B	A	1	B
1	1	B	A	OR (A, B)	0	B	A	0	
0	B	1	A		0	1	B	A	B + A’
B	A	1	0		1	B	1	A	
−1	−1	1	A	Buffer (A)	B	A	1	1	A + B′
−1	+1	−1	A	NOT (A)	1	0	B	A	A’B
B	C	-	A	Maj (A, B, C)	0	B	0	A	
0	C	B	A	MUX = A’C + AB	B	A	0	0	AB’
1	C	B	A	MUX = A’B + AC	B	0	0	A	0
C	B	A	0	MUX = AC + BC’	B	1	1	A	1
C	B	A	1	MUX = BC + AC’	B	A	0	C	AB’C′ + ABC
B	0	1	A	XOR (A, B)	B	A	1	C	A + B’C + BC’
B	1	0	A	XNOR (A, B)	A	0	C	B	AB’C + A’BC
A	C′	C	B	TIEO (A, B, C)	A	1	C	B	A’ + C + B′
B	A	A’	C						

consists of 27 cells and operates across two clock phases, as illustrated in Figure 7.

The equations governing the three outputs of this proposed memory design are meticulously detailed in equation (3).

TABLE 3 Energy analysis of suggested IGDI-QCA cell.

	Tunneling Energy		
	0.5 E_K	1 E_K	1.5 E_K
Avg Leakage Energy Dissipation	0.00150	0.00459	0.00826
Avg Switching Energy Dissipation	0.00951	0.00835	0.00722
Avg Energy Dissipation of circuit	0.01101	0.01294	0.01549
Max Kink Energy	0.00148	0.00148	0.00148

$$\begin{aligned} O1 &= R / W \\ O2 &= R / W'.PO + R / W.I \\ O &= R / W'.I + R / W.PO \end{aligned} \tag{3}$$

The subsequent section will delve into a detailed evaluation and comparison of these circuits, underscoring the benefits of the proposed block.

4 Comparison

In this section, the outcomes of the proposed design are juxtaposed with prior studies. The sequential and combinational circuits fashioned by the proposed block are scrutinized against analogous circuits from earlier research, focusing on metrics like area, delay, and quantum cost. The proposed circuit is simulated using QCADesigner-E version 2.0.3 in 18-nanometer technology. Both dual vector and coherence vector simulation engines are employed to ascertain cell polarization with default parameters, yielding congruent

TABLE 4 Assessing the suggested IGDI cell in comparison to other existing works.

Reference	Technique	QCA cell count	Area (μm^2)	Latency (Clock zones)	Crossover type	Cost (Area*Latency)
Abiri et al. (2019)	GDI	16	0.02	2	Without	0.022
Mandai and Chakrabarty (2017)	ULG	11	0.01	1	Coplanar	0.01
Hayati and Rezaei (2019)	ULG	30	0.011	1	Without	0.011
Tripathi et al. (2020)	GDI	19	0.02	1	Without	0.02
Sadrarhami et al. (2018)	GDI	11	0.01	1	Without	0.01
Riyaz et al. (2024)	ULG	39	0.03	1	Without	0.03
Proposed	IGDI	**10**	**0.01**	**1**	**Without**	**0.01**

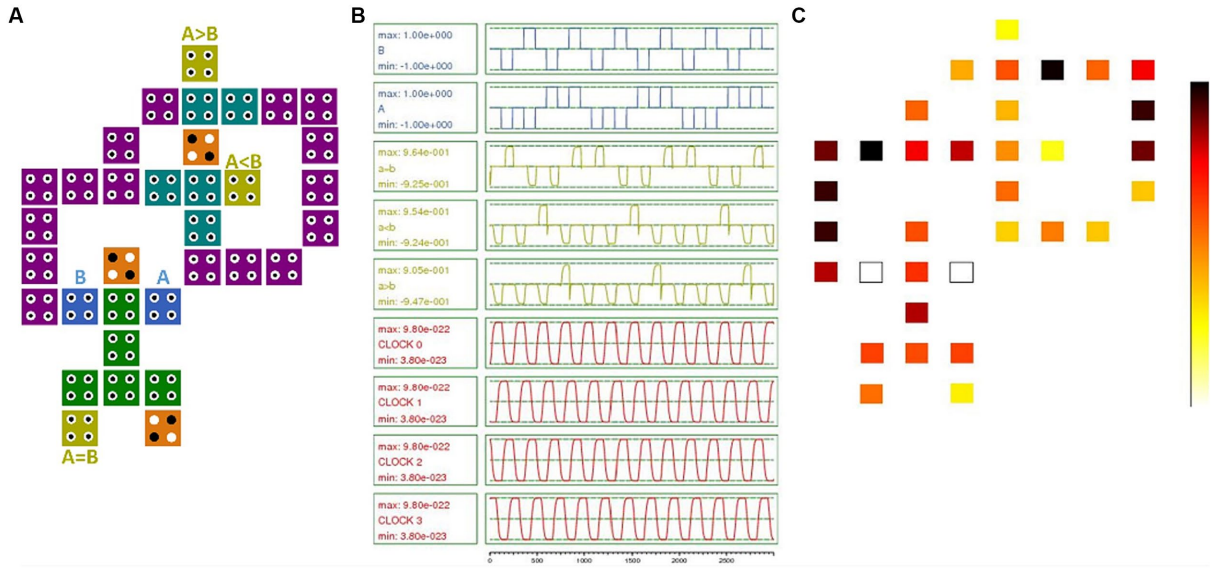

FIGURE 5
single-bit comparator using the proposed cell. **(A)** Proposed circuit simulation **(B)** Simulation results and **(C)** Energy dissipation map with 0.5 Ek.

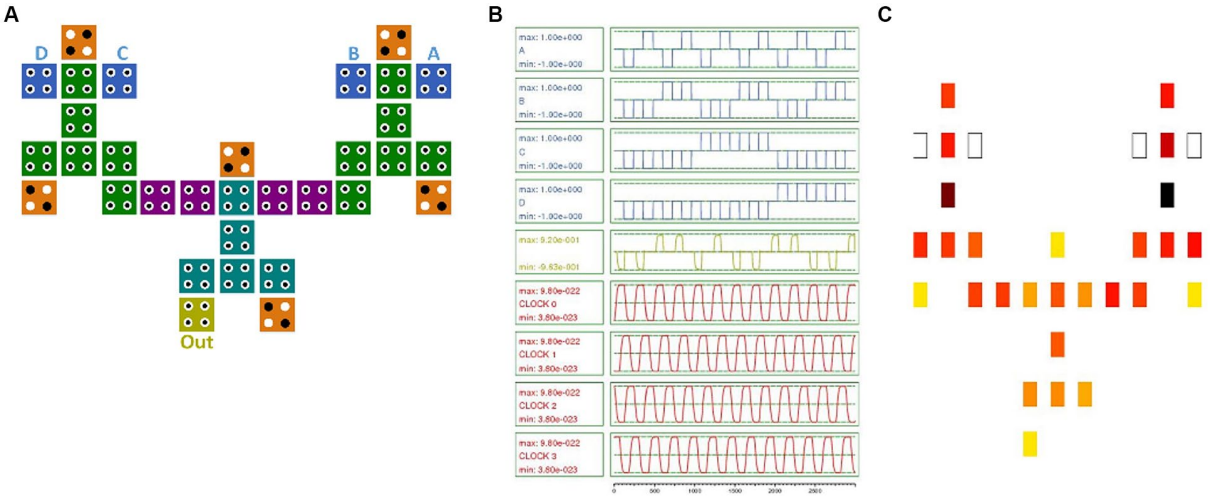

FIGURE 6
4-bit parity generator using the IGDI-QCA cell. **(A)** Proposed circuit simulation **(B)** Simulation results and **(C)** Energy dissipation map with 0.5 Ek.

results and affirming the design's accuracy. Comparison in Table 4 reveals the superiority of the proposed IGDI-QCA block in terms of cell count, area, and delay over prior works. When considering the cost function, defined as the product of area occupation and delay, only references (Mosleh, 2019; Perri et al., 2022) exhibit similar costs. Notably, reference (Mosleh, 2019) utilizes a coplanar type circuit, while reference (Perri et al., 2022) entails 11 cells. These insights are graphically depicted in Figure 8. Energy consumption is evaluated using QCAPro, indicating the proposed design's lower energy consumption relative to other works. Furthermore, Figure 9 illustrates the assessment results for total and average dissipated energy (Table 5).

Table 6 in the paper offers a comparative analysis between various 2/1 Multiplexers from prior studies and the proposed design. The proposed MUX gate, in number of cells compared to reference (Ahmadpour et al., 2022), and area compared to works presented in references (Rashidi et al., 2016; Naji Asfestani and Rasouli Heikalabad, 2017; Sushma et al., 2021; Ahmadpour et al., 2022), and delay compared to Naji Asfestani and Rasouli Heikalabad (2017), Shiri et al. (2019), Sushma et al. (2021) and Sreevani et al. (2023) and cost compared to Naji Asfestani and Rasouli Heikalabad (2017), and Sushma et al. (2021), shows no improvement. So, the analysis of Table 7 shows that the proposed MUX has the lowest number of cells compared to other works and is in an optimal state in other parameters.

According to Table 7, although the proposed X-circuit is the same as the reference (Wang and Xie, 2020) in terms of area, delay, and cost, it is better than all previous works in terms of the number of blocks.

As can be seen in Table 8, the reference comparator circuit (Shiri et al., 2019) has better results in terms of area, delay, and cost compared to the proposed scheme, while the proposed circuit is better than all the previous works in terms of the number of cells.

Table 9 in the article presents a comparative analysis of various 4-bit parity generators from past studies alongside the proposed design. While the circuit mentioned in Gassoumi et al. (2019), Safoev et al. (2022) shows better results in terms of area, and reference (Safoev et al., 2022) outperforms the proposed design in terms of cost, the proposed IGDI-QCA-based design notably excels in other aspects. Specifically, it shows a significant 31% improvement in cell count efficiency compared to previous models.

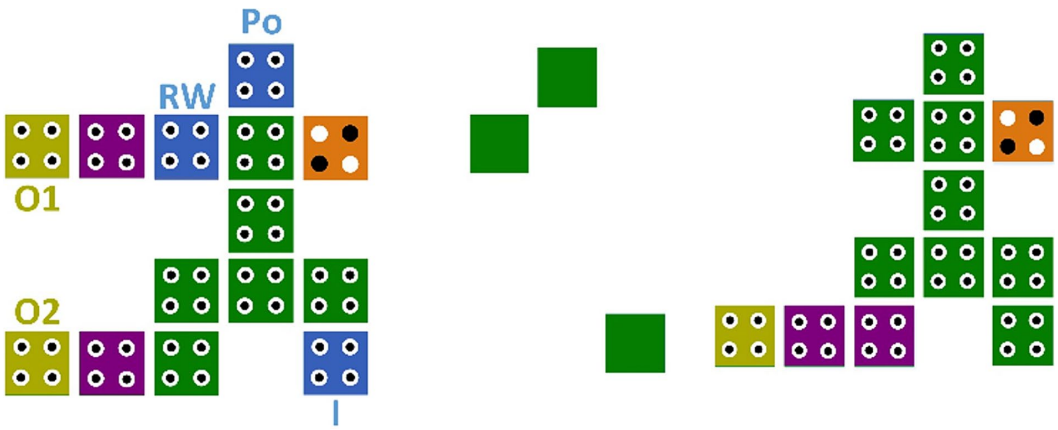

FIGURE 7
Proposed reversible memory layers.

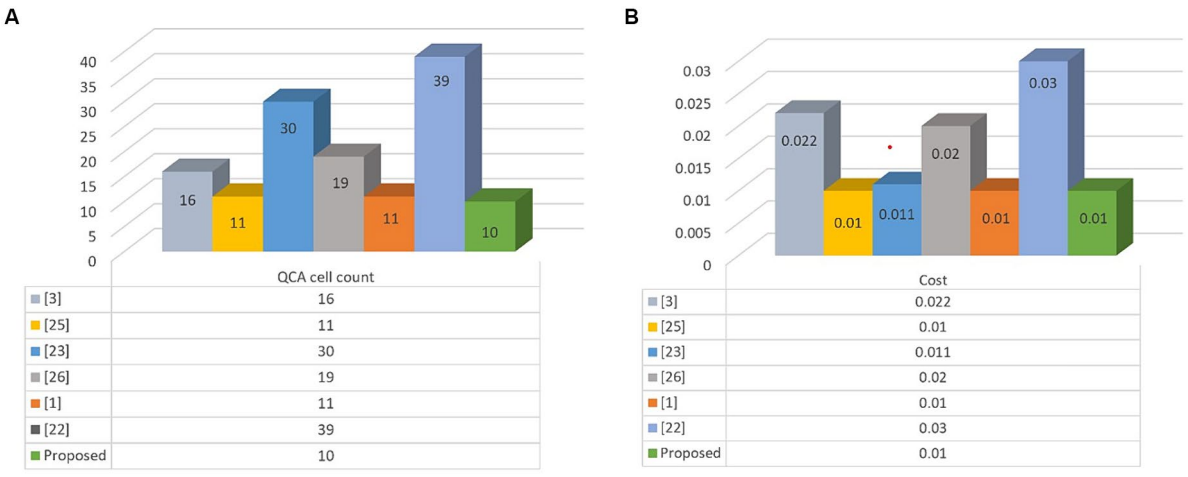

FIGURE 8
Comparison between the suggested block and existing works. **(A)** Number of cells **(B)** cost.

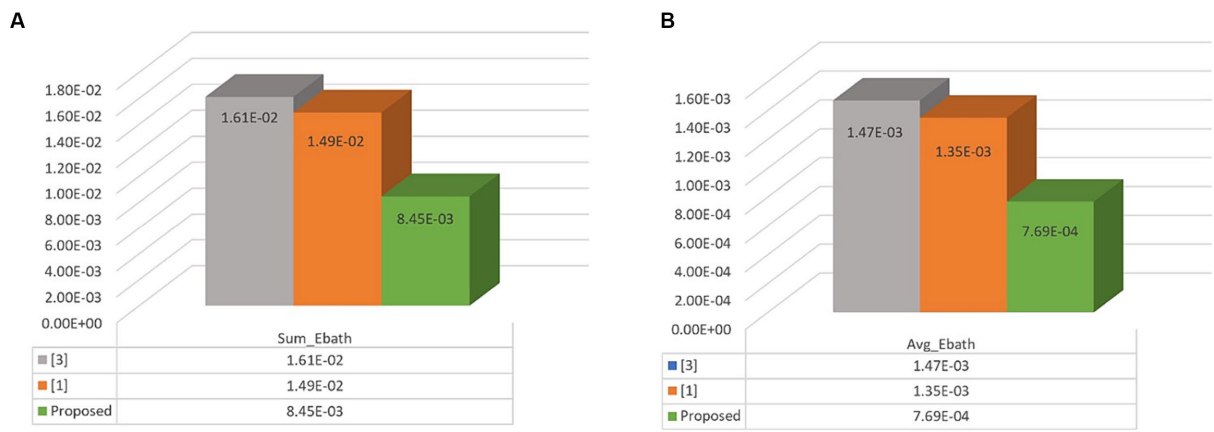

FIGURE 9
(A) Evaluation of the total energy consumed, **(B)** average energy consumed by the proposed.

TABLE 5 Results of evaluation of energy lost in the proposed IGDI-QCA cell and previous works.

Reference	Energy dissipation (total) eV		Energy dissipation (average per cycle) eV	
	Sum_Ebath	Error	Avg_Ebath	Error
Abiri et al. (2019)	$1.61e^{-002}$	$-1.75e^{-003}$	$1.47e^{-003}$	$-1.59e^{-004}$
Sadrarhami et al. (2018)	$1.49e^{-002}$	$-1.61e^{-003}$	$1.35e^{-003}$	$-1.46e^{-004}$
Proposed	$\mathbf{0.845e^{-002}}$	$\mathbf{-0.907e^{-003}}$	$\mathbf{0.769e^{-003}}$	$\mathbf{-0.825e^{-004}}$

TABLE 6 Comparison results of MUX 2 * 1 in the proposed design with previous works.

Reference	QCA cell count	Area (μm^2)	Latency (Clock zones)	Cost (Area*Latency)
Rashidi et al. (2016)	15	0.01	2	0.02
Naji Asfestani and Rasouli Heikalabad (2017)	12	0.01	1	0.01
Shiri et al. (2019)	16	0.02	2	0.04
Shiri et al. (2019)	19	0.02	1	0.02
Riyaz et al. (2024)	39	0.126	2	0.252
Sabbaghi-Nadooshan and Kianpour (2014)	26	0.02	2	0.04
Sen et al. (2015)	23	0.02	2	0.04
Sen et al. (2014)	19	0.02	2	0.04
Ahmadpour et al. (2022)	10	0.01	2	0.02
Sushma et al. (2021)	11	0.01	1	0.01
Sreevani et al. (2023)	13	0.02	1	0.02
Proposed	**10**	**0.01**	**1**	**0.01**

A comparative analysis of various memory designs is detailed in Table 10. The results show that the proposed design performs similarly to the circuit in reference (Macrae, 2022) in terms of area and cost, but it is superior in terms of the number of cells. Reference (Salimzadeh et al., 2020) is equivalent to the proposed work in terms of area and delay.

Furthermore, compared to the circuit mentioned in Sadeghi et al. (2020), the proposed memory design, leveraging the capabilities of the IGDI-QCA block, shows remarkable improvements. Specifically, it achieves a 34% reduction in area, 50% in delay, and 67% in overall cost. It's noteworthy that the circuit from Sadeghi et al. (2020) utilizes a combination of four AND gates, and one each of OR, NOT, and MUX gates. This configuration contributes to an increased area and delay in their design. In contrast, the proposed circuit effectively addresses these issues by integrating the efficient IGDI-QCA block, resulting in a more compact, faster, and cost-effective memory circuit solution.

It's important to note that the novelty of the presented manuscript lies in the improvement and modification of the conventional GDI structure from a 3-input to a 4-input configuration. As indicated in Table 2, this structure can perform 33 different functions compared

TABLE 7 Comparative results of XOR gate.

Reference	QCA cell count	Area (μm²)	Latency (Clock zones)	Cost (Area*Latency)
Singh and Sharma (2020)	24	0.02	3	0.06
Zhang et al. (2020)	27	0.02	3	0.06
Wang and Xie (2020)	13	0.01	1	0.01
Proposed	**10**	**0.01**	**1**	**0.01**

TABLE 8 Comparison result of single bit comparator.

Reference	QCA cell count	Area (μm²)	Latency (Clock zones)	Cost (Area*Latency)
Erniyazov and Jeon (2018)	85	0.06	5	0.3
Qadri et al. (2018)	58	0.05	3	0.15
Deng et al. (2017)	42	0.05	3	0.15
Shiri et al. (2019)	38	0.03	2	0.06
Pal et al. (2021)	37	0.06	3	0.18
Majeed et al. (2021)	35	0.04	3	0.12
Proposed	**34**	**0.04**	**3**	**0.12**

TABLE 9 4-bit parity generator comparison results.

Reference	QCA cell count	Area (μm²)	Latency (Clock zones)	Cost (Area*Latency)
Poorhosseini and Hejazi (2018)	111	0.14	8	1.12
Kassa et al. (2018)	97	0.1	7	0.70
Khakpour et al. (2020)	86	0.1	6	0.60
Gassoumi et al. (2019)	37	0.05	6	0.30
Safoev et al. (2022)	38	0.02	3	0.06
Proposed	**32**	**0.06**	**3**	**0.18**

TABLE 10 RAM comparison results.

Reference	QCA cell count	Area (μm²)	Latency (Clock zones)	Cost (Area*Latency)
Fam and Navimipour (2019)	55	0.06	10	0.6
Mubarakali et al. (2019)	87	0.07	6	0.42
Salimzadeh et al. (2020)	32	0.02	2	0.04
Ahmadpour et al. (2022)	26	0.03	4	0.12
Proposed	**29**	**0.02**	**2**	**0.04**

to 6 functions achievable by the traditional GDI structure. Additionally, to evaluate the proposed block, several combinational and sequential circuits have been designed using it and compared with existing works, demonstrating the efficiency of the proposed block.

5 Conclusion

This paper introduced an innovative four-input GDI variant, termed Improved GDI (IGDI), achieved through an Improvement of the traditional GDI structure. Subsequently, this IGDI has been adapted and tested within QCA technology. The IGDI block, comprising a mere 10 cells, emerges as a versatile design unit capable of performing basic Medium-Scale Integration (MSI) combinational functions and being integral to sequential circuits.

A key feature of the IGDI block is the absence of cross-wiring, which significantly enhances the circuit's operational efficiency. Its universal cell nature allows for implementing various logical gates by merely altering input values without necessitating any structural redesign. Consequently, by setting one of the inputs to either "0" or "1," the block can effectively realize gates such as AND, OR, XOR, and MUX within the IGDI-QCA framework. This flexibility leads to notable improvements in aspects like energy efficiency, cell count reduction, and occupied area minimization. Furthermore, the IGDI block is adept at designing other basic combinational functions including NOT, BUFFER, XNOR, and Majority (Maj). The design and simulation outcomes for sequential

functions, such as reversible memory, highlight the significant reduction in cell count achieved by the proposed cell compared to previous models. Additionally, the decrease in overall energy consumption (Sum_Ebath) and the cost function are key benefits of this innovative design, underscoring its potential for advancing circuit technology.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

HS: Conceptualization, Data curation, Formal analysis, Funding acquisition, Investigation, Methodology, Project administration, Resources, Software, Supervision, Validation, Visualization, Writing – original draft, Writing – review & editing. SZ: Conceptualization, Data curation, Formal analysis, Funding acquisition, Investigation, Methodology, Project administration, Resources, Software, Supervision, Validation, Visualization, Writing – original draft, Writing – review & editing. MD: Supervision, Writing – review & editing. BB: Supervision, Writing – review & editing.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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