UNIVERSIDADE DO ALGARVE

ELECTRICAL CHARACTERIZATION OF ELECTRONIC CIRCUITS PRODUCED BY INKJET PRINTING

Vitaliy Parkula

Dissertação

Mestrado Integrado em Engenharia Electrónica e Telecomunicações

Trabalho efetuado sob a orientação de:

Prof. Doutor Henrique Leonel Gomes

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"Declaração de autoria de trabalho"

Declaro ser o autor deste trabalho, que é original e inédito. Autores e trabalhos consultados estão devidamente citados no texto e constam da listagem de referências incluída.

Vitaliy Parkula

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Resumo

Impressão a jato de tinta tem atraído a atenção como uma nova tecnologia para a produção de dispositivos semicondutores, de grande área, a baixo custo. A eletrónica impressa irá ser fina, leve, flexível e inofensiva para o meio ambiente. Além disso, esta tecnologia possibilita a criação de uma ampla gama de componentes e circuitos eletrónicos que podem ser produzidos em massa e integrados em novas aplicações, como por exemplo nos dispositivos portáteis.

Esta dissertação reflete o trabalho efetuado na caraterização elétrica de dispositivos eletrónicos impressos a jato de tinta. Resumidamente, dois tipos de dispositivos foram estudados: (a) transístores de efeito de campo em estrutura MIS (Metal-Isolador-Semicondutor) e (b) díodos retificadores. Foram abordados vários aspetos relacionados com os parâmetros individuais do dispositivo, nomeadamente, foi estudada a estabilidade operacional quando o dispositivo é sujeito a uso contínuo, efeitos de envelhecimento, variabilidade e escalabilidade.

Foram fabricados e caracterizados circuitos lógicos de inversor e de porta NAND. Vários tipos de díodos retificadores foram avaliados em termos de resposta em frequência. Díodos Schottky, díodos compostos em estrutura MIS e transístores conetados como díodos. A propriedade incomum de retificação dos díodos em estrutura MIS é explicada. O díodo de tipo Schottky foi utilizado juntamente com um condensador impresso para montar um circuito retificador de meia-onda. Demonstra-se ainda, que este circuito é capaz de produzir um sinal DC retificado quando recebe na entrada uma onda sinusoidal com a frequência de 13.56 MHz. O uso deste circuito retificador como um bloco na construção de uma etiqueta de identificação por radiofrequência (RFID tag) é analisado.

Palavras-chave: Eletrónica orgânica impressa a jato de tinta; Transístor orgânico de película fina; Circuito inversor orgânico; Díodo retificador orgânico; Etiqueta orgânica de identificação por radiofrequência.

Abstract

Ink-jet printing has been attracting attention as a new technology for low-cost, large-area production of semiconductor devices. Printed electronics will be thin, lightweight, flexible and environmentally friendly. Furthermore the technology enables a wide range of electrical components and circuits that can be massively produced and integrated in new applications such as wearable devices.

This thesis reflects the work done in the electric characterization of electronic inkjet printed devices. Basically, two types of devices were studied: (a) metal-insulator semiconductor (MIS) field effect transistors and (b) rectifying diodes. We address several aspects related with individual device parameters, namely we studied the operational stability under continuous operation, ageing effects, variability and scalability.

Inverter and NAND logic gate circuits were also fabricated and characterized. Several types of rectifying diodes were assessed in terms of their frequency response. Schottky type diodes, MIS capacitor diodes and diode connected transistors. The unusual rectifying property of MIS diodes is explained. The selected Schottky type diode, was used together with a printed capacitor to assemble a half-wave rectifying circuit. It is shown that this circuit provides a DC rectified signal when excited by a sinusoidal input at the frequency of 13.56 MHz. The use of this rectifying circuit as a building block for a radio frequency identification (RFID) tag is discussed.

Keywords: Organic inkjet printed electronics; Organic thin film transistor; Organic inverter; Organic rectifying diode; Organic radio frequency identification tag.

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Abbreviations

AC	Alternate Current
Ag	Silver
BC	Bottom Contact
cPVP	Cross-linked Poly-4-Vinylphenol
Cu	Copper
DC	Direct Current
DS	Drop Space
ENEA	Energy and Sustainable Economic Development, Italy
FET	Field-Effect Transistor
HW	Half-wave
MAA	Methacrylate Acid
MIM	Metal-Insulator-Metal
MIS	Metal-Insulator-Semiconductor
MISFET	Metal-Insulator-Semiconductor Field-Effect Transistor
MMA	Methacrylic Acid
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OLED	Organic Light Emitting Diode
OTFT	Organic Thin-Film Transistor
PEN	Polyethylene Naphthalate
PET	Polyethelene Erephthalate
PFTP	Pentafluorothiophenol
PGMEA	Propylene Glycol Monomethyl Ether Acetate
PTAA	Polytriarylamine
PVP	Poly-4-Vinylphenol
RFID	Radio-Frequency Identification
TC	Top Contact
TDK4PE	Technology & Design Kit for Printed Electronics
TFT	Thin-Film Transistor
TUC	Technical University of Chemnitz

Chapter 1

INTRODUCTION

Organic Thin Film Field-Effect Transistors (OTFTs) involve particularly interesting fabrication processes, which are much less complex compared with conventional Si technology (involving high-temperature and high vacuum deposition processes and sophisticated photolithographic patterning methods). As a result, there is now a serious level of industrial interest in using OTFTs for applications currently incompatible with the use of a-Si or other inorganic transistor technologies. One of their main technological attractions is that all the layers of an OTFT can be deposited and patterned at low room temperature by a combination of low-cost, solution-processing, and direct-write printing using ink-jet printing techniques, which makes them ideally suited for realization of low-cost, large-area electronic functions on flexible substrates [**1**,**2**].

Inkjet printing represents a solution based technique that is characterized by its non-contact, material-efficient and reproducible processing. Major developments were lately made to improve inkjet printing techniques, where studied imply that nowadays, inkjet printing can bridge the gap between polymer synthesis and solid-state or surface property evaluation, since the technique opens the way to the automatic preparation of thin-film libraries of polymers, polymer blends and composites, with a systematic variation of parameters such as chemical composition or thickness [**3**].

The mechanical flexibility of organic materials provides a natural compatibility with plastic substrates for lightweight and foldable products. This way, the OTFTs gain a large area of applications, where they already have been demonstrated in applications such as electronic paper displays [**4**,**5**] and memory devices including radio frequency identification (RFID) tags [**6**,**7**]. While compared to conventional inorganic TFTs, the OTFTs are not meant to replace them (because of the upper limit of their switching speed), but they create a great potential for a wide variety of applications, new products with unique characteristics, such as electronic newspapers, inexpensive smart tags for inventory control, and large-area flexible displays.

This work aims to electrically characterize organic devices and some circuits where they are implemented.

1.1 CONTRIBUITIONS

Devices and knowledge imparted by various partners of the European project "Technology & Design Kit for Printed Electronics" (TDK4PE).

1.2 STRUCTURE OF THE THESIS

This work is divided into 10 parts:

- The first consists of brief introduction, where Chapter 2 and 3 focus on theoretical aspects of inkjet printing and organic transistor operation;
- Chapter 4 discusses electrical characterization of inverter and NAND logic gate;
- Chapter 5 focus on parameter variability of OTFTs, while in Chapter 6 their stability is studied;
- Chapter 7 and 8 present electrical characterization of organic diodes and capacitors, respectively;
- Radio Frequency Identification Tag is built and studied in Chapter 9;
- Finally, Chapter 10 identifies conclusions of this work.

Chapter 2

INKJET PRINTING TECHNOLOGY FOR ORGANIC BASED ELECTRONICS

Inkjet printing has grown to be a very promising technology as a method of deposition of functional materials. Some of examples of functional materials that can be ink-jet printed include metal inks, conductive and semiconductive polymers, proteins and nanoparticles.

High reproducibility, non-contact pattering, high speed and high quality deposition onto well-defined locations on a substrate, made the inkjet printing to be a cost-effective and flexible method to be used in several research areas such as chemical, mechanical, optical and in a wide range of applications like electronics, optoelectronics and displays.

This chapter is focused on the main features of inkjet printing and provides an overview of the piezoelectric inkjet printing method, which is used to fabricate the devices studied in this thesis.

2.1 INKJET PRINTING TECHNIQUES

Inkjet printing technique is based on printing graphical images by ejection of tiny droplets on a substrate, and can be divided in two main classes: continuous inkjet (CIJ) and drop on demand inkjet (DOD). Each of these printing techniques provide different ways to create droplets and to control their placement on the substrate.

2.1.1 CONTINUOUS INKJET

Continuous Inkjet requires a continuous generation of ink stream from a pressurized fluid reservoir and it is mainly used in high volume applications, such as industrial coding of products and packages.

During the printing process, the continuous stream of droplets that is leaving the nozzle, is exposed to an electric field by means of a charging electrode. The inkjet printed drops receive different charge, so when they move towards the substrate and passing through a second electric field, their path is bended and they are deflected more or less in different directions due to the field applied. The variation of the charge applied to each drop provides control over their deflection. Only a small amount of the droplets is used to print, the rest is directed into a gutter for recirculation. This way the

ink reuse process is created. Fig. 2.1 illustrates a schematic of continuous inkjet printing system.

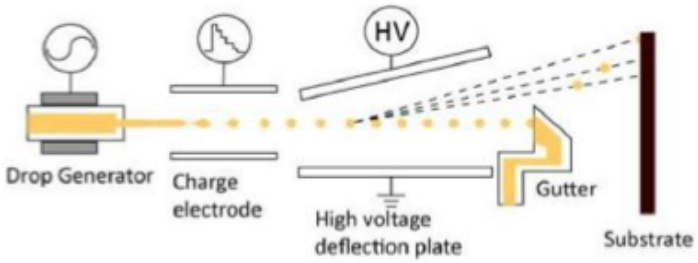

Fig. 2.1 - Schematic illustration of a multiple-deflection continuous inkjet [**8**].

Due to the continuous flow of ink through the nozzles, the risk of clogging them is severely minimized. The continuous inkjet printing can be divided into three main categories, which are related to the different levels of charge and of droplet deflection: Binary Deflection, Multiple Deflection and Hertz.

2.1.2 DROP ON DEMAND

Drop on Demand is a technology that only ejects drops required for printing and it is used in the majority of printers, dominating the market for home users. The smaller drop size and the higher positioning accuracy of DOD inkjet printers are their key advantages for the direct printing of the inks. This approach eliminates the complexity of drop charging and deflection hardware (since it is detrimental for functional materials) and the inherent unreliability of ink recirculation systems required for continuous inkjet technology. The available Drop on Demand techniques can be classified in five main types: Thermal, Piezoelectric, Electrostatic, Focused Acoustic and Piezo-Acoustic DOD inkjet printers, where the first two are mainly used.

Thermal Inkjet is considered as the most common inkjet technique and it dominates the market for home users. In this technique, the ink drops are ejected from a nozzle by the growth and collapse of a vapor bubble on the top surface of a small heater located near the nozzle. With a current pulse of less than a few microseconds through the heater, the ink's temperature rises to the critical value for bubble nucleation. When the nucleation occurs, a vapor bubble expands rapidly to force the ink to form a drop outside the nozzle. The whole process of bubble formation and collapse takes place in less than 10 μs. The ink then refills back into the chamber and the process is ready to restart. This process is schematically illustrated in Fig. 2.2.

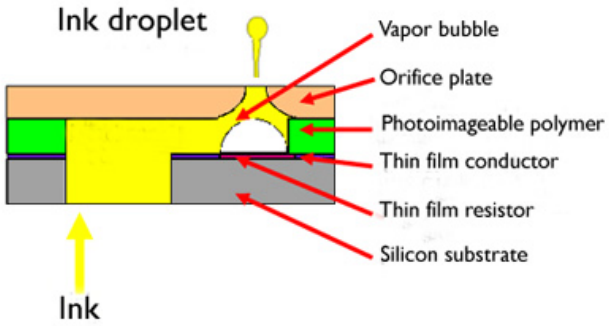

Fig. 2.2 - Schematic illustration of a thermal inkjet [**9**].

Due to the heating process included in thermal inkjet, which can cause a degradation of the material properties for functional inks, the focus goes to piezoelectric printer.

In a piezoelectric inkjet device, a piezoelectric material is used instead of a heating element to produce the force necessary to eject a droplet. Piezoelectric materials deform when a voltage is applied onto them. In an inkjet head, this deformation can be used to displace volume in a fluid chamber for droplet ejection (Fig. 2.3). Unlike thermal inkjet, the process is purely mechanical and therefore does not present degradation problem of the inks, e.g. no evaporation of solvents.

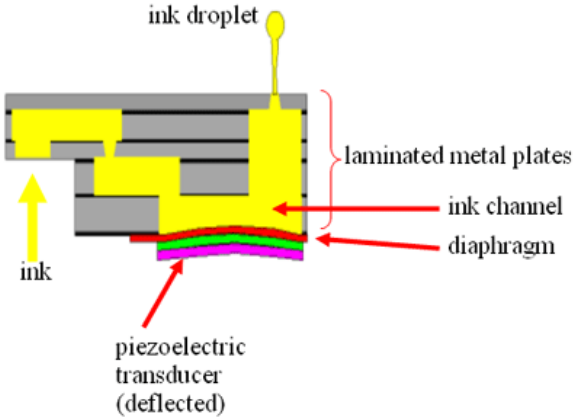

Fig. 2.3 - Schematic illustration of a piezoelectric inkjet [**9**].

2.2 PRINTING TECHNOLOGY

Piezoelectric inkjet technique was used to print devices studied in this thesis. The used printer is the Fujifilm Dimatix DMP2831 model, which is presented in Fig. 2.4.

Fig. 2.4 - Fujifilm Dimatix DMP2831 printer machine [**10**].

The Fujifilm Dimatix DMP2831 printer machine fits a wide range of applications, which according to its manufacturer, reside within material and fluid development and evaluation, prototype and sample generation. This system also allows deposition of biological fluids, including cell patterning and, DNA arrays.

The printer enables deposition of fluid materials maximum on an A4 substrate. It uses a disposable piezo inkjet cartridge, which allows to eject smaller droplets in comparison with the other inkjet technologies like the heating bubble. For every ink, the waveform that excites the piezoelectric jet must be adjusted.

The inkjet printer is able to eject 1 pL and 10pL drops (drop diameter size deposited depends on the material) with a resolution of 5μm. In the experimental printing setup, the printer was configured to 10 pL nominal drop volume and the used cartridge had 16 nozzles, where each of nozzles had a diameter of about 21.5 μm.

2.3 INK-SUBSTRATE INTERACTIONS

Printed electronics have been initially oriented towards the use of glass and a limited range of plastic substrates. PET substrates, which are low-cost, and PEN substrates offering a great dimension and low surface roughness, probably will continue to dominate the plastic substrates used in printed electronics.

The non-contact nature of inkjet deposition makes it a very versatile process being applicable to a wide range of substrates. One of the crucial factors in optimization of the deposition process resides within the interaction process between the deposited fluid and the substrate surface. Another critical aspect of the inkjet printing technique for the quality of the printed material is related to the drop drying process that is basically controlled by the “coffee-ring” effect, which will be discussed below.

2.3.1 WETTING OF THE SUBSTRATE

In the printing processes, the main ruling factor in the spreading of the fluid droplet on the substrate is the surface tension of components. This property is revealed, for example, in floating of some objects on the surface of water, although they are denser than water. Surface tension is caused by cohesion of molecules and is responsible of many behaviors of liquids. Because of surface tension, the surface of a liquid can support light objects. The surface tension is defined as the energy to increase the surface area of a unit. Therefore, its unit of measurement is energy for unit of area.

The wetting, which is the ability of a liquid to maintain contact with a solid surface, is determined not only by the liquid surface tension, but even by the surface energy of the solid surface and by the balance between adhesive (between molecules in the liquid and solid) and cohesive forces (between the molecules in the liquid) at the interface (interfacial tension). From the wetting perspective, is undesirable to have very low surface tension because of the wider spreading on the target substrate that makes difficult the realization of a well-defined structure. In order to modify the wetting, different surface treatments are applied. Typically, oxygen plasma, corona and silane treatments are the commonly used processes to modify the surface energy of the substrate.

2.3.2 "COFFEE-RING EFFECT"

One of the crucial features of the printing process is correlated to the droplet drying process that basically induces a final printed droplet, which is characterized by the presence of high ridges at drop edge. This effect, called "coffee-ring effect", was first explained by Deegan et al. in 1997 [**11**]. This phenomenon describes the tendency of the solute to flow out towards the droplet edge through a capillary flow during drying. This occurs owing to the maximum of the evaporation rate and to the drop pinning at the three-phase contact line [**11**,**12**,**13**].

During the evaporation of solvents incorporated in a printed droplet, while solvent molecules evaporating at the center of the droplet are readily reabsorbed, solvent molecules from the edge can easily escape without any reabsorbing process. This phenomenon results in a larger evaporation rate around the edge. Such a fast evaporation at the contact line induces an outward diffusive flow to compensate for the liquid removed by evaporation and, in turn, transports the suspending solute to the edge

region [**14**,**15**]. This effect is represented in Fig. 2.5, which causes a poor uniform distribution of the printed material that, in general, degrades the final device performance.

Fig. 2.5 - Illustration of the "coffee-ring" effect. Evaporation rate (represented by upward arrows) is highest at the edges of a printed droplet resulting in an accumulation of the solute at the periphery at the end of the drying process [**8**].

Possible approaches to reduce the 'coffee-ring' effect are based on the use of surface treatments (plasma, silane, etc.) and mixtures of solvents with different boiling points and surface tensions [**16**] (also known as "Marangoni effect") in order to modify the surface energy of the substrate and the surface tension of the liquid, respectively.

2.3.3 ELECTRONIC DEVICES FABRICATED BY INKJET

From the discussions above, we can appreciate that the printing parameters such as the drop space, the hydrodynamic properties of the ink formulations used and the hydrophobicity of the substrates, play a crucial role in the quality of the layers deposited. If we remember that electronics devices relay on interfaces to work properly we can see that the making electronic devices from printed solutions is a challenge because it requires a careful optimization of a very high number of parameters. The drop spacing the coffee-ring and the Marangoni effect will have a major influence on the layer thickness and also on the layer uniformity. The viscosity of the ink formulations must also to be carefully optimized, if a low boiling solvent is used, it may evaporate too fast leaving behind a network of pinholes, where the next printed layer can diffuse trough. The contamination of the surfaces is crucial. Often it is not possible to print the semiconductor layer on top of the dielectric because dewetting problems. Surface treatments are required. These treatments are aggressive such as UV exposure and they create a high density of electronic traps which destroy the device performance.

Even, if all the parameters are optimized and devices such as organic field effect transistors are printed and working properly, the technology still faces several challenges, one is scalability and the other parasitic effects .

In order to make circuits arrays of transistors with different active areas have to be printed. For instance inverter circuits and ring oscillators they require pairs of transistors

with different active areas. It is then crucial to assure that the technology is scalable. The model that describes a transistor with a small active area should also describe a transistor with a large active area. This is not trivial in ink-jet printing. When 1 mm square is printed may not produce the same layer thickness as a 2 mm square. For example, if the Marangoni effect is acting, the solvent will move towards the middle of the wet region creating a thicker printed layer.

The consequence is that large area transistors will have thicker layers than a small area transistor. If these effects are not corrected and take into account, they will cause variability on the transistor parameters. For instance a slightly thicker dielectric layer will cause apparent lower field effect mobility. Variations in the thickness of the semiconductor cause variations in the parasitic off current.

It is also crucial to assure that the electrical properties of the devices are intrinsic and not disturbed by parasitic effects. Most common parasitic are currents flowing trough the surface (lateral conduction) and fringing effects. These parasitic as are due to a bad device design. For other technologies these aspect have been studied deeply and eliminated or substantially reduced. In ink-jet printing is still in its infancy and the sources of variability in electronic devices and how they are related with the processing parameters are still unknown. In this thesis some of these aspects will be discussed in chapter 5.

Chapter 3

BASICS ABOUT ORGANIC THIN FILM TRANSISTORS

This chapter is focused on introduction about Organic Thin Film Transistors (OTFTs) architecture and operation modes, including some insights about organic semiconductor materials.

3.1 INTRODUCTION

The transistor was probably the most important invention of the 20th Century. The concept of field-effect controlled current appeared near year 1930, but the first device based on that theory was realized thirty years later, namely, the silicon-based metal-oxide-semiconductor field-effect transistor (MOSFET) [**17**]. These days, millions of MOSFETs are applied in the personal computer's processors and other microelectronic devices.

An alternative geometry approach was used on the thin-film transistor (TFT) [**18**]. The difference between TFT and MOSFET resides within the conducting channel, which is constituted by an accumulation layer in TFT, rather than an inversion layer.

In the late 1940s appeared organic semiconductors [**19**], but only an organic based semiconductor transistor was reported in 1986 [**20**]. The possibility of fabrication of organic TFT (OTFT) was presented in 1989 [**21**]. Through years of development of solution processed materials and innovative techniques of manufacturing, like spin-coating, spray-coating and inkjet printing, nowadays OTFTs had tremendously grown and they are being applied in products like radio-frequency identification (RFID) tags [**22**], single-use electronics, low-cost sensors and flexible displays [**23**].

3.2 INTRODUCTION TO ORGANIC SEMICONDUCTORS

Organic semiconductors are divided in two major classes: small molecules (low molecular weight material) and polymers. A major difference within these two classes lies in the process of formation of thin films: the small molecules are normally deposited from the gas phase by sublimation or evaporation, but also by solution; the conjugated polymers can only be processed from solution like by spin-coating or

printing techniques. Some examples of polymers and small molecules are presented in Fig. 3.1.

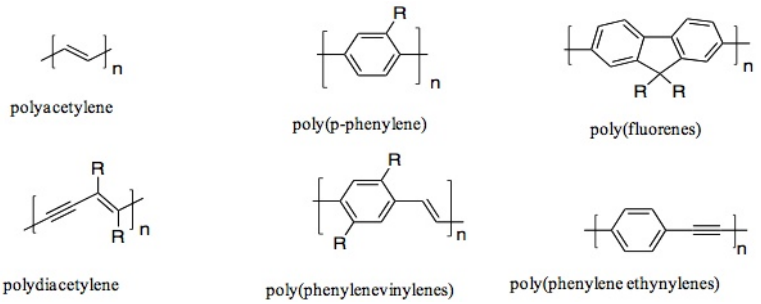

Fig. 3.1 - Different types of conjugated polymers, typically processed from solutions [**24**].

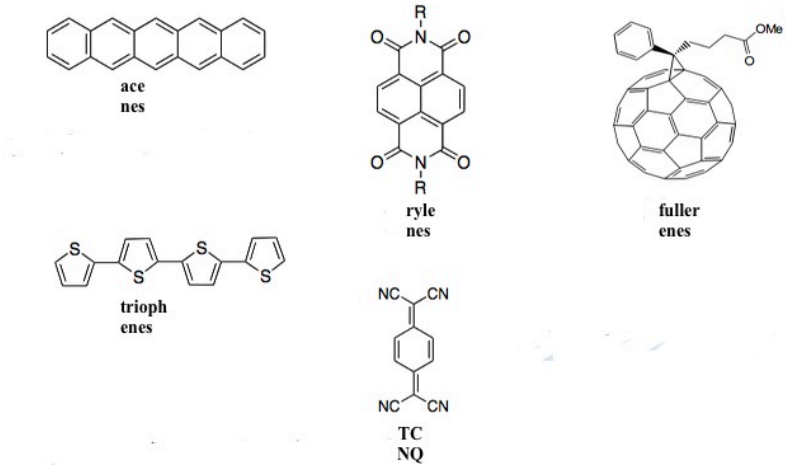

Fig. 3.2 - Different types of small molecules, typically processed by sublimation [**25**].

In general, the mechanisms ruling the charge transport in organic semiconductors are different from those operating in the conventional inorganic materials, such as silicon. The charge carrier transport mechanism in organic semiconductors is Hopping transport for polymer films. In well-ordered inorganics, such as a single-crystal Si, the delocalization of electrons over equivalent sites leads to a band-type mode of transport, with charge carriers moving through a continuum of energy levels in the solid. In organic materials, hopping between discrete and localized states of energy levels of individual molecules is the conduction mechanism, shown in Fig. 3.3.

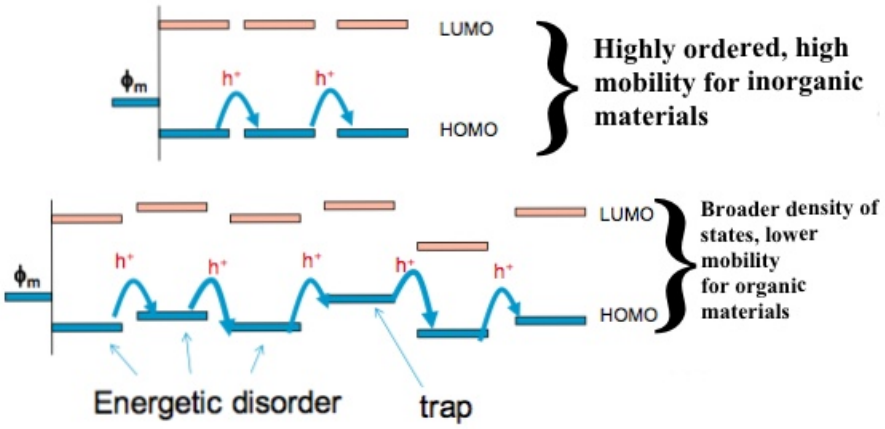

Fig. 3.3 - Energetic states for organic and inorganic material.

This way, the carrier mobility value (μ) is much lower in organic material than in the single crystal case. It is around 10^{-3}~$1\ cm^2/Vs$, while in crystalline Si carrier mobility can achieve values about $400\ cm^2/Vs$.

3.3 DEVICE ARCHITECTURE

In organic electronics, the term of MOSFET (Metal-Oxide-Semiconductor FET) is not suitable because of the gate dielectric type, which is not an oxide, but it is an insulator. The OTFT MISFET (Metal-Insulator-Semiconductor FET) has several structure variants and it is made of three main parts: an insulator, a thin semiconducting layer and three electrodes. Two of the electrodes, the source (S) and drain (D), are in direct contact with the semiconductor layer and provide the charge carrier injection; the third, the gate, is isolated from the semiconductor by the insulator.

The structure of the device depends on its fabrication, where the basic fabrication scheme consists of piling up thin films of the different elements. Since most organic semiconductors are fragile materials, the deposition of organic semiconductors on the insulator is much easier that the converse. This way, the majority of current OTFTs are built according to the bottom-gate architecture, which is divided in two alternatives, as illustrated in Fig. 3.4, bottom contact (BC) and top contact (TC) [**26**].

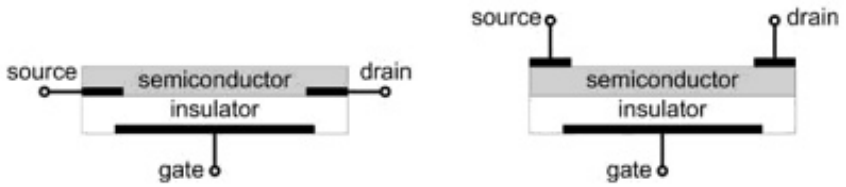

Fig. 3.4 - Top gated structure of organic thin film transistor: bottom contact (left) and top contact (right).

3.4 DEVICE OPERATION

Basically, the Thin Film Transistor operates like a capacitor. When a negative gate voltage (V_{GS}), for *p-type* semiconductor, is applied between gate and source terminals, charge carriers are electrostatically accumulated in the semiconductor at the interface with insulating barrier. When the gate electrode is biased positively, the channel region is depleted of carriers and the semiconductor operates in the depletion mode. Due to this field-effect, the charge carrier density in the semiconductor can be modulated in reversible way. Hence, the resistivity of the semiconducting channel compromised between the source and drain is a function of V_{GS}. This means that the current I_{GS} through the semiconductor (upon application of a source-drain field V_{DS}) can be varied over many orders of magnitude [**27**]. Since the TFT can be switched between a conducting and a non-conducting state, it is widely used as the basic building block of binary logic circuits.

Two different and complementary methods are commonly employed to characterize the electrical response of TFTs: either V_{GS} is kept constant and V_{DS} is swept (output curves, Figure 3.5 (a)) or V_{DS} is held constant and V_{GS} is swept (transfer characteristics, Figure 3.5 (b)).

The electrical characteristic of a transistor can be divided into two regions: linear and saturation regime. The transistor is told to operate in linear regime when the drain (V_{DS}) biases are much lower the gate (V_{GS}) voltages. Instead, the saturation regime takes place when V_{DS} becomes higher than V_{GS}. In the linear regime the current flowing between drain and source through the channel follows the Ohm's law being proportional to the drain and gate voltages. When the V_{DS}increases and approaches the gate voltage, the voltage at drain contact drops to zero, and the conducting channel is pinched off. At this point the I_{DS} becomes independent of the drain bias.

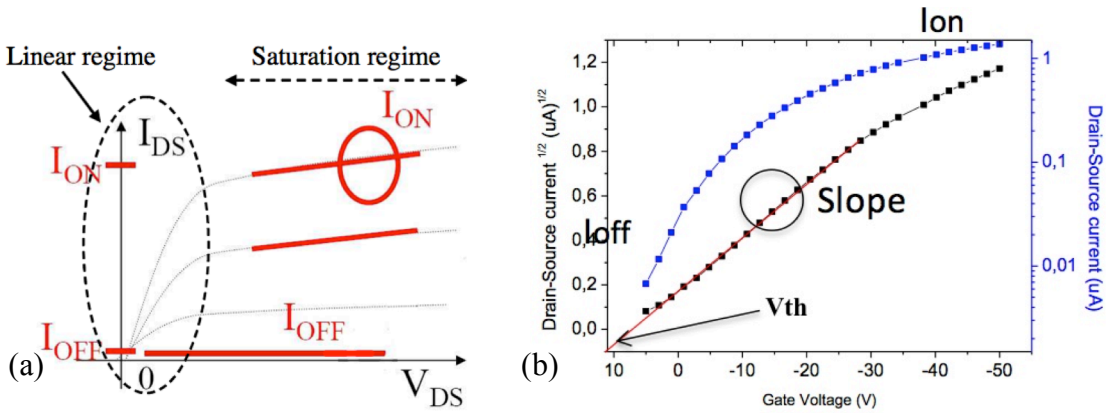

Fig. 3.5 - (a) output curve in an FET and (b) transfer curve.

Organic FET works in the *accumulation mode*, differently from the inorganic devices that operate in the *inversion mode*. The conduction mainly occurs, in the on-state, due to the layer of charge carriers which forms in the semiconductor within few angstroms from the insulator/semiconductor interface, and after the application of a suitable V_G. Thereby, OTFTs operate through the creation and elimination of a sheet of charge carriers at the gate dielectric/semiconductor interface. The basic operation is summarized in Fig. 3.6 [**28**].

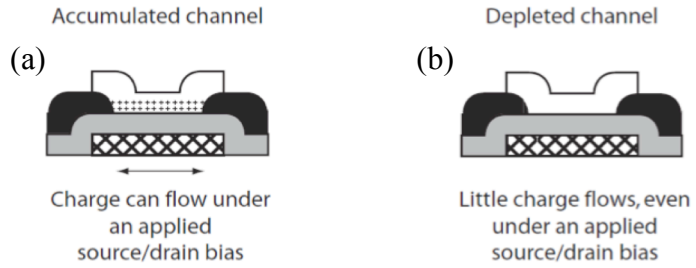

Fig. 3.6 - A traditional OFET design. (a) Sheet of charge, current can flow through the channel; (b) operating region (no sheet charge), the device is insulating and little current flows.

These charges are of the same type of the majority charge carriers responsible of the current in the off state. A small fraction of the total drain current is therefore determined by the free carriers in the semiconductor, which can be thermally generated or produced by unintentional doping. Despite this fundamental difference, the characteristic equations of the inorganic MISFET transistors can be applied, as a first approximation, also to an Organic MISFET.

In the linear regime, where $V_{DS} \leq (V_{GS} - V_{Th})$:

$$I_{DS} = \mu C_i \left(\frac{W}{L}\right)(V_{GS} - V_{Th})V_{DS} \quad (3.1)$$

and in saturation regime, where $V_{DS} > (V_{GS} - V_{Th})$:

$$I_{DS} = \frac{1}{2}\mu C_i \left(\frac{W}{L}\right)(V_{GS} - V_{Th})^2 \qquad (3.2)$$

The parameter L is the channel length of the transistor from source to drain in the direction of the current flow, W is the channel width of the transistor, C_i is the capacitance per unit area of the insulating layer, and μ is the field effect mobility.

One of the most important physical parameter defining the quality of the OFET electrical response is the field-effect mobility, μ [**27**,**29**,**30**,**31**,**32**], which is the drift velocity of the charge carriers flowing through the semiconductor when a unit electric field is applied. This parameter strongly affects the operation speed of the transistor and has a fundamental importance when fast logic circuits are desired. The mobility is also directly related to the switching time of the device. The slope of the $I_{DS}^{1/2}$ versus V_G is related to the mobility for the saturation region due to the square law relation. For the case of the lineal region, the slope I_{GS} versus V_G is related to the mobility.

Other important parameters are the I_{ON}/I_{OFF} ratio, which is the ratio between the current in the accumulation mode and the current in the depletion mode. The threshold voltage (V_{Th}) is the V_G corresponding to the opening of the conduction channel. The I_{ON}/I_{OFF} ratio is indicative of the switching performance of OTFTs, ratios of $10^4 - 10^6$ are suitable for most applications and can be reached by state-of-art OTFTs. All these parameters are shown in Figure 3.5.

Chapter 4

ELECTRICAL CHARACTERIZATION OF INVERTER AND NAND LOGIC GATES

In this chapter the electrical characteristics of simple inverter and NAND circuits are presented and discussed. The highest voltage gain measured was approximately -3. Under continuous operation, the gate-bias stress effect causes degradation of the gain. A NAND circuit was also fabricated and characterized. The dynamic response of the circuits is below 1 Hz.

4.1 INTRODUCTION

There are a number of relatively high performing circuits based on organic semiconductors. These include simple inverter [**33**], oscillators [**34**], logic circuits [**35**]. These circuits were achieved using vacuum processing methods or hybrid fabrication technologies where some of the layers were prepared from solution (spin-coating) while others were vacuum processed. This allows a more rigorous control of the dielectric/semiconductor interface. Furthermore is a relatively easy to use passivation layers to neutralize electrical active defects. There is a long history in selecting materials and processing methods to achieve a performance comparable with the amorphous silicon technology. However, these high performing devices are not cheap to produce. Their commercial success has been limited mostly because of the processing costs. Inkjet printing intends to offer a really low price production technology. However, for inkjet printed devices, the device optimization is still in its infancy. The materials and process recipes developed in other deposition methods are not directly transferable to printing because they rely on complex procedures and reactions in inert atmosphere. Furthermore, the number of printing parameters to be optimized is higher and a clear understanding of how the printing process and materials affects the electrically active defects is still lacking.

The number of circuits entirely fabricated by ink-jet printing is still limited. To the best of our knowledge only inverter circuits with a voltage gain of almost -20 have been reported [**36**].

In this chapter a fully ink-jet printed inverter circuit, using two p-type thin film transistors (OTFT) was fabricated and characterized.

4.2 EXPERIMENTAL

The design of the inverter logic gate is based on using one p-type TFT for logic control coupled with another p-type TFT connected as a diode acting as a load. This approach is used by application of a negative voltage (bias) at its gate (V_{SS}), as shown in Fig. 4.1.

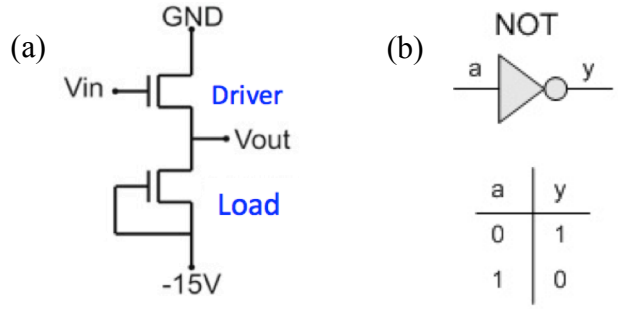

Fig. 4.1 - (a) Inverter circuit configuration; (b) Truth table

The advantage of the use of a TFT as a load is the implementation of a resistor without increasing the stack of materials. To get it, the TFT should be at the saturation region by short-circuiting the gate and source or drain. The resistor behavior is obtained from the resistance of the channel in saturation region. The resistance of channel in saturation region must be high enough to ensure a relation about several times more between drive and load transistors. As *L* is fixed by the technology, *W* must decrease in order to increase the resistance of the channel, and as consequence the ratio *W/L* will be lower. Thus, the *W/L* ratio of the drive transistors is always sized with a width several times bigger than the *W/L* ratio of the load transistors.

Individual transistor characteristics and inverter transfer characteristics were measured using a Keithley 6487 and a nano-voltimeter Keithley 2182 (input impedance >10 GΩ). Because of the extremely high output impedance of our OTFTs sometimes a semiconductor parameter analyser with an input impedance of 10^{16} Ω was used.

With the Keithley 2182, the inverter transfer characteristics could only be measured in the range of 10 V. This imposed a limitation on the bias voltages used to drive the inverters. Voltage swings higher than 12 V could not me measured.

Two production runs were used to fabricate the inverters circuits. The fabrication was carried out at the nodes of the *TDK4PE* project. Namely at *ENEA* and at *TUC*.

They will be refereed as RUN2 and RUN4. RUN2 uses the FS0027 semiconductor and RUN4 uses the FS0096 ink formulation as semiconducting material.

4.3 RESULTS AND DISCUSSION

4.3.1 FS0027 INVERTER

The OTFTs were arranged into the substrates into a configuration where they can easily be wired to make, inverter, oscillator and logic gates circuits. In the RUN2 foil (Fig. 4.2) fabricated at *ENEA*, the transistors are organized in four rows, where each of them have 11 OTFTs, with two fixed aspect ratios *W/L* (where *W* and *L* are the channel width and length, respectively). The values for the unipolar saturated load transistors are 5000/40 μm and for the driver (input) transistors, *W/L* are 40000/40 μm.

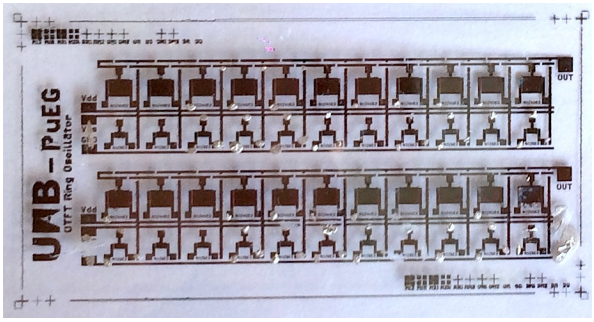

Fig. 4.2 - Arrays of transistors with two distinct sizes. They were pre-wired to make inverters and oscillators.

The results were obtained connecting two OTFTs (oscillator 2 inverter 10) based on FS 0027 semiconductor (see Fig. 4.3). The used inverter had a driver/load ratio of 8. Several inverter configurations were tested, but the best voltage gain was obtained with the configuration presented in Fig. 4.1 (a).

The driver and load OTFT I-V characteristic curves are presented in Fig. 4.4, and the transfer curves measured in linear region ($V_{DS} = -1V$) can be seen in Fig. 4.5.

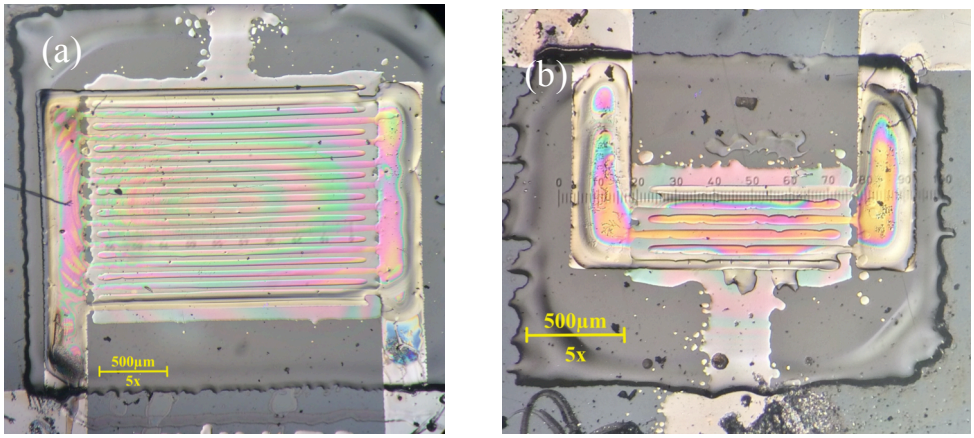

Fig. 4.3 – Optical microscope image. (a) Driver OTFT; (b) Load OTFT

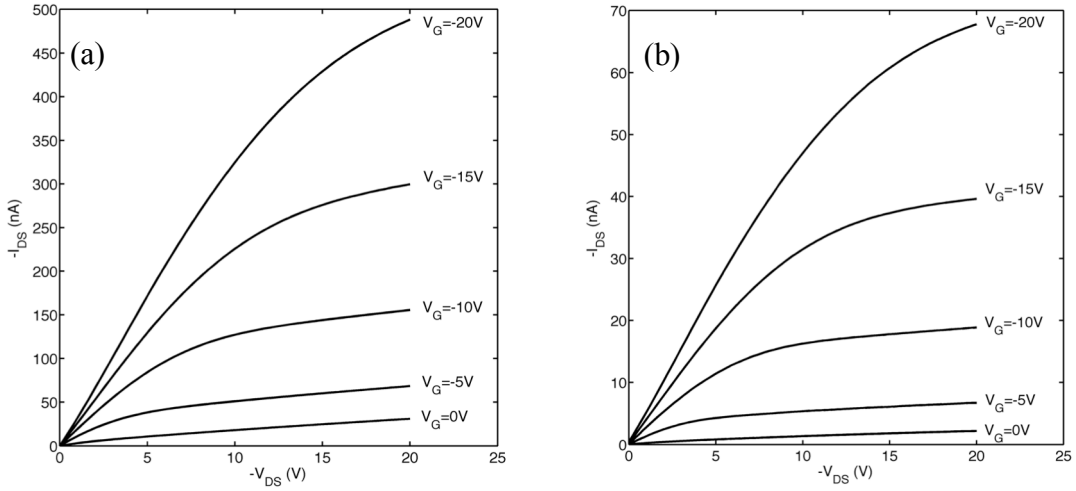

Fig. 4.4 – Output characteristics of the OTFT, (a) large area; (b) small area. The ratio between OTFTs areas is 8.

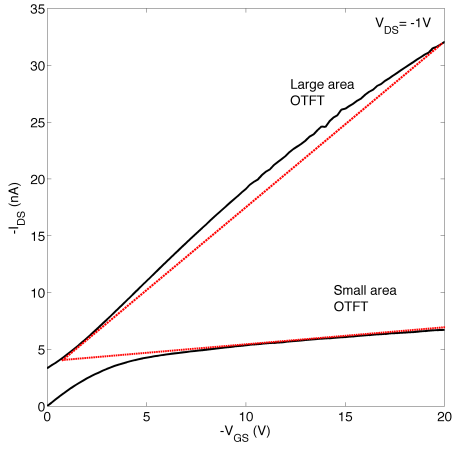

Fig. 4.5 – Comparison between the transfer curves measured in the linear region ($V_{DS} = -1V$). The dashed red line is a guide to the yea to estimate the threshold voltage.

The inverter circuit was operated under relatively low voltages ($V_{IN} = [0 - 7]V, V_{DD} = -15V$) in a dark chamber at ambient temperature. The input ramp was generated using Keithley 487 voltage source. The output voltage values were read by Keithley 2182 Nanovoltmeter.

Fig. 4.6 shows the transfer curve of the inverter made using the TFTs on Fig. 4.4 and Fig. 4.5. A full hysteresis loop, when V_{IN} was cycled in the range [0; -7] V. As the driver TFT moves into accumulation, its resistance decreases and V_{OUT} moves from a high voltage towards a value limited by the minimum resistance of the driver TFT. The maximum value of output voltage is determined by the resistance of the load TFT, which increases with time due to gate-bias stress.

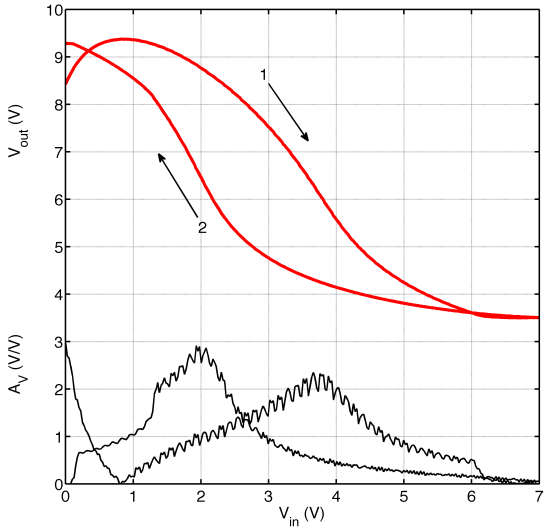

Fig. 4.6 – Output transfer curve of an inverter circuit and voltage gain.

The increase of load OTFT resistance, that represents the effect of gate-bias stress and lowers gain value, is illustrated in the Fig. 4.7 and Fig. 4.8, which represent the response of application of 3 consecutive input ramps to the inverter.

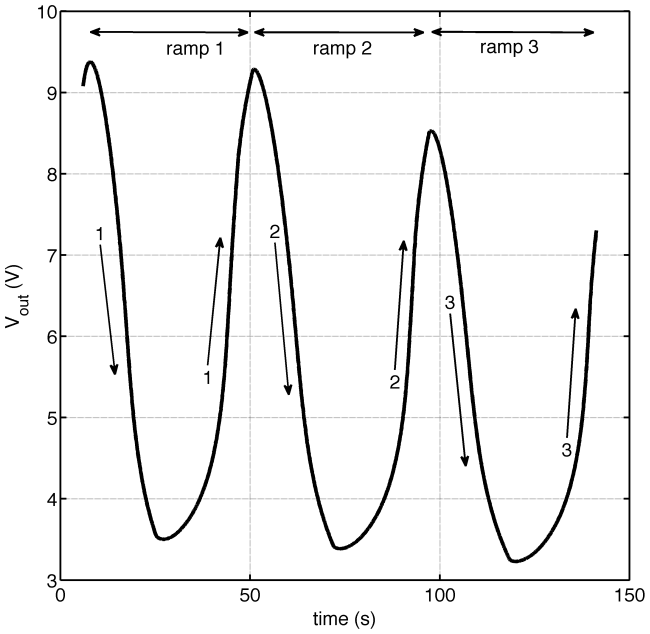

Fig. 4.7 – Time dependence of V_{OUT}.

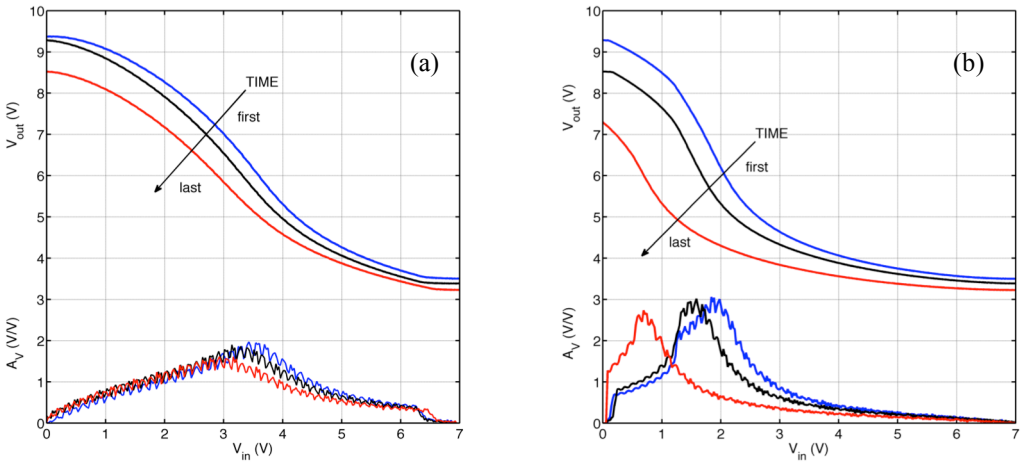

Fig. 4.8 – V_{OUT} *vs* V_{IN} and gain Av, (a) forward path voltage scans and (b) return path voltage scans.

Several consecutive inverter transfer functions are presented in Fig. 4.7 The amplitude of the gain decreases with time from value of 2 to 1.5 in forward path voltage scans (Fig. 4.8 (a)). In the return path, presented in Fig. 4.8 (b), the decrease of gain is subtler, going from value of 3 to 2.7, approximately.

Because of this degradation, the transistors are not capable of providing a long-term inverter characteristics. The implementation of an oscillator circuit from a cascade of inverters will not be feasible.

4.3.2 FS0096 INVERTER

OTFTs fabricated in RUN4 were made at *TUC* installations. In this run, the aspect ratio *W/L* of transistors was varied, providing four different types of driver/load ratios (8, 10, 12, 16). See Fig. 4.9. Furthermore the semiconductor used is the FS 0096.

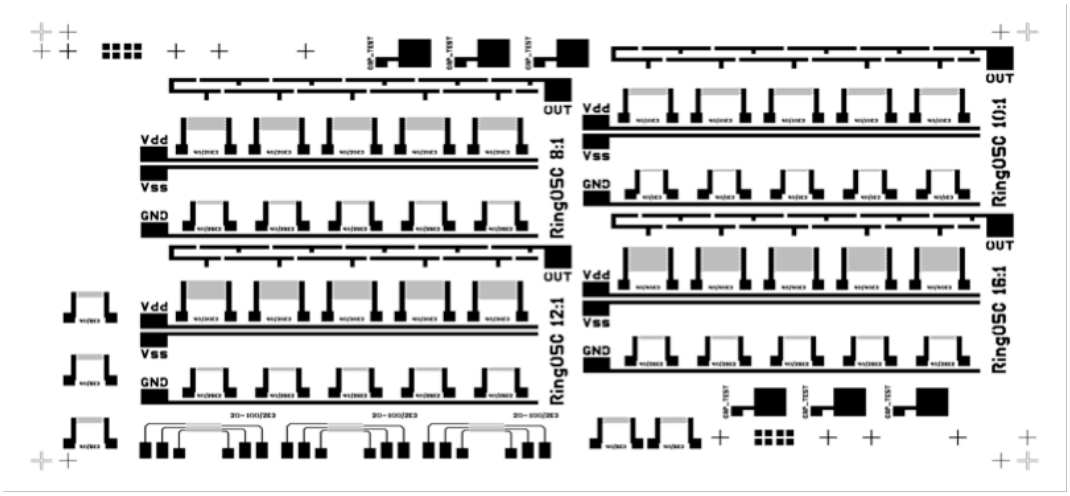

Fig. 4.9 - Design with arrays of individual OTFTs with different W/L ratios.

The I-V characteristic of the selected OTFTs, are shown in Fig. 4.10. The ratio between areas is 12.

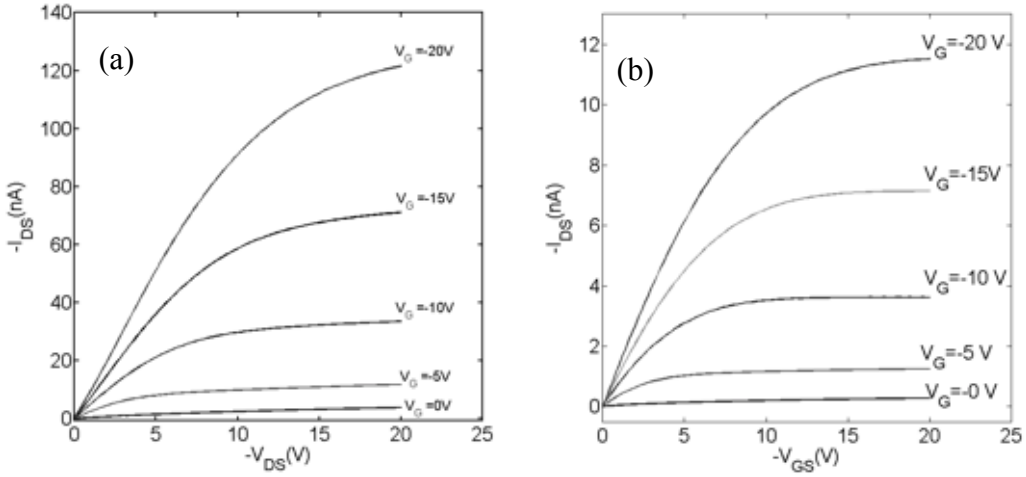

Fig. 4.10 - Output characteristics of the OTFT, (a) large area and (b) small area OTFT. The ratio between OTFTs areas is 12.

Fig. 4.11 compares the transfer curves measured in the linear region $(V_{DS} = -1V)$. The threshold voltage (V_{Th}) is approximately -2 V for both transistors.

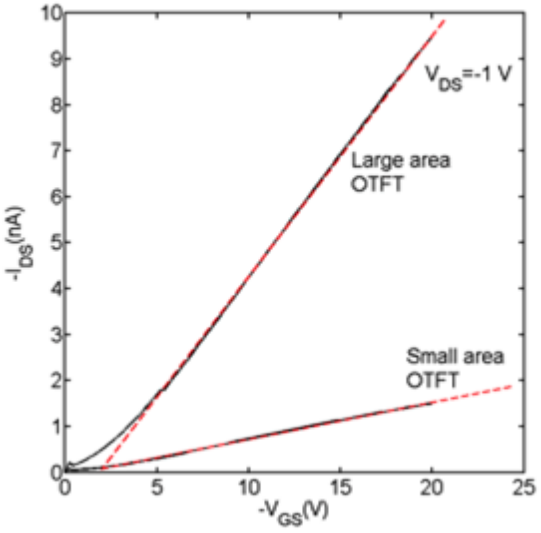

Fig. 4.11 - Comparison between the transfer curves measured in the linear region ($V_{DS} = -1V$). The dashed red line is a guide to the yea to estimate the threshold voltage.

The static transfer characteristic of the inverter is shown in Fig. 4.12. The output voltage swing is 10 V with V_{DD} = −20 V. The gain is close to 2.8. High and low noise margins are respectively N_{MH} =4.5 V and N_{ML}=1.8 V.

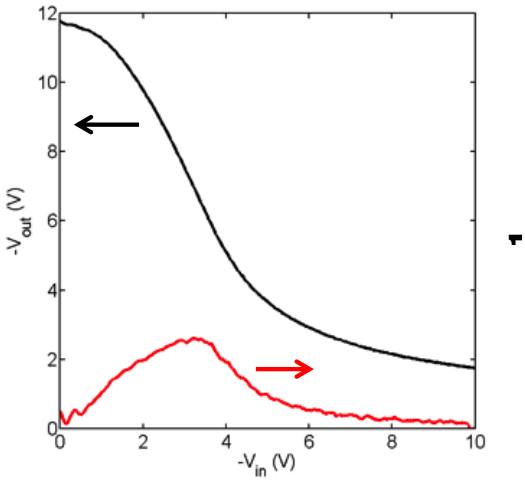

Fig. 4.12 - Inverter transfer characteristics (black solid line) and gain (red line), $V_{DD} = -20\ V$ and $V_{IN} = [0;\ -10]$V with a tamp speed of 0.1V/s. The drive/load ratio is 12.

The inverter transfer characteristic do not change with time when driven by a periodic waveform. This confirms that the threshold voltages of both TFTs (driver and load) are relatively stable. This stability is confirmed when the inverter transient response is measured. Fig. 4.13 shows the response of an inverter to a 10 V input square wave ($V_{DD} = -10\ V$). The driver transistor is able to pull down the output to −1.3 V and the load transistor pulls up the output on to −4.9 V. No degradation in the voltage swing was observed.

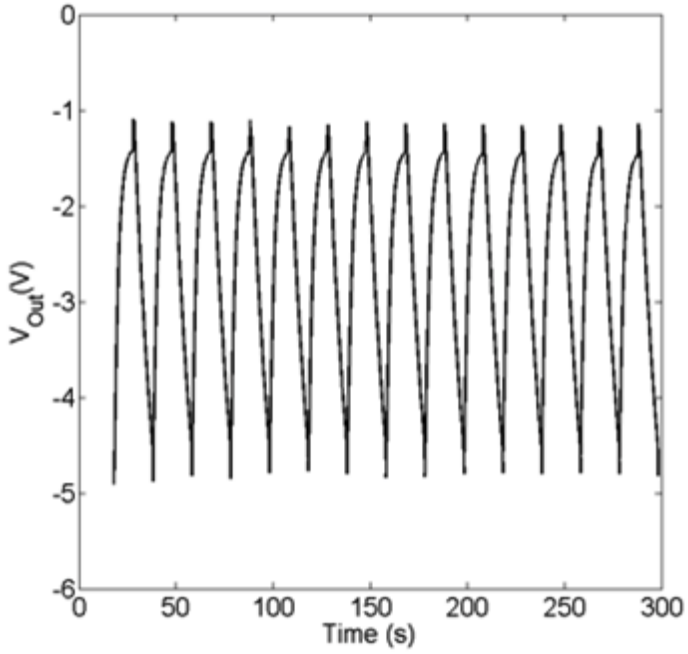

Fig. 4.13 - Inverter response to an input square wave ($V_{DD} = -10\ V$).

The application of successive square waves to the inverters shows that there is a small hysteresis effect. The inverter gain is smaller when it switches between low (-1.7V) and high (-11.5V) state. The process repeats periodically and generates a slightly asymmetric waveform as shown in Fig. 4.14.

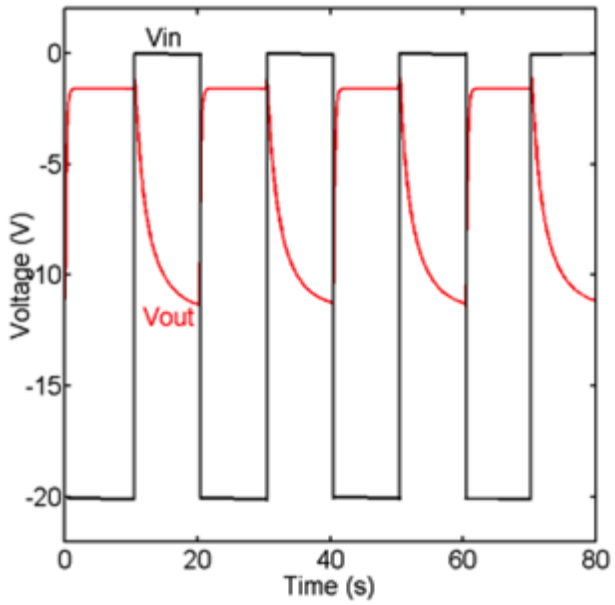

Fig. 4.14 - Transient response of the inverter ($V_{DD} = -20\ V$).

This asymmetry is caused by the different switching process because of the inner nature of the pseudo-pMOS circuit, the rising transitions of the output voltage (from '0' to '1') will be much faster that falling transitions (from '1' to '0'). This behaviour is due

to the fact that load OTFTs (discharging path) are worse conductors than drive transistors (charging path). The slow time can be comparable with the time length used to record the inverter transfer function. A voltage ramp with speed of 0.1V/s was used, therefore, it only takes 20 seconds to complete a voltage ramp loop [0; -20] V.

The circuit performance is not affect by threshold voltages instabilities (gate-bias stress). Thus in spite the OTFTs used to make these circuits are not encapsulated and been stored in ambient atmosphere laboratory for several months, these findings show that all-inkjet printed OTFTs are robust enough to make circuits.

4.3.3 NAND LOGIC GATE

In order to implement a NAND logic gate, it is necessary to add another OTFT to the inverter circuit (Fig. 4.1 (a)), which will create a possibility of another input. The used circuit and the truth table are presented below.

(a)

NAND Gate		
V_{IN1}	V_{IN2}	V_{OUT}
0	0	1
0	1	1
1	0	1
1	1	0

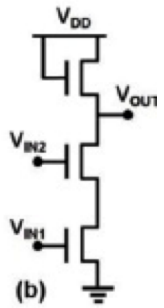

Fig. 4.15 - (a) NAND gate truth table, (b) NAND gate circuit.

Another OTFT was added to the previous inverter circuit and NAND logic gate was implemented.

The measured response of the NAND gate to square wave input signals V_{IN1} and V_{IN2} is shown in Fig. 4.16. As expected, V_{OUT} follows the truth table for a NAND gate (figure 4.15.(a)), i.e., remains high (−6 V) except when both inputs are high (−10 V).

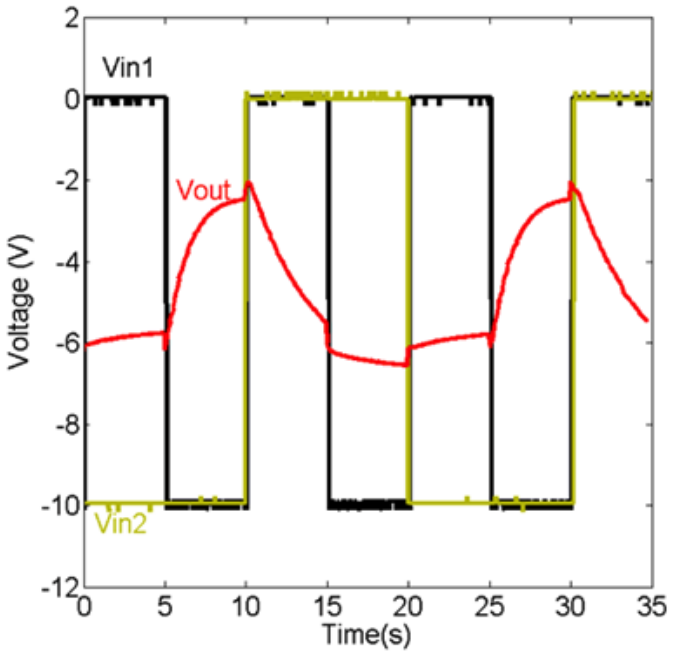

Fig. 4.16 - Response of NAND logic circuit, input square wave frequencies are 0.1Hz (V_{IN1}) and 0.2 Hz (V_{IN2}).

4.4 CONCLUSIONS

Inverter circuit and a NAND logic gate were fabricated. Two different runs were used. The maximum gain reached is -3. This is enough to make oscillators. Our findings show that higher gains are possible if the voltage range is extended. However this is not possible in our laboratory due to limitations of the instrument input impedance.

Comparing inverters made with different semiconductors, we found that the inverters using the FS0027 semiconductor show a relatively higher voltage gain degradation under continuous operation. Inverters using the FS0096 are relatively more stable. The reason may lay in slightly different processing methods because they were produced in different laboratories. The major limitation of the circuits is their dynamic response. They can only operate below 1 Hz. We believe this is due to a very large parasitic capacitance between the gate and source and drain terminals.

Chapter 5

PARAMETER VARIABILITY ON ALL-INKJET PRINTED ORGANIC TFTS

In this chapter, the variability observed in the transistor parameters, such as mobility, threshold voltage and on/off ratio are discussed. Intrinsic sources of variation caused by materials, processing, and handling, variations caused by a bad analysis of the data and finally variability caused by bad transistor design are also analysed and discussed. As a result of this study, the transistor layout was optimized to minimize parasitic effects such as lateral conduction and fringing. It is shown that by using a new pattern design the variability in mobility is minimized.

5.1 INTRODUCTION

Process variations present during transistor fabrication lead to a certain variability on the resulting transistor parameters. Variations between OTFTs had been a well-known problem, more acute than in silicon-based technologies by an inherently much higher parameter spread. Reasons for that, include, irregular morphology of the semiconductor, difficulty in controlling the precise dimensions of OTFTs, mobile trapped charges in the dielectric, uneven material deposition, roughness of the semiconductor-gate dielectric interface which leads to mobility variations between the different transistors.

The large transistor variability poses a serious challenge to the cost-effective utilization of organic analog circuits. Meeting this challenge requires comprehensive and efficient approaches for variability characterization and minimization. Accurate and efficient characterization of the different types of variation requires a large number of measurements on a variety of devices, layout styles, and environments. Data on transistor variability was previously reported by the Bao group [**37**]. Wei Xiong concluded that the variability observed prohibits the use of their OFETs in configurations that rely on precisely matched currents, as for instance current-steering D/A converters. The other group that has raised the issue of transistor variability is the IMEC group (Paul Heremans). Recently, this group reported that the methodology used in CMOS technologies to account for local parameter variations and transistor mismatch can be transposed to organic thin-film transistor technologies [**38**]. In general,

considerable parameter variations have been reported for organic thin-film transistors [**39**,**40**,**41**,**42**,**43**,**44**,**45**]. These variations find their origin in the organic materials employed and the rather immature printing, technology. They have an impact on one or more parameters of the saturation current equation of thin-film transistors (Eq. (5.1)).

$$I_{DS(sat)} = \frac{1}{2}\mu \frac{\epsilon_0 \epsilon_r}{d} \frac{W}{L} (V_{GS} - V_{Th})^2 \tag{5.1}$$

where V_{Th}, W, L, μ, ε_r and ε_o and d have their usual meaning.

Interesting, not all parameters affect the transistor current on the same way. Variations in the threshold voltage V_{Th} affect the saturation current of the transistor quadratically, while variations in μ, W, L, and d, influence the saturation current only linearly.

This chapter covers a study of parameter variability in all-inkjet printed transistors. It is organized in the following way; first look is based on how the transistor parameters depend on the printed active area. Next, it is shown that parameter extraction can be wrong, if the date is not proper corrected for parasitic off-state current. The strong dependence of the parameters on the active area indicated that the transistor design used was affected by lateral conduction. A new transistor layout was tested showing that the variability can be minimized.

5.2 RESULTS

Studies of variability require a large amount of TFTs. This study made use of 4 foils with TFTs as show in Fig. 5.1. Each foil had 44 TFTs. Two different sizes were available. Large area TFTs have L= 40 μm and W=4 cm. Small area TFTs have L= 40 μm and W=0.5 cm. Two types of organic semiconductors were used, the FS0027 and the FS0096. Not all the TFTs were working. The yield of working TFTs varies from 90% to 27% depending on the foil.

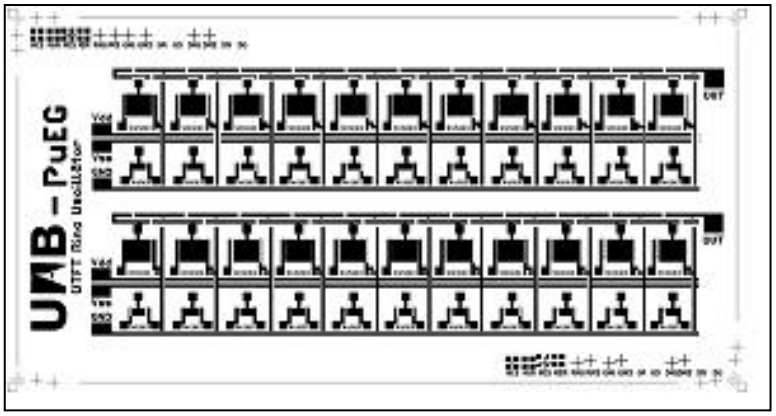

Fig. 5.1 - Transistor layout used for this study. Large TFT has have L= 40 μm and W=4 cm. The small area TFTs have L= 40 μm and W=0.5 cm.

5.2.1 THE EFFECT OF THE PRINTED AREA ON THE TFT PERFORMANCE

The printed active area has a strong influence of the TFT parameters. It affects charge carrier mobility and on/off ratio.

Fig. 5.2 shows that the mobility is always higher in large area TFTs. The threshold voltage is also higher in large area TFTs as show in Fig. 5.3. Finally, small area TFTs tend to have a better on/off ratio (Fig. 5.4).

This means that the TFT parameters do not scale with the active area. It is reasonable to assume that both polymer and dielectric layer thickness depends on the printed area. Shortly after printing, there are a number of phenomena, such as surface tension, viscosity and evaporation rate that determine the shape of the drops and how they organize to produce a thin film. This liquid re-organization may affect the final film thickness.

A convenient method to inspect for changes in layer thickness is capacitance measurements. Capacitance measurements in a transistor can be performed by connecting it as a capacitor. Source and drain terminals are shorted. The capacitance as a function of the voltage was measured between the gate terminal and the short-circuited drain and source terminals. The measured capacitance is proportional to the geometrical capacitance of the two layers (dielectric and semiconductor) in series. The measurements are shown in Fig. 5.5 for the two transistor areas. The high capacitance of large area TFTs show that the corresponding printed layers are thinner. The electric field will be higher across thinner dielectrics and will give rise to an apparent higher

mobility. Therefore, is reasonable to assume that the higher mobility estimated in large area TFTs is in reality an artifact caused by a thinner dielectric layer.

The observation that larger printed areas are thinner was also confirmed by optical measurements carried out at one of the partners in the project (ENEA).

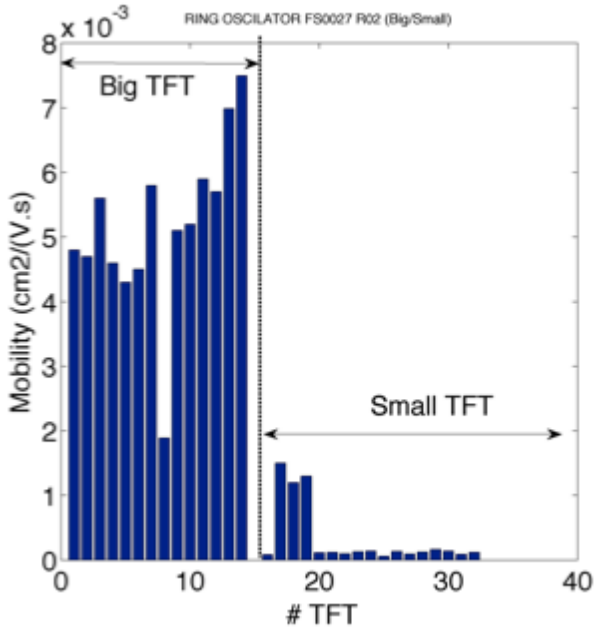

Fig. 5.2 - The effect of the active area on the charge carrier mobility as extracted from transfer curves measured in saturation. The semiconductor is the FS 0027 for the foil R02. Large TFTs have L= 40 μm and W=4 cm. The small area TFTs have L= 40 μm and W=0.5 cm.

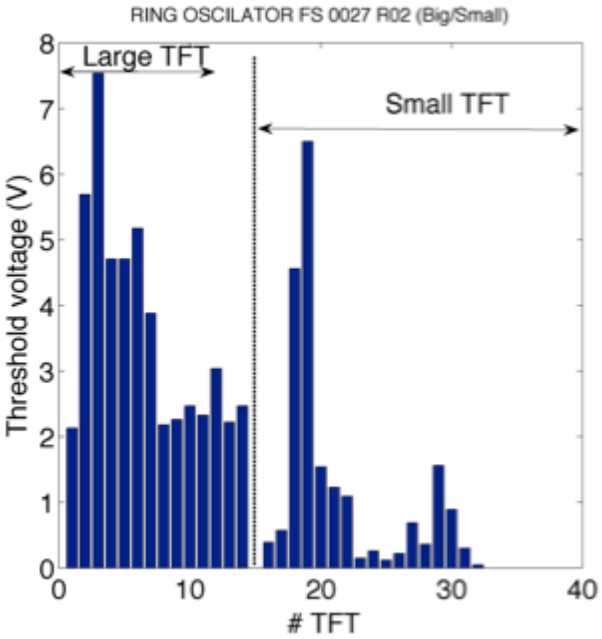

Fig. 5.3 - The effect of the active area on the threshold voltage. The semiconductor used is the FS0027.

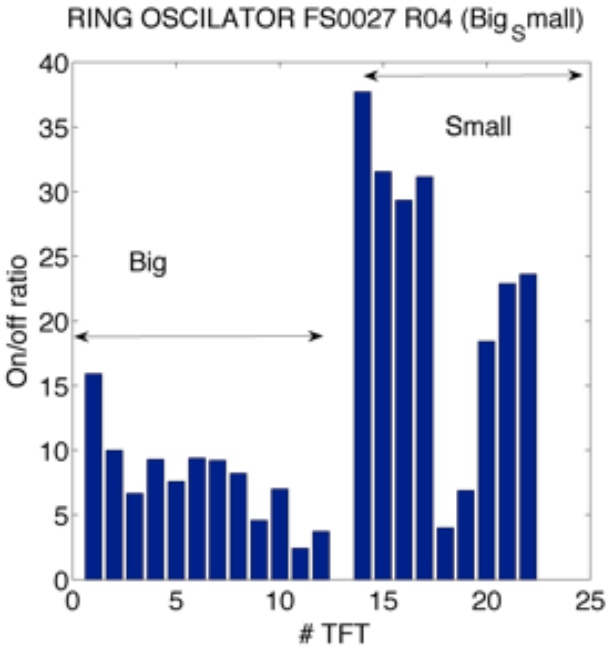

Fig. 5.4 - The effect of the active area on the on/off ratio as extracted from transfer curves measured in saturation. The semiconductor is the FS 0096.

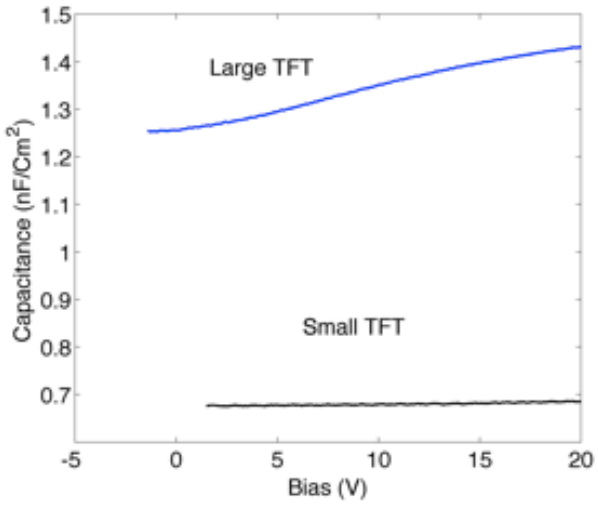

Fig. 5.5 - Capacitance-voltage plots for large and small TFTs. The semiconductor is the FS 0027. The transistor is connected as a capacitor. The procedure is described in the text.

5.2.2 PARASITIC EFFECTS CAUSED BY FRINGING AND LATERAL CONDUCTION

In this section, the way how parasitic effects caused, for instance, by the presence of a off-current can introduce errors in TFT parameter extraction is discussed. Furthermore, it is shown that the data analysis reveals the existence of parasitic effects caused by surface later conduction.

In order to study variability on OTFT parameters, the transfer curves of transistors produced in identical conditions and with the same active area were analysed. Fig. 5.6 shows a set of transfer curves. Apparently, there are variations in the off-current, in the threshold voltage as well as on the field-effect mobility.

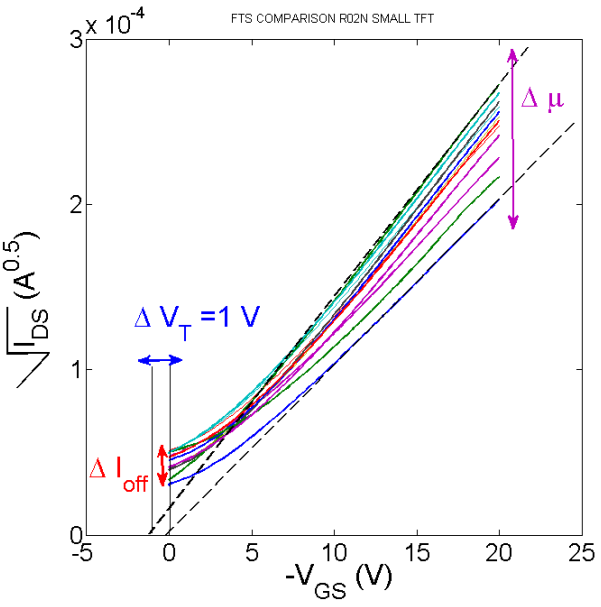

Fig. 5.6 - Set of transfer curves used to inspect for variability in an identical set of OTFTs. The OTFTs have a small active area, *W*=5000 μm *L*=40 μm.

When the transfer curves are corrected for the off-current, the variability on the threshold voltage becomes residual. This is shown in Fig. 5.7.

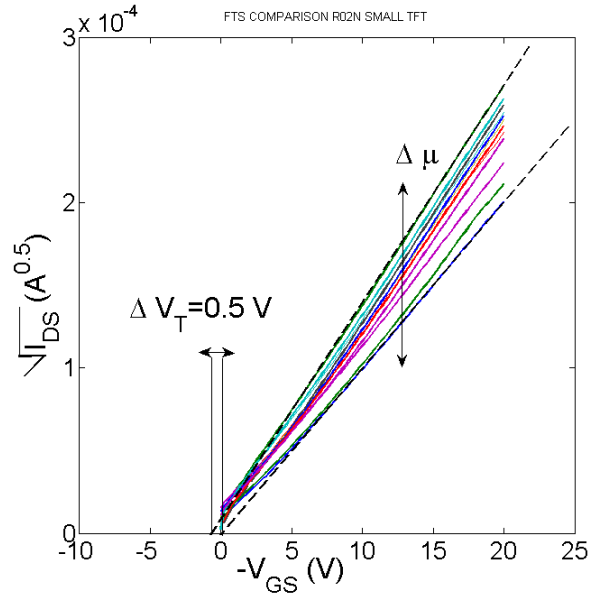

Fig. 5.7 - Set of transfer curves after removing the off-current. The variability on threshold voltage becomes residual.

After correction for the off-current only the mobility shows a dispersion. However, the application of the same correction procedure to a large area OTFT (*W*/*L*= 40.000 μm /40 μm) shows no variations on the mobility. Indeed, all the transfer curves run parallel to each other. This is shown in Fig. 5.8.

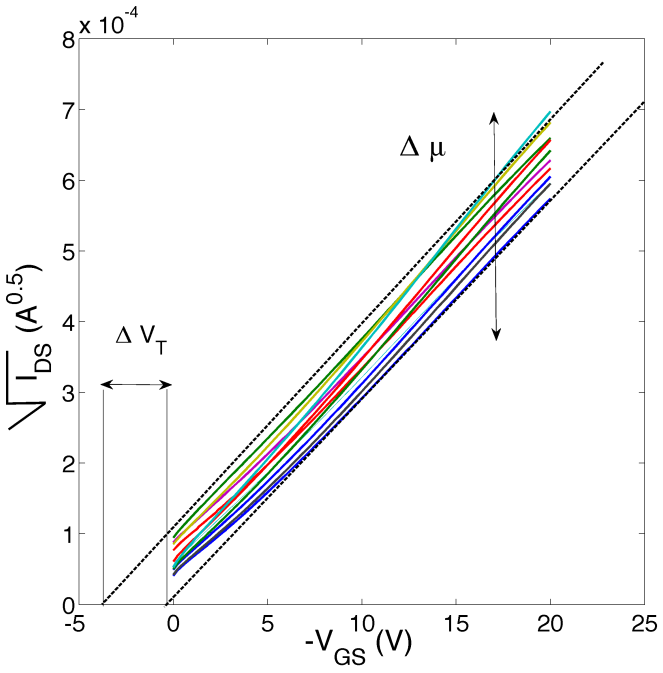

Fig. 5.8 - Transfer curves measured in an identical set of OTFTs with a large area (*W*=40.000 μm *L*=40 μm).

The fact that for small are TFTs, the mobility varies with the gate-bias suggests the presence of parasitic current which distorts the measurements.

5.3 DISCUSSION

It is well know that OTFTs are susceptible to a parasitic sheet conductance in the regions outside the main channel. This is because the area the semiconductor exceeds the border of the interdigitated S/D fingers. This parasitic source–drain fringe current can flow between the tip of one electrode and its counter-electrode (see in Fig. 5.9 (a)). The green layer represents the semiconductor area, and the red tracks are the source and drain electrodes. Due to the full coverage of electrodes with semiconductor layer, including their edges, when applied an electric field on the drain and source contacts (including gate electrode also), a parasitic artifact emerged. The black arrows represent the expected flow of charges between the drain and source electrodes, while the blue arrows represent the lateral current fringing parasitic effect. As the channel width (*W*) decreases the parasitic current provides a greater fraction of the total device current.

This additional parasitic current will increase the apparent field effect mobility. Since it depends on *W,* an artificial variability on mobility (increase in mobility for small *W*) will be also introduced. Furthermore, this parasitic contribution will increase with the electric field. The higher the gate bias, the higher the parasitic source–drain fringe current. This can introduce an apparent increase in the mobility with increasing gate bias.

To reduce this parasitic contribution a new layout for OTFT was implemented. In this new layout the polymer area is kept confined to a region inside the pattern of the metal interdigitated electrodes (see Fig. 5.9 (b)).

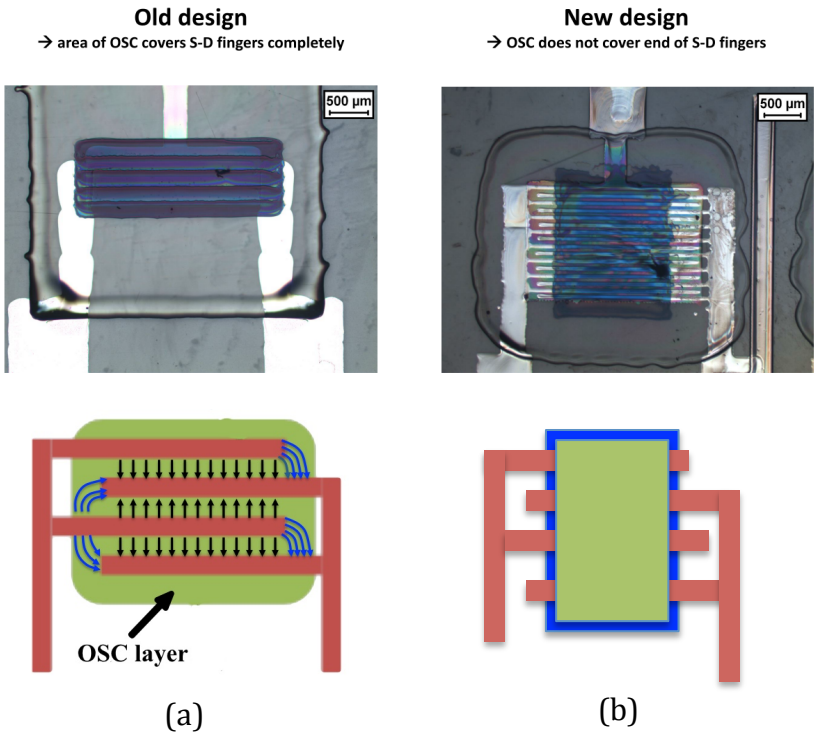

Fig. 5.9 - (a) Layout design susceptible to parasitic fringing effects. (b) The new layout design to reduce fringing effects. The blue square is the dielectric area and the green square is the semiconductor area.

The transfer curves (in saturation) were measured for a set of identical transistors with a small active area but now fabricated using the new OTFT design to reduce fringing (see Fig 5.9 (b). The transfer curves are shown in Fig. 5.10.

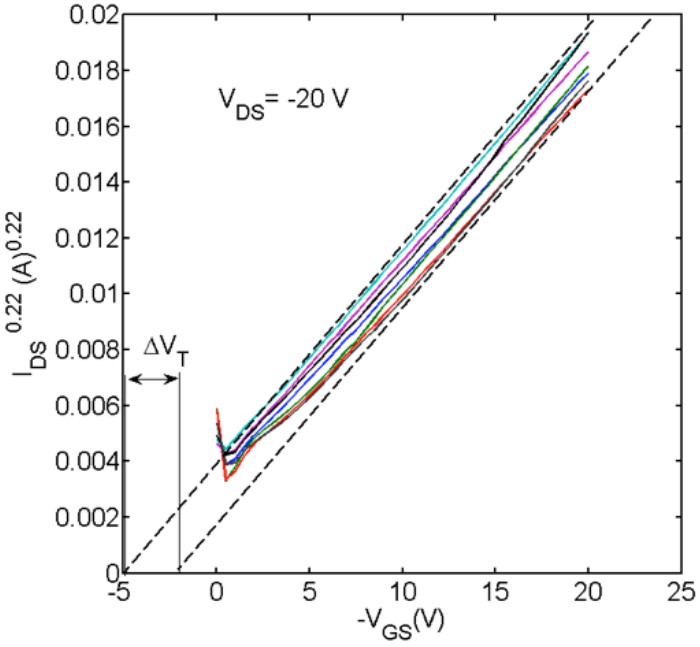

Fig. 5.10 - Set of transfer curves measured in an identical set of relatively small area OTFTs. The off-currents were removed. A correction γ factor was used to linearize the curves. A γ factor of 2.3 was used.

These transfer curves do not follow the square root law; therefore they were linearized using a correction γ factor of 2.3. This means the curves are plotted to a power law (V_{GS} vs. $I_{DS}^{1/(2+\gamma)}$). The transfer curves were also corrected for the off-current. Interestingly, all the transfer curves run parallel to each other. Although, the transistors have a small area, the mobility remains constant.

The comparison between Fig. 5.7 and Fig. 5.10 shows clearly that the variability on the field effect mobility is an artifact caused by a parasitic fringing effect.

5.4 CONCLUSIONS

TFT parameters do not scale with the printed area. Major discrepancies exist in mobility and in the on-off ratio as well on the threshold voltage. One of the reasons for this discrepancy comes from variations on the dielectric thickness. Large area TFTs have thinner dielectrics. Polymer layer thickness was inspected using optical and capacitance measurements.

Parasitic effects such as off-state currents distort the data and can introduce an artificial dispersion. Bad transistor design cause parasitic lateral conduction, which contributes to variability on the TFT parameters.

Chapter 6

OPERATIONAL STABILITY AND AGEING EFFECTS ON ALL-INKJET PRINTED ORGANIC TFTS

This chapter reports about the use of a printed pentafluorothiophenol layer on top of the dielectric surface as a passivation coating to improve the operational stability of all-ink-jet printed transistors. Transistors with bottom-gate structure were fabricated using cross-linked poly-4-vinylphenol (c-PVP) as dielectric layer and an ink formulation of an amorphous triarylamine polymer as semiconductor. The resulting TFTs had low turn-on voltage (V_{th}< |5V|) and a mobility ≈ 0.1 $cm^2/(V \cdot s)$. Long exposure to the ambient atmosphere causes an increase in the threshold voltage strongly dependent on the used semiconducting ink formulation.

6.1 INTRODUCTION

Inkjet printing is a desirable manufacturing technology for low-cost, large-area and flexible organic electronic circuits. This fabrication technique uses a small amount of materials, it is a mask-less additive method and well-suited for applications that require heterogeneous integration of different materials and functional devices on the same substrate [**46**].

Organic based thin transistors (OTFTs) entirely fabricated by inkjet have been reported [**47**,**48**,**49**,**33**,**50**,**36**]. Field effect mobility of $0.15 cm^2/(V \cdot s)$, on/off ratio of 10^5 and inverter circuits with a voltage gain of almost -20 demonstrate that the technology is progressing [**36**]. This performance has been achieved by improving the dielectric/semiconductor interface using interlayers. For vacuum processed and spin-coated devices, hydrophobic coatings and self-assembled monolayers have been devised and optimized to prevent or neutralize traps on the dielectric surface.

In presented device, the dielectric surface is coated with a printed pentafluorothiophenol (PFTP) layer. This molecule is commonly used to tune the energetic barrier at the metal/semiconductor interface [**51**]. The final results suggest that it also neutralizes the traps on the dielectric surface. This coating improves the operational stability of the OTFT by one order of magnitude.

In addition to the operational stability, the effects of ageing are studied. OTFTs left for long periods of time to the ambient atmosphere undergo a decrease in the overall performance. This degradation is dependent on the semiconductor ink formulation. These results are discussed in terms of used solvents and their evaporation rates, which may affect the film morphology and their permeability to atmospheric species.

6.2 EXPERIMENTAL

In terms of manufacture of the presented devices, a 125-μm-thick PEN film (Teijin DuPont Films, Teonex® Q65FA) was used as flexible substrate. Prior to printing, the PEN foil was cleaned with an ethanol impregnated clean-room wipe for some seconds. Then the cleaned foil was dried with nitrogen in order to remove remaining particles from the substrate. For printing, a Dimatix Materials Printer 2831 (DMP2831, Fujifilm Dimatix Inc.) was employed. The printer was equipped with 10 pL nominal drop volume, printheads having 16 nozzles each with a diameter of about 21.5 μm. At first, the gate was deposited on the PEN substrate using 20% weight silver nanoparticle ink from Sunchemical (EMD5603). The deposited layer was sintered at 130 ºC for 15 minutes on hotplate. The measured thickness of the resulting layer of the gate was about 450 nm. In the second step a solution of poly-4-vinylphenol (PVP) was printed on top of the gate electrode and cross-linked at 150 ºC for 40 min on a hotplate. The dielectric ink consisted of PVP (Mw ~25000, Sigma Aldrich Co.) and poly (melamine-co-formaldehyde) (Mn ~ 432, 84 wt%, Sigma Aldrich Co.) as cross-linking agent that were mixed in propylene glycol monomethyl ether acetate (PGMEA). The dielectric layer thickness was about 1μm. Next, interdigitated source-drain electrodes were printed using silver ink on top of the dielectric layer applying the same post-treatment described for the gate layer. For the deposition of the passivation layer, PFTP was dissolved in mesithylene at very low concentration. This ink formulation was printed on the pre-manufactured stack covering both the channel area and S/D fingers and exposed to ambient condition for some minutes.

Finally, the organic semiconductor ink was deposited by using the same pattern of PFTP and cured on a heating plate at 100 ºC for 15 min. The polymeric semiconductor inks were provided by Flexink and designated here as FS0027 and FS0096. FS0027 is triarylamine amorphous polymer dissolved in tetralin and the FS0096 is an ink formulation in mesitylene of a conjugated aromatic ordered polymer. The organic

semiconductor was estimated to have a thickness of around 1µm. Fig. 6.1 (a) shows the layer-by-layer manufacturing process for the bottom gate bottom contact all-inkjetprinted OTFTs. The OTFT device geometry was defined by the layout data of inkjet printing. The channel length (*L)* is 40 µm and channel width (*W)* is 4 cm. Fig. 6.1 (b) shows the optical image of a printed OTFT based on the FS0096 ink.

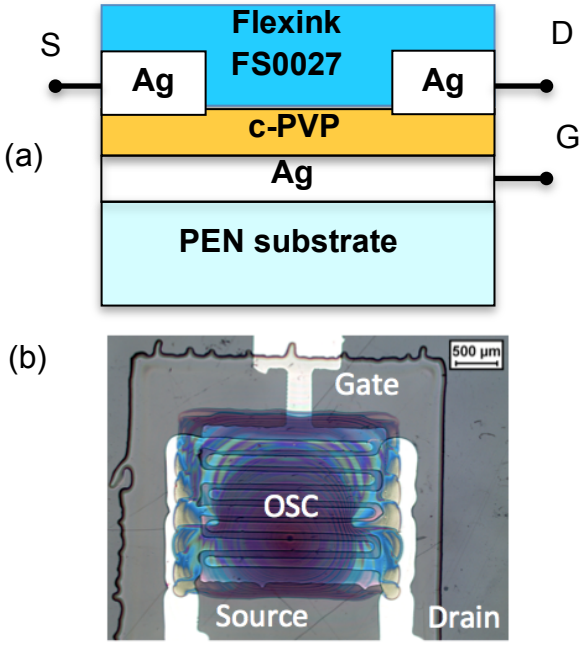

Fig. 6.1 - (a) Schematic diagram showing the OTFT structure, (b) Microscopic image of a inkjet printed OTFT on the flexible PEN substrate. The organic semiconductor (OSC) is the FS0096 ink formulation.

Electrical measurements were obtained using a Keithley 487 picoammeter/voltage source. All measurements were carried out in vacuum. For ageing studies, the OTFTs were stored in dark and ambient conditions.

6.3 RESULTS

Fig. 6.2 shows typical output current-voltage (*I-V*) characteristics measured for OTFTs using the FS0027 ink formulation.

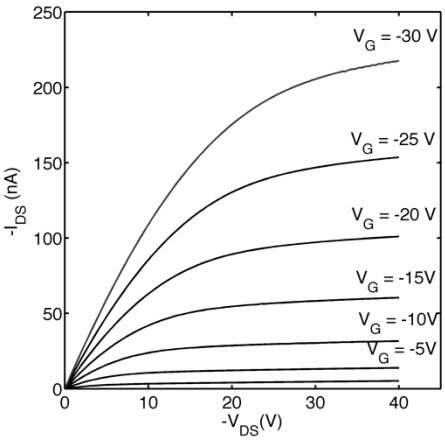

Fig. 6.2 - Output current-voltage characteristics for an inkjet printed OTFT. The semiconductor used is FS0027.

From the transfer curve shown in Fig. 6.3 a field effect mobility of 0.1 $cm^2/(V \cdot s)$ and a threshold voltage of 2.6 V are extracted. The small departure from linearity at low gate-source voltages (V_{GS}) is due to a relatively high off-state drain-source current. This off-current is due to an undesirable current path in parallel with the OTFT accumulation channel. This feature is typical of an OTFT with a doped semiconductor.

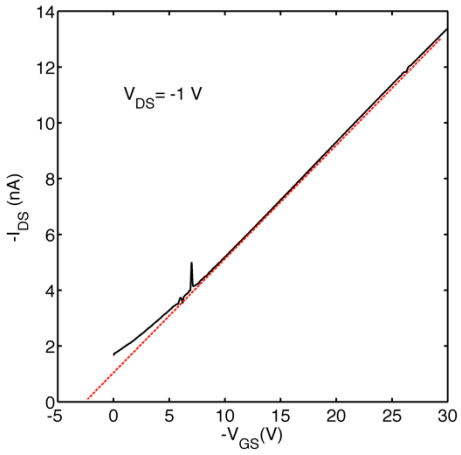

Fig. 6.3 - Transfer curve measured in the linear region (V_{DS} =-1 V). The curve shows a small positive threshold voltage (V_{th}= 2.6 V). The semiconductor used is FS0027.

In addition to the operational stability, it is also made a comparison of how the two semiconductors perform after being stored for several months in the ambient atmosphere. In order to carry out these studies, a set of devices prepared in identical conditions and also using the PFTP coating was considered. This set used two slightly different ink formulations: the FS0027, which is a triarylamine amorphous polymer dissolved in tetralin and the FS0096 a conjugated aromatic ordered polymer prepared in mesitylene. Table 6.1 summarizes the relative performances of both TFTs measured shortly after fabrication.

	μ_{FET} (cm^2/(V.s)	V_{th} (v)	I_{ON}/I_{OFF} (@V_G=-20 V)
FS0027	0.1	0 -5 V	≅10
FS0096	0.08	0 -6 V	≅ 50

Table 6.1 - Basic OTFT parameters fabricated using the two ink formulations. The numbers reflect an average of a total of 10 OTFTs measured.

Fig. 6.4 compares two transfer curves measured for FS0027-based OTFTs, one was measured two days after fabrication and the other recorded four months later. The current is reduced by 40 %. This decreases are at expenses of a decrease of the off-state current and an increase of the threshold voltage (ΔV_{th}=5V). The field effect mobility remains approximately constant as well as the modulation ratio.

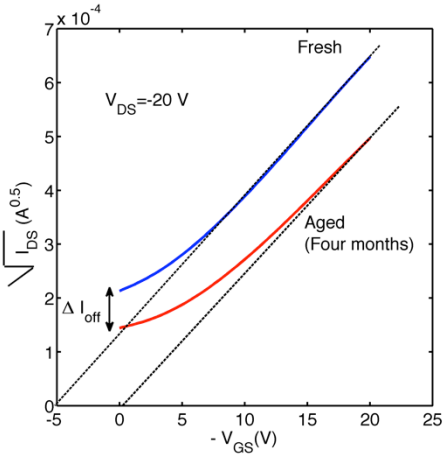

Fig. 6.4 - The effect of ageing on FS0027-based OTFTs. The ransfer curves were measured in the saturation region for a fresh OTFT and for a 4 months old device.

A similar comparison was done for FS0096-based OTFTs kept under identical ambient conditions. The transfer curves are shown and compared in Fig. 6.5.

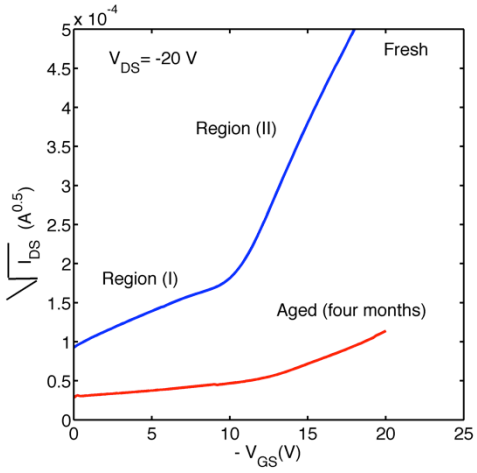

Fig. 6.5 - The effect of ageing on the FS0096-based OTFTs. The transfer curves were measured in the saturation region for a fresh OTFT and for a 4 months old device.

These devices exhibit a transfer curve with two distinct slopes. The transition from a low to a high slope originates a knee just below V_{GS} =-10 V. This behaviour is caused by a relative high contribution of the off-current to the total device current. For relatively low V_{GS}, the off-current dominates the total current, and the contribution of the field induced current is small. As V_{GS} increases the TFT channel current takes over and causes a rise in the slope of the transfer curve. As for FS0027-based devices, under ageing the off-current also decreases, but now the field effect modulation of the current is almost lost (it is lower by 96%). The on/off ratio has drop from 50 to only 2. Is merely possible that the threshold voltage increased dramatically. After ageing an applied gate bias of -20 V is not enough to modulate the accumulation channel and to follow the highest slope (region II in Fig. 6.5) of the transfer curve. In practical terms the measured transfer curve for the aged OTFT is still below the threshold voltage.

Unfortunately, extending the range of the gate-bias to more negative voltages is not feasible because the c-PVP layer would undergo to dielectric breakdown. It is not possible to extract V_{th} or μ_{FET} for an aged FS0096 OTFT.

In summary, upon ageing the two ink formulations undergo a similar degradation in the off-state current, but a remarkable different change on the threshold voltage. The increase in threshold voltage is much higher in the FS0096 than in the FS0027-based OTFTs.

6.4 DISCUSSION

The findings presented above show that all-inkjet printed OTFTs, produced from solutions in ambient conditions, show a performance and an operational stability as good as some of the reported vacuum processed OTFTs [**52**,**53**]. As demonstrated, a proper passivation of the dielectric surface is crucial for achieving a high operational stability. Results show that a solution of pentafluorothiophenol, successfully ink-jet printed on top of the insulating layer, neutralizes traps on the dielectric surface.

A similar approach to passivate the dielectric surface has been used by S. Chung et al. [**36**]. They report that a brush layer of dimethylchlorosilane terminated polystyrene PS-Si$(CH_3)_2$Cl on both dielectric and bottom source and drain electrodes improves dramatically operational stability and the performance.

Upon ageing the two formulation inks behave differently. OTFTs based on the FS0027 keep their basic parameters almost constant. OTFTs based on the FS0096 undergo a dramatic increase in the threshold voltage. The threshold voltage is an extrinsic parameter directly related with the number of traps on the dielectric surface. It is presumed that the reason for the different behaviour of the two inks lies on their different permeability to atmospheric species such as water [**54**,**55**]. Each ink formulation uses different solvents. The FS0096 is dissolved in mesitylene and the FS0027 ink is prepared in tetraline (higher boiling point than mesitylene). Whereas low-boiling solvents usually result in drying within seconds, high-boiling solvents increase the drying time to a few minutes. The slow drying might allow a better layer formation of the polymer, obtaining more compact films and consequently also less permeable to the diffusion of atmospheric species.

6.5 CONCLUSIONS

The effects of passivation layers on the operational stability and ageing effects when the devices were stored under dark ambient conditions were studied. By coating both the dielectric surface and the silver electrode with a printed PFTP layer, the operational stability improves one order of magnitude with respect to uncoated devices. Consideration goes to the PFTP, that possibly neutralizes deep electronic traps on the dielectric surface.

The exposure to the ambient atmosphere for extended periods of time causes an increase in the threshold voltage that is strongly dependent on the semiconductor ink formulation. The differences were attributed to different permeation barriers of the semiconductor layer to water diffusion.

Chapter 7

ELECTRICAL CHARACTERIZATION OF RECTIFYING DIODES

This chapter presents the electrical characteristics of rectifying diodes produced by ink-jet printing. Three types of diodes were measured, (i) Schottky diodes and (ii) Metal-Insulator-Semiconductor (MIS) diode structures and (iii) diode connected transistors. The MIS structures should in principle behave as pure capacitors. However, they have a leakage current, which is voltage polarity dependent. The mechanism behind of this unusual rectification is explained. The frequency response of both types of diodes is analysed. The MIS diodes show a poor frequency response limited by the charge carrier transport mechanism. Diode connected transistors were also explored as alternative way to make rectifying elements.

Since the most challenging application for diodes is a rectifying element in radio-frequency-identification (RFID) tags, the emphasis was put on the ability to rectify a signal the base-carrier frequency of 13.56 MHz. A suitable diode configuration was identified and an appropriate model proposed.

7.1 INTRODUCTION

In organic electronics the easiest way to make a diode is to choose an appropriate function metal to establish a Schottky barrier at the interface between an organic semiconductor and a metal. The most common metal used is the aluminium. However, this is not feasible by ink-jet printing because there are no ink-solutions of aluminium available. The only metal available in solution and that can be printed is cooper. In spite of the intense efforts, the *TDK4PE* consortium did not succeed to produce high quality coatings based on copper. To overcome this, the cooper was evaporated in vacuum and the semiconductor inks were ink-jet printed. The fabricated Schottky diodes were in reality hydrid, because one of the metal layers was vacuum processed. This diode was fabricated by the Tampere University.

There are basically two strategies to fabricate rectifying components, Schottky barrier diodes and diode connected TFTs. The diode connected TFT approach has the advantage of easy integration. However, TFTs have relatively long channels. By using photolithography the channel can be reduced but channel lengths below 10 μm are not

easy to produce by ink-jet printing. Cantatore et al. [**56**] have shown that it is possible to rectify a sinusoidal signal of 13.56 MHz using a diode connected TFT. However, an AC signal with 80 V peak amplitude was required to be obtained a dc level of 10 V. Schottky based diodes perform much better. A pentacene based diode can rectify an incoming AC signal of 18 V amplitude to a dc signal of 11 V at 13.56 MHz [**57**].

Depending on the channel length used, the diode connected transistor requires a several hundred times lager area as compared to the Schottky diode, which translates in a larger capacitance. The capacitance may not directly limit the frequency response, but the channel length due to slow carrier transport.

Table 7.1 provides a summary of the main characteristics and limitations of both type of devices.

Rectifying diode	Comments	Refs.
Schottky diode	The cut-off frequency is limited by the carrier time-of-flight and not by the diode capacitance. The low carrier mobility must be compensated by a thinner active layer. For high frequency response high mobility and thin organic layers must be used.	[**58**]
Diode connected TFT	Have a low current density. Requires the fabrication of large area TFTs which increases the occurrence of defects The channel length must be kept small.	[**56**]

Table 7.1 - Basic characteristics of the two approaches to fabricate rectifying diodes.

7.2 EXPERIMENTAL

The organic Schottky diodes were fabricated in Tampere University of Technology, Finland. The active layers were deposited on a flexible polyethylene erephthalate (PET) substrate (Melinex ST560 from Dupont Teijin Film), where the 50 nm copper (Cu) cathode was evaporated and patterned. The semiconductor polytriarylamine

(PTAA) and the top silver (Ag) anode were successively gravure printed. The diode with the biggest active area was chosen (sample name A45) with 1.0 mm^2. The device architecture is represented in Fig. 7.1.

The MIS capacitor diodes were fabricated by the TDK4PE consortium at Technical University of Chemnitz (TUC). The diodes are printed in rows of 14 diodes with constant parameters, where row 5-8 refers to diodes printed with varying layer thickness of semiconductor. Row 5 refers to thinnest semiconductor layers (25 µm DS) and row 8 to diodes with the thickest layers (10 µm DS) of semiconductor. Diodes printed in row 13-16 are printed varying the thickness of the c-PVP dielectric MMAcoMAA layer, where 13 refer to thin MMAcoMAA layers (1 layer) and 16 to thick MMAcoMAA layers (5 layers). Table 7.2 presents the basic characteristics of these devices.

Bag Label	Row number	Device name	Semiconductor Layer DS (µm)	Dielectric MMAcoMAA layers
Bag D1	Row 5	Dev01 to Dev14	25.0	Constant
	Row 6	Dev01 to Dev14	20.0	
	Row 7	Dev01 to Dev14	15.0	
	Row 8	Dev01 to Dev14	10.0	
Bag D2	Row 1	Dev01 to Dev14	>25	Constant
Bag D3	Row 13	Dev01 to Dev14	Constant	1.0
	Row 14	Dev01 to Dev14		2.0
	Row 15	Dev01 to Dev14		3.0
	Row 16	Dev01 to Dev14		5.0

Table 7.2 – Description of the MIS capacitor diodes

For DC electrical characterization a Keithley 487 Picoammeter was used. To test the diode as rectifying element an Agilent 33220W arbitrary waveform generator and Tektronix TDS210 oscilloscope were used to generate and measured the AC signals respectively. Capacitance and loss data were measured with Fluke PM6306 RCL meter.

7.3 RESULTS AND DISCUSSION

Fig. 7.1 shows the basic diode structure. As explained early, this diode was not entirely ink-jet printed, because the bottom copper electrode was deposited by vacuum evaporation. The copper electrode is a low-work function metal and established with the

polytriarylamine (PTAA) a Schottky barrier as schematically represented in Fig. 7.2. The silver/PTAA interface is an Ohmic contact. As expected, the current-voltage characteristics are rectifying.

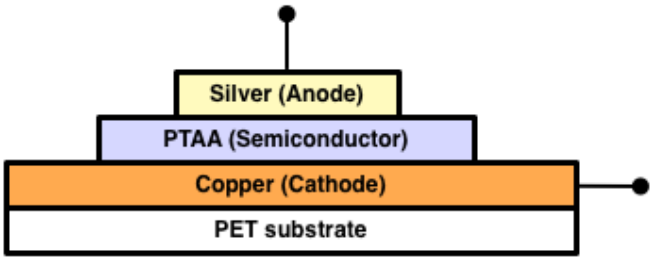

Fig. 7.1 - Basic diode structure. A Schottky barrier is established at the interface cooper/PTAA.

A typical current-voltage characteristics of the PTAA Schottky diode is shown in Fig. 7.2, as expected when positive voltages are applied to the top silver electrode the Schottky barrier is reduced and the diode conducts. Under low forward bias the current follows and exponential behaviour confirming the existence of a Schottky barrier. The forward bias current is approximately 330 μA at 5 V. The reverse bias leakage current does not saturate but is still significant lower that the forward current. The On/Off current ratio is 690 at |5V|. The frequency dependence of the diode was also studied up to 1 MHz. The capacitance and the loss ($1/R\omega$), as function of the frequency are represented in Fig. 7.3. Here R is the resistance and $\omega = 2\pi f$.

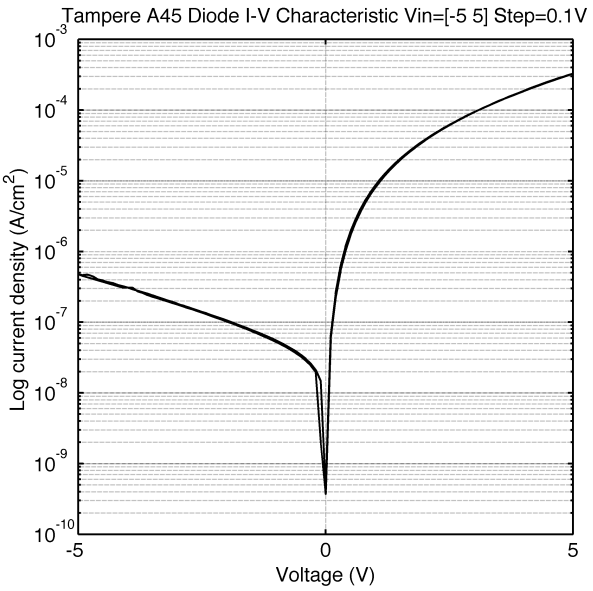

Fig. 7.2 - Current-voltage characteristics of the PTTA/Cu Schottky diode.

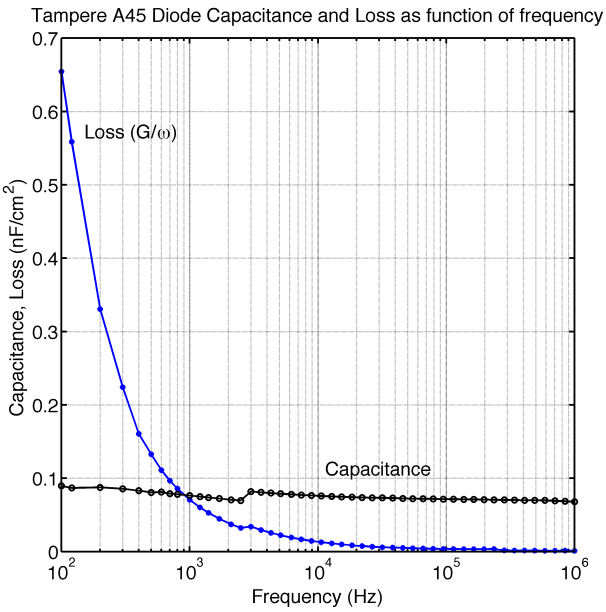

Fig. 7.3 - Frequency depdendence of the capacitance and loss for PTAA/copper Schottky diode.

The diode shows flat capacitance behaviour up to 1 MHz. The loss shows a low-frequency tail, which is an indication of DC leakage conduction. The flat behaviour of the capacitance shows that there are no significant series resistances. Series resistance can degrade the frequency response.

The capability of diodes to rectify AC sinusoidal wave was also tested. The diodes where mounted in a basic rectifying circuit shown in Fig. 7.4. The load resistor had a value of 1 MΩ and the capacitor 100 nF. For input wave a sine wave of 8 $V_{peak\text{-}peak}$ was used.

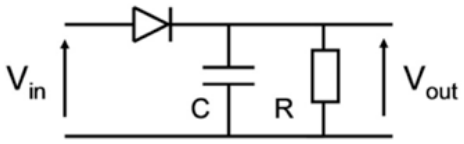

Fig. 7.4 – Half-wave rectifying circuit.

The output-rectified signal for different input wave frequencies is show in Fig. 7.5. For frequencies below 100 kHz the circuit successful produces a DC signal. However, as the frequencies increases the magnitude of the DC output dramatically decreases. For frequencies above 13.56 MHz is below 0.5 V.

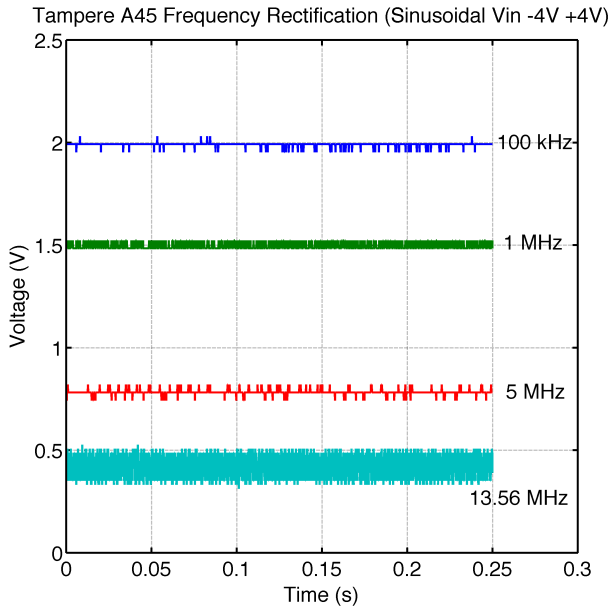

Fig. 7.5 - Rectified signals produced for different input signal frquencies. The rectifying circuit is shown in Fig. 7.4. The load capacitor is 100 nF and the load resistance of 1 MΩ. The diode used is the PTAA/Cu Schoktty diode.

Table 7.3 summarizes the general performance of Schottky diode in rectifying circuit.

Schottky A45 Diode High Frequency Rectification Performance		
Frequency (MHz)	**Output (V)**	**Input Rectification (%)**
0.1	2.0	50.0
1	1.49	37.3
5	0.78	19.5
13.56	0.42	10.5

Table 7.3 - Schottky diode high frequency rectification performance. The input is a sinusoidal wave, with an amplitude of |4V|.

7.3.2 METAL-INSULATOR-SEMICONDUCTOR (MIS) DIODES

The structure of diodes based on metal-insulator-semiconductor (MIS) is shown in Fig. 7.6. These diodes have asymmetric *I-V* characteristic. The current is higher when negative bias is applied to the bottom silver electrode. A typical *I-V* curve is shown in Fig. 7.7. These diodes may have a rectification ratios higher than 10^2 at |5V|.

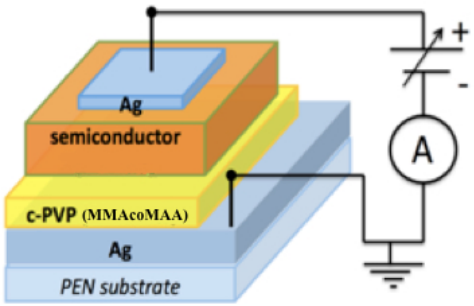

Fig. 7.6 - Schematic diagram of the structure of a MIS-Diode

The analysis of the forward *I-V* characteristics in a log-log plot (see Fig. 7.8) shows that the charge carrier transport is space charged limited (SCL) and follows approximately Child's law (slope 2). As it will be discussed later, this may impose an intrinsic limitation of the diode ability to rectify high frequency signals.

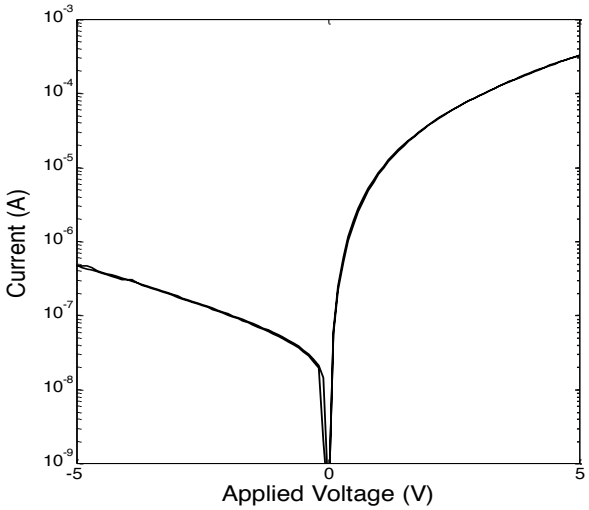

Fig. 7.7 - Current-voltage characteristic of a MIS-diode. Positive bias refers to the top silver electrode being positive.

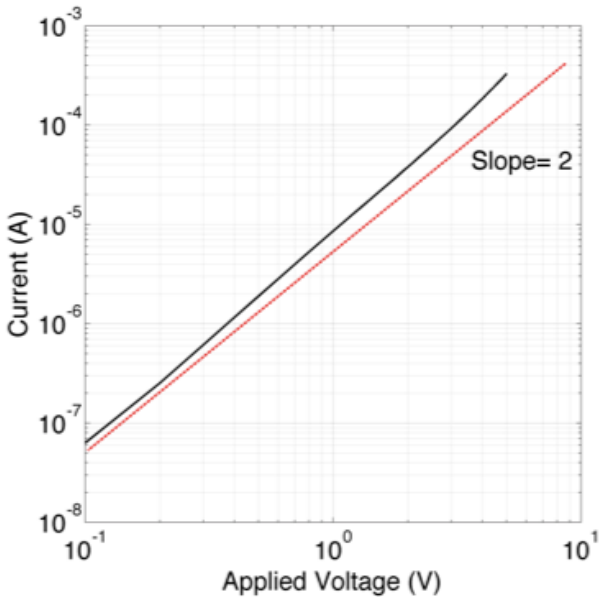

Fig. 7.8 - Log-log plot of the forward bias current-voltage characteristic showing that the slope is slightly higher than 2 showing that carrier transport is space charge limited.

Capacitance-voltage characteristics confirm the absence of depletion layers associated with interfacial barriers (see Fig. 7.9). The decrease in the capacitance with increasing bias is due to a high leakage current that bypass the diode capacitance.

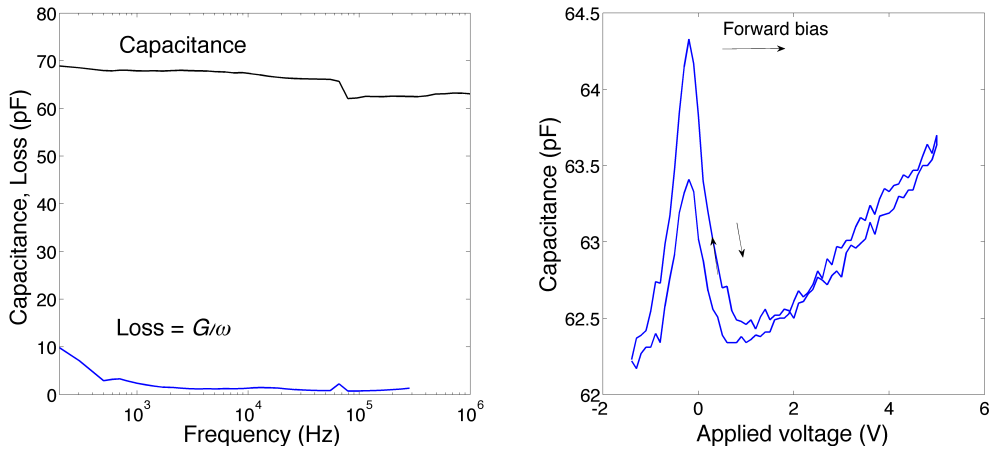

Fig. 7.9 - (a) Capacitance and loss as function of the frequency (b) Capacitance voltage plot recorded at a test frequency of 1 kHz. The diode area is 2 mm^2.

7.3.2.1 STUDY OF THE VARIABILITY ON THE RECTIFICATION PROPERTIES

In order to optimize the rectification properties of the MIS-diodes the semiconductor layer thickness as well as the dielectric layer thickness was varied systematically as described in the experimental section. The semiconductor layer thickness was varied

from 10 μm to 25 μm in steps of 5 μm. A similar variation was also studied for the insulator layer thickness. In each study, the corresponding semiconductor or dielectric layer thickness was kept constant with a thickness of 20 μm. For each layer thickness we measured 14 diodes. The diode parameter studied was the on/off ratio at |10 V|.

Fig. 7.10 shows the on/off current ratio for different semiconductor layer thickness. The dielectric layer thickness was kept constant.

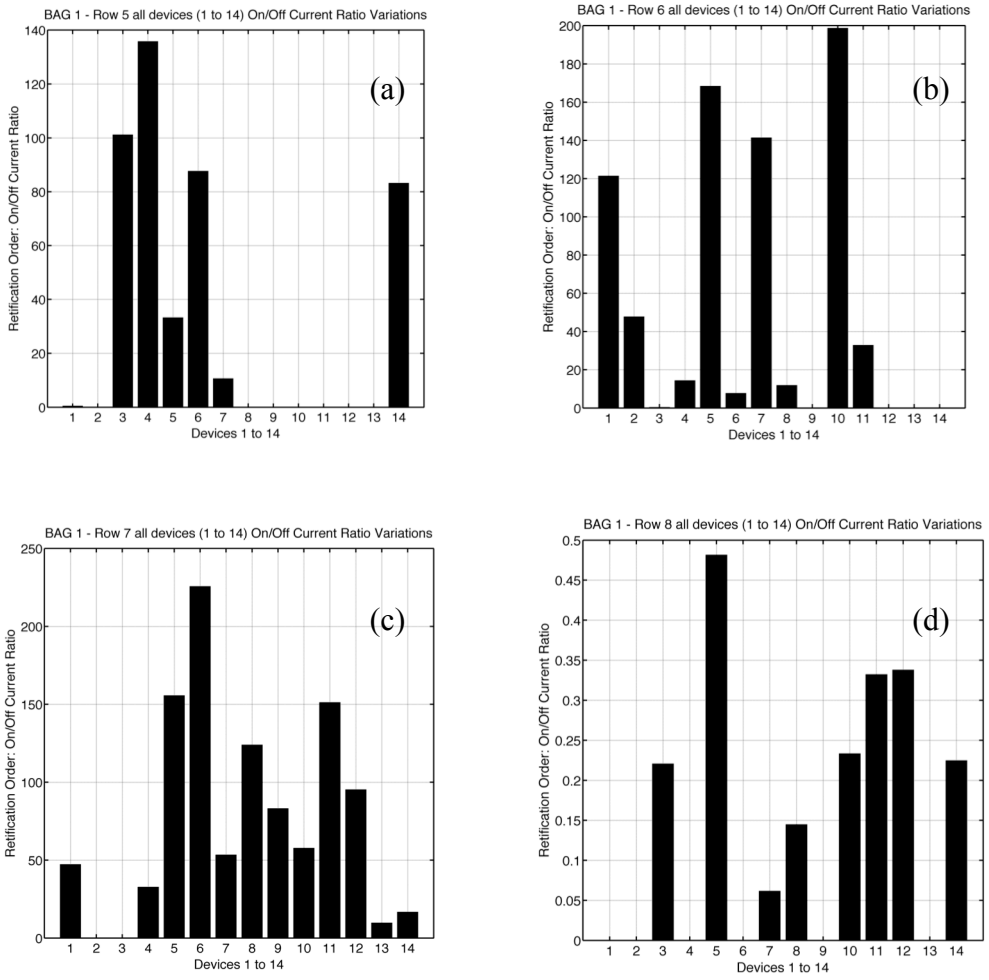

Fig. 7.10 - Diode on/off current ratios with different semiconductor layer thickness: (a) 25μm; (b) 20μm; (c) 15μm and (d) 10μm. The on/off ratio was measured at |10 V|.

The first thing to note is there is a large dispersion on the on/off ratio. For instance, for a 20 μm semiconductor layer the on/off ratio can vary from 20 to 200. This dispersion on the on/off ratio is common for all the semiconductor layer thickness. The best rectification values obtained are slightly above 200. For a 10 μm thick semiconductor layer the rectification is lost as show in the histogram (d) of Fig. 7.10. Rectification values below 1 mean that the rectification is inverted. The diode conducts

more in reverse bias than in forward. Apart from diode performance measured trough the rectification ration, the histograms in Fig. 7.10 also provide information about the yield. A few devices are short-circuited. For instance, for a 25 μm thick semiconductor only 6 of the 14 diodes were working (see histogram (a) on Fig. 7.10).

Fig. 7.11 shows the variation of the on/off current ratios as the dielectric layer thickness is varied for a constant semiconductor layer thickness (20 μm). The thickness was varied by printing several layers (from 1 up to 5 layers). The variability is extremely large. Rectification ratios vary from 10 to 450. Furthermore, the rectification properties do not show any particular trend with the insulator thickness.

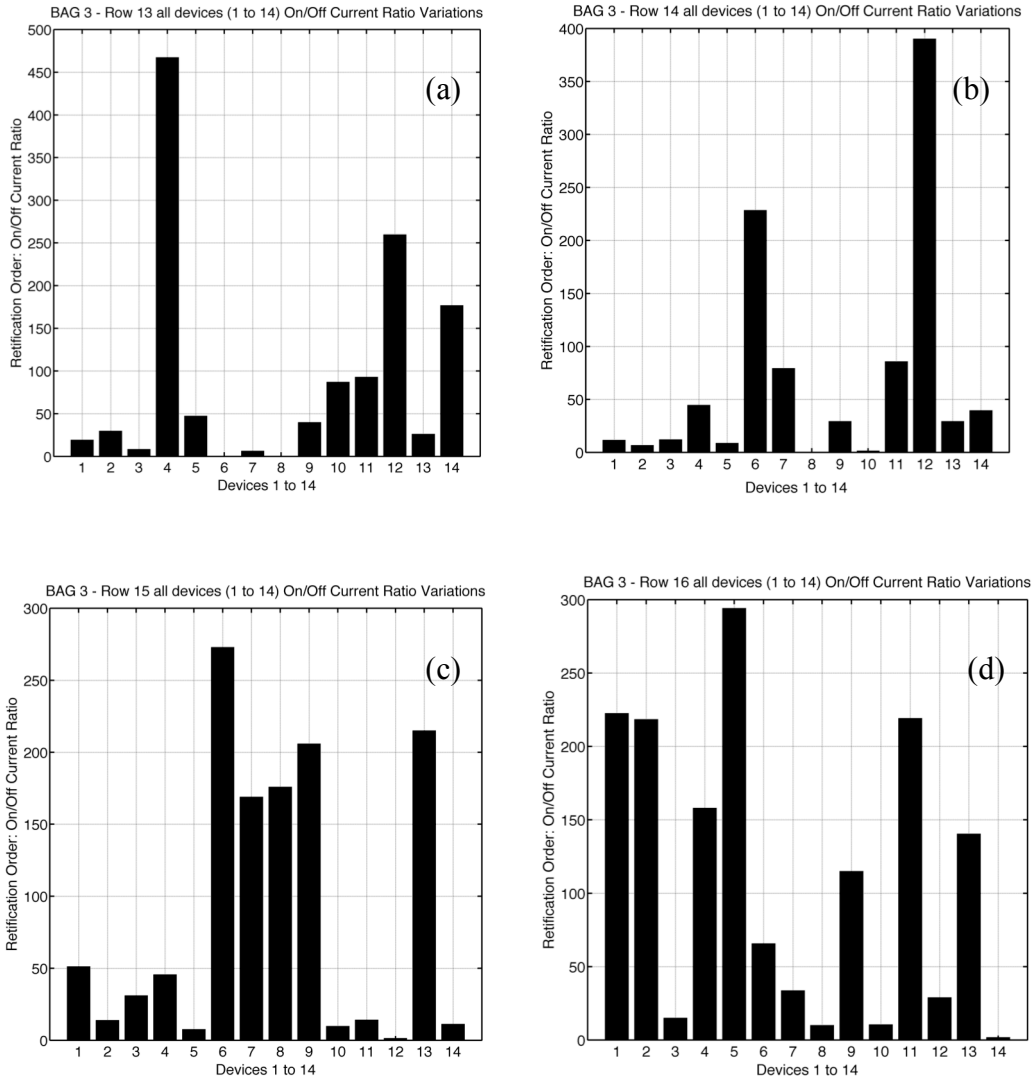

Fig. 7.11 – Diode On/off current ratios with different number of insulator (MMAcoMAA) layers: (a) 1 layer; (b) 2 layers; (c) 3 layers and (d) 5 layers. The rectification was measured at |10V|.

7.3.2.2 RECTIFYING PROPERTIES AT HIGH FREQUENCIES

The MIS diode is mounted in a half-wave rectifying circuit (see Fig. 7.4). The load capacitor is 1μF and the load resistance 1 MΩ. Fig. 7.12 shows the ouput DC signal was measured for different input signal frequencies. The input wave had a amplitude of ± 10 V.

The ouput signal is strongly attenuated for frequencies above 500 kHz. At the operating frequency of 1 MHz, the DC rectified output reaches only 0.5 V for an input signal with an amplitude of |10V|. At 5 MHz the diode behaves as a short-circuit.

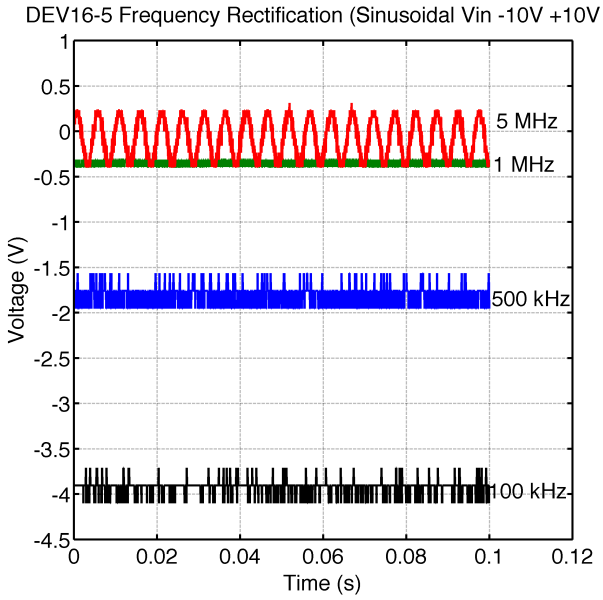

Fig. 7.12 - DC rectified signal for different sine-wave input frequencies. The circuit is show in Fig. 7.4. The load capacitor is 1μF and the load resistance of 1 MΩ.

Table 7.4 shows the attenuation of the DC rectified signal as the frequency of the input signal increase from 0.1 MHz up to 5 MHz.

TDK4PE Demo1 DEV16_5 Diode High Frequency Rectification Performance		
Frequency (MHz)	**Output (V)**	**Input Rectification (%)**
0.1	- 3.92	39.2
0.5	- 1.80	18.0
1	- 0.35	3.5
5	No rectification	0.0

Table 7.4 – MIS-diode high frequency rectification performance.

7.3.2.3 DEGRADATION CAUSED BY BIAS-STRESS

When consecutive experiments were carried out, the data was not reproducible. Under continuous operation the diode *I-V* characteristics degrade with time. In order to inspect for this degradation, two types of bias-stress experiments were carried out. In a first experiment several consecutive *I-V* curves were recorded. The voltage ramp was scanned both in positive and in negative polarities. This stress causes an overall increase in the diode current for both polarities. This effect is shown in Fig. 7.13 (a). In a second stress experiment the diode is always kept at 10V (positive on the top silver electrode) for two hours. This stress was periodically interrupted to record an *I-V* curve. The behaviour is shown in Fig. 7.13 (b). Now the diode current decreases for both polarities, but the decrease is significant higher in forward bias. The result is a dramatic degradation on the rectification properties.

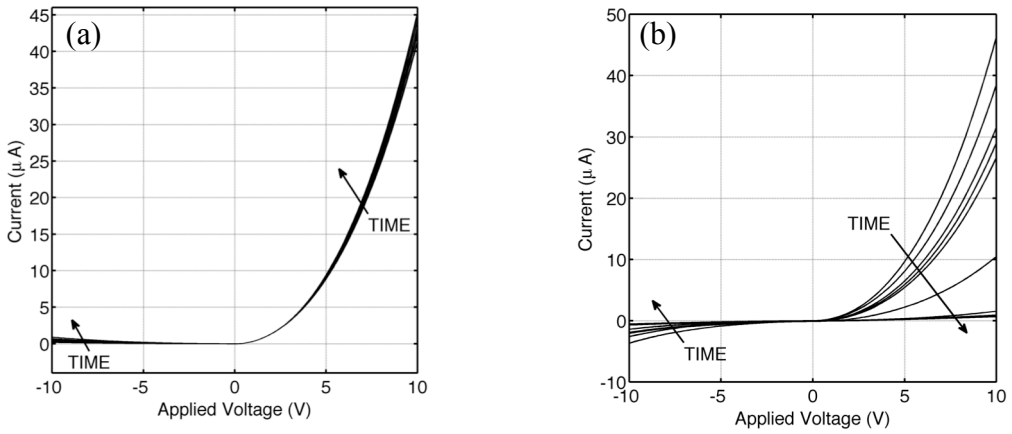

Fig. 7.13 - Degradation of the I-V cuvres after bias stress (a) the effect of consecutive volatge ramps. (b) the effect of continous volatge (10V) applied for 2 hours.

Interestingly, after few days of rest, the original behaviour is restored, showing that this degradation phenomenon is reversible.

7.3.2.4 THE OPERATING MECHANISM

The MIS diode should behave as capacitor because the insulator is reasonable thick. The fact that there is a substantial leakage current particularly when the semiconductor/insulator interface is driven into accumulation (positive voltages on the top silver electrode), suggest that the insulator is in reality thin enough to allow current passing trough. It is possible that the dielectric has pinholes, which are filled by the top semiconductor layer. In this view, the system is in reality nanostructured

dielectric/semiconducting matrix as show in Fig. 7.14. When negative bias is applied in the bottom metal electrode, a high free carrier density is induced in the semiconductor. At local thinner regions as show in Fig. 7.14 these carriers can tunnel across the dielectric. When a positive bias is applied, no free carriers are induced in the semiconductor and the leakage is substantially smaller. This mechanism explains the asymmetric *I-V* characteristics.

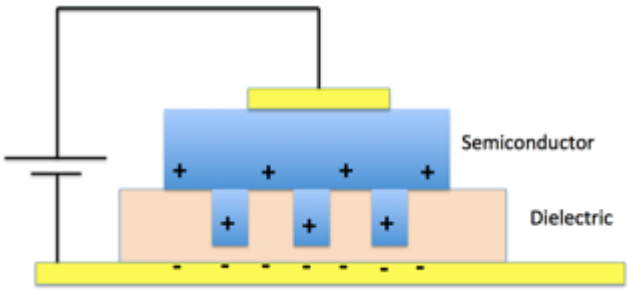

Fig. 7.14 - Schematic diagram showing the proposed mechanism to explain non-symmetric I-V curves in MIS structures.

The interpenetration of the two-adjecent layers is strongly dependent on the processing. This in principle explains the enormous variability observed in the rectification ratio discussed above.

7.3.3 THE DIODE CONNECTED TRANSISTOR

Fig. 7.15 shows the current voltage characteristic of a diode connected transistor. Under a forward bias of -20 V, it can supply 250 nA. Rectifying circuits were tested but the signal is strongly attenuated in the kHz range. This limitation is caused by a long channel length (L=40 μm) and low charge carrier mobility (10^{-3} $cm^2/(V.s)$). This diode was not considered an option for high frequency rectifying circuits because it requires and optimization not compatible with ink-jet printing (very small channel lengths and high mobility materials).

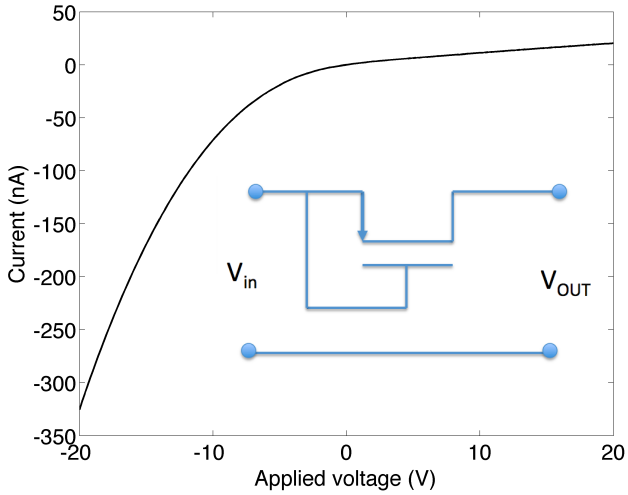

Fig. 7.15 - I-V characteristic of a diode connected TFT. The Inset shows the circuit configuration. The area of the TFT is 2.5x1.8 mm^2.

7.4 CONCLUSIONS

Different types of organic diodes were characterized. MIS diodes show poor rectification properties, the on/off ratio has a very large variability. Furthermore, when submitted to a continuous applied bias the rectification properties are lost.

Organic based Schottky diode has high on/off current ratio and a low capacitance. When inserted into rectifying circuits, they can produce a DC output signal for an input signal operating at 13.56 MHz. They are suitable to be used as rectifying element in RFID tags.

The frequency response of organic based diodes is limited by the low mobility of the carriers.

Chapter 8

ELECTRICAL CHARACTERIZATION OF CAPACITORS

In this chapter, organic inkjet printed capacitors with different dielectric types and active area sizes are electrically characterized. Sources of parasitic effects within these capacitors are also discussed.

8.1 INTRODUCTION

Smart fabrics have attracted growing interest in the last ten years, especially for wearable system applications [**59**]. Flexible capacitor is an essential electronic component, necessary for wearable electronic circuits and sensors. An all-inkjet printed capacitor is of great interest because of its use in direct write processed electronic sensors and circuits. Low-frequency passives including resistors, capacitors, and inductors have been demonstrated utilizing the inkjet process [**60**,**61**,**62**]. Printed Metal-Insulator-Metal (MIM) structures capacitors on flexible substrates [**63**] have a wide variety of applications, especially in printed wearable systems, which currently require the use of discrete mounted components and RFID tags [**64**].

The presented capacitors will be characterized through the capacitance and loss as function of frequency, and their sources of parasitic effects: (i) fringing effects, (ii) lateral conduction and (iii) series resistance caused by the metal tracks will be discussed.

8.2 EXPERIMENTAL

Printed capacitors are Metal-Insulator-Metal (MIM) sandwich structure as shown in Fig. 8.1.

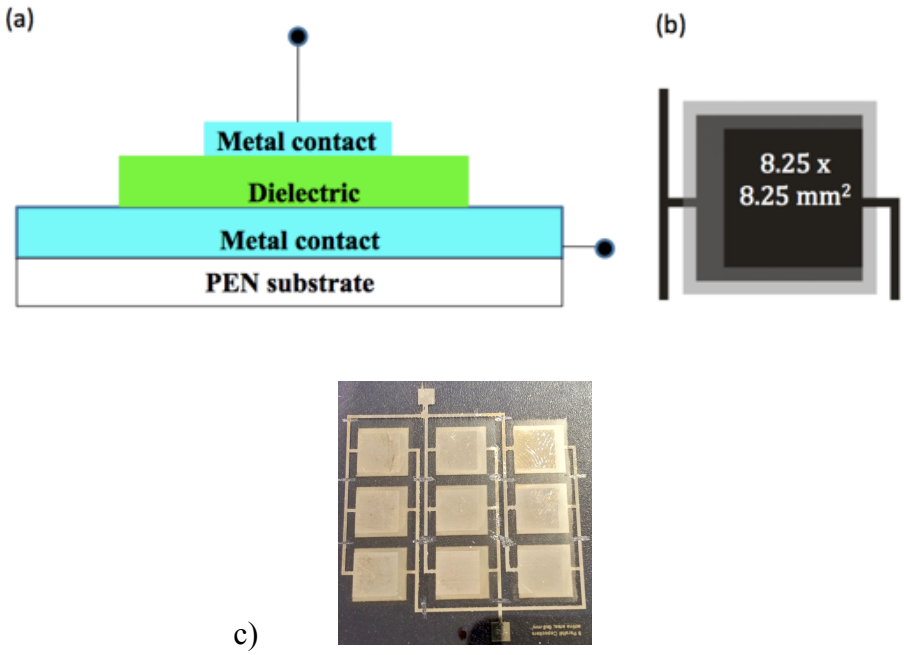

Fig. 8.1 - (a) Schematic cross section view of a printed capacitor, (b) Schematics of a top view showing the active area and printed tracks, (c) Final printed sample.

The capacitors are printed in parallel setups and are measured individually. The classification of capacitors goes by type of dielectric and their pattern size that varies from each bag sample, see Table 8.1.

MIM Capacitors Specifications				
Bag ID	**Sample ID**	**Dielectric type**	**Active Area (mm^2)**	**Pattern size (%)**
C1	311	cPVP (35µm) DS	8.25 x 8.25	100
C2	323	cPVP (35µm) DS	7.5 x 7.5	90
C3	333	cPVP (35µm) DS	6.75 x 6.75	80
C4	345	cPVP (35µm) DS	6.0 x 6.0	70
C5	1, 2	Atlana Bectron	1: 6.0 x 6.0; 2: 6.75 x 6.75	1: 70; 2: 80
C6	3, 4	Atlana Bectron	3: 7.5 x 7.5; 4: 8.25 x 8.25	3: 90; 4: 100

Table 8.1 – MIM Capacitors specifications

Fig. 8.2 represents the equivalent circuit for a printed capacitance.

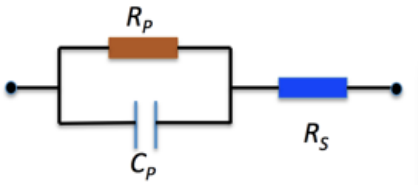

Fig. 8.2 - Equivalent circuit for a printed MIM structure including the series resistance caused by metal tracks.

In order to extract parameters, C_P and R_P can be evaluated by measuring the impedance at low frequencies (f<1 kHz) using an impedance analyzer.

R_S causes major disperison in the impedance as function of frequency, so the frequency of this dispersion allows the estimation of *Rs*. To estimate R_S one must measure the impedance as function of frequency.

All the measurements were made in dark chamber, at ambient temperature, using impedance analyzer Fluke PM6306 with |1V| AC signal input.

8.3 RESULTS AND DISCUSSION

The capacitance and loss (G/ω) ($\omega = 2\pi f$) as a function of the frequency measurements, for different samples with cPVP dielectric, with variation of active area size, are presented in Fig. 8.3.

Through the inspection of capacitors capacitance and loss (Fig. 8.3 and 8.4), the capacitance decreases slightly in a linear fashion with frequency. The pattern size difference of samples reflects directly on their capacitance value, as it is expected with capacitors, where bigger active area creates bigger capacity. 100% active area size capacitor (Fig. 8.3 a)) shows poor capacitance value.

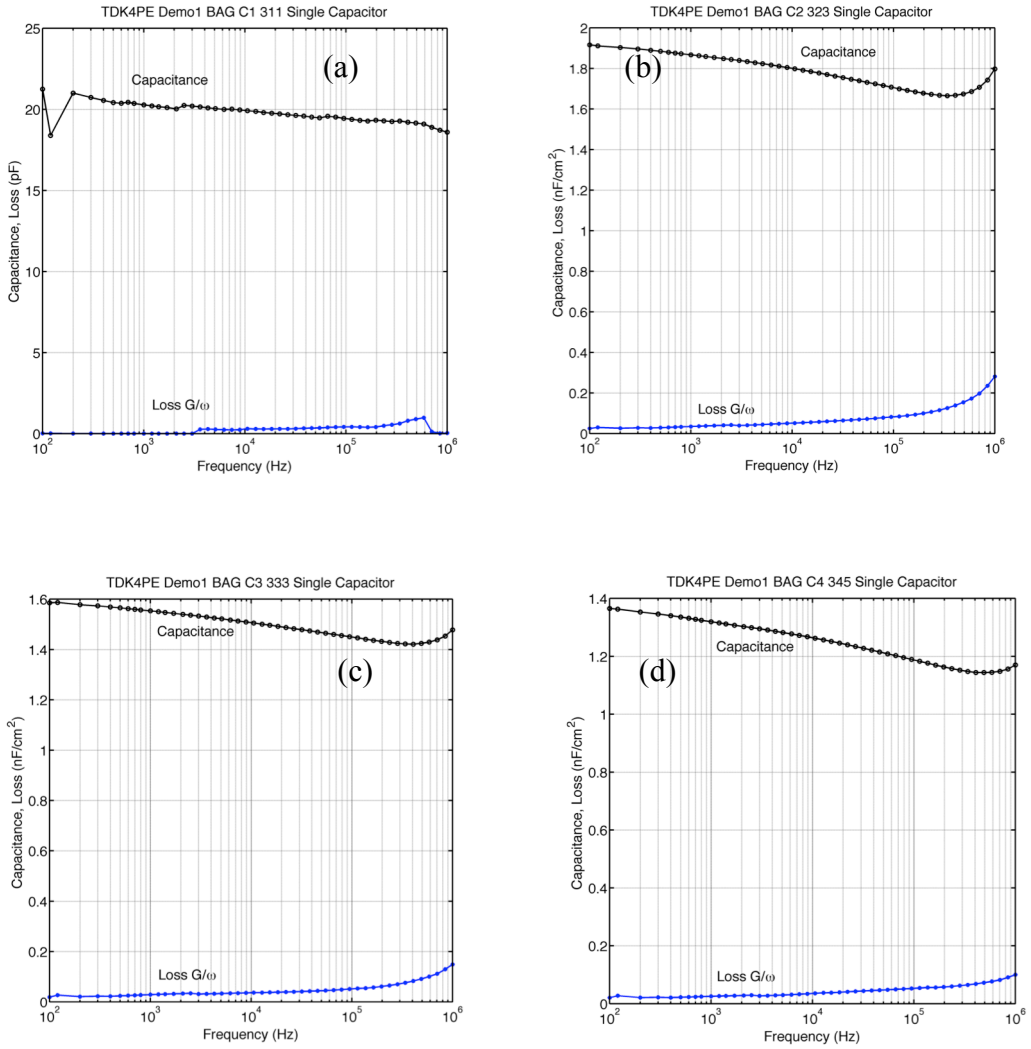

Fig. 8.3 - MIM capacitors capacitance and loss as function of frequency, cPVP dielectric, active area size: (a) 100 %; (b) 90 %; (c) 80 % and (d) 70 %.

While comparing different dielectric types, it can be seen that cPVP dielectric can provide more capacitance (above 1nF difference) than the Atlana Bectron.

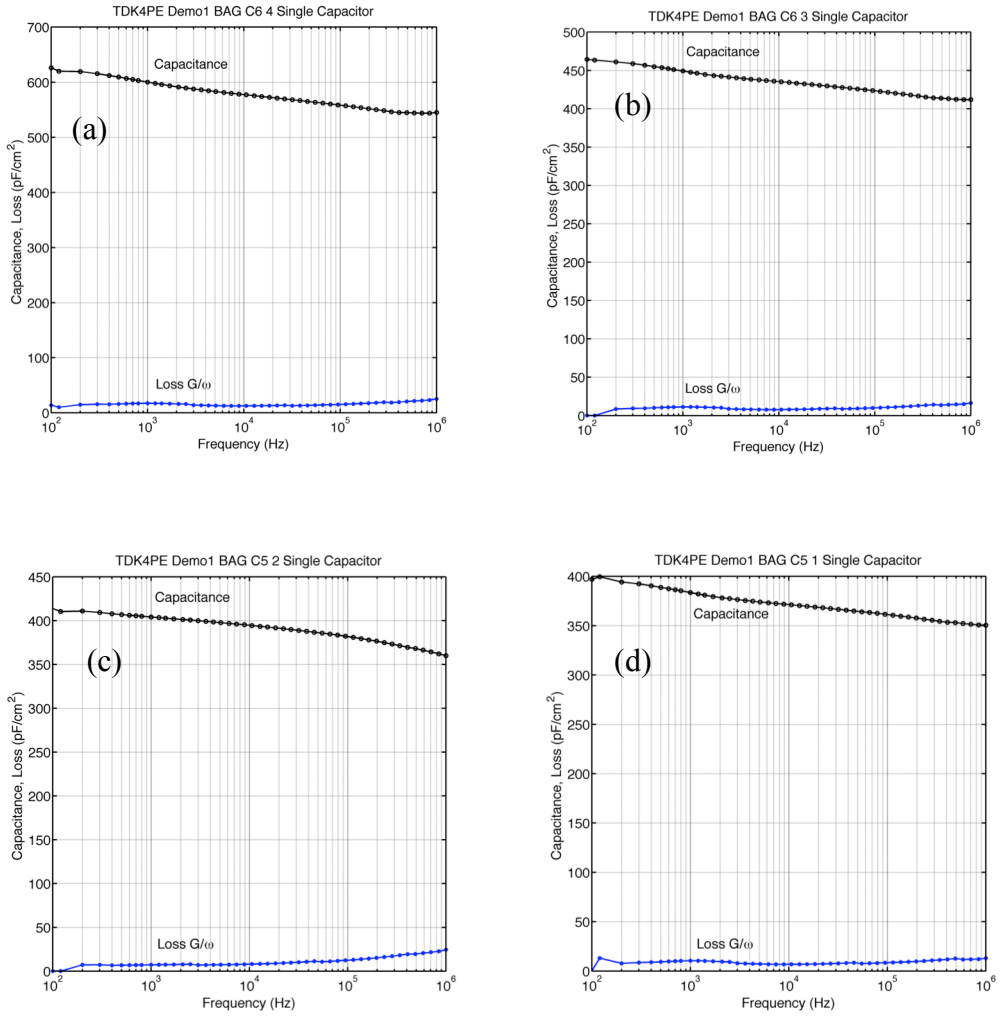

Fig. 8.4 - MIM capacitors capacitance and loss as function of frequency, Atlana Bectron dielectric, active area size: (a) 100 %; (b) 90 %; (c) 80 % and (d) 70 %.

As shown in Fig. 8.1 (b), the physical area of the bottom electrode coated with the dielectric is larger than the top metal layer. In a MIM structure the number of free carriers in the polymer is low and fringing effects are not really expected. Fringing may be significant in metal-insulator-semiconductor (MIS) structures. However, the presence of atmospheric moisture may contribute to fringing by making the dielectric surface conductive. When measurements are done under vacuum conditions, the additional parasitic capacitance observed in MIM structures may be due to a lateral conduction along the polymer near the bottom contact surface. This is schematically represented in Fig. 8.5 and can enhance the effective area of the capacitor. Other sources of parasitic capacitance may appear due to the alignment of top and bottom electrode tracks.

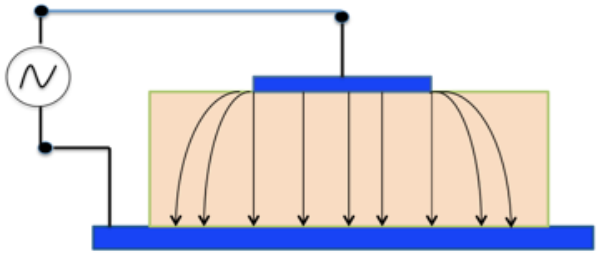

Fig. 8.5 - Schematic representation of an increase in the effective area of the top electrode caused by lateral conduction. This effect can enhance the measured capacitance.

Fig. 8.6 represents the frequency dependence of the capacitance of several printed structures with different types of dielectric material (cPVP and Atlana Bectron). The area of the top electrode was varied in respect to the total dielectric area and two different dielectric types were compared.

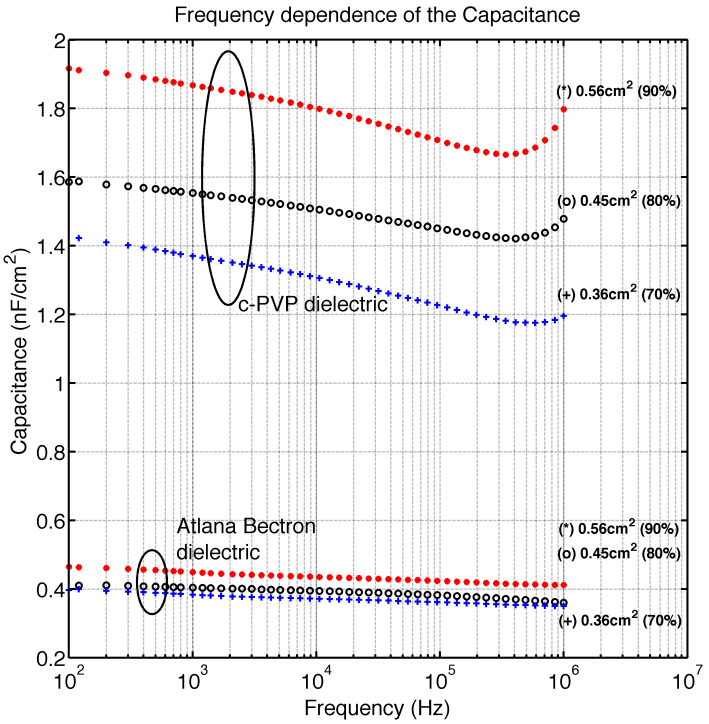

Fig. 8.6 - MIM capacitors frequency dependence of capacitance of several printed MIM structures. The area of the top electrode was varied in respect to the total dielectric area.

The frequency dependence of the capacitance of cross linked PVP dielectric decreases slightly with a frequency, but has some exponential growth near 1MHz value.

While analyzing samples made with Atlana Bectron DP8602 dielectric, the capacitance maintains a slight, but linear decrease with frequency. This is commonly observed in organic based electronic devices and it is a well-know process that is

modeled by a constant phase element. The admittance (Y) of the capacitor can be expressed by the empirical relation $Y = A_o(i\omega)^n$, where $1 \leq n \leq 0$ and A_o a constant. The physical origin of the process is unclear. In semiconductor materials it is reasonable to assume that is caused by dipolar relaxation with a wide distribution of relaxation times. However, this frequency dependence is relatively small and it can be neglected.

Similar analysis was made to compare the variation of the loss values through the frequency sweep, as seen in Fig. 8.7. The cPVP dielectric devices present exponential increase in loss values near MHz range, but Atlana Bectron dielectric seems to have a very slight and linear increase.

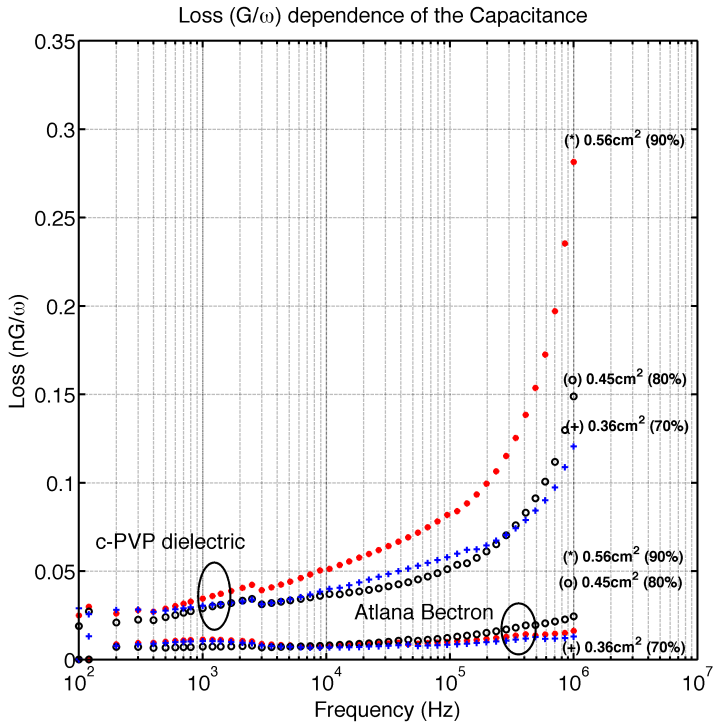

Fig. 8.7 - MIM capacitors frequency dependence of loss of several printed MIM structures. The area of the top electrode was varied in respect to the total dielectric area.

This loss effects may be related to printed silver tracks, which create a small series resistance (R<10 Ω) and can cause a relaxation frequency above or within the MHz range, limiting this way the frequency response of the capacitors. Printing wide and short tracks can minimize these effects.

8.4 CONCLUSIONS

Different dielectric types of MIM capacitor structures were studied. The variation of top electrode area had reflection on total capacitance of the device. Capacitance and loss

comparison between dielectric types was made. Fringing effects, lateral conduction and series resistance caused by metal tracks models were proposed and discussed.

Chapter 9

ORGANIC RFID

In this final chapter, a fully printed organic half-wave rectifying circuit for an RFID tag was fabricated and characterized. It is shown that a half-wave rectifying circuit can produce a DC signal with enough power to drive an organic light emitting diode.

9.1 INTRODUCTION

Radio frequency identification (RFID) is a compact wireless technology, utilizing electromagnetic waves for transmitting and receiving information stored in a tag or transporter to and from a reader, and it is used for object identification. In comparison with conventional methods of identification, RFID has several benefits, which rely within the higher reading range, faster data transfer, ability of integration of RFID tags within objects and the possibility of simultaneous reading of massive amount of tags [**65**]. This technology has a wide range of applications, which include retail supply chain, pharmaceutical tracking and management, sensing and metering applications, parcel and document tracking, real-time location systems (RTLS) and livestock or pet tracking [**66**].

With development and improvement of organic solutions and various inkjet printing techniques, a wide interest in fabrication of organic RFID (ORFID) emerged [**67**], due to the potential lower cost in manufacture compared to conventional RFIDs that use silicon based semiconductors.

RFID packages consist of 3 main components: (i) the antenna of the RFID tag receives a broadcast radio frequency (RF) signal from a reader, which induces a small AC current in the antenna through electromagnetic induction; (ii) the chip of RFID tag rectifies the AC signal received in the antenna and charges a capacitor, which provides power to operate the RFID. The output signal, which includes some information about chip ID is sent back to antenna, and it is modulated in time by tag's unique ID; (iii) the reader, through its own antenna, receives the new signal containing the ID of the chip.

The key technical requirements of ORFIDs include: (i) the ability to operate at 13.56 MHz for smart tags applications; (ii) have a long lifetime (two or more years) and (iii) be extremely low cost for large-scale applications [**68**].

One of key rectifying elements in RFID is a diode, which is responsible for creating DC output of AC signal received through antenna, and while charging capacitor, it powers RFID.

Organic rectifying diodes can be printable, flexible, and stable in ambient environments [**69**,**70**,**71**,**72**,**73**], properties that pointed to possibility of fabrication of low-cost circuitry consisting of numerous organic components. Printed organic diodes with PTAA semiconductor have been demonstrated to have excellent performance at frequencies around 13.56 MHz [**69**], [**70**], [**73**].

The half-wave (HW) rectifier including an organic rectifying diode and a filtering capacitor, is an example of organic rectifying circuit adopted from inorganic rectifier topologies, which has been used for many years due to its simplicity [**69**], [**70**], [**74**], [**75**].

This chapter introduce an organic rectifying diode, capable to work within 13.56 MHz range, and it is included in fully organic HW rectifier circuit. To prove that the circuit is working the DC output signal was used to power an organic light emitting diode (OLED). The circuit performance is studied and the results are presented.

The full RFID requires two induction coils, one working as RF emitter and other and a receiver. These coils have been inkjet printed and mounted (see Fig 9.1). Unfortunately to use them we need a high power radio-frequency generator capable to drive the coil with enough power. This was not possible with the signal generators available in the lab.

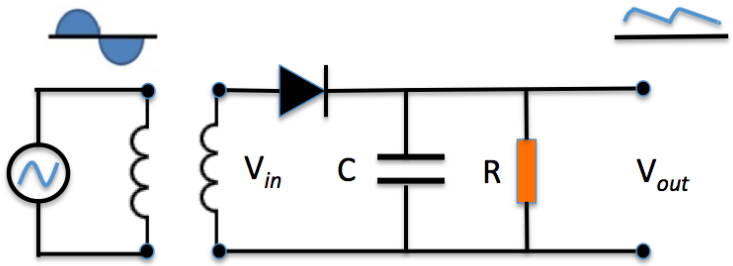

Fig. 9.1 - Basic components of RFID tag. The induction coils (emitter and receiver antenna) and the rectifying circuit.

9.2 EXPERIMENTAL

The major part of a working RFID tag consists of rectifying circuit, which is responsible for rectification of the signal received wirelessly from reader. A HW

rectifier has 3 main components: rectifying diode, load capacitor and resistor. The last one simulates a programmable chip. In our case it was replaced by an OLED to visualize the DC output signal. The rectifying circuit is presented in Fig 9.1.

Electrical characteristics of the main components used are presented below.

9.2.1 RECTIFYING DIODE

The rectifying diode used is an organic Schottky diode previously described in Chapter 7.

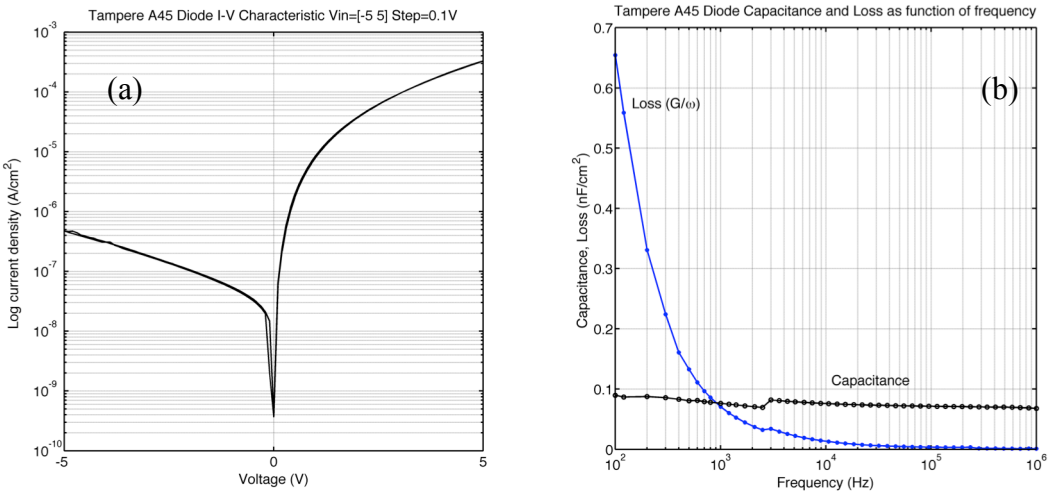

Fig. 9.2 - (a) Current-voltage characteristic of the Schottky diode, (b) Frequency dependence of capacitance and loss.

A Schottky diode with a on/off ratio of 700 (at |5V|) and a flat capacitance behaviour up to 1 MHz (see Fig. 9.2), was used.

9.2.2 LOAD CAPACITOR

In order to create a load capacitor, three inkjet printed MIM capacitors were connected in parallel to obtain a capacitor with approximately 4.7µF in a 2 cm^2 of active area. These capacitors were produced by the TDK4PE consortium. All these devices have identical characteristics and they use as dielectric the cPVP.

Fig. 9.3 shows the frequency dependence of capacitance and loss of one of the three individual capacitors selected to make the parallel connection.

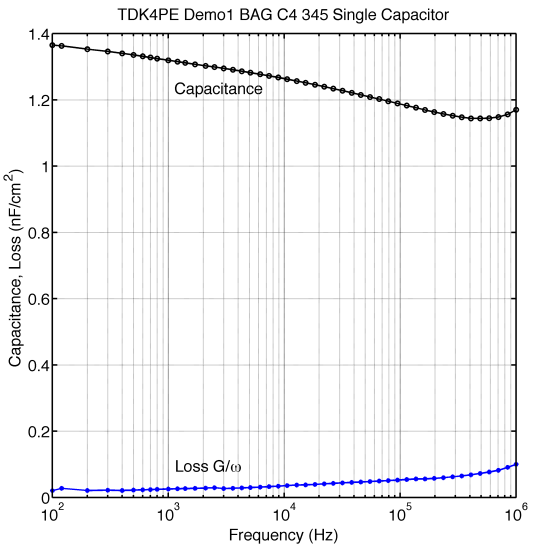

Fig. 9.3 - Capacitance (F) and Loss (G/ω) as function of frequency for the capacitors used in the rectifying circuit.

9.2.3 ORGANIC LIGHT EMITTING DIODE

To create an output load, an organic light emitting diode (OLED) shown in Fig. 9.4 was used. This OLED was produced by Philips at the high tech campus in Eindhoven.

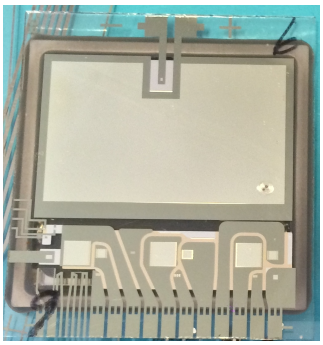

Fig. 9.4 – Organic Light Emitting Diode (OLED)

The HW rectifier RFID tag experimental was made in dark chamber, at ambient conditions without encapsulation. All the connections within the main components were made using silver solder and aluminium (Al-Si) with 25μm diameter wire. The input |10V| AC wave was generated using Agilent 33220A signal generator, and the output voltage was read by Tektronix TDS210 oscilloscope.

9.2.4 THE INDUCTION COIL

The induction coils we all inkjet produced from an ink formulation of silver. Unfortunately as stated early we do not have RF signal generator with enough power to drive them.

A Photograph of an induction coil is shown in Fig. 9.5. The induction coil connect to the rectifying circuit is shown in Fig. 9.6.

Fig. 9.5 – Photograph of an inkjet printed induction coil.

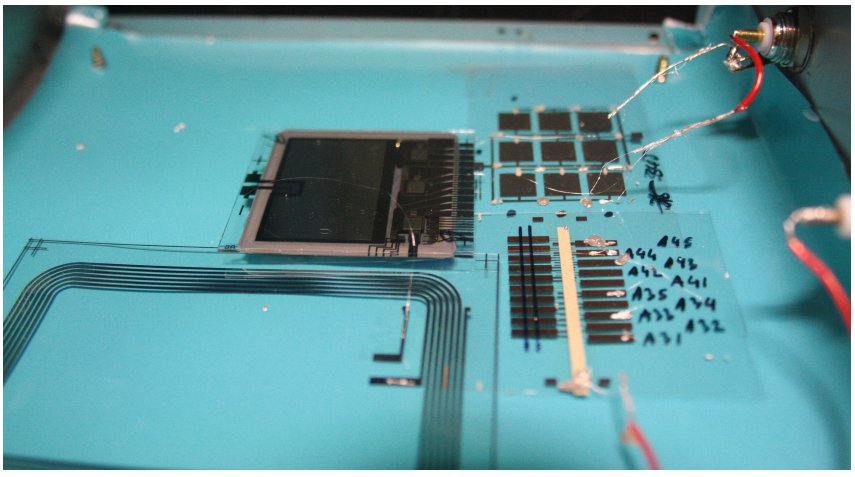

Fig. 9.6 - Photograph of the rectifying circuit implemented and wired to receiver antenna (induction coil).

9.3 RESULTS AND DISCUSSION

The receiver antenna was replaced by a signal generator. When an input sine wave of |10V| peak amplitude is used, the rectifying circuit produces a signal with an average DC level of 4 V and a small ripple fluctuation.

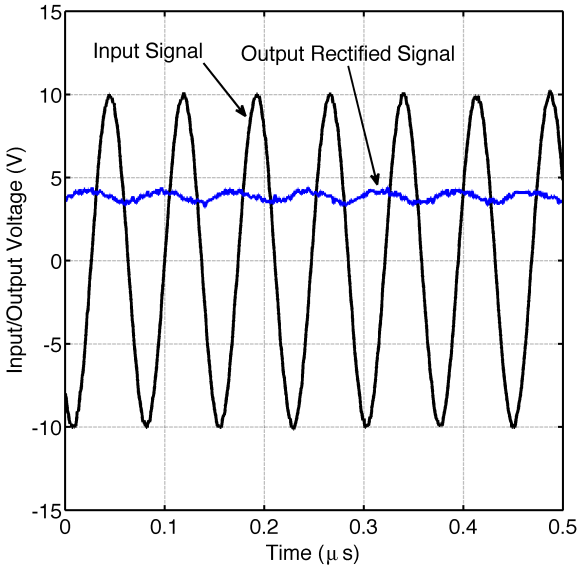

Fig. 9.7 - Comparison between the input sine wave and the output-rectified signal.

The practical working setup is presented in Fig. 9.8, showing the connected circuit with three main components (rectifying diode, load capacitor and organic emitting diode). The OLED was successfully powered, emitting a green light.

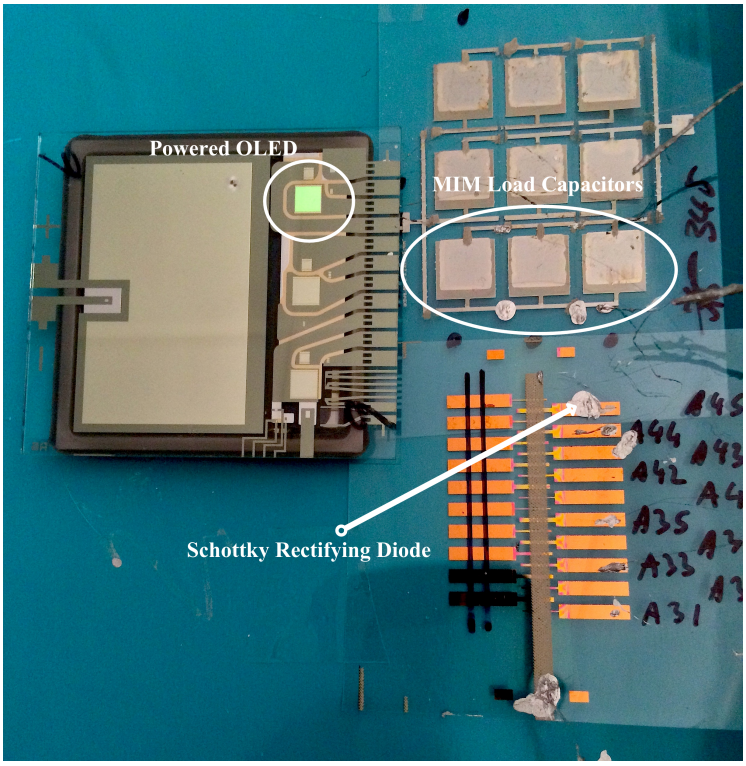

Fig. 9.8 - Experimental Working Setup.

9.4 CONCLUSIONS

The organic half-wave rectifier circuit was successfully implemented. The rectifier circuit was able to produce a DC signal with enough power to drive a light emitting diode. Although, the input power used is sill unrealistic for practical applications, the results are very promising and show the potential of the technology to make fully ink-jet printed RFIDs tags.

Chapter 10

CONCLUSIONS

Organic MISFETs and rectifying diodes fabricated by inkjet printing were electrical characterized and their performance assessed for applications in circuits.

This study focus in several aspects of the individual components, namely operational stability, degradation caused by ageing under ambient atmosphere and parameter variability.

While analysing device's individual parameters such as mobility, on/off ratio and threshold voltage, it was concluded that transistor parameters do not scale with the printed area. This is caused by two aspects; (i) a bad device design which is susceptible to lateral surface conduction and (ii) variations in the printed layer thickness. The re-design of the transistor layout eliminated the first source of error.

The Operational stability was assessed. By coating both the dielectric surface and the silver electrode with a printed PFTP layer. The operational stability was improved by one order of magnitude (with respect to uncoated devices). It is conclude that the PFTP neutralizes electronic traps on the dielectric surface. The use of this passivation layer is crucial to achieve reliable transistors to be used in circuits.

The degradation under ambient atmosphere is strongly dependent on the semiconductor ink formulation used. The FS0027 is more stable that the FS0096 ink formulation. We propose that the reason for that lies on the solvents used in the preparation of the inks. While the FS0027 is prepared in a solvent that evaporates slowly (high boiling point solvent) the FS0096 is prepared in a solvent that evaporates fast. The fast evaporation rate may cause pinholes which reduces the barrier to water permeation from the atmosphere.

Inverter circuits with a gain of -3 and NAND logic gates were characterized. Although, the inverter gain is enough to make simple oscillators, the dynamic response of circuits is still poor, operating below 1 Hz frequency. We believe the reason for this slow operation speed is caused by the large parasitic capacitance between gate, and source/drain terminals.

Different types of organic rectifying diodes were characterized. MIS diodes Schottky diodes, and diode connected transistors.

Schottky diode have a high on/off current ratio, low capacitance and were capable of rectifying an AC sinusoidal wave at 13.56 MHz .

An organic half-wave rectifier circuit was successfully implemented by connecting an Schottky diode and MIM capacitor. The rectifier can operate for input signals at 13.56 MHz and was able to produce a DC signal with sufficient power to drive an OLED. The inclusion of this rectifying circuit in a RFID tag is discussed.

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