UNIVERSIDADE DO ALGARVE

Light-induced effects on oxide based thin film transistors

André Lança Cardoso

Dissertação

Mestrado Integrado em Engenharia Eletrónica e Telecomunicações

Trabalho efetuado sob a orientação de:

Prof. Dr. Henrique Leonel Gomes

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Agradecimentos

Gostaria de começar dizendo que estou eternamente grato a todas as pessoas que fizeram de alguma maneira parte do desenvolvimento desta dissertação de Mestrado. Pois através do estímulo e ajuda prestada a conclusão deste projeto foi certamente mais fácil do que o inicialmente previsto. A todos eles um grande obrigado.

Gostaria de agradecer ao meu orientador, o Prof. Dr. Henrique Gomes, por ter aceitado o meu pedido para me orientar, e que com isso eu pudesse fazer este trabalho que gostei tanto e que me ajudou imenso para a minha vida futura, pois foi um trabalho muito integrado na minha área de interesse. Gostaria também de agradecer ao orientador, por todo o conhecimento que me passou, tanto nas aulas, como depois na orientação da dissertação e também por estar disponível para o esclarecimento de todas as dúvidas que foram surgindo.

Queria também deixar uma palavra de amizade a todos os meus amigos, que me acompanharam ao longo do projeto, tanto pela companhia, como pela entreajuda prestada em todos os momentos, não só durante a dissertação, mas durante totalidade do mestrado.

Gostaria também de mostrar o meu agradecimento à minha namorada pelo apoio dado principalmente na altura mais crítica, que coincidiu com o inicio da escrita da dissertação.

Por último gostaria de deixar aqui uma palavra de apreço a minha família, pois sem eles nada era possível. Pela ajuda desde o primeiro dia do curso até à conclusão desta dissertação, pelo apoio emocional que me foi prestado, e pelos valores que me foram ensinados, que me fizeram aquilo que sou hoje.

A toda a gente referenciada acima dedico todo este trabalho.

Acknowledgements

I would like to start saying that I am eternally grateful for all the people that somehow made part of the development of this Master degree dissertation. With the stimulus and the assistance provided, the conclusion of this project was certainly easier than initially expected. To all of them a great thank you.

I would like to express my acknowledgements to my adviser, Prof. PhD. Henrique Leonel Gomes, for chosen me as his guiding student in the dissertation theme. With that I was able to work in the area that I adore and with that helped me in my future career with more experience. I would like to thank my teacher for all the knowledge that he passed to me, through his classes or in the lab doing my dissertation. His availability when I needed some help, had great value to me also.

I wish to express my gratitude to all my friends that joined me in this journey, since the beginning of the course until the end of the project. Their companionship and help in all the moments was of great importance to me.

I also want to say a word of gratitude to my girlfriend for the support given, a critical time when the writing of this dissertation begun.

For last I could say some words of gratitude to my family, because without them, nothing of this could be possible. For their help since the first day until the last of the course, for the emotional support that they gave to me and for the values they passed me, made the conclusion of my course possible.

To all of the referenced above, I dedicate all my work.

"Coisas boas vêm com o tempo. As melhores, vêm de repente!"

Denise Lessa

Resumo

Este trabalho incidiu sobre a análise elétrica dos transístores com base em óxidos semicondutores. Esta é uma área emergente e tecnologicamente relevante. Numa primeira fase a dissertação aborda com detalhe, os aspetos essenciais dos transístores com base em óxido semiconductor: Discute-se a sua origem, estrutura, os métodos de fabrico e as aplicações. Depois desta introdução, os efeitos da exposição à luz nas propriedades elétricas dos transístores são apresentados e discutidos em detalhe.

Foram estudados transístores preparados através de uma solução líquida de ureia. Este processo de fabrico torna possível imprimir ou depositar o semicondutor em substratos flexíveis e de baixo custo, abrindo um conjunto de novas oportunidades para tecnologia eletrónica com base em óxidos amorfos semicondutores. Até recentemente esta possibilidade de imprimir eletrónica era apenas possível com transístores orgânicos.

Os problemas relacionados com a exposição de luz em transístores de óxidos amorfos tem sido estudados na literatura e atribuídos a interação de cargas elétricas com defeitos no semiconductor. Este tipo de defeito é conhecido por lacunas de oxigénio.

Estes defeitos eletrónicos foto-induzidos afetam a performance do transístor e modificam temporariamente os seus parâmetros, nomeadamente a mobilidade de efeito de campo, a tensão de arranque, a condutividade elétrica, as correntes de fuga e a estabilidade operacional.

Os resultados obtidos nesta dissertação mostram que a exposição prolongada à luz com energia igual ou superior ao *hiato* do *ZTO* induzem estados dopantes duradouros. Estes estados dopantes estão localizados aproximadamente a 0.14 eV do limite da banda de condução. É proposto que as espécies químicas responsáveis pelos estados induzidos pela luz, sejam os espaços não ocupados do oxigénio ionizado. Porém, mais experiências são precisas para provar esta proposta. A iluminação afeta também a estabilidade operacional do transístor. Transístores submetidos à iluminação sofre de uma rápida variação da tensão de arranque. Transístores fabricados usando ureia são mais instáveis do que que transístores fabricados usando técnicas de sublimação térmica. Estas diferenças de comportamento são atribuídas à presença de defeitos eletricamente ativos. Sugere-se que estes defeitos estão localizados na interface entre o dielétrico e semicondutor.

Estudos da corrente que flui no transístor em função da temperatura revelam um comportamento anómalo. Foram detetadas dois tipos de anomalias uma devido aos estado induzidos pela luz e outra causada pela presença de uma quantidade residual de água na superfície do dielétrico.

Palavras-chave: Transístores de filme fino, óxidos amorfos semicondutores, defeitos eletricamente ativos, correntes termo-estimuladas.

Abstract

This work is focused on the electrical analysis of oxide based thin film transistors (TFTs). This is an emergent and relevant technology.

This dissertation will present and the basic background related with fabrication, characterization and operating mechanism of thin-film-transistors. The main core of this thesis is the study of light-induced effects.

The transistors under study are bottom-gate staggered TFTs using ZTO as semiconductor and a thin layer of silicon dioxide (SiO_2) as dielectric. Some of these TFTs were prepared using a solution of urea. By using this method the ZTO semiconductor can be made soluble and be deposited from a liquid solution using spin-coating methods or even be printed.

Light induces a number of electrical instabilities on oxide based TFTs. According to the literature these effects are caused by trapping of photo-induced holes, or ionized oxygen vacancies Light exposure affects a number of TFT parameters, such as the field-effect mobility, the threshold voltage, the bulk conductivity, the off-current and the operational stability.

Our results show that prolonged light exposure with energy equal or above the ZTO band gap induces long-lived dopant states. These dopants are located at 0.14 eV from the conduction band edge. It is proposed that the chemical species responsible for the light induced states are ionized oxygen vacancies. However, further experiments are required to prove this.

Temperature dependent experiments have also shown a number of anomalies in the TFT current. Some of these anomalies are caused by the neutralization of light-induced species. Others are caused by a residual water contamination on the dielectric surface. Water act as a deep trap and degrades the transistor operational stability.

Keywords: Oxide based TFTs, solution based TFTs, light effects, temperature dependence, traps, water anomaly.

Contents

Agradecimentos ii
Acknowledgements iii
Resumo v
Abstract vii
Index of Figures x
Index of Tables xiii
Abbreviations xiv
CHAPTER 1 - Introduction 1
Summary 1
1.1 Structure of the Dissertation 2
1.2 Contributions 2
1.3 Objectives 2
CHAPTER 2 - Thin Film Transistors (TFTs) 3
Summary 3
2.1 Introduction 4
2.2 Thin Film Transistors (TFTs) 5
2.3 Oxide Thin Film Transistors 6
2.3.1 History on Oxide TFTs 6
2.3.2 Physical Structure 8
2.3.3 Manufacturing techniques 9
2.3.4 Characteristic curves and TFT parameters 22
2.3.5 State-of-the-art of oxide based TFTs 27
2.3.6 Applications 32
CHAPTER 3 - Experimental methods 36
Summary 36
3.1 Introduction 37
3.2 Description of equipment operated 38

CHAPTER 4 - Light-induced effects on ZTO based TFTs 43
Summary 43
4.1 Introduction 44
4.2 Experimental 45
4.3 Results and discussion 50
4.3.1 Results and discussion of experiments in Transistor A - s10t33 50
4.3.2 Results and discussion of experiments in Transistor B - s10t22 54
CHAPTER 5 - Conclusion 62
Summary 62
5.1 Conclusions 63
5.2 Suggestions for further work 64
References 65

Index of Figures

Figure 2.1 - Basic structure of a FET. 4
Figure 2.2 - Comparison between the structure of a MOSFET and a TFT. Adapted from [2]. 5
Figure 2.3 - Cross section of a TFT [4]. 6
Figure 2.4 - Cut view of the four configurations of a TFT. 8
Figure 2.5 – Schematic example of vacuum evaporation [23]. 10
Figure 2.6 – Schematic example of sputtering in a plasma environment [23]. 11
Figure 2.7 – Schematic of a) Cathodic Arc Vapor deposition; b) Anodic Arc Vapor Deposition with a thermoelectron source [24]. 12
Figure 2.8 - Examples of Ion Vapor Deposition. a) Ion Planting with a filament vaporization source, b) with a sputtering source, c) with an arc source. d) Ion Beam assisted deposition in a vacuum environment [24]. 13
Figure 2.9 - Illustration a parallel plate Plasma-Enhanced CVD (PECVD) reactor [23]. 15
Figure 2.10 - Simple schematic of Dip-coating method [30]. 17
Figure 2.11 - The main stages of Dip-coating technique. Adapted from [31]. 18
Figure 2.12 - Basic schematic example of Spin-Coating method [30]. 18
Figure 2.13 - Main stages of Spin-coating technique [33]. 19
Figure 2.14 - Basic schematic of Spray-pyrolysis equipment [35]. 20
Figure 2.15 - Comparison between decomposition of a precursor solution by sol-gel synthesis and solution combustion synthesis [39]. 22
Figure 2.16 - I-V characteristics of an oxide TFT. 23
Figure 2.17 - Transfer Function in the linear zone. 24
Figure 2.18 - Different operating modes of a TFT. Adapted from [42]. 25
Figure 2.19 - Example of linearization (red) of the blue dotted transfer curve using $\gamma = 1$ [43]. 25
Figure 2.20 - Example of a change in mobility captured after comparing two transfer functions. 27
Figure 2.21 - Transparent PM chipLED [2]. 32
Figure 2.22 - AM Backplane with TFTs based on GIZO as semiconductor: a) AM backplane on glass; b) image of one of pixels (with a dimension of 350 by 350 µm); c) Integration of the AM backplane on an LCD frontplane [63]. 32

Figure 2.23 – 70 inches UD LCD 3DTV by Samsung [67]. 33
Figure 2.24 - Seven Stage RO based on ZnO TFT with 31 ns of propagation delay [70]. 34
Figure 2.25 - a) Picture of the oxide paper-CMOS; b) Transfer characteristics of the oxide paper-CMOS and gain [2]. 35
Figure 3.1 - Schematic diagram showing how the voltages and current sources are connected to the transistor. 37
Figure 3.2 - Electrical connections made using gold wires glued with conductive silver paint. 38
Figure 3.3 - Front view of Keithley 487 picoammeter/voltage source [74]. 39
Figure 3.4 - Front view of Keithley 6487 picoammeter / voltage source [76]. 39
Figure 3.5 – a) Photograph of the rotary pump [77]; b) turbo-molecular pump (Varian Turbo-V70) and its controller [78]. 40
Figure 3.6- a) Triax 320 spectrograph [79]; b) 450 W Xenon Lamp. 40
Figure 3.7 - Oxford ITC showing room temperature (RT). 41
Figure 3.8 - Cryostat where the temperature dependent experiments were made. 41
Figure 3.9 – a) Microprobes used to measure the TFTs; and b) the vacuum chamber that holds the TFTs inside a vacuum and dark environment. 42
Figure 4.1 – a) Photograph of the wafer with several TFTs and b) schematic representation showing the device geometry of Transistor A - s10t33 with dimensions of W = 2400 μm and L = 40 μm. 46
Figure 4.2 – a) Photograph of the wafer with several TFTs and b) schematic representation showing the device geometry of Transistor B - s10t22 with dimensions of W=1400 μm and L=100 μm. 46
Figure 4.3 - Experimental set-up used to characterize the TFTs. a) Configuration used to measure the Transistor A - s10t33; b) Configuration used to measure Transistor B - s10t22. 47
Figure 4.4 – Blue LED light intensity spectrum as function of the wavelength [88]. 48
Figure 4.5 - Simple schematic of transistor configured as capacitor. 48
Figure 4.6 - Photo-generated current on a ZTO TFT as function of the light wavelength. 49
Figure 4.7 - Current-voltage (*I-V*) characteristics of the TFT **A** - s10t33. 50
Figure 4.8 - The effect of 100 s long pulse of blue LED light on the linear transfer curves. 51
Figure 4.9 - Effect of the blue LED light on TFT off-current ($Vg = 0\ V, VDS = 0V$). 52
Figure 4.10 – a) Consecutive Transfer functions recorded after 100s of light exposure; b) *I-V* characteristics after light exposure. 53

Figure 4.11 - TFT transfer functions before, immediately after light exposure and after 19 hours of resting under vacuum and dark conditions. 54
Figure 4.12 – The electrical properties of the TFT **B**. a) Transfer curve in the linear region with VDS = 0.25 V and b) the corresponding I-V characteristics. 55
Figure 4.13 – Comparison of the transfer curves before and after light exposure. a) Transfer curves before and after light exposure; b) VTs before and after light exposure, after linearization using a γ=1.. 56
Figure 4.14 - Comparison of TSCs taken upon light exposure and baseline (dark conditions). 57
Figure 4.15 Transfer curves measure before and after TSC experiments. a) Linear transfer curves as-recorded; b) Linear transfer curves linearized using γ =1. 58
Figure 4.16 – a) Temperature dependent current before and after light filling; b) Both curves are plotted as an Arrhenius graph. 58
Figure 4.17 - Activation energy and conduction bands in a light and dark situation............... 59
Figure 4.18 - Current decays of the light-induced states. The TFT was previously exposed to light and then kept in the dark while the time dependence of the current is monitored. 60
Figure 4.19 - Anomalies in the temperature dependence of the IDS current caused by super-cooled trapped water. The anomalies are highlight by the arrows and locate below 200 K and at 240-250 K.. 61

Index of Tables

Table 2.1 - Summary of the major CVD processes [26]. 14
Table 2.2 - Solution type and coating methods used to currently produce solution based TFTs [2]. 28
Table 2.3 – Recent and most relevant work on multiple solution-processed oxide n-type semiconductor. 29
Table 2.4 - Recent work on multiple oxide p-type semiconductors.. 30
Table 2.5 - Resume of recent state of the art on oxide TFTs from year 2015. 31

Abbreviations

3DTV	3-Dimensions Television
Al_2O_3	Aluminium(III) oxide
AM	Active Matrix
AT-ZIO	Al–Sn–Zn–In–O
CCD	Charge Coupled Device
CENIMAT-I3N	Centro de Investigação de Materiais - Instituto de Nanoestruturas, Nanomodelação e Nanofabricação
CMOS	Complementary Metal-Oxide Semiconductor
CSD	Chemical Solution Deposition
Cu_xO	Copper Oxide
CVD	Chemical Vapor Deposition
DC	Direct Current
FET	Field Effect Transistor
GIZO	Gallium Indium Zinc Oxide
HIZO	Hafnium Indium Zinc Oxide
HUD	Head-Up Display
IBAD	Ion Beam-Assisted Deposition
IGO	Indium Gallium Oxide
In_2O_3	Indium(III) oxide
ITC	Intelligent Temperature Controller
IZO	Indium Zin Oxide
IZTO	Indium Zinc Tin Oxide
LCD	Liquid Cristal Display
LED	Light Emitting Diode
NBIS	Negative Bias Illumination Stress
NBS	Negative Bias Stress
NMOS	N-channel Metal Oxide Semiconductor
OLED	Organic Light Emitting Diode
PBIS	Positive Bias Illumination Stress
PBS	Positive Bias Stress

PM	Passive Matrix
PSG	Phosphosilicate Glass
PVD	Physical Vapor Deposition
RF	Radio Frequency
RO	Ring Oscillator
RT	Room Temperature
SCS	Solution Combustion Synthesis
SiO_x	Silicon Oxide
S_nO_2	Tin Oxide
TCO	Transparent Conductive Oxides
TFT	Thin Film Transistor
TSC	Thermo-stimulated Current
TSiO	Tantalum Silicon Oxide
UBMS	Unbalanced Magnetron Sputtering
V_{th}	Threshold Voltage
Z_nO	Zinc Oxide
Z_rO_2	Zirconium dioxide
ZTO	Zinc Tin Oxide

CHAPTER 1 - Introduction

Summary

This chapter provides the introduction to this dissertation. It will cover the structure used to separate the topics and the people that contributed with help. Finally it will be presented the main objectives of my work.

1.1 Structure of the Dissertation

This dissertation will consist in 5 chapters. The Chapter 1 speaks about the objectives and the structure of the dissertation. Chapter 2 is completely theoretical. It starts on the basic Field Effect transistor moving to the oxide based Thin Film Transistors. Here it will be talked about the origin, physical structure, manufacturing process and applications of our TFTs. Chapter 3 it will cover experimental methods and the materials used in the experiments. Chapter 4 it will be focused on the primary goal of the dissertation. It will evaluate the light effects on our transistors. Finally a Chapter 5 will sum up and properly conclude all the aspects talked about in the dissertation.

1.2 Contributions

I want to thank my lab colleague Fábio Cabrita for helping me during my dissertation. We discussed some problems and solutions about the subject, taking the advantage for our works being very similar. Also thank him with his assistance in some measurements at the beginning of my work at the laboratory. Furthermore I want to express my gratitude for all the transistors made available from Asal Kiazadeh (CENIMAT) for test purposes. Also from all the information about these transistors that was shared by Daniela Salgueiro (CENIMAT). Finally I wanted to thank all the knowledge shared by my supervisor Prof. Dr. Henrique Gomes.

1.3 Objectives

The main goal of this dissertation is to study the light-induced effects on oxide based thin film transistors. It is important to observe and understand the anomalies of exposing light to this particular type of TFT. For that is important to electrical characterize the transistor and understand its properties to analyze why the light is inducing defects and anomalies on the transistor. For that is important also to know all the theory involving the oxide based devices and because of that a detailed Chapter will be talking about them.

CHAPTER 2 - Thin Film Transistors (TFTs)

Summary

This chapter provides a review of thin film transistors. It covers be covered aspects related with history, physical structure, manufacturing techniques, electrical properties and technological applications.

2.1 Introduction

Transistors are present in most electronic devices. Nowadays, they are the component most used in all that devices because of its characteristics.

The general type of transistor that is going to be discussed on this dissertation is the Field Effect Transistor. Namely the Thin-Film-Transistor (TFT). This transistor is similar to the well-known MOSFET transistor used in our electronics. Therefore we will use the MOSFET structure and operating principles to introduce the TFT. However, we have to keep in mind that there are some important differences between the two transistors. These will be discussed later.

A transistor has three electrical terminals: the source, the drain and the gate. The rest of the structure is completed with the substrate. The basic structure of a MOSFET is shown in Figure 2.1.

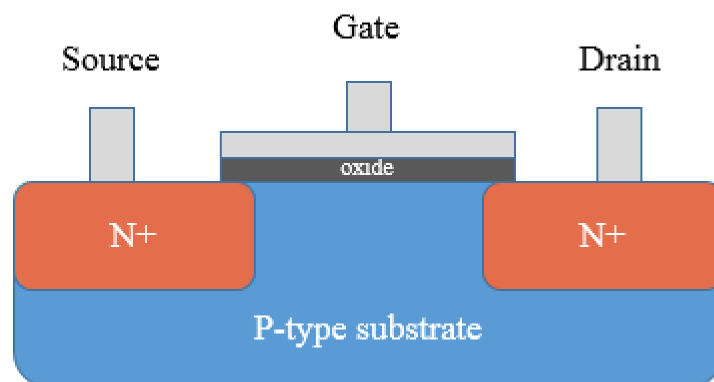

Figure 2.1 - Basic structure of a FET.

Now we can take a close approach on how a transistor really works. If applied current on source, with no voltage potential on the gate, with will be no flow of current from source to drain, because electrons simply cannot pass through the substrate by themselves. However if there is a positive voltage into the gate terminal, a positive electrical field appears, which attracts electrons from the n^+ regions (where they are in abundance) to the channel region, repelling holes down. Now these electrons form an n-channel along with the two n^+ regions on the substrate, which allows the passage of the current from source to drain. By increasing the voltage potential in the gate, the charge density increases and higher current will flow between the source and drain terminals [1].

2.2 Thin Film Transistors (TFTs)

In this section the basic operation of the TFT is introduced. TFTs are a type of Field Effect transistor, the main difference is on the way the layers are organized or deposited to make the actual transistor. The manufacture technique of this transistor is basically depositing layers/films of a semiconductor, insulator, metal contacts of the gate, source and drain and for last, a supporting substrate. Figure 2.2 shows the major differences in structure between a TFT and a MOSFET.

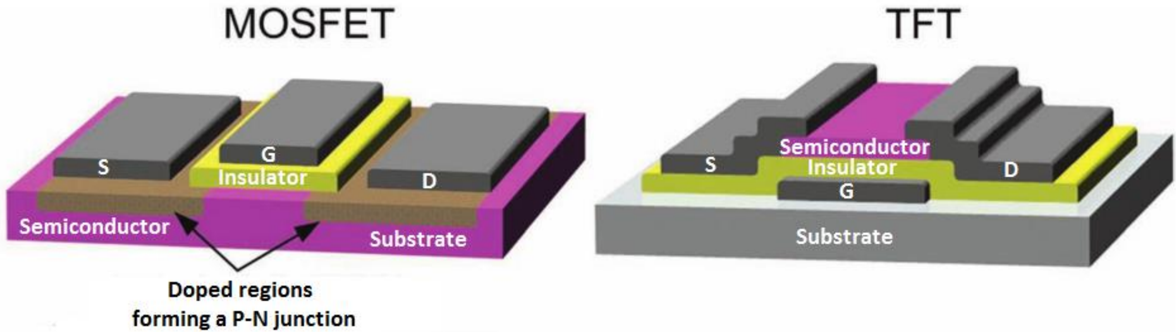

Figure 2.2 - Comparison between the structure of a MOSFET and a TFT. Adapted from [2].

Despite that in terms of operation TFTs and MOSFETs are quite similar, some major differences still exist between these two devices. Primary, as already seen, the TFTs use an isolated substrate, and in MOSFETs a wafer of silicon is used, and acts as both as substrate and semiconductor. MOFETS are fabricated using crystalline silicon while TFTs are usually made from amorphous semiconductors. This is the reason why MOSFET outperform TFTs. The manufacturing is also very different. MOSFETs require temperatures as high as 1000º C to create the dielectric layer. TFTs can be fabricated at room temperature (RT) and do not require ultra-clean conditions [3].

It is also important to note that the TFTs do not possess p-n junctions like MOSFETs, and this influences the device operation. Although both devices rely on the Field Effect to modulate the conductance of the semiconductor near to its interface with the insulator. TFTs

use an accumulation[1] layer and the MOSFETs used an inversion[2] region formed close to that interface [2].

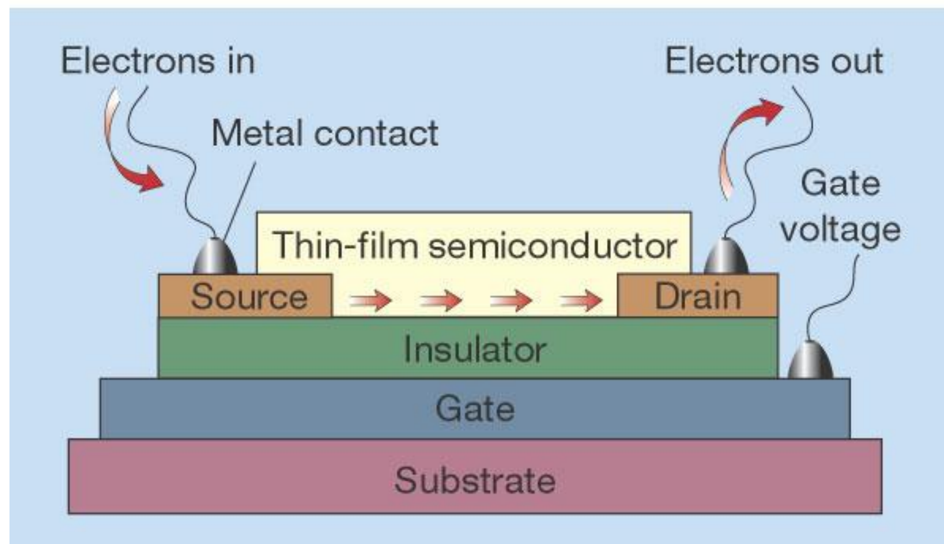

Figure 2.3 - Cross section of a TFT [4].

2.3 Oxide Thin Film Transistors

Many materials can be used as semiconductor, the most used one is definitely silicon. But for the purpose of this dissertation we will give the most attention to oxide semiconductors. An oxide TFT is just like a regular TFT. The main difference resides in the material used in the electron channel, which is an oxide semiconductor.

2.3.1 History on Oxide TFTs

As we know the main semiconductor used is silicon, and with his success it is going to remain the top semiconductor technology for the next following years [5].

However that did not prevented people from around the world from testing a different type of semiconductor material as channel layer. Let us start in 1964 when Klasens and Koelmans proposed a TFT that contained an evaporated SnO_2 as semiconductor on glass, with source, drain and gate made of aluminium, and an anodized Al_2O_3 dielectric [6]. The results on the performance of this experiment were not very detailed, because their main objective was to demonstrate a self-aligned lift-off process.

[1] Accumulation occurs for negative charges. Negative charges applied on the gate of the transistor attracts holes from the substrate (when substrate is p-type) [94].
[2] Inversion occurs for voltages greater than the threshold voltage. This region occurs because the minority carriers are attracted, by the positive gate voltage, to the interface (in a p-type substrate) [94].

In 1968 Boesen and Jacobs used a lithium doped ZnO single crystal semiconductor in their TFT, with also evaporated SiO_x dielectric and aluminium source, drain and gate. The results were not so good because the TFT showed a low drain to source current (I_{DS}) modulation when applying a voltage in the gate (V_G) and also no signs of I_{DS} saturation were observed [7]. Similar poor results were reported by Aoki and Sasakura back in 1970, while testing a TFT with SnO_2 as semiconductor [8].

Later in 1996 the oxide semiconductors as reappeared as channel layers, in the hands of Prins et al. with $SnO_2{:}Sb$ as semiconductor and by Seager with In_2O_3. Both were not aiming to show electric performance reports on these TFTs but either way Prins et al. reported a low on/off ratio of 60 [9], [10].

Was only in 2003 when first good results start appearing on TFTs with an oxide as semiconductor, in the reports on ZnO TFTs by Hoffman et al, Carcia et al. and Masuda et al [11]–[13]. The first two showed fully transparent devices with TCO (transparent conductive oxides) electrodes, with a respectable performance in terms of mobility, which reached 2.5 $cm^2V^{-1}s^{-1}$. The processing temperature of this semiconductor was still elevated (450-600 ºC), but Carcia et al. demonstrated that if RF magnetron sputtering was used to deposit the oxide, similar results could be achieved with room temperature processing of the semiconductor layer (not demonstrated on transparent TFTs) [2].

After these first tests on ZnO, more experiences followed after the year 2004 involving this semiconductor material. Numerous TFTs showing good performances in mobility while keeping processing temperature low (or RT) [14]–[16], non-vacuum processes on the production of the ZnO layers [17], new methodologies getting the mobility on ZnO TFT [18], production of fully transparent ZnO TFTs at RT [19] were some of the cases. For this reason ZnO had an important role on the experiments as an oxide semiconductor.

Even so that experiments were on binary oxides like ZnO, in 2003 Nomura and his team suggested to use a single-crystalline semiconductor layer in the TFT named GIZO (Gallium-Indium-Zinc Oxide). This new layer obtained excellent results in terms of effective mobility (around 80 $cm^2V^{-1}s^{-1}$) a V_T around -0.5 V and an on/off ratio of 10^6 . Despite this was accomplished at a very high temperature (around 1400 ºC), this paper proved that high performance oxide semiconductors TFTs can be made [20]. In the next year they published a work that showed the enormous potential on oxide semiconductors (again with GIZO as semiconductor layer). Once more demonstrating a transparent TFT with a flexible substrate at

RT processing. Showing results, not as good as the single-crystalline GIZO from his last work. But still managed to get a saturation mobility of $9\ cm^2V^{-1}s^{-1}$ a V_T of 1-2 V and on on/off ratio of 10^3. These results were obtained due to the low sensitivity of these multicomponent oxides to structural disorder [21]. After Nomura and his team had this results the number of publications using oxide semiconductors have grown, namely ones using GIZO, IZO and ZTO.

Now it is frequent to see outstanding electrical properties on these TFTs, namely on mobilities above 10 $cm^2V^{-1}s^{-1}$, V_Ts close to 0 V and on/off ratios above 10^7. Nowadays the processing temperature of these TFTs are not driven by the semiconductor, but by the dielectric. So it is of extreme importance the study of the dielectric as well as the semiconductor material.

To conclude, it seems that TFTs based on oxide semiconductors can provide a reliable alternative to old (generic) TFT technology. They have the advantage of allowing transparence, low cost, low temperature and also high performance devices. [2]

2.3.2 Physical Structure

The physical structure of a classic TFT can be observed in Figure 2.3. But it is actually one of many configurations of producing a TFT. In fact we can see in Figure 2.4, four main configurations of arranging the layers in a TFT.

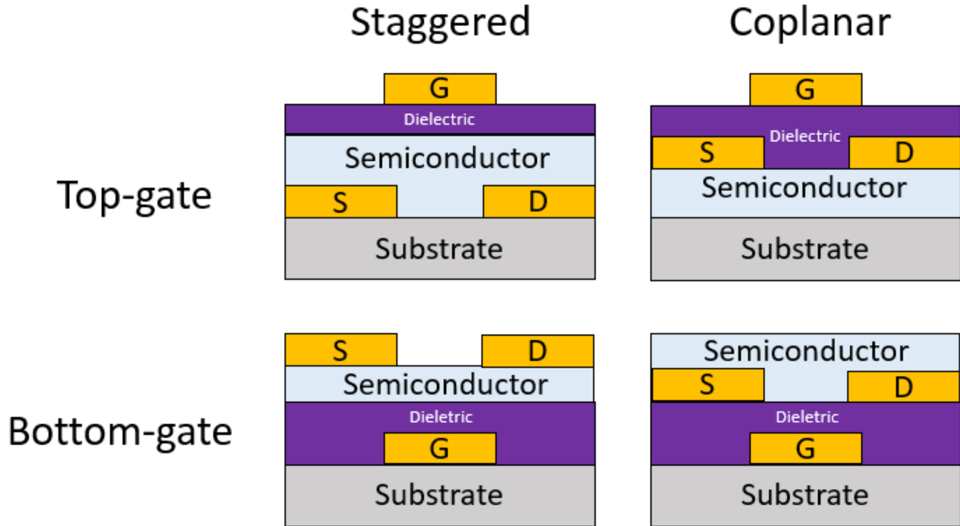

Figure 2.4 - Cut view of the four configurations of a TFT.

There are four categories of arranging the layers in a TFT. First division is in staggered and coplanar (If the drain/source electrodes are on opposite sides or on the same side of the

semiconductor relative to the gate). Then is in top-gate or bottom-gate, depending where the gate contact is in the structure.

The use of the materials on the semiconductor will dictate what configuration is more advantageous. If we produce TFTs with a-Si:H (Hydrogenated amorphous silicon), the best configuration is the staggered bottom-gate, because the processing is easier and the electrical properties are better. Taking convenience the fact that a-Si:H is light sensitive, the advantage of this type of configuration is mostly seen in the in LCDs. Mainly because the gate shields the semiconductor material from the back light effect on these displays.

If we produce a coplanar top-gate, normally it is used Poly-Si (Polycrystalline silicon) as semiconductor. The crystallization process of this semiconductor needs high temperatures that could damage other materials in the other layers of the TFT previously deposited. This does not happen if the semiconductor is flat and a continuous film with no layers beneath it.

In bottom-gate structure (staggered and coplanar), the semiconductor is exposed to the air. This can infiltrate some particles or impurities from the air that could carry instability effects in the channel, and therefore in the properties of the transistor [2].

The staggered structure has as main advantage, the reduction of the electric field in the drain section. The reason is the fact that source/drain electrodes are made in opposite sides of the semiconductor relative to the gate, resulting in a reduced field-dependent leakage current and kink/bend effect. The coplanar structure has the advantage of minimizing the parasitic capacitance of the TFT, because the source/drain contacts are aligned with respect of the channel region [22].

In the experiments of this dissertation, it is only used the bottom-gate configuration, as will be described in Chapter 4.

2.3.3 Manufacturing techniques

In this chapter is going to be addressed the three main ways of making these TFTs, the Physical Vapor Deposition (PVD), the Chemical Vapor Deposition (CVD) and the Chemical Solution Deposition (CSD).

Physical Vapor Deposition (PVD) is a deposition process where the material is vaporized from the solid or liquid state into the form of atoms or molecules. Then it is transported (in vapor state) over a vacuum environment until reach the substrate, place where

its condensation occurs. These substrates can range in a variety of sizes from very small to very large, and can also range in different shapes, from completely flat to complex geometries [23].

The main PVD techniques are Vacuum deposition, Sputter deposition, Arc Vapor deposition and Ion Plating. These set of techniques are going to be explain below.

Vacuum deposition:

It is also known as vacuum evaporation and it is a process where the material from a thermal vaporization source arrives at the substrate with no collision with gas molecules in the space between them. This vacuum environment provides the ability to decrease the gas contamination in the system to a minimum level. The rate of thermal vaporization deposition use to be very high especially compared to other vaporization techniques. The thermal evaporation is mostly done with a thermal heated source that could be tungsten wire coils or a high energy electron beam. To finalize the substrates used are mounted at a distance from the evaporation source, with the objective of reducing the radiant heating of the substrate by the vaporization source [23].

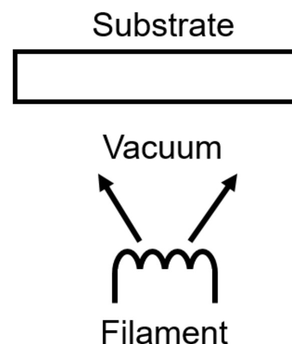

Figure 2.5 – Schematic example of vacuum evaporation [23].

Sputter deposition:

This kind of deposition also called “sputtering”, is the deposition of particles that got vaporized from a surface (also called target or source) by the sputtering process itself. Physical sputtering process is a non-thermal vaporization process. It ejects atoms from a solid surface by momentum transfer from an atomic-sized energetic bombarding particle. The distance from target to substrate is usually short compared to vacuum evaporation. Sputtering deposition can be done by energetic ion bombardment of a solid surface (target) in a vacuum using an ion gun. Additionally can be done by low pressure plasma (< 5mTorr) where the particles that have been sputtered experience low or no gas collision in that space between the target and the substrate.

It is also important to note that the sputter deposition can also be performed in a higher plasma pressure (5-30mTorr). In these conditions energetic particles that have been sputtered or reflected from the target are “thermalized” by gas phase collisions right before they reach the surface of the substrate. The sputtering target gives us a long-lived vaporization source that can be mounted so that can vaporize in any direction that we want [23].

Many variations of sputtering can be found in the literature as: DC diode sputtering, where a high negative DC voltage is set on a conductive surface in a gas. Then a plasma is formed filling up the container and positive ions are sped up to the surface; Magnetron sputtering use a magnetic field to confine the electrons near the surface; In reactive sputtering, reactive gases or gas mixtures are used, where the gas pressure is of extremely importance dictating if the substrate gets poisoning the target surface (too high pressure) or not even have a desired film composition (too low pressure); RF sputtering where Radio frequencies waves are used (usually in range of 0.5-30Mz); Ion Beam Sputtering where ion beams are used to deposit thin films. These ion beams can be constituted by the desired film material and be deposited directly into the substrate. Alternatively the ion beam can be an inert or reactive gas at higher energy and is directed at a surface target of the desired material; Finally we can distinguish UBMS (Unbalanced Magnetron Sputtering) where some of the electron ejected are allowed to escape by having a little bit of the magnetic field normal to the target. This configuration is very useful in reactive sputtering [24], [25].

Beside of this quick cover of sub-types of sputtering, some others exists.

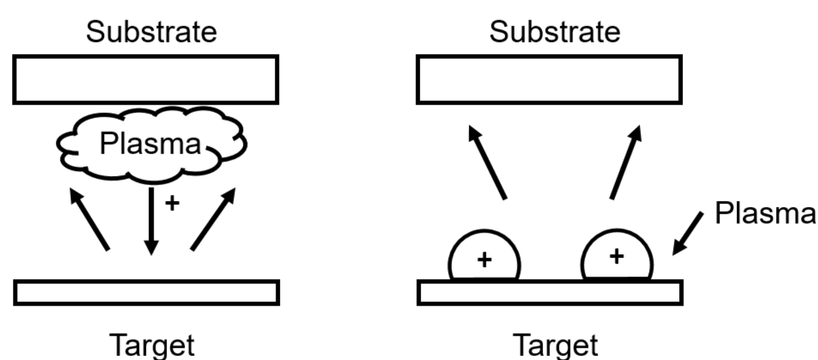

Figure 2.6 – Schematic example of sputtering in a plasma environment [23].

Arc vapor deposition:

This process utilize an excessive current and a low voltage arc to vaporize a cathodic electrode (negative pole) or anodic electrode (positive pole). Then the process deposit the vaporized material on the substrate. The material vaporized is hugely ionized and generally the substrate is biased in order to accelerate the “film ions” to the substrate surface [23].

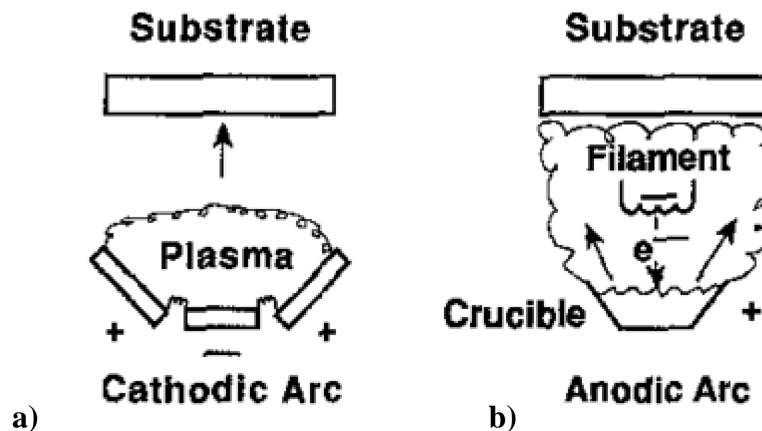

Figure 2.7 – Schematic of a) Cathodic Arc Vapor deposition; b) Anodic Arc Vapor Deposition with a thermoelectron source [24].

Ion vapor deposition:

Ion vapor deposition, also known as ion plating, uses concurrent or periodic bombardment of the film by atomic-sized energetic particles to modify the properties of the film to be deposited. In this type of deposition, the energy, flux and mass of the bombarding species as well as the ratio of bombarding particles to depositing particles, are very important variables to take into account. In terms of the depositing material it could be vaporized either by evaporation, sputtering, arc erosion or even by decomposition of a chemical vapor precursor[3]. The particles used for the bombardment are usually ions of a reactive (or inert) gas or from a condensing film material. The process can be done in different ways as with a plasma environment (where ions that are going to be bombarded are extracted from the plasma) or it may be done with a vacuum environment. In this last one, ions that are going to be bombarded are formed in an ion gun (this configuration is also known by ion beam-assisted deposition - IBAD). If a reactive gas is used in the plasma, films of compound materials can be deposit. For

[3] precursor – A precursor is a chemical substance that leads to another and more important substance [30].

last, it is important to note that ion vapor deposition can produce dense coatings at huge gas pressures, where the gas scattering can help enhancing the surface coverage [23].

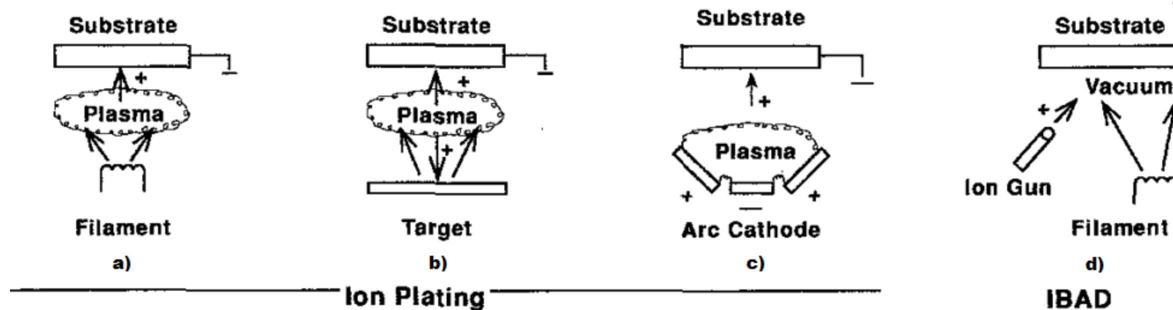

Figure 2.8 - Examples of Ion Vapor Deposition. a) Ion Planting with a filament vaporization source, b) with a sputtering source, c) with an arc source. d) Ion Beam assisted deposition in a vacuum environment [24].

Now it is going to be briefly explained other type of thin film deposition process that is also used on the manufacturing of these oxides TFTs. This deposition type is a non-PVD process called **Chemical Vapor Deposition (CVD).**

This CVD process is the deposition of atoms using high temperature reduction or decomposition of a chemical vapor precursor species, which incorporate the material to be deposited. That temperature reduction is consummated by hydrogen at a very high temperature. The decomposition of the chemical vapor is accomplished with thermal activation. The material that is going to be deposited may react with other gaseous species in the system to form compounds as oxides, nitrides, etc. The CVD process is usually attended with volatile reaction byproducts and not-used precursor species.

The deposition rate and film properties are in general affected by the nature of the reactants, the amount of energy applied, the ratio of reactants and the substrate temperature. The flow gas rates, the system pressure, the geometry of the chamber and the substrate surface preparation also affect the reactants nature. This technique has some advantages as all the layers produced are uniform, reproducible and adherent with no defects or impurities. It is also made at high rates in cheaper equipment. The disadvantages undergo as the high temperatures used in its processing and the use of chemical hazards caused by toxic, explosive, corrosive or inflammable gases [23], [26].

CVDs can also assume other name variations based on its function, and to facilitate, the following Table 2.1 will resume the major techniques of CVD.

Table 2.1 - Summary of the major CVD processes [26].

Name	Abbreviation	Description
Thermally-Activated CVD		
High-temperature CVD	HTCVD	The processing is under normal pressure conditions and at temperatures higher than 500ºC
Low-temperature CVD	LTCVD	The processing occurs under normal pressure conditions and its temperatures range below the 500ºC
Metalorganic CVD	MOCVD	The processing is based on the decomposition of an organometallic compound in a flow of a carrier gas, usually with the use of thermal energy.
Spray Pyrolysis	Spray Pyrolysis	The processing is based on the pyrolysis of a fine mist of an organic or aqueous solution of one or more metal salts on a top of a warmed substrate.
Low-Pressure CVD	LPCVD	The processing deposits thin films on heated substrates at high or low temperatures in a reactor but with reduced pressure.
Plasma-Enhanced CVD		
Plasma-Enhanced CVD	PECVD	The processing consists when a glow discharge is produced in the gaseous mixture (maintained at a pressure of 0.1 to 1 torr under an RF Plasma).
Plasma-Enhanced Metalorganic CVD	PEMOCVD	The processing is plasma-promoted using Metalorganic reagents, at RT and convenient growth rate, on a heat sensitive substrate.
UV Radiation-Enhanced CVD		
Photochemical-assisted CVD	Photo-CVD	The processing is based on the use of UV light to boost de decomposition of reactant gases at low pressure.
Photochemical-assisted Metalorganic CVD	Photo-MOCVD	This process deposits by using a vapor-phase ultraviolet dissociation of an organometallic source. It is usually accomplished by direct photolysis, irradiating with UV lamps
Laser-Induced CVD		
Laser-induced CVD	LCVD	This process can be accomplished using pyrolytic or photolytic decomposition of gaseous molecules, which usually use IR, UV or visible laser light.
Laser-induced Metalorganic CVD	LMOCVD	This process can laser-induce gas-phase photolysis and pyrolysis of metal alkyls and hexacarbonyls, forming a patterned metal deposit on the substrate.
Electron-Beam Assisted CVD		
Electron-Beam Assisted CVD	EBCVD	This processing uses an electron beam to create a spatially confined plasma reaction in a limited volume. The deposition occurs on a heated substrate.
Electron-Beam Assisted Metalorganic CVD	EBMOCVD	This processing uses the organometallic decomposition by electron beams to deposit films with a certain pattern. The beam is directed to the substrate which is surrounded by organometallic vapor.
Ion-Beam Assisted CVD		
Ion-Beam Assisted CVD	IBCVD	This processing uses a focused beam of ions to induce deposition from a convenient gaseous ambient.

Due to the high number of CVD methods, it was not given special attention to everyone. By example it will briefly be resumed the plasma-enhanced process.

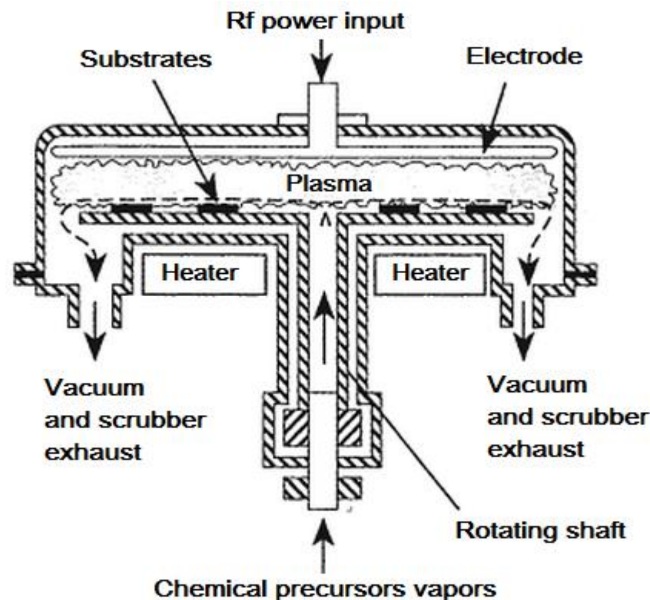

Figure 2.9 - Illustration a parallel plate Plasma-Enhanced CVD (PECVD) reactor [23].

It is known that the plasmas are used in the CVD process to activate and decompose the precursor species. More importantly they allow the deposition at a lower temperature than thermal CVD. This type was mentioned before as PECVD. Additionally these plasmas are usually generated by RF techniques. This can be observed in the Figure 2.9, showing a reactor that uses RF power to generate the plasma. This reactor is often used in the semiconductor industry to deposit silicon nitride (Si_3N_4) and phosphosilicate glass (PSG). Moreover it can encapsulate layers to the micron thick size and at a deposition rate about 5-100 nm/min. If the pressure level is kept low, the simultaneous bombardment of energetic particles during deposition affect the properties of the film deposited by PECVD [23].

Each TFT technique has its own advantages and disadvantages, but ultimately the choice from each one of the CVD process depends on the application, temperature limitations of the substrate and compatibility of the process with previous and consecutive processing steps [26].

CSD (chemical solution deposition) or chemical bath:

Chemical solution deposition or CSD is the deposition of a thin film of liquid precursor and consecutive thermal processing, in order to create the solid thin oxide film [27]. It is essential to manufacture the solution-based TFTs that will be covered in experiments talked in Chapter 4.

In CSD a method widely used is the well-known sol-gel for oxide films. In this method, a more-or-less viscous colloidal gel is deposited on top of the substrate by two ways: Dipping the substrate in the gel and slowly raising it from the solution (Dip-coating) or by Spin-coating. The thickness can be controlled by the viscosity of the sol and either by the rate of removal from solution or the rotation speed of the spin-coaster. Then the film is pyrolyzed to finally form the oxide [28].

The next topics will be focused on how apply this solution into a thin film.

The sol-gel formation is very advantageous in relation to CVD and PVD processes because it requires low-cost equipment that makes the all process affordable. Also another important aspects comparing with conventional coating processes is the ability to control the stoichiometry, homogeneity, the microstructure of the final films after drying. Additionally it can also control thermal treatment to form pure inorganic films. So knowing this, we understand that is necessary to control the influence of chemistry on deposition parameters. The mostly used methods to deposit sol-gel films are dip-coating and spin-coating. Next they will be examined with some detail [29].

Dip-coating:

In this process the coating fluid is inside a suitable tank and has a wire wrapped around the motor drum that is used to slowly withdraw the sample from the tank, as showed in Figure 2.10.

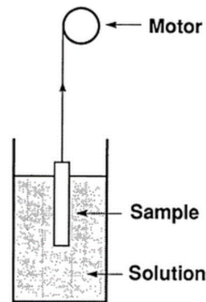

Figure 2.10 - Simple schematic of Dip-coating method [30].

The tank and the motor should be isolated on vibration damping equipment to guarantee that the liquid surface is fully undisturbed. The motor should be highest quality with a very smooth movement. The sample holder should be the simplest possible and not give drips on the sample during the withdrawal [30].

In order to the dip coating process to be successful, Scriven et al. [31] divided the process into five steps: Immersion, start-up, deposition, drainage and evaporation. The continuous process is much simpler then the all 5 steps, because it separates the immersion from the rest of the stages. Basically it eliminates start-up and hides drainage in the deposited film [32].

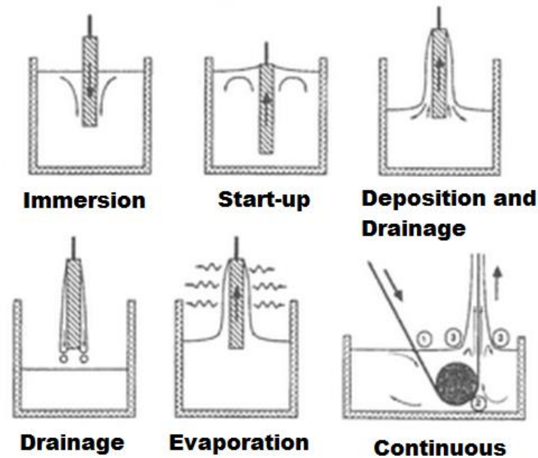

Figure 2.11 - The main stages of Dip-coating technique. Adapted from [31].

This method has some advantages over other coating methods. The fact that any size or shape can be coated, it is low cost and it is easy to keep the contamination at a minimum are one of them. However presents some disadvantages too as it needs to have a large amount of solution (especially to large substrates) and it is not a usable for multilayer systems due to cross contamination. Also it coats the both side of the substrate, which is undesirable if we only need one side [30].

Spin-coating:

Spin-coating is a very simple CSD method in which a precursor solution is handed out onto the substrate. Then this substrate is rotated at thousands of revolutions per minute to output a thin liquid film, as seen in Figure 2.12 [27].

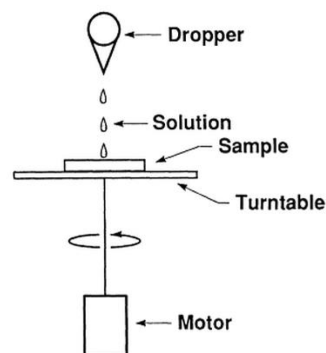

Figure 2.12 - Basic schematic example of Spin-Coating method [30].

The main controls in this process are the spin speed and the molarity of the precursor solution. Also the rotation is being inversely proportional and molarity is being proportional to the film thickness in the final form [27].

In order for spin coating to be efficient it has been divided in 4 stages (see Figure 2.13): Deposition: Where the solution is allowed to fall over the substrate from usually a micro syringe; Spin-up: Where the substrate is accelerated up to the desired rotation speed, and it is normal that exists some fluid expulsion from the substrate due to the rotation motion; Spin-off: Where the substrate is spinning at a constant rate and the fluid viscous forces command the fluid thinning action; Evaporation: Where the spin-off ends and the film drying begins. The centrifugal force stops and solvent evaporation commands the coating thinning behavior. The final two stages are the ones with most impact in the final coating thickness [33].

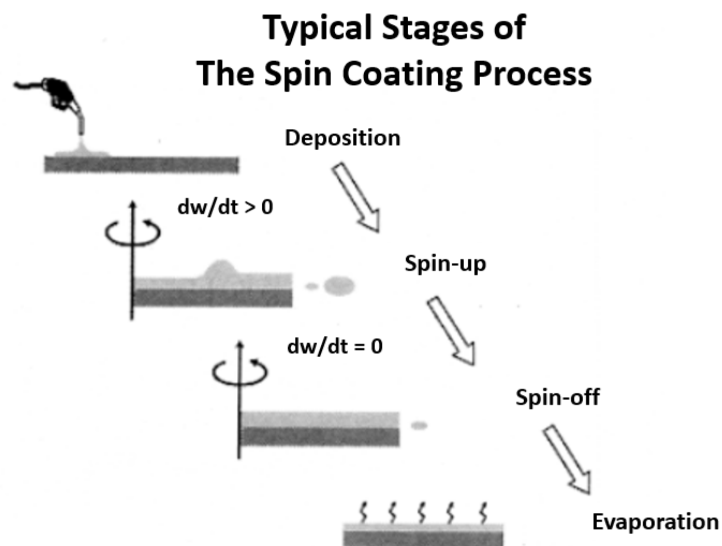

Figure 2.13 - Main stages of Spin-coating technique [33].

Spin Coating is decent because it is a fast and reproducible process that can give good film uniformities either on minor or large silicon wafers. Also, the film thickness can be controlled easily by changing the spin speed or switching to another viscosity photoresist. Another advantage of this process is the fact that is low cost.

The few disadvantages of spin coating are the fact that large substrates cannot be spun at a sufficiently high rate to allow the film to thin. Also spin coating technique is no well suited for non-circular substrates and non-planar surface topography substrates. But maybe the biggest disadvantage of all is the lack of material efficiency, in general only 2 to 5% of the material dispensed into the substrate is availed, the rest is waste [27], [33].

Side by side with these disadvantages, it still the possibility that some defects may appear after the coating. Such as the film staying too thin or too thick, the appearance of air bubbles on the surface, “comets”, lines, swirl pattern, uncoated sections, pinholes. All of these may appear if the material is not dispensed correctly, or exists some defects in the equipment or substrate [34].

<u>Spray-coating (Spray-pyrolysis):</u>

The spray coating process is utilized to prepare thin and thick films, ceramic coatings and powders. Therefore is one more method to be covered in this section. The technique is extremely easy to prepare films of any composition. It does not require high-quality substrates or chemicals, and it is been used for deposit dense films, porous films and produce powder.

The equipment in the Spray-coating method is quite simple, consists in an atomizer, a precursor solution, the substrate, the substrate heater and a temperature controller, as can be seen in Figure 2.14.

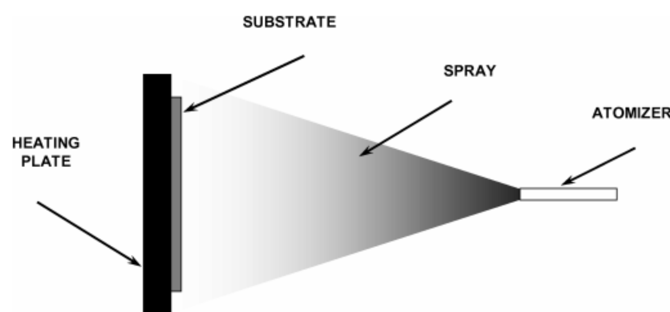

Figure 2.14 - Basic schematic of Spray-pyrolysis equipment [35].

The proceeding of spray-pyrolysis involves spraying a metal salt solution into the substrate. The droplets collide into de heated substrate surface, spread into a structure (with the shape of a disk) and go through thermal decomposition. The size and shape of the disk depends on the momentum, respective volume of the droplet and the substrate temperature. Also the film is generally composed of overlapping metal salt disks being converted in oxides on the substrate.

It is important to note that the quality and properties of the deposited film depends on the process parameters. One of them is the substrate surface temperature, the higher this one is rougher and more porous will be the films. Otherwise if temperature is too low the films will be cracked. Other parameter is the temperature of deposition that can influence the crystallinity

and texture of the deposited film. Lastly we consider the precursor solution the other important parameter since affects the morphology and properties of the deposited films [35].

Overall we can say that CSD has some interesting aspects as good stoichiometry control, the ability to cover large surfaces, cover a large range of thickness values (<10nm – 10um) and the advantage of needing very little equipment. The disadvantages resides in the high temperatures needed for crystallization (vary from 6 to 700ºC), the possibility of reactions with the substrate and the fact that the development of the precursor may be elaborate [36].

After this overview of this deposition techniques, it is important to introduce a method to prepare oxide materials. These method starts on a precursor solution and ends with an oxide. It is used to make the oxides used in the experiments from the next chapters.

Combustion Synthesis (CS) is also named Auto-Combustion. Depending on the experimental conditions can be described as solution combustion synthesis (SCS), gel-combustion synthesis, sol-gel combustion, etc. The diffusion of this technique has been huge and is due to the simplicity, the application range, the self- purifying feature and the ability to obtain products to a desired shape and size.

CS yields to solution combustion synthesis (SCS) if a precursor solution is used. That is the CS category of major interest for us, because our transistors used this method to prepare the precursor solution.

SCS is one of the most emerging methods for preparation of oxide materials. It basically consists in an aqueous solution of a redox system composed by nitrate ions of the metal precursor (called Oxidizer). Additional it has a fuel acting as reducing agent that can be urea, glycine, citric acid, carbohydrazide, maleic hydrazide. Then all is heated up to moderate temperatures (usually below 500ºC), and under dehydration, a huge exothermic redox reaction is created, that usually self-sustain and provide the energy needed to decompose all the organic materials and metal salts, and finally create the oxide [37], [38]. Figure 2.15 is illustrating what it needs to make the oxide and the difference of reaction by conventional sol-gel and the SCS explained above.

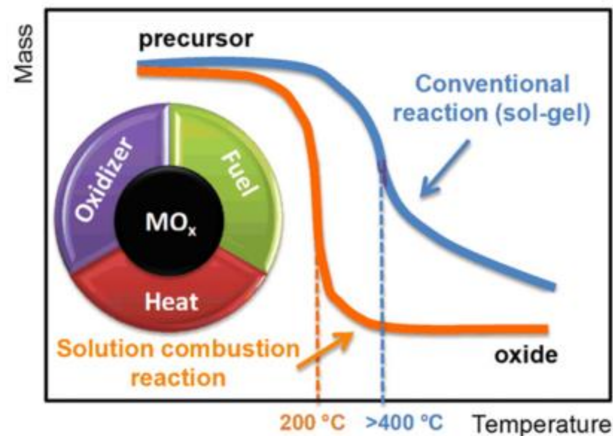

Figure 2.15 - Comparison between decomposition of a precursor solution by sol-gel synthesis and solution combustion synthesis [39].

2.3.4 Characteristic curves and TFT parameters

When analyzing these oxide TFTs (as well as regular TFTs) there are a set of graphics that are useful to our understanding of this devices. These graphics show really important information as current-voltage (I-V) characteristics, transfer curves, leakage current (I_{off}), threshold voltage (V_{th}) and mobility (μ).

I-V characteristics:

The graphics showing the I-V characteristics or I-V curves are of extreme importance when analyzing the behavior of a transistor. The I-V curves simply show the current between the drain and the source in function of the voltage between the source and the drain of the transistor V_{DS} , at the same time the V_G is also being controlled. For the process of seeing more information, we also apply range of V_G instead of just one, and with that more curves are observed. The information we extract after the processing is, once more, very important. It is possible to observe if the transistor is modulating the current. This happens when we have a linear zone, and a saturation region as is shown in Figure 2.16.

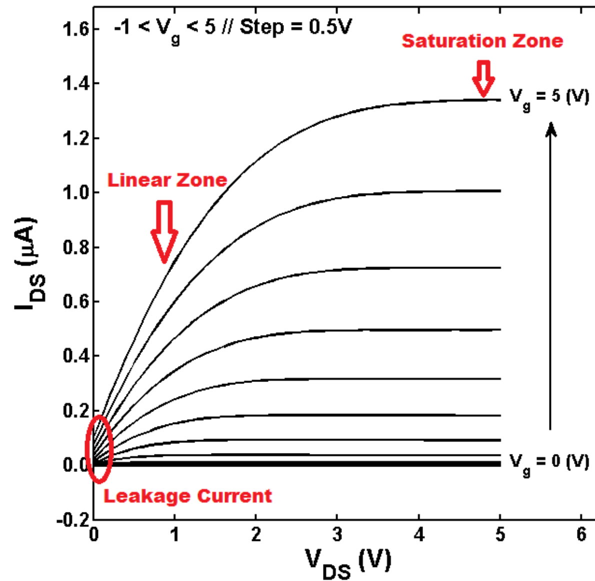

Figure 2.16 - *I-V* characteristics of an oxide TFT.

Other characteristic of the transistor visible in this type of graphic is the leakage current (I_{off}) also called off-current, evidenced when V_{DS} is 0 V. Leakage current is a bad parameter often observed when dealing with *I-V* curves. Normally this leakage is caused or by the manufacturing of the transistor itself. Since the TFT is layered with different materials, grain boundaries or intra-granular defects may be causing leakage currents. Other causes have been attributed to the leakage current such as the semiconductor being doped, the existence of a parallel conducting path through the semiconductor bulk layer and possibly the conducting path through the surface [40]. This problem has been addressed and a new device structure called triple gate has already been proposed by other authors. It was demonstrated that this structure significantly decreased the pseudo-subthreshold conduction leading to a huge reduction on the leakage current when comparing to the conventional TFT [41].

Transfer Functions:

Transfer curves are very useful because they allows us to extract a lot of information with just one curve. The process of plotting a transfer curve is very simple, first we establish in which zone we are going to evaluate the transistor, for example it could be in the linear region as in the Figure 2.17, then we fix a value of the V_{DS} and then we vary the values of V_G, and measure the current I_{DS}. The data extracted from this type of plot is the threshold voltage (V_{th}),

mobility (μ), activation energy (Ea), etc. Also the same analysis can be done in the saturation region, by simply changing the value of the V_{DS} to a higher one.

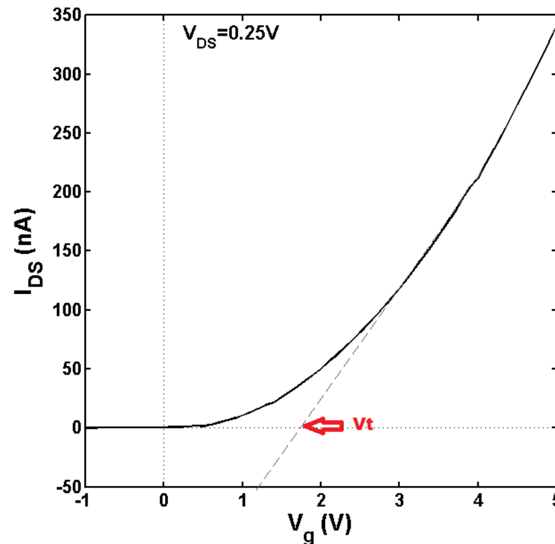

Figure 2.17 - Transfer Function in the linear zone.

Important parameters essential to the understanding of the transistor (that we extract from our curves) are going to be analyzed in detail in the next paragraphs.

V_{th} (Threshold Voltage or V_{ON}):

This parameter correspond to the V_G for which a conductive channel is formed between the source and the drain (channel), in other words corresponds to the V_G where the current (I_{DS}) starts increasing substantially. With this parameter we can conclude in which mode the transistor is working. If for example we have an n-type TFT and the V_{th} is positive the transistor is designated in enhancement mode, otherwise the transistor is in depletion mode, as we can see in Figure 2.18. In an enhancement mode transistor, we have to get $V_G > V_{th}$ to enhance the conductivity and make it conduct through the channel. In a depletion mode transistor, a $V_G = 0$ still finds the transistor conducting and therefore we need to apply some negative voltage in the gate to deplete the channel and turn it off [42]. Usually the enhancement mode is better for circuit operation, because no V_G is needed to turn off the transistor, this results in a much simpler circuit design and much less power dissipation [11]. In terms of its representation in a graphic, V_{th} is extracted simply making a straight line from where the curve is fairly straight to the x-axis, then the interception of the straight line with the x-axis gives us the V_{th} point. This point can also be seen in Figure 2.17.

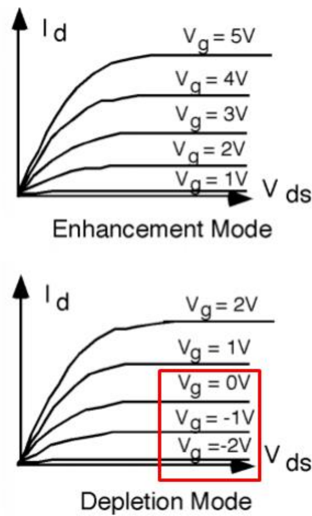

Figure 2.18 - Different operating modes of a TFT. Adapted from [42].

Another way of observing threshold voltage changes is by linearizing the transfer curve. This is special useful when a set of linear transfer curves are plotted and they are curved the whole time. So it is difficult to compare the V_{th} between them as well as mobility. The equation used is $\propto = 1/(1+\gamma)$, where γ is the value set up by us in order to make the linearization a straight line. Then when $\propto$ is found, the new currents (I_{DS}) are calculated as $I_{DS} = {I_{DS}}^{\propto}$. Then for final plotting, we use the *polyfit* function of Matlab® on these new currents to produce the final linearization, as can be seen in Figure 2.19. If $\gamma = 1$, $\propto$ will be ½. Its representation in y-axis has to be $\sqrt{I_{DS}}$. The result is a straight line as we intended.

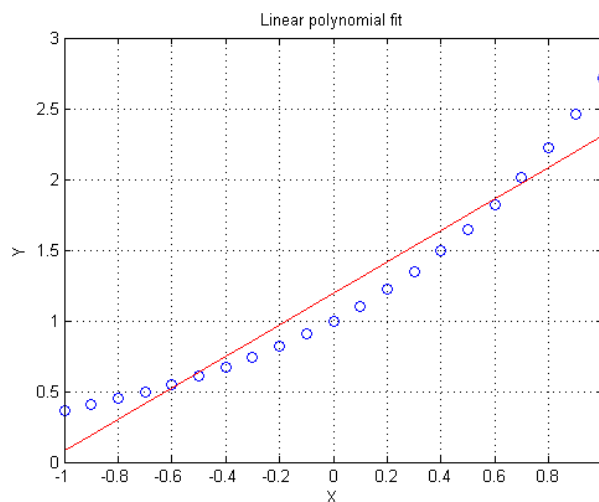

Figure 2.19 - Example of linearization (red) of the blue dotted transfer curve using $\gamma = 1$ [43].

Mobility (μ):

Mobility is a parameter of the transistor also visualized in the transfer function. It represents the efficiency of the carrier transport in the semiconductor material. The mobility is affected by scattering mechanisms, such as lattice vibrations, ionized impurities and grain boundaries. Also other structural defects from the interface material may affect. In a TFT additional sources of scattering should be considered, mainly because the movement of the charges is constrained to a narrow region. These additional sources are for example the Coulomb scattering from the insulator charges and interface states or the scattering provoked by the roughness of the surface. Although the scattering may be a general problem, in the specific case of a TFT, it has a low influence for some particular bias conditions, mainly because the mobility is modulated by V_G [2], [44], [45].

The mobility can be extracted from the transfer curves in the linear or alternatively in the saturation region.

Field Effect mobility (μ_{FE}):

$$\mu_{FE} = \frac{g_m}{C_i \frac{W}{L} V_{DS}} \qquad \text{Equation 1}$$

Where g_m is the transconductance of the transistor with low V_{DS} (linear zone).

Saturation Mobility (μ_{sat}):

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_{DS}}}{dV_G}\right)^2}{C_i \frac{W}{2L}} \qquad \text{Equation 2}$$

Obtained by the transconductance with high V_{DS} (saturation zone).

The μ_{FE} does not use V_{th} to its calculations, and therefore is easily calculated by the derivative of the transfer function. The μ_{sat} is less sensitive to contact resistance and does not require the calculation of V_T, however represents a situation where the channel is pinched-off [2].

In terms of the graphic, the change in mobility is observed by the change in slope of the transfer curve, as we can see in the Figure 2.20. If the curve has a high slope the transistor has a high mobility.

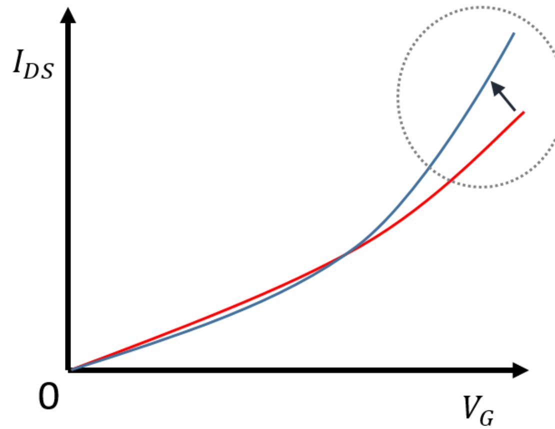

Figure 2.20 - Example of a change in mobility captured after comparing two transfer functions.

2.3.5 State-of-the-art of oxide based TFTs

State of the art on n-type oxide semiconductors:

In recent years the progress on the n-type oxide semiconductors has been huge. The semiconductors mostly used on those achievements were ZnO, ZTO, ITO, IZO, IGO, IZTO, IHZO and GIZO.

Actually the recent advances and state of the art devices are on solution processed n-type oxide semiconductors.

Nowadays methods of production properly working inorganics TFTs are based on sequential deposition of selected semiconductors, insulators and conductive materials. And as we know these processes involve high costs. The change to direct printing inorganic materials gives the opportunity to deposit films using direct additive patterning processes. That change will allow the manufacturing of high-performance devices at minimal cost.

Amorphous oxides semiconductors are the most used on high performing TFTs, showing high mobilities, and longer lifetimes. Only in recent times the inorganic materials, have been prepared from solution and deposited by spin coating or by ink-jet printed. In comparison with organic based TFTs it is very difficult to prepare ink-jet printable precursors [46]. Even though it is difficult, ink-jet printing has many advantages, as being a digital process, does not require masks or screen needs and being an additive process. Furthermore, has the advantage of being a non-contact process and the ability to apply the print where is desired.

Ink jet printing of inorganic materials are very rare compared to organic ones, because it is very difficult to prepare ink-jet precursors [46]. However, efforts have been made to surpass that problem and two main paths have been followed: nanoparticles precursor and molecular precursor.

Regarding the coating methods for solution processing, we have the spin coating, printing, and chemical batch deposition.

Regarding the nanoparticle approach that has been followed, the devices sometimes show instabilities, due to the large surface area of the nanoparticles. In the molecular precursors approach, exists the advantage of associate different metal precursors on the same solution [2].

This can be resumed in this following table:

Table 2.2 - Solution type and coating methods used to currently produce solution based TFTs [2].

Solution Type	**Coating method**
Nanoparticles	Spin-coating
Molecular precursor	Printing
	Chemical Bath Deposition

Next a list of the most recent advances on solution based n-type oxide semiconductors is presented.

Table 2.3 – Recent and most relevant work on multiple solution-processed oxide n-type semiconductor.

Material	**Process**	**Temperature [ºC]**	**Mobility** $[cm^2V^{-1}s^{-1}]$	**Reference**	**Year**
ZnO	Spray Pyrolysis	400	85	[47]	2011
GIZO	Spin Coating	95-hydrothermal[a]	7.65	[48]	2010
GIZO	Sol-gel spin coating	400	5.8	[49]	2010
IZO	Spin coating[b]	230	10	[50]	2011
ZTO	Auto-combustion	250	1.76	[51]	2011

[a] - 180ºC at 10 atm

[b] – "sol gel on chip" - In this method a more controlled low-temperature processing is applied from metal alkoxide precursors that, without mediated hydrolysis, would only decompose at higher temperatures [2].

As can be seen from Table 2.3, the multicomponent oxides are the ones that gave the best performance and with the lowest processing temperature possible. These TFTs are almost approaching the ones fabricated from thermal sublimation methods. The overall trend of these works is to lower the processing temperature but maintaining a good performance. If the processing temperature is low, it would be possible fabricate low cost circuits on plastic and on paper substrates. [2]

The TFTs characterized in this dissertation are based on solution based processes.

State of the art on p-type oxide semiconductors:

The n-type oxide TFTs are currently reported they have high mobility and they are reasonable stable. However p-type semiconductor oxides are very difficult to obtain.

Achieving high performing p-type oxide TFTs will provide a new era in the flexible and rigid substrates, and move away from the mostly used silicon substrate. But is still a long way to go.

There are a few articles published on p-type oxides. Table 2.4 briefly outlines the major published work on the area.

Table 2.4 - Recent work on multiple oxide p-type semiconductors.

Material	Process	Temperature Dep/Post[4] [ºC]	Mobility $[cm^2V^{-1}s^{-1}]$	Reference	Year
Cu_xO	PLD	500	4.3	[52]	2010
Cu_xO	PLD	500	2.7	[53]	2011
SnO_x	Rf sputtering	RT/200	1.2	[54]	2010
SnO_x	Rf sputtering	RT/200	4.6	[55]	2011

Copper Oxide (Cu_xO) is a promising semiconductor material for p-type oxide TFTs.

Other semiconductor is the SnO. It was possible to achieve a mobility of 4.6 $cm^2V^{-1}s^{-1}$ (saturation region) which is the highest valued ever achieved in this type of oxide [2].

With aim of presenting a state-of-the-art view of the recent advances in the area of amorphous oxides we collect the most relevant published work and summarize it on Table 2.5.

[4] Post – Post temperature is the Annealing temperature. Annealing temperature is when a metal is heated to a specific elevated temperature, then held the temperature of a period of time, and finally is allowed to cool down by another set of time. In order to annealing to work the cooling temperature must be particular slow, and the times may vary from some hours to days. Annealing temperatures processes are made in the final stage of the TFT fabrication and ensure that the TFT will have toughness, durability, and maintain its properties [52].

Table 2.5 - Resume of recent state of the art on oxide TFTs from year 2015.

Material	Process	Temperature Dep/Post [ºC]	Mobility $[cm^2V^{-1}s^{-1}]$	V_{th} [V]	Reference	Year
a-GIZO	Rf sputtering	RT/300	15.88	4.6	[56]	2015
ZnO	UBMS[a]	RT/300-400-500	4.03	11.5	[57]	2015
a-GIZO	Reactive Sputtering	200/250	19	-3.2	[58]	2015
a-GIZO	Dc sputtering	RT/150-200-250	6-7-7.3	11.3-4.53-4.14	[59]	2015

[a] – Unbalanced magnetron sputtering.

The TFTs used in this dissertation use solution-based ZTO as semiconductor. These TFTs were fabricated on the clean rooms of CENIMAT. So it is appropriate to review the recent work on this matter and in fact much work have been developed in this field by CENIMAT team.

Branquinho et al. have carried out experiments on environmental friendly solution based ZTO TFTs through solution combustion synthesis, where they use Ethanol as solvent. These devices show some good performances, as low threshold voltage (V_{th} = 0.36 V) and a saturation mobility of 0.8 $cm^2V^{-1}s^{-1}$ on low operation voltages. With this work it is demonstrated that Ethanol based TFTs are a good alternative low cost and environmental friendly devices [39].

Kiazadeh et al. work, they show evidences of an intrinsically more stable ZTO TFT by studying the time and temperature dependence of stress and recovery process. They then propose that this stability is stimulated by a defect passivation[5] or neutralization of the SiO_2 surface and therefore leading to a reduction of traps. They also suggest that this passivation is brought out during the fabrication of the ZTO solution [60].

[5] Passivation – The passivation is basically the growth of an oxide layer on top of the semiconductor to produce electrical stability. This happen because the transistor surface is isolated from electrical and chemical conditions introduced by the environment. The advantages of a passivation layer is to diminish the reverse-current leakage, boost breakdown voltage and increase the power dissipation [58].

2.3.6 Applications

Actually the main applications with TFTs are associated with displays, and oxide TFTs are not exception. In CENIMAT, oxide TFTs have been used for PM (passive matrix) and AM (active matrix) backplanes. The PM backplanes were produced using RT sputtered IZO patterned using photolithographic process on glass and using a polymeric substrate [61], [62]. The result is a transparent display with 7 segments integrated with chipLED front-plane technology, that is valuable in the automotive industry as HUD displays (see Figure 2.21).

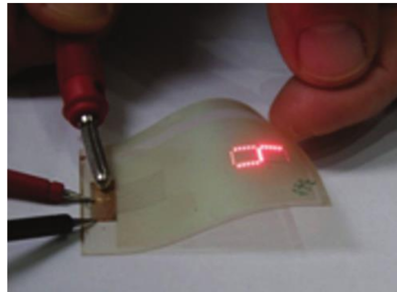

Figure 2.21 - Transparent PM chipLED [2].

The AM backplanes were produced on glass, consisting on a matrix of 128 x 128 pixels (see Figure 2.22a) were which pixel consists in a single TFT (Figure 2.22b). The oxide used as a channel was GIZO and the dielectric was TSiO. After the process of the backplane production, they were successfully integrated with reflective LCDs frontplanes (Figure 2.22c). Even so, small short-circuits were observed through the gate [63].

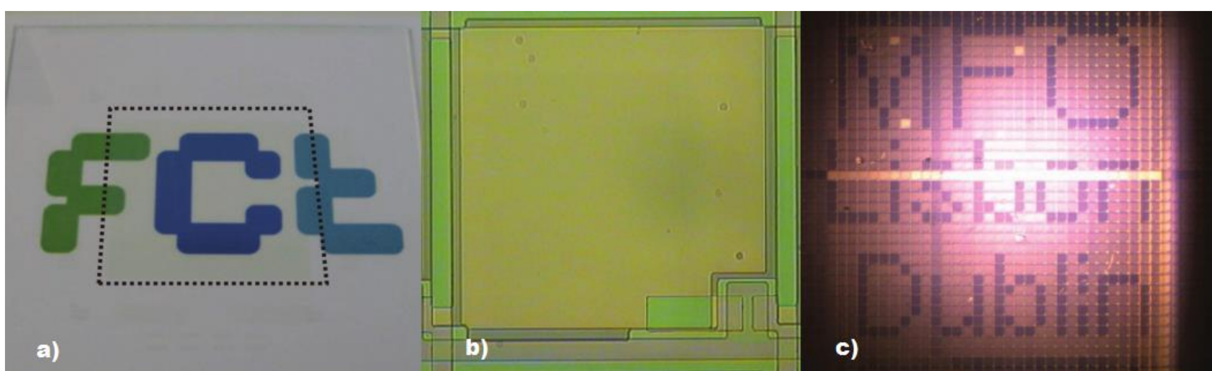

Figure 2.22 - AM Backplane with TFTs based on GIZO as semiconductor: a) AM backplane on glass; b) image of one of pixels (with a dimension of 350 by 350 µm); c) Integration of the AM backplane on an LCD frontplane [63].

Large companies are also investing on oxide TFTs. The aim is to show flexible and transparent displays. Some of this companies are well known like Samsung, that made a OLED display driven by a GIZO TFT, with a transmission higher than 20% [64]. Additionally LG made an OLED display with a 0.1mm thick stainless steel plate, also driven by GIZO TFTs [65]. Also from ZnO TFTs, Park et al. reported a transparent 220 x 176 resolution OLED display supported by a glass substrate [66]. Transparence is not the only goal, high mobility and large area uniformity is also crucial for displays. Samsung demonstrated in 2010 a 70 inches ultra-definition LCD 3DTV [67] with a scanning frequency of 240 Hz.

Figure 2.23 – 70 inches UD LCD 3DTV by Samsung [67].

Samsung also showed a 2.2 inches monochromatic display with a 128 x 160 pixels of resolution. This was fabricated using spin-coated IZO TFTs processed at 350ºC [68]. Other works have followed using spin coated GIZO TFTs, with even larger screen sizes and higher resolution. These were reported by Taiwan TFT LCD Association / Inpria Corp. / Oregon State University.

With this analysis we can see that the tendency shows us that oxide semiconductors will conquer the market step by step in the nearly future.

Displays are the mostly used application in oxide TFTs, but are not the only ones. Ring oscillators (RO) and a whole range of logic circuits have been also reported. These circuits are an important tool to assist materials and devices. For example, the propagation delay of a RO is used as a benchmark of how fast a TFT can operate [69].

In 2008 Sun et al. [70] reported the fastest oxide circuits on glass, ALD (Atomic Layer Deposition) deposited ZnO TFTs with a processing temperature of 200º C. The circuits possess seven-stage RO (Figure 2.24) that operated at 2.3 MHz and a propagation delay of 31 ns/stage.

Figure 2.24 - Seven Stage RO based on ZnO TFT with 31 ns of propagation delay [70].

One other application of using oxides in the semiconductor channel is the oxide CMOS. Mainly because this CMOS technology offers interesting advantages over NMOS technology (previously spoken). The most important are improvements on power dissipation and larger amount of logic functions inside a chip.

Reports on oxide CMOS are recent and the p-type oxide TFTs are still in the beginning of the experiments. This caused that the initial CMOS inverters were based on hybrid solutions containing n-type oxide TFTs and p-type organic TFTs.

Later in 2008 a fully oxide based CMOS inverter was made by Chu et al.[71] combining n-type In_2O_3 and p-type SnO_x, where the layers were produced by reactive evaporation. The results were fairly good for the first time, reaching a peak gain of approximately 11 but operated at very high voltages (approx. 100 V).

More recently a different approach was made on oxide based CMOS technology, leading a new range of applications. Martins et al. preformed a paper-CMOS inverter [72], where the n-type oxide TFT was GIZO and the p-type oxide TFT was non-stoichiometric SnO_x , with an IZO gate (Figure 2.25a). This was also done at RT and layers were deposited by reactive magnetron sputtering. Additionally, the paper acted as substrate and dielectric. The results were quite good, showing electron mobilities greater than 21 $cm^2v^{-1}s^{-1}$ and hole motilities greater than 1 $cm^2v^{-1}s^{-1}$. The peak gain was 4.2 and the operation voltages are around 16 V as seen in Figure 2.25b. The result obtained was actually a good value to look into the future of paper electronics.

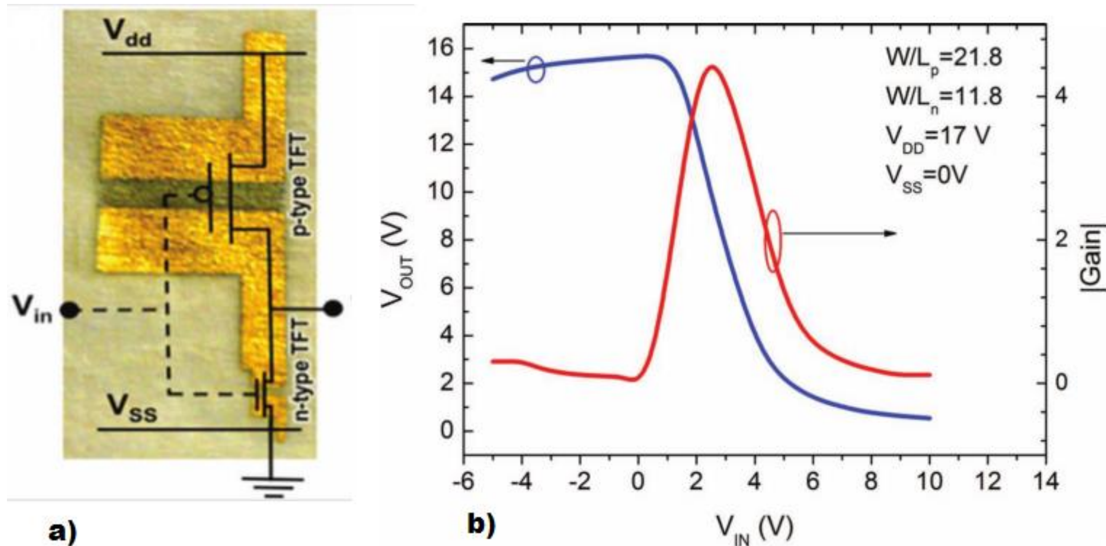

Figure 2.25 - a) Picture of the oxide paper-CMOS; b) Transfer characteristics of the oxide paper-CMOS and gain [2].

It is also important to say that this experiment showed high leakage current, which by the authors is normal giving the change from a rigid substrate to paper.

After this experiments it is right to say that paper circuits have a bright future in electronics. They open an opportunity for lightweight, low power consumption, low cost, fully recyclable and heavily packed integrated circuits. The applications of this type in the future undergo by smart labels, sensors, tags, memories, integrated systems, etc.

From all of these, it is certain that the oxide semiconductor technology is here to stay. Right now it may not replace the conventional silicon technology in some applications but has the capability to open new areas of application. Due to its characteristics, we can resume the greatest advantages of oxide semiconductors as low cost fabrication process in RT, high electron mobility, and huge compatibility with flexible and transparent applications [2].

CHAPTER 3 - Experimental methods

Summary

This chapter describes how the devices are mounted and connected during the electrical characterization process. It also presents basic information about the specifications of each individual instrument and how the electrical measurements are carried-out.

3.1 Introduction

As discussed before, a transistor is a 3-terminal device, constituted by the source, drain and gate. To fully characterize it, is necessary to use several voltage sources and current measuring instruments (picoammeters). Voltage sources to apply voltage between the source and drain terminus and in the gate. Picoammeters measure current at one terminal of the TFT (for example the drain). Ideally all the three currents entering the three terminals should be measured. Therefore fully systems should have up to three amperimeters and two voltage sources. The schematic diagram presented in Figure 3.1 shows the transistor and how the current and voltages are measured.

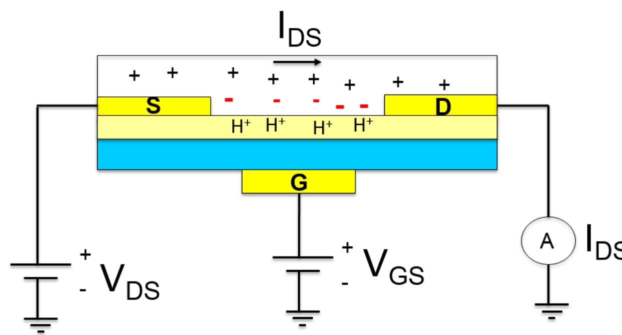

Figure 3.1 - Schematic diagram showing how the voltages and current sources are connected to the transistor.

The electrical characterization of the TFTs was carried out using an experimental set-up that makes use of several instruments. Namely picoammeters, voltage sources, a temperature controller, microprobes, vacuum pumps, optical systems and a cryostat.

The currents on the TFTs are typically below the micro-ampere (μA), this requires the use of ultra-sensitive instrument such as picoammeters.

When the TFT was mounted inside the Cryostat the connections to the TFTs were made using gold wires (with 25 μm in diameter). These wires were glued to the source and drain terminals using conductive silver paint, as can be observed in the schematic in Figure 3.2.

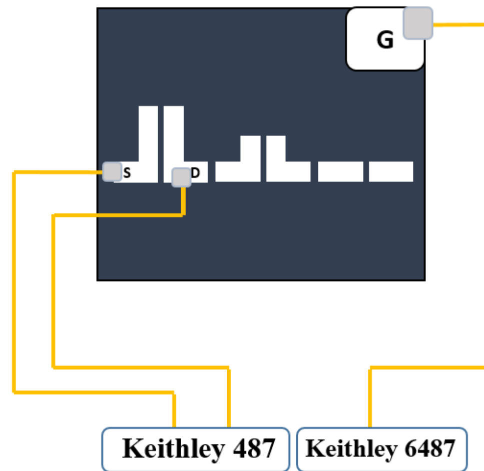

Figure 3.2 - Electrical connections made using gold wires glued with conductive silver paint.

The cryostat was only used for measurements as function of temperature. For room temperature measurements, a vacuum chamber and microprobes were used.

All the instrumentation (picoammeters, voltage sources, the temperature controller and the monochromator) was connected to a computer running DOS as operative system. This computer controls the instruments through GPIB and RS232 interfaces.

All the recorded data is saved in *.m* scripts for posterior analysis and processing in the Matlab® application.

3.2 Description of equipment operated

Keithley 487:

This is the picoammeter/voltage source supply. This 487 model is optimized to make measurements of a very low current and very high resistance. It possess the ability to measure current from a range of 10 fA to 2 mA. Also it include two voltage sources: one with 500 V range with 11 mV of resolution and another source with a 50 V range and 1mV of resolution. In terms of reading intervals, the 487 can be programmed from 10 ms to 1000 s. Also the device have a buffer which can store up to 512 readings to a faster data acquisition [73].

Figure 3.3 - Front view of Keithley 487 picoammeter/voltage source [74].

This Keithley 487 (Figure 3.3) was used as a current meter on the drain of the transistor, and its voltage source was used at the source terminal of the transistor.

Keithley 6487:

It is also a picoammeter / voltage source. This model is very similar with Keithley 487 as it can measure currents in the range of 20 fA to 20 mA, make measurements up to 1000 readings/s, and output source voltage in the range of 200 μV to 505 V. In general it is an upgradable device of its previous versions as it can give high accuracy and faster rise times [75].

Figure 3.4 - Front view of Keithley 6487 picoammeter / voltage source [76].

This Keithley 6487 (Figure 3.4) was used as voltage provider to the gate of the transistor.

The two vacuum pumps used are shown in Figure 3.5. One is a rotary pump than makes the primary vacuum. The other is a turbo-molecular pump. When connected in series both pumps can evacuate the cryostat to a pressure of 10^{-6} Torr. This vacuum is important to prevent

water condensation inside the cryostat when the TFT is cooled down to very low temperatures (140 K).

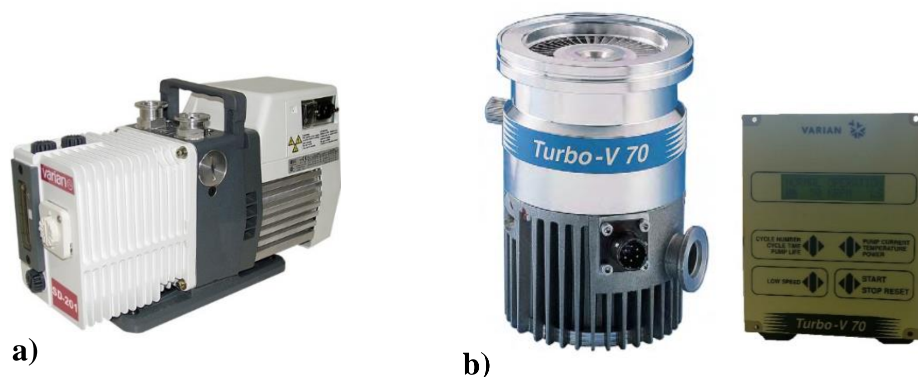

Figure 3.5 – a) Photograph of the rotary pump [77]; b) turbo-molecular pump (Varian Turbo-V70) and its controller [78].

The Triax 320 monochromator is shown in Figure 3.6a). The light source is a 450 W Xenon Lamp can be observed in Figure 3.6b).

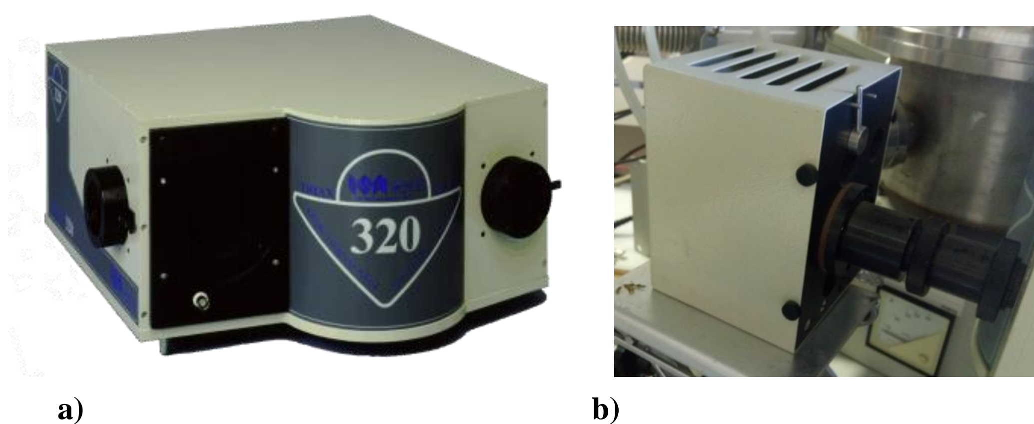

Figure 3.6- a) Triax 320 spectrograph [79]; b) 450 W Xenon Lamp.

The temperature was measured using the Oxford Intelligent Temperature Controller (ITC). This instrument is also capable to generate well-defined heating ramps. It uses as a temperature sensor a PT 100 (platinum sensor). This temperature controller is shown on Figure 3.7

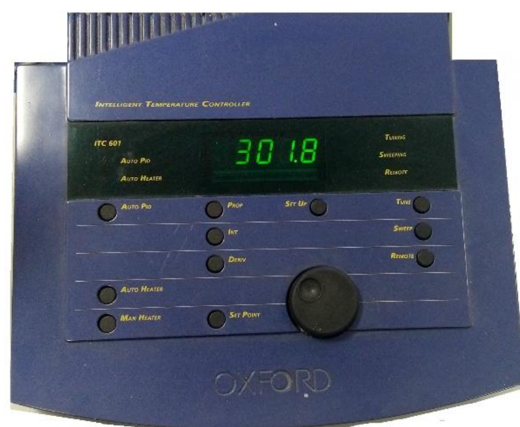

Figure 3.7 - Oxford ITC showing room temperature (RT).

The Cryostat (shown in Figure 3.8) has a cold finger inside connected to a reservoir that can be filled with liquid nitrogen. The temperature can be varied between 140 K and 360 K. The cryostat is also equipped with a sapphire window for optical experiments.

Figure 3.8 - Cryostat where the temperature dependent experiments were made.

Electrical microprobes (Figure 3.9a) were just sharp needles and were placed precisely above source, drain and gate terminals (that is why the probes were so tiny). They were placed inside the vacuum chamber (Figure 3.9b) to ensure a complete vacuum and dark environment at RT. Furthermore it would guarantee also that atmospheric agents (water, oxygen, etc.) are kept away from the TFT surface, since the TFT was not encapsulated. Also these little microprobes were attached to a micro-positioner that allowed a rapid connection of the measuring system to the devices.

These little probes were fixed by a magnetic weights to prevent the sample to move during the experiments specially during vacuum pumping.

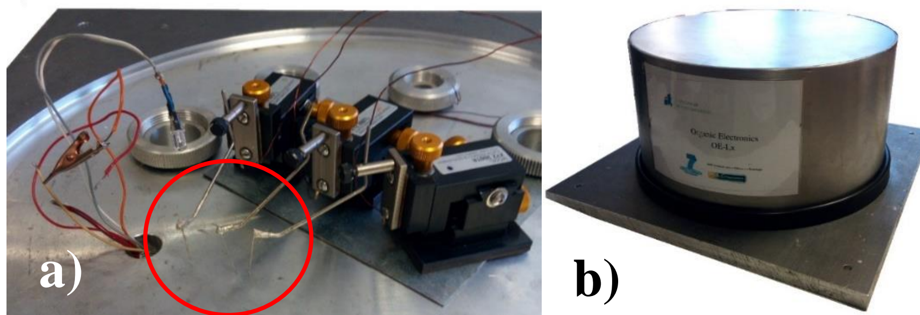

Figure 3.9 – a) Microprobes used to measure the TFTs; and b) the vacuum chamber that holds the TFTs inside a vacuum and dark environment.

CHAPTER 4 - Light-induced effects on ZTO based TFTs

Summary

Light-induced effects on the TFTs based on ZTO as semiconductor are presented and discussed in this chapter. A number of experiments aimed to gain insight into the physical nature of the electronic states induced by light were carried out. These include temperature dependent experiments and thermal stimulated currents.

4.1 Introduction

Light-induced effects on TFTs based on soluble oxides are still poorly understood. To the best of our knowledge there are only a few studies about photo-induced effects on TFTs based on soluble oxides such as the ZTO. However, there are number of studies on TFTs produced by sputtering. Several models have been proposed to explain light-induced effects. It has been claimed that the photo generated holes get trapped in the dielectric/channel interface or in the dielectric bulk layer [80], [81]. Alternatively it has also been proposed that light generates ionized oxygen vacancies [82] and/or photodesorption of absorbed oxygen ions (on AT-ZIO) [83], [2].

Recently in 2013 Park et al. [84] studied the effect of light exposure on a-GIZO TFTs under both positive bias stress (PBS) and negative gate-bias stress (NBS). They concluded the ΔV_{th} was caused by trapping carriers and also photodesorption of oxygen ions. In 2014, Liu et al. [85] investigated the role of oxygen vacancies on the bias illumination stress stability of solution processed ZTO TFTs. Their work showed that the ΔV_{th} is positive when the TFTs are under PBS and slightly negative under simultaneous illumination and gate-bias stress or negative gate-bias stress (NBIS). It also showed that the ΔV_{th} under NBIS is significantly large. Light can recover the ΔV_{th} induced by PBS. Liu et al. attributed these results to the photo-ionization and the transition of states of oxygen vacancies in ZTO. They also concluded that in their ZTO based TFTs there are 13.5% of oxygen vacancies. Furthermore the presence of these ionized vacancies does not degrade the field-effect mobility. Light photo-ionizes neutral oxygen vacancies creating positively charged states. These ionized states create an electrostatic field that interacts with the external applied bias and compensate for the ΔV_{th}. Accordingly to these authors the presence of oxygen vacancies in the channel layer may improve the TFT performance if the vacancy density is well controlled during the deposition stage.

In 2013, Ha et al. [86] reported a solution-processed TFT with ZTO as semiconductor and Zirconium dioxide (ZrO_2) as dielectric. The reported value for the μ_{FET} is 10 $cm^2\ V^{-1}s^{-1}$ and a low V_{th} of only 0.1 V. They also reported that the TFTs are not strongly affected by light and stress. Only a small hysteresis window is observed. Here they did not observe the usual ΔV_{th} shifts and sub-threshold swing degradation on ZTO devices after the NBIS. This stability was attributed to the ZrO_2 dielectric, which has been reported in the past for reducing the oxygen vacancies and lowering the off-current. A very important aspect referred in this work

was that the clean interface between ZTO and the ZrO_2 dielectric was crucial to achieve this high stability.

Also in 2013, Kim et al. [87] showed that increasing the annealing temperature, the density and the purity of the solution processed ZTO channel will increase too and with that oxygen vacancies defect diminished. Also the instability of the V_{th} values on NBS and NBIS was restrained with the increase of the annealing temperature. To analyze the charge trapping, the dynamics of V_{th} shifts with NBS and NBIS were analyzed. The results were that the negative V_{th} shift was accelerated under NBIS conditions when comparing with NBS. This resulted on higher dispersion parameter and shorter relaxation time regarding NBIS degradation. Finally Kim et al. [87] conclude that relaxation time to NBS and NBIS instability gets higher (more stable) the higher is the annealing temperature.

4.2 Experimental

The experiments reported here where carried out in two ZTO transistors prepared from solution (urea based process). Both TFTs use SiO_2 as a dielectric layer. The TFTs only differ on the geometrical dimensions. The first one has a W = 2400 µm and L = 40 µm (Transistor A - s10t33) and the second was made on a transistor with dimensions of W=1400 µm and L=100 µm (Transistor B - s10t22). Both transistors were fabricated on the same silicon wafer.

To the production of the semiconductor it was prepared 2 precursors solutions. In both of the precursors solutions, the metallic precursors were $Z_n(NO_3)_2.6H_2O$ (Zinc nitrate hexahydrate) and S_nCl_2 (Tin(II) chloride) dissolved in 2-methoxyethanol. Not adding anymore compost to the solution, the TFT stays with normal ZTO as semiconductor. Processed by sol-gel spin-coating method already talked in the last chapter. To accomplish the ZTO + urea, it must be added urea (that is used as a fuel) and NH_4NO_3 (Ammonium nitrate) to the previous talked solution. Processed using Auto-combustion.

These TFTs were deposited in staggered bottom-gate configuration. The source and drain contacts were made from aluminium and were deposited via thermal evaporation. The gate contact is made of doped silicon and the first wafer layer is Si/SiO_2. Both TFTs were produced at CENIMAT clean room located on the New-University of Lisbon.

An actual photo and a schematic of the transistor will be presented in the next figures, showing the main differences between these.

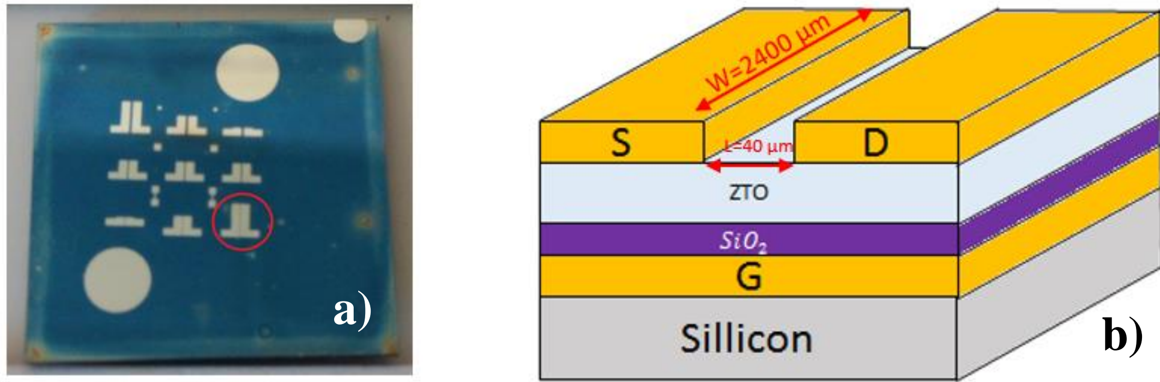

Figure 4.1 – a) Photograph of the wafer with several TFTs and b) schematic representation showing the device geometry of Transistor A - s10t33 with dimensions of W = 2400 µm and L = 40 µm.

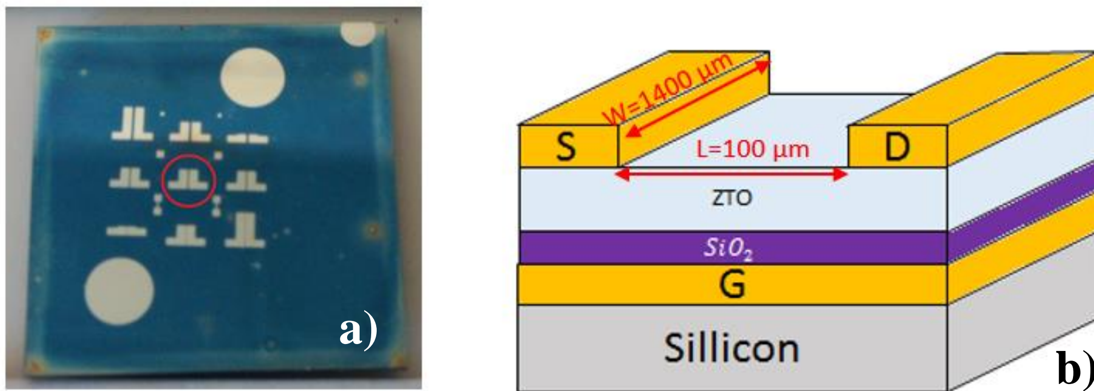

Figure 4.2 – a) Photograph of the wafer with several TFTs and b) schematic representation showing the device geometry of Transistor B - s10t22 with dimensions of W=1400 µm and L=100 µm.

The TFT label **A** was measured in a vacuum chamber but without the possibility of performing temperature dependent experiments. The TFT label **B** was mounted in a cryostat. Temperature dependent experiments were carried out in the temperature range 140 K-360 K. Liquid nitrogen was used to cool-down the sample. The illumination was also performed differently in both TFTs, while for the TFT in the vacuum chamber a blue LED was used, the TFT mounted in the cryostat was illuminated using a xenon lamp and a monochromator (Triax 320). All the Electrical measurements were carried out using two picoammeter/voltage sources Keithley 487 (Figure 3.3) one to supply the drain-source voltage and also to measure the drain-source current. A second Keithley 6487 (Figure 3.4) was used to provide the gate voltage. Both experimental set-ups are almost identical. The differences are on the light excitation sources

used and on the existence of a temperature controller (Oxford ITC) to monitor the temperature. The cryostat was pumped by a two-state pump system (rotary + turbo molecular pump). The chamber was only evacuated using a rotary pump. Figure 4.3a) and Figure 4.3b) shows a schematic representation of the experimental set-up used in both experiments.

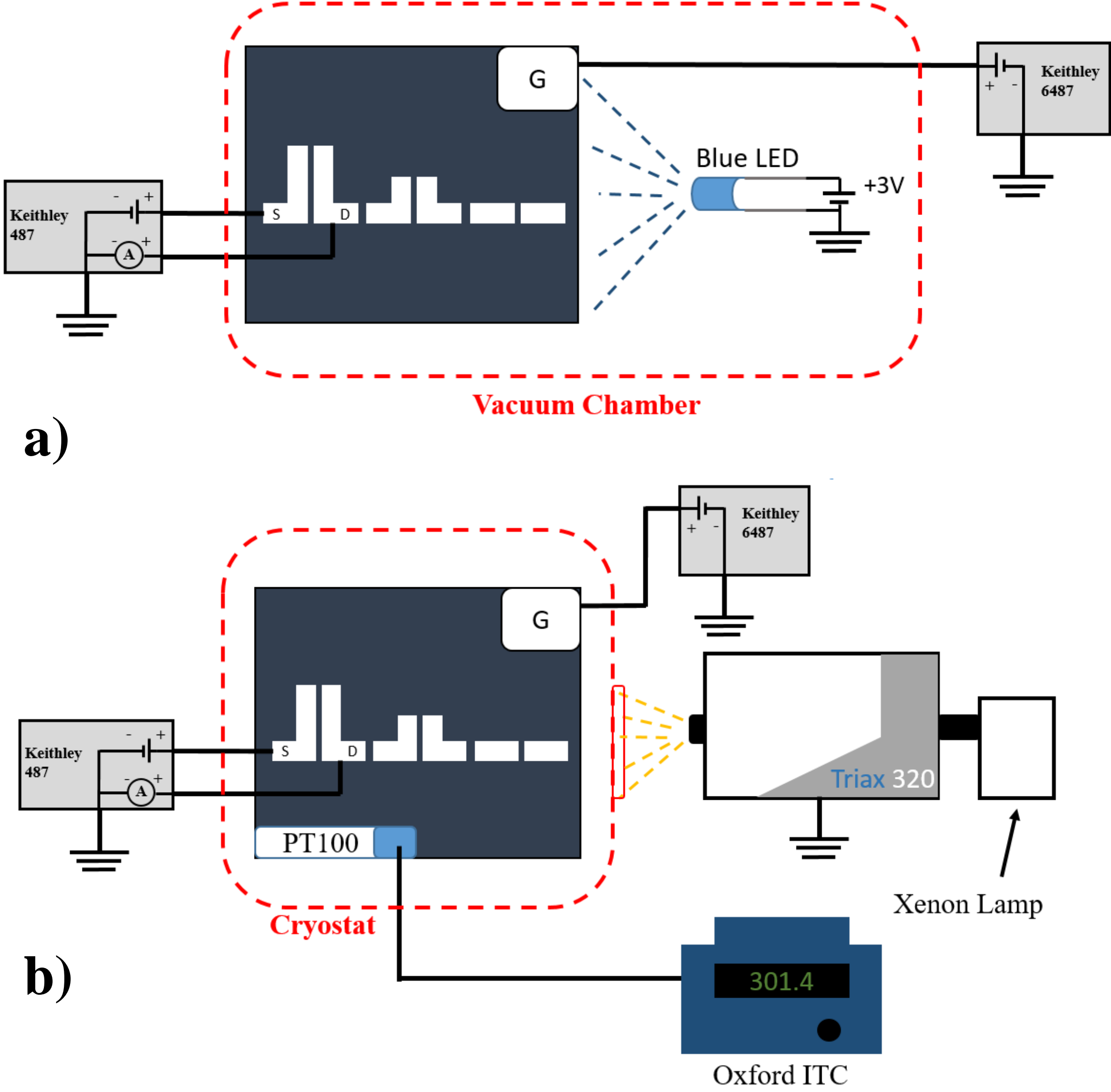

Figure 4.3 - Experimental set-up used to characterize the TFTs. a) Configuration used to measure the Transistor A - s10t33; b) Configuration used to measure Transistor B - s10t22.

Also a blue LED ($350 \leq \lambda \leq 650$ nm, $\lambda_{max} = 480$ nm), where its emission spectrum can be seen in Figure 4.4, is also used as optical excitation source during the experiment on TFT **A**. The light intensity was not calibrated but it was kept constant through the measurements.

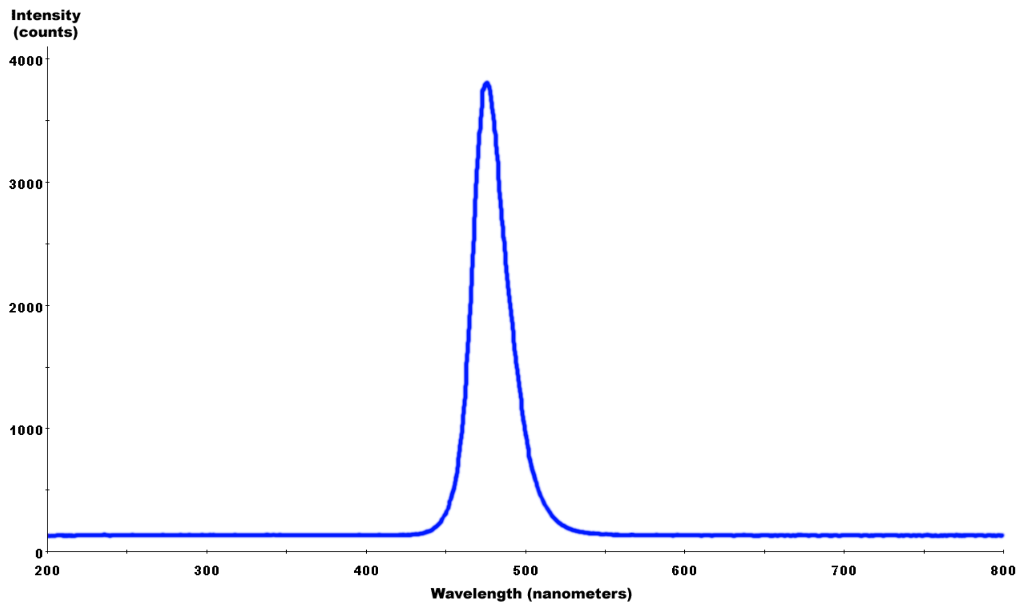

Figure 4.4 – Blue LED light intensity spectrum as function of the wavelength [88].

The device was electrical characterized before and after any temperature dependent experiment. This allow us to know exactly the conduction state of the TFT at the beginning and at the end of a temperature scan.

Thermal stimulated currents (TSCs) we conducted were made using the TFT wired as shown in Figure 4.5. Basically the TFT was connected as a capacitor. The drain and the source terminals are short-circuit and used as a single terminal. The current meter is connected between the short circuited drain and source terminals and the gate terminal. The aim of this connection is to measure charges released from the dielectric/semiconductor interface as the temperature rises [40].

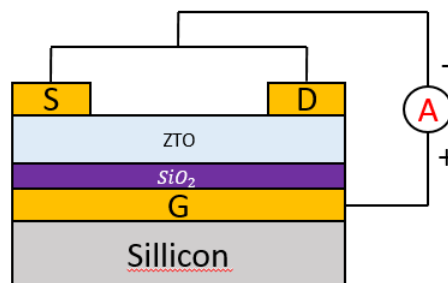

Figure 4.5 - Simple schematic of transistor configured as capacitor.

The photo-response of TFT as function of the wavelength is shown in Figure 4.6. In the wavelength range of 450-550 nm the photo-generated current is low and relatively flat with wavelength. In the infrared region (λ>560 nm), the current rises because of the heat generated by the infrared light.

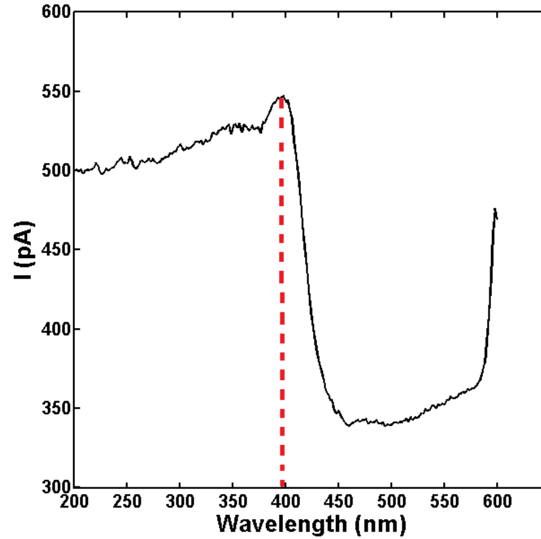

Figure 4.6 - Photo-generated current on a ZTO TFT as function of the light wavelength.

The photo-generated current rises as the energy of the light increases and for wavelength above 400 nm reaches a plateau. The maximum value is at 400 nm, where its corresponding energy is calculated with the Equation 3 below.

$$E_{eV} = \frac{\frac{h * c}{\lambda}}{e} \quad \text{Equation 3}$$

Where h is the Planck's constant ($6.626 * 10^{-34}\, Js$), c is the speed of light ($3.0 * 10^{8}\, m/s$), λ is the wavelength of the light ($400 * 10^{-9}\, m$) and e is the electron charge ($1.60217662 * 10^{-9}\, C$). So this equation tells us that the energy at 400 nm is approximately $3.10\, eV$. Which is in line with value around 3.7-3.9 eV [85],[89] reported in the literature for the band-gap of ZTO. So when a monochromator was used we exited the TFT with this light wavelength of 400 nm.

4.3 Results and discussion

Although, both TFTs, **A** and **B** should behave identically, the data analysis shows that this is not the case. Because of the differences in the electrical properties, the results are organized and presented according to the type of TFT being measured. This discussion starts with the analysis of electrical properties of TFT **A**.

4.3.1 Results and discussion of experiments in Transistor A - s10t33

The current-voltage (*I*-*V*) characteristics curves for the TFT **A** are shown in Figure 4.7. The device show no signs of I_{off} current or contact problems, it also seems to modulate and saturate well for higher values of V_g. The transistor is a normally-on device because there is a current passing through the TFT when V_g= 0 V. A $V_g = -1.5$ V is required to close-down the TFT channel as shown in Figure 4.8. Therefore, the TFT can work in depletion as well as in accumulation. However, for V_g > 5 V, the ability to open the TFT channel is substantially reduced. This lack of modulation is also clearly visible on the TFT transfer curves shown in Figure 4.8. The transfer curve slope starts to decrease for voltages above 1.5 V. This effect is caused by gate-bias stress effects. The V_{th} increases after prolonged application of a gate-voltage, the overall effect is a decrease in the TFT current with time for the same gate voltage.

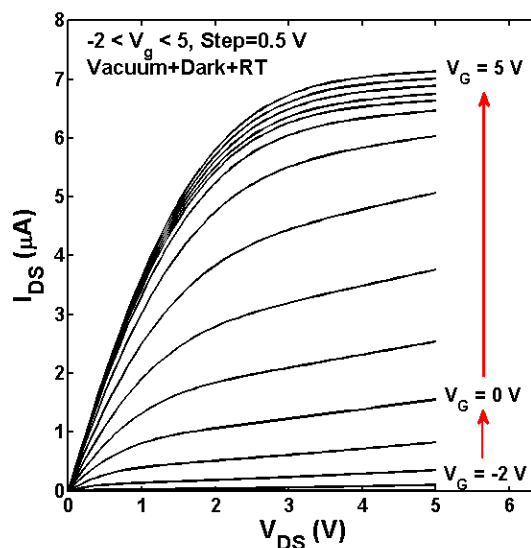

Figure 4.7 - Current-voltage (*I*-*V*) characteristics of the TFT **A** - s10t33.

The transfer function in the linear region (V_{DS}=0.25 V) was measured before and after a light exposure for a period of 100 seconds. Both transfer curves are shown in Figure 4.8

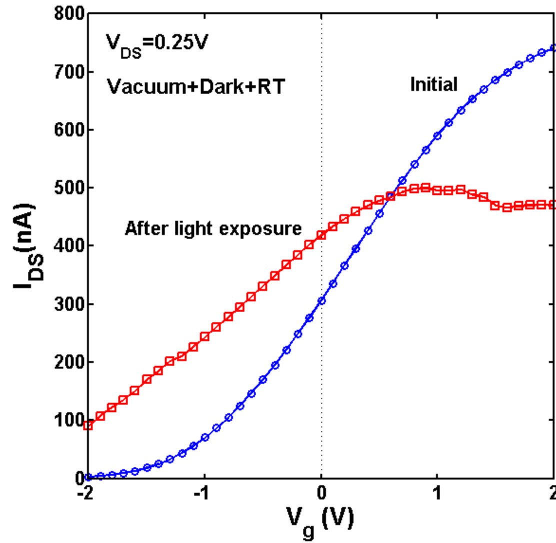

Figure 4.8 - The effect of 100 s long pulse of blue LED light on the linear transfer curves.

The light exposure causes two effects: i) The I_{Off} current increases; and ii) the slope of the transfer curves decreases suggesting that upon light exposure the field effect mobility decreases. The behavior upon gate-bias stress is also different, the TFT is highly susceptible to gate-bias stress if has been previous exposed to light. When kept under dark the threshold voltages variation are significant less. In overall aspect, the light also causes a negative-bias threshold voltage shift as reported in the literature and presented in the introduction. The phenomena is known as negative bias-illumination stress (NBIS).

The light-induced effects produced are long-lived and they remain for several hours or even days. This rules out the possibility of having a physical origin in thermal effects caused by infra-red radiation.

The kinetics of the light induced changes was also monitored. Figure 4.9 shows that the increase in the off-current (Vg = 0 V and V_{DS} = 0 V) during the light exposure is approximately linear with time.

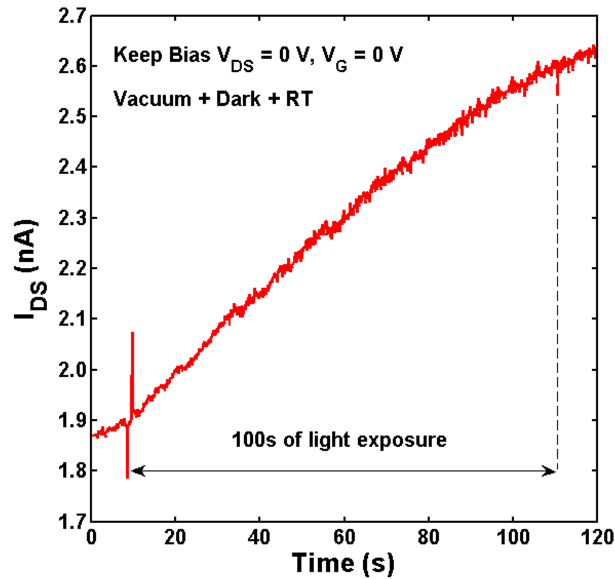

Figure 4.9 - Effect of the blue LED light on TFT off-current ($V_g = 0\ V, V_{DS} = 0V$).

When left in the dark and with time the TFT will recover their original behavior. The light induced effects are fully reversible. However, the recovering kinetics is quite complex. Figure 4.10a) shows a series of transfer curves recorded in a sequential manner after the TFT was exposed to 100 s long pulse of light. The first transfer curves shows that the threshold voltage hardly moves with time. However, the on-current decreases rapidly with time. In the 4th and 5th curve the TFT bounces back and the threshold voltage increases towards negative bias. This behavior is unusual. Furthermore, was not reproducible. Because of this lack of reproducibility, we do not propose an explanation since it may be an artifact.

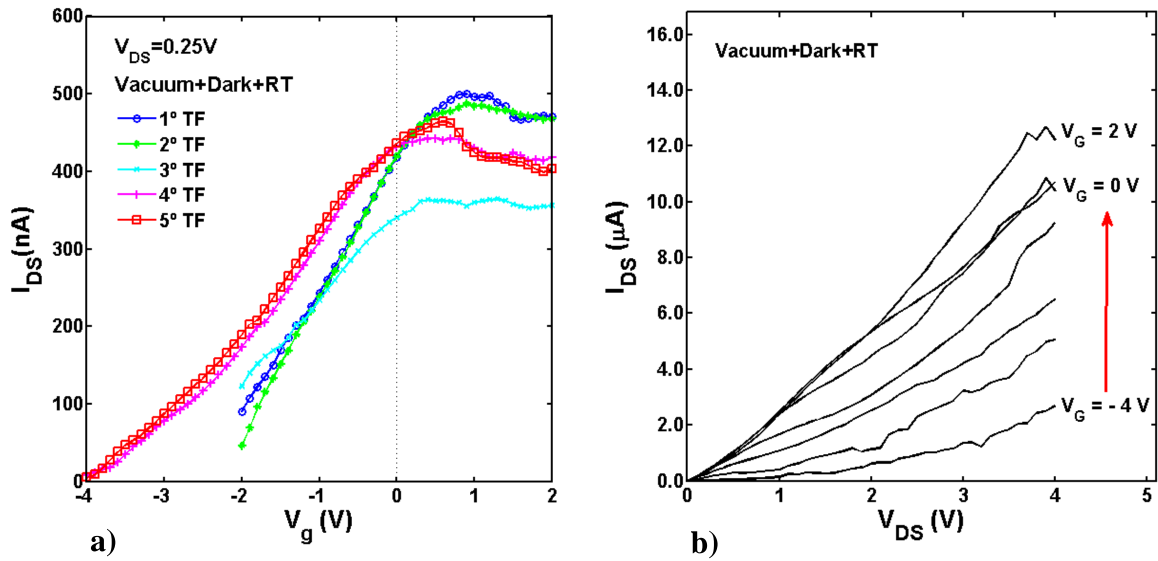

Figure 4.10 – a) Consecutive Transfer functions recorded after 100s of light exposure; b) *I-V* characteristics after light exposure.

I-V curves recorded after light exposure are shown in Fig. 4.10b). These are consistent with the transfer curves on Figure 4.10a). The current is gate-bias independent when the TFT operates under accumulation. Channel modulation is only observed when the TFT operates in depletion. Furthermore, *I-V* characteristics also do not reach saturation. This is because the current is very high (reaching 14 µA) while before being illuminated the maximum current for V_g= 5 V only reaches 7 µA (Figure 4.7).

The light induced effects did not caused permanent changes on the TFT characteristics. Figure 4.11 compares the transfer curves before illumination, immediately after illumination and 19 hours after illumination. After 19 hours of resting in the dark, the TFT recovers the original V_{th}. However, the TFT on-current remains below the original one.

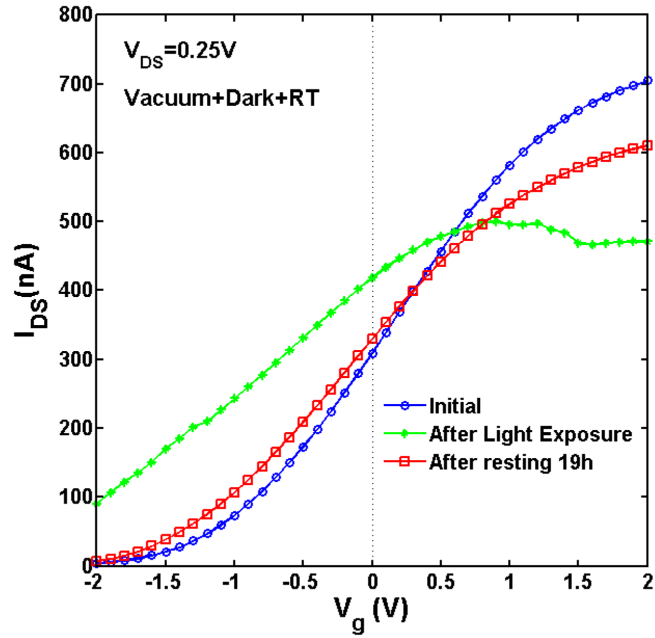

Figure 4.11 - TFT transfer functions before, immediately after light exposure and after 19 hours of resting under vacuum and dark conditions.

4.3.2 Results and discussion of experiments in Transistor B - s10t22

In a similar fashion as for the transistor **A**, TFT **B** was characterized before and after it was submitted to illumination. The linear transfer curves and the *I-V* curves are shown in Figure 4.12. The transfer curve is not linear which shows the TFT has a number of electrical active defects that charge under the applied bias. However, the slope keeps increasing with the gate–bias. This denotes that the gate-bias stress effects are not so pronounced in this transistor as in the TFT **A**.

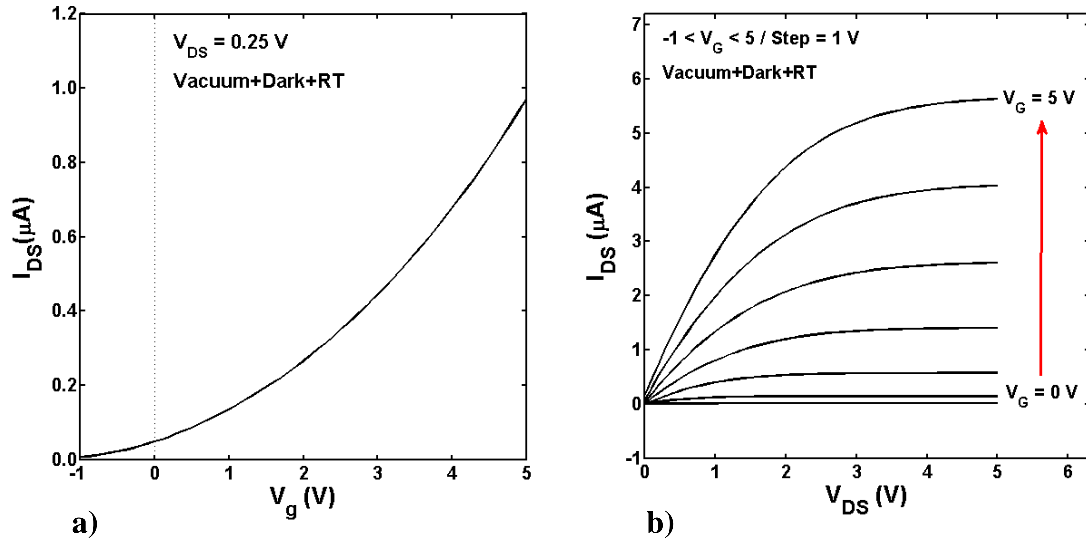

Figure 4.12 – The electrical properties of the TFT **B**. a) Transfer curve in the linear region with V_{DS} = 0.25 V and b) the corresponding *I-V* characteristics.

Light exposure effects are best represented by plotting the linear transfer curves before and after illumination. These are shown in Figure 4.13a). Upon light exposure the TFT current is significant enhanced. Since the transfer curves were recorded in the linear regions one expects they should be linear with voltage. The fact the transfer curves are curved over the entire voltage range makes difficult to extract quantitative information. Namely, it is difficult to estimate if there is a change in field-effect mobility and what are the real changes in the threshold voltage. In order to extract quantitative information we first have to linearize the curves. This is done in Figure 4.13b). To linearize the curves we use the γ parameter as described in Chapter 2. The curves in Figure 4.13a) were linearized using γ=1. The I_{DS} is then plotted as $I_{DS}^{1/2}$ vs V as shown Figure 4.13b). After this linearization process, both transfer curves follow a straight line.

The light increases the current but also changes the field-effect mobility and moves the threshold voltage towards more negative voltages from V_{th}= -1 V to a V_{th} = -4 V. In overall terms there is a change in the charge transport mechanisms. This effect can only be explained if light creates dopant states.

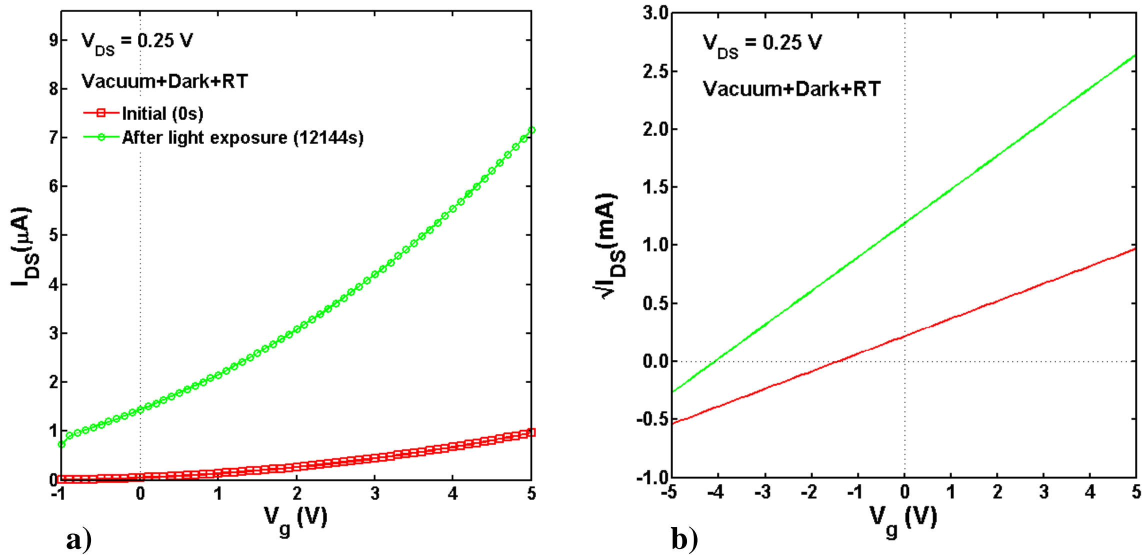

Figure 4.13 – Comparison of the transfer curves before and after light exposure. a) Transfer curves before and after light exposure; b) V_Ts before and after light exposure, after linearization using a γ=1.

To gain insight into the long-lived electronic states induced by illumination, TSC experiments were performed as described in the experimental section. States are filled with light at room temperature, then the illumination was switched-off and the TFT is connected as a capacitor as described in Figure 4.5. The current between the gate terminal and the short-circuited drain and source terminals was measured. The short-circuit current was measured as the TFT was warm-up from 300 K to 360 K with a well-defined heating ramp of approximately 1 K/min. TSC curves were also measured without having submitted the TFT to illumination.

Figure 4.14 compares a TSC curve measured without previous illumination with a TSC curve recorded after the transistor was illuminated. When the TFT is not illuminated the TSC current is almost flat with temperature and very low. The average value is approximately 20 pA. The physical origin of this current may be related with leakage through the gate-dielectric. The behavior of the TSC curves is substantially different if the transistor was exposed to light. In this case the TSC curve reaches a plateau between 320 K and 330 K. For temperatures above 330 K the current starts to decrease. It is also interesting to note that there is a clear change in the noise of the current. Initially, the noise is high and for temperatures above 330 K the noise clear diminishes. This behavior suggests that as the charge carriers are released they generate a significant amount of electrical noise.

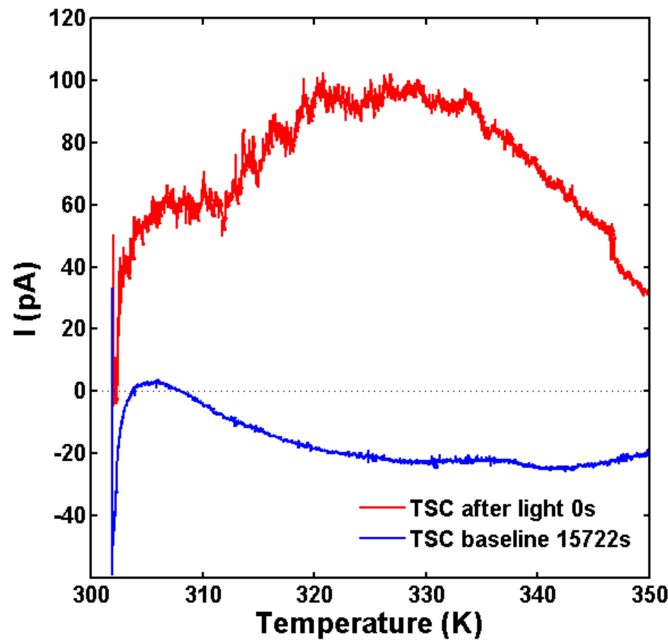

Figure 4.14 - Comparison of TSCs taken upon light exposure and baseline (dark conditions).

In order to full characterize the light-induced changes, TFT transfer curves were also recorded before and after the TSC experiments were performed. This comparison is shown in Figure 4.15. Figure 4.15a) shows the as-recorded curves, and Figure 4.15b) are the same curves but now linearized using γ =1 (as described above).

Two independent TSC were carried out one after the other in a sequential manner. This procedure was carried out because the original properties were note totally restored after the first TSC was made. Indeed, after the first TSC curve a significant reduction both in current as well as in the mobility was observed (see Figure 4.15a). However, it is puzzling that the threshold voltage remained unchanged at V_{th}= -4.1 V. A second TSC carried out immediately after the first, causes only additional small change in the transfer curves. This suggests that the TSC releases the charges responsible for the transistor on-current but not the charges which cause the threshold-voltage shift. In other words the TSC experiment removed localized states form the bulk semiconductor but it did not remove states from the dielectric layer (trap states).

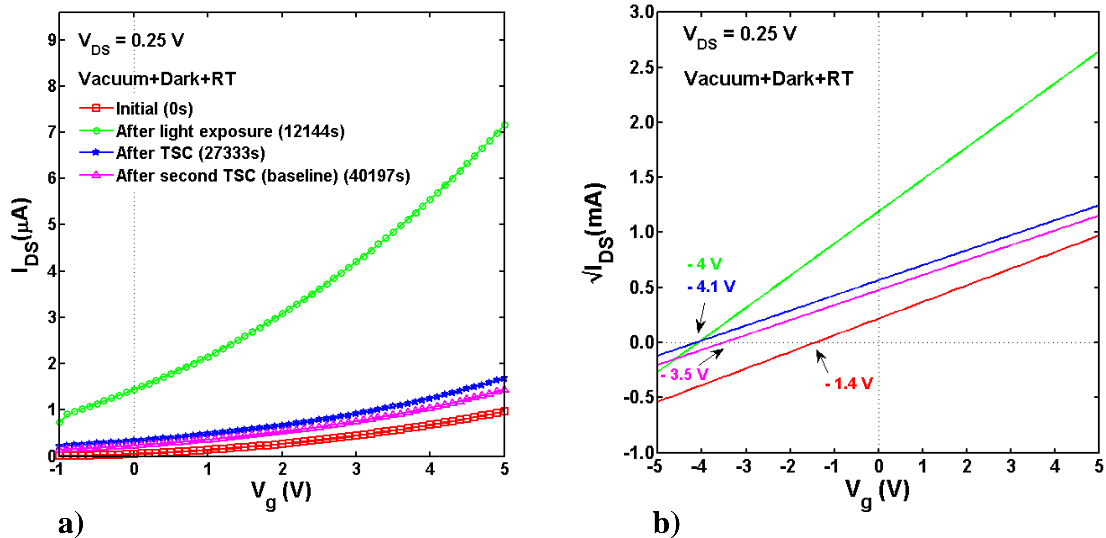

Figure 4.15 Transfer curves measure before and after TSC experiments. a) Linear transfer curves as-recorded; b) Linear transfer curves linearized using γ =1.

Further insight into the light-induced states can be obtained by studying how illumination affects temperature dependence of the TFT current. These studies were performed as follows; the TFT current was studied for the two programmed conductance states. The low conductance state is obtained when the TFT is kept under dark conditions for a few days and the high conductance state is programmed by exposing the TFT to illumination for several minutes at room temperature. The temperature dependence of the current was recorded for both conductance states. The two curves are shown in Figure 4.16a).

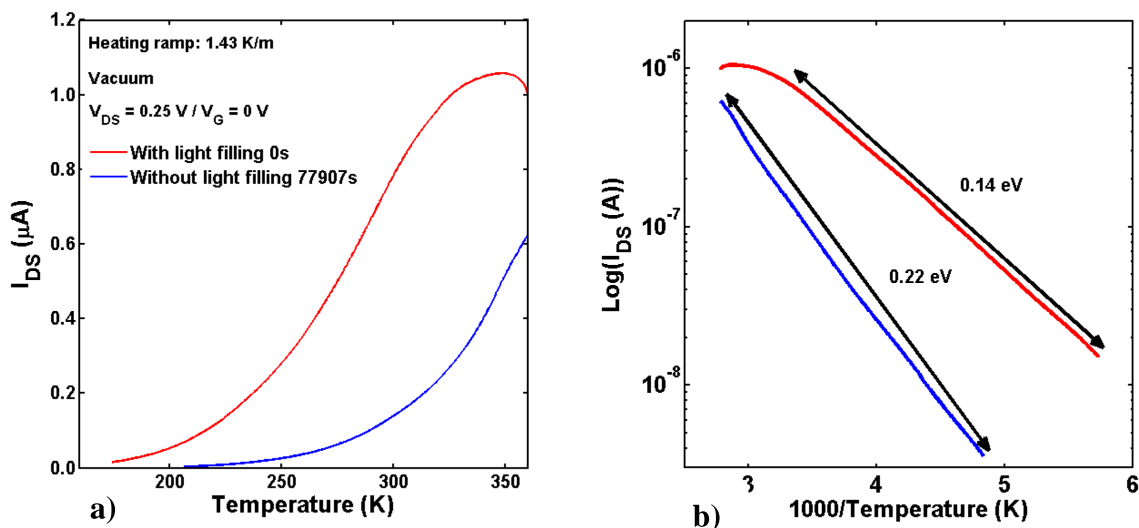

Figure 4.16 – a) Temperature dependent current before and after light filling; b) Both curves are plotted as an Arrhenius graph.

The results on the activation energy, shown on Figure 4.16b), are in line with other reports. Similar values of activation energy on oxide semiconductors have been achieved by other scientists. The values range between 0.22 to 0.8 eV of activation energy [60], [90]–[92].

The exposure to illumination decreases the activation energy from 0.22 eV to 0.14 eV. This suggest that shallow dopant states are induced by light. These shallow states are now responsible for the charge transport mechanism. The position of both dopant states in the ZTO band gap is show in Figure 4.17.

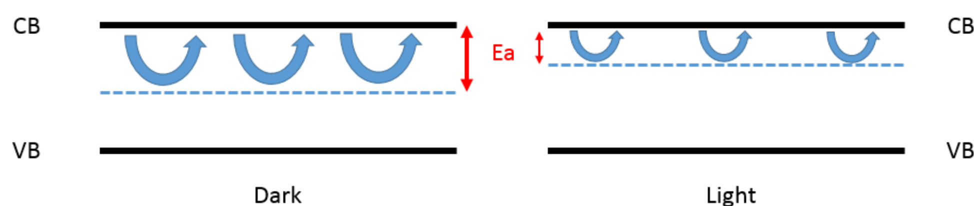

Figure 4.17 - Activation energy and conduction bands in a light and dark situation.

The analysis of the temperature depended of the current shows some interesting aspects. If the TFT is not exposed to light the temperature dependence of the current follows a perfect straight line (Arrhenius plot) with an activation energy of 0.22 eV. However, if the TFT was previously exposed to light not only the activation energy is reduced to 0.14 eV, but the temperature dependence also shows some anomalous behavior. When the temperature reaches approximately 300 K, the current starts to increase less rapidly and deviates from the perfect Arrhenius straight-line plot (see Figure 4.16b). At 340 K the current stops to increase and reach a plateau at 340K. For higher temperatures the current begins to decreases. This behavior can only be explained if the light-induced states are becoming depleted. Eventually, when all the light-induced states are neutralized, the anomalous behavior should disappear and the current should recover its normal thermal activated behavior.

Assuming that the decrease in current with temperature is caused by a neutralization of the light-induced dopant species. This neutralization is a thermal activated process, this is why it becomes visible for temperatures above 300 K. Therefore, the real shape of the temperature dependence of the current must be strongly dependent of the heating ramp. A fast heating ramp will not allow enough time to neutralize all the species and the plateau should move to higher temperatures.

To gain insight into the neutralization process of the light-induced states. The following experiment was carried out. The TFT was exposed to light at a particular temperature. Then the light was turn-off and the current decay in the dark was monitored as function of the time. Two typical current decays are shown in Figure 4.18. The Higher the temperature the faster the current decay. The decay is approximately a single exponential.

The time constant decay to the temperature of 303 K and 348 K are respectively 3.5 hours and 1 hour.

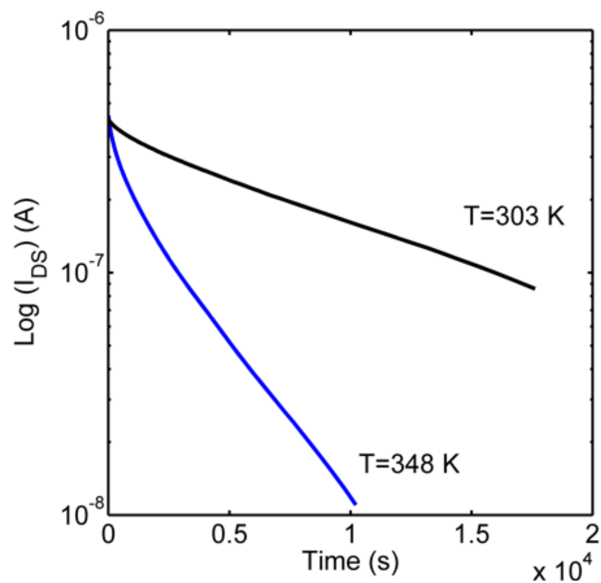

Figure 4.18 - Current decays of the light-induced states. The TFT was previously exposed to light and then kept in the dark while the time dependence of the current is monitored.

Anomalous behavior caused by water contamination.

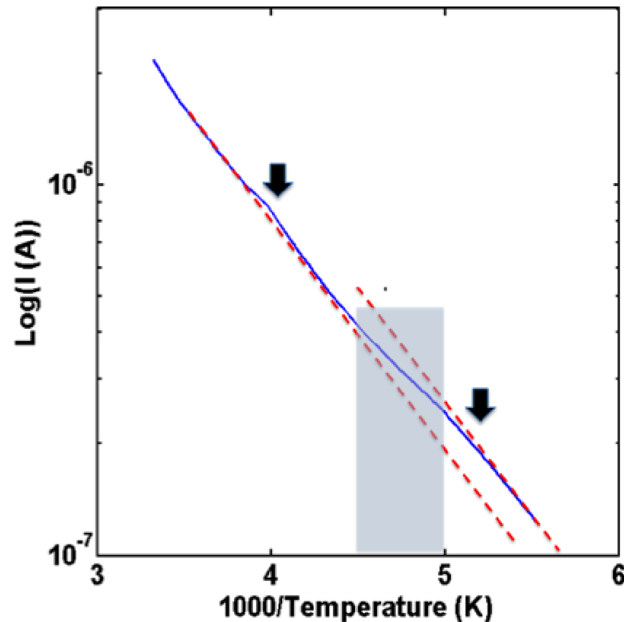

Figure 4.19 - Anomalies in the temperature dependence of the I_{DS} current caused by super-cooled trapped water. The anomalies are highlight by the arrows and locate below 200 K and at 240-250 K

Figure 4.19 shows the temperature dependence of the I_{DS} current for a TFT not exposed to light. As highlight by the dashed lines the real curve does not follow a perfect straight line. Two shoulders or knees are observed. One knee starts just below 200 K and the other is located between 240-250 K. This behavior has been previously observed and reported temperature dependence in TFTs using SiO_2 as a dielectric layer. The anomalous behavior at 240 K and 200 K coincides with phase transition of trapped water.

A trap filling mechanism explains quite well the anomalies in the temperature dependence of the current caused by water. At low temperatures (T<190 K) all the traps are empty. These traps are in a finite number. Furthermore, for reasons not yet fully understood these traps are active as the temperature approaches 200 K. Above 200 K the traps begin to capture electrons, which oppose the external gate-bias causing an increase in the threshold voltage shift and a corresponding decrease in the current. This trapping seems to evolve with the temperature and reaches its maximum at 240 K. Therefore, we propose that all the traps get full (traps are exhausted) and the current recovers its normal activated behavior. A similar process must cause the second anomaly above 240-250 K.

CHAPTER 5 - Conclusion

Summary

This chapter provides a final review of all the contents discussed in this dissertation. First it will give conclusions about the main topics discussed and then some suggestions for future work will be presented.

5.1 Conclusions

This dissertation presents a study of the electrical properties of oxide based TFTs. Among the important topics studied here was the electrical instability occurring when the TFTs is exposed to light. The experiments and the data analysis presented in this thesis lead to a number of important conclusions, namely:

1. Prolonged light exposure with energy equal or above the ZTO band gap induces long-lived dopant states. Temperature dependent experiments have shown these dopant states are located at 0.14 eV from the conduction band edge. These states become neutralized at high temperature. The neutralization process is thermal activated and causes an anomalous behavior on the temperature dependence of the TFT current. For temperatures above 300K the current increases less rapidly and eventually decreases with temperature.
2. Light induced dopant states are long-lived. The time constant for their neutralization is 3.5 hours at approximately 300 K.
3. Gate-bias stress effects and light-induced dopants are two distinct processes usually present in all the samples. However, if the gate-bias stress is pronounced, it is difficult to disentangle the light effects from the stress effects. Therefore, it is convenient to use relatively stable TFTs (against gate-bias stress effects).
4. Base on other studies reported in the literature, it is proposed that the chemical species responsible for the light-induced states are ionized oxygen vacancies. However, further experiments are required to prove this.
5. TFTs with a large number of defects have a poor operational stability.

5.2 Suggestions for further work

Light induces long-lived dopant species that change the electrical conductivity of the TFT. At RT these states remain active for several hours. The time constant of the current decay is 3.5 hours. In reality this means that the TFT can be programmed into a high conductance state. Although this state is volatile the life-time is long enough to consider their possible use in photosensitive devices. A particular interesting one is a Charge Coupled Device (CCD).

The main use of these CCDs is on scanners, digital cameras, satellite images, medical devices, instrumentation for astronomy equipment, etc. Basically where high quality images are required. [93]

When compared with sputtered films, solution based films have good electronic performances. They reach similar mobility values and low threshold voltages. These solution based films have an interesting advantage due to the fact they can be processed in flexible and low-cost substrates such as paper or plastic. However these TFTs are significant less stable than the ones produced by thermal sublimation. Research is required to improve the operational stability of solution based TFTs.

Other interesting area is the development the p-type oxide semiconductors. These semiconductors still have some problems to surpass. Their performance is very poor when compared with the characteristics achieved by the n-type oxides. Research in this area is crucial to achieve the fabrication of CMOS circuits.

Recently it has been a huge development on these inorganic solution based oxide TFTs, which will increase the use more often of this type of technology. Because of that, it is important that the abundant increase on semiconductors do not rely on toxic elements. So it is important to move on to environmental friendly solvents on solution processed oxide semiconductors [39].

The current limitation on solution-based processes still is the high temperatures. Solution-based processes and new notable applications will continue to be a researched target in the future. This can happen if improved low-temperature chemistries or processes start being developed. The achievement of low temperature processes and rational device reliability will be vital to the success of this promising technology [2].

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