Control of Distributed Power Flow Controllers using active power from homopolar line currents

Ivo M. Martins*, Fernando A. Silva**, Sónia F. Pinto**, Isménio E. Martins*
*CIEEE, Department of Electrical Engineering, ISE, University of Algarve, Faro, Portugal
**CIEEE, Department of Electrical and Computer Engineering, IST, TU Lisbon, Portugal

***Abstract* – Flexible AC Transmission Systems (FACTS) devices can be used for power flow control in AC transmission grids, improving power line utilization and performance. Nowadays, Unified Power Flow Controllers (UPFC) are one of the most useful FACTS, allowing the simultaneous control of the bus voltage and line active and reactive power. However, due to high costs and reliability concerns, the utilization of this technology has been limited in such applications.**

The concept of Distributed FACTS (DFACTS) and Distributed Power Flow Controller (DPFC) was recently introduced as a low coast alternative for power flow control. This paper presents a distributed power flow controller that uses third-harmonic frequency currents transmitted through the line to independently control active and reactive power flow at fundamental frequency.

Simulations were carried in the Matlab/Simulink environment.

***Index Terms* – FACTS, DFACTS, UPFC, DPFC, Power Flow Control.**

I. Introduction

All over the world electric power supply systems are widely interconnected, involving national and international connections. This is done for economic reasons, to reduce the price of electricity, but mainly to increase the capacity and reliability of the electrical energy supply. Interconnections between transmission networks can take full advantage of the availability of electricity production systems, depending on the diversity of the load, and minimize also the costs of energy production, maintaining stability.

Although energy transmission is often an alternative to the implementation of new energy production systems, the costs of transmission lines, losses associated with energy transmission and the difficulties to obtain new corridors limit the available transmission capacity. Moreover, the introduction of renewable energy has brought an increasing number of probabilistic variables to the electrical system, since the production of electricity became uncertain and less controllable. This uncertainty in production also leads to an uncertain power flow in transmission lines. Thus, it became essential to improve the performance of power lines and the optimization of power flow on existing lines.

The development of new technologies based on power electronic converters allows a solution for these problems, offering the possibility of power flow control both in static and dynamic conditions, making the transmissions systems more flexible. FACTS devices can be inserted in existing transmission lines to achieve control functions, including enhancement of power transfer capacity, decrease line losses and generation costs, and improve the stability and security of the power system [1,2]. The Unified Power Flow Controller is a third generation FACTS system and is the most powerful FACTS device currently. It uses solid state power semiconductors and can be used for power flow control, improvement of transient stability, damping oscillations and active filtering [3]. In most recent research works, the UPFC is primarily used to control a local bus voltage and active and reactive power flows of a transmission line. However, in practice, the UPFC series converter may have other control modes such as direct voltage injection, phase angle shifting and impedance control modes, [4].

The UPFC is the combination of a Static Synchronous Compensator (STATCOM) and a Static Synchronous Series Compensator (SSSC), coupled via a common DC link allowing active power exchange between the two converters. The converter in series with line acts as a synchronous ac-voltage source and provides the main function of the UPFC by injecting a controllable voltage vector. The shunt converter acts as a synchronous source controlling the voltage of the dc capacitor (U_{dc}). Fig. 1 illustrates the simplified diagram of UPFC.

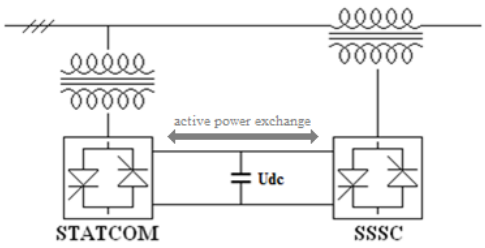

Figure 1 – Simplified diagram of UPFC

Typical FACTS devices can operate at up to 345 kV and can be rated as high as 200 MVA. Even though FACTS technology is technically proven, it has not seen widespread commercial acceptance due to a number of reasons [5,6]: *i)* High system power ratings require the use of custom high power devices; *ii)* High fault currents and basic insulation requirements stress the power electronics system; *iii)* Utilities require higher reliability levels than what they have so far experienced with FACTS devices; *iv)* Required skilled work force in the

field to maintain and operate the system; *v)* High total cost of ownership.

For a lower cost and higher reliability the concept of distributed FACTS devices has recently been proposed as an alternative approach for realizing the functionality of FACTS devices [5,6,7,8]. Currently, the presented DFACTS device is the Distributed Static Series Compensator (DSSC), presented in Fig. 2. Since the DSSC has no power source, it can only adjust the line impedance, and is not as powerful as UPFC.

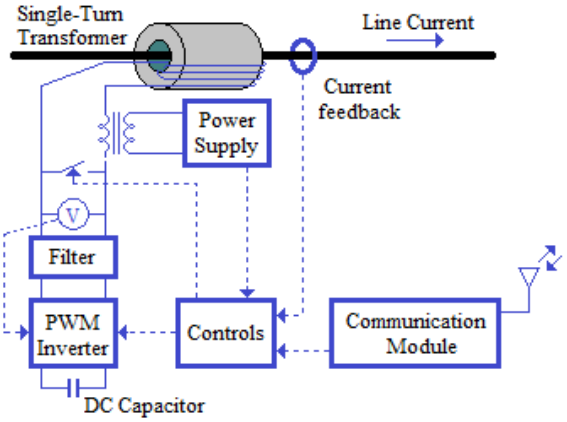

Figure 2 – Circuit schematic of a DSSC module

To obtain the functionality of UPFC using the concept of DFACTS devices, a new concept of distributed power flow controller (DPFC) that combines conventional FACTS and DFACTS has already been proposed [9]. The DPFC is derived from the UPFC but eliminates the common DC link between the shunt and series converters. The same as the UPFC, the DPFC gives the possibility to control system parameters, such as line impedance and power angle.

This paper presents the controller for a distributed power flow controller able to control active and reactive power flow in static and dynamic conditions. Third-harmonic currents injected into the line provide active power for the DPFC to control active power flow at fundamental frequency.

To test the designed controller, switching models were built in Matlab/Simulink environment. Some simulation results are presented and discussed.

II. Distributed Power Flow Controller

The DPFC uses multiple small-size single-phase converters, distributed in series with the transmission line, to inject a relatively small controllable voltage vector to vary the transmission angle and line impedance, allowing cross-coupled control of active and reactive power flow. The use of a large number of DPFC devices provides increased system reliability due to redundancy of the series converters. Each converter within the DPFC is independent and has its own dc capacitor to provide the required dc voltage. Fig. 3 shows the configuration of a transmission line with DPFC devices.

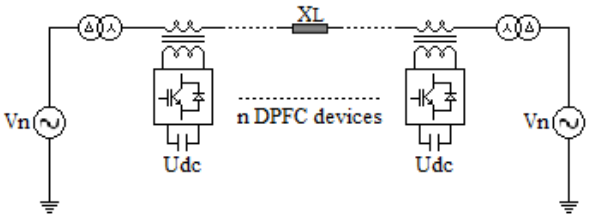

Figure 3 – Transmission line with DPFC devices

To provide independent control of active and reactive power (as in the UPFC) it is necessary to supply active power to all DPFC devices, to maintain the voltage of the dc capacitor (U_{dc}). So, in order to eliminate the common DC link of UPFC, in this paper it is proposed that the required active power is transmitted to all devices through the line at third-harmonic frequency. Once the active power at different frequencies is isolated from each other, it is possible to DPFC devices to absorb active power at third-harmonic frequency and release it at the fundamental frequency. Fig. 4 illustrates the power flow diagram in a transmission line with DPFC devices. As can be seen each DPFC device handles active and reactive power at fundamental frequency and active power at third-harmonic frequency.

The required active power needed by DPFC devices can be supplied by a conventional controlled voltage source shunt converter, as described in [9], represented in Fig. 4 as a third-harmonic current source (I_{3h}).

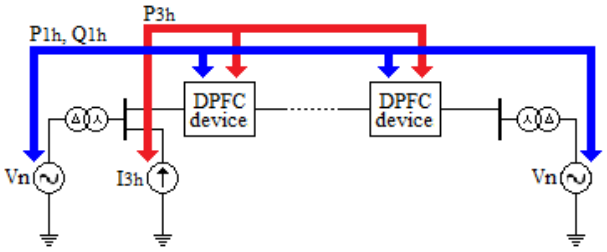

Figure 4 – Power flow diagram

As illustrated in Fig 4, the transmission line carries both the current at fundamental and third-harmonic frequency. In order to block the harmonic which carries the active power transmitted to DPFC devices, zero sequence harmonic is selected, since the most widely used transformer in power systems is Y-Delta transformer, which has the capability to block the zero sequence component naturally, preventing the harmonic leakage to the rest of the network.

A. DPFC Converter Model

The DPFC converter topology presented in Fig. 5 uses three single-phase half-bridge legs sharing a common dc bus subdivided by two capacitors (C_1 and C_2). The voltage across each capacitor is approximately half of the dc voltage bus (U_{dc}), allowing each converter leg to deliver one of two possible voltages levels $U_{dc}/2$

($Uc1$) or $-U_{dc}/2$ ($-Uc_2$) between its output and the converter neutral point (v_{ok}).

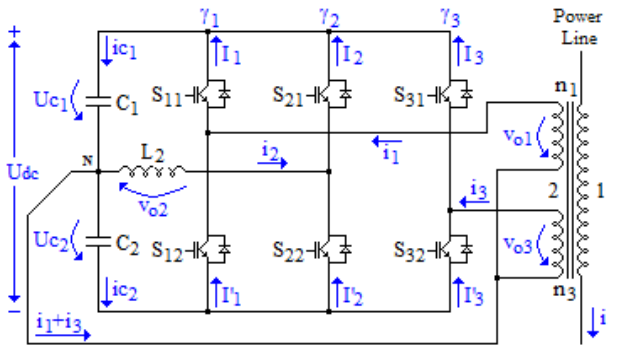

Figure 5 – DPFC converter topology

Switching Variables

Assuming semiconductors as ideal switches, each converter leg can be represented by the switching variable γ_k ($k \in \{1,2,3\}$), and each switch represented by the control variable S_{ki}. Each switch has two possible states, *on* ($S_{ki}=1$) or *off* ($S_{ki}=0$), allowing two possible switches states combinations to produce the two different voltage levels in each leg (Table 1).

Table 1 – Single-phase half bridge converter voltage levels and corresponding switch states

γ_k	S_{k1}	S_{k2}	v_{ok}
1	1	0	U_{C1}
0	0	1	$-U_{C2}$

To guarantee the topological constraints of this converter, for each leg the switching strategy must ensure complementary states between switches pairs:

$$S_{k1} = \overline{S_{k2}} \tag{1}$$

According to restrictions (1), the switching variable γ_k can be defined as:

$$\gamma_k(t) = \begin{cases} 1 & if \quad S_{k1} \quad ON \quad and \quad S_{k2} \quad OFF \\ 0 & if \quad S_{k2} \quad ON \quad and \quad S_{k1} \quad OFF \end{cases} \tag{2}$$

State-Space Model

Analyzing the converter in Fig. 5, the v_{ok} voltage and I_k and I'_k currents can be represented as function of the γ_k switching variable.

$$v_{ok} = \begin{cases} Uc_1 & if \quad \gamma_k = 1 \\ -Uc_2 & if \quad \gamma_k = 0 \end{cases} \tag{3}$$

$$I_k = \begin{cases} i_k & if \quad \gamma_k = 1 \\ 0 & if \quad \gamma_k = 0 \end{cases} \tag{4}$$

$$I'_k = \begin{cases} 0 & if \quad \gamma_k = 1 \\ -i_k & if \quad \gamma_k = 0 \end{cases} \tag{5}$$

Voltage v_{ok} equations and I_k and I'_k currents can be rewritten as:

$$v_{ok} = \gamma_k.Uc_1 + (\gamma_k - 1).Uc_2 \tag{6}$$

$$I_k = \gamma_k.i_k \tag{7}$$

$$I'_k = (\gamma_k - 1).i_k \tag{8}$$

Using the Kirchoff laws one can obtain the capacitor voltage differential equation (9).

$$\frac{d}{dt}\begin{bmatrix} Uc_1 \\ Uc_2 \end{bmatrix} = \begin{bmatrix} \frac{\gamma_1}{C_1} & \frac{\gamma_2}{C_1} & \frac{\gamma_3}{C_1} \\ \frac{\gamma_1 - 1}{C_2} & \frac{\gamma_2 - 1}{C_2} & \frac{\gamma_3 - 1}{C_2} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{9}$$

Considering the circuit in Fig. 5, where the converter output voltages v_{o1} and v_{o3} are applied to an isolated neutral power line, modeled by their Thevenin equivalent (R-L impedance and open-circuit electromotive force u_S), and v_{o2} is applied to the inductance L_2, the converter output currents i_k can be expressed:

$$\begin{cases} v_{o1} = -R.i_1 - L\dfrac{di_1}{dt} + u_S \\ v_{o2} = -L_2\dfrac{di_2}{dt} \\ v_{o3} = -R.i_3 - L\dfrac{di_3}{dt} + u_S \end{cases} \tag{10}$$

Replacing (6) in (10) and considering (9), the converter switching state-space model can be obtained:

$$\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ Uc_1 \\ Uc_2 \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & -\frac{\gamma_1}{L} & \frac{1-\gamma_1}{L} \\ 0 & 0 & 0 & -\frac{\gamma_2}{L_2} & \frac{1-\gamma_2}{L_2} \\ 0 & 0 & -\frac{R}{L} & -\frac{\gamma_3}{L} & \frac{1-\gamma_3}{L} \\ \frac{\gamma_1}{C_1} & \frac{\gamma_2}{C_1} & \frac{\gamma_3}{C_1} & 0 & 0 \\ \frac{\gamma_1 - 1}{C_2} & \frac{\gamma_2 - 1}{C_2} & \frac{\gamma_3 - 1}{C_2} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ Uc_1 \\ Uc_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} \cdot [u_S] \tag{11}$$

B. DPFC Simplified Model

From the conceptual viewpoint, each DPFC device can be replaced by two controllable voltage sources in series with the transmission line. Thus, each converter generates voltage at two different frequencies, one at fundamental frequency (v_{o1}) and the other at third-harmonic frequency (v_{o3}), as represented in Fig. 6.

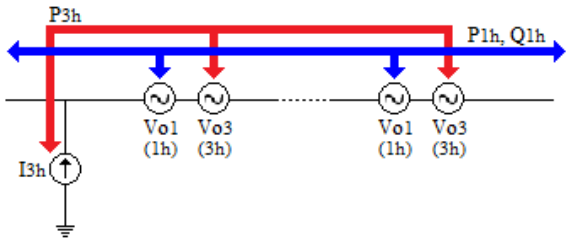

Figure 6 – DPFC converter power exchange diagram

The series injected voltage v_{o1} acts as a synchronous ac-voltage source at fundamental frequency with controllable magnitude and phase, resulting in active and reactive power injection or absorption between the converter and the transmission line, allowing independently control of the fundamental active and reactive power flow (P_{1h} and Q_{1h}). The reactive power is generated internally by the converter and the active power is supplied through the dc capacitors.

The series injected voltage v_{o3} regulate the dc bus voltage (U_{dc}) by absorbing or generating active power from the line at third-harmonic frequency (P_{3h}). This active power absorbed from third-harmonic is equal to the active power generated by the converter at fundamental frequency, if the converter is loss-less.

As presented in Fig. 5, the proposed DPFC converter topology has a third output voltage v_{o2}, internally applied to the inductance L_2, allowing the exchange of active power between the two capacitors. This generated voltage is responsible to balance the dc voltages Uc_1 and Uc_2, ensuring an approximately $U_{dc}/2$ neutral point voltage.

III. DPFC CONTROL

In a power transmission system with multiple DPFC devices each device needs a local controller for its own converter. Additionally, a central control system is required to generate reference signals for all devices.

The control of the DPFC converter, presented in Fig. 5, consists of the following three control loops:

- Fundamental output voltage control
- Third-harmonic output voltage control
- Capacitor voltages equalization

Each controller operates one of the three single-phase half-bridge legs of the converter, each one responsible for controlling the output voltages v_{o1}, v_{o3} and v_{o2}. The function of each controller is explained next.

A. Fundamental Output Voltage Control

The fundamental frequency control is the main control loop with the DPFC converter control. The principle of the controller is to inject a relatively small controllable voltage vector at fundamental frequency, cooperating to control active and reactive power flow through transmission lines. The power flow control capability of the DPFC depends on this injected voltage and has the following relationship:

$$(P_{1h}-P_{0,1h})^2+(Q_{1h}-Q_{0,1h})^2=\left(\frac{|V_{o1}|.|V_n|}{|X_{L,1h}|}\right)^2 \quad (12)$$

where $P_{0,1h}$ and $Q_{0,1h}$ are the fundamental active and reactive power flow of the uncompensated system, $X_{L,1h}$ is the line impedance at fundamental frequency, $|V_{o1}|$ is the injected voltage magnitude and $|V_n|$ is the voltage magnitude at both ends.

For this purpose, the injected voltage should emulate an *R-L* series impedance such that the transformer should see a secondary winding voltage v_{o1}:

$$v_{o1}=n_1.(R.i_{1h}+L\frac{di_{1h}}{dt}) \quad (13)$$

where i_{1h} is the line current at fundamental frequency and n_1 the transformer winding ratio. Determining parameters *R* and *L* results in active and reactive power injection or absorption between the converter and the transmission line, as presented in Table 2:

Table 2 – Power exchange at fundamental frequency between DPFC converter and transmission line according to parameters *R* and *L*

R	***L***	P_{1h}	Q_{1h}
< 0		Injection	
> 0		Absorption	
	< 0		Injection
	> 0		Absorption

To obtain the desired output voltage vector v_{o1}, the correspondent leg of the converter (γ_1) is operated as a pulse width modulation (PWM) converter and controlled to generate a v_{PWM} average voltage (V_{PWM}) within a switching period T_{PWM}:

$$V_{PWM}=\frac{1}{T_{PWM}}\int_0^{T_{PWM}} v_{PWM}\,dt \approx v_{o1} \quad (14)$$

Considering balanced dc capacitor voltages ($Uc_1=Uc_2=U_{dc}/2$), the v_{ok} voltage (6) can be expressed as:

$$v_{ok}=\frac{U_{dc}}{2}(2.\gamma_k-1) \quad (15)$$

According to (15) the instantaneous value of the output voltage v_{PWM} of the correspondent leg of the converter is:

$$v_{PWM} = \begin{cases} \frac{U_{dc}}{2} & if \quad \gamma_1 = 1 \\ -\frac{U_{dc}}{2} & if \quad \gamma_1 = 0 \end{cases} \tag{16}$$

The output voltage v_{PWM} must be modulated so that its mean value, in each switching period T_{PWM}, equals the desired v_{o1} voltage, considered constant at each switching period, since T_{PWM} is much smaller than the line period (20 ms). Therefore, it can be written:

$$\frac{1}{T_{PWM}} \int_0^{T_{PWM}} (v_{o1} - v_{PWM}) dt = 0 \tag{17}$$

Considering the error:

$$e_{v_{o1}} = \int_0^{T_{PWM}} (v_{o1} - v_{PWM}) dt \tag{18}$$

and from sliding mode theory [10], the sliding surface that determines the semiconductors switching law is:

$$S(e_{v_{o1}}, t) = K_{v_{o1}} \int_0^{T_{PWM}} (v_{o1} - v_{PWM}) dt = 0 \tag{19}$$

Fig. 7 represents the sliding surface block diagram of the fundamental output voltage controller.

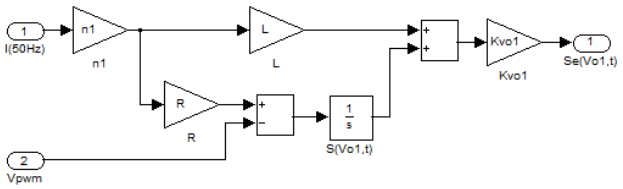

Figure 7 – Block diagram of the v_{o1} voltage sliding surface

To ensure reaching mode behavior and sliding mode stability [10], and assuming a small error ε for the sliding surface (19), the switching law is:

$$\begin{cases} S(e_{v_{o1}}, t) > +\varepsilon \Rightarrow \dot{S}(e_{v_{o1}}, t) < 0 \Rightarrow v_{PWM} \uparrow \Rightarrow v_{PWM} = \frac{U_{dc}}{2} \Rightarrow \gamma_1 = 1 \\ S(e_{v_{o1}}, t) < -\varepsilon \Rightarrow \dot{S}(e_{v_{o1}}, t) > 0 \Rightarrow v_{PWM} \downarrow \Rightarrow v_{PWM} = -\frac{U_{dc}}{2} \Rightarrow \gamma_1 = 0 \end{cases} \tag{20}$$

Switching law (20) provides the single-phase half-bridge PWM modulator presented in Fig. 8, and is implemented using one hysteretic comparator with ε width that directly gives the switching variable γ_1. The switching signals S_{11} and S_{12} applied to the semiconductors are obtained from γ_1.

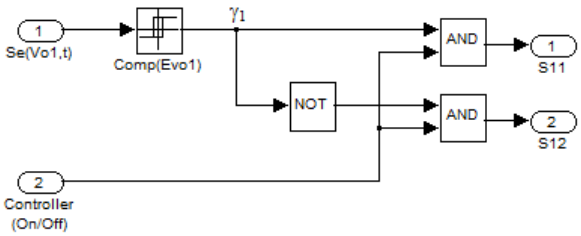

Figure 8 – Single-phase half-bridge PWM generator

B. Third-Harmonic Output Voltage Control

The third-harmonic frequency control loop is responsible to maintain the dc bus voltage of the DPFC converter by using the third-harmonic frequency power. As the line current contains two frequencies components, the third harmonic current through the line is selected as reference to inject a controllable voltage vector in series with the line, absorbing or generating active power from the transmission line.

For this purpose, the injected voltage should emulate a slow time varying series resistor *R(t)* such that the transformer should see a secondary winding voltage v_{o3}:

$$v_{o3} = n_3 . R(t) . i_{3h} \tag{21}$$

where i_{3h} is the line current at fundamental frequency and n_3 the transformer winding ratio. The exchanged energy between DPFC and the transmission line varies in response to the change of the virtual resistance *R(t)*. As a result, the dc bus voltage can be controlled. In the proposed controller, *R(t)* is controlled with a simple proportional-integral (PI) controller applied to the error between reference dc bus voltage U_{dcref} and actual dc bus voltage $U_{dc}=Uc_1+Uc_2$, as following:

$$R(t) = K_p (U_{dcref} - U_{dc}) + \frac{K_p}{T_i} \int_0^T (U_{dcref} - U_{dc}) dt \tag{22}$$

where K_p is the proportional gain and T_i is the integral time of the controller. Fig. 9 represents the virtual resistance control block diagram.

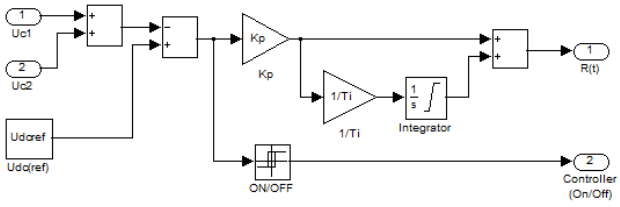

Figure 9 – Virtual resistance *R(t)* block diagram

To obtain the output voltage vector v_{o3}, the correspondent leg of the converter (γ_3) is controlled to generate a PWM output voltage v_{PWM} so that its mean value, in each switching period T_{PWM}, equals the desired v_{o3} voltage. Similarly to the controller presented in

section A, the sliding surface that determines the semiconductors switching law can be written as:

$$S(e_{v_{o3}},t) = K_{v_{o3}} \int_0^{T_{PWM}} (v_{o3} - v_{PWM})dt = 0 \quad (23)$$

Fig. 10 represents the sliding surface block diagram of the third-harmonic output voltage controller.

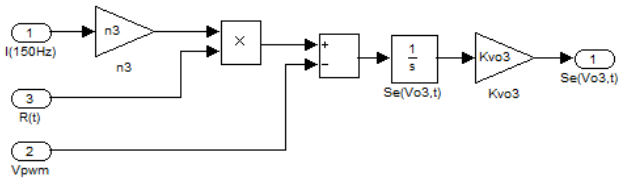

Figure 10 – Block diagram of the v_{o3} voltage sliding surface

As for the fundamental output voltage controller, from the sliding surface (23) one can obtain the correspondent switching law and the single-phase half-bridge PWM modulator that provides the switching variable γ_3. The switching signals S_{31} and S_{32} applied to the semiconductors are obtained from the switching variable γ_3.

C. Capacitor Voltages Equalization

In the DPFC converter topology presented in Fig. 5 it is essential to balance the capacitor voltages Uc_1 and Uc_2, to ensure an approximately $U_{dc}/2$ neutral point voltage. The capacitor voltages equalization technique is a level selection method for the v_{o2} output voltage in order to control the L_2 inductance current (i_2), allowing the exchange of active power between the two capacitors.

Uc_1 and Uc_2 voltage balance is given by:

$$e_{Uc} = Uc_1 - Uc_2 = 0 \quad (24)$$

To ensure condition (24), using sliding mode control method, the sliding surface (25) is defined.

$$S(e_{Uc},t) = k_{Uc}.e_{Uc} = k_{Uc}(U_{C1} - U_{C2}) = 0 \quad (25)$$

Considering identical capacitors ($C=C_1=C_2$) in the DPFC converter topology presented in Fig. 5, the capacitor voltage differential equation (9) can be rewritten as:

$$\frac{d}{dt}(Uc_1 - Uc_2) = \frac{i_1 + i_2 + i_3}{C} \quad (26)$$

where i_2 is the current to be controlled and i_1+i_3 are control disturbances.

Assuming a small error ε for the sliding surface (25) and considering the capacitor voltage differential equation (26), the switching law is:

$$\begin{cases} S(e_{Uc},t) > +\varepsilon \Rightarrow \dot{S}(e_{Uc},t) < 0 \Rightarrow i_2 \downarrow \Rightarrow \dfrac{di_2}{dt} < 0 \\ S(e_{Uc},t) < -\varepsilon \Rightarrow \dot{S}(e_{Uc},t) > 0 \Rightarrow i_2 \uparrow \Rightarrow \dfrac{di_2}{dt} > 0 \end{cases} \quad (27)$$

Considering the converter output current equation (10), where:

$$v_{o2} = -L_2 \frac{di_2}{dt} \quad (28)$$

the switching law (27) can be rewritten as:

$$\begin{cases} S(e_{Uc},t) > +\varepsilon \Rightarrow v_{o2} > 0 \Rightarrow v_{o2} = \dfrac{U_{dc}}{2} \Rightarrow \gamma_2 = 1 \\ S(e_{Uc},t) < -\varepsilon \Rightarrow v_{o2} < 0 \Rightarrow v_{o2} = -\dfrac{U_{dc}}{2} \Rightarrow \gamma_2 = 0 \end{cases} \quad (29)$$

Switching law (29) provides the switching variable γ_2 from which it obtains the switching signals S_{21} and S_{22} applied to the semiconductors.

IV. Simulation Results

In this section simulation results are presented in order to show the power flow control capability of the designed controller.

For the proposed controller, switching models were built in Matlab/Simulink environment and simulations were carried considering the implementation of the DPFC in a medium voltage network. All simulations parameters are presented in Table 3.

The simulation considers a transmission line with a total of 4500 DPFC devices (1500 devices per line) with an *0.1pu* power flow control capability, which means that each DPFC device must handle $S_{DPFC}=6,75KVA$. To guarantee a low harmonic distortion of the transmission line current, the injected third-harmonic current should not exceed 10% of the line nominal current, so $I_{3h}=74A$.

Fig 11 shows the sinusoidal waveforms of the third-harmonic output voltage (v_{o3}) and its reference (v_{o3ref}).

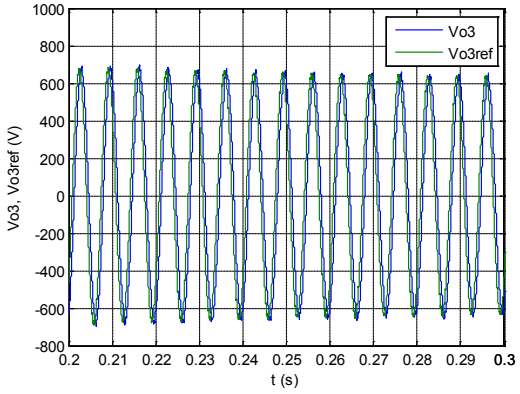

Figure 11 – Third-harmonic converter output voltage

This injected voltage is responsible to regulate the dc bus voltage by exchanging active power with the line at third-harmonic frequency. The reference output voltage varies in response to the change of the virtual resistance *R(t)*, proportional to the error between the reference dc bus voltage U_{dcref} and the actual dc bus voltage $U_{dc}=Uc_1+Uc_2$.

Fig 12 shows the sinusoidal waveforms of the fundamental output voltage (v_{o1}) injected by the converter and its reference (v_{o1ref}). As explained in section III, this capability of injecting a controllable voltage vector allows independent control of the active and reactive power flow. The reference output voltage is calculated according to the specified levels of active and reactive power. As can be seen, the output voltage follows its reference.

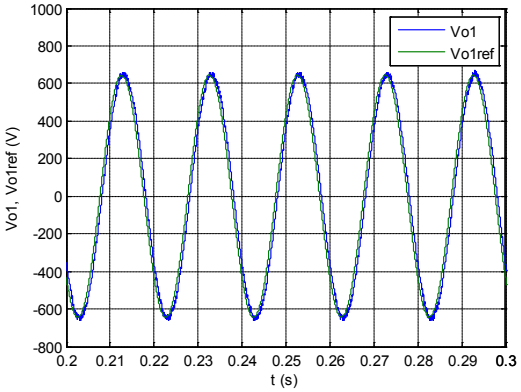

Figure 12 – Fundamental converter output voltage

Fig. 13 shows the simulation results of the active and reactive power injected by the converter. As can be seen the controller ensures the power tracking ($P_{DPFC}=3,38KW$ and $Q_{DPFC}=5,85KVAr$). The total power injected by the converter is $S_{DPFC}=6,75KVA$.

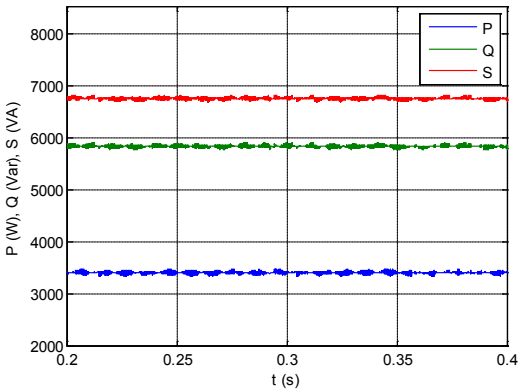

Figure 13 – Active, and reactive power injection

Fig. 14 shows the capacitor voltages Uc_1 and Uc_2.

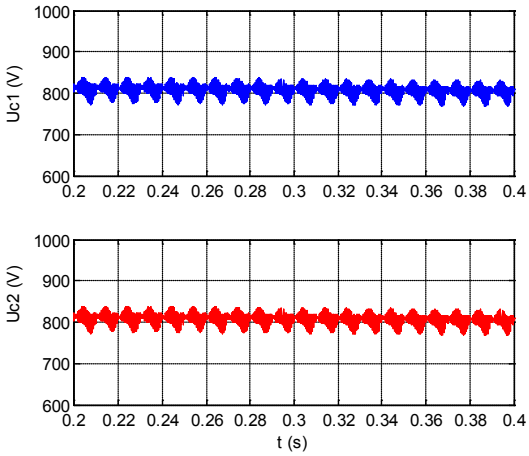

Figure 14 – C_1 and C_2 capacitor voltages

As can be seen the capacitor voltages are balanced, proving the capacitor voltages equalizing strategy capability. Fig. 14 shows both voltages stabilized at the reference dc voltage $Uc_{ref}=806V$.

V. Conclusions

This paper presented a method and a controller for a distributed power flow controller able to control active and reactive power flow through transmission lines. The DPFC controls the power flow by injecting a controllable voltage vector in series with the line at fundamental frequency. The required active power to maintain the converter dc bus voltage is transmitted through the line at third-harmonic frequency. The DPFC has the same control capability as the UPFC with high reliability because of the redundancy of the multiple series converters. The costs of the DPFC system can be lower than the UPFC because low component rating of the series converter but mainly to series production.

For the proposed converter the switching state-space models were obtained and the control laws of the alternating output voltages were studied using the sliding mode control method. The converter switching laws were defined so that a vector controller of the ac voltages of the converter were obtained.

The performance of the capacitors voltage equalizing strategy was also demonstrated, ensuring that the Uc_1 and Uc_2 capacitor voltages are balanced and active and reactive power thought the line are controlled.

VI. Appendix

Table 3 – Simulation parameters

Par.	Value	Description
V_n	220 KV	Transmission line nominal voltage
f_n	50 Hz	Network natural frequency
R_{line}	5,2756 Ω	Line resistance
L_{line}	0,0927 H	Line inductance
C_{line}	$5,8x10^{-7}$ F	Line electrostatic capacitance
P_{load}	100 MW	Load active power

Q_{load}	16,6 MVAr	Load reactive power
I_{3h}	74 A	Third-harmonic line current
n_1	5	Series transformer coupling factor 1
n_2	50	Series transformer coupling factor 2
C_1	$9{,}8x10^{-3}$ F	Converter C_1 capacitor
C_2	$9{,}8x10^{-3}$ F	Converter C_2 capacitor
L_3	$3{,}3\ x10^{-3}$ H	Converter L_3 inductance
Uc_{ref}	806 V	Capacitor reference voltage
E_{Uc}	8	Admissible error for C_1 - C_2 voltage
E_{Vo}	1 V	Admissible error for output voltages
S_{DPFC}	6,75 KVA	DPFC power flow control
P_{DPFC}	3,38 KW	DPFC reference active power
Q_{DPFC}	5,85 KVAr	DPFC reference reactive power

REFERENCES

[1] Narain G. Hingorani and Laszlo Gyugyi, *Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems*, IEEE Press, 1999.

[2] B. M. Zhang and Q. F. Ding, "The Development of FACTS and its Control", *Proceedings of the 4th International Conference on Advances in Power System Control, Operation and Management*, APSCOM-97, Hong Kong, November 1997.

[3] K. Sedraoui, K. Al-haddad and G. Olivier, "A New Approach for the Dynamic Control of Unified Power Flow Controller", *IEEE Power Engineering Society Summer Meeting*, 2001.

[4] L. Gyugyi, C. D. Schauder, S. L. Williams, T. R. Rietman, D. R. Torgerson and A. Edris, "The Unified Power Flow Controller: A New Approach to Power Transmision Control", *IEEE Transactions on Power Delivery*, 1995.

[5] Deepak Divan and Harjeet Johal, "Distributed FACTS – A New Concept for Realizing Grid Power Flow Control", *Power Electronics Specialists Conference*, 36th Annual IEEE[C], Recife Brazil, 2005.

[6] Deepak Divan, "Improving Power Line Utilization and Performance With D-Facts Devices", *Power Engineering Society General Meeting*, IEEE, 2005.

[7] Deepak M. Divan, William E. Brumsickle, Robert S. Schneider, Bill Kranz, Randal W. Gascoigne, Dale T. Bradshaw, Michael R. Ingram and Ian S. Grant, "A Distributed Static Series Compensator System for Realizing Active Power Flow Control on Existing Power Lines", *IEEE Transactions on Power Delivery*, vol. 22, nº. 1, January 2007.

[8] Harjeet Johal and Deepak Divan, "Design Considerations for Series Connected Distributed FACTS Converters", *IEEE Transactions on Industry Applications*, vol. 43, n.º 6, November 2007.

[9] Zhirui Yuan, Sjoerd W.H. de Haan and Braham Ferreira, "A New FACTS Component – Distributed Power Flow Controller (DPFC)", *European Conference on Power Electronics and Applications*, September 2007.

[10] F. Silva and S. Pinto, "Control Methods for Switching Power Converters", Chapter 34, in *Power Electronics Handbook*, 2nd edition, M.H. Rashid, Academic Press, Elsevier, USA, 2007.