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Electrical characterization of metal-oxide-polymer devices for non-volatile memory applications

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PhD thesis in Electronics and Telecommunications

Scientific area: Electronics and Optoelectronics

Work done under the supervision of:

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2013

Statement of Originality

Statement of authorship: The work presented in this thesis is to the best of my knowledge and belief, original, except as acknowledge in the text. The material has not been submitted, either in whole or in part, for a degree at this or any other university.

Candidate:

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(Paulo Roberto Ferreira da Rocha)

This work was financially supported by the Dutch Polymer Institute (DPI), Project No. 704, BISTABLE (resistive switching and OLED reliability) and by Fundação para Ciência e Tecnologia (FCT) through the Instituto de Telecomunicacões (IT).

Acknowledgments

Great things in life come with great effort and a bit of luck. Personally, I have been extremely lucky to have so many important people to guide my effort. My supervisor has undoubtedly been my mentor. Our fruitful discussions motivated me to understand and further my work. Professionally and personally, Prof. Henrique always showed dedication, respect and willingness to help. I also had the great privilege to discuss scientific results (among many other topics) with excellent worldwide researchers such as Dago de Leeuw, Stefan Meskers, John Vaan Haare, Frank Verbakel, and Lode Vandamme. I owe them my gratitude. Furthermore, I am extremely grateful to José Giacometti for the precious help and amazing guidance. I would also like to give special thanks to Prof. Carmo Medeiros. I am forever thankful for her willingness to train me and her belief in me.

I would like to thank my colleagues and friends that directly or indirectly helped me to cross some motivational barriers. I speak of Ricardo Avó, José Coimbra, Mark Guerreiro, Alvaro Barradas, Pedro Inácio, Ana Mestre, Joana Canudo, Qian Chen, Benjamin Bory and Aldric Negrier. Special thanks to my acting group which has been a great support during these last few years. Thank you so much Emilio and Felicidade Croa for teaching me to perform on the stage of life and for your ever present care and affection. And of course, thank you my very dear and precious friend, José Cabecinha.

Without love, life would be shallow, empty, and void of happiness and adventure. I am blessed to have found someone to be my life companion, Ida Gaspar. Through her understanding, motivation and presence, barriers became easier to cross. My parents, João and Neyde Rocha, are undoubtedly the best parents I could have. They never stopped believing and supporting my decisions. Thank you so much to my dear sister Raquel. During my PhD, you sailed to another place. I am sure you will be smiling from up above regarding my life accomplishments. *Foste e serás eternamente um motivo de orgulho e uma lição de vida para todos os que se cruzaram contigo. Obrigado pelo teu apoio.* I am also thankful for the support, motivation and love of my sister, Solange, and brother, João. Furthermore, thank you Fernando, Jessica, Pedro, Delfina, Samuel, Cláudia, Manuel and Olinda for your understanding and special care during these last few years. I am blessed to have you all in my life.

Abstract

The objective of this thesis is to study the properties of resistive switching effect based on bistable resistive memory which is fabricated in the form of Al_2O_3/polymer diodes and to contribute to the elucidation of resistive switching mechanisms.

Resistive memories were characterized using a variety of electrical techniques, including current-voltage measurements, small-signal impedance, and electrical noise based techniques. All the measurements were carried out over a large temperature range. Fast voltage ramps were used to elucidate the dynamic response of the memory to rapid varying electric fields. The temperature dependence of the current provided insight into the role of trapped charges in resistive switching. The analysis of fast current fluctuations using electric noise techniques contributed to the elucidation of the kinetics involved in filament formation/rupture, the filament size and correspondent current capabilities.

The results reported in this thesis provide insight into a number of issues namely:

(i) The fundamental limitations on the speed of operation of a bi-layer resistive memory are the time and voltage dependences of the switch-on mechanism.

(ii) The results explain the wide spread in switching times reported in the literature and the apparently anomalous behaviour of the high conductance state namely the disappearance of the negative differential resistance region at high voltage scan rates which is commonly attributed to a “dead time” phenomenon which had remained elusive since it was first reported in the ‘60s.

(iii) Assuming that the current is filamentary, Comsol simulations were performed and used to explain the observed dynamic properties of the current-voltage characteristics. Furthermore, the simulations suggest that filaments can interact with each other.

(iv) The current-voltage characteristics have been studied as a function of temperature. The findings indicate that creation and annihilation of filaments is controlled by filling and neutralizing traps localized at the oxide/polymer interface.

(v) Resistive switching was also studied in small-molecule OLEDs. It was shown that the degradation that leads to a loss of light output during

operation is caused by the presence of a resistive switching layer. A diagnostic tool that predicts premature failure of OLEDs was devised and proposed.

Resistive switching is a property of oxides. These layers can grow in a number of devices including, organic light emitting diodes (OLEDs), spin-valve transistors and photovoltaic devices fabricated in different types of material. Under strong electric fields the oxides can undergo dielectric breakdown and become resistive switching layers. Resistive switching strongly modifies the charge injection causing a number of deleterious effects and eventually device failure. In this respect the findings in this thesis are relevant to understand reliability issues in devices across a very broad field.

Keywords: Memristor, Negative Differential Resistance (NDR), Resistive Switching, Noise measurements, Electrical characterization, Resistive random Access Memories (RRAM).

Resumo extenso

As memórias resistivas baseiam-se na alteração da resistência elétrica de um material ou componente quando submetido a uma tensão elétrica. Este fenómeno deu origem a um novo elemento eletrónico que se passou a designar por "memristor" por sugestão de Leon Chua em 1971. [1] O "memristor" juntou-se assim aos componentes elétricos mais conhecidos, o condensador, a bobine e a resistência.

Desde os anos 60 que a comutação resistiva tem sido observada numa variedade de materiais. No contexto desta tese os mais interessantes são por exemplo o SiO_x, Al_2O_3, Ta_2O_5, ZrO_2 e TiO_2, onde a comutação resistiva é um processo eletrónico e não envolve uma mudança de fase do material.

Os processos físicos envolvidos na comutação de resistência tem permanecido pouco claros. Os vários mecanismos propostos não tem merecido o consenso da comunidade científica. A ausência de um modelo físico tem impedido o desenvolvimento tecnológico destas memórias que têm assim progredido de forma empírica.

Apesar da falta de conhecimento sobre os mecanismos físicos, as memórias resistivas oferecem um conjunto de vantagens sobre as tecnologias atuais. Isto despoletou uma intensa atividade de pesquisa quer no meio académico quer pela industria para comercializar este tipo de componente. As memórias resistivas combinam num só componente as vantagens de diversas tecnologias atuais. Podem ter a velocidade de acesso das memórias aleatórias de acesso dinâmico (DRAMs) com um custo muito inferior, com menor consumo de energia e sem necessidade de periodicamente fazer o restauro ou "refeshing". Oferecem as características não-voláteis de uma memória do tipo "flash", mas mais robustas, permitindo assim mais ciclos de leitura e escrita. Possibilitam uma elevada densidade e não sofrem dos problemas mecânicos dos discos duros associados com as cabeças de leitura.

A comercialização deste tipo de memórias irá revolucionar as tecnologias de informação ao disponibilizar uma elevada capacidade de memória a baixo custo, em dimensões reduzidas e com muito baixo consumo de energia. As memórias resistivas também não precisam de alguma da eletrónica que acompanha os sistemas atuais, nomeadamente os sistemas de "cache", reduzindo substancialmente os custos e a complexidade dos circuitos.

O trabalho desenvolvido nesta tese foi focado nas propriedades elétricas das memórias resistivas com o objetivo de aumentar o nosso conhecimento sobre os mecanismos físicos e elétricos que controlam a comutação resistiva e a velocidade de acesso.

As memórias estudadas nesta tese são estruturas do tipo metal-isolador-semicondutor (MIS). Foi usado óxido de alumínio e um polímero conjugado para a camada isolante e semicondutora respetivamente. Estas memórias comutam entre dois estados resistivos diferentes quando submetidas a voltagens definidas durante um certo período de tempo. Paralelamente, foi identificado que o processo físico que conduz a bi-estabilidade elétrica do óxido de alumínio é também responsável pela falha prematura de díodos emissores de luz orgânicos (OLEDs). A presença de óxido de alumínio nativo nos eletrodos dos OLEDs pode dar origem a transições resistivas que alteram o equilíbrio da injeção de portadores de carga e leva a degradação da eletroluminescência.

Quer as memórias quer os díodos emissores de luz foram caraterizados usando técnicas elétricas e óticas. Medidas da resposta da corrente a degraus e/ou rampas de tensão permitiram avaliar a velocidade de comutação resistiva. Medidas da impedância no domínio da frequência foram usadas para estudar variações de carga nas interfaces da memória, e por último medidas do ruído elétrico complementadas com medidas óticas permitiram estudar flutuações na corrente causadas pela criação e aniquilação de pequenos caminhos condutores ou filamentos. Todas as medidas foram feitas num grande intervalo de temperatura e frequência.

Esta tese contribui para o esclarecimento dos mecanismos físicos que originam comutações entre estados resistivos não-voláteis. As constantes de tempo que controlam o tempo de acesso à memória, isto é, o tempo para ler, escrever ou apagar foram também estudadas. Os resultados obtidos contribuíram para elucidar o mecanismo físico que determina o tempo de acesso. Estratégias para otimizar a rapidez deste tipo de memoria foram propostas. Foi identificado que a condução elétrica é não-homogénea. A corrente é transportada por filamentos. Foi possível quantificar as dimensões físicas e a densidade de corrente transportada por filamentos individuais. O estudo da dinâmica destes filamentos usando técnicas de análise de ruído elétrico permitiu concluir que os filamentos não são criados nem destruídos, mas sim ligados e desligados como interruptores. O mecanismo que liga os filamentos são buracos armadilhados na camada

de óxido de alumínio. Quando os buracos são neutralizados por eletrões o filamento é desligado. Este resultado foi um dos contributos mais importantes para a área científica.

A condução filamentar dá origem a um conjunto de observações não intuitivas. Concretamente, dá origem a uma dependência anómala da corrente elétrica com a temperatura. A corrente aumenta de forma discreta à medida que a temperatura diminui, isto porque o armazenamento de cargas em armadilhas a baixas temperaturas liga mais filamentos. Adicionalmente, a existência de condução filamentar dá origem a que a corrente elétrica diminua, quando as rampas de tensão rápidas são aplicadas sucessivamente. Os resultados desta tese também sugerem que filamentos de corrente vizinhos podem interatuar e dar origem a fenómenos correlacionados, quer durante o ligar, quer durante o desligar de filamentos. O campo elétrico associado a dois filamentos vizinhos induz um campo elétrico adicional na região intermédia que pode ligar um terceiro filamento. Se um filamento for desligado os filamentos na vizinhança terão mais probabilidade de ser desligados. Simulações usando o "COMSOL Multiphysics" parecem suportar a correlação destes fenómenos.

A comutação resistiva é uma propriedade de óxidos binários. Este fenómeno pode ocorrer de forma não intencional, nomeadamente em díodos emissores de luz, células solares, válvulas de spin, transístores de efeito de campo e de uma forma geral, todos os componentes que usam elétrodos que oxidam. O conhecimento adquirido nesta tese é assim relevante para detetar e prevenir problemas de confiabilidade num conjunto vasto de componentes eletrónicos.

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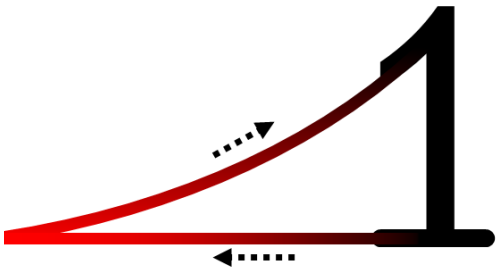
Acronyms

ADS	Advanced Design System
CMOS	Complementary Metal–Oxide–Semiconductor
DRAM	Dynamic Random Access Memory
E	Electric Field
EDX	Energy Dispersive X-Ray
EELS	Electron Energy-Loss Spectroscopy
EEPROMs	Electrically Erasable PROMs:
EFM	Electrostatic force microscopy
EML	Electroluminescence Layer
EPROMs	Erasable Programmable ROMs
ETL	Electron Transport Layer
FRAM	Ferro-electric RAM
FWHM	Full Width at Half-Maximum
HRS	High Resistance State
HTL	Hole Transport Layer
IV	Current Voltage
JV	Current density Voltage
KPM	Kelvin Probe Microscopy
LC-AFM	Local Conducting Atomic Force microscopy
LRS	Low Resistance State
MIM	Metal Insulator Metal
MIS	Metal Insulator Semiconductor
MLC	Multi-Level Cells
MOS	Metal–Oxide–Semiconductor
MOSFET	Metal-Oxide Semiconductor Field-Effect-Transistor
MRAM	Magnetic RAM
NDR	Negative Differential Resistance
NVM	Non-Volatile Memory
OLED	Organic Light Emitting Diode
OTPROMs	One-Time Programmable ROMs

PDF	Probability Density Function
PRAM	Phase change RAM
PTC	Positive Temperature Coefficient
RAM	Random Access Memory
ROM	Read Only Memory
RRAM	Resistive random Access memory
RTN	Random Telegraph Noise
SCL	Space Charge Limited
SLC	Single-Level Cells
SRAM	Static Random Access Memory
TEM	Transmission Electron Microscopy
UVEPROMs	Ultraviolet EPROMs
V_T	Threshold Voltage
WORM	Write Once Read Many
1D1R	One diode, one resistive switching device
1R	One resistive switching device



Introduction

1. Introduction

The aim for fast computation has been focused on many technological fields, mainly in data storage assets. Hard drives and flash memories are only a few components being extremely enhanced in order to offer high read-write speeds and large storage capabilities. All of these focus on delivering a product with the maximum downscale facility at minimum price.

In this chapter a short introduction to data storage techniques is provided as well as a discussion of novel types of memory. The organization of the thesis is also described.

1.1. Memory devices

1.1.1. State of the art

Existent semiconductor memories are mainly focused on Complementary Metal–Oxide–Semiconductor (CMOS) technology and volatile and non-volatile memory. Volatile memory is fast but loses its contents when power is removed. Non-Volatile Memory (NVM) is slower but retains the information without power supply. A NVM device based on semiconductors is a typical Metal–Oxide–Semiconductor (MOS) transistor, e.g. with a source, a drain and a gate terminal. Programming or erasing occurs through electron tunnelling over the insulating layer. Typically volatile memories are Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM). Storage of the charge on the transistor floating gate allows the threshold voltage (V_T) to be electrically altered between a low and a high value to represent logic 0 and 1, respectively. Therefore, DRAM stores a bit of data when a capacitor is charged. Meanwhile the capacitor needs to be periodically charged in a typical interval less than 100 ms, due to its leaking characteristics.

Semiconductor memories can be subdivided into two subcategories based on the ability to rewrite information, e.g. Random Access Memories (RAM) and Read Only Memories (ROM). In contrast to ROMs, in RAMs the information can be written to or read from any cells without read/write cycle limitations. Figure 1.1 illustrates the semiconductor memories explained in this section.

In RAMs the writing and reading times are about the same, whereas in ROMs writing takes more time than reading. In ROMs stored information remains even if the power is turned off, in other words, it is a NVM. On the other hand RAMs are not able to retain the stored information once the power is turned off which makes them volatile memories. Volatile memories such as DRAMs and SRAMs have very fast operation cycles. SRAMs can write and erase in a time of 0.3 ns and are used as a cache memory. [2] DRAMs are slower, being capable of operating in a range of 10 ns. They are used as main memories where the capacity is critical for temporary information storage and processing. [3] NVMs are characterized by their re-programmability. ROMs are classified as One-Time Programmable ROMs (OTPROMs) or Erasable Programmable ROMs (EPROMs). OTPROMs do not have the ability to be reprogrammable, in other words they are non-erasable. EPROMs can be erased either by exposing memory cells to ultraviolet radiation (Ultraviolet EPROMs: UVEPROMs) in which all cells are erased at the same time, or by electrical means (Electrically Erasable PROMs: EEPROMs) in which a byte can be erased through time.

Research is pursuing small, cheap, fast and reliable technologies. A number of alternatives to DRAMs and flash memories have been extensively studied to obtain more powerful and functional memories, so-called emerging memories (see Figure 1.1). The focus of research in emerging memories is on obtaining non-volatile, fast, high-density, low-power consumption, high data transfer rate and reliable memories. If these emerging memories satisfy the positive points of RAMs and ROMs, then they can be universal future memories.

The economic relevance of this matter has easily reached the billion dollar landing and according to MarketResearch.com report, the global market for emerging NVM is expected to increase to $1.6 billion by 2015 at an average annual growth rate of 69 per cent through the forecast period.

Most of non-volatile memories used today consist of four types: flash memory, Ferro-electric RAM (FRAM), Magnetic (MRAM) and Phase change memory (PRAM). Although these technologies are revealed to be quite promising, the scaling down process is proving to be a challenge. Figure 1.1 illustrates the categories of standard semiconductor memories and emerging memories.

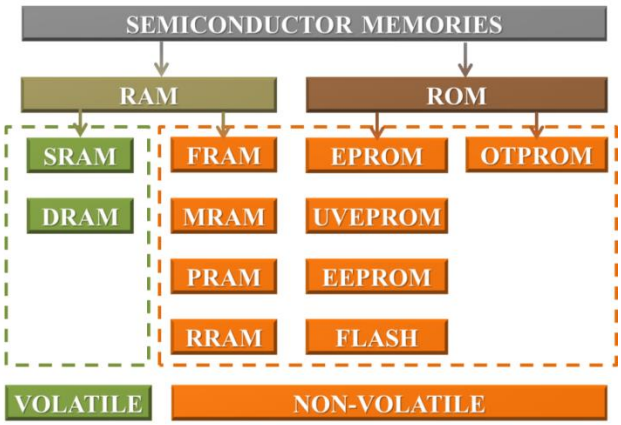


Figure 1.1 - Categories of standard semiconductor memories and emerging memories, e.g. FRAM, MRAM, PRAM and Resistive random Access memory (RRAM). [4]

1.1.2. Flash memories

Flash memory belongs to the class of EEPROM, and is the most suitable structure of non-volatile memory, since one cell consists of only one transistor. Each memory cell in a flash memory consists of only one metal-oxide semiconductor field-effect-transistor (MOSFET) with an additional floating gate, unlike EEPROMs (two MOSFETs). Charge can be stored in this floating node and determines the state of the memory by changing the threshold voltage of the transistor. The addressing process however is much slower than that of DRAM, although these gates can store their charge for a very long time typically write/erase times of 1 ms and 0.1 ms respectively. Figure 1.2 illustrates the cross section of a floating gate transistor.

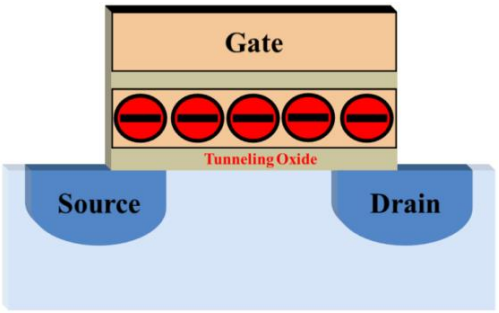


Figure 1.2 - Basic scheme (cross section) of a flash memory cell. Depending on the charge stored in the floating gate one bit Single-Level Cells (SLC) or multiple bits Multi-Level Cells (MLC) can be saved. [5]

The operation of flash is based on a process of removing or putting electrons on the floating gate. Charge on the floating gate affects the threshold of the memory

element. When electrons are present on the floating gate, no current flows through the transistor, indicating logic 0. The transistor is conducting, indicating logic 1, when electrons are removed from the floating gate. The process of forcing electrons to/from the floating gate is achieved by applying a voltage between the control gate and source or drain, e.g. Fowler-Nordheim (F-N) Tunneling.

Transistors organized in a chip form a memory array. Figure 1.3 represents the basics of a memory array.

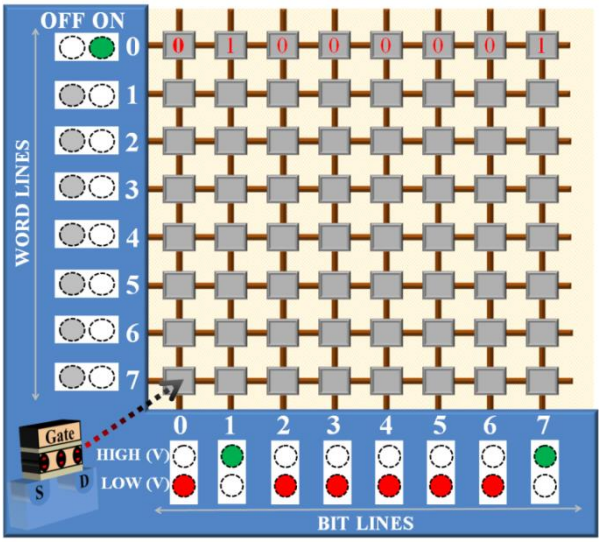


Figure 1.3 - A memory array based on transistors arranged into rows (word lines) and columns (bit lines) inside a memory chip. The illustration represents a byte of data being written in memory. [6, 7]

Transistors are arranged into rows (word lines) and columns (bit lines) inside a memory chip. To write a byte of data to memory, high voltage is applied to the word line on which the byte appears. Then high voltage is applied to the bit lines where a 1 should appear; low voltage is applied to bit lines where a 0 should appear. An example is given where character "A" is stored in the memory by applying voltage so that the binary value 01000001 is represented across a word line. With availability of megabytes (millions of bytes) of memory, sequences of word lines are combined to represent words, sentences, paragraphs and other combinations of alphabetic, numeric and special characters.

The demands of technology necessitate the scaling of flash devices which is becoming harder to achieve in a reliable way due to the limitations of current lithography technology. The operation speed of flash memory is still slow, compared to

volatile memory. The fastest programming times are in the range of μs (also depending on what kind of tunnel process is used) and the erase times are in the ms range. Additionally, although flash memories function well for the typical 5 V operation, there is an international agreement within the electronics industry that the standard Si-logic level will decrease from 5 V to 3.3 V to 1.1 V and eventually to 0.5 V in the coming years. This might represent a significant bottleneck for flash memories once they are based on Fowler-Nordheim tunnelling. Eventually, reliability could become a serious concern at low voltages such as 0.5 V.

In order to satisfy the previously discussed obstacles, a new hope has arisen. Memristor (memory resistor) devices [1] have given hope to semiconductor companies by offering an easier way to increase the storage density by using current fabrication technology. The device is a resistance that maintains a functional relationship between the time integrals of current and voltage. A memristor consists of a two-terminal device whose resistance depends on the magnitude, polarity and length of time of the voltage applied to it. When the voltage is turned off, the resistance remains as it did just before it was turned off. This makes the memristor a non-linear, nonvolatile memory device. In 1971 memristor was defined by Chua [1] as the fourth fundamental circuit element. In 2008, Hewlett-Packard (HP) Labs [8] presented the first experimental realization as well as a theoretical model of memristor. Current fabrication infrastructures warmly welcome a technology that requires even less wafer space which also reduces the complexity of circuit interconnections, and facilitates high density integration when used in crossbar structures. Furthermore, these devices do not suffer any drawback in relation to the quality and reliability of the tunnel oxide. Thus, it is expected that memristor devices will overtake flash memory in speed, scalability and durability.

1.2. Resistive switching

1.2.1. Resistive switching

Resistive switching can exhibit two or more different resistance states referred to in the simplest case as High Resistance State (HRS) and Low Resistance State (LRS). The resistance states are non-volatile and can be toggled by simply exceeding threshold voltages V_{th}, SET or V_{th}, RESET. The digital information like ‘‘0” can be defined by LRS and ‘‘1” by HRS. The information is retrieved by measuring the electrical current,

when a small read voltage V_{read} is applied. In addition intermediate states in LRS and HRS might be used to store more than one bit per cell. [9] Typically this type of element is a Metal Insulator Metal (MIM) structure (see Figure 1.4(a)) that can be incorporated into cross-point arrays (see Figure 1.4(b)), provided that it exhibits sufficient rectification or other nonlinear response.

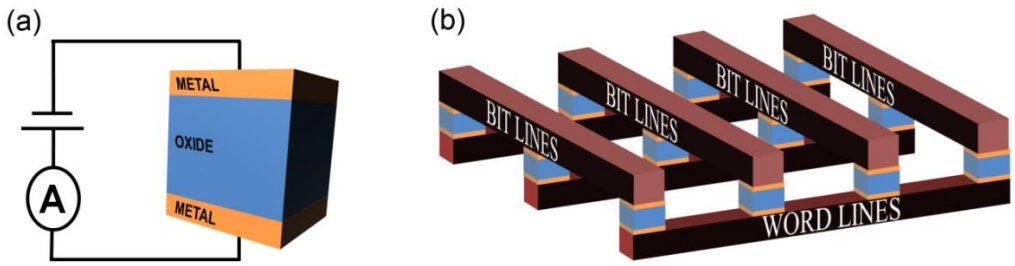


Figure 1.4 – (a) Diagram of a RRAM memory cell with a capacitor-like structure in which an insulating or semiconducting oxide is sandwiched between two metal electrodes. (b) Diagram of a cross-point memory structure. Word and bit lines are used for selecting a memory cell and writing/reading data, respectively.[10-12]

The concept of resistive switching cells deals with two terminal devices instead of three terminal devices as in DRAM where always one access transistor is used. This of course offers the opportunity for novel and advanced architectures. [13, 14]

1.2.2. Categories of resistive switching

Resistive Random Access memory (RRAM) is typically a simple capacitive structure whose resistance can be programmed reversibly by a voltage pulse to be high or low. Once switched, the memory cell retains the particular resistance level for a long time. Devices incorporating switchable resistive materials are generically classified as RRAM. There are numerous variations, few of which have clearly identified mechanisms of conductance and switching. In 1962, Hickmott [15] first reported hysteretic current density–voltage (JV) characteristics in metal-insulator-metal (MIM) structures of $Al/Al_2O_3/Al$, indicating that resistive switching occurs as a result of applied electric fields. Thus, RRAM devices show switching between a low current (OFF) state and a high-current (ON) state as illustrated in Figure 1.5.

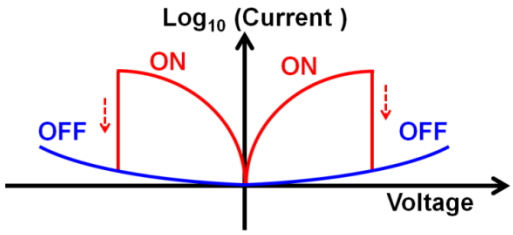


Figure 1.5 – Current -Voltage (I-V) characteristics in the Low Resistive State and High Resistive State of a bistable resistive switching diode.

The voltage controlled Negative Differential Resistance (NDR) region consists of a single or possibly a few switching-off events. The memory can be switched between HRS and LRS by applying voltage pulses with amplitudes corresponding to the top and bottom of the NDR respectively. [16-18] When the LRS current is highly localized to a small fraction of the device area, one has a phenomenon generally named "filamentary" conduction. [19-22]

Usually, resistive switching mechanisms can be classified as unipolar and bipolar switching. Unipolar switching depends only on the amplitude of the applied input (voltage/current), whereas bipolar switching depends on both amplitude and polarity. Unipolar switching means that switching-on and switching-off takes place with the same polarity e.g. either negative or positive (Figure 1.6(a)). Thereby the switching-on operation is limited with a current compliance as illustrated in Figure 1.6(b), the transition from HRS to LRS takes place with one polarity and the switching-off with the opposite polarity.

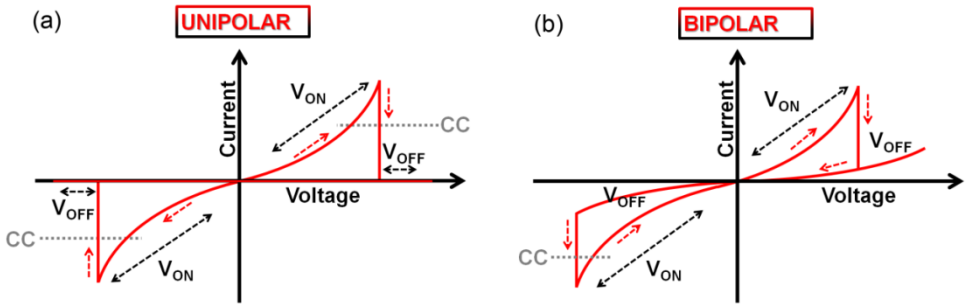


Figure 1.6 – Typical unipolar type of switching curve of a RRAM device. (b) Bipolar type of switching characteristics. In unipolar switching, the switching direction depends on the amplitude of the applied voltage. Bipolar switching shows directional resistance switching according to the polarity of the applied voltage. [12]

1.2.3. Materials for RRAMs

Resistive switching effect has been observed in a variety of materials, including perovskite oxide materials such as $Pr_{1-x}Ca_xMnO_3$ and Cr-doped $SrZrO_3$, [9, 23] binary oxides such as NiO [24] ZnO [25] and ZrO_2, [26] chalcogenides,[27] NiO, Nb_2O_5, Al_2O_3, SiO_x, TiO_2, [16, 28-33] organic materials, [34] and amorphous silicon. [35] Bozano *et al*. published a complete review of these non-volatile memory elements based on organic materials. [36] Already in 1970, switching in various polymers [37, 38] such as polystyrene, polyacetylene and polyaniline [39, 40] was observed. In semiconducting polymers such as poly(vinylcarbazole), [41] poly(thiophene), [42, 43] poly(spirofluorene) [21] and poly(phenylene vinylene) [44] similar switching was observed. Furthermore, switching has also been reported in small molecule semiconductors, such as anthracene, [45] pentacene, [46] Alq_3, [47, 48] TPD, [49] AIDCN, [50] incorporated in MIM diodes. Copper tetracyanoquinodimethane (CuTCNQ) has also been studied. [51-53] For some π-conjugated polymer films that are doped with inorganic salts, memory effects have been reported. [54-56] For this particular class of polymer films, the effects can be interpreted in terms of movement of inorganic ions, a notion that is supported by the observation of relatively gradual changes in conductivity. Another type of conjugated polymer memories, for which a mechanistic explanation of the switching has been established are the polymer fuses. [57] Here the conductivity displayed by conducting polymers (e.g. PEDOT:PSS, polyaniline) can be reduced irreversibly via chemical degradation as a result of Joule heating. These memories classify as Write Once Read Many (WORM). [58] Finally, memory effects have also been reproduced through the inclusion of nanoparticles of different types, like Al nanoparticles [17, 59] or Au nanoparticles [60-64] and the incorporation of a metal inter layer sandwiched between organic or polymeric layers. [64-66]

1.3. Resistive switching models

Up to now, a few models for the driving mechanism of resistive switching have been proposed, [67-71] e.g., thermochemical, oxygen vacancy migration, electrochemical and pure electronic mechanism.

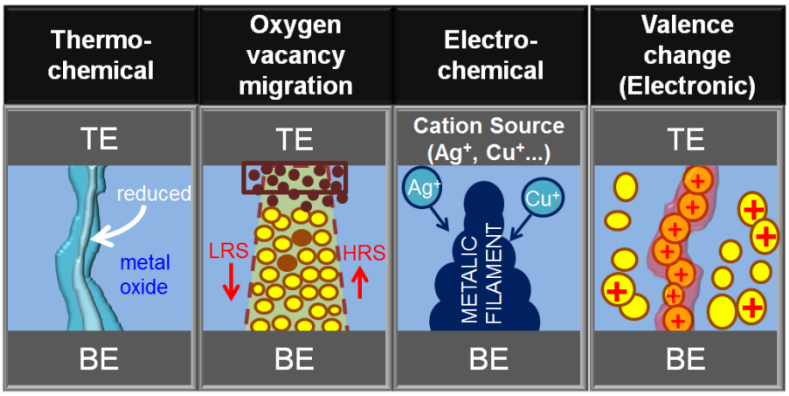


Figure 1.7 - Classification of resistive switching mechanisms in Meal-Insulator-Metal (MIM) structures between Bottom Electrode (BE) and Top Electrode (TE). [72]

The thermochemical mechanism is known as the fuse-anti-fuse type. Applied voltage induces partial breakdown of the switching material, which puts the system in a low resistance state. Then, the filament type conductive path is disrupted by Joule heating which is caused by the high current density through the conductive filament [12] as illustrated in Figure 1.7(a). A typical resistive switching based on a thermal effect shows unipolar characteristics. It is initiated by a voltage-induced partial dielectric breakdown in which the material in a discharge filament is significantly modified due to Joule heating. Due to the current compliance, only a weak conductive filament with a controlled resistance is formed. This filament may be composed of the electrode metal transported into the insulator, carbon from residual organics, [20] or decomposed insulator material such as sub-oxides. [73] The filamentary nature of the conductive path in the LRS has been confirmed (for NiO [74] and TiO_2 [75]). Pt/NiO/Pt thin film based cells have been successfully integrated into CMOS technology to demonstrate non-volatile memory operation. [76] A critical parameter for this unipolar switching effect seems to be the value of the current compliance. In fact, it has been shown that a TiO_2 thin film exhibits bipolar switching, and, on setting the current compliance to a larger value, can be turned into a unipolar switching characteristic. [77]

Oxygen vacancy migration mechanisms depend on binary oxide-based resistive memory structures [78] and the ability of some metals to get oxygen atoms from the rich oxide over layers. A good example is the Ti/HfO_x/Pt device. When a positive bias is applied on the TE, oxygen vacancies are driven towards the bottom interface (HfO_x/Pt) under electrical stimulus. [79] Inhomogeneous migration of oxygen vacancies would lead to the local formation of oxygen-deficient conducting channels [80-82] e.g. LRS. Once a negative bias is applied on the TE, the oxygen vacancies are forced

backwards and gathered near the Ti TE/HfOx interface. The device is therefore switched back to HRS due to the rupture of the oxygen-deficient conducting channel at the HfOx/Pt interface. [83]

The electrochemical mechanism is based on an electrode made from an electrochemically active electrode metal, such as Ag or Cu, an electrochemically inert counter electrode, such as Pt, Ir, W, or Au, and a thin film of a solid electrolyte sandwiched between both electrodes. [84] Using Cu as the active electrode (anode) and Pt as the counter electrode (cathode) metal: [84, 85] (i) anodic dissolution of Cu; (ii) drift of the Cu cations across the solid-electrolyte film under the high electric field; (iii) reduction and electro-crystallization of Cu on the counter electrode surface. The electro-crystallization process leads to the formation of a metal filament. After the filament has grown sufficiently far to make a contact to the opposite Cu electrode, the cell has switched to the LRS. (iv) A sufficient voltage of opposite polarity is applied and the electrochemical dissolution of the metal filament switches the cell to its initial HRS.

Valence change phenomena consist of a considerable generic class of the resistive switching mechanisms. Thus a few relevant mechanisms are discussed. Many binary transition metal-oxides as well as multinary oxides with at least one transition metal sublattice show bipolar resistive switching even though the electrodes do not inject metal cations. This missing cation injection may be either because the electrode metal is not easily oxidized (in the case of Pt, Au, etc.) or the oxidized form is not easily reduced back to the metal (in the case of Al, Ti, Nb, etc.). First reports which seem to fall into this category go back to the 1960s when Nb/NbO_x thin film cells were studied. [86] In the late 1990s, Tokura, Kawasaki and their colleagues started to study bipolar resistive switching phenomena for various manganites [87, 88] while Bednorz and his colleagues focused on titanates and zirconates. [9, 89] Similarly to the electrochemical metallization cells, usually an electroforming step is required before bistable switching is achieved. Often, the electroforming is a somewhat slower process (milliseconds to thousands of seconds), than the actual switching depending on the geometry of the system (thin film MIM structures, lateral MIM cells, single crystals) and the electroforming parameters. The polarity of the bipolar switching cycle is not always obvious. It seems to be determined by many factors such as the work function and the oxygen affinity of the electrode metals, in particular, if different metals are used for the two electrodes of a cell, the polarity of the electroforming process, the formation of

interface layers, etc. [84] A major contribution of this type of resistive switching mechanism falls into a so called electronic view. There are several conceivable mechanisms that lead to a resistance change of the system by purely electronic effects. One possibility is the charge-trap model, [16] in which charges are injected by Fowler–Nordheim tunnelling at high electric fields and become subsequently trapped at sites such as defects or metal nanoparticles within the insulator. This modifies the electrostatic barrier character of the MIM structure and, hence, the resistance of the structure, resembling the gate–channel resistance in Flash FET. For example, metal nano-clusters incorporated in either polymeric [60, 62] or inorganic insulator films [90] are reported as trapping sites. In contrast to the purely electronic switching models, a large body of literature has built up during recent years in which the participation of a transport of anions is considered essential for resistance switching. In many transition metal-oxides, oxygen ion related defects, typically oxygen vacancies, are much more mobile than the transition metal cations. Enrichment or a depletion of oxygen vacancies will affect the valence state of the transition metal cations and may lead to a considerable change in electronic conductivity. [84]

1.4. Aim of the thesis

Resistive switching memories are being investigated due to their huge potential application for data storage. The mechanism is still not well understood. The objective of this thesis is to understand the switching mechanism and to quantitatively explain the switching dynamics.

The thesis is organized as follows. In Chapter 2 the metal-oxide polymer diodes are analysed as a bi-layer structure. A physical model that describes the current-voltage characteristics of the bi-layer is derived. This model is then translated into a simpler and conveniently equivalent circuit that consists of the series-parallel combination of resistors and capacitors. The dynamic behaviour of this equivalent circuit was simulated for both conduction states using triangular voltage profiles with different scan rates. The results were used later to compare with the experimental results and disentangle the effects caused by the resistive switching process.

In Chapter 3 the dynamic response of the non-volatile bistable resistive memory was studied in both the HRS and LRS, using triangular and step voltage profiles. The

results provide insight into the wide spread in switching times reported in the literature and explain an apparently anomalous behaviour of the LRS, namely the disappearance of the negative differential resistance region at high voltage scan rates which is commonly attributed to a “dead time” phenomenon. The HRS response follows closely the predictions based on a classical, two-layer capacitor description of the device. The fundamental limitations on the speed of operation of a bi-layer resistive memory are reviewed and explained.

In Chapter 4, the current–voltage characteristics of RRAM are studied as a function of temperature. Findings indicate that creation and annihilation of filaments is controlled by the filling of shallow traps localized in the oxide or at the oxide/polymer interface.

Low-frequency noise is studied in resistive-switching memories based on metal–oxide polymer diodes in Chapter 5. The noise spectral power follows a $1/f^{\gamma}$ behaviour, with $\gamma = 1$ in the ohmic region and with $\gamma = 3/2$ at high bias beyond the ohmic region. The exponent $\gamma=3/2$ is explained as noise caused by Brownian motion or diffusion of defects which induce fluctuations in diode current. Evidence that the noise is generated in narrow localized regions in the polymer between the contacts is provided.

In Chapter 6, a study on random telegraph noise (RTN) current fluctuations in RRAM devices is presented. The influence of temperature and electric field on the RTN fluctuations is studied in different conductance states to reveal the dynamics of the underlying fluctuators.

In Chapter 7 a diagnostic tool for Organic Light Emitting Diode (OLED) reliability is proposed. The work addresses the early degradation problem using small-signal impedance measurements and electrical noise techniques. It is proposed that a combination of both measurements can be used as a diagnostic tool for OLED reliability.

Chapter 8 describes non intentional resistive switching in other systems. A relation between OLED degradation and resistive switching is discussed. Evidence of trapping mechanisms occurring in the OLED is provided by small-signal impedance results and the observation of optical bursts of higher wavelength than the band-gap electroluminescence. The nature of the trap responsible for resistive switching is suggested based on temperature measurements.

In conclusion, this thesis presents a detailed electrical characterization of the resistive switching mechanism in metal-oxide polymer memories. Resistive switching was also studied in small-molecule OLEDs. It was shown that the degradation that leads to a loss of light output under operation is caused by the presence of a resistive switching layer. A diagnostic tool that predicts premature failure of OLEDs was devised and proposed.

An equivalent circuit model for a metal-oxide polymer diode

Metal-oxide polymer diodes are analysed as a bi-layer structure. A physical model that describes the current-voltage characteristics of the bi-layer is derived. This model is then translated into a simpler and more convenient equivalent circuit that consists of the series-parallel combination of resistors and capacitors. The dynamic behaviour under voltages ramps was simulated for both conduction states; the frequency dependence of the admittance was also simulated. The results were used later in this thesis to compare with the experimental behaviour and disentangle the effects caused by the resistive switching process.

2. An equivalent circuit model for a metal-oxide polymer diode

2.1. Introduction

This chapter presents an equivalent circuit model for the internal capacitive bi-layer structure of metal-oxide polymer memories. A comprehensive analysis of the equivalent circuit response to varying voltages ramps speeds for both conduction states was carried-out. The model predicts the electrical behaviour for both high and low resistance states. The estimated time constants provide insight about which transitions (from high to low resistance or from low to high resistance) control the programming speed of these types of memories. The frequency response of the diode is also derived. It is shown that if the polymer is conductive enough, the bi-layer exhibits a Maxwell-Wagner type of relaxation.

2.2. Device physical structure and equivalent circuit model

The physical model treats the diode as a bi-layer with different conductivity and permittivity as well as different physical dimensions (see Figure 2.1). It also assumes that a space charge layer exists at the interface between the two layers. Although this is only an assumption, clear experimental evidences for this fixed space charge will be provided later in Chapter 3. The differential equation for the current across the bi-layer system is derived. The physical system can be described as a simple equivalent circuit if the physical parameters in the differential equation are replaced by resistances and capacitances. The frequency dependence admittance of the diode is also interpreted using this double RC equivalent network.

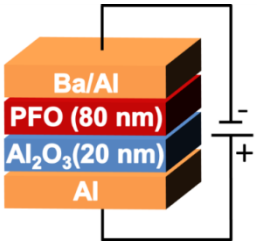


Figure 2.1 - Schematic diagram of the physical structure of a metal-oxide polymer diode

Aluminium oxide-polymer capacitors can be modeled as a two dieletric conductive layers as shown in Figure 2.2.

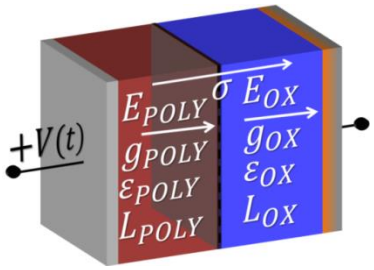


Figure 2.2 – Schematic representation of two dielectric conductive layers in series as a model for the metal-oxide polymer diode.

In Figure 2.2 the device is represented by two dielectric conductive layers, the oxide and the polymer layer, sandwiched between the electrodes and characterized by their thicknesses L_{OX} and L_{POLY} the electric permittivity's ε_{OX} and ε_{POLY}, and electric conductivities, g_{OX} and g_{POLY} respectively. The applied voltage is given by equation (2.1):

$$V(t)=E_{OX}(t)L_{OX}+E_{POLY}(t)L_{POLY}=V_{OX}(t)+V_{POLY}(t) \tag{2.1}$$

Being $V_{OX}(t)$ and $V_{POLY}(t)$ the corresponding voltage drop across the oxide and the polymer layer respectively.

The current density across the device is given by equation (2.2):

$$J(t)=g_{POLY}E_{POLY}(t)+\varepsilon_{POLY}\frac{dE_{POLY}(t)}{dt}=g_{OX}E_{OX}(t)+\varepsilon_{OX}\frac{dE_{OX}(t)}{dt} \tag{2.2}$$

A small current may flow across the two layers. This causes the appearance of a charge density at the interface between the layers as given by equation (2.3):

$$\sigma(t)=\varepsilon_{OX}E_{OX}-\varepsilon_{POLY}E_{POLY} \tag{2.3}$$

This set of equations can be solved allowing us to obtain the dependence of $E_{OX}(t)$, $E_{POLY}(t)$ and $\sigma(t)$ on the applied voltage V(t). The differential equation for $E_{POLY}(t)$ is given by equation (2.4):

$$\left(\varepsilon_{POLY}+\varepsilon_{OX}\frac{L_{POLY}}{L_{OX}}\right)\frac{dE_{POLY}(t)}{dt}+\left(g_{POLY}+g_{OX}\frac{L_{POLY}}{L_{OX}}\right)E_{POLY}(t)=\frac{g_{OX}}{L_{OX}}V(t)+\frac{\varepsilon_{OX}}{L_{OX}}\frac{dV(t)}{dt} \quad (2.4)$$

and can be analytically solved.

The permittivity's and conductivities can be replaced by the resistances, $R_{OX}=\frac{AL_{OX}}{g_{OX}}$ and $R_{POLY}=\frac{AL_{POLY}}{g_{POLY}}$, and capacitances, $C_{OX}=\frac{A\varepsilon_{OX}}{L_{OX}}$ and $C_{POLY}=\frac{A\varepsilon_{POLY}}{L_{POLY}}$. The differential equation for $V_{POLY}(t)$ is described in equation (2.5):

$$\frac{dV_{POLY}(t)}{dt}+\frac{R}{CR_{OX}R_{POLY}}V_{POLY}(t)=\frac{1}{C}\left[\frac{V(t)}{R_{OX}}+C_{ox}\frac{dV(t)}{dt}\right] \quad (2.5)$$

Where $C=C_{POLY}+C_{OX}$ and $R=R_{POLY}+R_{OX}$.

By analysing the above equations, written in terms of capacitances and resistances, one can recognize that the two conductive dielectric layers are equivalent to two parallel RC circuits connected in series as given by Figure 2.3.

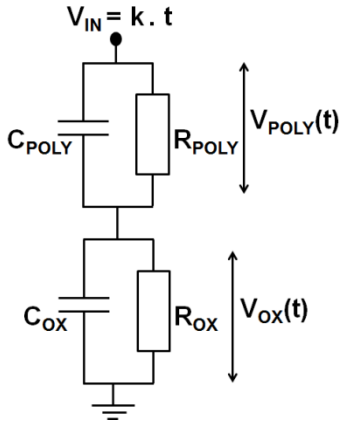


Figure 2.3 - The equivalent circuit used for modelling the bi-layer structure.

Assuming a ramp voltage as $V(t) = kt$ where k is the ramp speed, the expression for the $V_{POLY}(t)$ can be derived as shown in equation (2.6):

$$V_{POLY}(t) = kB\left(1 - e^{-t/\tau}\right) + k\frac{R_{POLY}}{R}t \quad (2.6)$$

Where $B=\frac{R_{POLY}R_{OX}}{R}\left(C_{ox}\text{-}C\frac{R_{POLY}}{R}\right)$.

The time constant for the device to be charged or discharged is $\tau = \frac{C}{R} R_{POLY} R_{OX}$. The electric current, I(t), trough the device can be readily calculated using the equation (2.2) as follows:

$$I(t)=\frac{V_{POLY}(t)}{R_{POLY}}+C_{POLY}\frac{dV_{POLY}(t)}{dt}= \\ =k\left(\frac{B}{R_{POLY}}+\frac{R_{POLY}C_{POLY}}{R}\right)+\frac{k}{R}t+kB\left(\frac{C_{POLY}}{\tau}-\frac{1}{R_{POLY}}\right)e^{-t/\tau} \quad (2.7)$$

2.2.1. Limits for the RRAM in LRS and HRS

The HRS with $C_{OX} \gg C_{POLY}$ and $R_{OX} \gg R_{POLY}$ leads to a time constant for the device of $\tau \cong R_{POLY}C_{OX}$. In this limit the electric current is described through equation (2.8):

$$I(t) \cong k\left(C_{OX}+\frac{t}{R_{OX}}-C_{OX}e^{-t/\tau}\right)=\frac{V(t)}{R_{OX}}+kC_{OX}(1-e^{-t/\tau}) \quad (2.8)$$

Similarly, the LRS $C_{OX} \gg C_{POLY}$ and $R_{POLY} \gg R_{0X}$ lead to $\tau \cong R_{0X}C_{OX}$. In this limit, the electric current is given by equation (2.9):

$$I(t) \cong k(C_{POLY}+\frac{t}{R_{POLY}})=kC_{POLY}+\frac{V(t)}{R_{POLY}} \quad (2.9)$$

The expressions above shows that the electric behaviour for the device in HRS is governed essentially by C_{OX} and R_{OX}, while the LRS is dependent of R_{POLY} and C_{POLY}.

The dependence of the current on the applied voltage, at several ramp speeds (equations 9 and 10) and in both resistive states are given in Figure 2.4(a) and Figure 2.4(b).

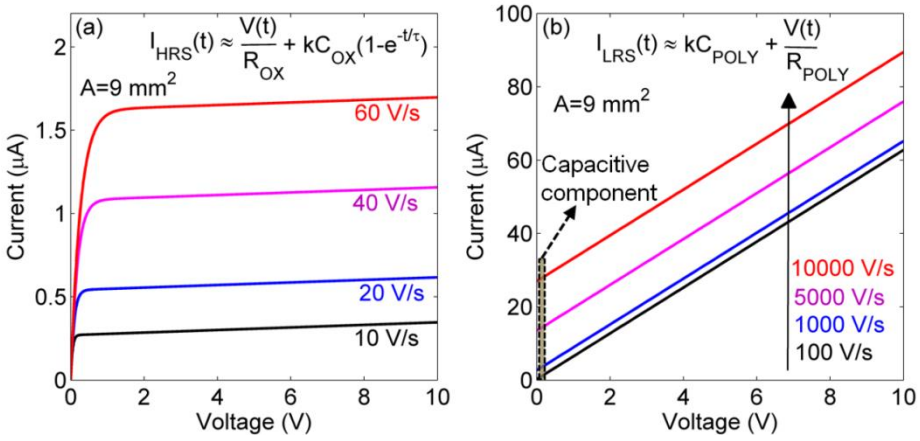


Figure 2.4 - Theoretical IV characteristics of an Al_2O_3/polyspirofluorene (PFO) bistable resistive switching diode obtained (a) in the HRS for different voltage sweep rates (b) obtained in the LRS for different voltage sweep rates.

Figure 2.4(a) shows the experimental JV characteristics for the HRS obtained with increasing voltage scan speeds. The HRS was considered with $C_{OX} \gg C_{POLY}$ and $R_{OX} \gg R_{POLY}$. Meanwhile, the LRS is based on $C_{OX} \gg C_{POLY}$ and $R_{POLY} \gg R_{OX}$. Equation (2.8) is represented in Figure 2.4(a) with a voltage sweeps of 10 V/s, 20 V/s, 40 V/s and 60 V/s. A dynamic behaviour of a parallel plate capacitor is observed. The current increases due to the effect of the displacement current density $j(t)=C_{OX}\, dV/dt$, where C_{OX} is the oxide capacitance per unit area. The current voltage characteristics in the LRS are shown in Figure 2.4(b). A capacitive component of the RC structure is represented in dash lines. The current response in Figure 2.4(b) relates to equation (2.9). The current increases linearly as higher ramp rates are applied. The internal device structure is basically a voltage divider. Since the oxide capacitance is much larger than the polymer capacitance, the voltage division of the applied external bias must depend on the voltage scan speed.

2.2.2. The time constants

The time constant τ_{off} for the device in HRS state is larger compared to the time constant τ_{on} for LRS state since $\tau_{off} \cong R_{POLY}C_{OX}$ and $\tau_{on} \cong R_{OX}C_{OX}$, i.e., $\tau_{off} \gg \tau_{on}$. In the HRS state using values C_{OX}=27 nF and R_{POLY}=160 kΩ, we get τ_{off}=4 ms. In the LRS state using values C_{OX}=27 nF and R_{OX}=50 kΩ, we get τ_{on}=1.5 ms. This agrees with the fact that the device can switch faster from the LRS to HRS than for the HRS to LRS

state. [91] This analysis is important for the diode optimization (in terms of physical dimensions) to achieve the highest switching speed.

2.2.3. The frequency dependence admittance of the diode

The equivalent circuit is also used to explain the frequency dependence admittance of the diode. The simulated frequency dependence of the capacitance and dielectric loss (G/ω) where G is the conductance and ω=2πf of the double RC network is shown in Figure 2.5.

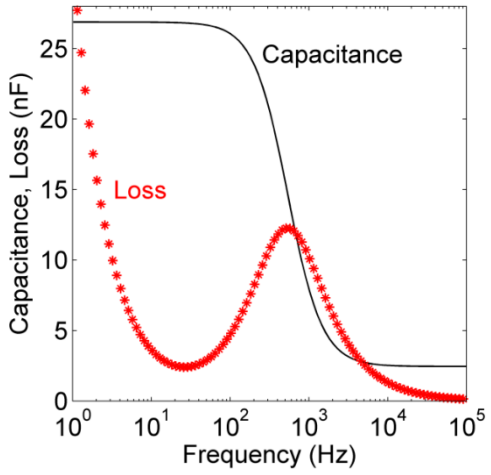


Figure 2.5 – Theoretical representation for the RRAM structure using the equivalent circuit represented in Figure 3. The parameters used are according to the geometrical capacitances as in [92] e.g. R_{OX}=5 MΩ, C_{OX}=27 nF, R_{POLY}=10 KΩ, C_{POLY}=2.7 nF.

In Figure 2.5, the capacitance (C) and loss (G/ω) for a conducting RRAM device is presented. As frequency increases, the capacitance varies between the oxide geometric capacitance to the series capacitance of the oxide and polymer. A high loss at low frequencies which rises as 1/f for a dc resistance is illustrated. The changes in the device are purely resistive. For conducting illustration purposes R_{OX} was set to 5 MΩ representing the LRS. The dispersion centred on 500 kHz is typical of the Maxwell–Wagner relaxation process [93] observed in two-layer dielectric structures and can be modelled by the double RC circuit represented in Figure 2.3. The dispersion in capacitance centred at frequency f_R is given by equation (2.10):

$$f_R = \frac{1/R_{POLY} + 1/R_{OX}}{2\pi(C_{POLY}+C_{OX})} \tag{2.10}$$

Which for $R_{OX} \gg R_{POLY}$ reduces to:

$$f_R = \frac{1}{2\pi R_{POLY}(C_{POLY}+C_{OX})} \tag{2.11}$$

At low frequencies the capacitance is dominated by the oxide capacitance. Above, in equation (2.11) the relaxation frequency the measured capacitance corresponds to the series sum of C_{OX} and C_{POLY}, therefore dominated by C_{POLY}.

2.3. Conclusion

Metal-oxide polymer diodes have been analysed as a bi-layer structure and a physical model that describes the current-voltage characteristics of the bi-layer derived. The dynamic response upon voltage ramps reveals that HRS behaves as a classical parallel plate capacitor. The LRS is ohmic. However, there is a voltage division effect due to the internal bi-layer. The electrical behaviour upon changing voltage ramp speed was calculated for both states. The findings show that the time constants of both states are very different; the time constant associated to the HRS is much longer than the time constant of the LRS. This difference in time constants causes the switch from a high to a low resistance state to take longer than a switch from a low to a high resistance state.

Provided that the polymer layer is conductive, a Maxwell-Wagner dispersion is expected to be observed in the frequency window [20 Hz-1MHz].

Chapter 3 will present the experimental HRS and LRS behaviour upon the input of high speed triangular profiles. Furthermore, a comparison between the calculated and experimental result will be described and the importance of the bi-layer structure in the resistive switching process enlightened.

The role of internal structure in the anomalous switching dynamics of metal-oxide polymer resistive RAMs

The dynamic response of a non-volatile, bistable resistive memory fabricated in the form of Al_2O_3/polymer diodes has been probed in both the HRS and LRS using triangular and step voltage profiles. The results provide insight into the wide spread in switching times reported in the literature and explain an apparently anomalous behaviour of the LRS, namely the disappearance of the negative differential resistance region at high voltage scan rates which is commonly attributed to a "dead time" phenomenon. The HRS response follows closely the predictions based on a classical, two-layer capacitor description of the device. As voltage scan rates increase, the model predicts that the fraction of the applied voltage, V_{ox}, appearing across the oxide decreases. Device responses to step voltages in both the HRS and LRS show that switching events are characterized by a delay time. Coupling such delays to the lower values of V_{ox} attained during fast scan rates, the anomalous observation in the LRS that, device currents decrease with increasing voltage scan rate, is readily explained. Assuming that a critical current is required to turn off a conducting channel in the oxide, a tentative model is suggested to explain the shift in the onset of negative differential resistance to lower voltages as the voltage scan rate increases. The findings also suggest that the fundamental limitations on the speed of operation of a bi-layer resistive memory are the time- and voltage-dependences of the switch-on mechanism and not the switch-off process.

3. The role of internal structure in the anomalous switching dynamics of metal-oxide polymer resistive RAMs

3.1. Introduction

The development of new non-volatile memory devices is being actively pursued. One type offering excellent prospects is the RRAM device, a simple diode structure whose resistance can be programmed reversibly by a voltage pulse to be high or low. Resistance switching has been reported for a wide variety of materials, including oxides, [94] molecular semiconductors such as pentacene, [46] anthracene, [45] copper-tetracyano-quinodimethane (Cu TCNQ), [95] blends of organic materials [96-98] and molecular materials doped with nanoparticles. [16, 62, 99] Semiconducting polymers have also been investigated. [36, 64] A promising one consists of a thin semiconducting organic film sandwiched between two metal electrodes, one of which is aluminium covered by a native- or thicker oxide. Although, it is becoming accepted that the oxide layer is required to achieve resistive switching, [21, 100] recent evidence [101, 102] shows that the polymer also plays a crucial role by providing an electron trapped charge layer at the polymer/oxide interface. This charge layer enhances tunneling across the oxide and tunes the formation of electrically bistable defects. In addition, the distributed series resistance of the polymer prevents thermal runway when a local defect (filament) switches on. Polymer/oxide diodes are then expected to provide not only better control of the RRAM properties but also superior endurance compared to oxide-only based memristors. Furthermore, polymer/oxide memories can be printed and integrated into complex, large area organic based circuits.

Polymer/oxide based memories show typical JV characteristics with a NDR. As early as 1967 Simmons and Verderber [16] studied the behaviour of NDR dynamics in SiOx memories using a triangular bias sweep profile. A peculiar, counter-intuitive behaviour was observed: upon increasing the voltage scan rate, both the current and magnitude of the NDR gradually decreased, the latter even disappeared completely. Here we characterize a similar temporal behaviour reported for Al_2O_3/polymer memories by Verbakel et al. [91] and reproduced here. Drawing upon the results of additional experimental measurements combined with simple theoretical considerations of processes occurring in these bi-layer structures, we arrive at a model

which provides a basis for explaining this apparently strange dynamic behaviour of bi-layer resistive switches, including the delay time and wide range of reported switching speeds.

This contribution is organized as follows. Firstly, we consider the dynamic behaviour of the HRS and show that it is readily predicted by a two-layer capacitor model reflecting the device structure. The transient response of the LRS is then explored in detail and the findings coupled with simulations based on the two-layer capacitor model to explain the anomalous behaviour observed on increasing the voltage ramp speed. Finally, the implications of our findings for the optimization of switching speed in such devices are discussed.

3.2. Experimental

The diode structure (Figure 3.1(a)) consisted of an Al bottom electrode, a sputtered layer of Al_2O_3 (20 nm), a spirofluorene polymer (80 nm), and a Ba/Al (5 nm/100 nm) top electrode which forms an ohmic, electron injecting contact to the polymer. The devices, with an active area of 9 mm^2, were encapsulated to exclude O_2 and H_2O. In all cases, the polarity of the applied voltage refers to that applied to the bottom Al electrode. Quasi-static J–V curves were obtained using a Keithley 487 picoammeter. The dynamic behaviour of the JV curves was recorded using the experimental arrangement in Figure 3.1(b) which comprised a signal generator and an oscilloscope combined with a low noise pre-amplifier. A photograph of an encapsulated device containing a number of diodes is shown in Figure 3.1(c). Device modelling was undertaken using the Advanced Design System (ADS) circuit simulator from Agilent.

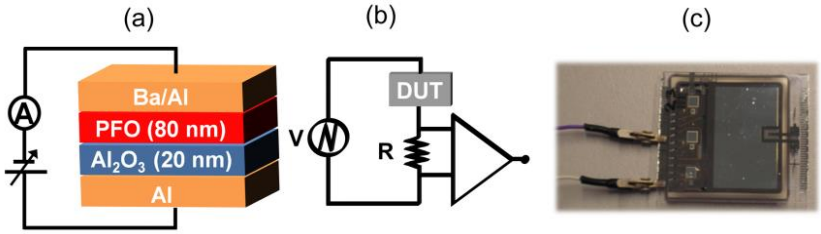


Figure 3.1 - (a) Diagram of the device cross-section and quasi-static measurement circuit. (b) The set-up to record JV curves at high voltage sweep rates. (c) A photograph of an encapsulated device containing a number of diodes

3.3. Results and Discussion

Pristine diodes were turned into programmable resistive switching memories by sweeping the voltage from 0 to 12 V. Following this electroforming process, the devices exhibited the usual NDR and bistable JV characteristics. Figure 3.2 shows that for the present diodes the NDR consists of a single or possibly a few switching events. The memory can be switched between HRS and LRS by applying voltage pulses with amplitudes corresponding to the top and bottom of the NDR in Figure 3.2, i.e. at about 5-6 V and 8-10 V, respectively. In the following, we investigate separately the dynamics of the device current response in both these memory states.

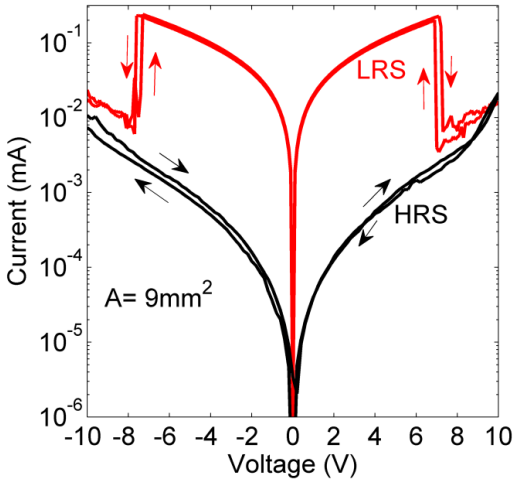


Figure 3.2 - JV characteristics in the LRS and HRS of an Al_2O_3/polyspirofluorene bistable resistive switching diode. The memory was electroformed at 12 V.

3.3.1. Transient response of the HRS

Figure 3.3(a) shows the experimental JV characteristics for the HRS obtained with increasing voltage scan speeds. We have already shown [100] that these two-layer devices can be modelled using the series-parallel combination of resistors and capacitors shown in Figure 3.3(b). The response of such a circuit to a ramp voltage is readily deduced in Chapter 2. Thus, assuming that $V_a=V_m.t/t_m$ where V_a is the voltage applied at time t, V_m and t_m the maximum amplitude and duration respectively of the ramp, the JV characteristic can be determined analytically by solving the differential

equation that describes the instantaneous current density, J(t) through the device which is composed of a displacement current and a conduction current. Since current continuity must apply, J(t) may be determined by considering the current flow through either of the parallel RC elements. Choosing the current flow through the oxide, we may write:

$$J(t)=C_{OX}\frac{dV_{OX}(t)}{dt}+\frac{V_{OX}(t)}{R_{OX}} \tag{3.1}$$

Where $V_{OX}(t)$ is the voltage appearing across the oxide layer and is given by equation (3.2):

$$V_{OX}(t)=\frac{\beta}{\alpha}+\left(\frac{\alpha K-\beta}{\alpha^2}\right)(1-\exp-\alpha t) \tag{3.2}$$

Here, $\alpha=\frac{R_{POLY}+R_{OX}}{R_{POLY}R_{OX}(C_{POLY}+C_{OX})}$, $\beta=\frac{V_m}{t_m}\cdot\frac{1}{R_{POLY}(C_{POLY}+C_{OX})}$ and $K=\beta C_{POLY}R_{OX}$.

An excellent fit with experimental results is obtained for R_{POLY}=14.4 KΩ.cm^2, C_{POLY}=30 nF/cm^2, R_{OX}=11.7 MΩ.cm^2 and C_{OX}=300 nF/cm^2 with the oxide capacitance being confirmed in low-frequency measurements using an impedance analyser.

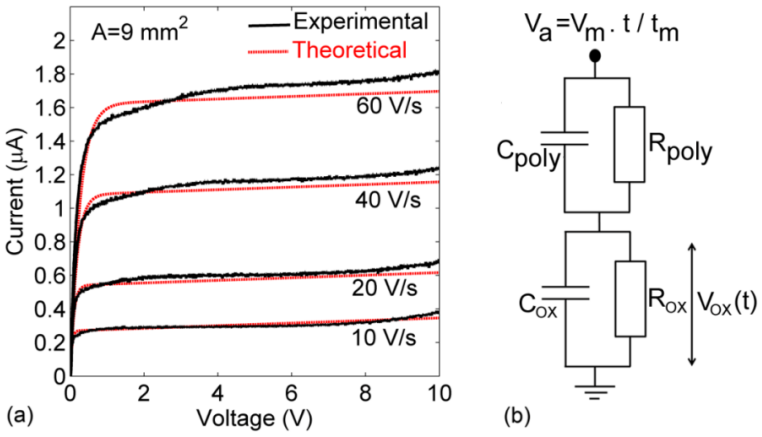


Figure 3.3 - (Colour online) (a) Experimental (black) and theoretical (red) JV characteristics of an Al_2O_3/polyspirofluorene (PFO) bistable resistive switching diode obtained in the HRS for different voltage sweep rates. (b) The circuit used for modeling the device. The values giving the best fit to experiment were R_{POLY}=14.4 KΩ.cm^2, C_{POLY}=30 nF/cm^2, R_{OX}=11.7 MΩ.cm^2 and C_{OX}=300 nF/cm^2. The memory was electroformed at 12 V.

3.3.2. Transient response in the LRS

We now turn to the LRS behaviour as exemplified by Figure 3.4. Here we see that, for increasing voltage scan speeds, both the device currents and the magnitude of the NDR gradually decrease: the latter disappears at a scan speed of 1000 V/s, in good agreement with literature reports. [16, 91] Furthermore, the NDR behaviour shifts to lower voltages upon increasing the scan speed.

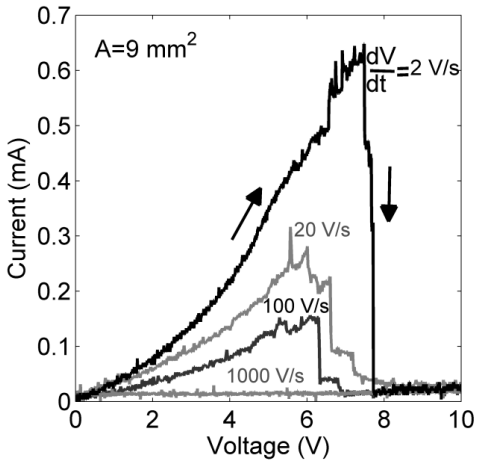


Figure 3.4 - Experimental JV characteristics of the LRS of an Al_2O_3 / polyspirofluorene memory as a function of scan speed. Both the onset voltage and magnitude of the NDR gradually decrease with increasing scan speed. At 1000 V/s the NDR is lost.

These results are counter-intuitive. As seen in Figure 3.3(a), increasing scan speeds should result in larger displacement currents. However, the LRS currents are orders of magnitude greater than the off-currents and, hence, dominate displacement currents. Nevertheless, we will argue that the internal capacitive structure of the device still plays an important role in the behaviour observed in Figure 3.4.

First we consider the nature of the on-current. We assume that the switching mechanism in these devices is physically located in the oxide layer and causes the opening and closing of micro-conducting paths across the oxide layer. A strong correlation has been established already between increased LRS currents and the appearance of local hot spots in the device. [21] We may assume, therefore, that the high LRS current flows through highly localised regions of the oxide and is likely to be filamentary in nature. [22] To represent the switching action of these local regions,

an additional parallel branch must be added to the equivalent RC network and is shown in Figure 3.5.

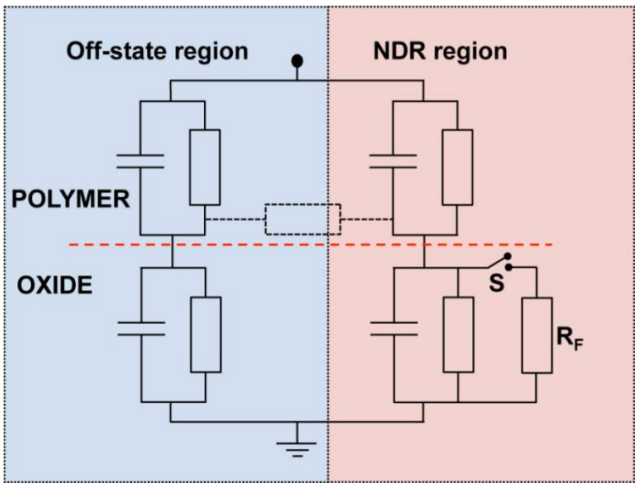


Figure 3.5 - Equivalent circuit representing a formed oxide/polymer diode in the LRS. The NDR branch is highly localised and connected to the formed (but HRS) region via the distributed resistance of the polymer layer represented by the dotted resistor. When the switch S is closed a conducting filament of resistance R_F shunts the normally high local oxide resistance.

The localised switching region leading to NDR is presumed to occupy an almost insignificant fraction of the total device area. It is, however, connected to the formed (but non-conducting) region by the distributed resistance of the polymer film which we represent here by the dotted resistance connection. The switch S represents the mechanism giving rise to the NDR. When closed it connects the resistance R_F into the circuit to simulate a highly conducting path (or filament). When S is open, the normal oxide resistance is connected to the circuit and the micro-filament turns off. In a real device a distribution of switches and corresponding low resistance paths exist.

Evidence for the existence of a distribution of such switches is provided by the noise measurements in Figure 3.6 undertaken on a device in the LRS. With a constant voltage applied, fluctuations are observed in the current. The inset in Figure 3.6 is an example for an applied voltage of 0.5 V. Here we see that a general increase in current occurs as a result of relatively low-frequency step changes on which are superimposed high-frequency RTN. The high frequency RTN noise can be attributed to the fast turning on and off of micro-filaments. On the other hand, the low-frequency steps correspond to the switching on and off of relatively long-lived conducting paths.

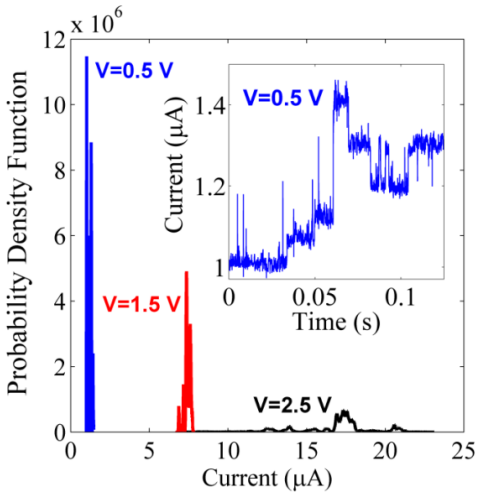


Figure 3.6 - Noise measurements for different voltages applied to a diode in the LRS presented as a probability density function (PDF). As the voltage increases, the PDF shifts to higher currents, the number of transitions reduces but their distribution becomes broader. The inset shows that for a constant applied voltage, in this case 0.5 V, the increasing current is composed of RTN superimposed on low-frequency micro-switching events.

In Figure 3.6 both on and off current steps are represented using their probability density function (PDF). With increasing bias voltage, the PDF shifts to markedly higher currents and becomes broader, suggesting that at higher voltages a smaller number of highly conducting filaments are active, albeit of broader distribution.

The magnitude of the applied bias also determines the time required for a device in the HRS to be turned on, as shown in Figure 3.7 where current is plotted as a function of time following the application of a step voltage.

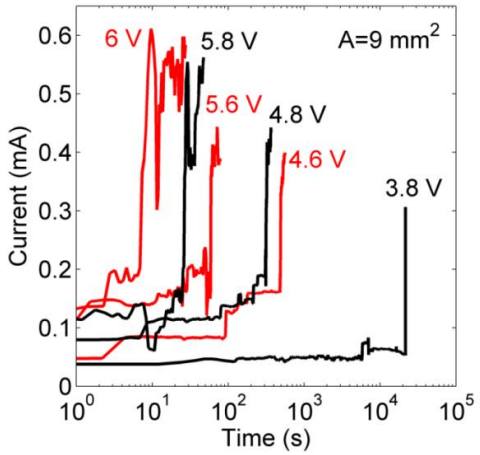


Figure 3.7 - Temporal evolution of current from the off- to LRS after applying voltage steps of different magnitudes. The experiment started from high to low bias.

In this experiment, a high voltage (6 V) near the NDR region was first applied. The voltage was then reduced to zero for 3-5 minutes before applying a step of lower amplitude. This procedure was repeated with gradually reducing voltage steps down to 3.8 V. As seen, switching does not occur immediately upon applying the voltage. A so-called delay time, t_d, must elapse after voltage application before switching occurs. Furthermore, the lower the applied voltage, the longer the delay time before switching occurs; a phenomenon also reported by Wang et al. [103]

In Figure 3.8 we show that the delay time, t_d, follows an exponential dependence on applied voltage according to the equation:

$$t_d = t_0 \exp(\gamma V_a) \tag{3.3}$$

Where t_0 is a constant and γ a voltage acceleration factor. A good fit to the data is obtained for $t_0 = 4.77\times10^9$ s and $\gamma = 3.37$.

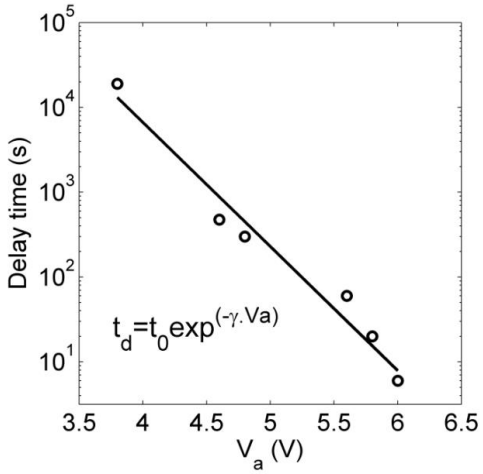


Figure 3.8 - Voltage dependence of the delay time for switching from off to on.

Interestingly, the functional dependence of t_d on applied voltage is similar to that observed for the time-to-dielectric-breakdown observed in thin films such as SiO_2 since the late 1970s [104] with γ ~7.5 for 5 nm thick films but asymptoting to lower values for thicker films. [105] This similarity suggests that the mechanism causing a change in the resistive state in an oxide-based RRAM is likely to arise from a breakdown mechanism ameliorated by the limiting resistance of the polymer layer i.e. a form of soft breakdown.

The results in Figure 3.8 clearly show that the magnitude of the applied voltage and the time for which it is applied play a crucial role in the switching process. It is important, then, to investigate the growth of the voltage, V_{ox}, dropped across the oxide layer for different applied voltage scan rates. This we may readily achieve using our double RC network and equation (3.2). The results are given in Figure 3.9.

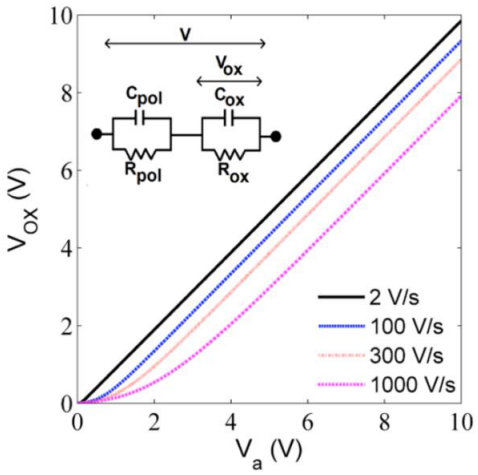


Figure 3.9 - The voltage dropped across the oxide layer, V_{ox}, plotted as a function of the applied voltage, V_a, for different voltage ramp rates. The calculations were based on the equivalent double RC network shown in the inset with the following parameters: R_{POLY}=14.4 KΩ.cm^2, C_{POLY}=30 nF/cm^2, R_{OX}=11.7 MΩ.cm^2 and C_{OX}=300 nF/cm^2.

In Figure 3.9, we used the Agilent ADS tool to simulate the response of the circuit utilising the resistance and capacitance values determined from the fit to the data in Figure 3.3(a). Not surprisingly, we note that V_{ox} lags increasingly further behind the applied voltage as the scan rate increases. At 2 V/s the voltage across the oxide reaches a maximum of 9.86 V when the applied voltage is 10V i.e. V_{ox} is practically the same as the external bias voltage. At 100 and 300 V/s, V_{ox} reaches 9.3 and 8.86 V respectively. As the scan rate increases to 1000 V /s now only 8 V appears across the oxide. It is clear, therefore, that increasing ramp speed reduces the fraction of the applied voltage appearing across the oxide. According to Figure 3.7, the time required for the RRAM to switch to an LRS increases exponentially with decreasing voltage. This imposes a limitation, therefore, on the ability to switch. Some of the conducting micro-paths, once switched-off (in a previous scan) will not recover during the subsequent faster voltage ramp because the lower V_{ox} attained does not remain applied for a sufficiently long time to effect turn-on. In a real material, local

differences in chemical structure, stoichiometry, defect density, morphology and film thickness will create numerous micro-switching regions resulting in a wide distribution of turn-on voltages and turn-on times. Reported switching times vary by orders of magnitude with values ranging from nanoseconds to milliseconds. [17, 41, 52, 63, 66, 106, 107] As seen in Figure 3.6, once programmed into the LRS, even low voltages trigger switching in low current capacity filaments, but still show a delay before the maximum current is achieved. Even in these more complex situations, by controlling the growth of V_{ox}, the internal device capacitances and resistances will determine which, and how many, local filaments switch on at a particular value of the applied voltage.

We now apply the above argument to the results in Figure 3.4. At very low voltage scan rates, V_{ox} follows closely the applied voltage so that a large number of micro-switches will be triggered, composed of a wide distribution of current carrying capacity (Figure 3.6). As the scan rate increases, the maximum V_{ox} attained decreases so that fewer switches, characterised by decreasing current magnitudes, will be activated. At sufficiently high scan rates, only low-voltage, low current switches will be activated so that the overall device current becomes dominated by the displacement current corresponding to the device in the HRS as observed in Figure 3.3(a). The model predicts that by sweeping the applied voltage to higher values, switching and NDR should be recovered and indeed this is the case. Figure 3.10 shows experimental JV characteristics obtained for a second diode at a constant ramp speed of 1000 V/s and recorded for increasing maximum applied voltages of 8, 9, 12 and 13.5 V.

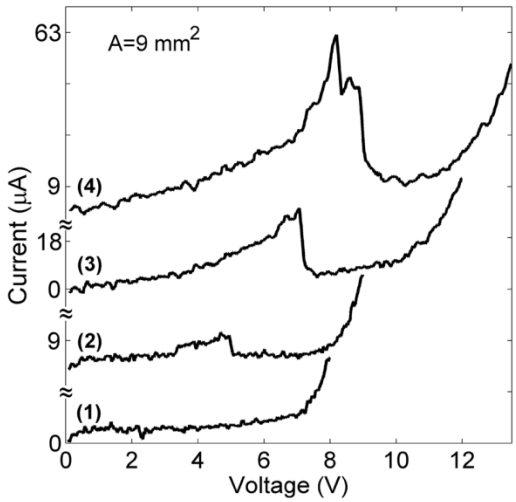


Figure 3.10 - LRS JV characteristics recorded at a fixed scan speed of 1000 V/s, with increasing external bias.

The NDR cannot be detected at 8 V, but is partially restored at 9 V and 12 V, and in the final sweep up to 13.5 V is clearly established. Hence, even at high scan speeds, the NDR and the ability to switch can be restored by successive voltage scans and enhanced as the maximum applied voltage increases. This suggests that the NDR observed in a particular curve must represent a cumulative response to the previous voltage sweeps. Such behaviour is consistent with the accumulation during each sweep, and therefore over time, of a long-lived interfacial trapped charge. [102]

3.3.3. Hot-spots and the NDR

Hot-spots are localised regions of high temperature associated with filamentary, LRS conduction in polymer/oxide RRAMs. [21] Any model for switching in these devices must also account for the lateral expansion of these spots as device current increases. The phenomenon is exemplified in the sequence of infra-red images in Figure 3.11 showing how two, isolated hot-spots expand and eventually merge as the bias voltage increases. While undoubtedly making a contribution, thermal diffusion laterally along such thin films is unlikely to extend several hundred microns away from a single conducting channel. Additionally, any model must explain the shift in the onset of NDR to higher voltages as the LRS current increases (Figure 3.4 and Figure 3.10).

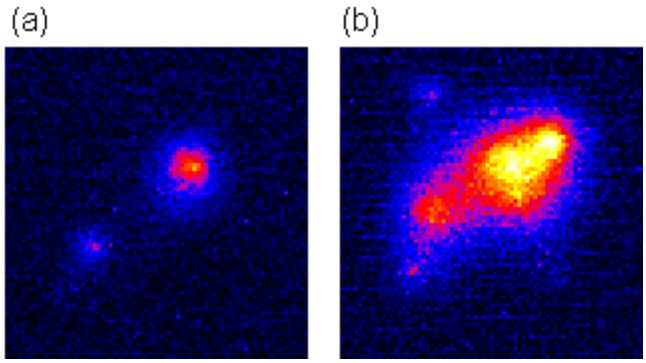


Figure 3.11 - Sequence of infra-red images showing two hot-spot regions in close proximity merging together into a single extended region as the applied voltage increases

3.3.4. Scan-rate dependence of the NDR region

In Figure 3.4, in addition to reducing the device current, higher scan rates also shift the NDR region to lower voltages. Previously, we have shown that during the electroforming process [102] deeply trapped electrons accumulate at the oxide/polymer interface. Interfacial electron trapping would also explain the cumulative effect of successive voltage sweeps in Figure 3.10. There is considerable evidence amassing in reports by us [91, 100-102, 108] and others, [109] suggesting that the RRAM switches to a high conductive state when the defects in the oxide, probably oxygen vacancies, are filled with positive charges. When a percolation path of such defects becomes established across the oxide, a conductive filament is created. Positive charge trapped in the oxide is compensated by the electrons trapped at the polymer/oxide interface thus establishing a dipole layer. The resultant high electric field across the oxide primes the conduction path so that when a critical voltage is reached, electron tunnelling occurs through the defect.

In the NDR region, the switching off of conducting filaments is accompanied by an electroluminescence burst of blue light. [110] This is indicative of recombination, presumably of electrons from the polymer with holes trapped in defect centres in the oxide. Recombination will empty the oxide traps and the conductive path will switch off. Since the potential drop across a highly conductive filament will be low, we argue that recombination and hence the onset of NDR is controlled by the magnitude of the current flowing through the filament.

It is instructive at this point to investigate the changes in potential distribution and current flow patterns in the diode in the vicinity of a conducting filament. This was achieved using the COMSOL Multiphysics simulator.

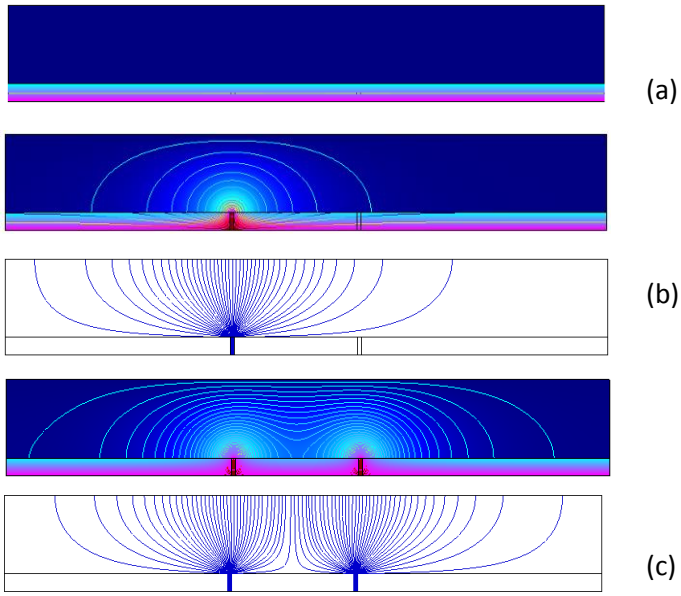


Figure 3.12 - (Colour online) COMSOL simulations showing potential distributions represented both in color (blue = -10V, pink = 0V) and by superimposed contour lines (a), (b), (d) and current streamlines (c) and (e) in our 2-layer capacitor model. The upper layer represents the polymer, the lower a thin oxide film. (a) Potential distribution in a device in the HRS. The corresponding current streamlines will be vertical and of low density. The changes in potential distribution and current streamlines arising from a single conducting filament in the oxide are shown in (b) and (c). The corresponding distributions for two adjacent filaments are given in (d) and (e).

In Figure 3.12 the device is represented by a simple two-layer structure composed of a thin, high resistivity oxide layer supporting a thicker, more conductive polymer layer. The colour (online) maps represent the potential distributions (blue = -10V, pink = 0V) which are further emphasized by superimposed contour lines. In (a) the device is in the HRS, leakage current through the oxide is minimal so that virtually all the applied voltage appears across the oxide layer owing to the higher conductivity of the polymer. Next we include a conducting filament in the oxide. This results in significant changes in the local potential (b) and in the current density profile (c). We note two important changes:

(i) The potential at the polymer/oxide interface decreases giving rise to lateral electric fields and extensive distortion of the potential in both the polymer and oxide layers.

(ii) The current tunnels through the polymer into the filament from a circular area of the electrode whose radius exceeds the polymer film thickness.

In the case of low on-currents, conducting filaments are isolated and well-separated. The non-uniform potential distribution (Figure 3.12(b) and (c)) allows electrons to be drawn through the polymer from a relatively large area of the electrode. The critical filament current required to effect efficient recombination and turn off the filaments is achieved at relatively low voltages.

For high on-currents, a large number of conducting paths are turned on, many in the neighbourhood of an originating filament as discussed above. As seen in Figure 3.12(d) and (e) the electrode area from which electrons are drawn does not increase in proportion to the number of neighbouring filaments. Higher voltages will be required then to provide the critical electron current through the polymer for extinguishing these filaments. Consequently, within a volume extending out from the filament into the polymer, considerable Joule heating will occur. Significantly, it is well known that the electrical breakdown strength of most insulating materials decreases with increasing temperature: a relevant example is soft breakdown in SiO_2 films a few nanometres thick. [111, 112] We postulate that as the applied bias increases, a combination of increasing oxide field and high temperature in the vicinity of the conducting filament triggers the switching of a nearby filament. Figure 3.12(d) and (e) shows that the region of disturbed potential and high current density now expands triggering further switching. This process is expected to continue until two local hot-spots overlap as in Figure 3.11 or expansion becomes limited by the process(es) leading to the NDR. Even if further filamentary conduction is not initiated, additional thermally induced currents will flow in both the polymer and oxide leading to a similar expansion of the hot-spot.

3.3.5. Implication for device design

An important outcome of the above findings is that the fundamental limitations on the speed of operation of the RRAM are the time- and voltage-dependences of the switch-on mechanism and not the switch-off process. The physical mechanism behind this limitation is not yet clear. However, we have demonstrated above that the switch-on time is degraded by the internal capacitive structure of the device. The switch-on time can be reduced, therefore, by decreasing the intrinsic relaxation time of the device. This in turn will reduce the rise time for the growth of V_{ox}, the voltage across

the oxide layer and may be achieved by minimising both the oxide capacitance and the polymer resistance. However, careful optimization will be required.

3.4. Conclusion

Non-volatile, bistable resistive memories have been fabricated in the form of Al_2O_3/polymer diodes. In quasi-static measurements the diodes display the well-reported negative differential resistance behaviour and are readily switched reversibly between the high and low resistive states. The responses of these diodes have been probed in both the HRS and LRS using triangular voltage profiles with different scan rates. We have shown that the HRS response follows closely the predictions based on a classical, two-layer capacitor description of the device. Using this model, we have further shown that, at high voltage scan rates, the rate of rise of the voltage appearing across the oxide layer lags significantly behind the applied voltage. When coupled to the experimental finding that, switching events are characterised by a delay time determined by the magnitude of the applied voltage, the seemingly anomalous observation that the device current decreases with increasing voltage scan rate is readily explained.

Simple electrostatic simulations confirm that major changes occur in potential distribution and current flow patterns in the vicinity of an isolated conducting filament in the oxide. Assuming that a critical current must be achieved to turn off a conducting filament, we tentatively suggest that such changes in potential distribution are responsible for the shift in the onset of NDR to lower voltages as the number of conducting filaments decreases as occurs, for example, when the voltage scan rate increases.

Anomalous temperature dependence of the current in metal-oxide polymer resistive RAMs

Metal-oxide polymer diodes exhibit non-volatile resistive switching. The current–voltage characteristics have been studied as a function of temperature. The HRS follows a thermally activated behaviour. The LRS shows a multistep-like behaviour and below 300 K an enormous positive temperature coefficient. This anomalous behaviour contradicts the widely held view that switching is due to filaments that are formed reversibly by the diffusion of metal atoms. Instead, these findings together with small-signal impedance measurements indicate that creation and annihilation of filaments is controlled by filling of shallow traps localized in the oxide or at the oxide/polymer interface.

4. Anomalous temperature dependence of the current in metal-oxide polymer resistive RAM

4.1. Introduction

Resistive switching has been observed in MIM diodes for a wide variety of insulator such as oxides, nanoparticles, organic or inorganic semiconductors, and currently attracts attention for application in future non-volatile memories. [36] It has been recently shown that functional memories can be obtained by inserting a thin oxide layer into a polymer diode. [113] A yield of switching diodes of almost unity has been reported. Switching is a generic property of metal-oxides, [9, 114-116] the polymer only acts as a current limiting series resistance. [100] The memory is formed by applying a high bias pulse to the pristine diode. After this so-called forming process, attributable to soft breakdown of the oxide, [113] the memory can be switched reversibly between a LRS and a HRS. Thermal imaging has shown that the conduction in the LRS is filamentary in nature. [21] At present, the nature and formation of these filaments is not clear. Several models for the switching have been proposed such as metal filaments that rupture locally by joule heating, [19, 117] or trap controlled tunneling between metal islands. [118]

In order to distinguish between these mechanisms, we focus on the temperature dependence of the current for an oxide-polymer switching device. The anomalous positive temperature coefficient (PTC) that we observe below 300 K, shows that more filaments become active when the device is cooled down. This observation contradicts explanations based on atomic diffusion. We argue that filaments switch on and off by filling and emptying of shallow trap states located in the oxide layer or at the polymer/oxide interface. This hypothesis is supported by small signal impedance measurements.

4.2. Experimental

The device studied in this chapter is described in the experimental part of Chapter 3.The IV curves were obtained using a Keithley 487 picoammeter voltage source and capacitance–frequency and capacitance–voltage (CV) curves were obtained using an Agilent 4192 impedance analyzer. Temperature dependent

measurements were carried out in a liquid helium cryostat (Advanced Research Systems, ARS - HC2).

4.3. Results and discussion

4.3.1. IV characteristics of the RRAM

The pristine devices were turned into programmable resistive switching memories by applying a 12 V voltage ramp as described previously. [16, 113] After forming, the devices exhibit the usual bistable JV characteristics and a NDR in the LRS, see Figure 4.1.

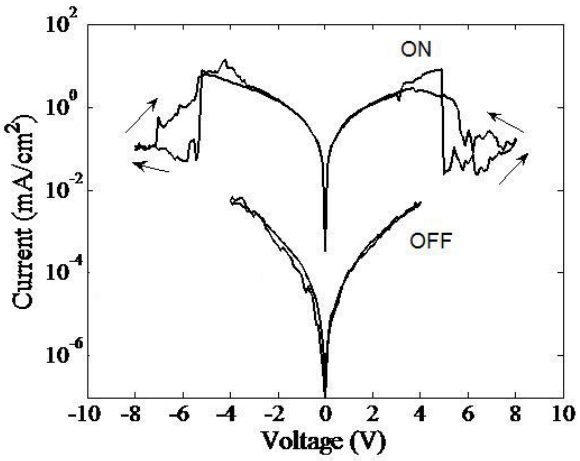


Figure 4.1 - JV characteristics of the device in the HRS and in the LRS.

At room temperature, the memory can be switched between HRS and LRS by applying voltage pulses with amplitudes corresponding to the top and bottom of the NDR, [17] here about 3-4 V and 6-8 V respectively.

4.3.2. Thermal behaviour in the HRS

A stable HRS is induced by applying high bias voltage for a long time, in the order of minutes. The time necessary to induce a switching to the LRS is now much longer than the time necessary to record a full JV curve. In agreement with literature, [46] the electrical current in the programmed HRS follows a thermally activated behaviour (see Figure 4.2).

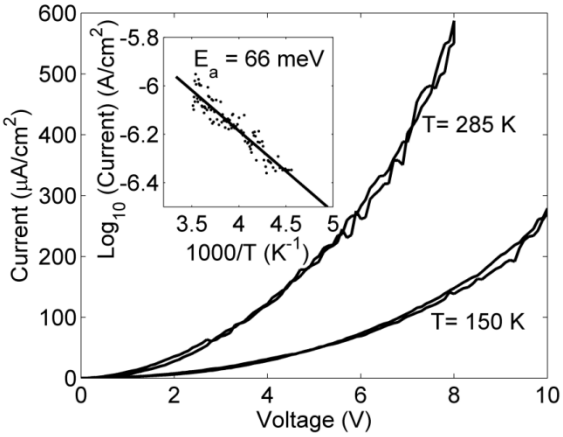


Figure 4.2 - Typical JV characteristics for the HRS. The inset shows the Arrhenius plot of the current measured at the voltage of 1 V.

The Arrhenius plot of the current measured at 1 V is shown in the inset; yielding activation energy of 66 meV for the temperature range of 280-200 K. Below 200 K, the current is not thermally activated.

4.3.3. Thermal behaviour in the LRS

Interestingly, the JV characteristics for the LRS show a large increase in the magitude of the current upon lowering the temperature of the diode. This behaviour is illustrated in Figure 4.3. The increase in current is more pronounced at higher bias voltage, in the voltage range below the sharp onset of the NDR. The lower the temperature the higher is the swicthing-off voltage. The physical mechanisms behind this shift in voltage are under study.

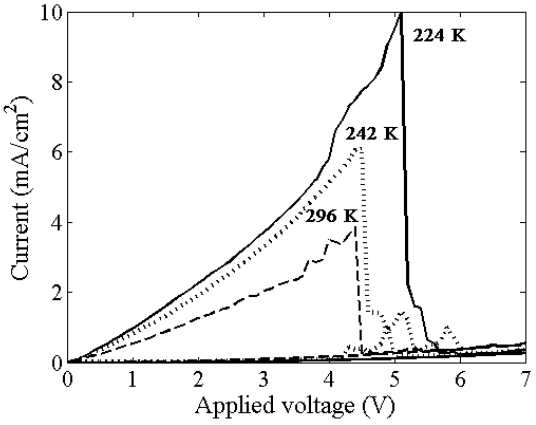


Figure 4.3 - Temperature dependence of the J –V curve of a diode programmed into the LRS.

To further explore this unusual temperature dependence, the diode was programmed into the LRS at room temperature and then cooled down while applying a continous bias voltage (2 V). The magnitude of the current becomes more than double in a temperature range of 150º C, see Figure 4.4. This corresponds to a PTC of the electrical resistivity, $\alpha \approx 0.01\ K^{-1}$, an anomalously large value when compared with typical values for metals ($\alpha = 0.0039\ K^{-1}$ for Cu). Furthermore, in contrast to the smooth decrease of the resistivity in metals, the resistivity of the diodes lowers in a step-like fashion upon cooling.

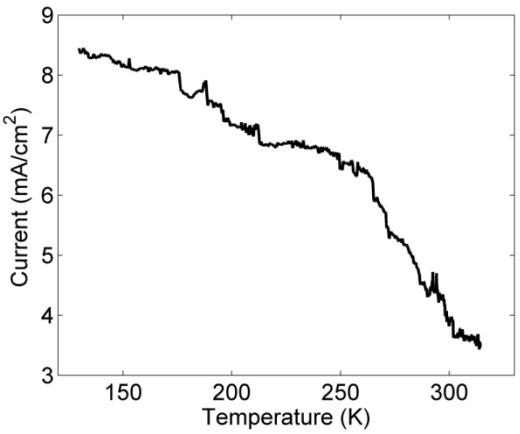


Figure 4.4 - The temperature dependence of the current in the high-conductance LRS monitored at 2V. The cooling speed is $1 K min^{-1}$.

The step-like nature of the rise in current strongly suggests that additional conducting filaments become active at low temperature. In order to check for self-heating effects during the experiments, we also carried it out in other sample cooling runs where the applied bias was temporarily removed for intervals of times ranging from a few seconds to minutes, allowing for thermal equilibration. During these times the current across the sample becomes zero. In these runs, a similar increase in conduction was observed as shown in Figure 4.5.

A small section of the curve is magnified to show that the rise in current is through small discrete events (see inset of Figure 4.5). Furthermore, the PTC of the current is independent of heating speed and direction of temperature ramping. Thus self-heating effects can be disregarded.

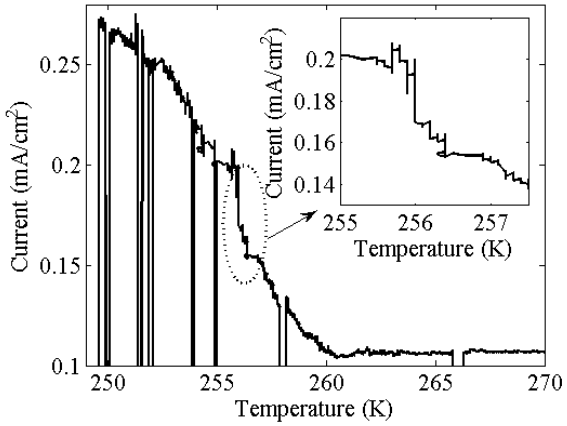


Figure 4.5 - The temperature dependence of the current in the LRS monitored at 1V in a similar sample to the one shown in Figure 4.4. In this cooling run the bias was temporarily removed for time intervals ranging from a few seconds to minutes, allowing for thermal equilibration. The cooling speed is 1 $Kmin^{-1}$. The inset shows the discrete nature of the current variation with temperature.

Small PTC effects were reported by others [46, 119, 120] and attributed to metallic filaments. The abnormally large PTC cannot be explained by a metallic type of conduction. The large and stepwise increase in current can be rationalized by the temperature dependence of trap occupancy. Here we assume that shallow trap sites around the Fermi level could control the activity of filaments. At room temperature they are depopulated by thermal emission. However, upon cooling the diode, the shallow traps will be gradually filled and activate filaments.

4.3.4. Small-signal impedance measurements

In order to test the reported hypothesis that these trap sites are located in the oxide, [19] we performed small-signal impedance measurements. Figure 4.6 shows the temperature dependence of the capacitance (C) and loss (G/ω) where G is the conductance and ω is the angular frequency.

The low-frequency capacitance remains constant. At low frequencies the loss is proportional to $1/\omega$, which implies a constant DC conductance. As shown in Figure 4.6, upon decreasing the temperature, the low-frequency conductance increases. This is in agreement with the PTC observed for the DC conductance as shown in Figure 4.4.

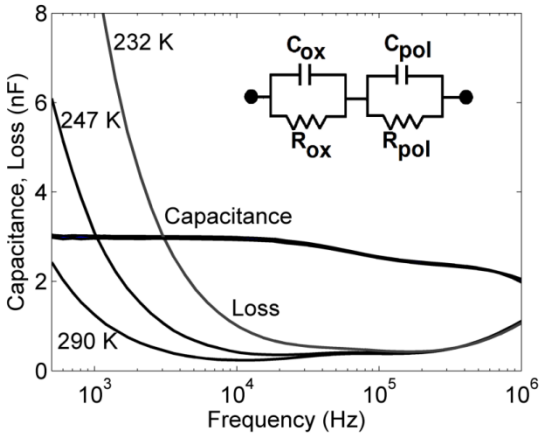


Figure 4.6 - Frequency dependence of the capacitance (C) and the loss (G/ω) in the LRS. The inset shows the corresponding equivalent circuit which describes the device as a double-layer structure.

The temperature dependence of the loss recorded with a signal test frequency of 300 Hz is shown in Figure 4.7. Similar to the DC measurements, the loss shows a discontinuous, step-like increase upon cooling.

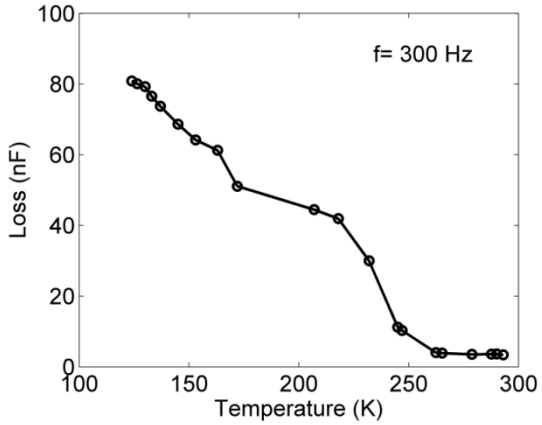


Figure 4.7 - Low-frequency loss (G/ω) of the diode as a function of temperature. Measurements were carried out at with a test frequency of 300 Hz. The solid line is a guide to eye.

In the previous work, [100] it has been shown that the frequency dependent response of the diode can be modeled as a double RC circuit represented in the inset of Figure 4.6. At low frequencies the response is determined by the properties of the oxide layer, while at higher frequencies the polymer layer dominates. This equivalent circuit was used to fit the loss curves recorded at different temperatures (shown in Figure 4.8).

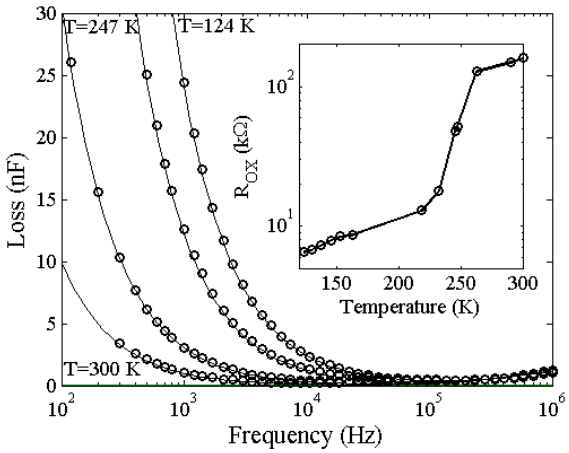


Figure 4.8 - Experimental measured loss (points) and theoretical fits (continuous lines) using the equivalent circuit of Figure 4.6. The changes are resistive and located in the oxide layer of the sample; only changes in R_{OX} are necessary to account for the changes in the loss with temperature. All other circuit parameters were kept constant. The inset shows the values of R_{OX} used to fit the loss at a particular temperature.

Since the measured capacitance does not change significantly with temperature, changes are mostly resistive and only located in the oxide layer (represented as R_{OX}). The dependence of R_{OX} with temperature as estimated from the equivalent circuit is shown in the inset of Figure 4.8. A decrease in R_{OX} from 160 kΩ (at 300 K) to 6.6 kΩ (at 124 K) is required to provide a good fit to the data. The increase in the loss at low frequencies indicates that the oxide conductance increases upon cooling. Therefore, the trap sites active in switching are located in the oxide or at the oxide polymer interface.

For these memory devices, the presence of shallow traps cannot be detected by small-signal impedance measurements because the large dc current across the sample masks the contribution of traps to the low-frequency capacitance.

Concerning the chemical nature of the trap sites, we mention the possibility of a water-related defect. This defect is known to contribute to temperature dependent changes in electrical properties at temperatures around 200 K, related to a phase transition. [121-123] The fact that both the dielectric loss and dc current do not change significantly near 200K suggests that the water-related traps do not contribute to the PTC effect. Furthermore, the PTC effect is still observed for temperatures as low as 130K which is well below 200 K, the temperature where the water-related defect becomes a trap for charge carriers. This strongly suggests that although water

related traps maybe be present, they are not responsible for the PTC effect reported here.

In order to get insight into the trap characteristics, thermally stimulated currents were also attempted. However, switching diodes show relatively noisy currents, which hinder the observation of the discernible structure in thermally stimulated currents.

4.4. Conclusions

We note that the commonly reported view that filaments are created by the diffusion of metallic species from the electrode into the bulk region cannot explain the abnormal positive temperature coefficient. Instead we argue that in the forming process conducting paths are pre-formed. Here diffusion of metal atoms can be involved, as indicated by a number of experiments. [115, 120, 124] However, this does not imply that every time the memory switches, a filament is formed or ruptured by diffusion of atoms. Instead, our findings support that preformed paths exist and that these are turned on and off by filling and emptying of trap states, acting as micro-switches. Equivalent circuit modelling shows that these micro-switches are physically located in or near the oxide layer.

Low-Frequency diffusion noise in Resistive-Switching Memories Based on Metal-Oxide Polymer Structure

Low-frequency noise is studied in resistive-switching memories based on metal–oxide polymer diodes. The noise spectral power follows a $1/f^{\gamma}$ behaviour, with $\gamma = 1$ in the ohmic region and with $\gamma = 3/2$ at high bias beyond the ohmic region. The exponent $\gamma=3/2$ is explained as noise caused by Brownian motion or diffusion of defects which induce fluctuations in diode current. The figure of merit to classify 1/f noise in thin films has an estimated value of 10^{-21} cm^2/Ω, which is typical for metals or doped semiconductors. This value in combination with the low diode current indicates that the 1/f noise is generated in the narrow localized regions in the polymer between the contacts. The analysis unambiguously shows that the current in bistable non-volatile memories is filamentary.

5. Low-Frequency diffusion noise in Resistive-Switching Memories Based on Metal-Oxide Polymer Structure

5.1. Introduction

Resistive switching in metal–oxide polymers has been intensively studied for RRAMs. Detailed characterization has been reported using a variety of methods. Filamentary conduction and low-frequency current fluctuations are often observed. [21, 100, 125] Although these experimental observations strongly suggest that electrical-noise-based techniques can provide insight into the localized conduction, surprisingly, few studies on noise in RRAMs have appeared. [125-127]

The 1/f noise as a fluctuation in the conductance has a power spectral density proportional to $1/f^{\gamma}$ with $0.9 < \gamma < 1.1$.

This behaviour is commonly observed in the frequency range [1 Hz, 100 kHz]. Low-frequency noise with a $1/f^{3/2}$ spectrum, random telegraph noise, and multilevel switching noise are considered as having a physical origin different with that of the 1/f noise. This frequency dependence is often attributed to diffusion-like processes. According to the general theory, [128] a large number of diffusion transport mechanisms give rise to $1/f^{3/2}$. Voss and Clarke found a $1/f^{3/2}$ spectrum due to number fluctuations of particles in Brownian motion. [129] The $1/f^{3/2}$ spectrum was also observed in a variety of metal–oxide related structures and attributed to transport noise associated with long-range diffusion of hydrogen impurities in metal films. [130-132]

Noise with $1/f^{3/2}$ was also reported for thin silver films subject to electromigration damage. [133] Here, the $1/f^{3/2}$ spectrum was attributed to long-range diffusion of atoms through pathways opened during electromigration.

In this paper, we study the noise characteristics of metal–oxide-polymer-based RRAMs as a function of the applied voltage. The noise is studied in both frequency and time domains. The findings provide evidence that, under a high bias, a diffusion mechanism is responsible for the noise.

5.2. Experimental

The device studied in this chapter is described in the experimental part of Chapter 3.The IV characteristic is measured with Agilent 4156C semiconductor parameter analyzer. The noise is observed in the frequency and time domains, through Agilent 35670A dynamic signal analyzer. Current noise measurements are made under a constant bias voltage through the internal bias supply of the Stanford model SR570 current amplifier. The noise spectra were analyzed with Agilent 35670A spectrum analyzer in three frequency spans, i.e., 512 Hz–102.4 kHz, 16 Hz–3.2 kHz, and 0.5–100 Hz, in order to present spectral values from 1 Hz up to 100 kHz.

5.3. Results and Discussion

5.3.1. IV characteristics of the RRAM

Pristine diodes were turned into programmable resistive switching memories by sweeping the voltage from 0 to 12 V. After this electroforming process, the devices exhibit bistable IV characteristics, a low-conductivity state, and a high-conductivity state. Figure 5.1 shows the corresponding IV characteristics.

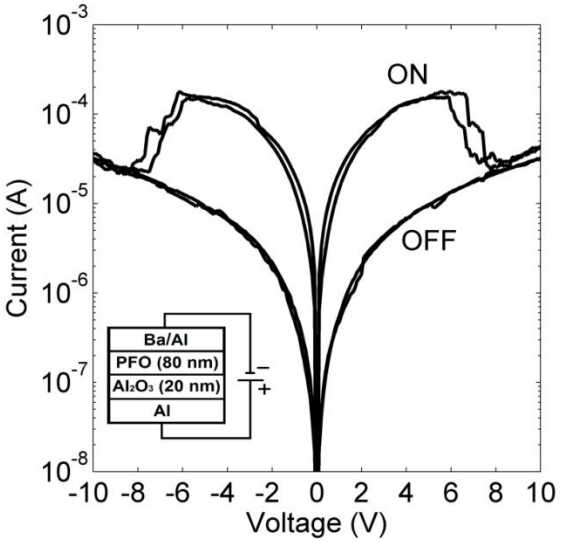


Figure 5.1 - IV characteristics in the LRS and HRS of an $Al/Al_2O_3/PFO/Ba/Al$ bistable resistive-switching diode. The inset shows the device structure

The LRS shows a region with NDR. It is assumed that the NDR region is caused by a cascade of switching-off events that turns off the high conductivity state

and the corresponding filamentary paths. The IV curve returns to the HRS (see Figure 5.1). The mechanism that causes the switching-off at high bias (V >6 V) remains elusive. The application of a bias slightly above the onset of the NDR regions will bring diode to the HRS, and the $1/f^{3/2}$ behaviour will not be observed.

The $1/f^{3/2}$ behaviour is observed clearly before the onset of the NDR. According to our view of the physical origin of the NDR, we would expect that, as the highly conducting paths are turned off, the $1/f^{3/2}$ behaviour will disappear. The memory is programmed between LRS and HRS with voltage pulses with amplitudes corresponding to the top and bottom of the NDR, which are about 2-5 and 8-10 V in Figure 5.1, respectively.

5.3.2. Definition of charge injection regimes

A detailed analysis of the LRS IV characteristics shows that, below 2 V, the charge carrier injection is ohmic and, above 2 V, it becomes Space Charge Limited (SCL), showing $I \propto V^m$, with $3/2 < m < 2$, [134, 135] as shown in Figure 5.2.

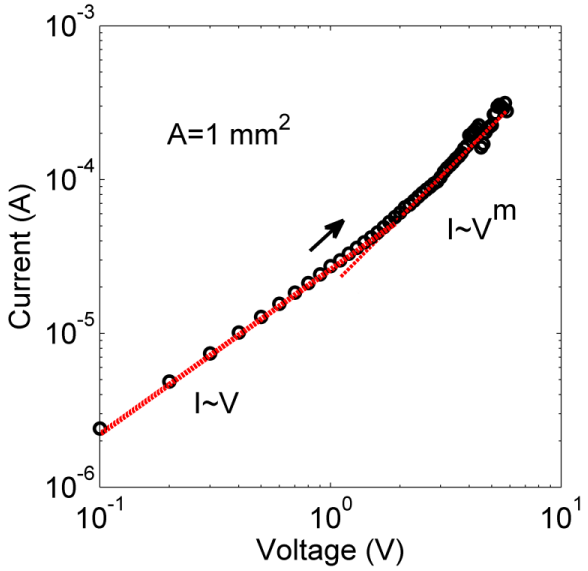


Figure 5.2 - LRS I–V characteristic represented in log–log plot showing the transition from ohmic to SCL transport

The noise behaviour of the current was measured for both conduction regimes, with the usual 1/f noise interpretation and application of the Hooge empirical relation. [136, 137]

5.3.3. 1/f noise measurements

Hooge's relation for the 1/f noise, the noise parameter $C_{1/f}$, and the figure of merit qαμ is given by the following equation, [138] for homogeneous samples submitted to homogeneous fields:

$$\frac{S_I}{I^2}=\frac{S_V}{V^2}=\frac{S_R}{R^2}=\frac{S_G}{G^2}=\frac{C_{\frac{1}{f}}}{f}=\frac{\alpha}{Nf}$$
$$C_{\frac{1}{f}}\equiv\frac{fS_I}{I^2}=\frac{\alpha}{N}=\alpha\frac{Rq\mu}{t^2}<=>C_{\frac{1}{f}}=\frac{q\alpha\mu}{t^2}R \quad (5.1)$$

Where, $C_{1/f}$ is the relative 1/f noise, S_I, S_V, S_R, S_G the current, voltage, resistance and conductance noise spectra respectively, N the number of free carriers, α the Hooge empirical parameter, q the elementary charge, t the contact thickness and R the device resistance.

Figure 5.3 shows spectra measured in the ohmic and the NDR region.

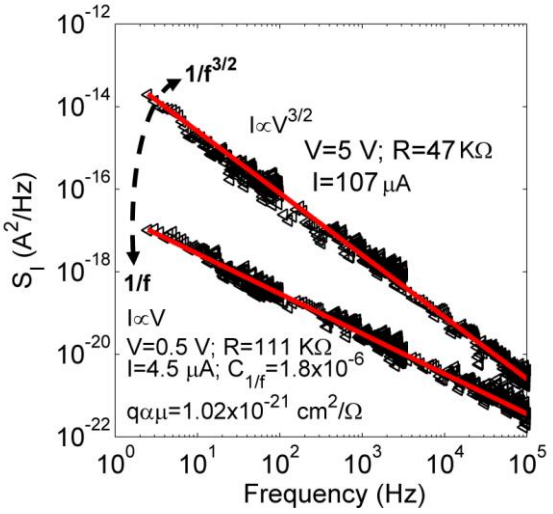


Figure 5.3 - Current noise spectrum in the transition from ohmic to SCL region, indicating a diffusion mechanism at higher bias.

For a bias of 0.5 V (ohmic region), the noise follows the 1/f dependence. The $C_{1/f}$ is extremely high (1.8×10^{-6}). Such high values are expected when the current is carried by a low number of free charge carriers, [136, 137] or due to the presence of nano-constrictions. [138, 139] When the diode is biased at 5 V (SCL region), the noise follows a $1\gamma/f^{3/2}$ dependence that is in close agreement with the results of Ostadal et al. in $Al/Al_2O_3/Au$ structures. [140] This noise is presumably originated in

a different physical process than the 1/f noise. Hence, a new physical mechanism becomes active at high bias just below the NDR region. Switching was also proposed as a new low-frequency noise source in high-temperature superconductors. [141] The influence on the noise from the diffusion of defects originating switching conducting spots in the Al_2O_3 contacts is dominant over the 1/f noise of the polymer that becomes proportional to $I^{3/2}$ instead of I^2 at low bias. [125] The qαμ value is often used as a figure of merit to compare and classify 1/f noise in thin films. [125, 142, 143] For the ohmic region, we calculated the coefficient qαμ by using the polymer thickness $t=80\times10^{-7}$ cm in (1); this results in $q\alpha\mu = 1.02 \times 10^{-21}$ cm^2/Ω. This value is equivalent to $q\alpha\mu = 5\times10^{-21}$ cm^2/Ω in [125] and is typical for semiconductors, metals, or polysilicon (10^{-21} cm^2/Ω). [142, 143] Switching-on and switching-off of new channels at high bias are a diffusion process (switch fluctuator) at the Al_2O_3 contact. That process dominates the 1/f spectrum and the observed slope of the spectrum ($1/f^{3/2}$). The 1/f noise in the tunnel current through thin AlxOy layers is often from another variety. [142]

Analysis of the current level (3×10^{-4} A) at a bias of 5 V in view of the Mott–Gurney law is given by the following equation with values $\mu = 10^{-8}$ $m^2/V\cdot s$, $\varepsilon_0\varepsilon_r = 1.6\times10^{-11}$ F/m, and t = 80 nm as in [125]:

$$I = \frac{9}{8}\frac{S\varepsilon_0\varepsilon_r\mu}{t^3}V^2 \qquad (5.2)$$

Where $\varepsilon_0\varepsilon_r$ represents the polymer permittivity, t is the polymer thickness, μ is the mobility, S is the effective area, and V is the critical voltage. The effective estimated area ($\approx 10^{-8}$ m^2) is much lower than the real device area (10^{-6} m^2). This strongly suggests that the noise is generated in a small fraction of the polymer sandwiched between a perfect contact and some conducting spots at the Al_xO_y contact. This view is supported by other studies which show that conduction is filamentary and only a fraction of the device carries current. [21, 100]

5.3.4. Probability Density Function (PDF) measurements

The noise was also measured in the time domain. Figure 5.4 shows the probability density function (pdf) for (a) 1 and (b) 5 V.

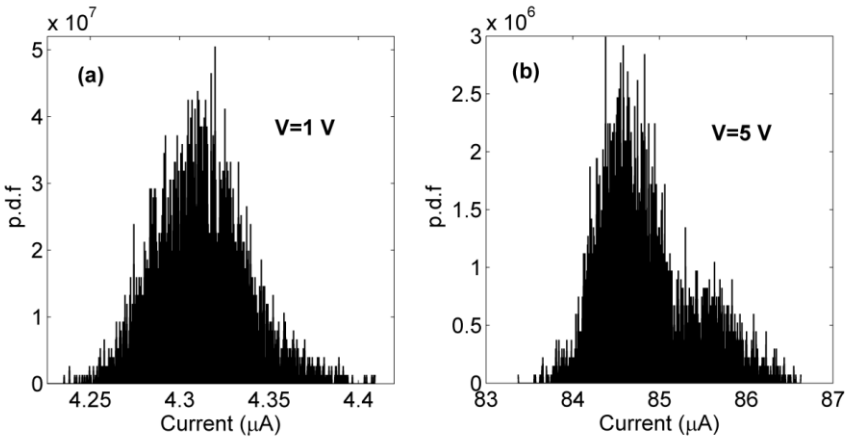


Figure 5.4 – Probability Density Function (PDF) of the RRAM with (a) 1 and (b) 5 V applied

In the ohmic region, the noise exhibits a typical Gaussian response. Figure 5.5 shows that, as the bias increases, the full width at half-maximum (FWHM) widens, and at 5 V, the noise becomes non-Gaussian, as shown in Figure 5.4(b).

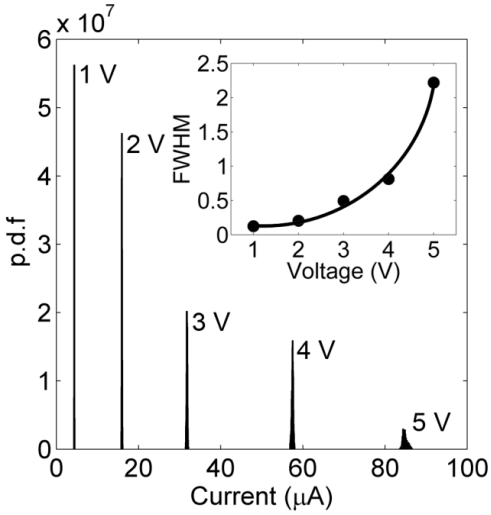


Figure 5.5 - PDF representation with different biases. The inset shows the FWHM of the Gaussian p.d.f. for each different bias.

The inset of Figure 5.5 shows that FWHM increases rapidly above 3 V. Widening of FWHM can be seen as indication that more conducting paths become active at higher bias. Indeed, as the bias approaches the top of the NDR region, the system can develop multilevel switching which shows as RTN noise.

From a physical point of view, the signature of the noise described previously is consistent with a localized conduction in narrow regions of the Al_2O_3 layer. These

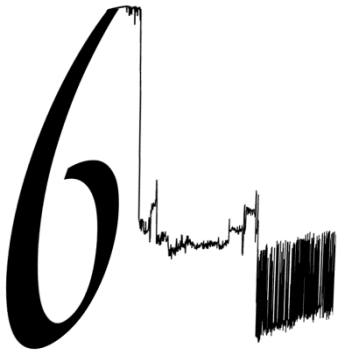
local conducting regions can be established by some microscopic diffusion of defects. The fact that the noise follows a $1/f^{3/2}$ behaviour supports this view.

The chemical nature of the oxide defects is still a matter of debate. Oxygen-vacancy migration is becoming a popular model to explain the formation of conducting paths through the oxide layer. [143, 144] Nian et al., [144] proposed that the resistance change in $Ag/Pr_{0.7}Ca_{0.3}MnO_3/Pt$ heterostructures is proportional to the concentration of oxygen vacancies. The authors also compared the resistance relaxation behaviour of their samples with the oxygen diffusion in $Bi_2Sr_2CaCu_2O_{8+\delta}$ samples. [143] The conclusion was that switching is related to the stack of oxygen vacancies near the metal electrodes. Quintero et al. [145] reported that the resistive switching in $silver/Pr_yLa_{0.375-y}Ca_{0.325}MnO_3/silver$ shows a maximum at a certain low temperature. The data were interpreted in terms of an oxygen content dependence with temperature. This observation was in agreement with the anomalous temperature behaviour reported by Gomes et al. [108]

5.4. Conclusions

The noise behaviour of resistive switching memories was studied. For the conducting state at high bias, where NDR can occur, the noise shows $1/f^{3/2}$ frequency dependence. This is normally assigned to a diffusion process. This supports the view that the migration of oxygen vacancies promotes the establishment of local conducting spots over the oxide layer in contact with the Al bottom contact. Under high biases, Brownian motion may induce microscopic fluctuations in the conducting paths with corresponding fluctuations in diode current. The noise becomes non-Gaussian and approaches to a RTN type of noise.

The analysis of the relative noise intensity revels the estimated figure of merit, $q\alpha\mu=10^{-21}$ cm^2/Ω, which is typical for conducting materials such a metals or doped semiconductors. The low current levels in the device and the value for $q\alpha\mu$ support the view, that the regions responsible for current and noise must be narrow localized regions in the polymer with a common perfect contact and separated conducting contact spots at the AlxOy oxide layer.



Characterization of filamentary current paths in metal-oxide-polymer resistive switching memories

The non-homogeneous electrical conduction of metal-oxide-polymer memristors is presented. The conduction is created though filaments during an electroforming process. These filaments are turned on and off like switches by an electronic process. The size and current density transported by the filaments is estimated using a combination of low-frequency capacitance and current measurements. Small filaments transport current as low as 3.75 mA/cm^2 and they switch on and off at frequencies as high as a few kHz at room temperature.

The current is limited by the polymer layer. Bias and temperature dependence of the switching rate confirms that the filaments are not metallic. Furthermore, it is shown that the filaments are not randomly distributed in size but that there is a network of identical filaments.

The switching rate of the filaments is controlled by the free electron concentration in the polymer layer. A recombination mechanism is proposed for turning off the filaments and charge, trapping in the oxide for the turning on mechanism.

6. Characterization of filamentary current paths in metal-oxide-polymer resistive switching memories

6.1. Introduction

It is extensively accepted that the current in memristor devices is not homogeneous but transported through localized paths or filaments. This view is supported by a significant amount of evidence. A simple example is the observation of hot regions using spatial resolved thermal images. [21] A second indirect approach is the relationship between device area and resistance. Usually the LRS current conduction is localized without area dependence. [100, 146, 147] A third one is the temperature dependence of the current; some authors reported resistance versus temperature curves showing metallic-like conduction when the memory is in the LRS. [108, 148, 149] Electrical noise measurements also show behaviour typical of high conducting materials such as metals and doped semiconductors. This behaviour in combination with the low current density through the device suggests that the regions responsible for current transport and electrical noise are narrow filaments between the contacts. [22]

Other techniques for identifying filaments are based on high-resolution microscopy techniques. Filamentary current paths have been confirmed by local conducting Atomic force microscopy (LC-AFM) in resistive memories based on BFO, [150] TiO2, [151] ZnO [152] and NiO [153] thin films. Electrostatic force microscopy (EFM) and Kelvin probe microscopy (KPM) were also used and have been recently reviewed by Lee et al. [154] High resolution transmission electron microscopy (TEM) images provide images of filaments and information about micro structural changes. Energy dispersive X-Ray (EDX) spectroscopy and electron energy-loss spectroscopy (EELS) measurements were used to confirm the composition of the filaments.

The nature of filaments varies according to the type of material and type of resistive switching. In bipolar type of switching, the mechanism consists in the formation and dissolution of metallic filaments, the so-called fuse-antifuse mechanism. [114] In oxides where typically the type of switching is unipolar, filaments are not metallic but comprised of oxygen vacancies paths. The prevalent view is that these conducting paths are created only once during an early

electroforming process. Upon resistive switching, filaments are neither generated nor destroyed by the diffusion of atoms, but instead individual filaments are turned on and off, like switches. The switching mechanism is electronic. This view is corroborated by infrared images that shows the same original hot spot distribution as the memory turns on and off many times. The study of the anomalous temperature dependence of the LRS also reveals that, upon lowering the temperature, the conduction increases in a step-like fashion. Furthermore, the positive temperature coefficient of the electrical resistivity of about 0.01 K^{-1}, an anomalously large value when compared to typical values of metals, such as 0.0039 K^{-1} for Cu. This behaviour could only be explained on the basis of a trap assisted mechanism that controls the density of active filaments. [108]

Filamentary conduction is also responsible for the observation of RTN. This noise is due to the relatively fast switching on and off of filaments which causes discrete current fluctuations.

In this contribution the small discrete current fluctuations are analysed in detail. Basically, two types of filaments are described: long-lived filaments responsible for the non-volatile memory properties and short-lived, or flicker filaments, responsible for the noise behaviour of the memristor. The long-lived paths were studied using a combination of quasi-static IV characteristics and small-signal impedance techniques. Flicker filaments give rise to high frequency RTN and, therefore, were studied using electrical noise-based techniques. Both types of filaments share a common physical origin. Flicker filaments affect the memory reproducibility and scalability.

This contribution is organized as follows: First, the time and voltage dependence of the RTN signal is studied. Information about the average lifetime of a filament at a particular temperature and applied bias is provided. Next, it is shown that the size of filaments can be measured using electrical techniques provided that there is access to the oxide capacitance. In high conducting devices, this condition is satisfied and the low-frequency capacitance reflects the active conductive area. The fluctuations in capacitance correlate very well with corresponding fluctuations in the current and provide a direct estimation of the active filament area as well as the associated current density. The study of filament properties is completed with an investigation about how RTN fluctuation varies as a result of temperature. It is shown that by varying the temperature, the current changes in discrete and equal steps in

magnitude. This suggests that a network of identical filaments transports the current. Finally, we discuss the physical model responsible for switching on and off the filaments and the role of the internal device structure in this process.

6.2. Results

The device studied in this chapter is described in the experimental part of Chapter 3. The noise and IV measurements procedures are described in Chapter 5.

The RRAM shows bistable IV characteristics, a HRS and a LRS. Figure 6.1 shows the corresponding IV curves. The LRS shows a region with NDR. It is assumed that the NDR region is caused by a cascade of switching off events that turn-off the high conductive state and the corresponding filamentary paths. The application of a bias slightly above the onset of the NDR regions will bring diode to the HRS. [91]

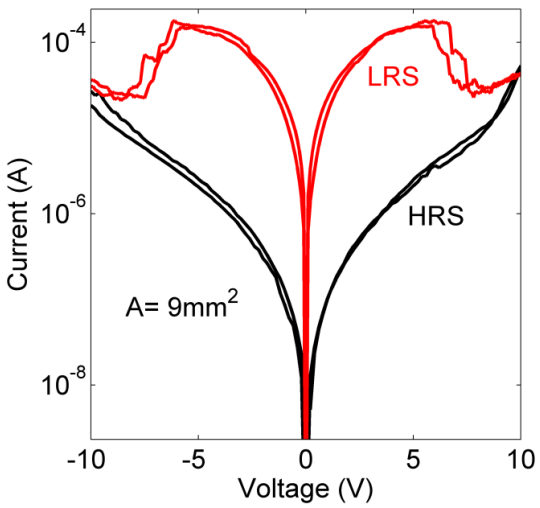


Figure 6.1 - JV characteristics in the LRS and HRS of an Al_2O_3 / polyspirofluorene (PFO) bistable resistive switching diode.

In order to obtain the electrical bistability shown in Figure 6.1, the diode has to be submitted to an electroforming procedure. This can be done using two different methods: (i) by a applying a voltage ramp up to a voltage near the oxide breakdown, or alternatively (ii) by applying a current step. Both methods have been reported previously. [101, 102] After electroforming the device behaves as a programmable memory with a reasonable on/off ratio (10^4) and good cycle endurance. These memory properties have been published before.

6.2.1. Small-signal impedance characteristics

In order to understand the small-signal impedance characteristics namely the changes in capacitance upon resistive switching it is convenient to describe the internal device structure by an equivalent circuit. The memristor is physically a bi-layer structure comprised of an oxide layer in series with a polymer layer. When the memory is in the HRS, it behaves as simple parallel plate capacitor with capacitance (C) and dielectric loss (G/ω) almost independent of frequency (f), where G is the conductance and $\omega = 2\pi f$, is the angular frequency. As no free carriers are able to follow the modulation of the external voltage, the system behaves like a passive dielectric medium. The capacitance is frequency independent. The curve (1) in Figure 6.2(a) shows this behaviour. The capacitance measured is the series sum of C_{OX} and C_{POLY}. When the memory is the LRS, the polymer resistance becomes so low that is possible to modulate the charge carrier density near the oxide layer. Furthermore, at low frequency the capacitance rises substantially. If the entire device area is participating in the conduction, the capacitance at low frequency should correspond to the oxide capacitance. As the frequency increases, the carriers cannot follow the ac field. The capacitance should decrease with the frequency to the geometrical value. This causes a relaxation often named Maxwell-Wagner relaxation, as shown in curve (2) of Figure 6.2(a). Under these conditions, the diode can be described by a double-RC circuit in Figure 6.2(b). The double RC circuit represented in Figure 6.2(b) easily interprets the Maxwell-Wagner relaxation. This circuit exhibits dispersion in capacitance centred on a relaxation frequency already introduced by equations (2.10) and (2.11) in Chapter 2.

As a summary, when the memory is in the high conductance state, the polymer has enough free carriers to modulate the oxide capacitance and the capacitance as function of frequency exhibits a Maxwell-Wagner dispersion. In the HRS, the memory behaves as a parallel-palate capacitor. A resistive switching event in the LRS should then be accompanied by a corresponding capacitive change.

We expect that at low frequency, the measured capacitance should be the oxide capacitance (39.8 nF for a 20 nm thick oxide). The experimental observed value (5.2 nF) is smaller than the expected value for oxide capacitance. The reason is that only a

small fraction of the total area is actually involved in the resistive switching. Most of the physical diode area remains insulating.

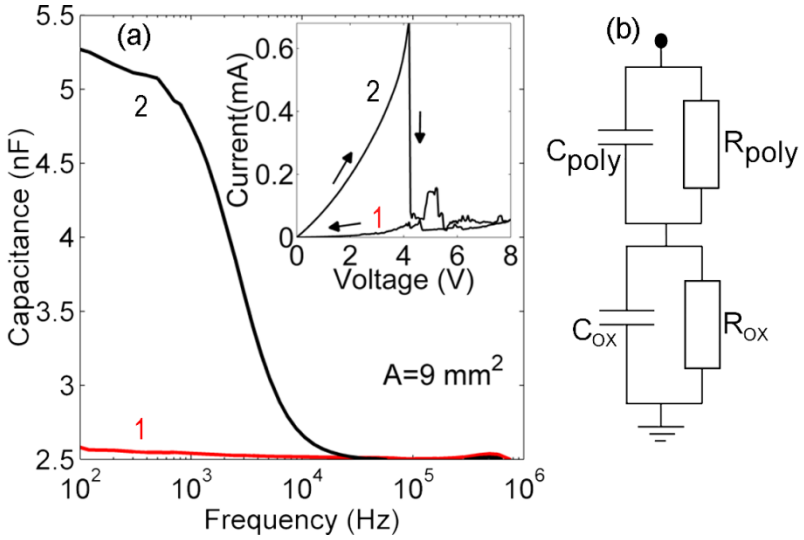


Figure 6.2 - (a) Frequency dependence of the measured capacitance in the HRS (1) and in the LRS (2). Inset represents the IV characteristics of the diode illustrating the different capacitance values. (b) Equivalent double RC circuit.

The observation of a low-frequency capacitance higher than the geometrical capacitance depends strongly on the amount of free carriers available, and consequently on the resistance. This LRS varies from device to device. The reason is still not clear. It is probably related to small variations introduced by the electroforming process.

Assuming that capacitance changes can be related to the active area of the oxide, then it is possible to estimate the current density transported by the active region involved in the switching. In summary, the active area undergoing resistive switching can be obtained through changes in capacitance (ΔC) and the current transported by that area is calculated by the corresponding changes in current (ΔI). Applying this to the data in Figure 6.2(a) we estimate the area of the conducting region A_f to be:

$$A_f \approx \frac{5.25\ \text{nF}}{39.8\ \text{nF}} \times 0.09\ \text{cm}^2 \approx 0.01\ \text{cm}^2 \qquad (6.1)$$

With a current density J_f given by:

$$J_f \approx \frac{0.6\ \text{mA}}{0.01\ \text{cm}^2} \approx 61\ \text{mA/cm}^2 \tag{6.2}$$

The first conclusion is that only 11% of the device area is actually involved in the resistive switching. It is difficult to estimate how many filaments contributed to this area. Under the NDR region, the switching–off is too fast to discern current fluctuations caused by individual filaments. These filaments are turned-off under the NDR region and they contribute to the non-volatile memory properties.

When the memory is in a LRS with bias applied bias below the onset of NDR region, (V<4 V) the current is still noisy. The fluctuations are relatively small and fast. Figure 6.3 shows the IV characteristics of a high conducting device where these fluctuations can be observed. The inset of Figure 6.3 exhibits the high capacitance values of such a high conducting device. A detailed view of the RRAM fluctuations is shown in Figure 6.4.

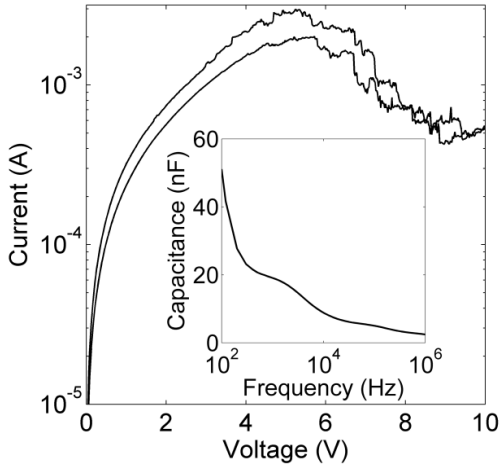


Figure 6.3 – IV characteristics of a high conducting RRAM with 9 mm^2 area. Inset represents the Capacitance-Frequency response of the RRAM.

The fluctuations can be discrete between two well-defined levels as a pure RTN signal. When the capacitance is recorded at the same voltage as function of the time, fluctuations in capacitance are also observed. Using a similar analysis as the one carried out for the switching under the NDR region, we estimate that these fluctuations are caused by a single filament switching consecutively between resistive states and carrying a current of 0.05 mA. The corresponding capacitance fluctuations

reach up to 6 nF. The active area required to give this extra capacitance is 0.013 cm^2. The single filament causing the RTN is carrying a current density of 3.85 mA/cm^2.

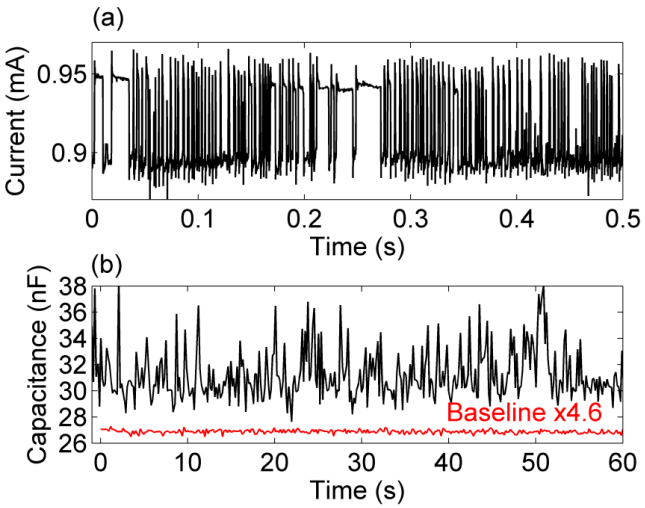


Figure 6.4 – (a) Current discrete fluctuations in the form of RTN measured with 2 V constantly applied. (b) Capacitance fluctuations measured with 2 V constantly applied at 200Hz. Baseline represented in the bottom of the capacitance measurement was measured at V=0 V and has an offset of x4.6 for visualizations purposes.

The observation of capacitance fluctuations associated with resistive switching fluctuations is only possible if the polymer resistance is relatively low. When the high conductance state resistance increases above a few tens of kΩ the oxide capacitance is not accessible and the estimation of filamentary current density is no longer possible. However, the memory current still exhibit pronounced RTN. In the following sections, a detailed study of the RTN as function of the applied bias and temperature is presented. Typical time records of 250 ms from a continuous measurement are presented in Figure 6.5. The time records show RTN with large discrete current fluctuations of about 45 nA, corresponding to $\Delta R/R \sim 5$ %. The large discrete current fluctuations allow us to quantify the time that a filament is turned-on, τ_{on}, and is turned-off, τ_{off}. The first and second trace in Figure 6.5 exhibits a filamentary path that is active most of the time, and is only switched off once in a while with $\tau_{off} \approx 0.7$ ms. The third trace shows the filament being turned on and off at similar time scales of about 1.7 ms.

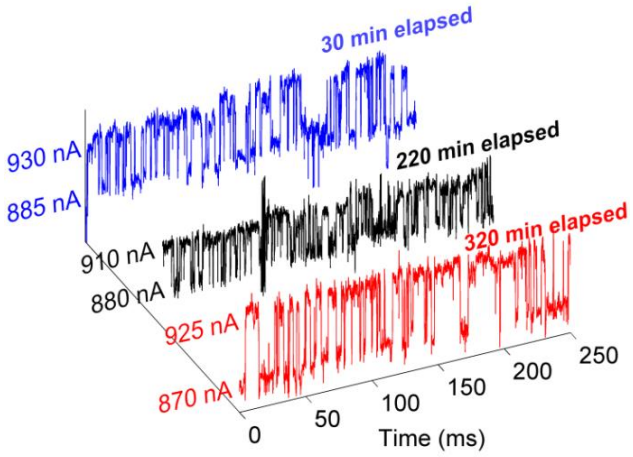


Figure 6.5 - Time records of current RTN fluctuations measured at 290 K under the applied bias of 1.2 V. Measurements were taken during 6 hours, and the time is recorded on the right of the RTN plot. For each of the three RTN examples the current discrete levels are written on the left.

We derived the lifetime of a filament from a statistical analysis of the time traces by taking the probabilities P_{on} and P_{off} as exponentially distributed in time as [155]:

$$P_{on,off}(t) \propto \exp\left(-t/\tau_{on,off}\right) \tag{6.3}$$

Figure 6.6 shows the extracted time distribution for the up and down states. We could fit the experimental data for this particular case with a value for τ_{on} of 1.7 ms and for τ_{off} of 0.7 ms. A good agreement is obtained. The voltage noise spectral power density $S_I(\omega)$ from a two level random signal can be derived through the equations (6.4) and (6.5) as in: [156]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{on}} + \frac{1}{\tau_{off}} \tag{6.4}$$

$$S_I(\omega) = 4\left(\delta I^2\right)\left(\frac{\tau_{eff}}{\tau_{on}+\tau_{off}} \cdot \frac{\tau_{eff}}{1+\omega^2\tau_{eff}^2}\right) \tag{6.5}$$

Where, $\omega = 2\pi f$ is the angular frequency and $\delta I = 0.5$ μA the amplitude of the voltage fluctuations.

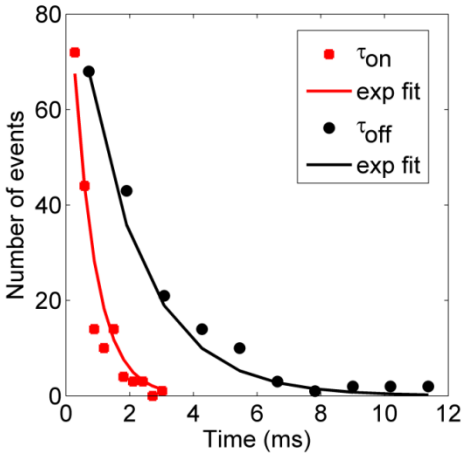


Figure 6.6 - Histograms of the up and down times for RTN fluctuation at room temperature. Both times follow an exponential distribution.

Figure 6.7 show that a quantitative agreement is obtained using the previously derived time constants for τ_{on} and τ_{off}. Time constants depend on device structure, history and applied bias. It only confirms that in the LRS the current flows through filaments. The switching is due to the opening and closing of the filaments.

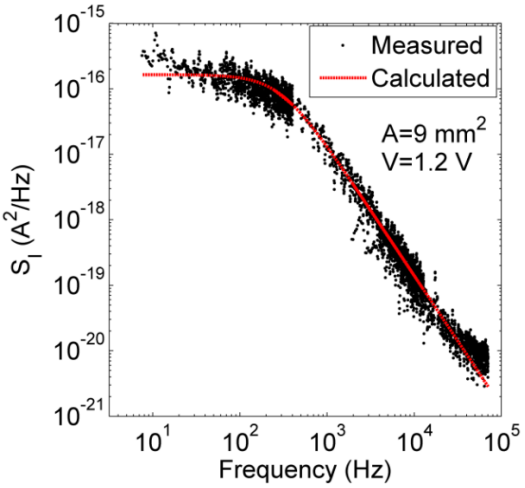


Figure 6.7 - Measured (black dots) and calculated (dotted red line) current noise spectral power density $S_I(\omega)$ memory cell with a two level RTN as shown in Figure 6.5.

Figure 6.7 illustrates a Lorentzian spectrum, which corresponds to randomly distributed RTN fluctuations previously observed. These fluctuations originate from a trapping mechanism with exactly the same time constants calculated in Figure 6.6, e.g. τ_{on}=1.7 ms and τ_{off}=0.7 ms.

6.2.2. Electric filed dependence of RTN fluctuations

Figure 6.8(a) shows typical time traces of the RTN signal for different applied voltages below the onset of the NDR region. Upon increasing bias two effects occur (i) the magnitude of the current fluctuations increases and (ii) the frequency of the switching events increases. Under an applied bias of 0.5 V the current fluctuations reach 20 nA with a characteristic τ_{eff} of 10 ms. At 4 V the current fluctuations reach 100 nA with a τ_{eff} as fast as 10 μs. The dependence of τ_{eff} with the electric field (E) follows power-law decay kinetics, $\tau_{eff} \sim 1/E^{\alpha}$. The exponent α is equal to 2.4 as show in Figure 6.8(b).

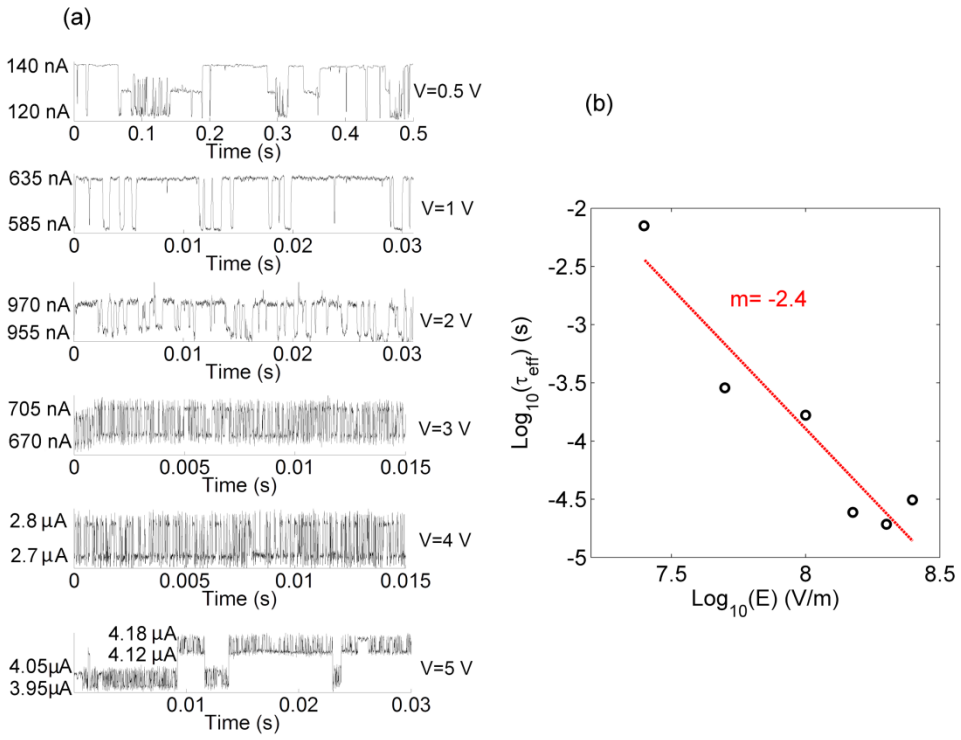


Figure 6.8 – (a) Time records of RTN fluctuations measured at 290 K under different applied voltages. (b) Trap effective time as function of the average applied electric filed through the memory diode. The exponential fit in red-dash has a slope m of -2.4.

With increasing bias larger filaments are active, furthermore, these filaments switch on and off at a higher rate.

6.2.3. Temperature dependence of RTN signal

The impact of temperature on the RTN signal was also studied. Figure 6.9(a) shows several current time traces recorded at different temperatures. The first thing to note is that the frequency of up (on) and down (off) events increases rapidly with increasing temperature. When the temperature is 200 K, τ_{eff} is approximately 70 ms. This time constant decreases with temperature in a linear fashion down to 1 ms at 330 K as shown in Figure 6.9(b).

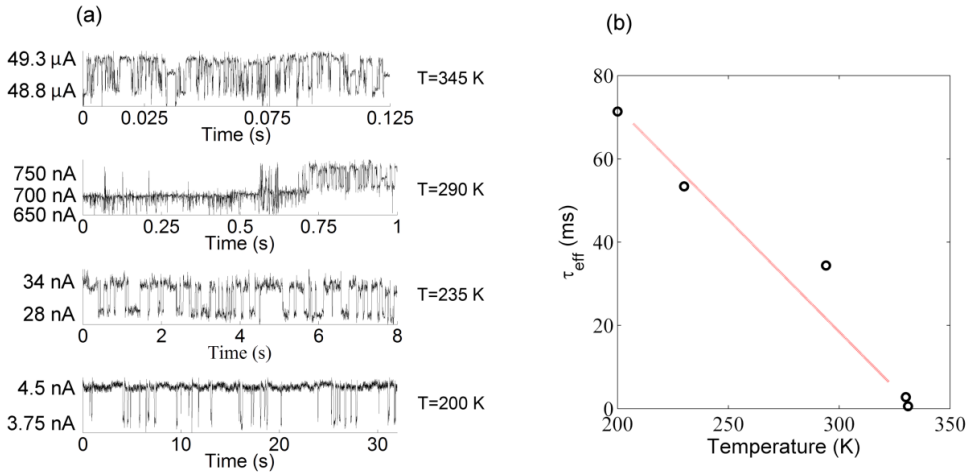


Figure 6.9 - (a) Time records of RTN fluctuations measured at different temperatures with a constant applied voltage of 1.9 V. (b) Temperature dependence of $\tau_{eff.}$

The temperature and bias dependence of the RTN signal is similar. For example, the higher the temperature, or the bias, the higher the switching rate of the current fluctuations increases. Both temperature and bias cause an increase in the population of the free available charge carriers. This clearly suggests that the turning on and off of filaments is strongly dependent of free carrier density.

Another interesting finding is that the current fluctuations are not only discrete but also of equal magnitude. Figure 6.10(a) shows a clear example of three discrete fluctuations equally spaced by 5 nA. A better analysis can be made with the p.d.f. as illustrated in Figure 6.10(b). A good fitting can be made with four equally spaced Gaussian peaks with the same standard deviation ($\sigma \approx 0.7$). This type of behaviour can be explained by the existence of three distinct filaments each one carrying 5 nA.

Similar behaviour was also found at other temperatures. Not only are fluctuations of 5 nA observed, but fluctuations of 1 nA are also common.

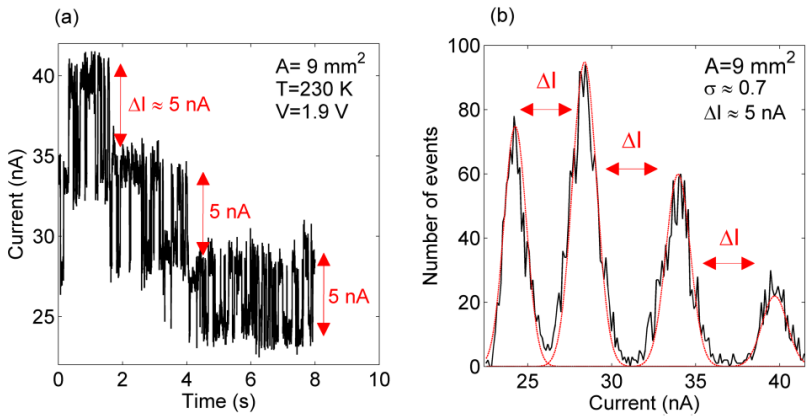


Figure 6.10 – (a) Record of an RTN signal with 4 current levels multiple of 5 nA at 230 K. A bias of 1.9 V was constantly applied during measurements. (b) P.d.f analysis of the RTN signal in (a) exhibiting 4 Gaussian peaks. A bias of 1.9 V was constantly applied during measurements

Figure 6.11 shows the p.d.f of noise traces recorded at different temperatures.

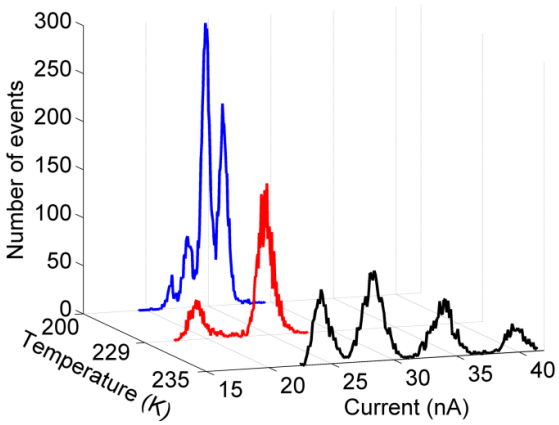


Figure 6.11 – P.d.f analysis measured at different temperatures. A bias of 1.9 V was constantly applied during measurements.

At 200 K the peaks are equally spaced by 1 nA. The peak centred at 25 nA is observed for all three different temperatures 200 K, 229 K and 235 K. Furthermore, it is also evident that the peaks tend to be equally spaced by 5 nA. This is only possible if the filaments are identical. Comparisons with other samples show the size of filaments may vary from sample to sample and that it is possibly controlled by the electroforming process.

6.3. Conclusion

The electrical conduction in resistive switching memories is not homogeneous. Only 11% of the device area is actually involved in the electrical conduction. This active area is comprised of a network of filamentary current paths, probably uniformly distributed as thermal images suggest. [21]

The filamentary current paths are intermittently switching on and off and giving rise to current fluctuations which were analysed as RTN signals.

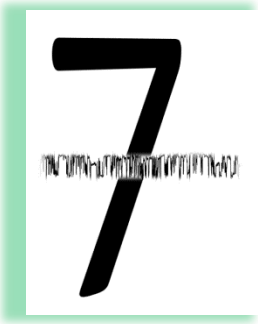
By combining low-frequency capacitance fluctuations with the corresponding current fluctuations it was possible to estimate the overall current density (61 mA/cm^2) of the active area involved in the resistive switching. This corresponds to the area responsible for the NDR region of the IV curves.

The analysis of small fluctuations occurring for voltage lower than the NDR region shows that the filaments transport a current density of 3.85 mA/cm^2. These values are not typical of metallic filaments and cannot generate deleterious effects by Joule heating. We propose the current is limited by the polymer layer.

The bias and the temperature dependence of the current fluctuations reveal that the switching frequency increases dramatically as the free carrier density increases. It is proposed that the switching off mechanism is determined by the free electron concentration in the polymer layer.

The switching frequency of individual filaments is relatively high (kHz). This seems to confirm that these filaments are not created and destroyed by movement of atomic species, such as metal ions but instead they are turned on and off like switches.

The temperature dependence analysis reveals that the fluctuations in current tend to be discrete and of equal magnitudes. This suggests that the filaments are alike in size.



OLED degradation and resistive switching

OLEDs, either based on polymers or small molecules, suffer from early failure: an unpredictable sudden increase in current with a total loss of light output. This reliability issue is studied using a combination of electro-optical measurements. OLED degradation is initially triggered by a trapping mechanism near the Al/LiF interface. Evidences for this trapping are provided by small-signal impedance measurements, observation of optical bursts at a wavelength higher than the polymer band-gap electroluminescence and low-frequency electrical noise measurements.

Charged traps induce a dipole layer at the Al/LiF interface. When a critical internal field is reached, the dipole recombines through a radiated process giving rise to optical blinks. In the final degradation stage, a resistive switching layer is formed which can lead to current fluctuations and filamentary current paths. Furthermore, the double-carrier injection equilibrium is no longer maintained, and the normal electroluminescence is inhibited.

7. OLED degradation and resistive switching

7.1. Introduction

OLEDs either based on small-molecules or polymers have been studied extensively for applications in flat panel displays and lightning. [157-165] OLED quality has been expressively improved during the last two decades. Power efficiency has increased, threshold voltage was lowered, and brightness has been improved. Surprisingly, the operational lifetime remains poor. This is because of an intrinsic degradation process for which detailed physical explanation is still lacking. Intrinsic degradation refers to the progressive and spatially uniform loss of luminance efficiency over time under continuous operation. The luminance degradation is mostly associated with the rise in operating voltage. In fact, in many cases the luminance decay is almost a mirror reflection of the voltage rise. Several mechanisms have been proposed in the literature, namely damage caused by thermal effects, [166-168] formation of traps acting as luminescence quenchers, [169-174] interface and anode degradation. [171, 175-178]

In this chapter we provide evidences that degradation in small molecule OLEDs is caused by a trapping mechanism occurring at the cathode interface. IV measurements, Light-voltage (LV) characteristics, small signal impedance and noise measurements were used to elucidate the origin of the OLED degradation phenomenon.

7.2. Experimental

The diode consists on ITO/ N,N'-di(1-naphthyl)-N,N'-diphenyl-(1,1'-biphenyl) 4,4'-diamine (NPD) (55 nm)/ tris(8-hydroxy-quinoline) aluminium (AlQ_3) (80 nm)/ LiF (1 nm)/ Al (100 nm) as illustrated in Figure 7.1(a). The current–voltage (JV) curves were obtained using a Keithley 487 pico ammeter voltage source and an Agilent semiconductor parameter analyzer 4156C. Light output measurements were obtained using a silicon photosensor connected to the Keithley 487 picoammeter voltage source and temperature dependent measurements were carried out in a liquid helium cryostat (Advanced Research Systems, ARS - HC2). Small-signal admittance measurements over the range 50 Hz to 1 MHz were carried out with a Fluke PM 6306 RCL meter. All the 15 OLEDs investigated were fabricated under the same conditions.

The OLED light emission is detected with picoammeter through a silicon photosensor as illustrated in Figure 7.1(b). Luminescence results are reported in arbitrary units (a.u.) once the OLED contact area with the light sensor slightly varied for each tested OLED.

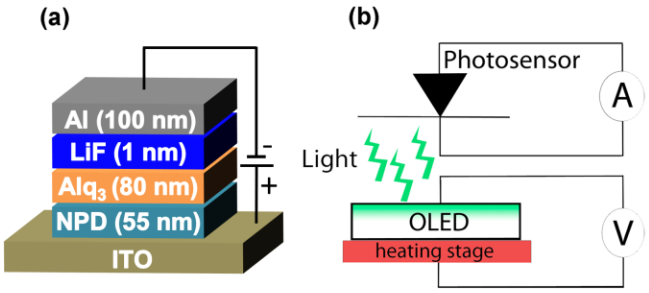


Figure 7.1 - a) Schematic of OLED construction. b) Schematic of OLED experimental setup

7.3. Results

An illustrative example of early failure in OLEDs is presented in Figure 7.2. The voltage and luminance as a function of time is represented in Figure 7.2(a) and the current as a function of time is illustrated in Figure 7.2(b). In this example after 450 hours the light-emitting diode suddenly dies. The time to reach failure under continuous operation varies from sample to sample. The short is always first preceded by a slow rise in voltage. In the example of Figure 7.2(a), the voltage increases from 5 to 6 V in a time span of 400 hours (more than 16 days under continuous operation). Interestingly, the light output keeps roughly constant and only decreases in very small steps coinciding with downward steps in the voltage. After 400 hours, a change in behaviour occurs and the voltage starts to decrease accompanied by a pronounced decrease in the light output. This behaviour occurs in a relatively short period (two days). Finally, the current becomes nosier and a short occurs. In summary, the degradation evolves through two distinct phases: First there is a slow process leading to an increase in the barrier built-in voltage without changes in the light output. Second, the barrier built-in voltage decreases quickly leading to a dramatic loss output.

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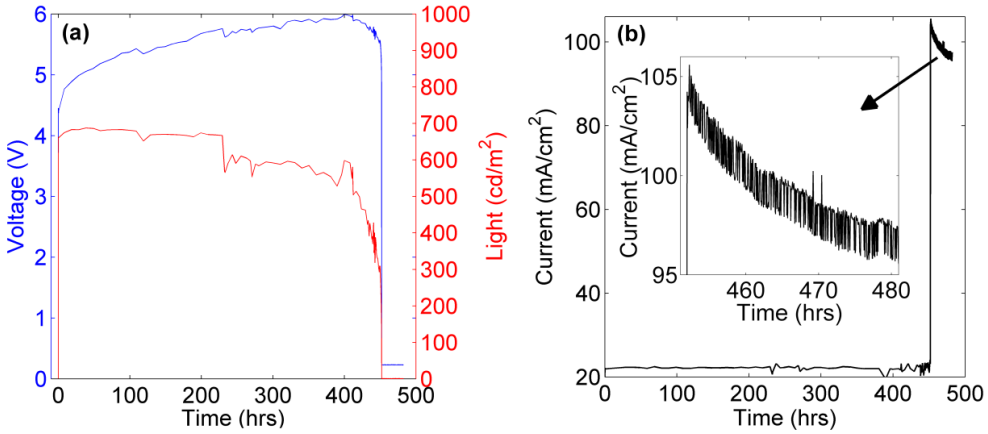

Figure 7.2 - a) Luminance and voltage versus time curves recorded for an ITO/NPD/Alq_3/LiF/Al OLED. During measurements the current was kept constant at 2 mA in a device with an area of 3x3 mm. b) The time dependence of the current. After the total loss of EL the current switch from 22mA/cm2 to near 100 mA/cm^2 and exhibits discrete current fluctuations.

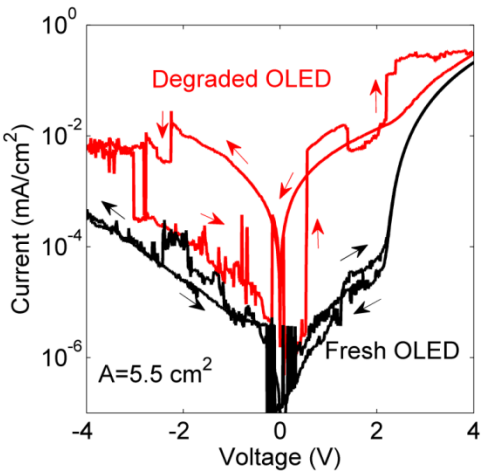

Figure 7.3 - JV characteristics of both fresh and degraded OLED. Degraded OLEDs exhibit higher current densities. In reverse bias it is common to observe NDR and a pronounced hysteresis. In fresh OLEDs at forward bias a threshold voltage is observed at 2.2 V. In a degraded OLED the threshold voltage shifts to near 0 V.

Figure 7.3 compares the JV curve of a degraded OLED with the characteristics of an as received OLED. The JV curve of the as received (or fresh) OLED show the knee at 2.2 V corresponding to the onset of electroluminescence. Interestingly, for reverse and small forward bias the current is unusually high and noisy. This is an indication that the OLED is already deteriorated.

Figure 7.3 further illustrates that fresh OLEDs exhibit lower current than degraded ones. In reverse bias, small current fluctuations are observed and in forward bias, the onset voltage correlates with the light emission voltage.

Degraded OLEDS show in reverse bias NDR regions as well as large switching events. These current fluctuations become more pronounced as the degradation evolves.

In fresh OLEDs, small light fluctuations under reverse bias (V= -3 V) can be monitored as illustrated in Figure 7.4(a). The optical blinks show two interesting features. First, they only occur in the voltage return scan. This suggests that the optical emission requires first the application of a high reverse field. Their intermittent nature further indicates that they originate in a sporadic recombination process. In addition, these blinks are on the blue part of the spectrum and therefore the emissive process is not related with the bulk organic layer. Blinks or flashes are most frequently observed when the OLEDs already exhibit some sign of degradation (for instance has an anomalous high reverse current as in Figure 7.3.

In order to study the optical blinks the light output was monitored simultaneously with the corresponding current as a function of the time. The time dependence of the light and current is shown in Figure 7.4(b). The magnitude of the current spikes correlates well with the optical flashes.

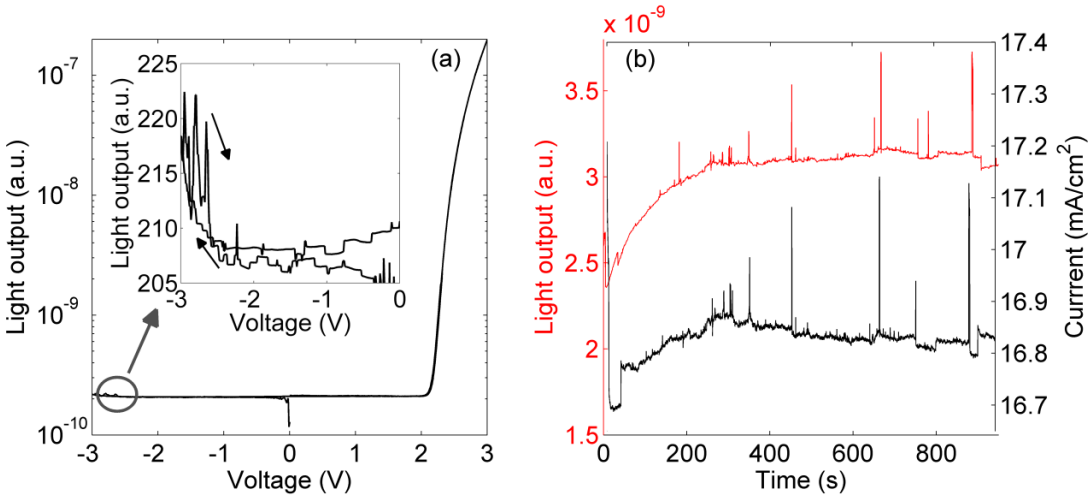

Figure 7.4 - a) Light-Voltage characteristic showing the normal green electroluminescence above 2 V. The inset shows a very small light emission after the diode was driven under reverse bias. b) Optical blinks in phase with current switching events. A blue filter that only allows light to pass between 455 nm and 492 nm was interposed between the LED and the sensor and a voltage of 3.5 V was applied.

A physical mechanism that can account for this correlation between current and light blinks will be presented in the discussion section.

7.3.1. Small signal impedance measurements

In order to correctly interpret the impedance data and used it to locate the origin of the degradation in the device structure, it is important to evaluate first all the expected capacitances of each individual layer. The capacitance of each layer was estimated using equation (7.1):

$$C=\frac{\varepsilon_r \varepsilon_0 A}{d} \qquad (7.1)$$

Where ε_0 is the permittivity of free space, ε_r is the relative dielectric constant, A the area of the OLED and d the thickness of the layer. Thus, the estimated capacitance for each layer is 8 $\mu F/cm^2$ (LiF), 27 nF/cm^2 (Alq_3) and 48 nF/cm^2 (NPD).

Figure 7.5 shows the evolution of the capacitance-voltage (CV) characteristics as the OLED degrades. The lower curve (in black) corresponds to the pristine state. For voltages well below the double injection regime (V<1.9 V), the measured value of the capacitance is relatively constant and equal to the geometric capacitance C_{geo} as given by equation (7.2):

$$\frac{1}{C_{geo}} \approx \frac{1}{C_{NPD}} + \frac{1}{C_{ALq_3}} + \frac{1}{LiF} \approx 17 \text{ nF/cm}^2 \qquad (7.2)$$

For voltages above 1.9 V, the capacitance rises in hand with the increasing electroluminescence up to the maximum value. The increase in capacitance is caused by the injection and accumulation of electrons at the NPD/Alq_3 interface. The capacitance value will correspond basically to the capacitance of the Alq_3 layer as given by the equation (7.3).

$$\frac{1}{C} \approx \frac{1}{C_{ALq_3}} \approx 27 \text{ nF/cm}^2 \qquad (7.3)$$

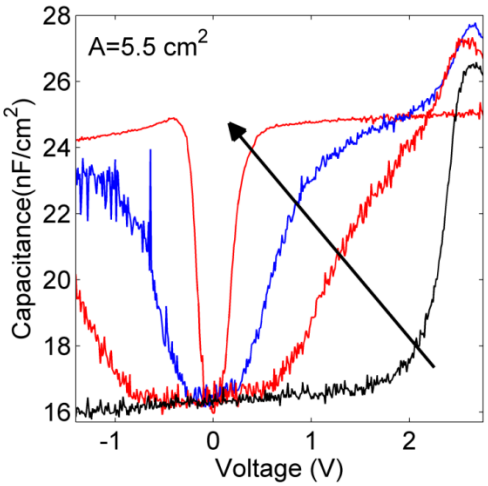

Figure 7.5 - Capacitance-voltage characteristics for different degradation stages. Measurements were carried out at the frequency of 100 Hz. The sign of the arrow points the direction of the degradation.

As the OLED degrades, the onset for the rise in capacitance occurs at lower voltages. The onset voltage decreases from 2.2 V to below 1 V and no longer relates with the light emission.

The decrease on the onset voltage is accompanied with the appearance of a capacitance rise under reverse bias. This phenomenon has been reported previously by others and attributed to a deterioration of the LiF layer. [179]

During degradation, the CV plot becomes nosier. However, at final stages of degradation the CV plot becomes symmetrical and the noise disappears.

The increase in capacitance observed in Figure 7.5 for forward bias below the double injection regime ($0<V<2$) has been explained by others through the existence of an interfacial charge that inhibits electron injection. [180, 181] This allows more and more holes to be injected, therefore raising the capacitance of the device. As the OLED degradation evolves, the onset voltage decreases further to near 0.1 V and the reverse bias capacitance also increases. The CV plot becomes symmetric and varies from the minimum geometric capacitance (C_{geo}) to a capacitance value (25 nF/cm^2), which cannot be related with any combination of the internal layer capacitances.

7.4. Discussion

The analysis of the CV and IV characteristics shows that as the degradation evolves the devices lose the rectifying properties and both IV and CV characteristics become symmetric. Furthermore, at low bias, the conduction is ohmic and the capacitance saturates at a constant value for both polarities.

It is reasonable to assume that the interface responsible for the rectifying behaviour was modified. This interface is the Alq_3/Al/LiF layer. In practical terms, the Al/LiF contact is no longer blocking the hole injection.

LiF is used in OLEDs because it lowers the barrier for electron injection from Al into organic semiconductor. This occurs due to a change in the effective work-function of the LiF/Al contact. [182] The mechanism by which the change in work-function occurs is still under debate. [183, 184]

Recently, it has been shown that alkali halides such as the LiF can undergo electroforming [110, 185] and can be used in memristors. In line with these studies, we propose that under the application of a forward bias (during normal OLED operation) positively charged defects are introduced in the LiF layer. These defects may be stabilized electrostatically by the presence of electrons on the aluminium electrode. Holes trapped in the LiF layer will modify the electric field strength in such a way that the electric field in the LiF layer lowers over time, enhancing tunneling of holes across the interface.

A type of defect that has been shown to form in alkali halides at low energies is the Frenkel Defect. Frenkel defects consist of an anion vacancy (F) and a halogen interstitial (H). Holes trapped in the vacancy can recombine with electrons injected from the electrode and give rise to electroluminescence spikes. Furthermore, these defects can facilitate trap-assisted tunneling of the holes across the LiF, leading to a decrease in the effect barrier height. Bipolar charge transport trough the OLED is no longer dominant and the diode has to switch to unipolar charge transport. Figure 7.6(a) shows a schematic band diagram of the non-degraded ITO/NPD/Alq_3/LiF/Al diode under forward bias. Figure 7.6(b) exhibits the schematic band diagram when the OLED is in a degradation stage.

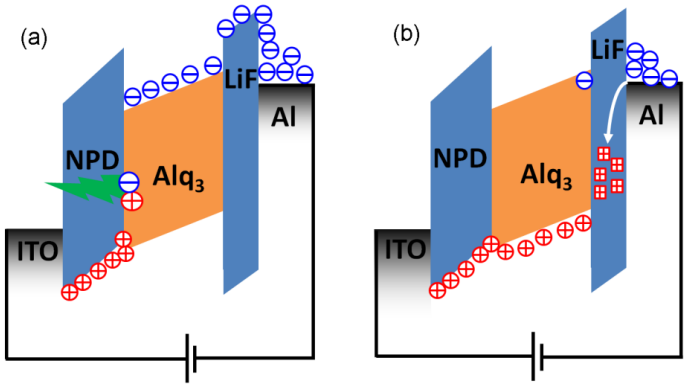

Figure 7.6 - Simplified band diagram for forward applied bias in: (a) Pristine OLED and (b) Degraded OLED.

7.5. Conclusions

In summary, OLED degradation is initially triggered by a trapping mechanism near the Alq_3/Al/LiF interface. This change occurs because the LiF layer is modified or electroformed. This change of the LiF layer is caused by a dielectric soft-breakdown and leads to the formation of anion vacancies. The LiF is converted into a resistive switching layer. The Alq_3/LiF/Al interface becomes transparent for holes. Bipolar charge transport is no longer efficient and the diode switches to unipolar charge transport. Normal polymer electroluminescent is quenched but recombination in the LiF can give rise to spikes or flashes.

The proposed modification of the LiF (like a p-type doping of the LiF) explains the symmetric nature of the IV curves around zero bias voltage and the absence of a built-in potential.

This will inhibit the injection equilibrium, corrupting the injection of electrons leading to the OLED degradation.

As the OLED degrades, an evolution from a double carrier injection diode to a single carrier injection (holes) is observed.

Electrical noise as a diagnostic tool for OLED reliability

The premature failure of OLEDs, described in Chapter 7, has a major impact on the production yield. The degradation will occur during operation causing the failure of a commercial product. To avoid faulty devices and complains from the consumer, the manufacturer must be sure that his product meets the lifetime requirements. It is then crucial to be able to predict which OLEDs are susceptible to failure and remove them from the production line. This work addresses this problem using small-signal impedance measurements and electrical noise techniques. Robust OLEDs show a current noise spectrum proportional to 1/f. OLEDs susceptible to failure have $1/f^{3/2}$ and/or may start exhibiting a standard 1/f behaviour that rapidly evolves with time (typical 30 minutes) to $1/f^{1.6}$. In addition, OLEDs susceptible to early failure have a higher DC leakage. It is proposed that a combination of both measurements can be used as a diagnostic tool for OLED reliability in a production line.

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8. Electrical noise as a diagnostic tool for OLED reliability

8.1. Introduction

OLEDs either based on small-molecular or polymers have been studied extensively for their potential applications in flat panel displays. [157-161] OLED quality has been extensively improved during the last two decades. Power efficiency has been increased, threshold voltage lowered, brightness improved, and operational lifetime enhanced. However, OLEDs as luminaries need a reliability of luminaries. A conservative figure is 15 years. The technology has not reached its peak mainly because of prevailing degradation mechanisms such as the dark spot formation [186, 187] and the gradual decrease of performance with current passing through the device, e.g. intrinsic degradation. [187] Dark spot formation is a process independent of whether the device is operating or not and therefore has a great impact in the OLED shelf life. [188] The degradation of OLED devices due to operation is well documented and appears to be caused by chemical degradation of the organic materials [188-190] during device operation.

OLEDs processed in the same conditions, often show different types of degradation. The OLEDs that will degrade faster will interfere in the device lifetime. Improvement in lifetime can be ultimately achieved through improvements in materials and device architectures. However, time to market entrance is mandatory. Thus, a fast selection of the non-failing OLEDs to improve the technology lifetime has become of extreme relevance. A characterization method is needed to predict early failure or the absence directly after fabrication.

Here we propose electrical noise together with small signal impedance measurements to arrive to a diagnostic criterion. Furthermore, we argue that the degradation is caused by a trapping mechanism occurring at the cathode interface.

8.2. Results

8.2.1. 1/f noise measurements

The device and the experimental apparatus have been already described in Chapter 7.

Hooge's relation for the 1/f noise, the noise parameter and the figure of merit qαμ are given in Chapter 5 by equation (5.1). Here, t is the NPD thickness. The value of the parameter K=qαμ is often used as a figure of merit to compare and classify 1/f noise in thin films. We suggest the NPD layer as the dominant noise source in pristine OLEDs. We calculated the coefficient K by using a NPD thickness $t=5.5x10^{-6}$ cm in equation (5.1). This results in $K\approx10^{-21}$ cm^2/Ω. This value is typical for semiconductors, metals or polysilicon (10^{-21} cm^2/Ω). [142, 143]

A robust OLED shows a current noise spectrum exhibits a $1/f^{\gamma}$ proportionality where $0.85 \leq \gamma \leq 1.2$. In Figure 8.1, we can observe such behaviour where $\gamma = 0.9$. Typical noise parameters for a robust OLED are: $K \approx 10^{-21}$ and $C_{1/f} \approx 10^{-7}$. This behaviour is independent of time.

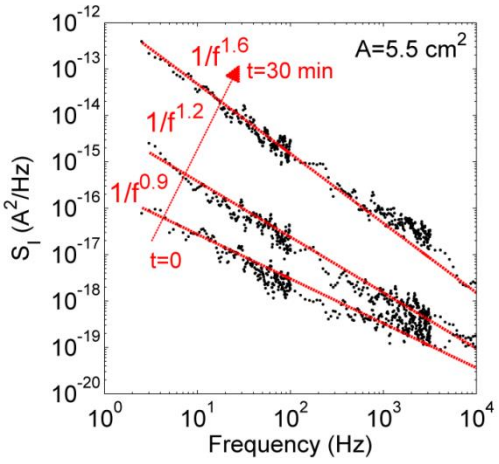

Figure 8.1 - Temporal evolution of the current noise spectra for an unreliable OLED under a constant bias of 2.5 V near the onset of electroluminescence (EL). The increase in $1/f^{\gamma}$ varies in a time scale of approximately 30 minutes. At t = 0, I = 29 μA and the typical 1/f noise parameters are: $C_{1/f} \approx 10^{-6}$ and $K\approx10^{-21}$.

For unreliable OLEDs the 1/f proportionality of the current noise spectrum exhibit two characteristics: (i) it shows with time an increase in the $1/f^{\gamma}$ proportionality from $\gamma = 0.9$ up to $\gamma=1.6$ (see Figure 8.1), and (ii) when $\gamma=1.5$ or 1.6 it shows voltage independent behaviour (see Figure 8.2). The increase in γ with time was previously reported by others [191, 192] and it means that as the OLED degrades the total low-frequency noise increases.

The $C_{1/f}$ increases from typical values $10^{-7} \leq C_{1/f} \leq 10^{-6}$ before to 10^{-5} after deterioration, with huge resistance fluctuations. Perhaps electroforming at the LiF layer

[22, 101, 102, 110] and creation of filamentary paths are responsible for the 1/f noise increase just before light and /or current bursts become dominant. [139]

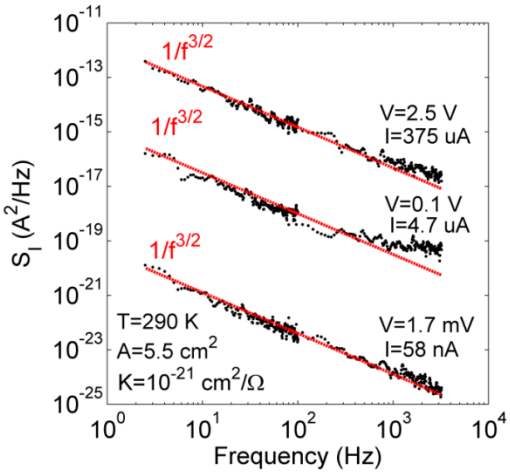

Figure 8.2 - Current noise spectra for an unreliable OLED

8.2.2. Small signal impedance measurements

The small-signal impedance was measured in the frequency range of 50 Hz to 1 MHz. OLEDs prone to fail exhibit unusual DC leakage current. Figure 8.3 shows the typical loss (G⁄ω) spectra measured in different OLEDs, G is the conductance and ω is the angular frequency. The high loss at low frequencies rises as 1/f as expected for a DC resistance.

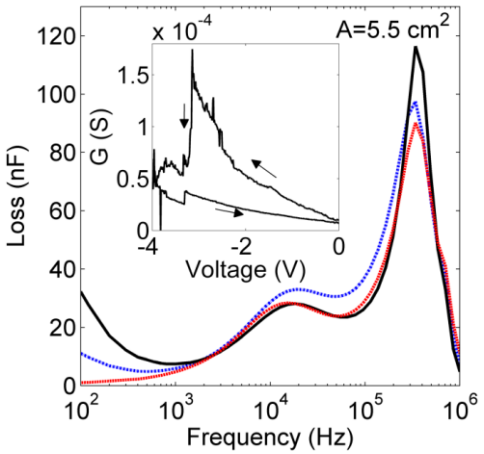

Figure 8.3 - Loss (σ/ω) spectra for 4 pristine OLEDs. Inset shows a G-V curve with a switching event.

A batch of fifteen OLEDs was inspected for high leakage currents in which five exhibited higher leakage values. Typical responses for high and low leakage values are illustrated in Figure 8.3. High leakage current is associated with defects in organic layers and is expected to be enhanced though the developments of electrical shorts that will eventually cause a partial or even total loss of EL. [189, 190] Furthermore, in OLEDs exhibiting brightness degradation and high leakage, the G-V characteristics commonly show resistive switching as illustrated in the inset of Figure 8.3. Applying a voltage sweep from 0 to -4 V, we can observe a resistive switching event at -3 V.

8.2.3. Temperature dependent measurements

Failing and robust OLEDs show a current noise almost temperature independent. However, preliminary results indicate that failing OLEDs exhibit at 240 K a $1/f^2$ contribution with an intersection at f ≈ 100 Hz. (See Figure 8.4). Beyond 250 K, the noise recovers the initial proportionality of $1/f^{1.2}$. The characteristic frequency of the trapping is lower than 2 Hz and τ>0.1s and it appears at the same temperature as the phase transition of super-cooled water. [121-123]

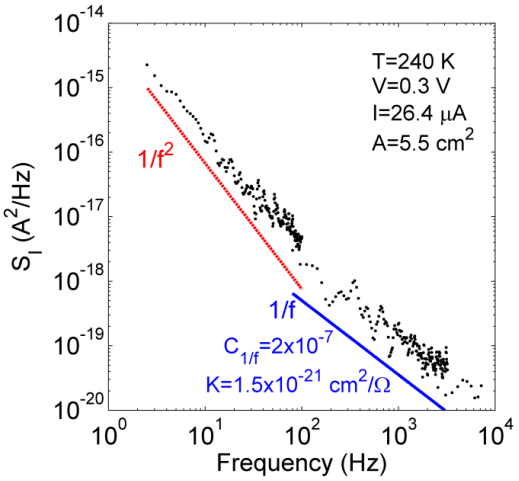

Figure 8.4 - Current noise spectrum recorded at 240 K with a bias of 0.3 V. At frequencies bellow 100 Hz S_I is proportional to $1/f^2$. Above 1/f noise with $C_{1/f}$= 2x10^{-7} and K = 1.5x10^{-21} cm^2/Ω appears

8.2.4. Electro-optical measurements

The OLED light output is monitored as a function of the applied bias. In forward bias, light blinks are frequently observed on top of the steady state green electroluminescence light. These optical blinks are accompanied by upward current jumps as shown in Figure 8.5. Inspection of the blinks spectral region was performed. A deep blue filter (492 nm > λ > 455 nm) was inserted between the OLED and the photo-sensor. Once the green band was removed by the filter the blinks dominated the light output. Therefore, the recombination mechanism behind these blinks did not originate in the band-gap electroluminescence.

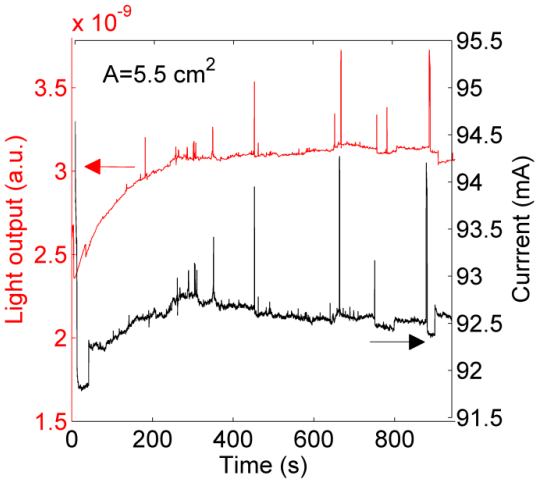

Figure 8.5 - Optical blinks in phase with current switching events measured under a constant bias of 3.5 V. A blue filter (492 nm > λ > 455 nm) was interposed between the LED and the sensor.

Step changes in current can reach magnitudes as high as 1.6 mA and are in phase with EL blinks. As the OLED degradation progresses, these transient events become more frequent. In fact, it has been reported that under high forward voltage, large switching currents occur prior to breakdown and catastrophic failure. [193, 194]

8.3. Discussion

The measured $C_{1/f}$ is extremely high ($\approx 10^{-6}$). Such high values are expected when the current is carried by a low number of free charge carriers or due to the presence of nano-constrictions. [138, 139]

The interface deterioration has been proved to play an important role in the device degradation process, [195] which definitely increases energy barrier fluctuations and causes fluctuations in the number of charge carriers. [191]

The existence of high conductance fluctuations further suggests that a fraction of the OLED turns into a resistive switching layer due to internal modification. Electroforming and soft-breakdown can occur in layers where materials can become bistable e.g. oxides. [101, 196-198] Also, LiF/Polymer interfaces can become electrically bistable. [110] Therefore, we propose that LiF/Alq_3 interface undergoes an electroforming process and becomes bi-stable. Electroformed LiF layers store charges and radiative recombination at the Alq3/LiF interface can explain optical blinks accompanied by current spikes.

8.4. Conclusion

A diagnostic tool for OLED reliability is proposed. Unreliable OLEDs exhibit the following characteristics: (i) relatively high DC leakage current, (ii) current noise spectrum proportional to $1/f^{3/2}$, and (iii) current noise spectrum with a $1/f^{\gamma}$ proportionality that varies in a time scale of 30 minutes between $0.9 \leq \gamma \leq 1.6$ under an applied voltage near the onset of electroluminescence.

The observation of optical blinks and current fluctuations suggests that during the OLED degradation a thin resistive switching layer begins to be formed near the LiF electrode.

Temperature dependent measurements show that the OLED electrical noise is dramatically enhanced at 240 K (temperature of a phase transition of confined water).

Conclusions and Future Work

9. Conclusions and Future Work

9.1. Conclusions

The work presented in this thesis focuses on unipolar switching in polymer RRAMs. The memristor consists on an Al_2O_3 layer on top of a thin semiconducting polymer layer. The IV characteristics are symmetric. The device can be switched between a LRS and a HRS at biases corresponding to the top and bottom of the NDR presented in both polarities. Our findings emphasize the role of the oxide in the observed unipolar switching. The distributed series resistance of the polymer prevents thermal runaway when a local filament is turned on. Furthermore, it delivers a crucial electron trapped charge layer at the oxide/polymer interface.

The IV characteristics are ohmic at low bias and non-ohmic at higher bias, e.g. typically SCL. The memristor switches from LRS to HRS by a cascade of large current fluctuations. The RRAM current fluctuations are inspected with noise measurements. Noise measurements at low bias show 1/f noise and reveal a figure of merit consistent with filamentary current paths. Thermal images together with Comsol simulations have shown that the number density of filaments is still large. Therefore the LRS and HRS currents scale with device area. At high bias noise measurements reveal $1/f^2$ dependence at high frequencies of the noise in the frequency domain. In the time domain discrete current fluctuations in the form of RTN are observed. The RTN noise indicates that the switching is due to opening and closing of discrete filaments. Hence, we assume that a filament can be turned on and off by trapping of a single charge carrier. This assumption is also supported by the anomalous positive temperature coefficient in the LRS.

A filament is switched on by injection of a trapped hole. Holes are minority carriers and are injected above the flat-band voltage, which sets the threshold voltage for switching. Their density however is injection limited. Assuming that a certain critical hole density is needed for switching, then it is not surprising that the delay time for switching the HRS to the LRS depends exponentially on applied bias.

A filament is switched off by annihilation of a trapped hole by a mobile electron.

A fundamental limitation on the speed of operation of the memory device is not the switch-off process but the time- and voltage-dependence of the switch-on mechanism in the oxide.

As the voltage scan speed increases, the NDR shifts to lower voltages. At low scan rates the voltage over the oxide represents almost 100% of the total applied voltage so that a large number of micro-switches are triggered. The fraction of the voltage across the oxide lags significantly behind as the scan rate increases. The fact that we observe lower current magnitudes can explain that fewer switches are activated. Furthermore, at sufficiently high scan rate, the overall device current becomes dominated by the displacement currents that correspond to the device in the HRS. The solution, at this point, to restore the NDR, is to sweep the input ramp with higher voltages.

Currently, in state of the art RRAMs, there is an incompatibility between the long retention time and short read/write pulses at high densities at low applied voltages. This general dilemma can be overcome by an exponential dependence of switching time on applied bias and by a threshold voltage that originate from injection of trapped holes in the oxide.

9.2. Future Work

9.2.1. Optimisation of the forming procedures

There is some variability on the samples parameters particular on the on/off ratio and on the width of the NDR region. We suspect this variability is caused by the electroforming. A proper recipe for the electroforming has to be devised. This procedure should lead to high on/off ratios and narrow NDR regions. Although electroforming by a constant current method seems to be adequate to control the power dissipated and prevent deleterious effect cause by Joule heating, ideal parameters that maximize the on/off ratio have not yet been found. Additional work is required for the optimisation of the forming. It is also important to understand to which degree the forming is homogeneous. In practical terms, forming is not suitable for the industrial fabrication of memories. In a production line, the samples have to be pre-formed by a reliable method.

9.2.2. Rectifying elements for crossbar array structures

Currently there are two approaches to inhibit cross talk. One is serially connecting a rectifying diode to each resistive switching memory element to form the one diode, one resistive switching device (1D1R) structure. The other is directly using self-rectifying RRAM (called 1R structure) as illustrated in Figure 9.1. Crosstalk phenomenon can be eliminated if a diode is serially connected to each resistive memory cell in the 1D1R structure-based RRAM crossbar array. However, compared with the self-rectifying 1R structure, integrating a diode not only increases the complexity of fabrication but also causes operation voltage increase and stability degradation of the memory device. The key issue to be solved urgently in the 1D1R structure is to investigate the rectifying diodes suitable to be in series with RRAM elements. Furthermore, the performances of diodes are not good enough. For example, the rectification ratio is not high enough to meet the requirements of the crossbar array; the current density is not so high that the cell operation voltage increases largely, even the memory could not be switched from HRS to LRS. Consequently, researchers have been seeking the resistive switching memories with self-rectifying effect.

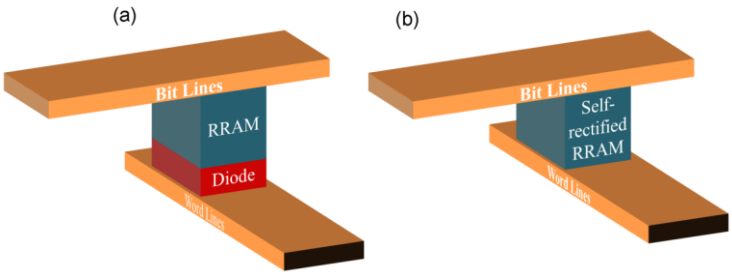

Figure 9.1 - 1Diode-1RRAM (1D-1R) structure and b) Self-rectifying RRAM (1R) structure for passive crossbar array.

9.2.3. Transmission electron microscopy (TEM) studies of the filaments

The filament formation discussion in this thesis consistently explained the behaviour of our memristive devices. However, it is still based on indirect observations. Direct observation of filaments will lead to valuable information about their distribution and sizes. TEM studies are adequate for this purpose.

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