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The role of internal structure in the anomalous switching dynamics of metal-oxide/polymer resistive random access memories

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The dynamic response of a non-volatile, bistable resistive memory fabricated in the form of Al_2O_3/polymer diodes has been probed in both the off- and on-state using triangular and step voltage profiles. The results provide insight into the wide spread in switching times reported in the literature and explain an apparently anomalous behaviour of the on-state, namely the disappearance of the negative differential resistance region at high voltage scan rates which is commonly attributed to a "dead time" phenomenon. The off-state response follows closely the predictions based on a classical, two-layer capacitor description of the device. As voltage scan rates increase, the model predicts that the fraction of the applied voltage, V_{ox}, appearing across the oxide decreases. Device responses to step voltages in both the off- and on-state show that switching events are characterized by a delay time. Coupling such delays to the lower values of V_{ox} attained during fast scan rates, the anomalous observation in the on-state that, device currents decrease with increasing voltage scan rate, is readily explained. Assuming that a critical current is required to turn off a conducting channel in the oxide, a tentative model is suggested to explain the shift in the onset of negative differential resistance to lower voltages as the voltage scan rate increases. The findings also suggest that the fundamental limitations on the speed of operation of a bilayer resistive memory are the time- and voltage-dependences of the switch-on mechanism and not the switch-off process. © 2013 American Institute of Physics. [http://dx.doi.org/10.1063/1.4799093]

I. INTRODUCTION

The development of new non-volatile memory devices is being actively pursued. One type offering excellent prospects is the resistive random access memory (RRAM) device, a simple diode structure whose resistance can be programmed reversibly by a voltage pulse to be high or low. Resistance switching has been reported for a wide variety of materials, including oxides,[1] molecular semiconductors such as pentacene,[2] anthracene,[3] copper-tetracyano-quinodimethane (Cu TCNQ),[4] blends of organic materials[5–7] and molecular materials doped with nanoparticles.[8–10] Semiconducting polymers have also been investigated.[11,12] A promising one consists of a thin semiconducting organic film sandwiched between two metal electrodes, one of which is aluminum covered by a native- or thicker oxide. Although, it is becoming accepted that the oxide layer is required to achieve resistive switching,[13,14] recent evidence[15,16] shows that the polymer also plays a crucial role by providing an electron trapped charge layer at the polymer/oxide interface. This charge layer enhances tunneling across the oxide and tunes the formation of electrically bistable defects. In addition, the distributed series resistance of the polymer prevents thermal runaway when a

local defect (filament) switches on. Polymer/oxide diodes are then expected to provide not only better control of the RRAM properties but also superior endurance compared to oxide-only based memristors. Furthermore, polymer/oxide memories can be printed and integrated into complex, large area organic based circuits.

Polymer/oxide based memories show typical current density-voltage (*J-V*) characteristics with a negative differential resistance (NDR). As early as 1967, Simmons and Verderber[10] studied the behavior of NDR dynamics in SiO_X memories using a triangular bias sweep profile. A peculiar, counter-intuitive behavior was observed: upon increasing the voltage scan rate, both the current and magnitude of the NDR gradually decreased, the latter even disappeared completely. Here, we characterize a similar temporal behavior reported for Al_2O_3/polymer memories by Verbakel *et al.*[17] and reproduced here. Drawing upon the results of additional experimental measurements combined with simple theoretical considerations of processes occurring in these bilayer structures, we arrive at a model which provides a basis for explaining this apparently strange dynamic behavior of bilayer resistive switches, including the delay time and wide range of reported switching speeds.

This contribution is organized as follows. First, we consider the dynamic behavior of the off-state and show that it

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is readily predicted by a two-layer capacitor model reflecting the device structure. The transient response of the on-state is then explored in detail and the findings coupled with simulations based on the two-layer capacitor model to explain the anomalous behavior observed on increasing the voltage ramp speed. Finally, the implications of our findings for the optimization of switching speed in such devices are discussed.

II. EXPERIMENTAL

The diode structure (Fig. 1(a)) consisted of an Al bottom electrode, a sputtered layer of Al_2O_3 (20 nm), a spirofluorene polymer (80 nm), and a Ba/Al (5 nm/100 nm) top electrode which forms an Ohmic, electron injecting contact to the polymer. The devices, with an active area of 9 mm^2, were encapsulated to exclude O_2 and H_2O. In all cases, the polarity of the applied voltage refers to that applied to the bottom Al electrode. Quasi-static J–V curves were obtained using a Keithley 487 picoammeter. The dynamic behavior of the J-V curves was recorded using the experimental arrangement in Fig. 1(b) which comprised a signal generator and an oscilloscope combined with a low noise pre-amplifier. A photograph of an encapsulated device containing a number of diodes is shown in Fig. 1(c). Device modeling was undertaken using the Advanced Design System (ADS) circuit simulator from Agilent.

III. RESULTS AND DISCUSSION

Pristine diodes were turned into programmable resistive switching memories by sweeping the voltage from 0 to 12 V. Following this electroforming process, the devices exhibited the usual NDR and bistable J-V characteristics. Fig. 2 shows that for the present diodes the NDR consists of a single or possibly a few switching events. The memory can be switched between off- and on-states by applying voltage pulses with amplitudes corresponding to the top and bottom of the NDR in Fig. 2, i.e., at about 5–6 V and 8–10 V, respectively. In the following, we investigate separately the
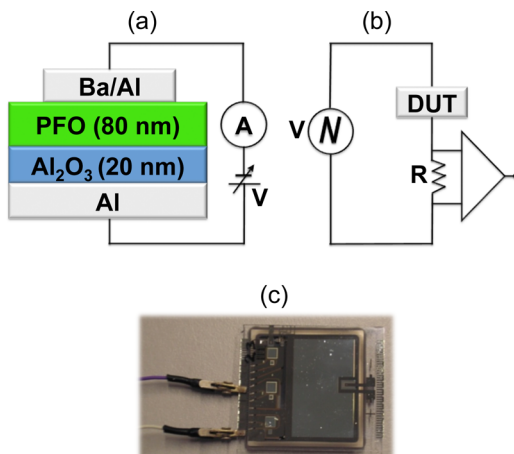

FIG. 2. I-V characteristics in the on- and off-state of an Al_2O_3/polyspirofluorene bistable resistive switching diode. The memory was electroformed at 12 V.

dynamics of the device current response in both these memory states.

A. Transient response of the off-state

Figure 3(a) shows the experimental J-V characteristics for the off-state obtained with increasing voltage scan speeds. We have already shown[14] that these two-layer devices can be modeled using the series-parallel combination of resistors and capacitors shown in Fig. 3(b). The response of such a circuit to a ramp voltage is readily deduced. Assuming that $V_a = V_m.t/t_m$, where V_a is the voltage applied at time t, V_m and t_m the maximum amplitude and duration, respectively, of the ramp, the J-V characteristic can be determined analytically by solving the differential equation that describes the instantaneous current density, $j(t)$ through the device which is composed of a displacement current and a conduction current. Since current continuity must apply, $j(t)$ may be determined by considering the current flow through either of the parallel RC elements. Choosing the current flow through the oxide, we may write

FIG. 1. (a) Diagram of the device cross-section and quasi-static measurement circuit. (b) The set-up to record I-V curves at high voltage sweep rates. (c) A photograph of an encapsulated device containing a number of diodes.
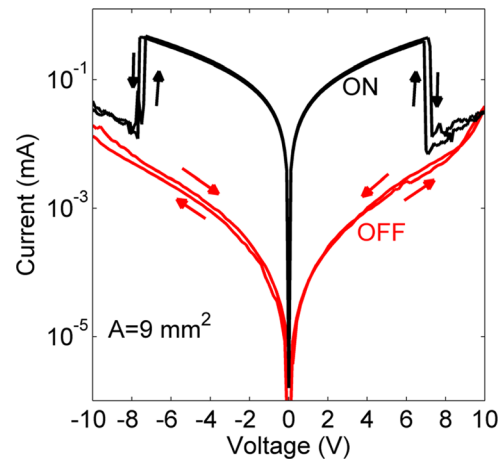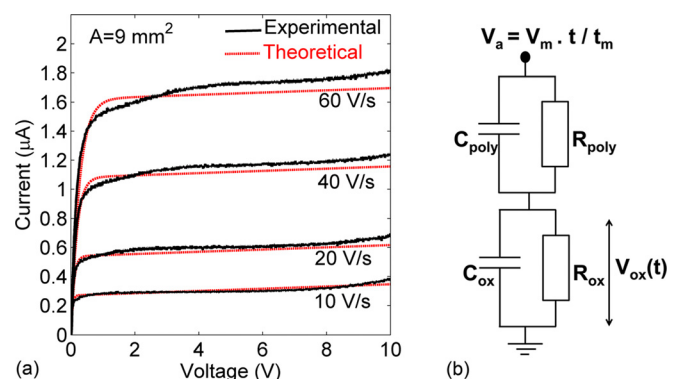

FIG. 3. (a) Experimental (black) and theoretical (red) I-V characteristics of an Al_2O_3/polyspirofluorene (PFO) bistable resistive switching diode obtained in the off-state for different voltage sweep rates. (b) The circuit used for modeling the device. The values giving the best fit to experiment were $R_{poly} = 14.4$ $K\Omega$ cm^2, $C_{poly} = 30$ nF/cm^2, $R_{ox} = 11.7$ $M\Omega$ cm^2, and $C_{ox} = 300$ nF/cm^2. The memory was electroformed at 12 V.

$$j(t) = C_{ox}\frac{dV_{ox}(t)}{dt} + \frac{V_{ox}(t)}{R_{ox}}, \tag{1}$$

where $V_{ox}(t)$ is the voltage appearing across the oxide layer, and is given by

$$V_{ox}(t) = \frac{\beta t}{\alpha} + \left(\frac{\alpha\kappa - \beta}{\alpha^2}\right)(1 - \exp - \alpha t). \tag{2}$$

Here $\alpha = \frac{R_{poly} + R_{ox}}{R_{poly}R_{ox}(C_{poly}+C_{ox})}$, $\beta = \frac{V_m}{t_m} \cdot \frac{1}{R_{poly}(C_{poly}+C_{ox})}$, and $\kappa = \beta C_{poly}R_{ox}$.

An excellent fit with experimental results is obtained for $R_{poly} = 14.4$ KΩ cm^2, $C_{poly} = 30$ nF/cm^2, $R_{ox} = 11.7$ MΩ cm^2, and $C_{ox} = 300$ nF/cm^2 with the oxide capacitance being confirmed in low-frequency measurements using an impedance analyser. Similar circuit parameters were found for the diode with 1 mm^2.

The currents in Fig. 3 are essentially capacitive displacement currents because of the relatively high ramp speeds used, which varied from 10 V/s up to 60 V/s. Conduction currents from turned-off filaments give rise to the slight slope in the saturation region and, therefore, are very small. The off-state in Fig. 2 was recorded at a voltage ramp speed of 0.1 V/s and is essentially dominated by the direct conduction.

B. Transient response in the on-state

We now turn to the on-state behavior as exemplified by Fig. 4. Here we see that, for increasing voltage scan speeds, both the device currents and the magnitude of the NDR gradually decrease: the latter disappears at a scan speed of 1000 V/s, in good agreement with literature reports.[10,17,18] Furthermore, the NDR behavior shifts to lower voltages upon increasing the scan speed. These results are counterintuitive. As seen in Fig. 3(a), increasing scan speeds should result in larger displacement currents. However, the on-state currents are orders of magnitude greater than the off-currents and, hence, dominate displacement currents. Nevertheless, we will argue that the internal capacitive structure of the
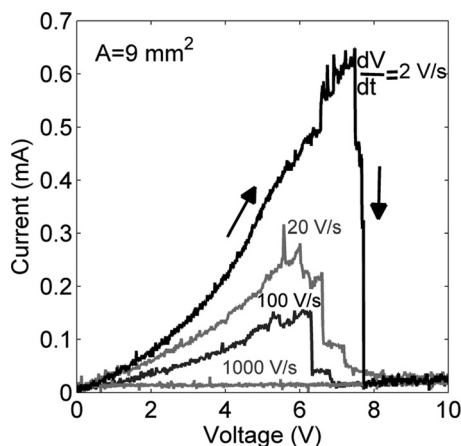
device still plays an important role in the behavior observed in Fig. 4.

First, we consider the nature of the on-current. We assume that the switching mechanism in these devices is physically located in the oxide layer and causes the opening and closing of micro-conducting paths across the oxide layer. A strong correlation has been established already between increased on-state currents and the appearance of local hot spots in the device.[13] We may assume, therefore, that the high on-state current flows through highly localised regions of the oxide and is likely to be filamentary in nature.[19] To represent the switching action of these local regions, an additional parallel branch must be added to the equivalent RC network and is shown in Fig. 5.

The localised switching region leading to NDR is presumed to occupy an almost insignificant fraction of the total device area. It is, however, connected to the formed (but non-conducting) region by the distributed resistance of the polymer film which we represent here by the dotted resistance connection. The switch S represents the mechanism giving rise to the NDR. When closed it connects the resistance R_F into the circuit to simulate a highly conducting path (or filament). When S is open, the normal oxide resistance is connected to the circuit and the micro-filament turns off. In a real device, a distribution of switches and corresponding low resistance paths exist.

Evidence for the existence of a distribution of such switches is provided by the noise measurements in Fig. 6 undertaken on a device in the on-state. With a constant voltage applied, fluctuations are observed in the current. The inset in Fig. 6 is an example for an applied voltage of 0.5 V. Here, we see that a general increase in current occurs as a result of relatively low-frequency step changes on which is superimposed high-frequency random telegraph signal (RTS) noise. Although, several mechanism can be proposed to explain the origin of such noise, on the basis of previous results[15,16,19] we suggest the high frequency RTS noise can be attributed to the fast turning on and off of micro-filaments. On the other hand, the low-frequency steps correspond to the switching on and

FIG. 4. Experimental *I-V* characteristics of the on-state of an Al$_2$O$_3$/polyspirofluorene memory as a function of scan speed. Both the onset voltage and magnitude of the NDR gradually decrease with increasing scan speed. At 1000 V/s the NDR is lost.
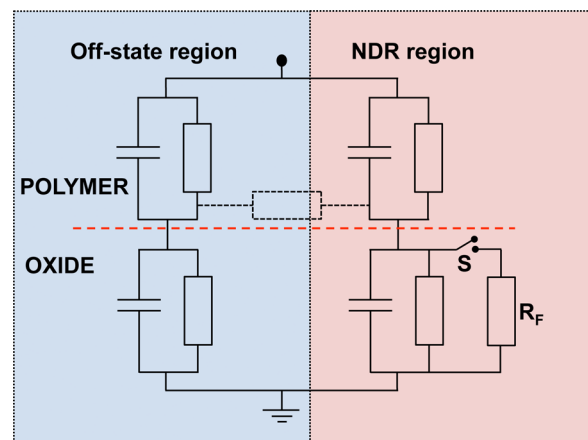

FIG. 5. Equivalent circuit representing a formed oxide/polymer diode in the on-state. The NDR branch is highly localised and connected to the formed (but off-state) region via the distributed resistance of the polymer layer represented by the dotted resistor. When the switch S is closed a conducting filament of resistance R$_F$ shunts the normally high local oxide resistance.
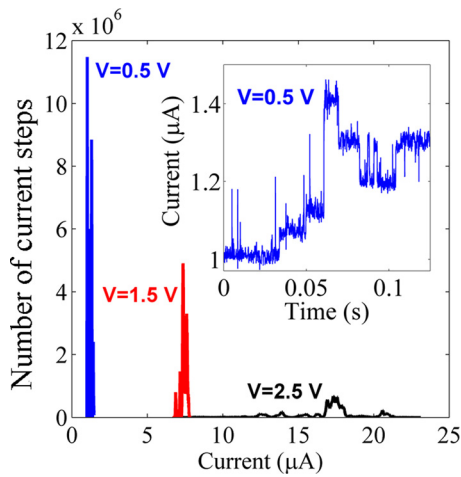
FIG. 6. Histogram showing the number of increasing and decreasing current steps. As the voltage increases, the number of steps reduces but their distribution becomes broader. The inset shows the current steps for a constant applied voltage of 0.5 V. The number of current steps was measured in a time interval of 0.1 s for all applied bias.

FIG. 8. Voltage dependence of the delay time for switching from off to on.

off of relatively long-lived conducting paths. In Fig. 6, both on and off current steps are represented. With increasing bias voltage, the number of current steps decreases and becomes broader, suggesting that at higher voltages a smaller number of highly conducting filaments are active, albeit of broader distribution.

The magnitude of the applied bias also determines the time required for a device in the off-state to be turned on, as shown in Fig. 7 where current is plotted as a function of time following the application of a step voltage. In this experiment, a high voltage (6 V) near the NDR region was first applied. The voltage was then reduced to zero for 3–5 minutes before applying a step of lower amplitude. This procedure was repeated with gradually reducing voltage steps down to 3.8 V. As seen, switching does not occur immediately upon applying the voltage. A so-called delay time, t_d, must elapse after voltage application before switching occurs. Furthermore, the lower the applied voltage, the longer the delay time before switching occurs; a phenomenon also reported by Wang *et al.*[20]

In Fig. 8, we show that the delay time, t_d, follows an exponential dependence on applied voltage according to the equation,

$$t_d = t_0 \exp(-\gamma V_a), \qquad (3)$$

where t_0 is a constant and γ a voltage acceleration factor. A good fit to the data is obtained for $t_0 = 4.77 \times 10^9$ s and $\gamma = 3.37$. Interestingly, the functional dependence of t_d on applied voltage is similar to that observed for the time-to-dielectric-breakdown observed in thin films such as SiO_2 since the late 1970s (Ref. 21) with $\gamma \sim 7.5$ for 5 nm thick films but asymptoting to lower values for thicker films.[22] This similarity suggests that the mechanism causing a change in the resistive state in an oxide-based RRAM is likely to arise from a breakdown mechanism ameliorated by the limiting resistance of the polymer layer, i.e., a form of soft breakdown.

The results in Fig. 8 clearly show that the magnitude of the applied voltage and the time for which it is applied play a crucial role in the switching process. It is important, then, to investigate the growth of the voltage, V_{ox}, dropped across the oxide layer for different applied voltage scan rates. This we may readily achieve using our double RC network and Eq. (2). The results are given in Fig. 9. In this figure, we used the Agilent ADS tool to simulate the response of the circuit utilising the resistance and capacitance values determined from the fit to the data in Fig. 3(a). Not surprisingly, we note that V_{ox} lags increasingly further behind the applied voltage as the scan rate increases. At 2 V/s, the voltage across the oxide reaches a maximum of 9.86 V when the applied voltage is 10 V, i.e., V_{ox} is practically the same as the external bias voltage. At 100 and 300 V/s, V_{ox} reaches 9.3 and 8.86 V, respectively. As the scan rate increases to 1000 V/s, now only 8 V appears across the oxide. It is clear, therefore, that increasing ramp speed reduces the fraction of the applied voltage appearing across the oxide. According to Fig. 7, the time required for the RRAM to switch to an on-state increases exponentially with decreasing voltage. This imposes a limitation, therefore, on the ability to switch. Some of the conducting micro-paths, once switched-off (in a previous scan) will not recover during the subsequent faster
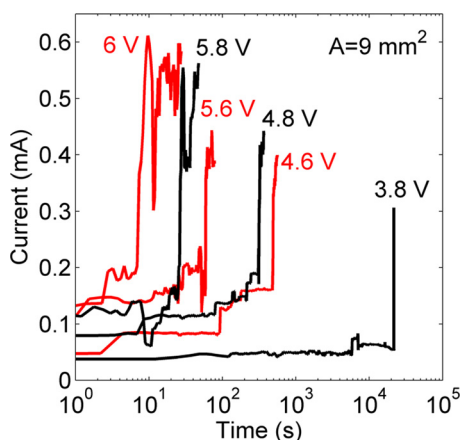

FIG. 7. Temporal evolution of current from the off- to on-state after applying voltage steps of different magnitudes. The experiment started from high to low bias.
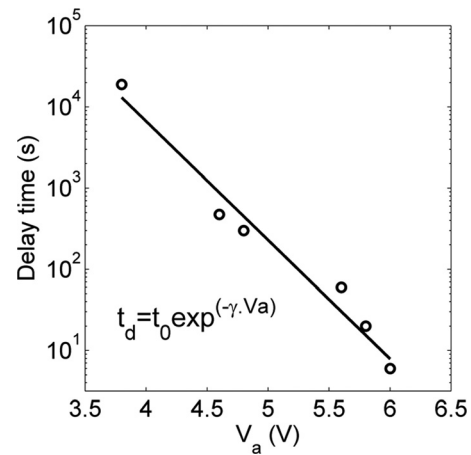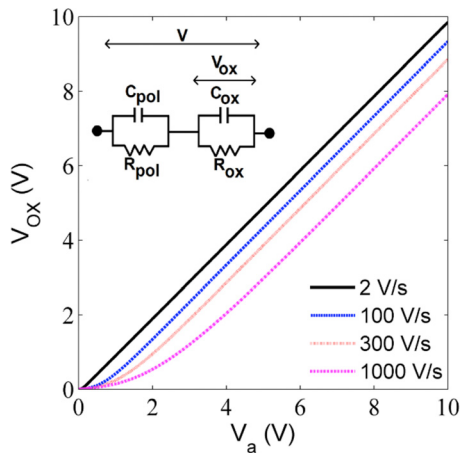
FIG. 9. The voltage dropped across the oxide layer, V_{ox}, plotted as a function of the applied voltage, V_a, for different voltage ramp rates. The calculations were based on the equivalent double RC network shown in the inset with the following parameters: $R_{poly} = 14.4$ KΩ cm^2, $C_{poly} = 30$ nF/cm^2, $R_{ox} = 11.7$ MΩ cm^2, and $C_{ox} = 300$ nF/cm^2.

FIG. 10. On-state *I-V* characteristics recorded at a fixed scan speed of 1000 V/s, with increasing external bias.

voltage ramp because the lower V_{ox} attained does not remain applied for a sufficiently long time to effect turn-on. In a real material, local differences in chemical structure, stoichiometry, defect density, morphology, and film thickness will create numerous micro-switching regions resulting in a wide distribution of turn-on voltages and turn-on times. Reported switching times vary by orders of magnitude with values ranging from nanoseconds to milliseconds.[23–29] As seen in Fig. 6, once programmed into the on-state, even low voltages trigger switching in low current capacity filaments, but still show a delay before the maximum current is achieved. Even in these more complex situations, by controlling the growth of V_{ox}, the internal device capacitances and resistances will determine which, and how many, local filaments switch on at a particular value of the applied voltage.

We now apply the above argument to the results in Fig. 4. At very low voltage scan rates, V_{ox} follows closely the applied voltage so that a large number of micro-switches will be triggered, composed of a wide distribution of current carrying capacity (Fig. 6). As the scan rate increases, the maximum V_{ox} attained decreases so that fewer switches, characterised by decreasing current magnitudes, will be activated. At sufficiently high scan rates, only low-voltage, low current switches will be activated so that the overall device current becomes dominated by the displacement current corresponding to the device in the off-state as observed in Fig. 3(a).

The model predicts that by sweeping the applied voltage to higher values, switching and NDR should be recovered and indeed this is the case. Fig. 10 shows experimental *J-V* characteristics obtained for a second diode at a constant ramp speed of 1000 V/s and recorded for increasing maximum applied voltages of 8, 9, 12, and 13.5 V. The NDR cannot be detected at 8 V, but is partially restored at 9 V and 12 V, and in the final sweep up to 13.5 V is clearly established. Hence, even at high scan speeds, the NDR and the ability to switch can be restored by successive voltage scans and enhanced as the maximum applied voltage increases. This suggests that the NDR observed in a particular curve must represent a cumulative response to the previous voltage
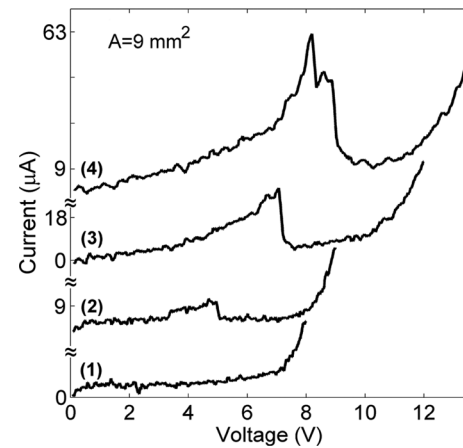
sweeps. Such behaviour is consistent with the accumulation during each sweep, and therefore over time, of a long-lived interfacial trapped charge,[16] a theme we return to in Sec. III C.

C. Scan-rate dependence of the NDR region

In Fig. 4, in addition to reducing the device current, higher scan rates also shift the NDR region to lower voltages. Previously, we have shown that during the electroforming process[16] deeply trapped electrons accumulate at the oxide/polymer interface. Interfacial electron trapping would also explain the cumulative effect of successive voltage sweeps in Fig. 10. There is considerable evidence amassing in reports by us[14–17,30] and others,[31] suggesting that the RRAM switches to a high conductive state when the defects in the oxide, probably oxygen vacancies, are filled with positive charges. When a percolation path of such defects becomes established across the oxide, a conductive filament is created. Positive charge trapped in the oxide is compensated by the electrons trapped at the polymer/oxide interface thus establishing a dipole layer. The resultant high electric field across the oxide primes the conduction path so that when a critical voltage is reached, electron tunnelling occurs through the defect.

In the NDR region, the switching off of conducting filaments is often accompanied by electroluminescence.[31–33] This is indicative of recombination, presumably of electrons from the polymer with holes trapped in defect centres in the oxide. Recombination will empty the oxide traps and the conductive path will switch off. Since the potential drop across a highly conductive filament will be low, we argue that recombination and hence the onset of NDR is controlled by the magnitude of the current flowing through the filament.

In the case of low on-currents, conducting filaments are well-separated from each other. Simple electrostatic simulations using COMSOL® (to be presented in a future publication) reveal a highly non-uniform potential distribution extending out from the filament to the electrode. Thus electrons may be drawn through the polymer from a relatively large area of the electrode. The critical filament current

required to effect efficient recombination and turn off the filaments is thus achieved at relatively low voltages.

For high on-currents, a large number of conducting paths are turned on, many will be in the neighbourhood of other filaments. COMSOL® simulations show that when the inter-filament distance is equivalent to the polymer film thickness or less, there is strong interaction between the potential disturbances caused by individual filaments. Now, the electrode area from which electrons are drawn does not increase in proportion to the number of neighbouring filaments. Higher voltages will be required then to provide the critical electron current flow from the electrode through the polymer in order to extinguish these filaments.

D. Implication for device design

An important outcome of the above findings is that the fundamental limitations on the speed of operation of the RRAM are the time- and voltage-dependences of the switch-on mechanism in the oxide and not the switch-off process. The physical mechanism responsible for this intrinsic limitation is likely to be the same, therefore, as in MIM devices and as such is not yet clear. However, we have demonstrated above that the switch-on time is further degraded by the internal capacitive structure of the device. The switch-on time can be reduced, therefore, by decreasing the intrinsic relaxation time of the device. This in turn will reduce the rise time for the growth of V_{ox}, the voltage across the oxide layer and may be achieved by minimising both the oxide capacitance and the polymer resistance. However, careful optimization will be required.

IV. CONCLUSIONS

Non-volatile, bistable resistive memories have been fabricated in the form of Al_2O_3/polymer diodes. In quasi-static measurements, the diodes display the well-reported negative differential resistance behavior and are readily switched reversibly between the off- and on-state. The responses of these diodes have been probed in both the off- and on-state using triangular voltage profiles with different scan rates. We have shown that the off-state response follows closely the predictions based on a classical, two-layer capacitor description of the device. Using this model, we have further shown that, at high voltage scan rates, the rate of rise of the voltage appearing across the oxide layer lags significantly behind the applied voltage. When coupled to the experimental finding that, switching events are characterised by a delay time determined by the magnitude of the applied voltage, the seemingly anomalous observation that the device current decreases with increasing voltage scan rate is readily explained.

Simple electrostatic simulations confirm that major changes occur in potential distribution and current flow patterns in the vicinity of an isolated conducting filament in the oxide. Assuming that a critical current must be achieved to turn off a conducting filament, we tentatively suggest that such changes in potential distribution are responsible for the shift in the onset of NDR to lower voltages as the number of conducting filaments decreases as occurs, for example, when the voltage scan rate increases.

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