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Study of trap states in zinc oxide (ZnO) thin films for electronic applications

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Abstract

The electrical properties of ZnO thin films grown by pulsed laser deposition were studied. Field-effect devices with a mobility reaching 1 cm^2/V s show non-linearities both in the current–voltage and in the transfer characteristics which are explained as due to the presence of trap states. These traps cause a reversible threshold voltage shift as revealed by low-frequency capacitance–voltage measurements in metal insulator semiconductor (MIS) capacitors. Thermal detrapping experiments in heterojunctions confirm the presence of a trap state located at 0.32 eV.

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1. Introduction

The electrical and optical properties of zinc oxide (ZnO) thin films are being studied for use in transparent electronics [1,2]. Fully transparent thin film transistor (TFT) devices [3–7] are particularly attractive because it is expected that their characteristics will not degrade under sunlight exposure due to the wide band gap. Besides, ZnO thin films can be grown in many different polycrystalline or nanoscale forms at relatively low deposition temperatures on diverse substrates.

Although electronics based on ZnO is promising, there are still many drawbacks that hinder a successful introduction into the market, namely the device stability in the presence of atmospheric agents and other undesirable effects caused by the presence of deep traps. The aim of this work is to study defect states and associated charges, both in the bulk and at the interface with other materials.

ZnO thin films were grown by pulsed laser deposition (PLD) on top of crystalline silicon substrates. Thermally oxidized silicon substrates were used for the fabrication of metal–insulator–semiconductor field-effect transistors (MISFETs) and MIS capacitors (see Fig. 1). Rectifying heterojunctions were built in highly doped n-type silicon substrates to perform thermal detrapping experiments (temperature stimulated current, TSC). The MISFET structures were used to estimate the field-effect carrier mobility and the capacitors were measured using small-signal impedance techniques to assess the interface states.

2. Experimental details

ZnO thin films were deposited by PLD [8] in a high vacuum deposition apparatus. A Q-switched Nd:YAG laser (at 1024 nm) was used to ablate the ZnO target (zinc powder purity 99.99%), with a pulse energy of 100 mJ and pulse duration of 5 ns at a frequency of 10 Hz. Thin films were grown at oxygen pressures of 10^{-3} mbar and 10^{-5} mbar.

Thin films ranging from 50 nm to 200 nm thick were deposited on top of silicon substrates consisting of a heavily

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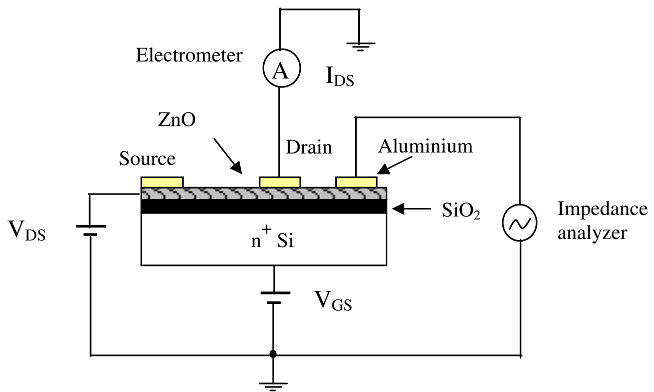

Fig. 1. Schematic diagram of the device structure.

n-doped silicon gate electrode coated with 680 nm thick (thermally grown) SiO_2 insulating layer. Aluminum metal electrodes were then deposited on top of the ZnO film by thermal evaporation through a shadow mask. The channel had a width (W) and a length (L) of 4000 μm and 200 μm, respectively. For the heterostructure, the ZnO was deposited on top of the n-doped silicon.

3. Results

3.1. Transistor characteristics

The thin film transistors (TFT) used in this study exhibit good electrical characteristics, with a low off current, a field-effect mobility of 1.13 cm^2/Vs and modulation ratio $\sim 10^4$. The I_{DS}–V_{DS} curves (see Fig. 2(a)) exhibit n-channel operation, current saturation and negligible non-linearities in the linear region. The transistor can be normally-on when the ZnO film thickness is high (>100 nm). When comparing these characteristics with other ZnO data in the literature it is important to note that the dielectric thickness used (680 nm) is unusually high. If a typical 200 nm thick dielectric was used instead, we expect to reach a similar current modulation with only a gate bias of 18 V.

As in many other materials, the transistor transfer characteristics are non-linear in a linear plot, therefore, it is difficult to obtain a unique slope and intercept from which the mobility (μ) and the threshold voltage (V_{th}) can be extracted. This problem is well known and has been addressed in a-Si TFT technology [9] as well as in organic based devices [10,11].

This behavior occurs when there is a large density of traps compared to the density of free carriers [11]. Particular care is then needed when one has to estimate values for the mobility. Usually it is considered that the parametric field-effect mobility (μ_{FET}) increases with the gate voltage as $\mu_{FET} \propto (V_{GS}–V_{th})^{\gamma}$ where V_{GS} is the gate-source voltage and γ_0 is an empirical parameters defining the variation of the mobility with V_{GS}.

The drain current in the linear region, *i.e.*, for small drain voltage and for $V_{GS} > V_{th}$ is then given by

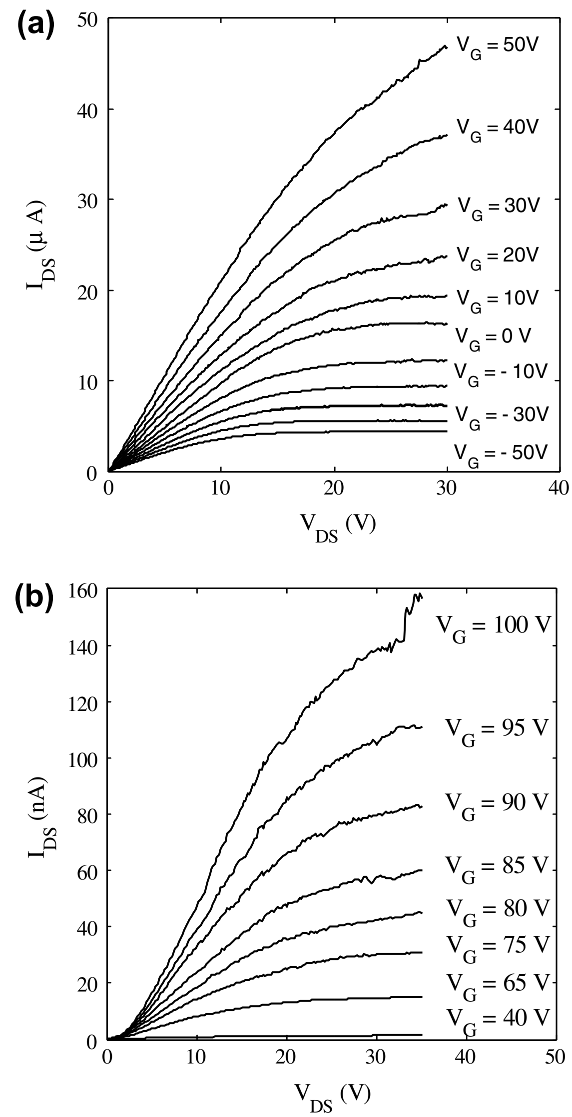

Fig. 2. Transistor current–voltage characteristics (a) when the ZnO film was grown under relatively oxygen (base pressure of 10^{-3} mbar) and (b) showing supra-linear behavior for small V_{DS} when the ZnO thin film was grown under low oxygen atmosphere (base pressure 10^{-5} mbar).

$$I_{DS} = k(V_{GS} - V_{th})^{1+\gamma} V_{DS}$$

with $k = \mu_0 C_{OX} W/L$, μ_0 is an empirical parameter, C_{OX} is the oxide capacitance per unit area and V_{th} the threshold voltage. The linear transfer curves plotted as $I_{DS}^{1/(1+\gamma)}$ give straight lines. Fig. 3 shows the transfer characteristics for $\gamma = 1.5$. Two clear straight lines are then obtained.

The TFTs characteristics strongly depend on the oxygen content during deposition. Fig. 2(b) shows I_{DS}–V_{DS} curves for a ZnO TFT grown under low oxygen concentration. The lower the oxygen content during deposition, the smaller the current. Furthermore, the curves become clearly supra-linear for small V_{DS}, phenomena often called 'contact effects', however, non-linearities are also readily explained by assuming a Poole and Frenkel field assisted thermal excitation from abundant deep levels [11].

As a summary, ZnO TFTs characteristics exhibit non-linearities, both in the I–V and the transfer characteristics,

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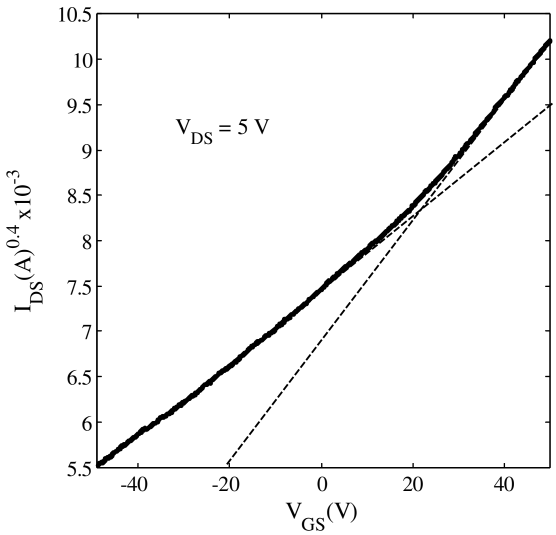

Fig. 3. Linear transfer curves for $V_{DS} = 5$ V and plotted as $I_{DS}^{1/(1+\gamma)}$ for $\gamma = 1.5$. The dashed lines are guides to the eye.

both effects are known to be caused by the presence of abundant deep localized levels.

To obtain more information about the establishment of the accumulation channel as well as charges trapped at the ZnO/silicon interface, capacitance–voltage (*C–V*) measurements were carried out in MIS capacitors. Fig. 4 shows a low-frequency *C–V* measurement. When the voltage is swept across the MIS capacitor, the semiconductor surface goes through accumulation to depletion and eventually to inversion. The central region of the *C–V* curve, where the capacitance changes rapidly with the gate voltage, are the depletion and inversion regions. The capacitance decreases until the depletion width reaches a maximum and inversion sets in. Inversion forms a layer of minority carriers (holes in this case). The inversion region should disappear as the frequency increases, typically a few Hz in silicon based devices. It is peculiar that the inversion plateau at high positive bias (see Fig. 4) is capable of responding to ac signals with a frequency as high as 8 kHz. The *C–V* plot also shows substantial hysteresis, with a lateral shift along the voltage axis. This indicates the presence of interface states which are charged as the device is driven into depletion and discharged when in inversion, causing a large threshold voltage shift of nearly 4 V. This threshold voltage shift is fully reversible.

3.2. Thermal detrapping currents

Physical properties of charge carrier traps in semiconductors are usually studied by thermally stimulated current (TSC) techniques. In TSC experiments the traps are filled by the bias when cooling down to low temperature. Upon heating, the trapped carriers are released to the appropriate band and there is an increase in the free carrier density. The amount of trapped charge is finite, being limited by the number of traps, and as the temperature is increased further, all the trapped carriers are eventually released. There is a peak in a plot of the current change as a function of temperature. The temperature at which this peak occurs is related to the energy level of the trap and the area under the peak is related to the trap concentration.

The TSC experiments were performed in a heterojunction device. These structures exhibit rectifying *I–V* characteristics, the current is higher for positive bias applied to the aluminum electrode. Charging of the traps was performed by application of a forward bias (3 V) at a temperature of 320 K. The device was then cooled down to 150 K, while keeping the bias on. At low temperatures the bias was

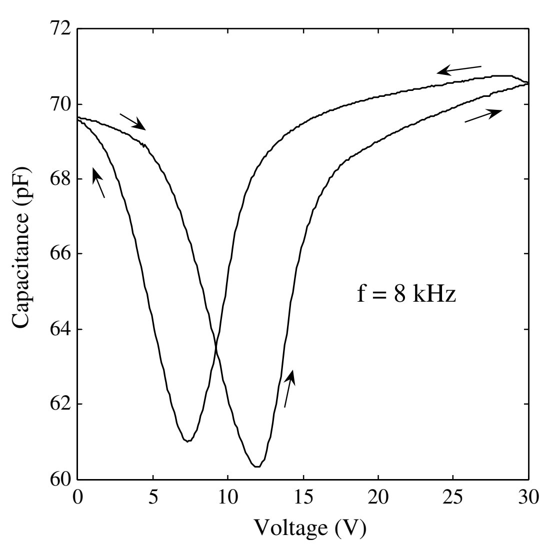

Fig. 4. Low-frequency capacitance–voltage measurement carried out in an MIS capacitor.

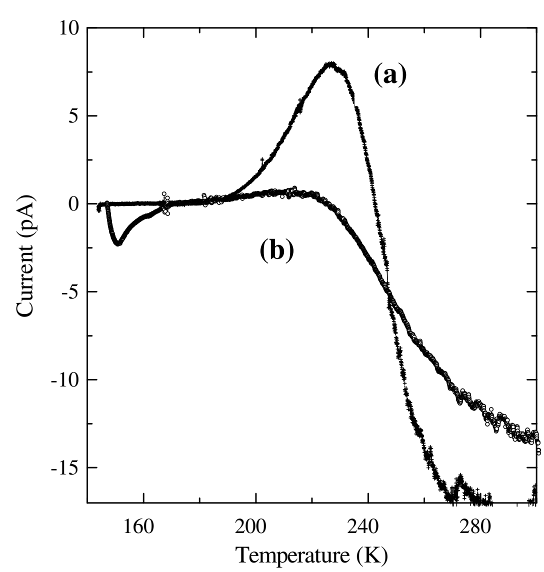

Fig. 5. Experimental TSC curve (a) obtained in a heterojunction structure after applying a forward bias of 3 V while cooling (trap-filling procedure) and (b) without trap filing. The TSC peak at 235 K is caused by a detrapping current. The heating rate was 2 K/min.

removed, the terminals connected to a picoammeter, and the device heated with a well-defined heating rate. Fig. 5 shows a TSC curve compared with a base-line curve measured without trap-filling bias. Only the peak structure appearing at 235 K can thus be assigned to the trap-filling process. The experimental TSC curves can be analyzed by the initial rise method [12]. This analysis is based on the assumption that, the TSC is proportional to $\exp(-E_t/k_BT)$ when traps begin to empty with temperature, where E_t is the energy of the trap in the band gap, k_B is the Boltzmann constant and T the temperature. Thus, a semi-logarithmic plot of the current versus $1/T$ gives a straight line with a slope of $(-E_t/k_B)$. On the basis of our experimental TSCs curves we obtain a trap depth of 0.32 eV. In principle, the trap density can be estimated from the area under the TSC curve. However, there are clear evidences for strong re-trapping above a temperature of 240 K, the re-trapping distorts the curve and makes trap density estimation unreliable.

4. Conclusions

The electrical characterization of ZnO thin films in metal insulator semiconductor structures has revealed that traps are strongly affecting the electrical characteristics. Particular care is then needed in the interpretation of the TFT parameters and the use of conventional models to extract device parameters such as the field-effect mobility.

The oxygen content during ZnO deposition by PLD has a remarkable effect on the thin film conductivity by changing the trap density. TFT devices deposited under high oxygen content (base pressure 10^{-3} mbar) have higher current densities and they behave as normally-on devices. Devices deposited under low oxygen content (base pressure 10^{-5} mbar) exhibit non-linear I–V and transfer characteristics, behavior typical of devices having a large density of trap states.

The experimental findings reported here suggest that the lack of oxygen during the growth conditions creates more defects. The field-effect mobility is also substantially decreased because of a large density of traps. Thermal detrapping experiments have revealed that the traps are relatively shallow and located at 0.32 eV from the conduction band edge. According to the literature [3], the two most common defects in ZnO thin films are oxygen vacancies and zinc interstitials. In oxygen rich growth conditions zinc vacancies dominate [3]. Further studies are needed to clarify the nature of these defects at 0.32 eV and their relation with the growth conditions.

Acknowledgments

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