EPJ Photovoltaics **15**, 11 (2024)
© A. Lachowicz et al., Published by EDP Sciences, 2024
https://doi.org/10.1051/epjpv/2024008

EPJ Photovoltaics

Available online at:
www.epj-pv.org

Special Issue on 'EU PVSEC 2023: State of the Art and Developments in Photovoltaics', edited by Robert Kenny and João Serra

ORIGINAL ARTICLE   OPEN ACCESS

Aging tests of mini-modules with copper-plated heterojunction solar cells and pattern-transfer-printing of copper paste

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Received: 28 September 2023 / Accepted: 24 January 2024

Abstract: Mini-module aging tests with differently interconnected heterojunction solar cells having industrially viable copper metallization are presented. The plating process comprises 3 steps: firstly, screen printing of a seed-grid layout using a copper-based paste, followed by deposition of a dielectric layer over the entire wafer surface, and finally, selective copper electrodeposition on grid positions. Modules with Smartwire interconnection, fabricated with M6 half-cells, are stable in extended TC and PID tests. DH degradation is at 5% after 2700 h (glass-glass modules without edge sealing). Shingle modules, realized in collaboration with CEA INES and AMAT, exhibit notably higher fill factor compared to reference modules with screen-printed silver paste. This improvement is attributed to the superior line conductivity achieved with plated copper. TC stability of shingle modules is very good, whereas after 2000 h damp-heat aging more than 2% loss in fill factor is observed. Using pattern-transfer-printing technology narrow, high aspect-ratio lines have been obtained: with a seed-grid of pure copper paste, reinforced with electrodeposited copper. Line dimensions and line resistance as well as first cell results are presented.

Keywords: Heterojunction solar cells / copper metallization / plating / module stability / pattern transfer printing / electrodeposition

1 Introduction

The substitution of silver with copper is considered a pivotal step in enabling the large-scale production of PV while continuously driving down costs [1]. The heterojunction structure offers a significant advantage when it comes to copper plating. This advantage arises from the absence of a direct contact between the metal and the silicon, and the presence of transparent conductive oxide (TCO), which is an excellent barrier against copper diffusion [2,3].

Although copper is substantially more cost-effective than silver, its application is not as straightforward as conventional screen printing. The complexity of the process must be factored in, as each additional step adds to the overall cost. Several processing routes for copper-plated metallization on heterojunction cells have been developed [4], with some even implemented in production [5,6]. Regrettably, these methods didn't endure in the long run. The competition with screen printing persists, as silver consumption per watt-peak —and thus the cost—continues to decline. Additionally, the recent introduction of silver-coated-copper paste and its seamless integration into the production of heterojunction cells have alleviated the need for the immediate introduction of new processes [7].

The three-step plating process involves screen printing and the deposition of a dielectric layer as plating mask (usually by PECVD), both of which are well-established and proven techniques in solar cell manufacturing. Furthermore, the application of a dielectric layer is part of two strategies to reduce indium consumption: (i) creating a stack of thin indium tin oxide (ITO ≤ 30 nm) and a dielectric layer to form an antireflective coating and (ii) adding a dielectric layer on top of aluminum zinc oxide (AZO) to ensure good module stability [8,9]. Just the plating step itself is new to solar cell manufacturers.

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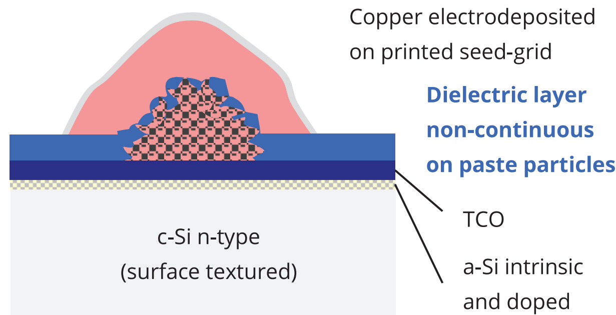

Fig. 1. Contact structure resulting from the 3-step process: with thin TCO, dielectric layer, seed-grid of copper particle paste, electrodeposited copper, and capping layer.

2 Plating process

The key for selectivity is that the dielectric layer is not continuous on a line consisting of particles, while it tightly covers the transparent conductive oxide in between the printed grid (Fig. 1). Current for electrodeposition is applied by contacting the printed grid and passes through the voids in the dielectric on top of the paste, resulting in selective copper deposition on grid positions. However, both the paste and the dielectric layer need to be carefully chosen. The formation of voids is more likely to be induced by the presence of larger particles and more directional deposition method for the dielectric, such as plasma-enhanced chemical vapor deposition (PECVD) rather than thermal atomic layer deposition (ALD).

The requirement on seed-grid conductivity is not high. It has to transport the current for electrodeposition, typically in the range of 10–20% of the photogenerated current in the final cell. Remarkably, uniform plating over the wafer surface has been observed even on a seed-grid of pure copper paste, with line resistivity close to 100 Ω/cm. Depending on the paste and on plating conditions copper is deposited not only on the surface of the lines but also in between the paste particles. More details about the process are available in reference [10].

Pure copper paste is still in development by the suppliers for screen printing of narrow lines without interruptions. In the interim, we have used silver-coated-copper paste (SCC) for seed-grid formation and obtained lines of about 30 μm width using knotless screens. The best cell result with SCC seed-grid, PECVD dielectric layer, and electrodeposited copper on a high quality industrial M6 precursors is at 24.2% (bifacial cell with 9 busbar-layout, internal measurement) [10].

3 Smartwire modules

Glass–glass modules with one M6 half-cell were fabricated using wires with In-free low melting point alloy and with polyolefin encapsulant. The cells were prepared on M6 external industrial heterojunction cell precursors with standard ITO, either with screen-printed silver-coated-copper paste only or with additional PECVD dielectric layer, electrodeposited copper and capping layer (on the same SCC seed-grid).

All modules exhibited excellent stability in thermocycling (TC), with minor degradation after 690 cycles: −1.4% for the SCC reference and −0.2% for modules with copper (see Fig. 2). In damp-heat (DH) strong degradation of modules with silver-coated-copper paste only was observed, mainly in fill factor. This particular paste had not been previously tested with materials used in this experiment. In general, the stability of commercial SCC pastes in DH is good, confirmed even by the industry through the fast implementation of this paste type in production [7].

Degradation of modules with copper, and probably more important in this case, with a dielectric layer, was significantly reduced and at 5% after 2700 h.

In electroluminescence images (EL, Fig. 3) we observe the onset of degradation at cell edges closest to the unsealed module edge. Such small modules may represent the hardest condition for DH testing due to their high ratio of perimeter to module area, resulting in increased moisture ingress per cell area. For the next module experiment the application of an edge sealant is planned. Edge sealing with polyisobutylene is used in commercial heterojunction modules to improve the stability in damp-heat [11].

Modules after storage and after TC were further subjected to potential induced degradation (PID). The testing was conducted under standard conditions: 85 °C and 85% rel. humidity and an applied potential of either +1000 or −1000 V. All modules have withstood two 96-h testing cycles, without any deterioration.

4 Shingle modules

The shingle pattern consists of separate tiles of 25 mm width. The effective current path on the cell is significantly longer than for multi-busbar configuration, comparable rather to a 3-busbar-cell, and thus lower fill factors are achieved, despite of the high amount of silver generally deposited on such devices [12]. Furthermore, the current transport in the module occurs entirely through the fingers. Copper metallization is therefore particularly interesting for shingle interconnection.

The modules were realized in collaboration with CEA INES and AMAT. Heterojunction M2 precursors were manufactured in the CEA INES pilot-line, incorporating amorphous silicon and standard ITO layers on both sides. A seed-grid was then printed using silver low-temperature paste and in standard six-shingle layout.

In this experiment, lines of ~60 μm width were printed with significantly reduced silver paste consumption than usual (single print, lower line aspect ratio targeted: reduction of ~1/3 of paste deposit) because of the planned subsequent reinforcement with electrodeposited copper. Cells with initial efficiencies at 22.5% (fill factor in the 80.5% range) were fabricated. After deposition of the dielectric layer and copper plating at CSEM, the line conductivity and, consequently, the fill factor were significantly improved, resulting in an overall higher efficiency of 22.9% (group mean value).

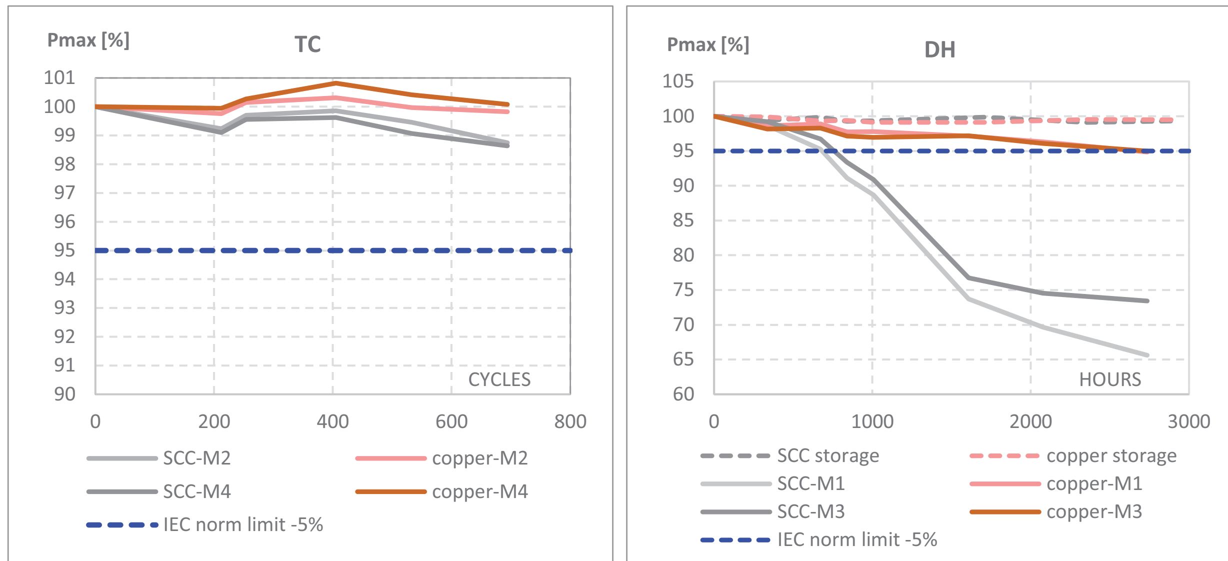

Fig. 2. Smartwire module power decrease after TC (on the left) and DH (on the right). Grey lines represent modules with silver-coated copper paste only, orange/brown lines modules with copper, dashed lines represent control modules only stored in the laboratory.

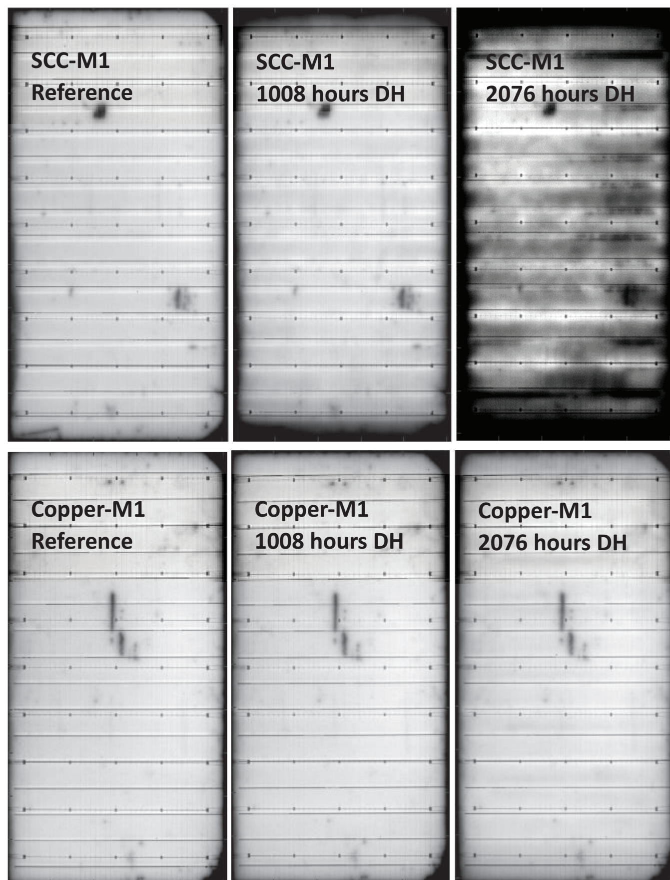

Fig. 3. EL images of modules with Smartwire interconnection in damp-heat test. Top row: module with silver-coated-copper paste only, at test start (“Reference”), after 1008 and after 2076 h. Bottom row: with additional dielectric layer and plated copper, at test start (“Reference”), after 1008 and after 2076 h.

The shingling process was performed on an automatic tool developed at Applied Materials, suitable for production as well as for small strings processing. The HJT cells were scribed with a 100 W nanosecond IR laser to approximately half of the thickness and subsequently mechanically separated. About 3.5 mg electrically conductive adhesive were applied per shingle by screen printing and six shingles per string were then automatically aligned with an offset of 1 mm and cured at 150 °C. The final module lamination was conducted at CEA INES, with polyolefin encapsulant and in glass-glass configuration (without edge sealing).

The stability in TC is very good, with less than 0.5% change in power after 400 cycles. A significant decline in fill factor, exceeding 2%, is observed after 2000 h damp-heat testing. EL images confirm that degradation initiates at the module’s edges (Fig. 4). Application of edge sealing is considered for future modules.

5 Pattern-transfer-printing technology (PTP)

The PTP process involves two stages: first, filling of trenches in a transparent film and then transferring the paste using a laser. A metal blade pushes the paste into the trenches and simultaneously cleans excess paste from the surface in between the trenches. The film is then positioned above the wafer with a small gap (non-contact printing), and the filled trenches are scanned by a continuous-wave infrared high-power laser that drives the paste out of the trenches, resulting in the deposition of an entire line onto the wafer. The laser transfer takes less than 1 s per M10 wafer (per side).

In Figure 5, lines obtained from trapezoid-shaped trenches and using either SCC or copper paste are shown. The line width is approximately 20 μm after PTP and

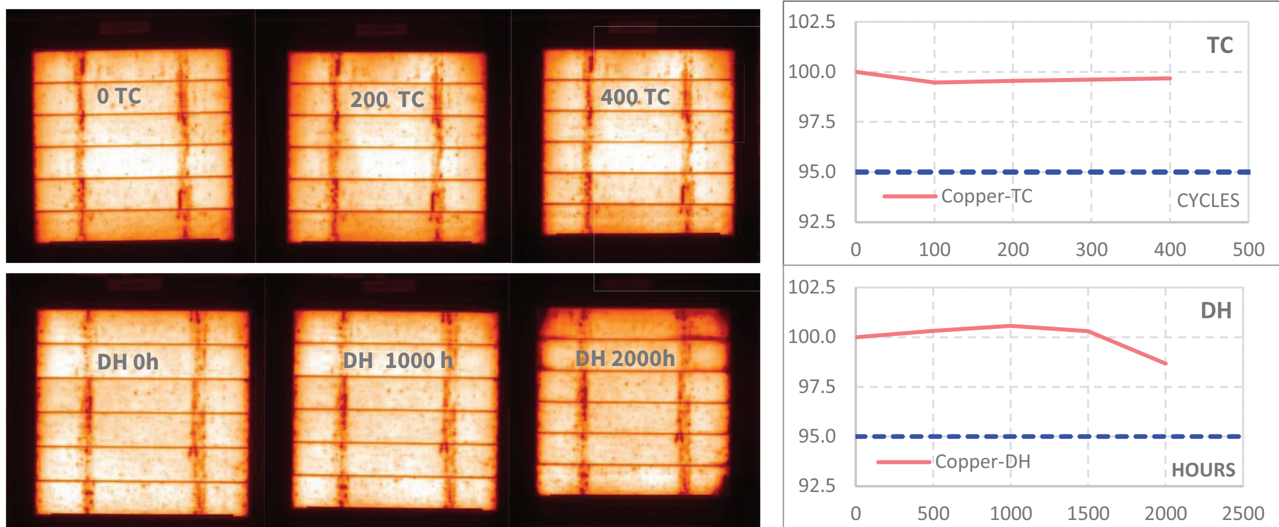

Fig. 4. EL images of shingle modules after TC (top row) and DH (bottom row) testing and corresponding Pmax degradation diagrams. The vertical lines are traces of transport belts in the cell pilot line.

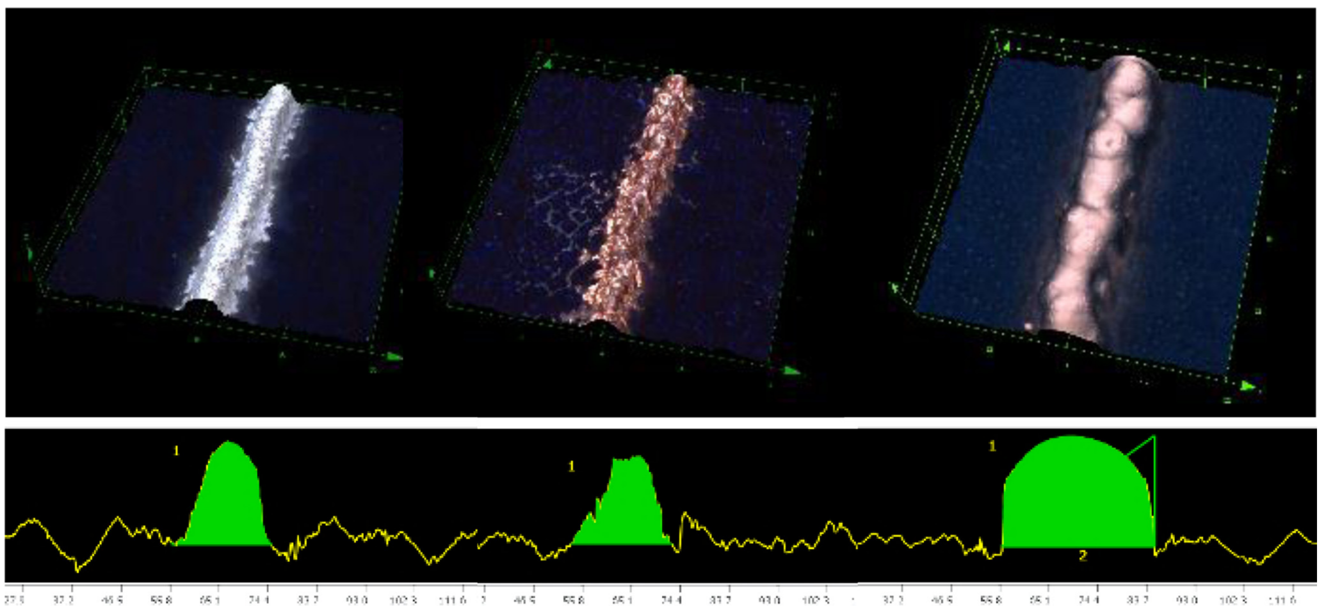

Fig. 5. Confocal microscope images of PTP lines and corresponding profiles. On the left: silver-coated-copper paste, center: copper paste, right: electrodeposited copper on copper paste.

25 µm with electrodeposited copper. All line dimension values and line resistance are given in Table 1. Line resistance measurements were conducted using Kelvin probes directly on the cell layout, on pads intended as contacting areas for plating (placed on busbars, distance 26 mm).

Figure 6 illustrates an ion beam cross-section of a line that has copper plated on copper paste, along with an EDX material analysis. This line consists solely of copper and organic material from the paste. Line dimensions, as determined through scanning electron microscopy (SEM) of the cross-section, are 26.1 µm in width and 21.9 µm in height.

The contact resistivity of the copper paste on indium thin oxide is at 1.5 $m\Omega \cdot cm^2$. This value has been determined with screen-printed TLM pattern.

At the time of the experiment, the laboratory equipment at DR Utilight could handle only M2 precursors. Therefore, older industrial HJT precursors were used for this test. SCC or copper paste from Namics were printed on the front side.

Table 1. Line dimensions (obtained from confocal microscope), cross sectional area, and line resistance measurement after pattern transfer printing and after copper plating on Cu paste.

Line	Unit	SCC paste	Cu paste	Cu paste + plated Cu
Width	μm	18.9	21.5	25.0
Height	μm	10.3	9.3	17.6
CS area	μm^2	116	102	335
Resistance	Ω	1.5	5.1	0.2

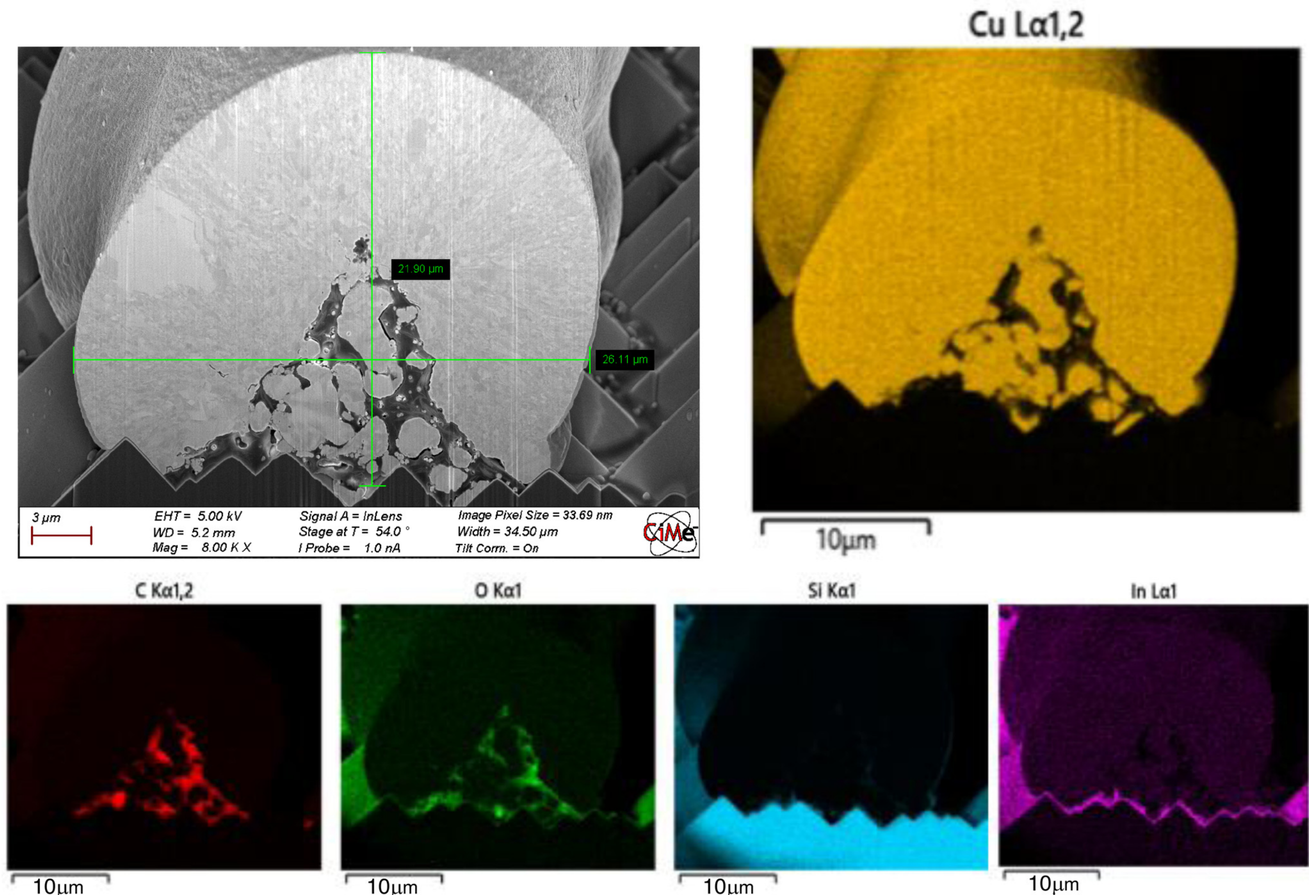

Fig. 6. SEM image of an ion beam cross section and EDX element maps of a line with copper plated on copper paste. Line dimensions measured on the cross section: width 26.1 μm, height 21.9 μm.

Both pastes underwent identical thermal treatment: at 200 °C and in air (on a hot plate). For cell evaluation additional back fingers and busbars, including contacting pads, were screen-printed at CSEM, all with SCC paste. Drying and curing were done in a belt oven.

All the thermal treatments led to significant oxidation of the copper paste surface and the pretreatment before copper electrodeposition, specifically the deoxidation step, had to be modified to ensure complete removal of the oxide.

The cell IV values are shown in Figure 7. The result with SCC paste, with 80.2% fill factor and 22.5% efficiency, aligns with expectation for these precursors, i.e., is comparable with the performance of cells with screen-printed silver or SCC paste. The extremely low fill factor observed with copper paste alone can be attributed to its high line resistivity. However, when copper was electrodeposited onto the copper paste, values close to the SCC reference were achieved. The diagram shows the results of only the three best plated cells that underwent the modified deoxidation step.

Process optimization is ongoing, mainly focused on the pretreatment, in order to further improve fill factor and overall cell efficiency. DR Utilight has upgraded its laboratory equipment, and the upcoming experiment will utilize M10 precursors.

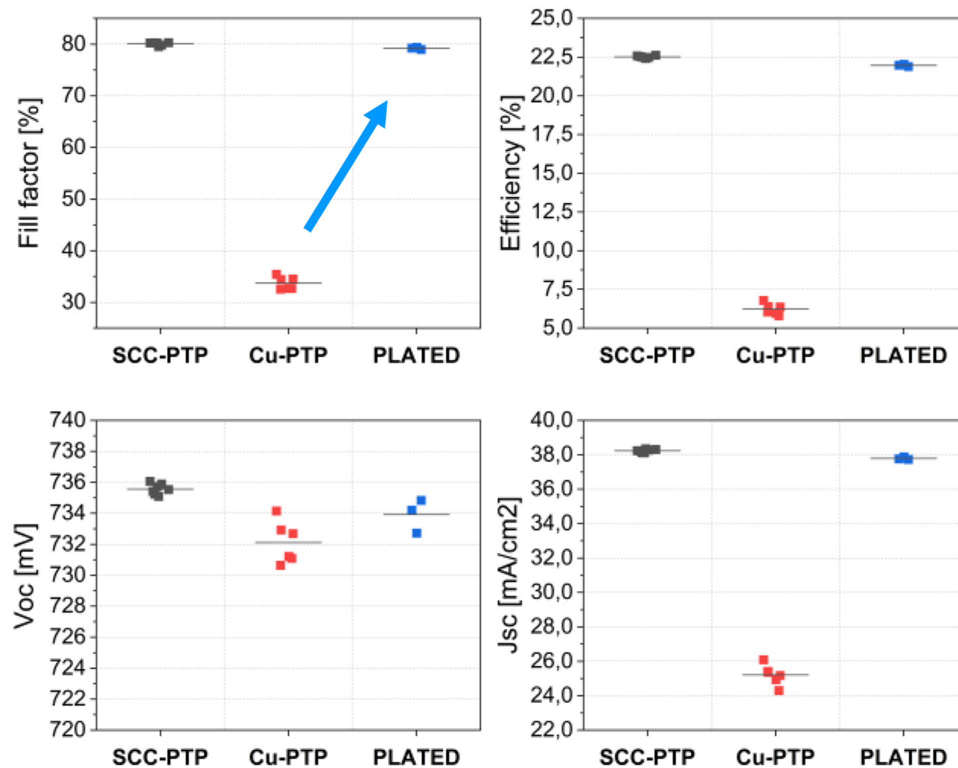

Fig. 7. IV measurement of M2 cells with silver-coated-copper paste (SCC-PTP), copper paste (Cu-PTP) or with copper electrodeposited on copper paste (PLATED).

6 Summary

The process has several advantages: firstly, it comprises only three steps, of which printing is already part of the production. Even a pure copper paste can be used for seed-grid formation because it only needs to conduct a small current for electrodeposition. Once some copper is electrodeposited, the transport occurs through this highly conductive layer. The presence of a dielectric layer enables the use of thin ITO, leading to a reduction in indium consumption; moreover, it is beneficial for module stability [13]. There is no material waste: all deposited materials are integral parts of the final cell. Consequently, there is no need for additional steps to remove or etch material.

Very good module stability in thermocycling has been confirmed for both Smartwire and shingle interconnection. DH heat stability is to improve. Edge sealing is planned for the next modules to enhance the resistance to damp-heat. Laser pattern transfer enables printing of narrow and high aspect ratio all-copper lines. Higher efficiency is still to demonstrate on larger industrial precursors and module stability to reevaluate with new pastes and materials. Overall, the process seems to be industrially feasible, with electrodeposition being the only unconventional step in solar cell manufacturing.

Remarkably, several HJT manufacturers have already established pilot production with copper plating. New plating lines have been developed for these companies and their specific processes, partially by equipment suppliers being new in this field or even by start-ups [14–16]. Also, the interest in plating on Topcon cells is high [17]. Given the considerable activity in the industry, it appears that plating, after more than three decades of development and production trials, may finally be on the path toward broad implementation in solar cell manufacturing. The trend seems to be progressing, even without a highly urgent need to completely eliminate silver.

Acknowledgments

We thank the company Namics Corp. for providing us copper paste and the companies Atotech, Dupont and Sytron for plating chemistry. We also thank Lucie Navratilova from EPFL CiME laboratory for ion beam cross sections, SEM pictures and EDX analysis.

Funding

This work has been partially carried out within the European projects HighLite (GA 857793) and Resilex (GA 101058583).

Conflicts of interest

The authors have nothing to disclose.

Data availability statement

This article has no associated data generated and/or analyzed.

Author contribution statement

Agata Lachowicz: coordination, writing, plating process; Nicolas Badel: screen printing, module manufacturing; Alexis Barrou: module manufacturing, aging tests, data evaluation; Vincent Barth and Samuel Harrison: contribution shingles and shingle modules aging tests, Marco Galliazzo and Nicola Frasson: contribution shingle separation and stringing; Natali Cohen and Eyal Cohen: contribution pattern transfer printing; Jun Zhao, Betrand Paviet-Salomon and Christophe Ballif: support and review.

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Cite this article as: Agata Lachowicz, Nicolas Badel, Alexis Barrou, Vincent Barth, Samuel Harrison, Nicola Frasson, Marco Galiazzo, Natali Cohen, Eyal Cohen, Jun Zhao, Bertrand Paviet-Salomon, Christophe Ballif, Aging tests of mini-modules with copper-plated heterojunction solar cells and pattern-transfer-printing of copper paste, EPJ Photovoltaics **15**, 11 (2024)