AC-Voltage Harmonic Control for Stand-Alone and Weak-Grid-Tied Converter

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***Abstract*—This paper presents an ac voltage controller that can operate under a wide range of loads thanks to its high robustness to plant model variations. A robust voltage controller is required in a droop-controlled inverter that operates connected to a grid or in island mode with other generators. In such modes of operation, the voltage source converter (VSC) can experience large load impedance variations depending on the number of parallel generators or the grid impedance value. Concerning the controller performance, the transient response is improved by selectively minimizing the output impedance of the system at the frequencies that typically contain the largest components of the output current. Complete harmonic control is achieved due to its zero output impedance at a set of design-selected frequencies. The proposed controller only measures the output voltage, and it contains a single-loop structure that uses all available bandwidth. In addition, a fast converter-current estimator provides protection against a fault and inrush output currents. The design process only requires, as input parameters, the LC filter values, the sampling frequency, and a set of harmonics where load-current circulation is expected.**

***Index Terms*—Voltage control, LC filter, parameter sensitivity, resonant controller (RCs), power converter.**

I. Introduction

THE ac voltage controller is an essential component of a power converter that operates in island mode [1] or connected to a micro grid (MG) using a droop control [2]–[6], specially when there is a large integration of renewable energy sources within the MG [7].

In order to regulate the ac voltage, power converters commonly use a double-loop [8]–[17] or a single-loop controller [18]–[23]. On the one hand, double-loop structures provide a stable system using simple (low-order) proportional-integral (PI) or proportional-resonant (PR) controllers because they divide a complex plant model into two parts. An inner current loop simplifies the plant model seen by the voltage controller. The inner current controller assumes the plant is an L filter, whereas the outer voltage loop mainly sees a capacitive plant in the low frequency range where it operates. Typically, the bandwidth of the current controller is larger than the bandwidth of the voltage controller so as to avoid interaction between both loops. Nevertheless, such extra bandwidth of the current controller does not provide any improvements to the system performance besides the desired decoupling between controllers [10]. Actually, the output impedance of the system augments when the bandwidth of the current loop increases [11], as expected from the fact that good current sources have a high output impedance. Furthermore, double loop controllers have stability problems when controlling frequency components close or above the critical frequency ($f_s/6$), where f_s denotes the sampling frequency [1]. On the other hand, single loop structures with classical transfer-function-based controllers [19] offer a simple design process. Nevertheless, they lack the flexibility, modularity and robustness to parameter variations of double-loop controllers [24]. Moreover, they may need to measure additional variables, such as the capacitor current to achieve stability [18], or the converter current for protection against a short circuit or inrush currents [12]. In particular, single-loop control cannot stabilize the system when the resonant frequency of the LC filter is less than one fourth of the sampling frequency [13].

Concerning the type of controller, transfer-function-based solutions are commonly adopted in the literature. On the one hand, the voltage loop typically contains PR or synchronous-reference-frame (SRF)-PI controllers in order to achieve zero steady-state error in the output voltage at the fundamental frequency and at the main low-order harmonics [18], [25]. On the other hand, the current loop usually comprises a simple P controller [10] so as to reach a high bandwidth, which results in sufficient decoupling between the two loops. Nevertheless, these solutions do not optimize the performance of the voltage controller in terms of the achievable bandwidth or the robustness against a large variation in the load impedance, in particular when the resonant frequency of the LCL filter is above the critical frequency [1].

Contrarily to these solutions from classical control theory, state-space controllers from modern control theory have proven to have a high robustness [14], [21], [22], [26]. Such robustness is convenient during grid-connected mode [15] or during parallel operation [20], [27], because the converter sees a low load impedance, which is the parallel equivalent of the load impedance and the coupling impedance. The voltage controller presented in [22] incorporates an integral action to

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remove steady-state error at the fundamental output frequency. In [21], a voltage controller is designed using a pole-placement technique. Such design [21] provides a stable operation in parallel configurations with a grid impedance down to short circuits and intermodule coupling impedances as low as 1%. The solution presented in [14] uses a pole-placement strategy and improves the reference tracking performance compared to transfer-function-based controllers.

This paper is an extension of the conference version [28], which includes additional experimental results and a more complete theoretical presentation. In the following a thorough comparison to previously proposed voltage controllers is detailed.

The presented scheme uses a single-loop control structure that has the following advantages compared to double-loop solutions [8]–[17]:

- The bandwidth of the proposed voltage controller can be set as large as the available bandwidth in the physical system without compromising the system stability whereas control structures with an inner current loop inherently limit the achievable voltage-loop bandwidth, which should be smaller smaller than that of the current loop [22].
- Concerning the system stability, the presented state-space controller requires a simple design process which results in a stable system with a good dynamic performance irrespectively of the plant parameters, provided that the resonant frequency of the LC filter is below the Nyquist frequency of the digital controller. Contrarily, conventional double-loop structures become unstable when controlling voltage harmonics close or above the critical frequency ($f_s/6$), where f_s is the sampling frequency [1]. In order to avoid this limitation, previously proposed solution require additional damping strategies, which increase the system complexity, in order to obtain a stable system.
- Double-loop structures do not have enough degrees of freedom to completely control the output impedance of the voltage-controlled VSC. When the output impedance is lowered at a set of frequencies by adding multiple PI or PR controllers tuned at such frequencies, then the output impedance increases in an uncontrolled manner at other frequencies due to the appearance of peaks in the system sensitivity function. The proposal permits to shape the output impedance of the converter in order to minimize the output voltage distortion. In particular, the presented design obtains a zero output impedance at a set of design-selected frequencies without generating sensitivity peaks.

Compared to previously proposed single-loop controllers [18]–[23], the presented solution has the following advantages:

- It results in a voltage-controlled VSC with zero output impedance at a set of design-selected frequencies sensing only the capacitor voltage. Such characteristics ensures a low output voltage distortion even when the converter is connected to a nonlinear load, which demands a distorted current, or to a grid with a distorted grid voltage.
- The presented controller contains a multi-frequency observer that offers a high robustness to changes in the load impedance and ensures a stable operation even when operating in grid-connected mode with a small coupling impedance. This is in accordance with the results obtained in [21], where a similar control structure but without harmonic control capability, was presented. It should be noted that adding harmonic control to the controller presented in [21] and maintaining its stability and robustness is not an immediate process.

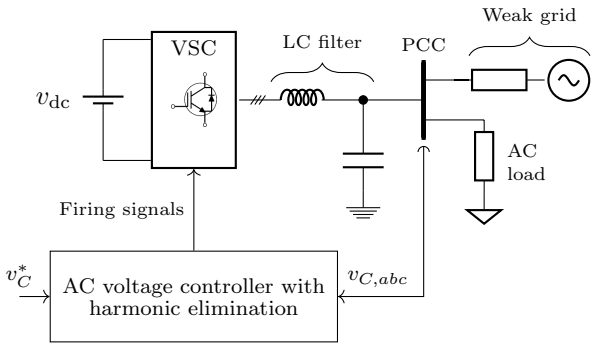


Fig. 1. Grid-connected VSC with an LC filter and an ac voltage controller.

The rest of the paper is organized as follows. Section II introduces a model of the plant and of the design-selected harmonic disturbances. This model is used in Section III to design the proposed controller. Next, in Section IV, the robustness of the proposal is assessed and compared to a classical solution. Furthermore, the performance under different load conditions is studied. In Section V, the theory is validated by experimental results. Finally, Section VI concludes the work.

II. Modeling of the Plant and the Disturbances

The proposed voltage controller consists of two main components, namely, a compensator and an observer. In order to design these two components, a mathematical model of the plant and of the design-selected disturbances is required.

Fig. 1 shows a diagram of the physical system, where $v_{C,abc}$ is the measured load voltage and v_C^* is the load voltage reference in the $\alpha\beta$ frame. For simplicity, the subscript that denotes the $\alpha\beta$ frame, which is the reference frame where the controller operates, is omitted.

The plant model required to design the proposed voltage controller relates the controller output voltage v with the capacitor voltage v_C. Fig. 2(a) shows a detailed block diagram in the $\alpha\beta$ frame of such plant model, where L and C denote the values of the LC filter reactive elements; $R_{\rm L}^{\rm ESR}$, R_C, and $R_{\rm VSC}^{\rm ESR}$ represent the equivalent series resistances (ESRs) of the filter and the VSC [29]; the zero-order-hold (ZOH) block models the pulse width modulator (PWM) by introducing a half-sample delay; the z^{-1} block symbolizes a one-sample computational delay; and $Z_{\rm load}$ models the impedance of an unknown load connected at the output. v_C and i_L are the LC-filter state variables (the capacitor voltage and the inductor current, respectively); $v_{\rm dl}$ is the PWM voltage reference, which is the one-sample delayed controller output voltage v; and $v_{\rm PWM}$ is the VSC output voltage. It should be noticed that v does

not exist in the real system because, by the time the controller output voltage is computed, a one-sample computational delay has already passed; hence the value provided by the embedded controller is v_{dl}.

Such model depends on the current demanded by a load connected at the output i_{o}. Fig. 2(b) shows the frequency response of this plant model when a linear load is connected. Three different types of linear loads are considered, namely, a resistive, a capacitive, and an inductive load. A resistive load damps the resonance of the LC filter, i.e., it lowers the gain of the plant model at the resonant frequency. Inductive and capacitive loads shift the resonant frequency of the system.

The proposed design aims to give a good performance under a wide range of loads because the load value is usually unknown at the design stage and often variable and nonlinear. The nominal plant model assumes that the load is an open circuit (no load). This is the model used to design the controller. Such choice minimizes the plant modeling error when both capacitive and inductive loads are considered, cf. Fig. 2(b). Moreover, at low frequencies, the open-loop output voltage usually decreases when a load is connected at the output due to the loading effect, i.e., the gain of the model diminishes when the load impedance lowers; hence, stability is usually improved with respect to the nominal case. A thorough study of the load effect in the system performance is analyzed in Section IV-A.

A. Model of the Plant for the Compensator

The mathematical modeling of a converter with an LC filter takes place in several steps, similarly to the modeling process of a grid-tied inverter with an LCL filter [26, Sec. II]. Each step adds features to the model equations obtained in the previous stage. In the first place, a continuous-time model of the LC filter in the $\alpha\beta$ frame, including losses, is presented. This model relates the capacitor voltage v_C to the VSC output voltage v_{PWM} in the LC filter of the plant diagram shown in Fig. 2(a). The first-order differential equations in the continuous-time domain (written in state-space form) are

$$\frac{d\mathbf{x}(t)}{dt} = \underbrace{\begin{bmatrix} \frac{-R_C}{L} & \frac{-R_C R_L}{L} + \frac{1}{C} \\ \frac{-1}{L} & \frac{-R_L}{L} \end{bmatrix}}_{\mathbf{A}} \mathbf{x}(t) + \underbrace{\begin{bmatrix} \frac{R_C}{L} \\ \frac{1}{L} \end{bmatrix}}_{\mathbf{B}} v_{\text{PWM}}(t)$$

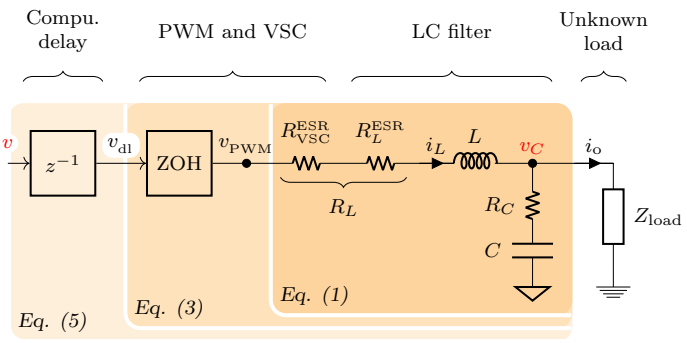
$$v_C(t) = \underbrace{\begin{bmatrix} 1 & 0 \end{bmatrix}}_{\mathbf{C}} \mathbf{x}(t)$$

$$\mathbf{x}(t) = \begin{bmatrix} v_C & i_L \end{bmatrix}^{\text{T}}. \tag{1}$$

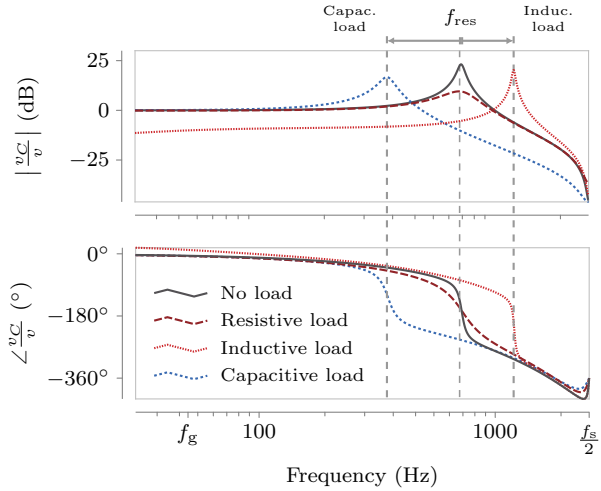
Boldface denotes a vector or a matrix. Equation (1) does not include the effect a load current i_{o} in the state variables. This disturbance is studied later.

Then, the continuous-time model (1) is discretized by using a ZOH equivalent [30]. The ZOH introduces a half a sample delay, which matches the PWM delay [29].

$$\begin{aligned} \mathbf{F} &= e^{\mathbf{A}T_s} \\ \mathbf{G} &= \mathbf{A}^{-1}(e^{\mathbf{A}T_s} - \mathbf{I})\mathbf{B} \\ \mathbf{H} &= \mathbf{C}. \end{aligned} \tag{2}$$



(a)



(b)

Fig. 2. Model of the plant. (a) Plant diagram in the $\alpha\beta$ frame when a load is connected at the output: LC filter, PWM (modeled as a ZOH), and one-sample computation delay. (b) Bode of the plant model ($v_{C_{\text{f}}}/v$) under different load conditions.

The obtained discrete-time model relates the PWM voltage reference v_{dl} with the sampled capacitor voltage:

$$\begin{aligned} \mathbf{x}(k+1) &= \mathbf{F}\mathbf{x}(k) + \mathbf{G}v_{\text{dl}}(k) \\ v_C(k) &= \mathbf{H}\mathbf{x}(k). \end{aligned} \tag{3}$$

Next, the computational delay is incorporated to the discrete-time LC filter model (3). The model of this one-sample delay on the controller output voltage v is

$$v_{\text{dl}}(k+1) = v(k). \tag{4}$$

Therefore, augmenting (3) with (4), the following plant model is obtained:

$$\underbrace{\begin{bmatrix} \mathbf{x}(k+1) \\ v_{\text{dl}}(k+1) \end{bmatrix}}_{\mathbf{x}_2(k+1)} = \underbrace{\begin{bmatrix} \mathbf{F} & \mathbf{G} \\ \mathbf{0} & 0 \end{bmatrix}}_{\mathbf{F_2}} \underbrace{\begin{bmatrix} \mathbf{x}(k) \\ v_{\text{dl}}(k) \end{bmatrix}}_{\mathbf{x}_2(k)} + \underbrace{\begin{bmatrix} \mathbf{0} \\ 1 \end{bmatrix}}_{\mathbf{G_2}} v(k)$$

$$v_C(k) = \underbrace{\begin{bmatrix} \mathbf{H} & 0 \end{bmatrix}}_{\mathbf{H_2}} \underbrace{\begin{bmatrix} \mathbf{x}(k) \\ v_{\text{dl}}(k) \end{bmatrix}}_{\mathbf{x}_2(k)}$$

$$\mathbf{x}_2(k) = \begin{bmatrix} v_C & i_L & v_{\text{dl}} \end{bmatrix}^{\text{T}}. \tag{5}$$

Equation (5) models the LC filter and the computational delay.

This model relates the converter output voltage $v_C(k)$ to the controller output voltage $v(k)$, cf. Fig. 2(a). Equation (5) is the nominal plant model and it is used in Section III to design the controller.

B. Disturbance Model for the Observer

The proposed controller includes a multi-frequency resonant action in order to eliminate steady-state errors in the controlled capacitor voltage v_C caused by non linear loads or any other unmodeled nonlinearity in the system. The resonant action is obtained by placing open-loop poles (infinite gain) in the observer at the targeted frequencies. Since the proposed controller operates in the $\alpha\beta$ frame, the positive- and the negative-sequence voltage harmonics can be controlled independently by placing a single pole instead of a complex conjugate pair of poles in the observer.

In order to implement such resonant action in the observer, the model of the plant in (5) is augmented with a high-order disturbance model. This mathematical modeling process was presented in [26, Sec. II], and it is included below for the sake of self-containment and continuity.

A single-frequency (first-order) voltage disturbance in the $\alpha\beta$ frame tuned at the hth-harmonic frequency has the following expression:

$$w_h(t) = A_h e^{j(2\pi f_o h t + \phi_h)}, \tag{6}$$

where A_h and ϕ_h are the amplitude and initial phase, respectively; f_o is the fundamental output frequency; and the sign of h defines the sequence (positive or negative) of the harmonic disturbance [31].

A multi-frequency disturbance $w(t)$ that is composed of n harmonics $(h_1, h_2, \ldots, h_n)$ is obtained by combining multiple single-frequency disturbances (6) of different frequencies:

$$w(t) = w_{h_1}(t) + w_{h_2}(t) + \cdots + w_{h_n}(t). \tag{7}$$

In order to include the multi-frequency disturbance into the model used by the observer, Equation (7) should be expressed in state-space notation:

$$\frac{d\mathbf{r}(t)}{dt} = \underbrace{\begin{bmatrix} j\omega_g h_1 & 0 & \cdots & 0 \\ 0 & j\omega_g h_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & j\omega_g h_n \end{bmatrix}}_{\mathbf{A_d}} \mathbf{r}(t)$$

$$w(t) = \underbrace{\begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}}_{\mathbf{C_d}} \mathbf{r}(t), \tag{8}$$

where

$$\mathbf{r}(t) = \begin{bmatrix} w_{h_1} & w_{h_2} & \cdots & w_{h_n} \end{bmatrix}^{\mathrm{T}}. \tag{9}$$

Similarly to the continuous-time plant model (1), the continuous-time disturbance model (8) is discretized by using a ZOH equivalent [30] to obtain the state and output matrices of the discrete-time state-space disturbance model:

$$\begin{aligned} \mathbf{F_d} &= e^{\mathbf{A_d} T_s} \\ \mathbf{H_d} &= \mathbf{C_d}. \end{aligned} \tag{10}$$

Finally, in order to obtain a model that describes both the physical plant and the design selected disturbances, the nominal plant model (5) is augmented with the previously calculated disturbance model. The resultant system model is:

$$\underbrace{\begin{bmatrix} \mathbf{x}_2(k+1) \\ \mathbf{r}(k+1) \end{bmatrix}}_{\mathbf{x}_3(k+1)} = \underbrace{\begin{bmatrix} \mathbf{F_2} & \mathbf{G_2 H_d} \\ \mathbf{0} & \mathbf{F_d} \end{bmatrix}}_{\mathbf{F_3}} \underbrace{\begin{bmatrix} \mathbf{x}_2(k) \\ \mathbf{r}(k) \end{bmatrix}}_{\mathbf{x}_3(k)} + \underbrace{\begin{bmatrix} \mathbf{G_2} \\ \mathbf{0} \end{bmatrix}}_{\mathbf{G_3}} v(k)$$

$$v_C(k) = \underbrace{\begin{bmatrix} \mathbf{H_2} & \mathbf{0} \end{bmatrix}}_{\mathbf{H_3}} \underbrace{\begin{bmatrix} \mathbf{x}_2(k) \\ \mathbf{r}(k) \end{bmatrix}}_{\mathbf{x}_3(k)} \tag{11}$$

In the augmented model, the disturbance $[w(k) = \mathbf{H_d r(k)}]$ has the same effect on the plant state vector $\mathbf{x_2}$ as the plant input signal $v(k)$; hence w is usually named input-equivalent disturbance. This model is used in the next section to develop the observer of the proposed controller.

III. Design of the Controller

This section describes the proposed controller structure. Such structure consists of three modules, cf. Fig. 3: a compensator, an observer, and an ac-side converter-current estimator that provides overcurrent protection [28, Sec. III-D]. Then, the controller design process is presented. The mathematical background of the design process, which employs a Kalman filter and a pole-placement strategy, has already been successfully applied to a current controller for a VSC with an LCL filter [26]. By applying the same design principles, a designer can address two very different problems (a current controller and a voltage controller) with a consistent and unified approach.

A. Proposed Controller Structure

The proposed voltage controller implements a single-loop high-order state-space controller that only measures the output voltage v_C. The design of the proposed controller follows the principle of separation of estimation and control. On the one hand, the compensator determines the response to reference changes by maintaining the output voltage close to its reference. It establishes the reference-tracking bandwidth and the type of response. The proposed design provides a damped response to reference commands equivalent to a first-order system with a bandwidth that can be adjusted by the designer. The maximum bandwidth that can be achieved is limited by the sampling rate and by the available bandwidth in the physical system (where overmodulation does not occur) [32, Sec. III-A]. The compensator also includes a saturator so as to provide to the observer a more accurate value of the VSC output voltage when overmodulation occurs. This eliminates the wind-up problem when the VSC is commanded with a reference that cannot be achieved [33], [34].

On the other hand, the observer is designed to provide a robust estimation of the system state vector $\mathbf{x}_3$, which is composed of the plant state vector $\mathbf{x}_2$ and of the disturbance state vector $\mathbf{r}$, even in the presence of plant model variations. The estimated multi-frequency disturbance w, cf. (8), cancels the effect on the capacitor voltage of current harmonics

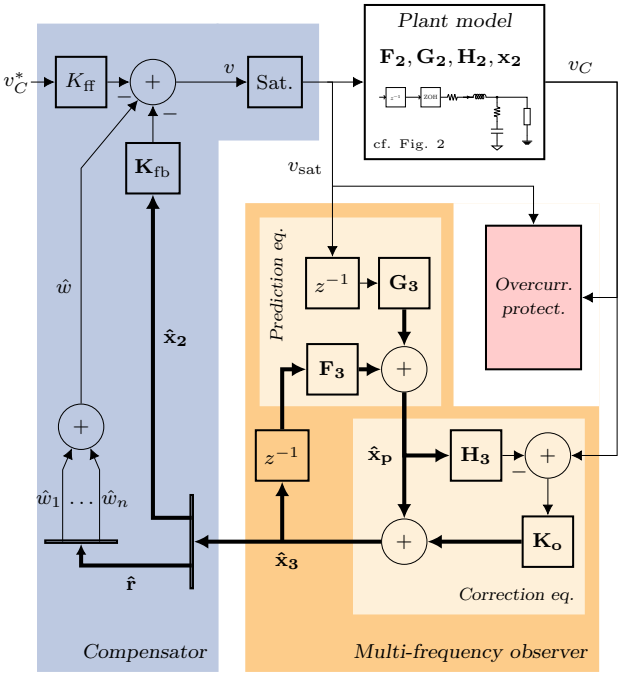


Fig. 3. Detailed scheme of the proposed voltage controller structure.

generated by a nonlinear load or a distorted grid voltage. Therefore, the observer reduces the output impedance of the VSC at the frequencies where the load is expected to demand current. Moreover, since the plant model can experience large deviations depending on the load value, cf. Fig. 2(b), the proposed observer design ensures a high robustness against changes in the load impedance in order to maintain the performance when different loads are connected.

B. Design of the Compensator

In order to obtain the desired control law, the compensator employs two gains, namely, a feedback gain K_{fb} and a reference feedforward gain K_{ff}. The mathematical operations required to obtain such gains are detailed below. The design employs a pole-placement method, and it requires three parameters: the resonant frequency of the LC filter f_{res}, the sampling period of the digital controller T_{s}, and the desired controller bandwidth f_{BW}.

In order to obtain a damped response, the open-loop resonant poles of the LC filter $p_{1,2}^{\text{ol}}$ are moved to a more damped region $p_{1,2}^{\text{cl}}$ using a radial projection [30], cf. Fig. 4(a). A damping factor ζ of 0.7 is used because it provides enough damping while requiring a low controller effort [30]. The computational delay pole p_3^{ol} is moved to a lower frequencty p_3^{cl} in order to make it the dominant pole, and set the desired bandwidth, cf. Fig. 4(b). Such pole locations are summarized in Table I.

The plant model also contains a fast zero z_1. Such zero is caused by the capacitor ESR of the LC filter. Since it is located at a high frequency, it does not require compensation. Fig. 4(a) shows a pole-zero map of the open-loop and the closed-loop roots of the plant.

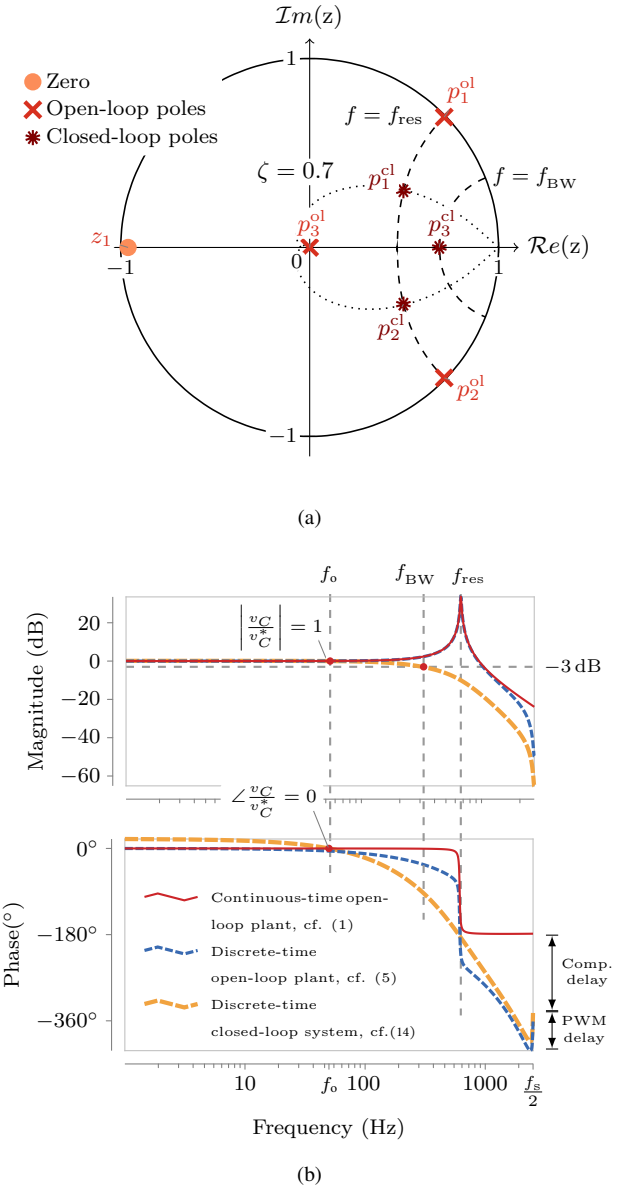


Fig. 4. Frequency domain models of the nominal plant and of the closed-loop system. (a) Discrete-time pole-zero map. (b) Bode diagram.

In order to obtain a closed-loop system with the specified closed-loop poles (cf. Table I), Ackermann's formula is applied to compute the gain K_{fb}:

$$K_{\text{fb}} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \mathbf{G_2} & \mathbf{F_2 G_2} & \mathbf{F_2}^2\mathbf{G_2} \end{bmatrix}^{-1} A_{\text{cl}}(\mathbf{F_2}), \quad (12)$$

where $A_{\text{cl}}(\mathbf{F_2})$ is the characteristic polynomial evaluated at $\mathbf{F_2}$:

$$A_{\text{cl}}(\mathbf{F_2}) = (\mathbf{F_2} - p_1^{\text{cl}}\mathbf{I})(\mathbf{F_2} - p_2^{\text{cl}}\mathbf{I})(\mathbf{F_2} - p_3^{\text{cl}}\mathbf{I}).$$

The previous closed-loop pole locations provide a damped response to reference commands with the desired bandwidth. Nonetheless, they do not provide unity gain at the nominal output frequency f_o. The negative feedback changes the open-

TABLE I
DIRECT DISCRETE-TIME POLE PLACEMENT OF THE PLANT POLES

Poles	Position in the z-plane	
	Open-loop	**Closed-loop**
LC filter	Radial projection of resonant poles to $\zeta = 0.7$.	
	$p_{1,2}^{\mathrm{ol}} = e^{\pm j\omega_{\mathrm{res}}T_{\mathrm{s}}}$	$p_{1,2}^{\mathrm{cl}} = e^{-(\zeta\omega_{\mathrm{res}} \pm j\omega_{\mathrm{res}}\sqrt{1-\zeta^2})T_{\mathrm{s}}}$
Comp. delay	Shifted to a lower frequency so as to set the desired bandwidth.	
	$p_3^{\mathrm{ol}} = 0$	$p_3^{\mathrm{cl}} = e^{-2\pi f_{\mathrm{BW}}T_{\mathrm{s}}}$

loop plant model (5) into the following closed-loop system:

$$\begin{aligned}\mathbf{x}_2(k+1) &= \overbrace{(\mathbf{F_2} - \mathbf{G_2}\mathbf{K}_{\mathrm{fb}})}^{\mathbf{F}_{\mathrm{cl}}}\mathbf{x}_2(k) + K_{\mathrm{ff}}\mathbf{G_2}v_C^*(k)\\ v_C(k) &= \mathbf{H_2}\mathbf{x}_2(k).\end{aligned} \tag{13}$$

The frequency response of such system from its reference $v_C^*(k)$ to its output $v_C(k)$ is

$$T(f) = \frac{v_C}{v_C^*} = K_{\mathrm{ff}}\mathbf{H_2}(e^{j2\pi f T_{\mathrm{s}}}\mathbf{I} - \mathbf{F}_{\mathrm{cl}})^{-1}\mathbf{G_2}. \tag{14}$$

Therefore, the necessary feedforward gain K_{ff} that restores unity gain at the nominal output frequency, e.g., $T(f_{\mathrm{o}}) = 1$, is

$$K_{\mathrm{ff}} = \frac{1}{\mathbf{H_2}(e^{j2\pi f_{\mathrm{o}}T_{\mathrm{s}}}\mathbf{I} - \mathbf{F}_{\mathrm{cl}})^{-1}\mathbf{G_2}}. \tag{15}$$

The resultant closed-loop transfer function is shown in Fig. 4(b) in comparison with the continuous- and discrete-time open-loop transfer functions of the nominal plant model.

C. Design of the Observer

In order to estimate the plant state vector $\mathbf{x}_2$ and the disturbance state vector $\mathbf{r}$, i.e., the system state, two types of linear observers can be implemented, namely, a Luenberger observer or a Kalman filter. A Kalman filter offers some advantages over a Luenberger observer in terms of robustness and simplicity of design when a high-order system, such as the proposed voltage controller, is considered. This point is explained in detail in Section IV.

The Kalman filter contains a gain $\mathbf{K}_{\mathrm{o}}$, which is computed off-line using, for instance, the iterative numerical solution described in [26, Algorithm I]. The input parameters of this algorithm are the measurement noise N, the process noise $\mathbf{Q}$, and the augmented model of the system $\mathbf{F_3}$ and $\mathbf{H_3}$, cf. (11).

Concerning the measurement noise N, the proposed ac voltage controller only measures the capacitor voltage; therefore, N is the expected value [34] of the squared capacitor voltage measurements v_C when no load is connected at the output and the VSC is on with its capacitor voltage reference v_C^* set to zero:

$$N = \mathcal{E}\{|v_C(k)|^2\}, \quad v_C^* = 0. \tag{16}$$

In our setup, N is $0.1\ \mathrm{V}^2$.

As regards the process noise $\mathbf{Q}$, this parameter indicates how much the real plant changes its state with respect to the state predicted by the nominal model, due to unmodeled disturbances. The diagonal of $\mathbf{Q}$ contains the variance of each state variable in the observer state vector $\mathbf{x_3}$. A physical interpretation of this parameter has been presented in [26].

The parameters N and $\mathbf{Q}$ define the bandwidth of the observer by controlling the distance between the closed-loop poles and the disturbance zeros of the sensitivity function of the system, which is a transfer function that determines the performance of the system, as explained in the next section. The authors recommend using a value of 0.1% [26]:

$$\mathbf{Q} = \frac{0.1}{100}\begin{bmatrix} V_{\mathrm{o}} & 0 & 0 & \cdots & 0 \\ 0 & \frac{P_{\mathrm{o}}}{3V_{\mathrm{o}}} & 0 & \cdots & 0 \\ 0 & 0 & V_{\mathrm{o}} & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & V_{\mathrm{o}} \end{bmatrix}. \tag{17}$$

Fig. 5 shows the root locus of the system sensitivity function $S(f)$ for a sweep in $\mathbf{Q}$ when the design selected frequencies are both sequences of the fundamental output frequency $\pm f_{\mathrm{o}}$ and the main low-order harmonics $-11f_{\mathrm{o}}, -5f_{\mathrm{o}}, +7f_{\mathrm{o}}$, and $+13f_{\mathrm{o}}$.

On the one hand, some of the roots of S are in fixed locations irrespectively of the value of $\mathbf{Q}$. The disturbance zeros $z_{hf_{\mathrm{g}}}^{\mathrm{d}}/h \in \{-11, -5, \pm 1, +7, +13\}$ are always placed over the unit circumference at the design selected frequencies to ensure that the sensitivity is always zero at such frequencies. The so called plant-model zeros $z_{\mathrm{delay}}^{\mathrm{p}}$ and $z_{\pm f_{\mathrm{res}}}^{\mathrm{p}}$ are placed at the location of the plant-model poles. In addition, the plant closed-loop poles $p_{1,2,3}^{\mathrm{ol}}$ are also at a fixed position, cf. Table I because of the direct pole-placement strategy applied to design the compensator. On the other hand, the rest of the poles and zeros are automatically placed by the proposed observer design method. The Kalman filter automatically places them in locations which provide a robust system and a high bandwidth.

In order to facilitate the test and implementation of the proposed voltage controller, a design example and an implementation example of the proposed voltage controller written in Matlab code has been included as supplementary material.

IV. RELATION BETWEEN ROBUSTNESS, PERFORMANCE, AND OUTPUT IMPEDANCE

This section explains how the presented controller enhances the steady state and transient performance of the system. To obtain a good performance during steady state and transient events, the output impedance of the system Z_{out} should be as low as possible. A low output impedance permits to deliver any load currents without affecting the output voltage.

In a VSC with an LC filter, a low output impedance can be achieved in two different ways. The first one is to install an LC filter with reactive elements that have a low impedance, i.e., the values of L, R_L, and R_C are small and the value of C is large, cf. $Z_{\mathrm{out}}^{\mathrm{ol}}$ in Fig. 6(a). The second one is to design a controller that lowers the output impedance of the system formed by the converter and the LC filter by using feedback of the output voltage.

Fig. 6(b) shows the output impedance $Z_{\mathrm{out}}^{\mathrm{ol}}$ of a converter that operates in an open-loop configuration, i.e., without a closed-loop controller that regulates the output voltage. The illustrated waveform is clamped for values greater than $10\,\Omega$.

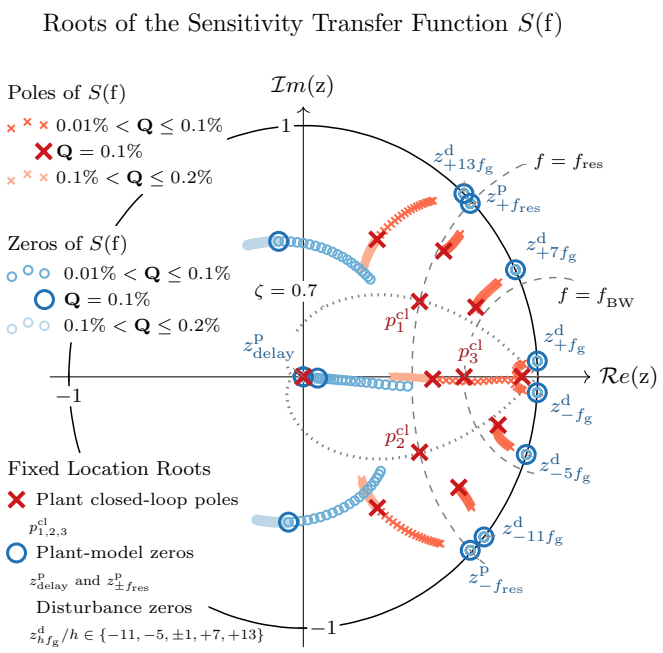


Fig. 5. Roots of the sensitivity tranfer function for a sweep in the design parameter (Q).

Such output impedance achieves very low values at dc and at high frequencies, namely, R_L and R_C. However, Z^{ol}_{out} increases in the mid-frequency range and it tends to a high value at f_{res}. If the value of L is reduced and the value of C increased, a lower impedance is obtained maintaining the same resonant frequency at the expense of increasing the inductor current ripple and the capacitor size, cf. Fig 6(b). In addition, this approach has the following problems. It does not provide a true zero output impedance at any frequency and the impedance around f_{res} is always too high.

In order to solve these limitations, the proposed feedback controller reduces the output impedance. This is accomplished by lowering the sensitivity of the system at a set of design-selected frequencies. The sensitivity function of the system S is a transfer function that describes how the controller responds to disturbances [34]. A controller modifies (amplifies or attenuates) the effect of a disturbance (such as the load current) on the controlled variable (the capacitor voltage) with respect to the open-loop response, according to the value of S. In other words, it represents the change in the output impedance that the closed-loop controller imposes to the open-loop plant:

$$Z^{cl}_{out} = SZ^{ol}_{out}. \tag{18}$$

Fig. 6(c) shows the change in the output impedance caused by the proposed closed-loop controller. The proposal provides a zero output impedance at a set of arbitrarily selected frequencies ($-11f_o, -5f_o, \pm f_o, +7f_o$, and $+13f_o$, in this example). Since the spectrum of the load current in the $\alpha\beta$ frame typically contains such frequency components, this design improves the transient and steady-state responses of the voltage controller because the output voltage distortion is minimized.

The design presented in the previous section can, theoretically, provide a zero output impedance at as many frequencies as desired because the number of frequencies where a resonant action (infinite gain) [33] can be placed is unlimited, provided that they are below the Nyquist frequency of the digital controller $f_s/2$. The only obvious practical limitation is the computational burden. In any case, current processors can execute the proposed control equations, which consist only of simple additions and multiplications (cf. Fig. 3), without any problems even for large orders [cf. (11)]; hence, this constraint is virtually eliminated. Unfortunately, the robustness of the system to load changes or parameter variations is restricted by a fundamental limitation that is common to all linear controllers, namely, Bode's sensitivity integral theorem. This is a fundamental constraint that limits the number of frequencies where the controller can reduce the output impedance.

Bode's integral theorem states that the average attenuation ($S < 1$) and amplification ($S > 1$) of disturbances over the complete frequency range where the controller operates ($-f_s/2, f_s/2$) is zero:

$$\int_{-f_s/2}^{f_s/2} \ln|S(f)|\, df = 0, \tag{19}$$

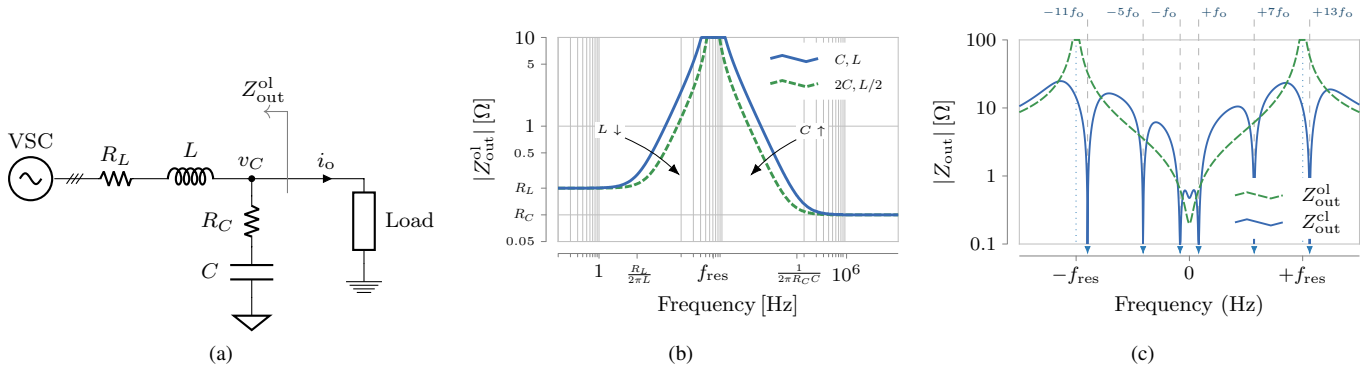
where f_s is the sampling frequency. Thus, the choice of the sensitivity function $S(f)$ at one frequency affects its value at other frequencies. This effect is illustrated in Figs. 7(a) and 7(c). The red area above the frequency axis ($S > 1$) must be equal to the blue area below the frequency axis ($S < 1$) according to (19). Consequently, when the sensitivity is reduced at some frequencies, it necessarily increases at other frequencies.

The previous mathematical result has an important physical and practical consequence because the sensitivity function is related to the output impedance of the system according to (18). Therefore, if a controller reduces the sensitivity to decrease the output impedance in some frequency range, then the output impedance must be increased at some other frequencies, cf. Figs. 7(b) and 7(d).

For this reason, the output impedance should be reduced only at the frequencies where the load is expected to demand current. In order to achieve this requirement, the Kalman filter uses a model of the plant and of the design-selected disturbances that permit to optimize the performance of the system by reducing the sensitivity only at the frequencies of the disturbances and at the resonant frequency of the LC filter.

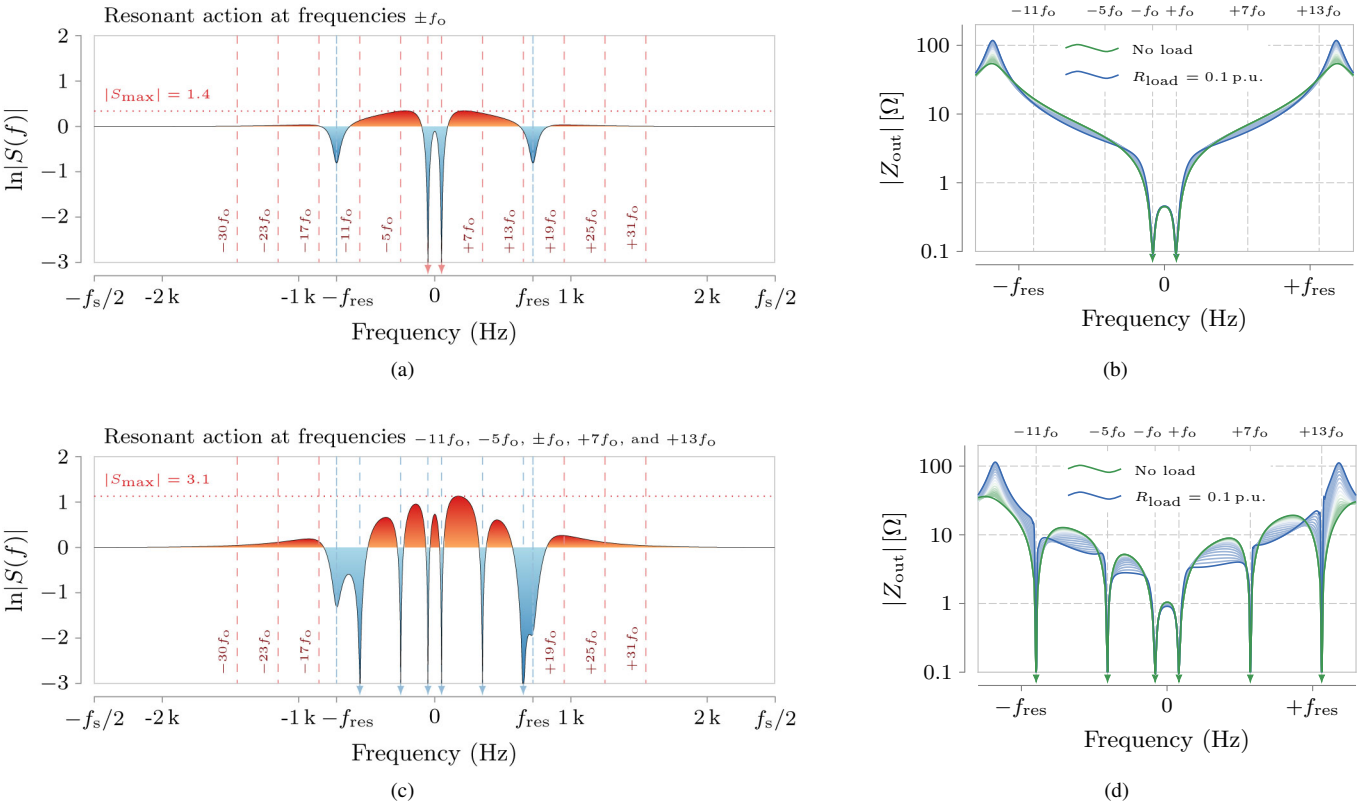
It should be noticed that when the plant model is modified with respect to the nominal model, e.g., if a load is connected, then some of the roots of the sensitivity are moved from the previously described locations. Therefore, both the sensitivity function and the output impedance are changed [11]. Figs. 7(b) and 7(d) illustrate this change when the load impedance value is swept from infinity (no load) to a value of 0.1 p.u. Nevertheless, the proposed controller always provides a zero output impedance at the design-selected frequencies because the disturbance zeros, cf. Fig. 5, do not move irrespectively of the change in the plant model.

In order to design a robust controller, this change in the output impedance of the system caused by a load variation should



(a) (b) (c)

Fig. 6. Output impedance of a VSC with an LC filter. (a) Circuit diagram of a converter without a closed-loop controller. (b) Change in the magnitude of the output impedance Z_{out}^{ol} of a converter without a closed-loop controller when the values of the LC filter are modified. (c) Change in the output impedance when the proposed controller is implemented.



(a) (b) (c) (d)

Fig. 7. Comparison of two controllers designed according to the proposed method. (a) and (b) The design includes a resonant action only at the positive- and the negative-sequence of the fundamental output frequency $\pm f_o$. (c) and (d) The design includes a resonant action at the main low-order harmonic sequences $-5f_o, +7f_o, -11f_o, +13f_o$ and at the positive- and the negative-sequence of the fundamental output frequency $\pm f_o$. (a) and (c) Graphical interpretation of Bode's integral theorem, which illustrates the regions where the controller amplifies (red areas) or attenuates (blue areas) disturbances that affect the capacitor voltage. (b) and (d) Output impedance Z_{load}^{cl} when a resistive load R_{load} is connected, $R_{load} > 0.1$ p.u.

be minimized. This is accomplished by reducing the frequency ranges where the controller responds to disturbances, i.e., the frequencies where $S(f) \neq 1$, because the controller relies on the nominal plant model to perform such change in the output impedance.

This range can be reduced in two ways. The first one is by selecting a lower value of **Q** [26, Fig. 7(b)]; hence reducing the bandwith of the observer. The second one is by reducing the set of design-selected frequencies where a zero output impedance is requested, i.e., where $S(f) = 0$.

The previous analysis gives a qualitative insight into the relation between the robustness of the controller to plant parameter variations and the output impedance of the power converter using the sensitivity function. However, such analysis does not provide a quantitative indication of the range of load impedance values where transient performance requirements are met. In the following section, a quantitative analysis of the stability of the system as a function of the load impedance

is presented; resistive (R), inductive (RL), and capacitive (RC) loads are considered.

A. Analysis of the Stability as a Function of the Load

Although the load is usually modeled as a current disturbance, this common practice is an approximation that does not take into account the change in the system dynamics that a load causes. Only when the load is a true current source (with infinite output impedance), it is accurate to model it as a disturbance. Therefore, the effect of a load should be analyzed as a change in the plant model, cf. Fig. 2(b), in order to determine the stability margins and transient performance, specially when large changes in the load impedance are considered.

From the control point of view, two factors determine the range of loads that can be connected to the system before the performance is significantly degraded. The first one is the robustness of the controller. A robust controller can tolerate a severe change in the plant model (caused by connecting a low impedance load) without changing its steady-state and transient performance significantly. The second factor is the impedance of the LC filter installed. For a given LC filter, a smaller change is obtained in the plant model, cf. Fig. 2(b) when the impedance of the load $Z_{\rm load}$ is large compared to the impedance of the filter, e.g., when $Z_{\rm load} \gg j\omega L$ and $Z_{\rm load} \gg 1/(j\omega C)$. Hence, for a given load power factor, stability is most affected when the load impedance is minimum.

Two parameters are commonly used to specify the range of loads which can be connected to the system during islanded operation: the nominal output power $P_{\rm o}$ and the rated output power factor $\cos\phi$ [35]. The nominal output power $P_{\rm o}$ sets a lower bound in the magnitude of the load impedance during islanded operation.

$$|Z_{\rm load}^{\rm nom}| = 3V_{\rm o}^2/P_{\rm o}, \tag{20}$$

where $V_{\rm o}$ is the rated output voltage. The rated output power factor describes the ratio of the maximum active and apparent loading that the converter can handle, that is, the maximum admissible load impedance angle during nominal power operation.

Nevertheless, when the power converter operates in grid-connected mode, cf. Fig. 1, a much lower load impedance can be seen by the converter without exceeding its power limit because the load impedance in such configuration is the parallel equivalent of the grid impedance with the local load impedance, whereas the power transfer depends on the relation between the grid voltage and the converter output voltage. As explained previously, the worst case in terms of stability and plant parameter variations corresponds to a setup with a low impedance load, such as during grid-connected mode, because the nominal model [used to design the controller, cf. (5)] assumes an infinite load impedance value (no load). For such reason, this section analyzes the stability of the system when the load impedance is changed from $0\,$p.u. (a short circuit) to a value of $10\,$p.u. For load impedance values greater than $10\,$p.u., the performance is almost identical to the nominal case, when no load is connected.

The presented analysis studies the robustness of the proposal by calculating the time constant τ of the poles of the closed-loop system for different values of load impedance. The time constant (or decay time-constant) of a pole at frequency f and damping ratio ζ is $\tau = 1/(2\pi f\zeta)$. Fig. 8 shows regions of load impedance whose colors denote the value of the largest time constant $\tau_{\rm max}$ in the system, that is, the time constant of the pole with the slowest dynamics. The load time constant has been excluded from the calculation. The relation between each color and its corresponding time constant interval is indicated in the label at the right of the figure. Both the resistive and the reactive components of the load impedance ($R_{\rm load}$ and $X_{\rm load}$ respectively) are changed from a light load condition ($R_{\rm load} = 10\,$p.u., $X_{\rm load} = \pm 10\,$p.u.) to a short-circuit situation ($R_{\rm load} = X_{\rm load} = 0$. The system base values are indicated in Table II.

Since the proposed controller allows the designer to arbitrarily specify a set of frequencies where a zero output impedance is obtained, three different designs with zero-output impedance at different sets of frequencies are studied. The first one only offers a zero output impedance at the nominal output frequency $\pm f_{\rm o}$, cf. Fig. 8(a). The second one adds to the previous set of frequencies the main low-order harmonics $-11f_{\rm o}, -5f_{\rm o}, +7f_{\rm o}, +13f_{\rm o}$, cf. Fig. 8(b). The third one includes all the previous frequencies plus $-17f_{\rm o}$, and $+19f_{\rm o}$, cf. Fig. 8(c).

As expected from the study included in Section IV, the robustness of the controller is reduced ($\tau_{\rm max}$ increases) when the number of frequencies with a zero-output impedance increases. This is a fundamental limitation, cf. Bode's integral theorem, that applies to any linear controller. Nonetheless, the achieved performance is acceptable even when the output voltage v_C is controlled with zero steady-state error at a large set of frequencies, cf. Fig. 8(c).

In summary, the proposal can operate connected to a wide range of loads without significantly degrading its performance and without requiring a low-impedance LC filter or a high switching frequency. This analysis has considered R, RL, and RC loads. This type of loads assess the operation when the output current is in phase, lags, or leads, respectively, the output voltage. Nonetheless, this analysis can be extrapolated to the case of a complex (high-order) impedance network, such as a an LC load whose impedance is comprised within the shaded regions shown in Fig. 9.

B. Comparison to a Double-Loop Controller

In order to perform a comparison of results to relevant publications in the literature, this section compares in terms of the sensitivity and the output impedance the proposal to a system with a transfer-function-based (classical) controller. A classical design is selected because it is regarded as one of the most commonly used mechanisms for the ac voltage control of power converters.

Among the different classical alternatives studied in the literature, double-loop structures are considered to be a good solution thanks to their modularity and robustness, compared to classical single-loop controllers. Fig. 10 displays a block diagram representation of the analyzed classical controller [10]

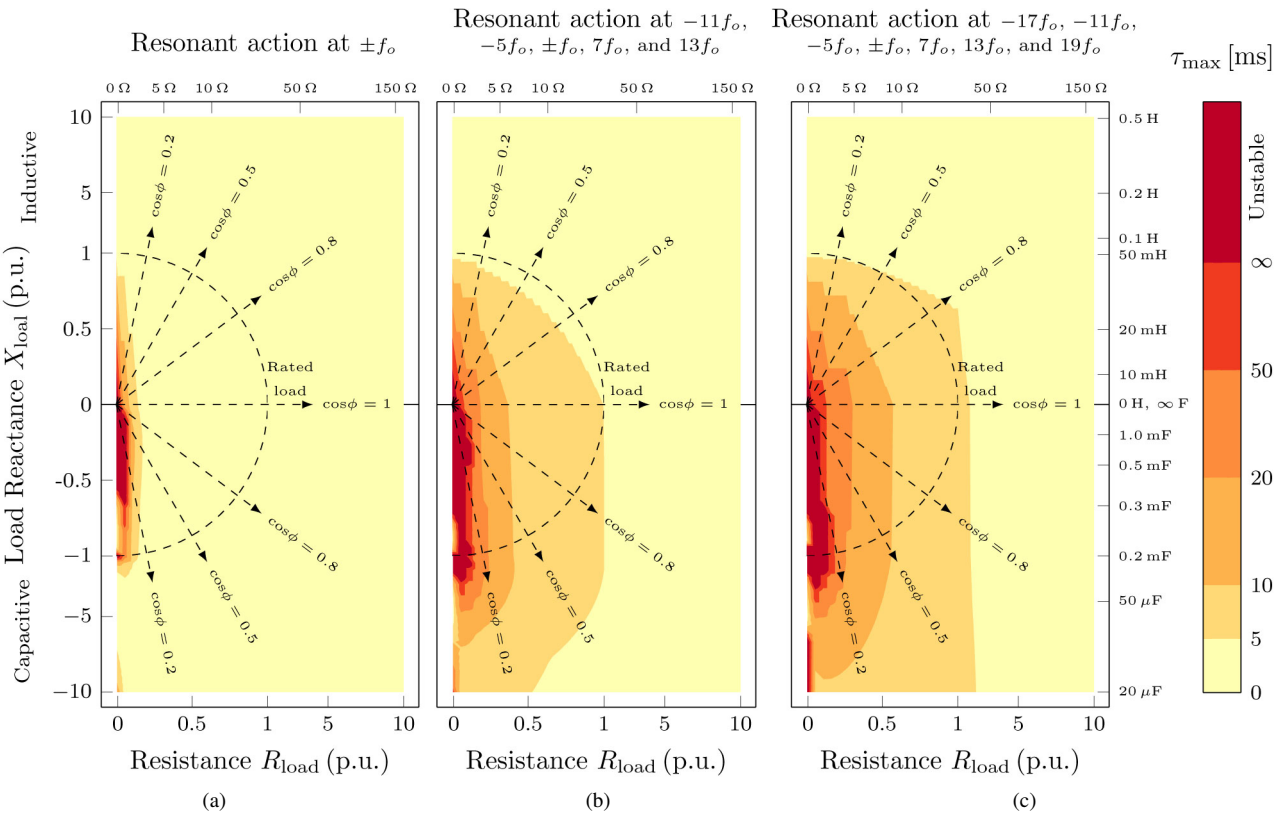


Fig. 8. Regions of load impedance whose colors denote the value of the largest time constant τ_{max} in the system, that is, the time constant of the pole with the slowest dynamics. (a) Zero output impedance is requested only at the fundamental output frequency $\pm f_o$. (b) Zero output impedance is requested at the fundamental output frequency $\pm f_o$ and at the following main low-order harmonics $-11f_o, -5f_o, +7f_o$, and $+13f_o$. (c) Zero output impedance is requested at the fundamental output frequency $\pm f_o$ and at the following main low-order harmonics $-17f_o, -11f_o, -5f_o, +7f_o, +13f_o$, and $+19f_o$.

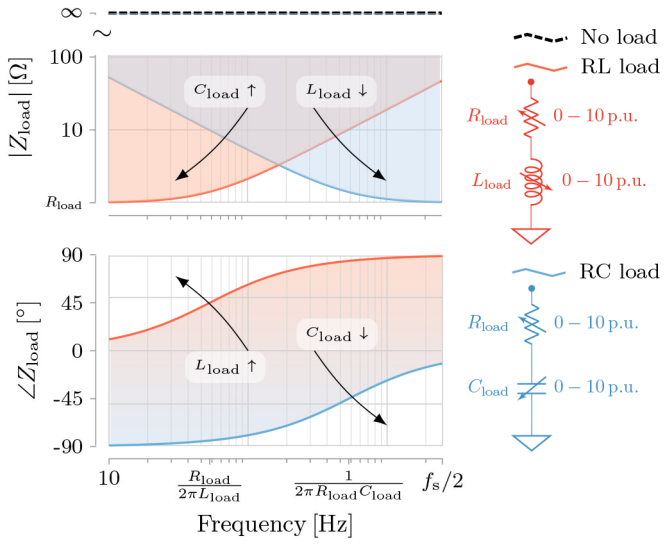


Fig. 9. Magnitude and phase of the loads used to assess the performance of the proposal.

in the $\alpha\beta$ frame. This controller structure consists of a single proportional controller in the current loop and multiple PR controllers in the voltage loop, tuned at both sequences (positive and negative) of the fundamental output frequency $\pm f_o$ and at the main low order harmonics $\pm 5f_o$ and $\pm 7f_o$, so as to remove steady-state errors in the output voltage. Additionally, it incorporates a decoupling term G_{dec} to improve the transient response of the system.

Fig. 11(a) shows the sensitivity function of such controller. As expected from the resonant action of the PR controllers, it successfully eliminates disturbances at the targeted harmonics $\pm 7f_o$, $\pm 5f_o$, and at the fundamental output frequency $\pm f_o$. Nevertheless, such classical design does not have enough degrees of freedom to avoid the following problems:

- The sensitivity function presents several peaks, which can lead to resonances if a disturbance excites the system, e.g., during a load step.
- The value of the sensitivity function is different from one at high frequencies ($S \neq 1$), which reduces the robustness of the system to plant variations.
- If a designer rises the controller gains in order to increase the width of the narrow low-sensitivity regions ($S < 1$) where the resonant action is tuned ($\pm f_o$, $\pm 5f_o$, and $\pm 7f_o$), then the sensitivity peaks also rise, which affects the system robustness and stability.

In summary, this classical design method does not have enough degrees of freedom to simultaneously increase the disturbance-rejection bandwidth (frequencies where $S < 1$) and maintain low sensitivity peaks that do not compromise the robustness and stability of the system.

Contrarily to a classical design, the proposed controller

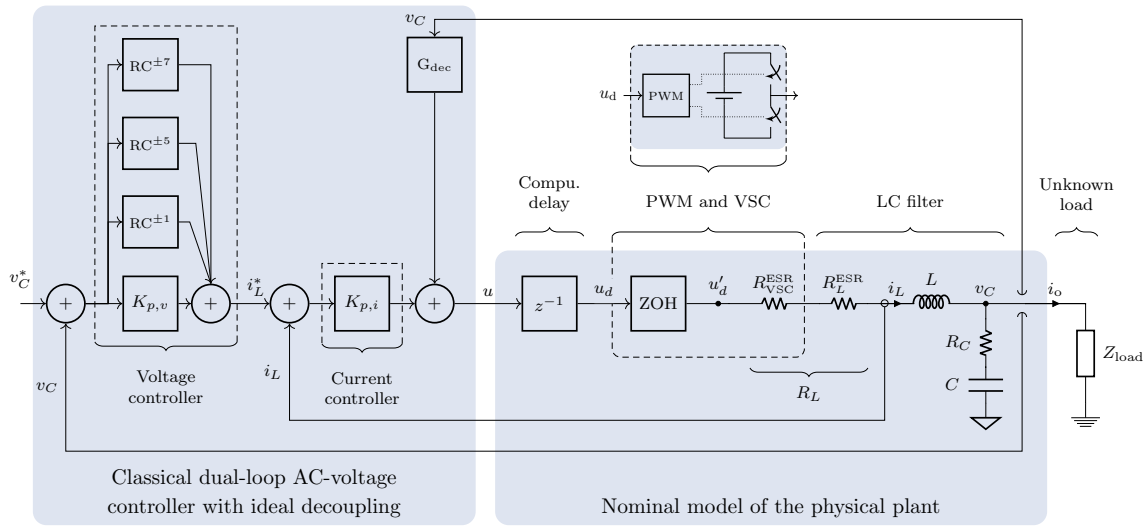


Fig. 10. Classical double-loop voltage controller structure, nominal model of the physical plant in the $\alpha\beta$ frame, and load.

avoids the previous limitations thanks to its higher number of degrees of freedom. Compared to the classical design, the proposal results in a lower sensitivity peak, cf. Fig. 11(b). In particular, the sensitivity peak is reduced from a value of 6.9 to a value of 1.9. Secondly, the sensitivity function quickly tends to one at high frequencies, above the resonant frequency of the LC filter f_{res}, in order to improve the robustness. Finally, this method allows the designer to modify the disturbance-rejection bandwidth by changing the parameter $\mathbf{Q}$, cf. Fig. 5.

Using (18), Fig. 12 shows the magnitude of the closed-loop output impedance $\left|Z_{\text{out}}^{\text{cl}}\right|$ for the two previously compared controllers. At the frequency regions where disturbances are expected to have the largest amplitude, the proposed design, cf. Fig. 3, results in a lower output impedance, compared to a classical dual-loop controller, cf. Fig. 10, when the same LC filter is installed and the same number of harmonics are controlled with zero steady-state error ($\pm 7f_o$, $\pm 5f_o$, and $\pm f_o$). This lower output impedance permits to reduce the output voltage distortion caused by the load current.

V. Experimental Results

The proposed ac voltage controller has been tested in a 10-kW VSC working both in stand-alone and in grid-connected modes. An LC filter designed according to [36] is used. The filter reactive values are $L = 2.5\,\text{mH}$ and $C = 30\,\mu\text{F}$ ($f_{\text{res}} = 580\,\text{Hz}$). The switching frequency is $f_{\text{sw}} = 2.5\,\text{kHz}$, and the dead-time is $3\,\mu\text{s}$. A double-update sampling strategy is implemented, resulting in a sampling frequency f_{s} of 5 kHz. The controller is designed using the proposed method and the set of design-selected frequencies with zero output impedance is $-17f_{\text{o}}, -11f_{\text{o}}, -5f_{\text{o}}, +7f_{\text{o}}, +13f_{\text{o}}, +19f_{\text{o}}$ and both sequences of the fundamental frequency $\pm f_{\text{o}}$. This validates the operation of the proposal when controlling harmonics close to the resonant frequency of the LC filter. The bandwidth of the controller f_{bw} is set to 300 Hz. It should be noticed that, the compensator bandwidth is limited to f_{bw} in order to reduce the controller effort and avoid overmodulation when a reference step is commanded. Nonetheless, the low-sensitivity regions of the controller are placed at frequencies above and below f_{bw}; hence, the controller can cancel disturbances above its reference-tracking bandwidth. The setup parameters are summarized in Table II. Figs. 13(a) and 13(b) show a diagram and a photograph of the experimental setup, respectively.

Fig. 14 illustrates the execution order of the proposed controller and indicates the computational load as a function of the number of design-selected frequencies where a zero output impedance is requested n. The hardware implementation contains three main parts that are executed sequentially during a sampling period: the overcurrent protection, which controls the PWM-enable signal; the multi-frequency observer, which provides the state of the plant and the estimated disturbances; and the compensator, which executes the control law, i.e., it computes the saturated controller output voltage v_{sat}. Finally, the signal v_{sat} is transformed from the $\alpha\beta$ frame to the abc frame and sent to a PWM, which generates the VSC firing signals.

A. Islanded Operation

In order to asses the operation in an islanded configuration (S_2 open in Fig. 13), a nonlinear load is connected to the converter. The nonlinear load consists of a three-phase full-wave thyristor rectifier with an inductive load and a displacement power factor (DPF) of 0.3.

The first test shows the reference tracking capability of the proposal under no load, cf. Fig. 15(a), and with a nonlinear load connected at the output, cf. Fig. 15(b). The capacitor voltage in the abc frame $v_{C,\text{abc}}$ and in the positive-sequence dq frame $v_{C,\text{dq+}}$ is shown for a reference step $v^*_{C,\text{abc}}$. Since in this test the VSC operates in islanded mode, the phase required to define the dq frame is generated by the controller. In Fig. 15(b), a small voltage is applied before the step is commanded so as to ensure that the nonlinear load is operating during the transient event because the response of the voltage controller is faster than the start-up time of the nonlinear load. When no load is connected at the output, the plant model used

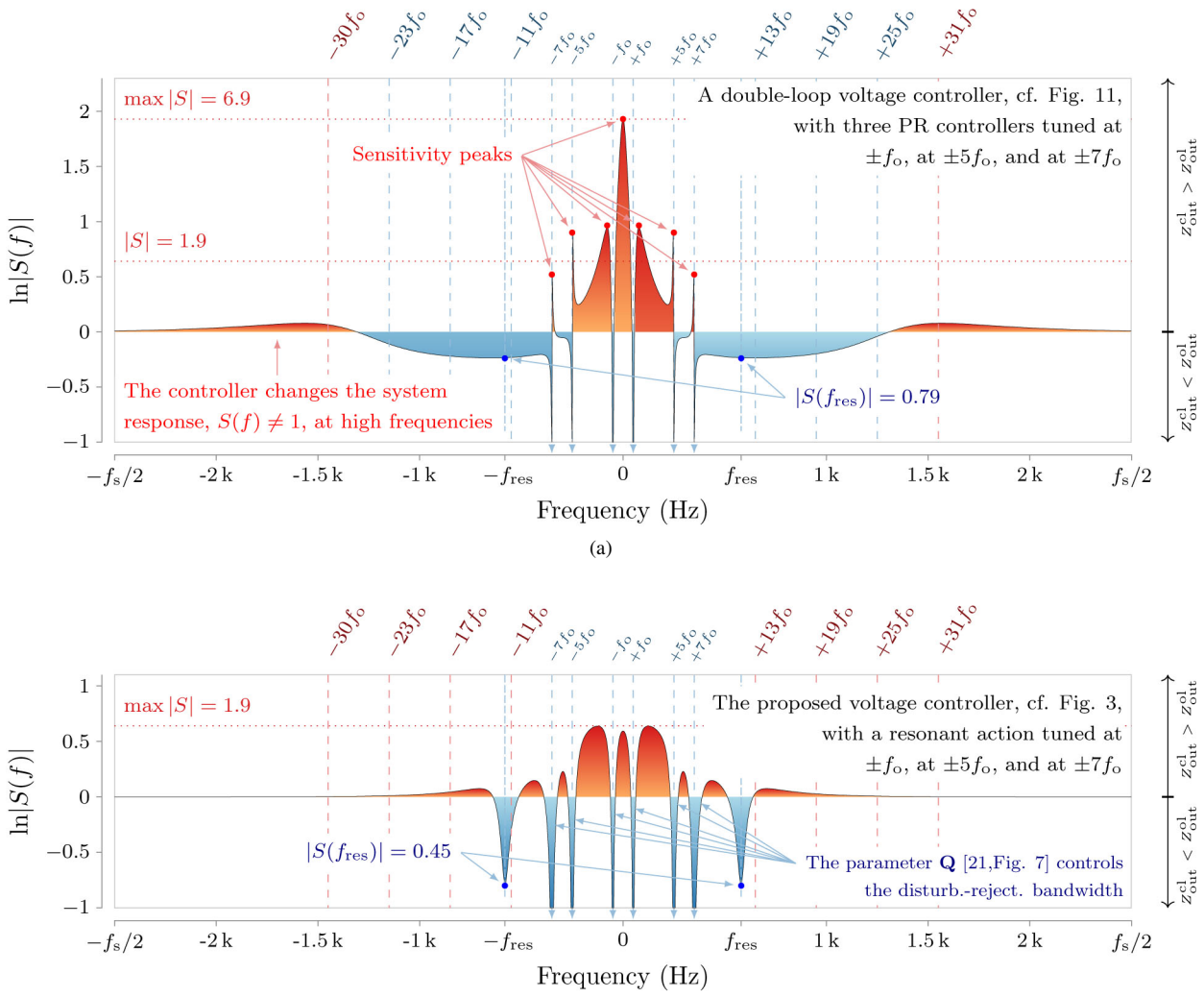


Fig. 11. Comparison of the magnitude of the sensitivity function $|S(f)|$ in a logarithmic scale of a VSC with an LC filter and a closed-loop voltage controller. (a) A classical dual-loop controller, cf. Fig. 10. (b) The proposed controller, cf. Fig. 3.

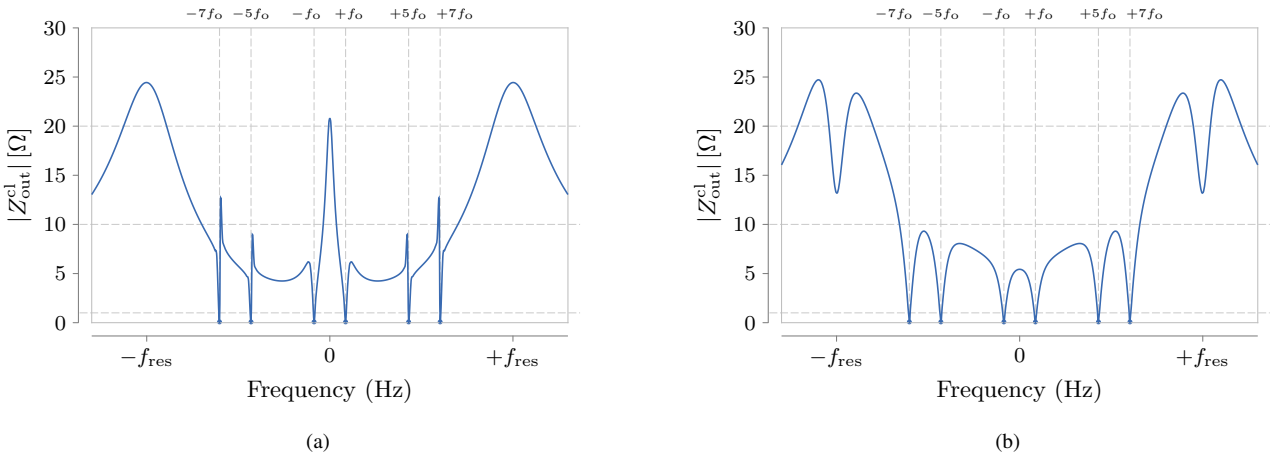
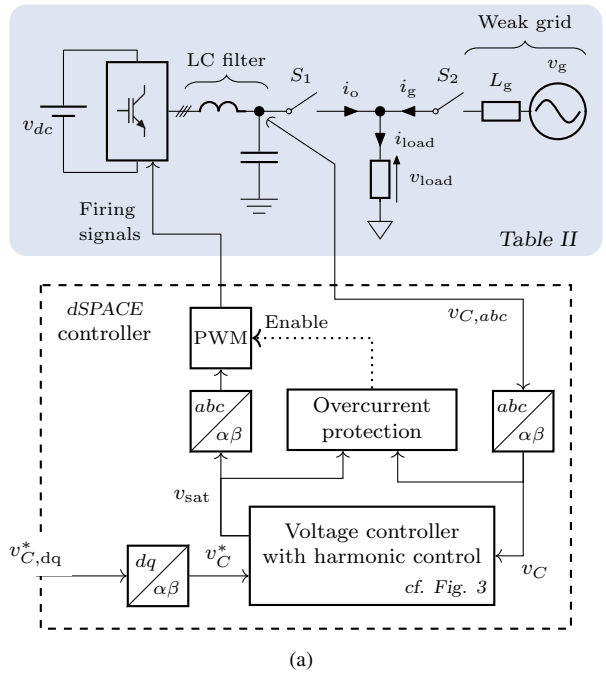
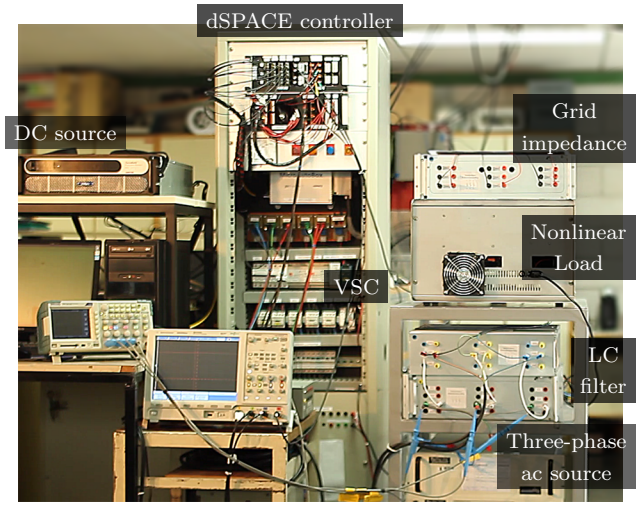


Fig. 12. Comparison of the magnitude of the closed-loop output impedance $\left|Z_{\text{out}}^{\text{cl}}\right|$ of a VSC with an LC filter and two types of closed-loop voltage controllers. (a) A classical dual-loop controller, cf. Fig. 10. (b) The proposed controller, cf. Fig. 3.

to design the controller (5) accurately describes the physical system because the nominal model used to design the compensator assumes a no load condition. Therefore, the response precisely follows the transient response of a first-order system



(a)



(b)

Fig. 13. Experimental setup of the grid-connected converter. (a) Diagram. (b) Photograph.

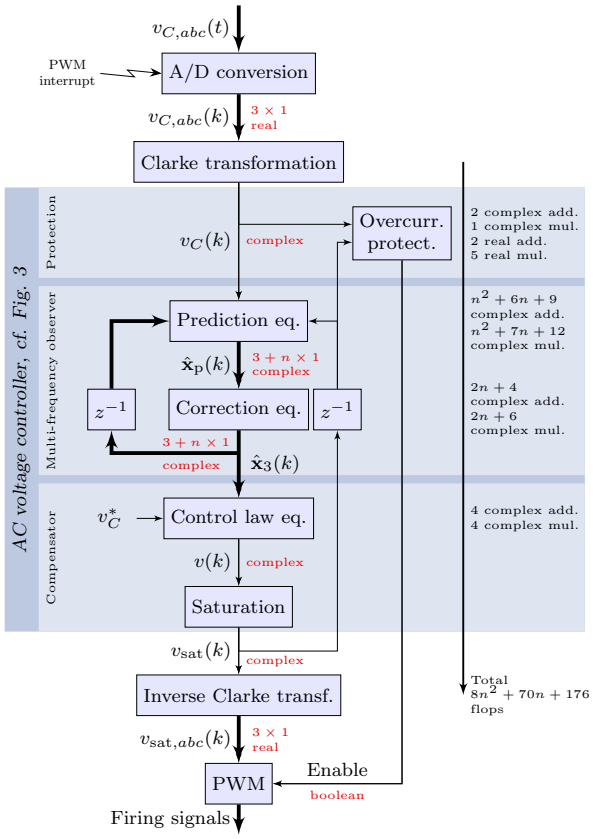


Fig. 14. Execution chronogram of the proposed controller and computational load as a function of the number of design-selected frequencies n where a zero output impedance is requested.

of the design selected bandwidth f_{bw}, as expected from the proposed direct discrete-time pole-placement strategy adopted for the compensator. When a nonlinear load is connected at the output, the response is not significantly modified, compared to Fig. 15(a), in spite of the plant model change caused by the load because of the robustness of the proposal, as explained in Section IV.

The second test evaluates the performance of the controller to a load step and compares its performance to the transfer-function-based (classical) design analyzed in Section IV-B. Both connection and disconnection events are tested. Figs. 16(a) and 16(b) show the output voltage $v_{C,\text{abc}}$ and the load current $i_{\text{o,abc}}$ during a connection and a disconnection event, respectively. In order to asses the dynamic output performance, Fig. 16(c) displays the voltage error $v^*_{C,\text{abc}} - v_{C,\text{abc}}$ in comparison with the limits defined in [35] for the two previous load step tests. The proposal meets class-one limits of such specification using an LC filter with reduced reactive values and a low switching frequency because the presented design optimizes the transient response, cf. Section IV. During steady-state, Fig. 16(c) shows a small high-frequency voltage error which is the 400-μs switching ripple of the VSC, see Figs. 16(a) and 16(b).

Fig. 16(d) shows the magnitude of the spectrum and the total harmonic distortion (THD) of the output voltage v_C and of the load current i_o. As expected, no output voltage distortion appears at the main low-order harmonics in spite of the large load current due to the resonant action of the controller, which provides a zero output impedance. Therefore, a low output voltage distortion is obtained ($\text{THD}_{v_C} = 1.5\,\%$) in spite of the highly distorted output current demanded by the nonlinear load ($\text{THD}_{i_o} = 32.0\,\%$).

Fig. 17 shows the transient response of a classical controller, cf. Fig. 10, during the previously described nonlinear load step. Although the output voltage $v_{C,abc}$ is not significantly affected by the load current $i_{o,abc}$, the converter current $i_{L,abc}$ clearly manifests an instability in the system, which triggers the converter overcurrent protection. Such instability is caused by the connection of the nonlinear load and a low robustness of the classical controller to load impedance variations. Classical

TABLE II
EXPERIMENTAL SETUP PARAMETERS

Base values			
Nominal output power	P_{o}	10	[kW]
Nominal output voltage	V_{o}	230	[V]
Minimum load power factor	$\cos\phi$	$0.2^{\dagger}$	
Output frequency	f_{o}	50	[Hz]
LC filter			
Filter inductance	L	$2.5, 0.05$	[mH, p.u.]
Filter capacitance	C	$30, 0.14$	[μF, p.u.]
Filter resonance	f_{res}	581	[Hz]
VSC			
Switching frequency		2.5	[kHz]
Dead time		3	[μs]
DC bus voltage	v_{dc}	700	[$\mathrm{V_{DC}}$]
Controller			
Sampling frequency	f_{s}	5	[kHz]
Bandwidth	f_{bw}	300	[Hz]
Measurement noise	N	0.1	[V^2]
Process noise	$\mathbf{Q}$	0.1	[%]

† Minimum load power factor depends on the number of voltage harmonics controlled with zero steady-state error, c.f. Fig.8.

TABLE III
GRID VOLTAGE HARMONICS

Order	Sequence	*h*	Magnitude
1	+	+1	230 V
3	0		5 %
5	−	−5	6 %
7	+	+7	5 %
9	0		1.5 %
11	−	−11	3.5 %
13	+	+13	3 %
THD			10.5 %

controllers offer a low robustness to load impedance variations, specially when controlling frequency components close or above the critical frequency [1] ($f_s/6 = 833$ Hz).

In order to address this limitation of classical designs when using a low sampling frequency and multiple resonant controllers, the sampling frequency of the classical controller is increased to a value of 10 kHz. Fig. 18(a) and Fig. 18(b) show the experimental transient response to the previous nonlinear load step during a connection and a disconnection event, respectively. As shown, when the sampling frequency is doubled, the classical controller provides a stable response, even when the nonlinear load is connected. Nonetheless, a large transient is observed in the output voltage during both connection and disconnection events. Such transient is clearly displayed in Fig. 19, which shows the output voltage error in comparison with the limits defined in [35]. As shown, the classical design achieves a worse output voltage regulation during the load transient event compared to the proposal [see Fig. 16(a), Fig. 16(b) and Fig. 16(c)] due to its higher output impedance [cf. Fig. 6(b)] in spite of it using a higher sampling and switching frequencies.

B. Grid Connected Operation

In order to asses the operation in a grid-connected configuration (S_2 closed), the proposed voltage controller is connected to a three-phase grid using a coupling impedance L_{g} of value 0.1 p.u. (5.4 mH). A three-phase ac voltage source is used to generate a distorted grid voltage. The grid voltage v_{g} has a THD of 10.5% and the harmonic content is indicated in Table III. The nonlinear load described in the previous section is used as a local load, as shown in Fig. 13.

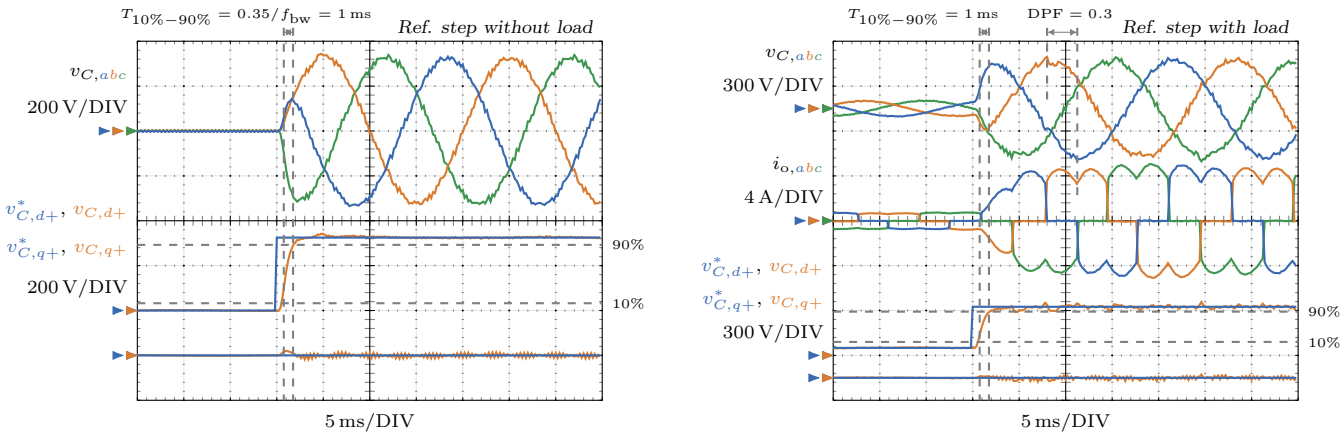
Fig. 20 shows the experimental waveforms in the abc frame during the connection event of the VSC to such distorted grid. Before the VSC is switched to grid-connected mode (S_1 is open and S_2 is closed), the load voltage v_{load} has a large distortion caused by the nonlinear load current i_{load} and the distorted grid voltage v_{g}. When S_1 is closed, the VSC output voltage v_C is maintained sinusoidal in spite of the distorted output current i_{o} delivered to the nonlinear load i_{load} and to the distorted grid i_{g}.

In order to assess the harmonic distortion during grid connected operation, the spectrum and the THD of the current and voltage waveforms shown in Fig. 20 are presented in the following.

Fig. 21 shows the spectrum and the THD of the output current i_o and of the output voltage v_C. Before the VSC is connected to the grid [S_1 is open and S_2 is closed, cf. Fig. 13(a)], the output current i_o is zero and the output voltage v_C has a negligible distortion ($\mathrm{THD}_{v_C} = 0.1\,\%$). After the VSC is connected to the grid [S_1 and S_2 are closed, cf. Fig. 13(a)], the converter output voltage distortion is zero at the design selected frequencies, which are $-17f_{\mathrm{o}}, -11f_{\mathrm{o}}, -5f_{\mathrm{o}}, +7f_{\mathrm{o}}, +13f_{\mathrm{o}}, +19f_{\mathrm{o}}$ and both sequences of the fundamental frequency $\pm f_{\mathrm{o}}$. Nonetheless, the measured voltage distortion ($\mathrm{THD}_{v_C} = 1.0\,\%$) slightly increases compared to when no load is connected at the VSC output due to the appearance of harmonic output currents above the previously indicated frequencies, where the output impedance is not zero.

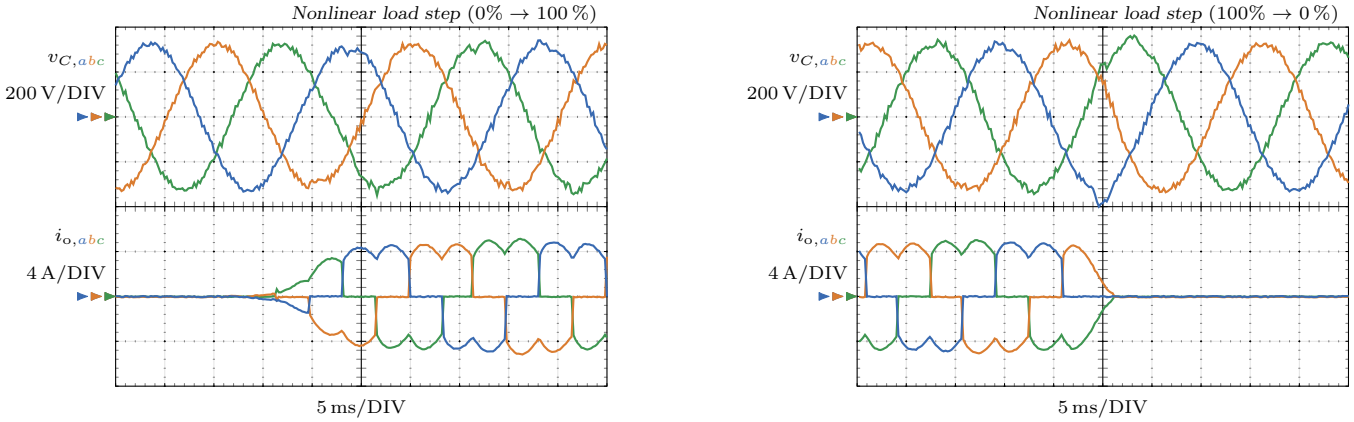
Fig. 22 shows the spectrum and the THD of the load current i_{load} and of the load voltage v_{load}. When the VSC is disconnected from the grid (S_1 is open and S_2 is closed), the load voltage v_{load} contains a large distortion ($\mathrm{THD}_{v_{\mathrm{load}}} = 17.5\,\%$), which is caused by a distorted grid voltage and the voltage drop originated by the highly distorted load current i_{load} that circulates by the weak grid impedance ($\mathrm{THD}_{i_{\mathrm{load}}} = 31.5\,\%$). During grid-connected operation (S_1 and S_2 are closed), the load voltage v_{load} coincides with the converter output voltage v_C. Therefore, a negligible load voltage distortion is observed ($\mathrm{THD}_{v_{\mathrm{load}}} = 0.9\,\%$) because the proposed voltage controller eliminates the main voltage harmonics. Moreover, when the VSC is connected to the grid, the THD in the load current slightly increases its value ($\mathrm{THD}_{i_{\mathrm{load}}} = 35.5\,\%$) because, in this configuration, the nonlinear load sees a lower source impedance which is the parallel equivalent of the grid impedance and the VSC output impedance

Fig. 23 shows the spectrum and the THD of the grid current i_g and of the grid voltage v_g during the two previously

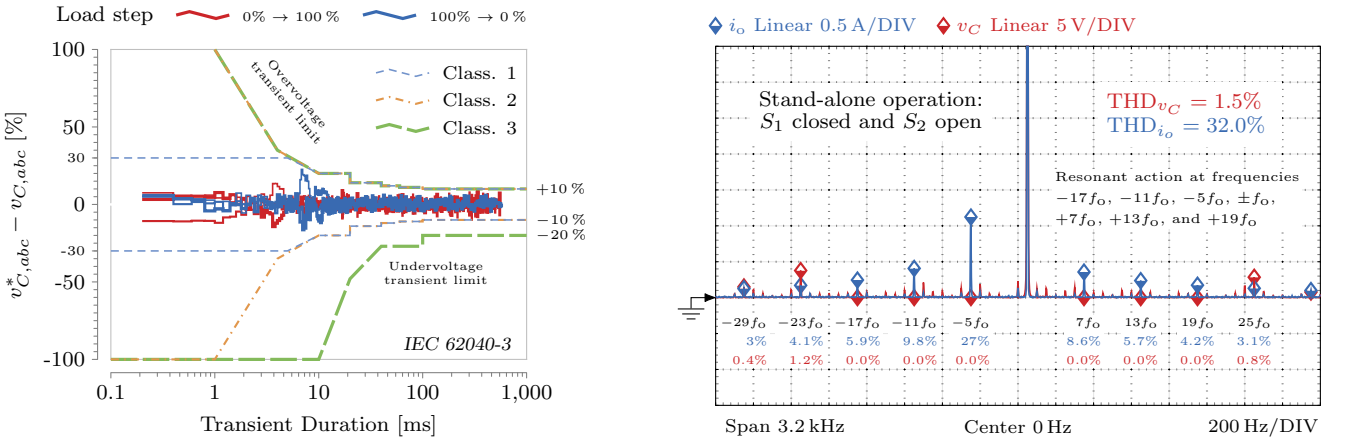


(a) (b)

Fig. 15. Experimental output voltages in the abc frame $v_{C,\text{abc}}$ and in the positive synchronous frame dq+ rotating at the fundamental output frequency f_o $v_{C,\text{dq+}}$ for a reference step $v^*_{C,\text{dq+}}$. (a) Without a load. (b) With a nonlinear load connected at the output.

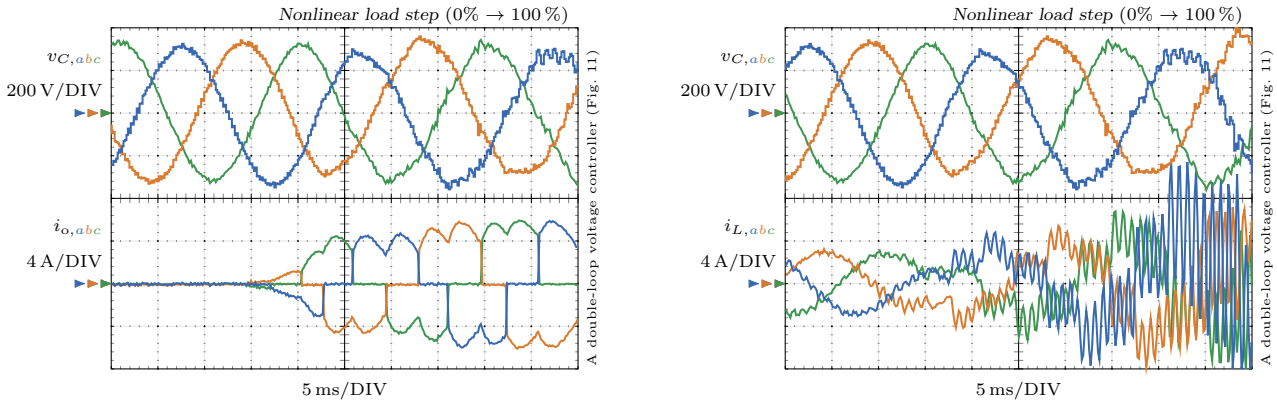


(a) (b)



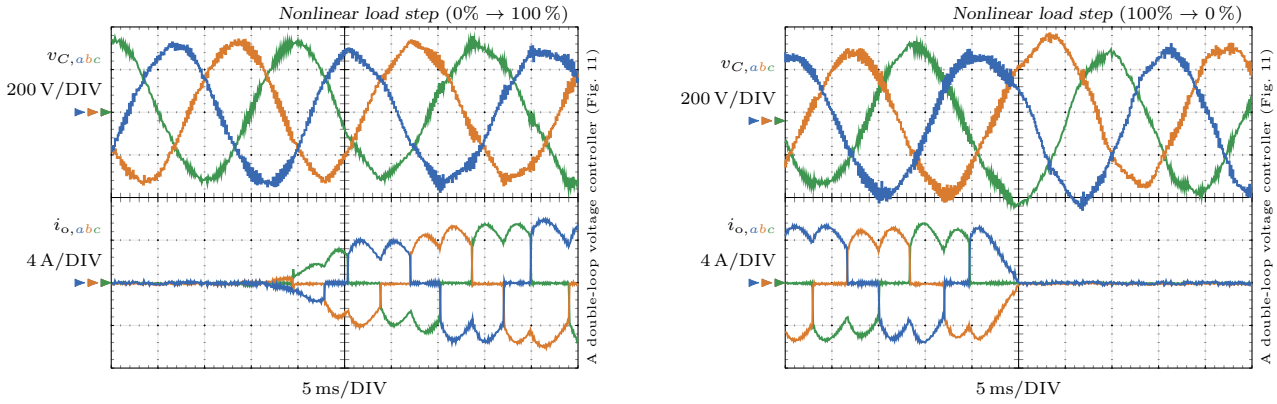
(c) (d)

Fig. 16. Transient response to a nonlinear load step. (a) Connection test: load step test from 0 % to 100 % of rated power. (b) Disconnection test: load step test from 100 % to 0 % of rated power. (c) Dynamic output performance according to [35]. (d) Magnitude of the spectrum of the output voltage v_C and of the load current i_o.



(a) (b)

Fig. 17. Experimental transient response of a classical dual-loop controller, cf. Fig. 10, during a nonlinear load step from 0 % to 100 % of rated power ($f_s = 5$ kHz and $f_{sw} = 2.5$ kHz). (a) Output voltage $v_{C,abc}$ and load current $i_{o,abc}$ in the abc frame. (b) Output voltage $v_{C,abc}$ and converter current $i_{L,abc}$ in the abc frame.



(a) (b)

Fig. 18. Experimental transient response of a classical dual-loop controller, cf. Fig. 10, during a nonlinear load step ($f_s = 10$ kHz and $f_{sw} = 5$ kHz). (a) Connection test: load step from 0 % to 100 % of rated power. (b) Disconnection test: load step from 100 % to 0 % of rated power.

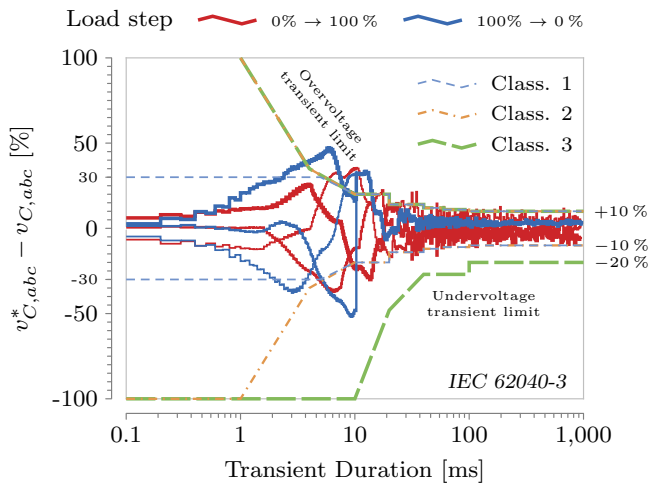


Fig. 19. Dynamic output performance according to [35] of a classical dual-loop controller, cf. Fig. 10, during a nonlinear load step ($f_s = 10$ kHz and $f_{sw} = 5$ kHz).

indicated conditions. On the one hand, before the VSC is connected to the grid, a large grid-current distortion is observed. Such distortion is caused by the nonlinear load and the highly distorted grid voltage. On the other hand, when the VSC is connected to the grid, the proposed voltage controller achieves a sinusoidal voltage at the load terminals. In such scenario, the nonlinear current demanded by the nonlinear load is provided by the VSC instead of by the grid and the grid-current THD is reduced, as shown in Fig. 23(b) compared to Fig. 23(a). Nonetheless, since the grid contains a large voltage harmonic distortion (see Table III), a significant distortion in the grid current still exists.

VI. Conclusion

This paper has presented an ac voltage controller with a high robustness to variations in the load. Both islanded operation and grid-connected mode have been tested. The proposed controller uses a single-loop structure that improves the transient performance by selectively minimizing the output impedance of the system at a set of design-selected frequencies. These frequencies can be located above the critical frequency of the

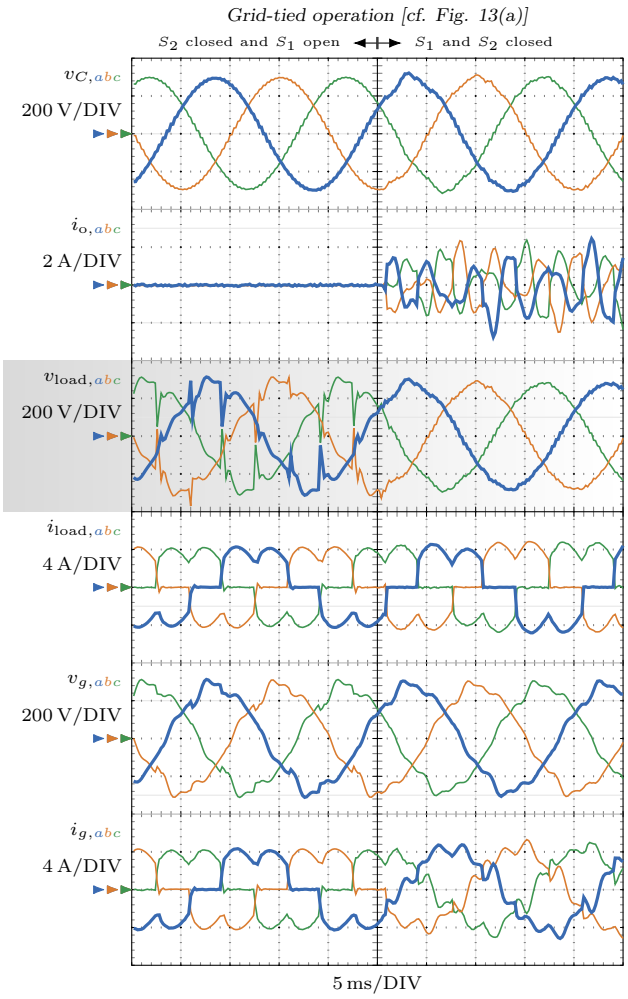


Fig. 20. Experimental waveforms in the abc frame during the connection event of the VSC to a distorted grid.

system $f_s/6$ where previous proposals have stability problems, provided that they are below the Nyquist frequency of the digital controller. Thanks to these characteristics, the presented controller achieves a low output voltage distortion, even when providing a distorted output current. System stability has been demonstrated for a wide range of load values. Moreover, the above properties are maintained irrespectively of the LC filter installed, or the sampling frequency used, provided that overmodulation of the VSC is avoided and the resonant frequency of the LC filter is lower than the Nyquist frequency.

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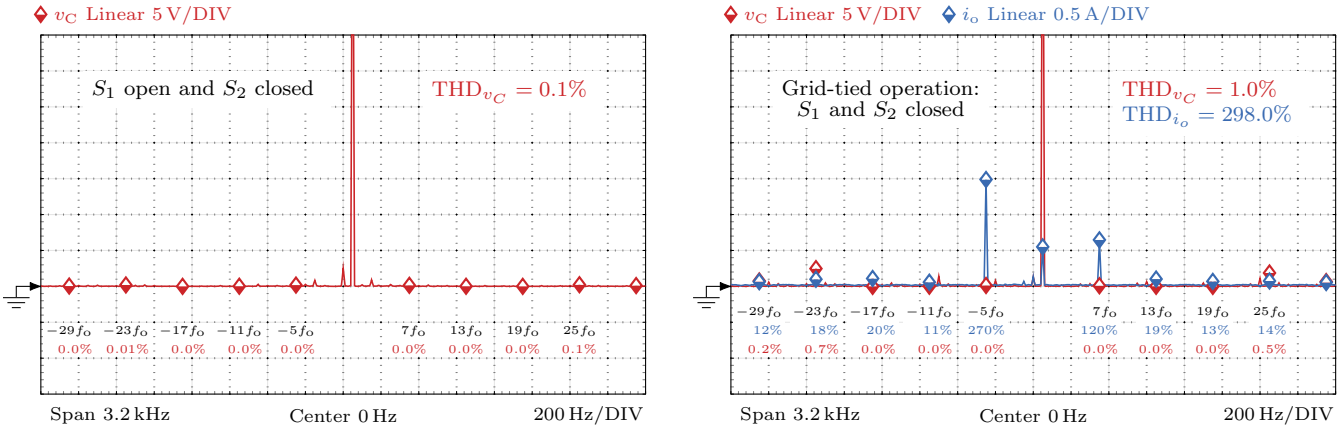

Fig. 21. Spectrum and resultant THD of the output current i_o and of the capacitor voltage v_C during two different conditions: (a) No load is connected at the output [S_1 is open and S_2 is closed, cf. Fig. 13(a)]. (b) The VSC is connected to the grid [S_1 and S_2 are closed, cf. Fig. 13(a)].

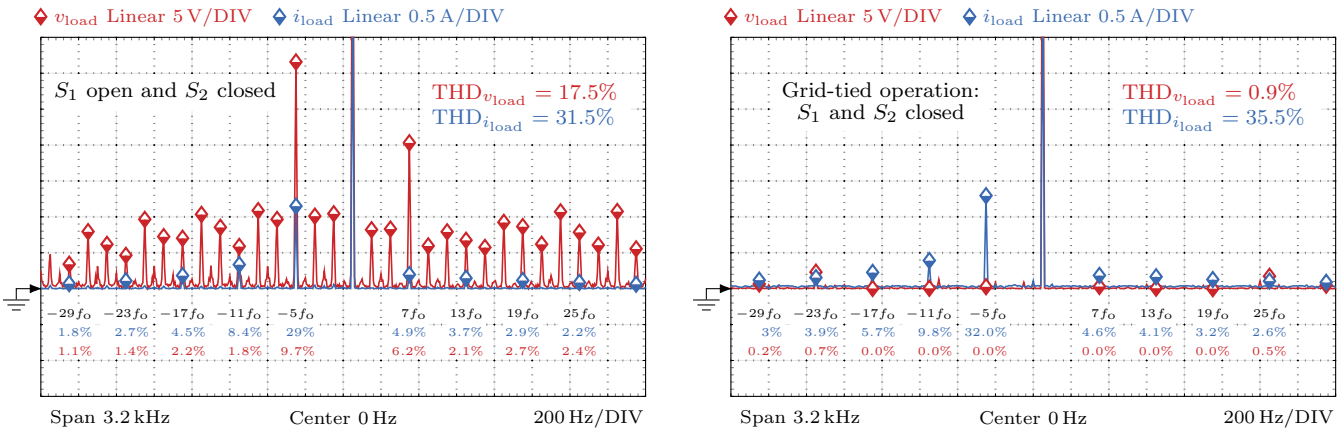

Fig. 22. Spectrum and resultant THD of the load current i_{load} and of the load voltage v_{load} during two different conditions: (a) The nonlinear load is connected to a weak grid with a distorted grid voltage [S_1 is open and S_2 is closed, cf. Fig. 13(a)]. (b) The proposed voltage controller regulates the load voltage [S_1 and S_2 are closed, cf. Fig. 13(a)].

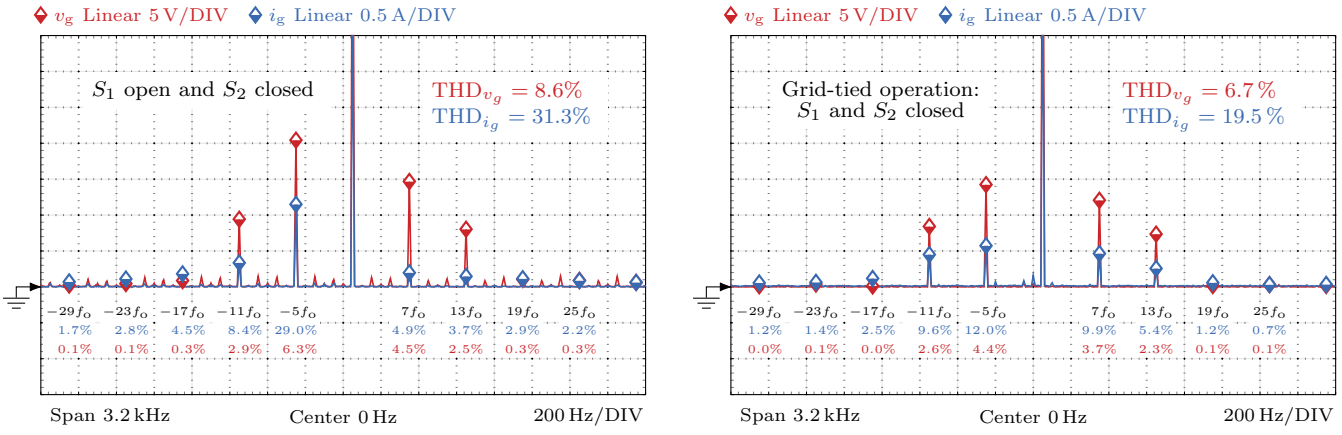

Fig. 23. Spectrum and resultant THD of the grid current i_g and of the grid voltage v_g during two different conditions: (a) A nonlinear load is connected to the grid [S_1 is open and S_2 is closed, cf. Fig. 13(a)]. (b) When the VSC operates connected to the grid [S_1 and S_2 are closed, cf. Fig. 13(a)].

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