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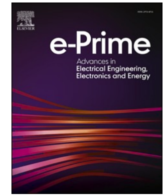

Study of 100V GaN power devices in dynamic condition and GaN RF device performances in sub-6GHz frequencies

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ABSTRACT

AlGaN/GaN devices for both power and RF applications have been investigated in this work. In particular, regarding power applications, 100 V p-GaN gate transistors have been analysed both in DC and in dynamic conditions with specific attention to the high temperature behaviour.

As a first step, the high temperature behaviour of the on-resistance (R_{ON}) of a reference process (STD process) has been investigated. The role of the different resistive components of the transistor has been analysed by evaluating how their relative weight changes with the temperature increase. Then, two different p-GaN process variations (process A and process B) have been proposed and compared to the STD process to show their improvement in terms of a limited R_{ON} increase at 150 °C, highlighting the relevance of an improved p-GaN gate processing.

Secondly, the temperature effect on the R_{ON}-degradation induced by off-state drain voltage stress has been investigated in process B-like devices. The impact of temperature on the time required to reach a steady state degradation has been addressed, enabling the comparison of the R_{ON} degradation (R_{ON}/ R_{ON0}) at equilibrium. Tests performed on several samples have demonstrated the invariance of the R_{ON}/ R_{ON0} ratio in the 25 °C to 150 °C range, suggesting the possibility to reduce the measurements required for dynamic-R_{ON} evaluation at different T.

Finally, RF devices (featuring Schottky metal gate) have been characterized in terms of DC/RF performances and long-term reliability (through HTRB tests). Different trials with increasing aluminium content of the AlGaN barrier have been compared, showing the correlation with the maximum saturation current and the output power. Moreover, the trade-off with reliability specifications has been put in evidence.

Introduction

GaN-based High Electron Mobility Transistors (HEMTs) (see Figs. 1 and 2) are well suited to high power/frequency applications thanks to the many intrinsic benefits of the material [1], especially coming from its wide bandgap and from its crystal structure (high voltages and capability to sustain high current density due to spontaneous and piezoelectric polarizations [2]). These are the reasons why GaN-based devices have many fields of application such as power amplifiers, millimetre-wave integrated circuits (MMIC) [3], next generation information communication systems [4] and power switching converters [5].

During the operation in actual applications, e.g., in power converters, GaN devices are switching for many cycles, thus inducing power dissipation (conduction and switching losses) [6]. Therefore, heat production generates an increase of the device temperature, drifting its characteristics from the ones expected at room temperature [7]. It is thus important to study the temperature behaviour of the main HEMT parameters to evaluate their degradation and to find proper tailoring of the device to better its performance at high temperature. The main

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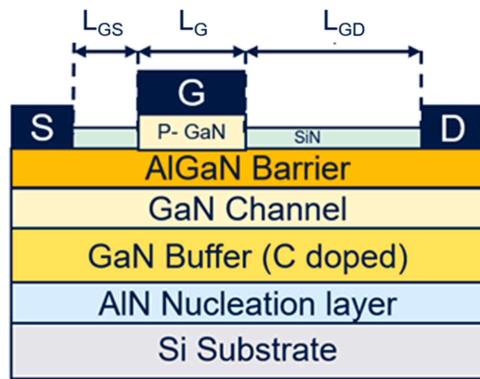

Fig. 1. Typical structure of the enhancement-mode (e-mode) Device Under Test (DUT) for normally-off operation (required for power devices), which is achieved by means of a p-GaN layer grown on top of the AlGaN Barrier. A proper design of the AlGaN thickness and Al% is used to modulate the two-dimensional electron gas (2DEG) density at the AlGaN/GaN interface.

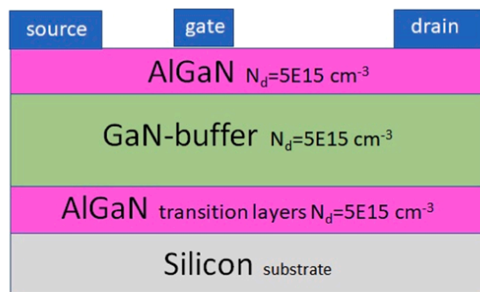

Fig. 2. Typical structure of the depletion-mode (d-mode) Device Under Test (DUT) for normally-on operation (RF devices), implementing a Schottky gate module. A proper design of the AlGaN thickness and Al% is used to modulate the two-dimensional electron gas (2DEG) density at the AlGaN/GaN interface (the reference DUTs reported in this work are characterized by Al%=23 %). An intrinsic background n-doping (with a concentration "Nd") is present in all the GaN-based layers, due to the impurities (e.g., Oxygen) of the epitaxial growth.

parameter considered for power devices is the on-resistance (R_{ON}), which is the most important figure-of-merit (FOM) of the device when it is used as a power switch. In fact, R_{ON} directly affects the conduction losses of GaN power devices, thus yielding a significant impact on the efficiency of switching converters.

Temperature may also have a significant effect on dynamic R_{ON} [8], since it could impact the trapping/de-trapping dynamics [9] and the amount of degradation induced by off-state drain voltage stress [10]. To ensure the correct modelling and characterization of GaN HEMTs, it is crucial to gain insights on the dynamic R_{ON} under conditions that are close to the device operating temperature [11]. This requires careful characterization of the device thermal behaviour to be aware of the performances that the device will reach in its final operative scenario. Therefore, p-GaN gate transistors (Fig. 1) have been deeply analyzed both in DC and dynamic conditions at high operating temperature (up to 150 °C).

Differently from power devices, RF applications usually do not require normally-off operation, enabling the exploitation of the total 2DEG density, which is found at the AlGaN/GaN heterointerface, without the need for a structural modification for the electron channel interruption at zero gate bias.

Moreover, requirements for RF devices typically involve high maximum saturation current and high output power at high frequency operation. Therefore, one of the main parameters that can be tuned to improve DC and RF performances is the aluminum mole fraction (Al%) of the AlGaN barrier (Fig. 2). Nonetheless, the robustness of the device must be taken as well into account in terms of lifetime and long-term stability, suggesting that a proper balance has to be found between DC/RF specifications and the mitigation of failure mechanisms.

The paper has been organized in three main sections, the first two related to power devices while the last one concerns RF transistors: 1) Improved High Temperature Behaviour of On-Resistance in 100 V p-GaN HEMTs; 2) Temperature Effect on R_{ON}-degradation Induced by Off-State Drain Voltage Stress in 100 V p-GaN HEMTs; 3) DC and Load Pull Characterization of RF GaN-based HEMTs with Increased aluminum Content of the AlGaN Barrier and Trade-Off with HTRB Performances.

(1) Improved High Temperature Behaviour of On-Resistance in 100 V p-GaN HEMTs.

Experimental

From the DC measurement of the drain current versus gate-source voltage (I_D-V_{GS} curves) in linear region at 25 °C and 150 °C (which is usually considered an upper temperature bound), the R_{ON} Temperature Ratio (RTR) can be calculated at the nominal on-state V_{GS} (Fig. 3).

This temperature ratio (R_{ON}(150 °C)/R_{ON}(25 °C)) has been studied in order to understand how each different resistive contribution of the structure impacts on the overall on-resistance of the device (see Fig. 4).

Then, the modulation of the RTR induced by variations on the nominal Magnesium (Mg) concentration level and on its thermal activation process has been analyzed in detail.

Results and discussion

Differently from 650 V p-GaN HEMTs (L_{GD} ≤ 20 µm, L_G ≤ 2 µm), where the resistance in the access regions represents the main contribution on the overall on-resistance [12,13], in 100V-rated devices (L_{GD} ≤ 2 µm, L_G ≤ 1 µm), a relevant weight is represented by the resistance under the p-GaN gate, namely the channel resistance (R_{CH}). The analysis of the temperature behaviour of each resistive portion of the HEMT has revealed that, for the technology under evaluation in this paper, R_{CH} has an increasing impact on R_{ON} at higher temperature, as reported in Fig. 5.

Therefore, R_{CH} has been further investigated (Fig. 6) in a dedicated structure with increased gate length (L_G >> L_{GD}+L_{GS}).

The overall temperature variation of R_{CH} is dependent on both the threshold voltage (V_{TH}) increase and the transconductance (g_m) reduction. Comparing the temperature behaviour of the STD process p-GaN HEMT with the one of an equivalent HEMT without p-GaN (as the one depicted in Fig. 2), it is observed that the positive V_{TH} shift is induced only in the case of p-GaN gate while the V_{TH} is quite stable in D-mode

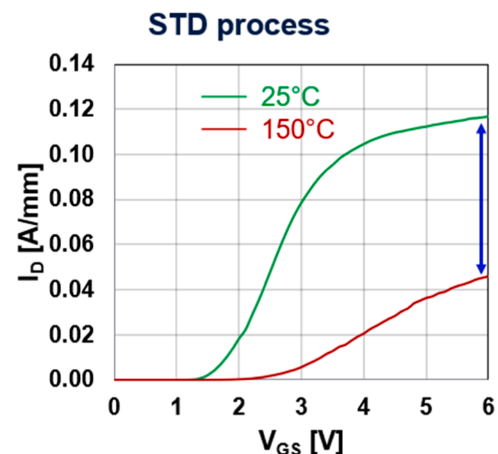

Fig. 3. I_D-V_{GS} curves acquired with V_{DS}=0.5 V (linear region) at 25 °C and 150 °C on tested devices of the STD process. R_{ON} is extracted at VGS=6 V as the ratio between V_{DS} and I_D.

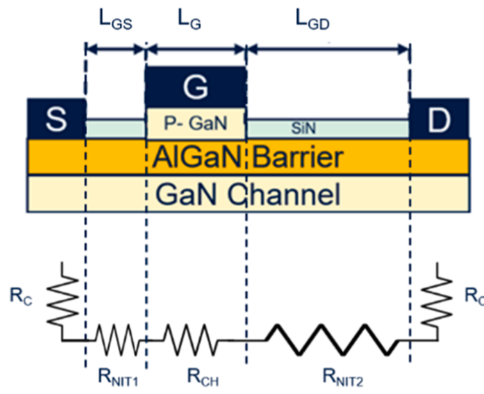

Fig. 4. R_{ON} division for tested devices. R_C: contact resistance, R_{NIT1}: Source-Gate access region resistance, R_{CH}: channel resistance and R_{NIT2}: Gate-Drain access region resistance.

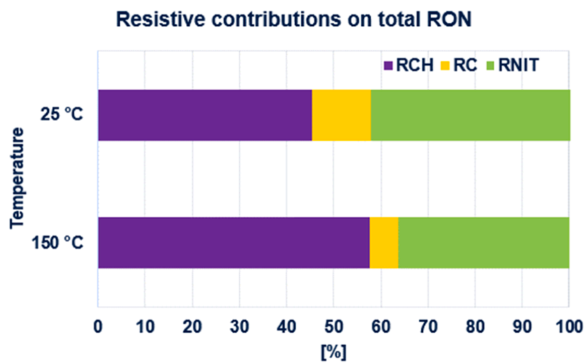

Fig. 5. Comparison between the different R_{ON} components at 25 °C and 150 °C (STD process). R_C: total contact resistance, R_{NIT}: total access region resistance, R_{CH}: channel resistance.

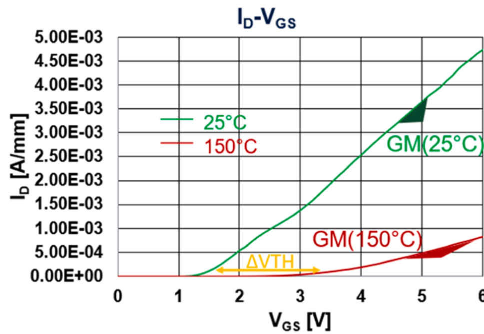

Fig. 6. I_D-V_{GS} curves acquired with V_{DS}=0.5 V at 25 °C and 150 °C on dedicated structures for R_{CH} study.

devices sharing the same epitaxial structure up to the AlGaN barrier layer. The effect of a p-GaN gate on the V_{TH} temperature shift could be explained by the fact that, as temperature modifies the gate leakage, there is actually a change of the net flow of hole injection (from gate metal p-GaN) and electron trapping (from 2DEG to p-GaN/AlGaN) at positive V_{GS} and this can be related to a different threshold voltage shift [14,15]. (Fig. 7)

Moreover, it has been proved that g_m decrease at high temperature of the STD process DUT can be linked not only to the mobility degradation [16–18] but also to the decrease of the gate capacitance (Fig. 8), given the fact that, in a field-effect transistor, gm is proportional to both mobility and gate capacitance [6].

Based on these considerations, two process variations are then proposed to improve device performances with temperature, while ensuring the correct normally-off behaviour: 1) process A consists in an improved thermal annealing for the Magnesium activation in the p-GaN gate; 2) process B is instead related to a proper increase of the nominal Magnesium concentration of the p-GaN.

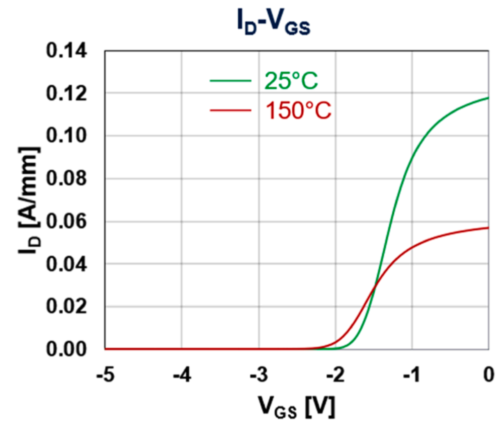

Fig. 7. I_D-V_{GS} curves acquired with V_{DS} = 0.5 V at 25 °C and 150 °C on a D-mode device.

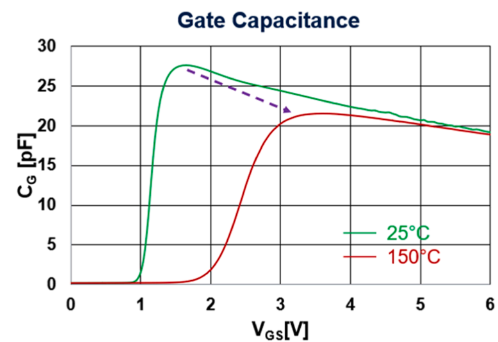

Fig. 8. C_G-V_{GS} curves acquired with f = 1 MHz at 25 and 150 °C on dedicated structures for R_{CH} study (STD process).

As shown in Figs. 9 and 10, both process A and B allow to reach a similar reduced R_{ON} temperature ratio: however, process A is effective in obtaining a reduced V_{TH} shift at high temperature while process B helps in improving the maximum transconductance at 150 °C.

(1) Temperature Effect on RON-degradation induced by Off-state Drain Voltage Stress in 100 V p-GaN HEMTs.

Experimental

The experimental procedure for dynamic-R_{ON} evaluation under off-state drain voltage stress is schematically depicted in Fig. 11.

The fresh R_{ON} (1) is measured by pulsing V_{GS} (2 μs) to V_{GH}=6 V, while V_{DS} is kept at V_{DL}=0.5 V to bias the DUT in its linear region. Then (2) an off-state stress is performed by biasing the DUT at V_{GL}=0 V and V_{DH}=50 V for a predefined time interval (stress-time). At the end of the stress (3) V_{GS} is pulsed again to V_{GH} to acquire the RON value after stress.

Results and discussion

Devices Under Test (DUTs) are 100 V p-GaN gate AlGaN/GaN HEMTs grown on Silicon substrate characterized by process B-like improvements (as shown in section 1). The fresh I_D-V_{GS} characteristics shown by tested devices at different temperatures (T) are reported in

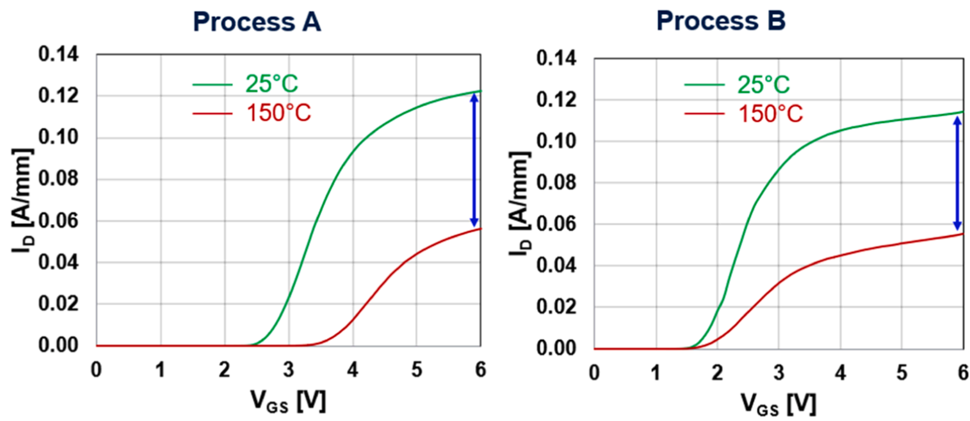

Fig. 9. Comparison between I_D-V_{GS} characteristics obtained on (a) Process A and (b) Process B devices at 25 and 150 °C.

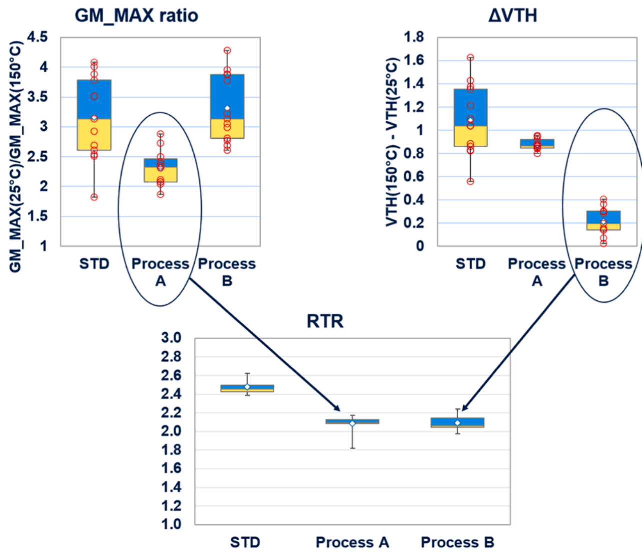

Fig. 10. Comparison between the RTR shown by the standard process (STD), improved process A and improved process B (red circles represent the actual measurements on 13 on-wafer devices).

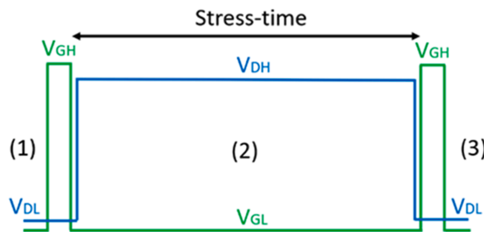

Fig. 11. Measurement sequence employed for Dynamic-R_{ON} measurement. The fresh R_{ON} is acquired by pulsing V_{GS} to 6 V (1). Then an off-state drain voltage stress is applied to the DUT for a given stress-time (2) and the post stress resistance is evaluated by pulsing again V_{GS} to 6 V (3).

Fig. 12.

An increase in T yields a lower current level in linear region, due to a reduced electron mobility [19]. This causes an almost linear increase of the fresh on-state resistance (R_{ON0}) with increasing temperature (see Fig. 13).

In particular, in the case of negligible V_{TH} shift with temperature (as observed on process B devices analyzed in section 1), the RTR and the MTR (Mobility Temperature Ratio) can be quite well correlated, as shown in Fig. 14.

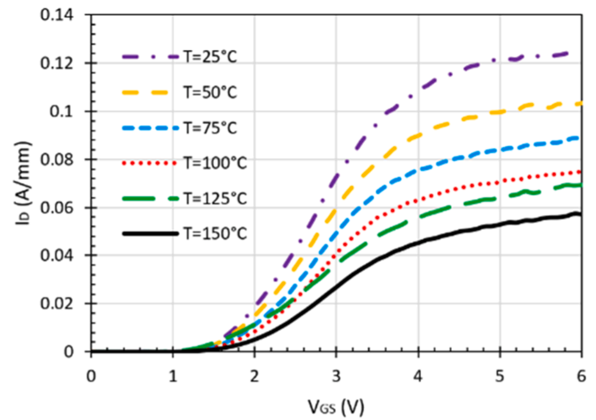

Fig. 12. I_D-V_{GS} curves acquired at different temperatures in the 25 to 150 °C range. An increase in T yields a reduction in the triode current due to a reduced electron mobility.

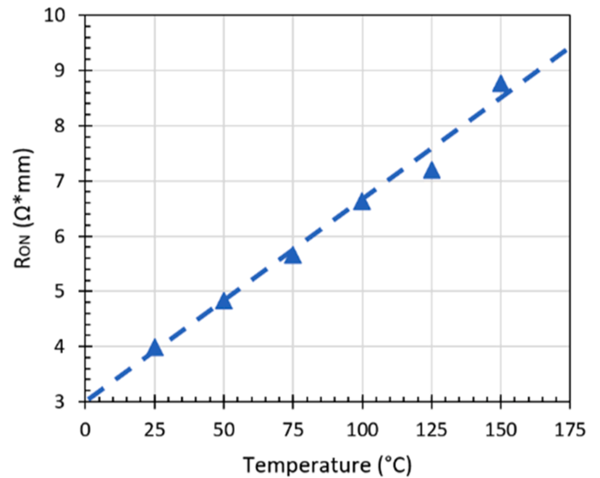

Fig. 13. Fresh on-state resistance (R_{ON0}) acquired at different temperatures in the 25 to 150 °C range. An increase in T yields an increased resistance due to a reduced electron mobility.

At this point, the experimental procedure was applied on tested samples, by varying the stress-time between 15 s and 1000s to see the impact of this parameter on the amount of R_{ON} degradation.

In Fig. 15 we reported the R_{ON}-degradation (R_{ON}/R_{ON0}) obtained for

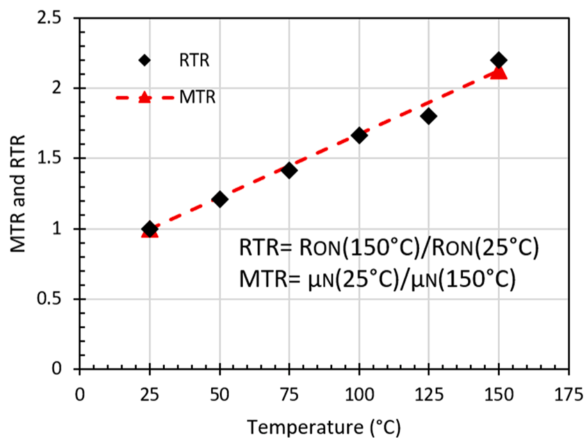

Fig. 14. Normalized R_{ON} and electron mobility (μ) temperature ratio with respect to 25 °C. 2DEG mobility of the access regions has been evaluated through measurements on dedicated structures.

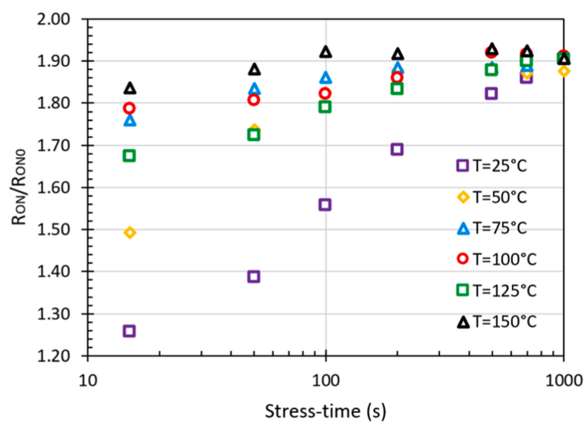

Fig. 15. Normalized R_{ON}-degradation (R_{ON}/R_{ON0}) obtained with different stress times (between 15 s and 1000s) and different temperatures (between 25 °C and 150 °C).

different stress times and different temperatures in the 25 °C to 150 °C range.

Looking at Fig. 15, we see two important effects: (i) At 25 °C the R_{ON}-degradation increases with the applied stress-time and requires 1000s to reach a steady state condition. (ii) At higher T values, the time required for reaching the R_{ON}/R_{ON0} equilibrium reduces, yielding a similar level of degradation in steady state that is weakly affected by the DUT temperature.

To fairly compare the R_{ON}/R_{ON0} extracted at different temperatures, we consider the results obtained for a stress-time of 1000s. In fact, this time length was found to be sufficient to yield a steady state degradation on the tested device for the whole temperature range considered.

We immediately observed that the R_{ON}/R_{ON0} induced at different T are quite aligned, indicating that the amount of degradation is insensitive to temperature. This is valid if and only if two important conditions are satisfied: (i) the stress time is long enough to appreciate the complete degradation induced at equilibrium and (ii) no additional trapping/de-trapping mechanisms come into play at higher temperatures.

To assess the generality of the experimental evidence, we characterized several devices with the same experimental approach, collecting the results reported in Fig. 16.

The results obtained for all tested samples presented quite aligned degradation (inside the data variability range) at different temperatures. This is totally in line with the theoretical expectations. In fact, the ratio R_{ON}/R_{ON0} is directly proportional to the ratio between the charges

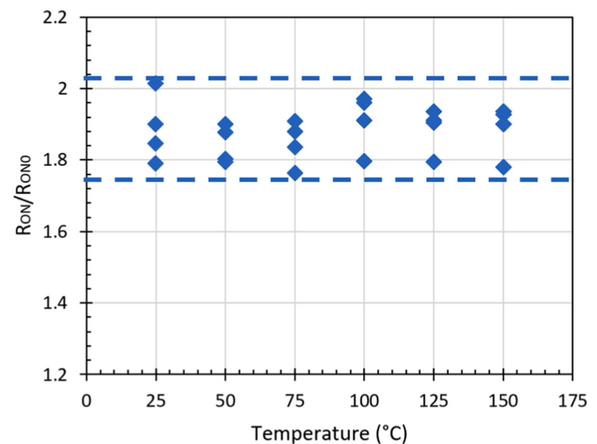

Fig. 16. Normalized R_{ON}-degradation (R_{ON}/R_{ON0}) obtained at different temperatures for a stress time equal to 1000s.

available in the two-dimensional electron gas (2DEG) in the pre- and post-stress conditions (Q0/Q). Assuming that the trapping/de-trapping mechanism occurring in the considered T range is always the same, the trapped charge variation ($\Delta Q = Q0 - Q$) induced by the applied stress will be weakly affected by temperature. In fact, since temperature is expected to have approximately no impact on the 2DEG charge density, the ratio Q0/Q is expected to be constant at different T (within the range under exam), yielding the same R_{ON}/R_{ON0} degradation.The fact that all the tested devices showed a similar behaviour indicates the generality of the phenomenon. Accordingly, the on-state resistance degradation can be invariantly measured in the whole 25 °C to 150 °C range, providing consistent results.

This suggests the possibility to test the R_{ON} degradation at a single temperature and extrapolate the R_{ON} after stress in the whole temperature range by simply measuring its fresh value (R_{ON0}) at each considered temperature. This could significantly speed-up the time required for a complete dynamic-R_{ON} characterization, provided that, (i) the degradation is evaluated at equilibrium and (ii) no additional trapping/de-trapping mechanisms are introduced by operations at higher temperatures.

(1) DC and Load Pull characterization of RF GaN-based HEMTs with increased aluminum content of the AlGaN barrier and Trade-Off with HTRB performances.

Experimental

DC and Load Pull characterizations can be performed to evaluate the performances of RF GaN-based HEMTs in terms of different electrical parameters for on-wafer devices. In particular, through DC measurements, one of the main parameters to be evaluated is the maximum drain current (I_{max}) supplied by the transistor in saturation regime (evaluated at $V_G = 2$ V and $V_{DS} = 7$ V for the DUT, as shown in Fig. 17). On the other hand, harmonic Load Pull measurements, performed through Mixed-Signal Active Load Pull system by Anteverta–mw (MauryMicrowave), can be exploited to extract RF performances in term of gain, output power (P_{out}) and efficiency [20]. The DUT has been characterized with a single-tone pulsed 2nd harmonic Load Pull at 3.5 GHz of fundamental frequency. Pulsed-mode is used to avoid self- heating (on-time = 10us; duty cycle = 10 %). The quiescent bias has been set with the objective of extracting RF performances in class AB operation (I_D = 20 mA/mm and V_{DS} = 50 V) [21].

Apart from DC and RF measurements, it is also important to characterize devices in terms of expected lifetime and this is usually measured through reliability tests. One of the mandatory reliability tests for device qualification is the HTRB (High Temperature Reverse Bias),

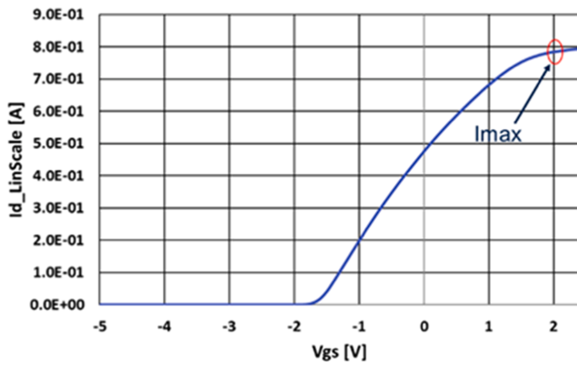

Fig. 17. Example of typical transfer characteristic measurement to extract the maximum drain current in saturation condition (V_G = 2 V, V_{DS} = 7 V).

which has the objective of stressing the device with a high electric field at high temperature to accelerate the degradation and failure phenomena. The stress conditions depend on the specific application of the device and can induce different failure mechanisms [22]. The HTRB test has been performed on the DUT to evaluate its reliability behaviour.

Results and discussion

Three different trials characterized by increasing aluminum concentration for the AlGaN barrier (see Fig. 2) have been processed in order to deeply investigate the effect of this parameter on the overall performances of the device. The main results of these splits are reported in the following figures (where the reference trial corresponds to an aluminum content of 23 %). (Fig. 18, Fig. 19, Fig. 20).

A clear linear correlation between higher I_{max} and increasing Al mole fraction has been observed and the same trend is maintained for the P_{out} versus Al%. This finding could suggest that the best choice in terms of AlGaN barrier relies in the highest possible Al%. However, the reliability aspect must also be taken into account. In other terms, an optimization of the Al content of the AlGaN barrier needs to be found, in order to match both the DC/RF performances and reliability requirements. As a matter of fact, the results with increased Al% show indeed a possibility to improve DC and RF parameters [23], but the experimental data also suggests worse reliability behaviour, as shown in Fig. 21.

In the graph of Fig. 21, it is well visible that there is a worsening of the device behaviour (from reliability point of view) with increasing of aluminum concentration in the AlGaN barrier. This confirms the importance of an optimized Al% to obtain adequate robustness to failure mechanisms.

Conclusions

(1) A study of the high temperature behaviour of the on-resistance in 100 V p-GaN transistors has been carried out by analysing each different resistive portion along the pitch of the transistor. As a result, the relevance of the resistive component under the p-GaN gate in the 100 V technology under exam has been proved, showing that its increase with temperature is caused by the positive VTH shift and by the gm degradation. To improve the high temperature behaviour of the device, while preserving normally-off operation, two process variations have been proposed, consisting of A) an improved thermal annealing for Mg activation; B) an increase in the nominal Mg concentration. It has

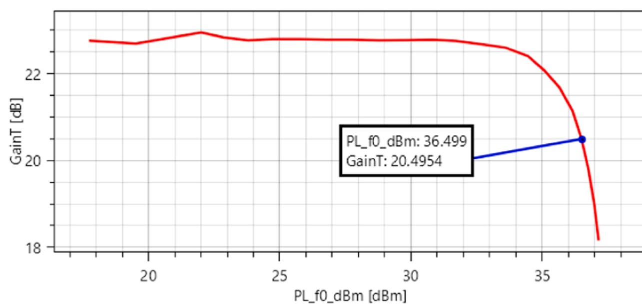

Fig. 18. Example of typical RF Load Pull measurement to extract the maximum P_{out} at 2.5 dB gain compression point (gain vs P_{out}).

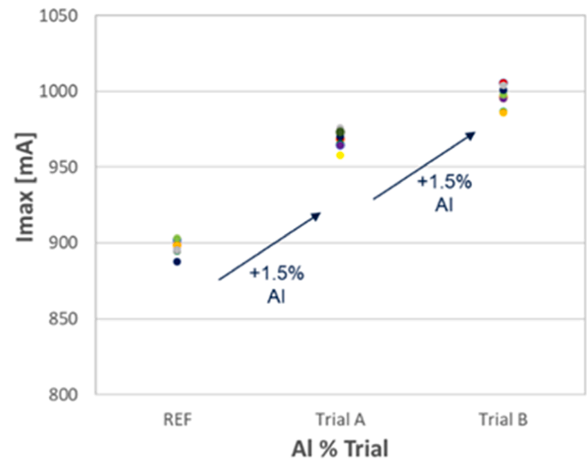

Fig. 19. Linear correlation between I_{max} and Al% (DC measurements).

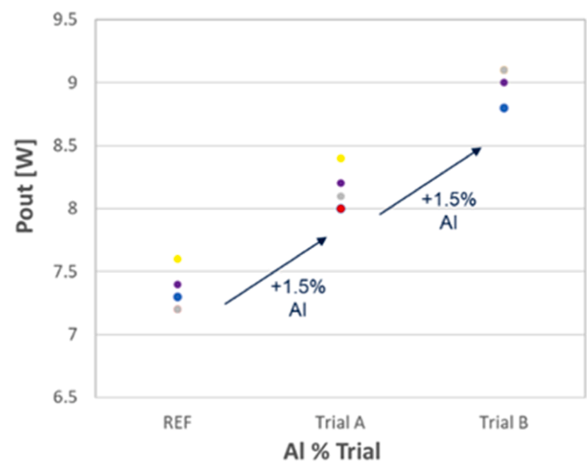

Fig. 20. Linear correlation between P_{out} and Al% (Load Pull measurements).

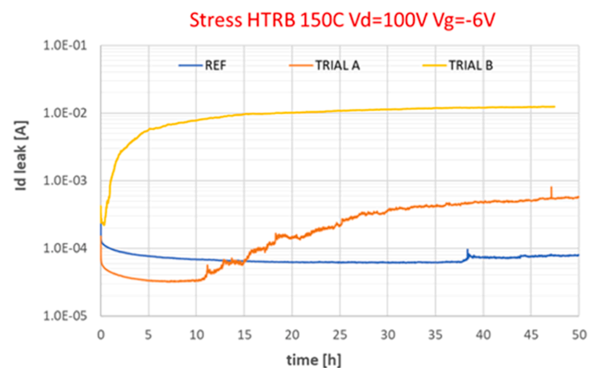

Fig. 21. Monitoring of the DUT behaviour during HTRB stress (T = 150 °C, V_{DS} = 100 V, V_G = −6 V) for different Al% trials.

been shown how both processes are effective in reducing the RON Temperature Ratio, acting respectively on the gm degradation and on the VTH shift. This further confirms the dominance of the RCH component on the total on-resistance of 100 V p-GaN HEMTs and traces the road for further improving its thermal stability.

(2) The temperature effect on the RON-degradation induced by off-state drain voltage stress has been studied for 100 V p-GaN HEMTs. The invariance of the RON-degradation in temperature has been observed on several samples, suggesting the generality of the observed behaviour. This finding allows to reduce the number of characterizations required for evaluating the RON degradation under different thermal conditions.

(3) The trade-off between DC/RF performances and reliability specifications has been analyzed by comparing devices with increasing aluminum concentration in the AlGaN barrier. In particular, it has been shown that an Al% increase of the AlGaN barrier can lead to improved saturation currents and higher output power levels while producing a detrimental effect on the lifetime of the device, as observed through HTRB tests. Therefore, an optimal Al% must be chosen for ensuring adequate device robustness while targeting sufficiently high current and power levels.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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