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An Introduction to Nanomaterials for Nanopackaging

James E. Morris, *Fellow, IEEE*

Abstract— The multiple purposes of an electronics “package” include the provision of mechanical support to the silicon chip, for example, and protection from the environment, the delivery of power in and the facilitation of heat out, and the reliable input and output of information signals, whether electrical or optical. In the age of heterogeneous integration, this includes the internal conversion of signal modes between multiple technologies within the package, while maintaining the traditional requirement of reliable information transmission between packages, e.g., on a traditional circuit board. This article presents some selected examples of nanopackaging, i.e., the application of nanotechnologies, (nanoparticles, carbon nanotubes and graphene here,) to electronics packaging.

Index Terms—Carbon nanotubes, CNTs, graphene, nanopackaging, nanoparticles.

I. INTRODUCTION

IMAPS defines electronics packaging as “Everything in electronics between the chip and the system,” but the term is usually applied to all technologies involved in the encapsulation of chips (1st level) and their subsequent assembly into board level systems (2nd level.) Over the years, the field has morphed from the materials reliability issues of glass/metal seals in vacuum tubes, to ceramic and plastic dual in-line encapsulation, to 2.5D chiplet redistribution, and from wire-bond interconnect to flip-chips. Currently, the industry is facing the challenges of the heterogeneous integration of multiple technologies and functions into a single package and the evolution of the “2.5D” redistribution technology into true 3D interconnections which require through silicon vias (TSVs), but with ever increasing on-chip device densities and clock frequencies, thermal dissipation remains packaging’s biggest problem, as it was for vacuum tubes. It has been said that “All electronics problems are materials problems” [1] and so the industry’s integration of nanotechnologies is primarily in advanced materials.

II. NANOPARTICLES

Most applications of nanoparticles are based on their high surface-to-volume ratios (S/V) and the greater chemical reactivity of the dangling surface bonds, which translates for example into increased metal-to-polymer or metal-to-ceramic bonding strengths in nanocomposites in comparison to micro-composites. In addition, nanoparticles are more likely to be single-crystal and therefore inherently stronger than

polycrystalline microparticles. The weaker bonding of the surface atoms to the internal lattice facilitates their surface diffusion and nanoparticle sintering [2,3]. It also accounts for the melting point (MP) depression observed in metallic nanoparticles [4], but note that the normalized curves of nanoparticle melting points versus size show that the effect is less than often assumed in the literature, with an approximate rule-of-thumb that 5nm radius particles are required for a 5% reduction from the absolute bulk value, e.g., from 490K to 465.5K (192.5°C) for no-Pb solder [5]. Of course, the coalescence of multiple solder nanoparticles into a continuous bulk MP film following lower temperature melting is necessary to take advantage of MP depression, and the dynamics of this process presents challenges. However, MP depression follows the same pattern for nanowires based on the nanowire radius as for nanoparticle radii, and two nanowires can be successfully soldered in this way [6]. In fact, most of the “nano-solder” papers in the literature are based on nanoparticle sintering rather than MP depression, and more likely for Cu interconnections than solder [7]. The difference in melting and sintering is that the internal lattice structure must be destroyed and reconstituted in the former whereas sintering is primarily due to surface diffusion even at ambient temperatures, with a sintering time, t , relationship with the particle radius, R , and neck radius, X , of $t \propto (X/R)^2 R^4$ [8] or approximately $t \propto R^4$ if $X \sim R$. So in the move from the micro to nano scales, particle sintering can apparently be accomplished 10^{12} times faster.

Metallic nanoparticle lines can be deposited on circuit board substrates by ultrasonic or pressure driven print heads for subsequent oven or laser sintering into electrical interconnect [9] but it has been shown that polymer coated Ag nanoparticles can be completely sintered within one hour of being dipped in methanol [10]. In developing an undergraduate lab experiment, the author found that the resistivity of a Ag nanoparticle suspension abruptly drops within a few minutes of the addition of water, methanol, or ethanol as appropriate for the removal of the polymer coating which is necessary to prevent premature coalescence. Notwithstanding that sintering of such nanoparticle films can be accomplished at room temperature, sintering is faster and the resistivity lower at higher temperatures due to faster diffusion and lower porosities [9-11]. The grain size, film density and conductivity can all be raised by subsequent annealing.

Ag nanoparticles can also be added to isotropic conductive adhesives (ICAs) which are typically comprised of bimodal distributions of Ag flakes and powder (spheres) in an epoxy composite. The primary benefit was originally seen to be a reduction of the conductivity percolation threshold since the

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functional ICA resistivity increased [12]. In fact, past the percolation threshold, it can be shown that the Ag added as nanoparticles, e.g., by precipitation from AgNO_3 , would have been more effective in resistivity reduction if it was added as additional flakes [13]. This effect was attributed to increased numbers of contacts along the percolation paths and reduced electron mean free paths within the nanoparticles, but in addition the reason Ag is used in ICAs is that it forms a conducting oxide layer on the surface which resists further oxidation and sintering. With the addition of suitable surfactants, the nanoparticles provide a sintering role between the flake and powder components and significantly reduce the ICA resistivity [14]. A further dramatic resistivity has been demonstrated by the use of sintered nanoscale dendritic Ag particles instead of flakes [15].

A recent packaging trend has been to get discrete passive components off the circuit board surface by embedding them inside to provide more surface space for the active silicon components. Thin film cermet (ceramic/metal) resistors have been utilized for decades, balancing the positive temperature coefficient of resistance (TCR) of the continuous metallic paths with the negative TCR of electrostatically activated tunneling mechanism of the nanoscale metal islands. For power-supply, very high dielectric constant (~ 2000) capacitors have been fabricated as Ag/epoxy composites, (with the Ag precipitated in situ from AgNO_3), with the Ag nanoparticles acting as Coulomb blocks to limit DC conduction at low fields [16]. But this is actually a low-density cermet structure and suffers from very high dielectric loss (≤ 1.0). Nanodielectrics can also achieve stable RF capacitors. One such approach is to stack two nanoscale thin films of positive and negative temperature coefficients of capacitance (TCCs), with thicknesses and areas d_i and A_i ($i=1,2$) with series capacitance

$$C = [(d_1/\epsilon_1 A_1) + (d_2/\epsilon_2 A_2)]^{-1}$$

and zero TCC if

$$d_1/d_2 = -(\epsilon_1/\epsilon_2)(TCC_2/TCC_1),$$

where ϵ_i are the dielectric constants [17]. For embedded inductances and transformers, we need high permeability and low coercivity, which are normally mutually exclusive, but can be obtained simultaneously with grains or nanoparticles less than 10nm in size [18] that need to exchange-coupled to each other to retain high permeability, while also being in thinfilm format to suppress eddy currents.

The study of reliability pervades the electronics packaging literature, from basic theory to modeling to testing to design strategies. Piezoresistive Si strain sensors, for example, have been integrated into test packages to monitor thermomechanical stress fields [19], but nanosensors offer much greater sensitivity through the exponential dependence of quantum-mechanical tunneling currents on gap widths [20]. Such sensors could take the form of ultrathin films of discrete metal nanoparticles [21] or single electron transistors. The modulation of the tunneling gap width can also be employed for the detection of H_2 as a byproduct of galvanic corrosion in such films of Pd nanoparticles, which expand as they absorb H_2 , increasing the inter-particle tunneling current [21-26].

It is worth noting in passing that the addition of TiO_2 nanoparticles reduces the formation of brittle Cu_6Sn_5 intermetallic compounds in Sn0.7Cu solder, and reduces the contact angle, and hence increases adhesion to the Cu substrate for Sn3.5Ag0.5Cu [27].

III. CARBON NANOTUBES (CNTs)

Following on from the last item, single-wall CNTs (SWNTs) in the grain boundaries have been shown to improve multiple properties of both eutectic Sn-Pb and Pb-free solders, by varying amounts depending on the specific property, typically 10-30% but significantly more (6x) for the no-Pb creep rupture times, and $\sim 20\%$ for the no-Pb contact angle [28]. Multi-wall CNTs (MWNTs) have been similarly found to decrease the contact angles for no-Pb solders by $\sim 15\%$. CNTs have the reputation of better electrical conductivity than more conventional materials by virtue of their high electron mobility, (around 70x that of Si,) and electron mean free path (mfp $\sim 1-3\mu\text{m}$), but in many interconnect applications care must be taken that the CNTs have open ends for effective electrical contact, roughly halving via resistances after steam or plasma processing [29]. For the CNT to have a conductance advantage over Cu or Ag, for example, the length in question must be greater than the electron mfp in the metal before the larger CNT mfp becomes significant. So CNTs are generally only seen to be advantageous over longer lengths $\geq 1\mu\text{m}$, i.e., typically for power delivery rather than for signals or in through-Si vias (TSVs.) However, this judgment is usually based on dc comparisons and for high frequency signals, $\geq 1\text{GHz}$ say, skin effect comes into play and although the metal inductance goes down, the dominant effect is the resistance increase with frequency [30]. In many cases, the advantage of CNTs over Cu is the greater maximum current limit ($\sim 1000\text{x}$) which means no electromigration issues, a growing problem for microelectronics interconnect, and suggests the use of CNT bundles for contact bumps, (with the added advantage of flexibility) [31]. CNT TSVs have been demonstrated [32-33] and modeled [34]. Another under-appreciated property of CNTs is the negative coefficient of thermal expansion (CTE) at around 300K [35]. With almost all packaging materials, polymers, ceramics, and metals, having significantly higher CTEs, the mechanical reliability issues at high temperatures are almost all driven by CTE mismatch which CNT composites can reduce, in Cu/CNT composite TSVs in particular [36]. A particular Cu-TSV CTE mismatch problem is the extrusion of Cu from the TSV due to its higher CTE than Si's, and it has been shown that a 29% aligned CNT content can completely match the Cu-CNT axial CTE to Si to zero out this Cu pumping [37]. CNTs added to Cu interconnect lines can also reduce electromigration significantly [38] and CNT antennas are being studied for interchip communication within the package at up to tens of THz [39].

Another well-known CNT property, in addition to high mechanical strength and electrical conductivity, is high thermal conductivity, which suggests that aligned SWNTs offer the best option for an order of magnitude improvement in thermal dissipation over the best conventional alternatives

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[40]. CNT bundles have been organized into columns separated by cooling fluid channels in a microstructure reminiscent of a traditional Cu-fin heat sink [41]. The problem is that while heat transfer from the CNTs adjacent to the channels is effective, the thermal transfer between internal CNTs in the fins is not. This problem can be solved by the lateral growth of secondary CNTs on the primary vertical CNTs, providing effective 3D heat transfer [42].

IV. GRAPHENE

CNTs are rolled up tubes of graphene, which was discovered much later. Graphene is also the fundamental component of graphite, the electronic properties of all three being governed by their sp^2 electron configuration. The single atomic layer graphene displays similar thermal conductivity as CNTs, but in 2D rather than 1D, and it is interesting to compare the thermal properties of graphite, graphene and CNTs with the sp^3 allotrope diamond [43]. Of particular note is that the 3000-5000 W/m.K figures often cited for graphene's thermal conductivity are only valid for a single one atom thick layer, and that every additional layer decreases the conductivity until it equals the thermal conductivity of high-quality graphite at 4 layers thick, and further degrades to the thermal conductivity of "regular" graphite at around ten layers [43]. The 2D form lends itself to heat spreader applications for hot spot mitigation on IC surfaces. Of the different heat spreader configurations compared, compression nearly doubles the thermal conductivity of laminated graphene flakes [44], while "few-layer" graphene beats CNT/polymer composites [45].

Of course, graphene is also highly conductive and the van der Waals forces between adjacent graphene layers in a stack that degrade the single layer properties can be defeated by intervening layers of FeCl₃ or other materials, permitting multi-layer graphene interconnects to act as single layers in parallel. The vision is to combine graphene nanoribbon interconnects with CNT TSVs in all-carbon electrical and thermal networks with the ultimate goal of integrating such a system with CNT FET logic.

IV. SUMMARY

Advances in packaging are predominantly driven by new materials with superior properties. Nanomaterials have enabled several such advances in high-performance interconnections, reliable encapsulants, improvements in processability, advanced dielectrics, new modalities of sensing functions, and new classes of thermal materials. This paper highlights the key classes of nanomaterials, viz., nanoparticles, nanowires and graphene, as the exemplary 2D material, and their roles in nanopackaging. While electrical interconnect performance has been described in this paper, these advantages extend to other functions such as magnetic properties, charge storage in capacitors, electromagnetic properties as metasurfaces and other domains, as described in the other papers of this special issue.

REFERENCES

[1] D. Seraphim, IBM-Endicott (1984)

- [2] H. Zhu and R.S. Averback, "Sintering processes of two nanoparticles: a study by molecular-dynamics simulations," *Phil. Mag. Lett.*, vol. 73 no. 1 pp. 27-33, 1996.
- [3] P. F. Asoro and D. Kovar, "In situ transmission electron microscopy and scanning transmission electron microscopy studies of Ag and Pt nanoparticles," *Acta. Mater.*, vol. 81 pp.173-183, 2014.
- [4] J. R. Sambles, "An electron microscope study of evaporating gold particles: the Kelvin equation for liquid gold and the lowering of the melting point of solid gold particles," *Proc. Roy. Soc. Lond. A*. vol. 324, pp. 339-351, 1971.
- [5] J. E. Morris, "Nanoparticle Properties," in *Nanopackaging: Nanotechnologies and Electronics Packaging, 2nd ed.*, J.E. Morris, Ed. Cham, Switzerland, Springer, 2018, ch. 6, pp. 201-217.
- [6] F. Gao and Z. Gu, "Nano-soldering of magnetically aligned three-dimensional nanowire networks," *Nanotechnology* vol. 21 115604, 2010, doi:10.1088/0957-4484/21/11/115604
- [7] J. Zürcher, K. Yu, G. Schlottig, M. Baum, M. M. Visser Taklo, B. Wunderle, P. Warszyński and T. Brunschweiler, "Nanoparticle assembly and sintering towards all-copper flip chip interconnects," in *Proc. 65th IEEE ECTC*, San Diego CA, USA, 2015. doi: 10.1109/ECTC.2015.7159734.
- [8] M. Ohring, *Materials Science of Thin Films: Deposition & Structure 2nd ed.*, Academic Press, 2002, pp. 395-397.
- [9] J. Felba "Silver Nanoparticles for Inkjet-Printed Conductive Structures in Electronic Packaging" in *Nanopackaging: Nanotechnologies and Electronics Packaging, 2nd ed.*, J.E. Morris, Ed. Cham, Switzerland, Springer, 2018, ch. 14, pp. 439-481.
- [10] D. Wakuda, M. Hatamura, and K. Suganuma, "Novel Room Temperature Wiring Process of Ag Nanoparticle Paste," in *Proc. 6th International Conference on Polymers and Adhesives in Microelectronics and Photonics*, Tokyo, 2007.
- [11] C. Weber, M. Hutter, S. Schmitz, and K.-D. Lang, "Dependency of the porosity and the layer thickness on the reliability of Ag sintered joints during active power cycling," in *Proc. 65th IEEE ECTC*, San Diego CA, 2015. doi: 10.1109/ECTC.2015.7159854.
- [12] Ulrich Behner, "Electrically Conductive Adhesive Contacts Characterised by the 1/f Noise Behaviour," Ph.D. dissertation, Fachbereich Elektrotechnik und Informationstechnik der Technische Universität Darmstadt (1999).
- [13] L. Fan, B. Su, J. Qu, C.-P. Wong, "Electrical and Thermal Conductivities of Polymer Composites Containing Nano-Sized Particles", in *Proc. 54th IEEE ECTC*, Las Vegas NV, 2004, pp. 148-154.
- [14] Y. Li, K. Moon, and C.-P. Wong, "Electrical Property of Anisotropically Conductive Adhesive Joints Modified by Self-Assembled Monolayer (SAM)", in *Proc. 54th IEEE ECTC*, Las Vegas NV, 2004, pp. 1968-1974.
- [15] B. Song, K.-S. Moon, and C.-P. Wong, "Stretchable and Electrically Conductive Composites Fabricated from Polyurethane and Silver Nano/Microstructures," in *Proc. 67th IEEE ECTC*, Orlando FL, 2017, pp. 2181-2186.
- [16] J. Lu, K.-S. Moon, J. Xu, and C.-P. Wong; "Dielectric Loss Control of High-K Polymer Composites by Coulomb Blockade Effects of metal Nanoparticles for embedded Capacitor Applications", in *Proc. 10th IEEE/CPMT Internat. Sympos. Adv. Packaging Mater.*, Irvine CA, 2005.
- [17] I. R. Abothu, B. W. Lee, P. M. Raj, E. Engin, P. Muthana, C. K. Yoon, M. Swaminathan, and R. R. Tummala, (2006) "Tailoring the temperature coefficient of capacitance (TCC), dielectric loss and capacitance density with ceramic-polymer nanocomposites for RF applications," in *Proc. 56th IEEE ECTC*, 2006, pp. 1790-1794.
- [18] G. Herzer, "Grain size dependence of coercivity and permeability in nanocrystalline ferromagnets," *IEEE Trans. Magn.*, vol. 26, pp. 1397-1402, 1990.
- [19] J. C. Suhling and R. C. Jaeger, "Silicon piezoresistive stress sensors and their application in electronic packaging," *IEEE Sensors Journal*, vol. 1, no. 1, pp. 14-30, June 2001.
- [20] B. T. Boiko, L. S. Palatnik, and A. N. Sinel'nikov, "Electric conductivity and structure of discontinuous metal films on dielectric," *Thin Solid Films* vol. 7 no. 5, pp. 305-311, 1971.
- [21] J. E. Morris, "Nanosensors for Electronics Package Reliability," in *Nanopackaging: Nanotechnologies and Electronics Packaging, 2nd ed.*, J.E. Morris, Ed. Cham, Switzerland, Springer, 2018, ch. 29, pp. 893-905.
- [22] A. G. Bishay, D. A. Abdelhady and A. M. Darwish, "Applicability of discontinuous palladium films as strain gauges," *J. Mater. Sci: Mater. Electron.* vol. 3 pp. 195-199, 1992, doi:10.1007/BF00695521

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- [23] S. El-Gamal, "Effect of strain on the I-V characteristics of discontinuous silver films and determination of their gauge factor," *J. Mater. Sci: Mater. Electron.* Vol. 24 (2013) pp. 4311-4315, doi:10.1007/s10854-013-1403-z
- [24] A. Barr, "The effect of hydrogen absorption on the electrical conduction in discontinuous palladium films," *Thin Solid Films*, vol. 41, pp. 217-226, 1977.
- [25] J. E. Morris, A. Kiesow, M. Hong, and F. Wu, "The effect of hydrogen absorption on the electrical conduction of discontinuous palladium thin films," *Int. J. Electronics* vol. 81 no. 4, pp.441-447, 1996.
- [26] J. van Lith, A. Lassesson, S. A. Brown, M. Schulze, J. G. Partridge and A. Ayesh, "A hydrogen sensor based on tunneling between palladium clusters," *Appl. Phys. Lett.* Vol. 91, 181910. 2016; doi: <http://dx.doi.org/10.1063/1.2802730>
- [27] L. C. Tsao, B. C. Wang, C. W. Chang and M. W. Wu, "Effect of nano-TiO₂ addition on wettability and interfacial reactions of Sn0.7Cu composite solder/Cu solder joints," in Proc. 11th ICEPT-HDP, 2010, Xi'an, China, pp. 250-253.
- [28] V. Kripesh, K. Mohankumar and A. Tay, "Properties of Solders Reinforced with Nanotubes and Nanoparticles", in *Proc. 56th IEEE ECTC*, San Diego CA, 2006.
- [29] Z. Xiao, Y. Chai, P. C. H. Chan, B. Chen, M. Zhao, and M. Liu, "Sacrificial removal of caps of aligned carbon nanotubes for interconnect application," in Proc. 59th IEEE ECTC, pp. 1811-1815, 2009.
- [30] K. Banerjee, H. Li, and N. Srivastava, "Current Status and Future Perspectives of Carbon Nanotube Interconnects," in *Proc. 8th IEEE NANO*, Arlington TX, pp. 432-436, 2008.
- [31] T. Wang and J. Liu, "Use of Carbon Nanotubes in Potential Electronics Packaging Applications," in Proc. 10th IEEE-NANO, Seoul, South Korea, pp. 160-166, 2010.
- [32] A. P. Graham, G. S. Duesberg, R. Seidel, M. Liebau, E. Unger, F. Kreupl, and W. Hönlein, "Towards the integration of carbon nanotubes in microelectronics," in *Proc. 14th European Conference on Diamond, Diamond-Like Materials, Carbon Nanotubes, Nitrides and Silicon Carbide (DIAMOND 2003 S.I.)*, 7-12 September 2003, Salzburg, Austria, *Diamond & Related Materials*, vol. 13 nos. 4-8, pp. 1296-1300, 2004.
- [33] T. Xu, Z. Wang, J. Miao, X. Chen, & C.M. Tan, "Aligned carbon nanotubes for through-wafer interconnects," *Appl. Phys. Lett.* Vol. 91, 042108, 2007. doi.org/10.1063/1.2759989
- [34] A. Gupta, B. C. Kim, S. Kannan, S. S. Evana, and L. Li, "Analysis of CNT based 3D TSV for emerging RF applications," in *Proc. 61st IEEE ECTC*, 2011.
- [35] H. Jiang, B. Liu, Y. Huang, and C. Hwang, "Thermal Expansion of Single Wall Carbon Nanotubes," *J. Eng. Materials & Technology*, vol. 126 pp. 265-270, 2004.
- [36] L. Aryasomayajula, R. Rieske and K.-J. Wolter, "Application of Copper-Carbon nanotubes Composite in Packaging Interconnects," in *Proc 34th ISSE*, Trstanska Lomnica, Slovakia, pp. 531-536, 2011.
- [37] A. Sinha, J. A. Mihailovic, J. E. Morris, H. Lu and C. Bailey, "Modeling Thermal Conductivity and CTE for CNT-Cu Composites for 3-D TSV Application," in *Proc. IEEE NMDC*, Monterey CA, Oct., 2010, pp. 262-266.
- [38] Y. Chai, P. C. H. Chan, Y. Fu, Y. C. Chuang, and C. Y. Liu, "Copper/carbon nanotube composite interconnect for enhanced electromigration resistance," in *Proc. 58th IEEE ECTC*, 2008.
- [39] P. Franck, D. Baillergeat and B. K. Tay "Mesoscopic model for the electromagnetic properties of arrays of nanotubes and nanowires: a bulk equivalent approach" *IEEE Trans. Nanotechnol.* Vol. 11 p. 964, 2012.
- [40] N. R. Pradhan, H. Duan, J. Liang, and G. S. Iannacchione, "The specific heat and effective thermal conductivity of composites containing single-wall and multi-wall carbon nanotubes," *Nanotechnology* vol. 20 245705, 2009. doi: 10.1088/0957-4484/20/24/245705.
- [41] Y. Fu, N. Nabiollahi, T. Wang, S. Wang, Z. Hu, B. Carlberg, Y. Zhang, X. Wang and J. Liu, "A complete carbon-nanotube-based on-chip cooling solution with very high heat dissipation capacity," *Nanotechnology* vol. 23 045304, 2012.
- [42] CiNTRA/XLIM-University of Limoges, 2016
- [43] A. A. Balandin, "Thermal Properties of Graphene, Carbon Nanotubes and Nanostructured Carbon Materials," *Nature Materials*. vol. 10 pp. 569-581, 2011.
- [44] H. Malekpour, K.-H. Chang, J.-C. Chen, C.-Y. Lu, D.L. Nika, K.S. Novoselov and A. A. Balandin, "Thermal conductivity of graphene laminate," *Nano Lett.*, vol. 14, pp. 5155-5161, 2014.
- [45] A. A. Balandin, "Excellent thermal properties of graphene and prospects of graphene's applications in thermal management," *Advancing Microelectronics*, vol. 38 no. 4, pp. 6-10, July/August 2011.



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