Performance Instability of 650 V *p*-GaN Gate HEMTs under Temperature-Induced Negative Gate Bias Stresses

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***Abstract*—In this article, the effect of negative gate bias stress and temperature on threshold voltage (V_{th}) and on-state resistance (R_{on}) instability of 650 V Schottky *p*-GaN gate HEMT devices from different manufacturers was explored. It is found that the there was an immediate V_{th} drift once the device was stressed. With the decrease in the negative gate voltage (V_{gs}), the variation in V_{th} (ΔV_{th}) and the variation in R_{on} (ΔR_{on}) became more significant. The measuring V_{gs} also played an important role when the testing V_{gs} was low. The low temperature can lead to the constant increment in ΔV_{th}, while ΔV_{th} decreased and then increased at elevated temperatures. The trapping/de-trapping speeds of electrons and holes were enhanced with temperature. The substantial increase in ΔR_{on} at high temperatures can increase the loss of devices to a great extent. The instability of the static performances of Schottky *p*-GaN gate HEMT devices are harmful to the real application.**

***Index Terms*—GaN HEMT, Negative Bias Stress Instability, Temperature.**

I. Introduction

Wide-bandgap power semiconductor devices, i.e. Silicon Carbide (SiC) [1] and Gallium Nitride (GaN) [2] are now key in power electronics applications. GaN High Electron Mobility Transistors (HEMTs) are in particular regarded as promising competitors in high frequency and high power density power electronic systems owing to the exceptional material properties [3]–[5]. In the pursuit of safe operation, accurate measurements [6] and to simplify gate driver designs [7], the adoption of normally-off GaN devices becomes important. Among many approaches to achieve normally-off design, the implementation of a *p*-GaN structure between gate metal and AlGaN/GaN junction to lift up the band diagram has received wide application due to the balance among cost, manufacturability and performance [8], [9]. Depending on the selection of the metal, doping of *p*-GaN stack and manufacturing process, the contact between *p*-GaN layer and gate electrode is either Ohmic type or Schottky type. The Ohmic *p*-GaN gate HEMT device has the merits of threshold voltage (V_{th}) stability, but it is a current-driven device, which has the drawback of large gate leakage current and high driving loss. The Schottky *p*-GaN technology can effectively reduce the gate current and achieve voltage-driven characteristics, which is advantageous to reduce the loss and facilitate the design of the gate driver.

Nevertheless, the introduced *p*-GaN layer between the gate metal and the barrier layer is floating in terms of electrical potential, as shown in Fig. 1. The existence of the Schottky *p*-GaN layer naturally forms two back-to-back connected p-n junctions. The *p*-GaN/gate electrode is a Schottky diode (J_1) with a parallel-connected capacitance (C_1), while the *p*-GaN/AlGaN/GaN forms a P-i-N diode (J_2) with a parallel-connected capacitance (C_2). The floating stack makes the device susceptible to various forms of stress and is likely to induce performance instability [10], [11]. Recently, the researchers have investigated the impact of static/dynamic gate voltage (V_{gs}) stress and off-state drain-source voltage stress on the device performance [12], [13]. Considering that the negative gate voltage is often applied to avoid false turn-on and the necessity of GaN HEMT devices to work under various temperatures, it is imperative to study these operating conditions on the performance instability of GaN HEMT devices. Therefore, negative gate bias stress/recovery tests were conducted on the Schottky *p*-GaN gate HEMT devices from different manufacturers under different gate biases and a wide temperature range. The experiment methodology was illustrated in Section II. The drift patterns and mechanisms in V_{th} and on-state resistance (R_{on}) under different test conditions were measured and analyzed in Section III. The conclusion was drawn in Section IV.

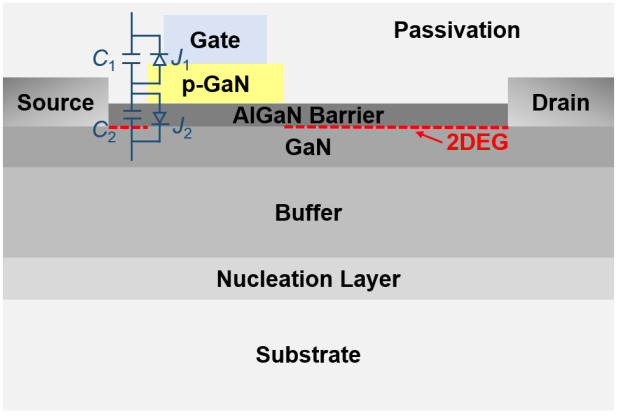

Fig. 1. Cross section of Schottky *p*-GaN gate HEMT.

II. Experiment Methodology

Two separate devices of different manufacturers are tested, GPI65015DFN as 650 V/15 A Schottky *p*-GaN gate HEMT and GS-065-018-2-L as 650 V/18 A Schottky *p*-GaN gate HEMT. The experimental procedure adhered to the typical measure-stress/recovery-measure sequence [14]. The schematic diagram of the test method is depicted in Fig. 2. In the bias stress test [15], negative V_{gs} of -2 V, -4 V, -6 V, -8 V, and -10 V was applied on the devices for 1000 sec. Subsequently, the electrical stress was removed in the recovery phase and the devices naturally recovered for another 1000 sec. To examine the static performance instability of GaN HEMT devices under various temperatures, the devices were stressed and recovered in the thermal chamber (TAS LTCL600) for each 1000 sec. The test temperature ranged from -50°C to 150°C, with a fixed V_{gs} of -10 V. To characterize the performance of the devices, the I-V curves of devices were collected by the source measuring unit (B2902A) after 1 ms, 10 ms, 100 ms, 1 sec, 10 sec, 50 sec, 100 sec, 500 sec, and 1000 sec during stress and recovery phases. The measuring V_{gs} was swept from 0-6 V, and drain-source voltage (V_{ds}) was chosen at a low value of 0.1 V intentionally to minimize the injection of electrons/holes during characterization. The resistance on the wires can be excluded by adopting four point probe method.

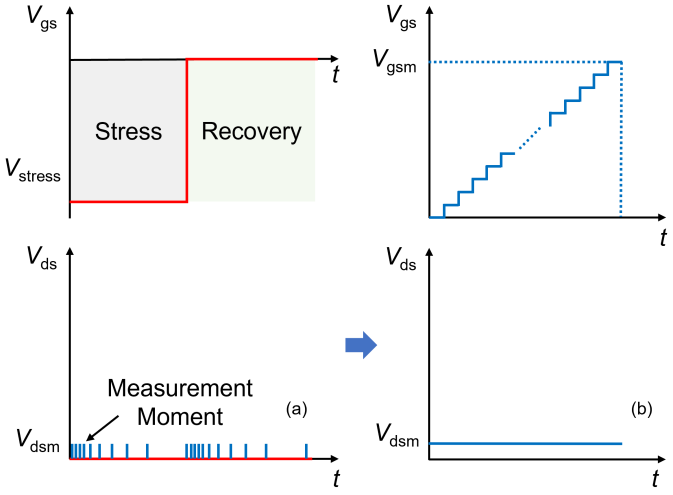

Fig. 2. Test schematic: (a) Stress & recovery phase, (b) I-V characterization.

III. Negative BTI Test Results and Analysis

A. Negative Gate Bias Stress Test under Different V_{gs}

The variations in V_{th} (ΔV_{th}) under different negative gate bias stress (NBTI) tests [16] are depicted in Fig. 3 and Fig. 4, respectively. ΔV_{th} is defined as the change in V_{th} during the stress and recovery phases compared with the initial V_{th} at each group of the test. For the GPI65015DFN GaN HEMT device, a sharp ΔV_{th} increase of 0.4 V happened once the stress was applied, regardless of the magnitude of V_{gs}. At low V_{gs} of -2 V, ΔV_{th} kept decreasing until the last data collection point. With the decrease in test V_{gs}, ΔV_{th} started to increase at earlier time points. During the recovery phase, a voltage jump also happened after applying the first measuring voltage. Then, V_{th} slowly returned to the initial value at a similar speed under all conditions. As for the GS-065-018-2-L GaN HEMT device, a sharp initial ΔV_{th} jump was observed as well, which was voltage-related and was higher than the GPI65015DFN device. Besides, ΔV_{th} of the GS-065-018-2-L device kept decreasing at -2 V, while it decreased before 500 sec during stressing and finally increased at 1000 sec at other test V_{gs}. The turning point of ΔV_{th} occurred much slower than the GPI65015DFN device. In the recovery phase, ΔV_{th} reduced at a equivalent speed, similar to the GPI65015DFN device.

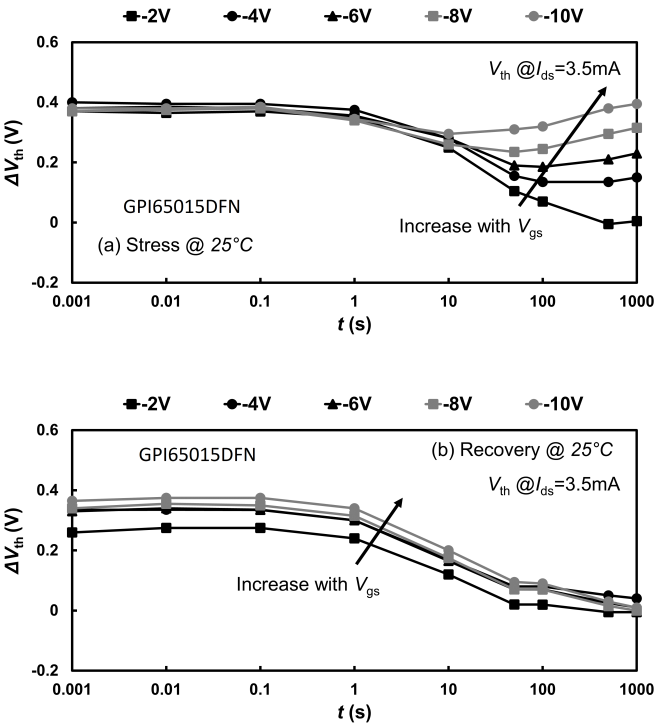

Fig. 3. Shift of ΔV_{th} of GPI65015DFN device in negative gate bias test at different V_{gs}: (a) Stress phase, (b) Recovery phase.

Under the negative gate bias stress, the Schottky diode J_1 of GaN HEMT devices was forward biased and the P-i-N diode J_2 was reversed biased. The barrier height of the gate metal/*p*-GaN was reduced, which facilitated the electron tunneling from the gate metal to the *p*-GaN layer and the hole emission from the *p*-GaN layer to the gate metal [17]. As the gate bias became more negative, more electrons were injected to the gate *p*-GaN stack and more holes were emitted to the gate metal. The progressively deficient holes and increased ionized negative acceptors in the *p*-GaN layer induced the increase in ΔV_{th} and the right shift in I-V curves for the GPI65015DFN device, especially at low V_{gs} tests. As for the GS-065-018-2-L device, ΔV_{th} demonstrated a slower shifting speed, which was caused by the difference in trapping/de-trapping time constant of electrons and holes

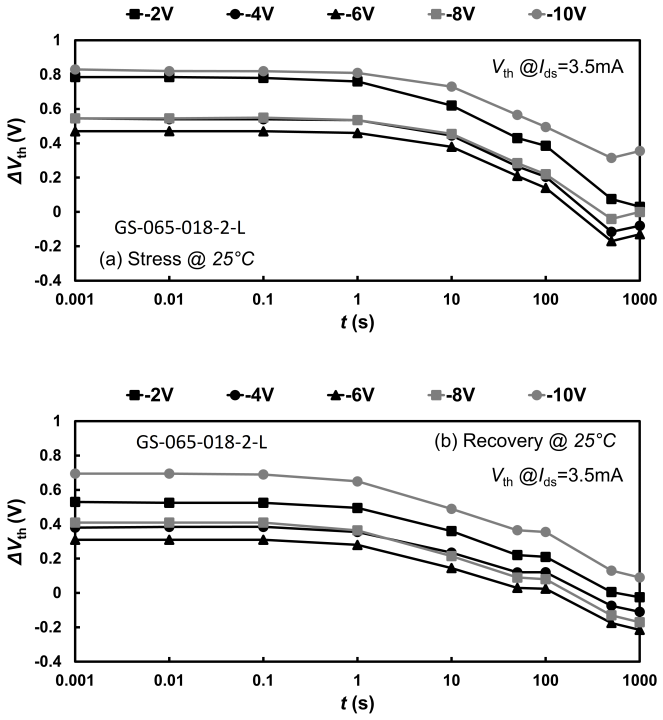

Fig. 4. Shift of ΔV_{th} of GS-065-018-2-L device in negative gate bias test at different V_{gs}: (a) Stress phase, (b) Recovery phase.

due to different device technology. It should be mentioned that for both devices, an initial V_{th} jump was observed. Since positive V_{gs} was applied to characterize the device performance, the testing V_{gs} shortly induced the reverse bias of J_1 and the forward bias of J_2. In this transient, holes can accumulate at the p-GaN/AlGaN interface or even trapped in the AlGaN layer, while the electrons were injected from the 2DEG (Two-Dimensional Electron Gas). However, the release of electrons was much faster than the emission of holes [14], [18], which led to the transient deficiency of positive charges and increased in V_{th}. During the recovering phase, the injected electrons and holes started to drift back to the original state and V_{th} gradually reduced to original values.

The variations in R_{on} (ΔR_{on}) of GPI65015DFN and GS-065-018-2-L devices under different negative gate bias conditions are demonstrated in Fig. 5 and Fig. 6, respectively. Likewise, ΔR_{on} is defined as the variance of R_{on} in comparison to the initial R_{on} measured at the beginning of each test. For the GaN HEMT device from GPI65015DFN, ΔR_{on} increased with the decrease of the applied V_{gs}, and the obvious change in ΔR_{on} was seen after 50 sec. During the recovery, ΔR_{on} increased at the -2 V test, while ΔR_{on} decreased under the rest of test conditions. Regarding the GS-065-018-2-L GaN HEMT device, ΔR_{on} constantly decreased during the stressing phase and continuously increased during the recovery phase at the -2 V test. However, ΔR_{on} decreased at first and then increased after 100 sec in the stressing stage, while ΔR_{on} increased originally and then experienced a drop after 500 sec at all the other V_{gs} tests.

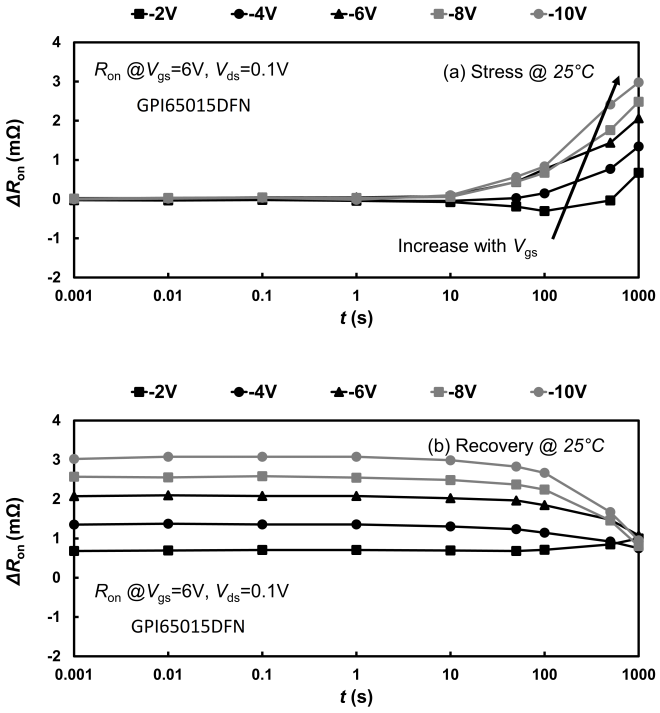

Fig. 5. Shift of ΔR_{on} of GPI65015DFN device in negative gate bias test at different V_{gs}: (a) Stress phase, (b) Recovery phase.

The shift in ΔR_{on} was related to the variation in ΔV_{th}. For both tested GaN HEMT devices, the injection of electrons into the p-GaN layer and the emission of the holes from the p-GaN stack can lead to the depletion in the positive charges under negative gate bias stress. With the decrease in negative V_{gs}, the p-GaN stack became less positive, further inducing the increase in ΔR_{on} during stressing period. However, the recovery of R_{on} of GPI65015DFN and GS-065-018-2-L devices behaved differently. ΔR_{on} of the GPI65015DFN HEMT decreased with time under most test conditions, while ΔR_{on} of the GS-065-018-2-L HEMT increased and then decreased. For the device from GPI65015DFN, the removed holes drifted back and R_{on} gradually recovered. Because the time constant of holes is larger compared with electrons, the p-GaN stack slowly reestablished and the evident recovery of R_{on} was not observed until 50 sec. For the GS-065-018-2-L device, the positive drift of ΔR_{on} was more affected by the measuring V_{gs}. The fast spill over of the electrons from the 2DEG channel during the characterization reduced the holes in the p-GaN stack, leading to a positive shift in the I-V curve, thereby increasing the R_{on}. After abundant recovery time, the restore of holes became dominant. Hence, ΔR_{on} started to recover again. It is worth mentioning that at the negative V_{gs} test of -2 V, the reduction in holes in the p-GaN stack was minor for both devices. The measuring V_{gs} of 6 V had an strong impact on the performance instability of Schottky p-GaN gate HEMT devices.

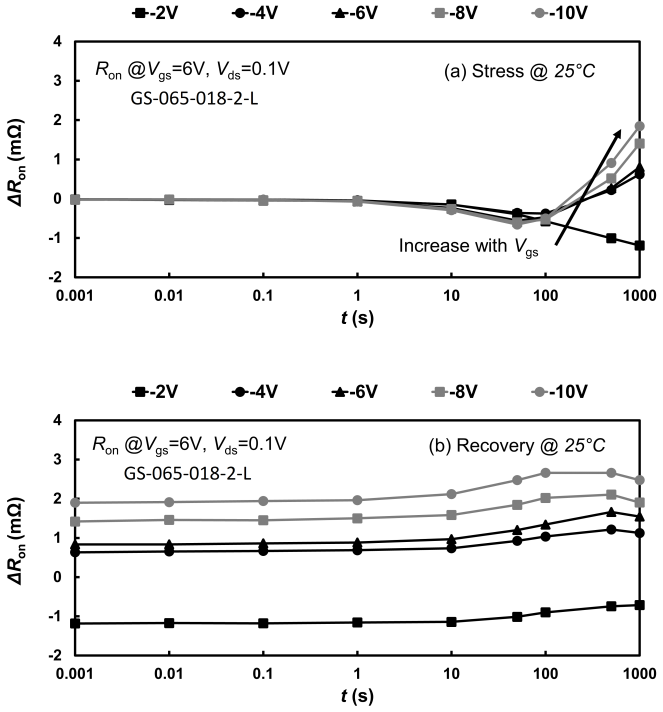

Fig. 6. Shift of ΔR_{on} of GS-065-018-2-L device in negative gate bias test at different V_{gs}: (a) Stress phase, (b) Recovery phase.

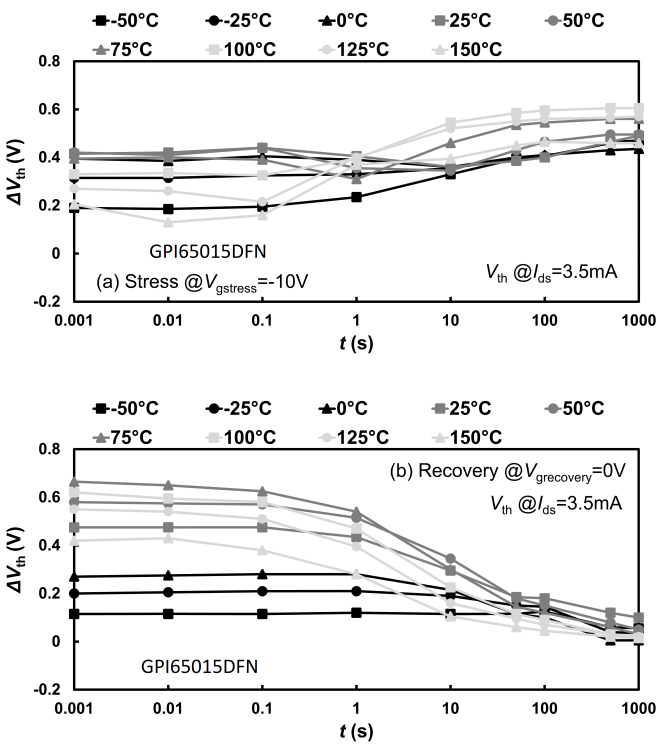

Fig. 7. Shift of ΔV_{th} of GPI65015DFN device under negative gate bias test at different temperatures: (a) Stress phase, (b) Recovery phase.

B. NBTI Gate Bias Stress Under Different Temperatures

The shifts in ΔV_{th} of GPI65015DFN and GS-065-018-2-L devices under V_{gs} stressing test of -10 V at different temperatures are shown in Fig. 7 and Fig. 8, respectively. Several interesting phenomenon can be found. Firstly, for the GPI65015DFN device, ΔV_{th} increased with the progress of the stressing test at -50°C and -25°C. When the ambient temperature rose above 0°C, ΔV_{th} decreased at first and then increased. The turning point moved leftwards as the temperature was elevated, as can be found in Fig. 7. Secondly, the initial V_{th} increment increased with temperature from -50°C to 75°C, but the increment dropped instead when the temperature was further increased. Thirdly, the shift of ΔV_{th} of GS-065-018-2-L device under different temperatures behaved in a different way. At -50°C and -25°C, the overall increasing trend in ΔV_{th} was slowed, and the obvious ΔV_{th} change happened after 100 sec. At 0°C, ΔV_{th} kept declining after the initial jump. Although the drop-and-increase trend was also found at elevated temperatures, the reduction in ΔV_{th} became much more significant compared with the GPI65015DFN device. Finally, the recovery of ΔV_{th} was accelerated with the increase of temperature for both devices.

For the negative gate bias stress test at -10 V, the testing temperature had a significant impact on the device performance. Since the initial ΔV_{th} jump increased with temperature under specific conditions, it can be inferred that the tunneling of electrons was greatly restrained at low temperatures below 0°C. With the increase in temperature, the

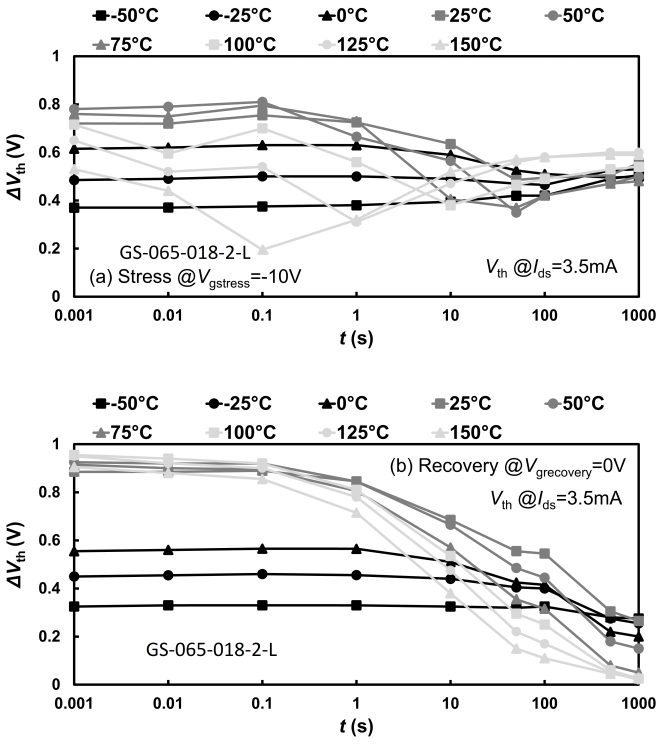

Fig. 8. Shift of ΔV_{th} of GS-065-018-2-L device under negative gate bias test at different temperatures: (a) Stress phase, (b) Recovery phase.

trapping of electrons became easier due to enhanced energy. In the meantime, the holes injected into the *p*-GaN stack by the positive measuring gate bias also became stronger [19]. Hence, a ΔV_{th} drop happened faster in Fig. 7 and Fig. 8. Due to different gate structure technology, the magnitude of the drop for two devices was different. The recovery of V_{th} was also accelerated because of faster de-trapping speed.

The changes in ΔR_{on} of GPI65015DFN and GS-065-018-2-L devices under negative gate bias tests at different temperatures are shown in Fig. 9 and Fig. 10, respectively. For both GaN HEMT devices, ΔR_{on} had minor variations at low temperatures below 0°C. With the increase in temperature, the drift in ΔR_{on} became more substantial and faster during the stressing phase. At the end of the test, ΔR_{on} increased by 23.99 mΩ for the GPI65015DFN device and 32.65 mΩ for the GS-065-018-2-L device. In the recovery phase, ΔR_{on} slowly recovered to the initial state and the recovery was expedited with the increasing temperature.

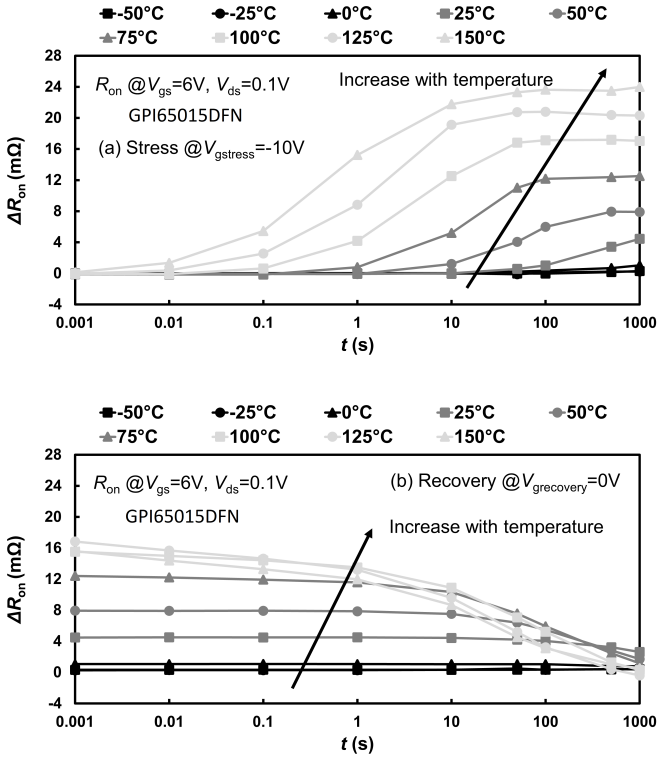

Fig. 9. Shift of ΔR_{on} of GPI65015DFN device under negative gate bias test at different temperatures: (a) Stress phase, (b) Recovery phase.

The reduction in positive charges led to the positive shift of I-V curves. Correspondingly, R_{on} increased with time. With the rise in ambient temperature, the deficiency of holes became more significant and the drift in ΔR_{on} occurred faster. Apart from the tunneling of electrons from the gate metal and the emission of holes from the *p*-GaN layer, it is deduced that the increased temperature has energized the electrons in the 2DEG. The electrons with high energy can inject into the *p*-GaN layer and contributed to the increase in ΔR_{on} as well.

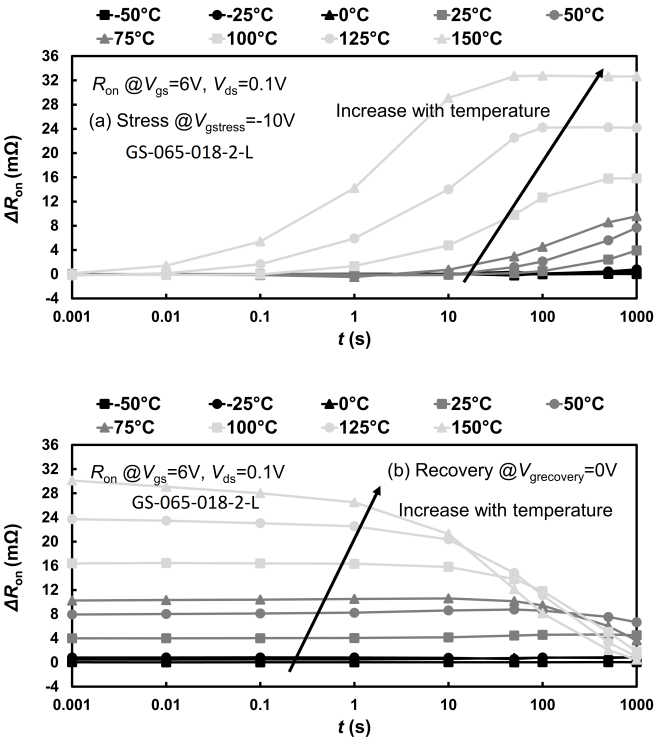

Fig. 10. Shift of ΔR_{on} of GS-065-018-2-L device under negative gate bias test at different temperatures: (a) Stress phase, (b) Recovery phase.

IV. Conclusion

In this paper, the static performance instabilities of 650 V Schottky *p*-GaN gate HEMT devices were characterized under various negative gate bias stresses. Based on the test results, the drifts in ΔV_{th} and ΔR_{on} were dependent on the V_{gs} magnitude, temperature, and device technology. It was discovered that as long as the measuring V_{gs} was applied, there was a positive ΔV_{th}. With the decrease in negative V_{gs}, the decrease in ΔV_{th} gradually turned into increase during the stressing stage, and the increment in ΔR_{on} was larger. The positive shifts in ΔV_{th} and ΔR_{on} were attributed to the holes deficiency in the *p*-GaN stack, and the measuring V_{gs} played an important role when the negative gate bias was low. Besides, ΔV_{th} increased at temperature below 0°C in the stressing period. With the increase in temperature, the overall trend of ΔV_{th} decreased and then increased. The initial ΔV_{th} jump increased with temperature below 75°C, but it reduced once the temperature reached above 75°C. The ΔR_{on} drifted significantly with the increase in ambient temperature at -10 V, which is disadvantageous to the device application.

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