

# Language Modeling on a SpiNNaker2 Neuromorphic Chip

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**Abstract**—As large language models continue to scale in size rapidly, so too does the computational power required to run them. Event-based networks on neuromorphic devices offer a potential way to reduce energy consumption for inference significantly. However, to date, most event-based networks that can run on neuromorphic hardware, including spiking neural networks (SNNs), have not achieved task performance even on par with LSTM models for language modeling. As a result, language modeling on neuromorphic devices has seemed a distant prospect. In this work, we demonstrate the first-ever implementation of a language model on a neuromorphic device – specifically the SpiNNaker2 chip – based on a recently published event-based architecture called the EGRU. SpiNNaker2 is a many-core neuromorphic chip designed for large-scale asynchronous processing, and the EGRU is architected to leverage such hardware efficiently while maintaining competitive task performance. This implementation marks the first time a neuromorphic language model matches LSTMs, setting the stage for taking task performance to the level of large language models. We also demonstrate results on a gesture recognition task based on inputs from a DVS camera. Overall, our results showcase the feasibility of this neuro-inspired neural network in hardware, highlighting significant gains versus conventional hardware in energy efficiency for the common use case of single batch inference.

**Index Terms**—Neuromorphic, Language model, Energy efficient, Sparse activity, Sparse weights

## I. INTRODUCTION

Most deep learning systems, from edge to cloud, rely on highly regular SIMD processing. The tremendous success of this processing paradigm has encouraged further convergence of hardware accelerators and algorithms to high throughput SIMD systems [1]. At the same time, deep learning algorithms exhibit a surprisingly high degree of inherent sparsity, which SIMD accelerators are unable to exploit. Experimental and theoretical studies have shown that a large fraction of connections can be removed entirely without sacrificing learning accuracy [2], [3]. Furthermore, deep learning models can operate on highly sparse representations without sacrificing precision [4]–[7]. These findings challenge the design principles of today’s SIMD-based deep learning systems from an energy efficiency perspective. Communication is the central energy and latency cost factor in contemporary computer architectures [8]. Dense

matrix operations are omnipresent in deep learning and require  $\mathcal{O}(n^2)$  messages for  $n$ -dimensional representations. This unfavorable behavior is under growing pressure as the annual growth rate of density of computational operations in hardware is about twice as fast as the growth rate of memory and interconnect bandwidth.

In this work, we present an implementation of a sparsely connected and sparsely activated architecture implemented on an processor that can take advantage of this unstructured sparsity for energy efficiency. More specifically, we present an implementation of a sparse network based on the EGRU [6] architecture on a SpiNNaker2 chip. The EGRU [6] is a recently proposed event-based network that naturally exhibits high levels of activity sparsity and was shown to have high levels of task performance on language modeling and gesture recognition tasks among others. To make full use of its potential, we implement it on the SpiNNaker2 chip, which is a digital neuromorphic system optimized for sparse communication and event-based processing [9]. Our implementation operates on unstructured sparsely connected units that communicate sparse in time. Both operations can be accelerated on SpiNNaker2, but not on conventional SIMD architectures. We choose language modeling as our demonstrator. Since the EGRU is a recurrent network, it is able to exploit the temporal inductive bias of sequence modeling tasks such as language modeling for computationally efficient processing. While transformers [10] are the dominant architecture for language modeling, they are computationally very expensive, which makes it even more urgent to find an energy efficient alternative. This first demonstration of the energy gains achievable using a recurrent architecture on neuromorphic hardware will set the stage for neuromorphic language modeling using even more powerful recurrent architectures [11], [12].

## II. RELATED WORK

Recent advances in machine learning have led to increased interest in energy-efficient hardware accelerators. Hardware-software co-design for machine learning accelerators have been used to target scaling to extremely large models [13], [14]. More recently, there has been an increased focus on mak-

ing transformer-based neural networks more efficient using accelerators for conventional hardware (see [15] for a review). A 4-bit quantized accelerator in 5 nm presented recently [16] demonstrated high energy efficiency and throughput. Spiking variants of popular transformer architectures have also recently been introduced [17]–[19], but no advantage on custom hardware has been reported yet. Neuromorphic LSTM accelerators have been developed using FPGAs [20], systolic arrays [21], and memristors [22]. A hybrid LSTM/spiking neuron architecture was implemented on Intel’s Loihi chip, demonstrating energy gains [23]. None of these LSTM-based approaches have been scaled to standard NLP benchmark tasks yet. Spiking LSTM [24] and EGRU [6] are two attempts at bringing event-based properties to the respective base architectures and allow for full precision gates and graded spike communication between units. Other related approaches include Sigma-delta quantised networks that communicate only quantised changes in activations to the next layer in a feed-forward network [25] and its extension to recurrent networks [4]. An FPGA accelerator for sparsely connected and sparsely communicating Delta Networks greatly reducing required memory access, was presented in [26].

### III. BACKGROUND

#### A. The SpiNNaker2 System

SpiNNaker2 is an accelerator for large-scale event-based and asynchronous processing [9]. The chip consists of 152 processing elements (PEs) connected via a network-on-chip (NoC). Each processing element is composed of an Arm M4f core, 128 kB SRAM, and a set of accelerators for exponential functions, random number generation and multiply-accumulate (MAC) operations. The total of 19 MB on-chip SRAM is accompanied by 2 GB LPDDR4 memory. Communication between the PEs in a single chip can be implemented by direct memory access (DMA) to other PEs’ local memory. The local SRAM is organized into 4 memory banks of 32 kB each. One is usually reserved for program memory, and three banks for values such as RNN weights and intermediate variables. See Table I for details of memory footprint of EGRU Language model.

#### B. Event-based Gated Recurrent Unit

The Gated Recurrent Unit (GRU) is an effective recurrent neural network that has been widely adopted for sequence modeling [27]. To reduce the communication between logical neurons, [6] apply a biologically inspired thresholding mechanism to the GRU. In this model, called Event-based Gated Recurrent Unit (EGRU), a layer consists of  $n$  neurons with output  $\mathbf{y}$  and state  $\mathbf{c}$ . A sparse output  $\mathbf{y} = (y_1, \dots, y_n)$  is generated from the GRU cell state  $\mathbf{c} = (c_1, \dots, c_n)$  via the following mechanism

$$y_i^{(t)} = c_i^{(t)} H\left(c_i^{(t)} - \vartheta_i\right), \quad H(x) = \begin{cases} 1, & x \geq 0 \\ 0, & x < 0 \end{cases} \quad (1)$$

Only the sparse output  $\mathbf{y}$  is communicated between neurons to compute the update gate  $\mathbf{u}$  and the reset gate  $\mathbf{r}$  of the GRU

$$\mathbf{u}^{(t)} = \sigma\left(\mathbf{W}_u \left[\mathbf{x}^{(t)}, \mathbf{y}^{(t-1)}\right] + \mathbf{b}_u\right) \quad (2)$$

$$\mathbf{r}^{(t)} = \sigma\left(\mathbf{W}_r \left[\mathbf{x}^{(t)}, \mathbf{y}^{(t-1)}\right] + \mathbf{b}_r\right). \quad (3)$$

As outlined in [28], the sparse state  $\mathbf{y}$  and the gates  $\mathbf{u}$  and  $\mathbf{r}$  compute a proposed state  $\mathbf{z}$  and the new cell state  $\mathbf{c}$

$$\mathbf{z}^{(t)} = g\left(\mathbf{W}_z \left[\mathbf{x}^{(t)}, \mathbf{r}^{(t)} \odot \mathbf{y}^{(t-1)}\right] + \mathbf{b}_z\right) \quad (4)$$

$$\mathbf{c}^{(t)} = \mathbf{u}^{(t)} \odot \mathbf{z}^{(t)} + (1 - \mathbf{u}^{(t)}) \odot \mathbf{c}^{(t-1)} - \mathbf{s}^{(t)}. \quad (5)$$

Similar to biologically plausible spiking neural networks, [6] subtract already communicated signals  $\mathbf{y}$  from the cell state via the reset term  $\mathbf{s}^{(t)} = \vartheta H(\mathbf{c}^{(t)} - \vartheta)$ . During training, the surrogate function  $\frac{dH}{dc} = \lambda \max(1 - |c|/\epsilon)$  provides gradients below the threshold.

#### C. Language Modeling with EGRU

Word-level language modeling is a popular benchmark task to measure the performance of sequence models, including RNNs. A language model processes a sequence of words  $w_1, \dots, w_t \in \mathcal{D}$  from a dictionary  $\mathcal{D}$ , and predicts the conditional distribution  $p(w_{t+1} | w_1, \dots, w_t)$ . Its training objective is minimizing the cross entropy  $H(p, q)$  between this prediction  $p$  and a one-hot encoding  $q$  of the actual next word in the sequence. The standard metric for measuring performance is perplexity (PPL), the exponential cross entropy  $e^{H(p, q)}$ . Artificial texts can be generated by a trained language model by iterative sampling from the next-word distribution  $p$  predicted by the model.

We trained three EGRU layers without skip connections to processes word embedding vectors drawn from a learned look-up table similar to [29]. The model estimates the likelihood of the next word in a sequence by computing the dot-product similarity between the output vector of the final EGRU layer and all word embedding vectors of the dictionary. Softmax applied to this set of values serves as an estimate of the conditional distribution  $p$ . The dimension of word embedding vectors and the final layer cell state was 750. The dimension of intermediate layers’ cell state was 1350. We used a model from Mukherji et al. [28] trained on the WikiText-2 dataset [30] with a parameter sparsity of 95 % per weight matrix. The model weights were stored on SRAM in a Sparse CSR format. The three EGRU layers were implemented on 150 PEs.

#### D. DVS gesture recognition

We also evaluated our model on gesture prediction, using the DVS128 Gesture Dataset [31]. This dataset contains 11 gestures from 29 subjects recorded with a DVS128 event camera [32]. Each event encodes a relative change of illumination and is given as spatio-temporal coordinates of X/Y position on the 128×128-pixel sensor and time stamp.

Our model consisted of a CNN feature extraction head and 2 EGRU layers of 256 units each. The dimension of features extracted from the CNN was 512. Finally a linear layer was

used to predict the class of the gesture. For this task we used only dense weights and stored them directly on SRAM since the model is small enough to fit in local memory. The two EGRU layers were implemented on 128 PEs.

#### IV. SPINNAKER2 IMPLEMENTATION

##### A. Implementation of EGRU on a single processing element

We were able to fit the simplest EGRU model on a single PE of SpiNNaker2. There are three operations that need to be performed as part of EGRU algorithm: 1) input matrix multiplication 2) recurrent matrix multiplication and 3) point-wise operations. For a single PE implementation, we can simply execute these operations sequentially. There is no data transfer needed as all the results are available in local memory. Although there is a Multiply-accumulate (MAC) accelerator on SpiNNaker2, we do not use it in this application to take full advantage of EGRU’s dynamic sparsity.

##### B. Parallelization approaches

Since any realistic model, including our larger EGRU models, will not be small enough to fit onto a single PE, we need to split the network over multiple PEs. To do this, we split the network and place the neurons on different PEs. This approach reduces the communication and synchronization required within the network. The output generated by the units placed on a single PE determined the output of that PE. This output  $y^{(t)}$ , at time  $t$ , needed to be broadcast to the rest of the units in the EGRU layer. On receiving such a broadcast each PE concatenated the outputs from all other PEs together with the output of the units stored locally to form the next recurrent input. This broadcast was implemented by sending internal NoC packets between PEs. This operation is demonstrated in Fig. 1 and the algorithm is presented in Algorithm. 1

With this parallelization, we only split one dimension of the  $R$  weight matrix. Since the second dimension was as large as the number of units in a layer, the recurrent weight matrix was still too large to fit in individual PE memory. To mitigate this, we used a 95% pruned EGRU model for language modeling. The pruned weights were stored in compressed sparse row (CSR) format. In this format the non-zero (NZ) elements of the matrix were represented using three one-dimensional arrays. These contained NZ values, column indices of the NZ elements and the extents of rows, which required  $2 * NZ + N\_rows + 1$  memory.

##### C. Dataset and pre-processing

1) *Language Modeling*: The model was trained and validated on WikiText-2 dataset. The text was tokenised and split into sequence of length 70. The embeddings were pre-computed and transferred to the LPDDR4 memory.

2) *DVS*: We combined the DVS raw event times into ‘frames’ by binning them over time windows of 25 ms, and then downscaled them to  $32 \times 32$  pixels using a maxpool layer. The dataset was pre-processed and the features extracted using the CNN head. The extracted features were stored in the LPDDR4 memory.

#### Algorithm 1 EGRU algorithm for multi PE implementation

##### procedure EGRU

###### Input:

- Network Configuration Parameters
- Input Data
- Output Data Destination

###### Output: Processed output data

###### Initialization:

- Initialize temporary variables.

###### while run is true do

- Check for input data availability.
- Process input data and prepare it for computation.

###### for each time step $t$ do

- $Wx \leftarrow$  Matrix Multiplication:  $W_x \times x_t$ .
- $Rh \leftarrow$  Matrix Multiplication:  $W_r \times y_{t-1}$ .
- Point-wise operation on  $Wx$  and  $Rh$ .
- Store output data.

- Wait for host to read output data.

###### if run is false then

- Stop.

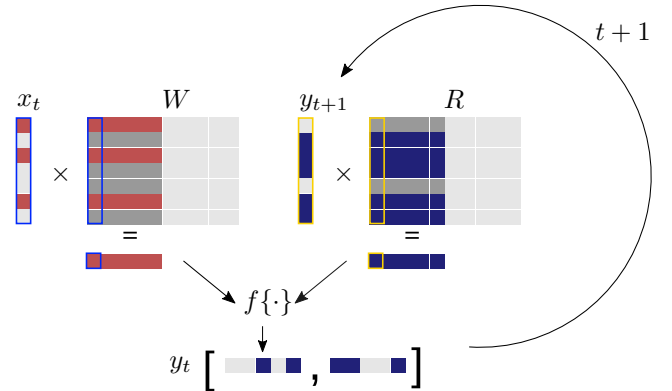


Fig. 1. EGRU operations and distribution strategy: This figure shows computation performed on a single PE as part of a multi-core implementation, the grayed out portions are computed on other PEs,  $W$  and  $R$  are kernels processing current input  $x_t$  and previous output  $y_{t-1}$  respectively.  $f\{\cdot\}$  represents point-wise operations.

#### V. RESULTS

We measured the time required by the EGRU operations using an internal timer. This timer ticks at 1 MHz rate and decrements a counter. We logged the timer value at various points in the algorithm to estimate the time spent by the algorithm at each stage. The results of this profiling are shown in Fig. 2. As can be seen, the most expensive part was the recurrent matrix multiplication (*egru\_internal*). Broadcasting of layer activations was a comparably cheap operation, since the broadcast uses efficient NoC packets to communicate. The bottleneck of the algorithm was therefore found to be dominated by memory reading and writing rather than communication, for the single chip case. However, this might not be the case for multi-chip communication.

TABLE I

MEMORY FOOTPRINT OF 95% PRUNED EGRU MODEL. WEIGHT MATRICES STORED IN SPARSE CSR FORMAT. TOTAL AVAILABLE INSTRUCTION MEMORY IS 32 KB AND THE AVAILABLE DATA MEMORY IS 96 KB.

	Instruction	Debug	Weights	Variables
Memory (KB)	17.9	5	88.3	2.6

TABLE II

EGRU LM ON SPiNNAKER2 COMPARISON WITH GPU

Measurement	Nvidia A100	SpiNNaker2
Batch size	1	1
Power (W)	60	0.39
Time (mS)	19.9	170.25
Energy (J)	1.1935	0.0653
Test PPL	79.3	79.3

### A. Power and energy consumption

The power consumption of the EGRU language model is shown in Table. II. We show that for inference, our implementation on SpiNNaker2 consumes only a fraction of a Watt. Whereas the time required on SpiNNaker2 scales linearly with batch size, the GPU can process larger batch sizes in the same time. Hence at larger batch sizes GPU tend to be more efficient. This is only shown for the DVS task because the LM task has a memory bottleneck that only allows a batch size of one on a single chip. See Table. III for this energy comparison. The test accuracy on the classification task was identical on both GPU and SpiNNaker2 implementation, demonstrating numerical equivalence, since we perform 32-bit floating point operations on both architectures.

## VI. OUTLOOK

The successful implementation of a language model on the SpiNNaker2 chip using the EGRU event-based architecture represents a significant milestone in the field of neuromorphic computing. We compare our implementation with the one on the Nvidia GPU and show a real energy advantage in the single batch size setting, which we expect to be the most relevant for inference, especially on edge devices. We also identified several bottlenecks in our implementation that need improvement for even further efficiency. In particular, quantizing the model will allow us to work with even tighter memory constraints

TABLE III

EGRU DVS GESTURE PREDICTION ON SPiNNAKER2 COMPARISON WITH GPU. TIME AND ENERGY MEASUREMENTS NORMALIZED OVER BATCH SIZE.

Measurement	Nvidia A100		SpiNNaker2	
Batch size	1	6	1	6
Power (W)	61.0	61.0	0.39	0.42
Time (mS)	1.09	0.19	60.19	56.20
Energy (J)	0.067	0.011	0.023	0.023
Accuracy (%)	96.83	96.83	96.83	96.83

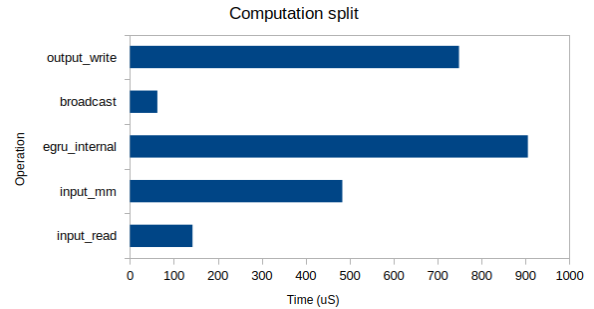


Fig. 2. Profiling of internal EGRU operation for Language modeling. EGRU model has 1350 units, 3 layers and 95% pruned. Weights stored in sparse CSR format.

to fit larger models and further increase energy efficiency, albeit with a slight reduction in task performance. Quantization will also allow us to take advantage of the MAC accelerator available on the SpiNNaker2 chip. We also plan to further scale the deployed model to multiple chips, as SpiNNaker2 is designed for efficient distributed computing.

Scaling up neuromorphic language models to more contemporary large sizes by harnessing very recent innovations in recurrent architectures [33], [34] is the self-evident next step. However, bringing the performance on par with standard deep learning also suggests expanding the range of real-world applications for neuromorphic hardware in future work, including real-time applications, which they are well suited for. Overall, our implementation has demonstrated, for the first time, that challenging machine learning tasks are not beyond the scope of neuromorphic computing and heralds the beginning of more mainstream use of neuromorphic devices as complementary to GPUs for appropriate use cases.

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