Virtual Inertia for Suppressing Voltage Oscillations and Stability Mechanisms in DC Microgrids

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Abstract

Renewable energy sources (RES) are gradually penetrating power systems through power electronic converters (PECs), which greatly change the structure and operation characteristics of traditional power systems. The maturation of PECs has also laid a technical foundation for the development of DC microgrids (DC-MGs). The advantages of DC-MGs over AC systems make them an important access target for RES. Due to the multi-timescale characteristics and fast response of power electronics, the dynamic coupling of PEC control systems and the transient interaction between the PEC and the passive network are inevitable, which threatens the stable operation of DC-MGs. Therefore, this dissertation focuses on the study of stabilization control methods, the low-frequency oscillation (LFO) mechanism analysis of DC-MGs and the state-of-charge (SoC) imbalance problem of multi-parallel energy storage systems (ESS).

Firstly, a virtual inertia and damping control (VIDC) strategy is proposed to enable bidirectional DC converters (BiCs) to damp voltage oscillations by using the energy stored in ESS to emulate inertia without modifications to system hardware. Both the inertia part and the damping part are modeled in the VIDC controller by analogy with DC machines. Simulation results verify that the proposed VIDC can improve the dynamic characteristics and stability in islanded DC-MG. Then, inertia droop control (IDC) strategies are proposed for BiC of ESS based on the comparison between conventional droop control and VIDC. A feedback analytical method is presented to comprehend stability mechanisms from multi-viewpoints and observe the interaction between variables intuitively. A hardware in the loop (HIL) experiment verifies that IDC can simplify the control structure of VIDC in the promise of ensuring similar control performances. Subsequently, a multi-timescale impedance model is established to clarify the control principle of VIDC and the LFO mechanisms of VIDC-controlled DC-MG. Control loops of different timescales are visualized as independent loop virtual impedances (LVIs) to form an impedance circuit. The instability factors are revealed and a dynamic stability enhancement method is proposed to compensate for the negative damping caused by VIDC and CPL. Experimental results have validated the LFO mechanism analysis and stability enhancement method. Finally, an inertia-emulation-based cooperative control strategy for multi-parallel ESS is proposed to address the SoC imbalance and voltage deviation problem in steady-state operation and the voltage stability problem. The contradiction between SoC balancing speed and maintaining system stability is solved by a redefined SoC-based droop resistance function. HIL experiments prove that the proposed control performs better dynamics and static characteristics without modifying the hardware and can balance the SoC in both charge and discharge modes.

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Nomenclature and Abbreviations

Abbreviations

bi-DC	Bidirectional DC
BiC	Bidirectional DC converter
CCL	Constant current load
CCS	Current coordinate system
CPL	Constant power load
DC-BVF	DC bus voltage fluctuation
DC-MG	Direct current microgrid
DFIG	Doubly fed induction generator
DG	Distributed generations
DLC	Dual loop control
DVI	Dynamic virtual impedance
ESS	Energy storage system
ESU	Energy storage unit
EU	European Union
EV	Electric vehicle
HESS	Hybrid energy storage system
HIL	Hardware in the loop
H-MG	Hybrid AC/DC microgrid
HVDC	High voltage direct current
HPF	High pass filter
IDC	Inertia droop control
IDA-PBC	Interconnection and damping assignment-passivity-based control
IEL	Inertia emulation loop
IM	Impedance model
LFO	Low-frequency oscillation
LPF	Low pass filter
LVI	Loop virtual impedance
MIMO	Multi-input multi-output
MMC	Modular multilevel converter
MSD	Mass-spring-damper
MTDC	Multi-terminal DC

ND	Negative damping
NF	Negative feedback
PBC	Passivity-based control
PBSC	Passivity-based stability criterion
PCH	Port-controlled Hamiltonian
PD	Positive damping
PDRL	Positive-damping reshaping loop
PEC	Power electronic converter
PFB	Positive feedback
PV	Photovoltaics
RES	Renewable energy source
RHP	Right half plane
RoCoV	Rate of change of voltage
SC	Super-capacitor
SG	Synchronous generator
SISO	Single-input single-output
SM	Switch model
SMES	Superconducting magnetic energy storage
SoC	State-of-charge
SSO	Sub-synchronous oscillation
SST	Solid-state transformer
SVR	Secondary voltage regulation
TVN	Transient voltage nadir
VCS	Voltage coordinate system
VDCM	Virtual DC machine
VIC	Virtual inertia control
VIDC	Virtual inertia and damping control
VSC	Voltage source converter
VSG	Virtual synchronous generator
VSM	Virtual synchronous machine

Parameters and Variables

C_{bus}	DC bus capacitance
C_f	Output capacitance of buck converter

C_{in}	Input capacitance of buck converter
C_{out}	Output filter capacitor of bidirectional DC converter
d	Duty ratio
i_m/i_s	Input current of bidirectional DC converter
i_{out}/v_{out}	Output current and voltage of bidirectional DC converter
$J_{vir}/k_{vd}/k_{svr}$	Virtual inertia, damping and stiffness coefficient of VIDC
k_{ip}/k_{ii}	Proportional and integral gain of current-loop controller
k_{vp}/k_{vi}	Proportional and integral gain of voltage-loop controller
L_f/R_f	Filter inductor and its parasitic resistance of buck converter
L_s/R_s	Input filter inductor and its parasitic resistance of bidirectional DC converter
P_{const}/P_{cpl}	Power of CPL
R_{cpl}	Small-signal impedance of CPL
R_d	Droop coefficient
R_{line}/L_{line}	Line impedance
v_{bus}	Rated value of DC bus voltage
v_{out_buck}	Load voltage of buck converter
v_s/v_{in}	Input voltage of bidirectional DC converter

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1 Introduction

1.1 Background and Motivation

As an important measure to deal with the energy crisis and climate change, carbon neutrality has become the focus of current and future global energy policies to promote the development of renewable energy sources (RES). A number of legislations and proposals have been passed to ensure that the European Union (EU) meets its climate and energy targets, including the Emissions Trading System, the Effort Sharing Regulation, and the transport and land use legislation [1]. New ambitious targets for RES and energy efficiency have been set: the intermediate target of a net reduction in greenhouse gas emissions is raised from 40% to at least 55% by 2030, as well as at least 32% share for renewable energy and at least 32.5% improvement in energy efficiency [1-2]. By 2050, the EU aims to achieve climate neutrality and strive to become the first climate-neutral continent [3]. As the world's largest emitter of carbon dioxide, China promised to peak CO_2 emissions before 2030 and achieve carbon neutrality before 2060, which will require significant changes to transform China's energy system [4-5].

Obviously, the fossil fuels dominated energy structure has difficulties in meeting the requirements of sustainable development. It is urgent to improve the energy consumption mode and reduce the dependence on fossil energy. Therefore, the development and utilization of RES, such as wind and solar energy, have gradually gained attention and shown a strong growth trend. On average, RES accounted for 19.7% of gross final energy consumption in the EU in 2019, up from 13.9% in 2009. Sweden ranked first in the EU, with RES accounting for 56.4% of its gross final energy consumption in 2019, and Germany ranked 16 across the EU with 17.4% while the EU average was 19.7%. Newly installed RES capacity in Asia accounted for 54% of the global total installed capacity in 2019. Among them, solar and wind energy accounted for 90% of the newly installed RES in 2019 [6]. The vigorous development and increasing penetration of RES force the global energy market and power system to undergo an unprecedented revolution.

Influenced by geographical differences, climate changes, and other factors, RES presents the characteristics of volatility, intermittency and randomness which threaten the secure and stable operation of power system and severely restrict the development of RES and related technologies. On the other hand, the wide and diverse access of DC sources and DC loads has become

a trend in electric energy applications. Driven by power electronics technology, the DC microgrid (DC-MG) thus emerges as an effective form for the local consumption of RES. Compared with the AC system, DC-MG has promising advantages of its high power-conversion efficiency, natural interface with RES, electronic loads and energy storage systems (EES), and no concern for power angle stability [7].

Considering the advantages of DC-MG, its usage covers various residential and industrial applications, such as rail transportations, aircrafts, and ship power systems, data centers, fast electric vehicle (EV) charging stations, high-efficiency households and renewable energy parks [8]. Nowadays, the electric traction DC power supply technology has matured. In terms of residential DC power supply, the EU, Japan and the United States have carried out relevant research and demonstration projects, which have laid a good theoretical and practical foundation for the promotion of DC-MG [8, 18, 34-35]. At present, there is no clear standard voltage class for the DC bus voltage. Usually, DC power supplies and DC loads convert and adjust their voltages according to their own requirements and industry standards. For instance, integrated circuits or chips usually operate at 5V and 12V, electronic devices such as computers and tablets operate at 12V, the DC voltages of EV batteries and on-board supplies are 12V, 24V, or 48V, the power supply system of telecom operates at 48V, the DC voltages of data centers and high-power appliances are 280V-400V, and charging piles operate at 250V-700V.

As an emerging technology, standardization is another obstacle to the proliferation of DC-MG in industrial and commercial applications. Several organizations and institutions have therefore developed practical standards. The European standard ETSI EN 300 132-3-1 is mainly designed for low-voltage DC (LVDC) systems, such as data/telecom equipments with voltage levels of up to 400V [9]. As an open industry association, the EMerge Alliance deploys advanced architectures and control systems based on DC-MGs in occupied spaces, data/telecom centers, building exteriors, and building services [10]. IEC SG4 delivers standards for LVDC distribution systems of up to 1500V [11] and coordinates the standardization of different utilizations of LVDC distribution systems. IEEE DC@Home concerns with developing the standards and defining the roadmap for research and commercialization of DC-MGs [12]. In addition, IEEE 946, Rebus and MIL-STD-1399 are proposed for standardizing the operation of DC-MG [8]. IEEE 946 is designed for the DC auxiliary power system, Rebus normalized the operation of DC-MG in residential and commercial applications, and MIL-STD-1399 provided the military standard for shipboard power systems.

Power electronic converters (PECs) are the key to integrating RES units, ESS, and various DC

loads into DC-MG, replacing traditional synchronous generators (SGs) that provide rotational inertia. In conventional power systems, SGs autonomously slow down or speed up in accordance with the grid frequency. In this way, SGs release/absorb the energy to/from the power grid so that the power mismatch can be partially compensated. This effect is quantitatively evaluated by the per unit kinetic energy, which is defined as the inertia of power systems [75]. As the penetration level of RES increases, more SGs are phased out and replaced by PEC, since RES is usually coupled to power systems through power electronic devices without rotational inertia. As a result, the entire power system becomes less inertial [81].

The PEC increases system bandwidth and its fast response capability brings flexibility to power systems. It also makes DC-MGs a typical power electronics dominated power system and exhibits low-inertia characteristics. In DC-MG, its inertia manifests the ability to prevent sudden changes in the DC bus voltage [73]. More specifically, due to the fast-response interface converters, the DC bus voltage may easily fluctuate beyond the acceptable range, resulting in undesirable load shedding and system collapses [54]. This means that DC-MG does not have sufficient inertia to stabilize the DC bus voltage. Therefore, it is necessary to develop measures to improve the dynamic behavior.

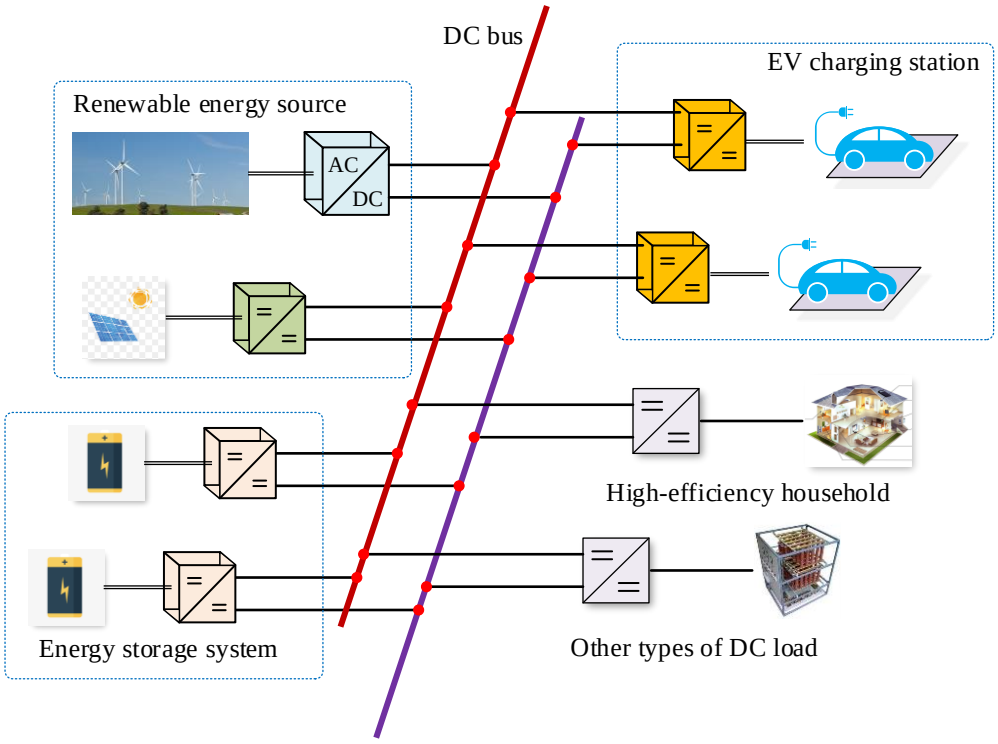


Figure 1.1: A typical layout of RES-integrated single-bus DC-MG.

Besides, most loads are connected to the DC bus via PECs, which makes the loads behave as constant power loads (CPLs). Further, the negative impedance characteristics of CPLs would

reduce the system damping, make DC-MG poor damping, and destabilize the DC-MG after being disturbed. In addition, RES would bring the problem of power quality degradation and difficult energy management. ESS, as a supporting source, can provide better conditions for integrating RES into DC-MG because ESS can balance the output power of RES and load demand to solve the voltage fluctuation/oscillation problem caused by power fluctuations of RES.

DC-MG would become the main access target of RES and an important component of the future smart grid. The typical structure of a single-bus RES-integrated DC-MG is shown in Figure 1.1. It mainly includes photovoltaic plants, wind farms, ESS, EV charging stations, high-efficiency buildings and other DC loads. The studies in Chapters 3-6 of this dissertation are mainly based on Figure 1.1 or its simplified version.

It can be seen from Figure 1.1 that most RES, ESS and loads have DC properties and can be connected to DC-MG directly or via interface converters. Thus DC-MG would become one of the main forms or an important element in the future power systems to cope with the large-scale RES integration into the grid. Therefore, ensuring the secure and stable operation of DC-MG is conducive to overcoming the bottleneck of connecting RES to the grid and solving the problem of efficient consumption of RES, which is of great theoretical and practical significance for the development of the future power system.

As the only indicator of the security and stable operation of the DC-MG, the instability of the DC-bus voltage would jeopardize the stable operation of the whole DC-MG. The main motivation of this research is to improve the stability of DC-MG and power quality for users by providing sufficient virtual inertia and damping. Increasing inertia can slow down the dynamic response of DC-MG and thus reduce RoCoV, while increasing damping can suppress the amplitude of voltage oscillations. Taking full advantage of ESS's ability to suppress DC bus voltage fluctuations provides a theoretical basis for accessing RES into DC-MG with high penetration. Further, it is of great significance to study the stabilization technology and low-frequency oscillation (LFO) mechanism of DC-MG to ensure its stable operation.

1.2 Research Questions and Corresponding Sulutions

This research focuses on how to improve voltage stability without additional hardware and intuitively reveal the LFO mechanism in islanded DC-MG. Especially, the following problems are worthy of more in-depth investigations:

(1) *Problem of how to enhance the inertia and damping of suppressing voltage oscillations*. An appropriate stabilization control method is a good solution to improve the dynamic

response of DC-MG. Without modifications to the system hardware, the inertia can be synthesized by the energy stored in ESS to mitigate voltage oscillations caused by power disturbances. By properly regulating ESS to release or absorb energy as the rotors of DC machines and capacitors do and connecting a virtual resistance in series with the output port, DC bus voltage oscillations can be alleviated. Compared with connecting capacitors which will bring additional power losses and are limited by certain application scenarios with limited space, such as ship electrical systems, stabilization control methods basically would not increase system costs, because the virtual inertia power and damping power are provided for ESS which is always required in islanded DC-MG for voltage stabilization. Moreover, control parameters should be carefully determined to ensure better control performance and excellent dynamic response.

(2) *Problem of how to simplify the structure and complexity of virtual inertia and damping control to reduce the difficulty of its realization.*

The existing virtual inertia and damping control (VIDC) strategy for DC-MG is derived from the external characteristic of a capacitor or the operation principle of a rotating machine. An additional loop is requested to imitate the inertial response, complicating the overall control system and its implementation. How to streamline the control structure of VIDC for easier utilization in engineering applications becomes an important issue. Besides, a unified analytical method and related analysis tool are necessary to illustrate the stability mechanism of various inertia controls and intuitively observe the interaction between feedback variables. Therefore, the physical significance and control function of the parameters can be explained from multiple perspectives.

(3) *Problem of establishing an impedance modelling framework for analyzing LFO mechanisms in an intuitive view.*

The stability mechanism of VIDC, the influence of CPL on VIDC, and the LFO mechanism of VIDC controlled DC-MG (VIDC-DC-MG) with a clear physical significance are less investigated. Besides, there is a lack of appropriate analysis tools to identify the potential instability factors of VIDC-DC-MG.

At present, three mainstream modelling approaches are used for the stability analysis of power electronics systems: the transfer-function-based method, the state-space-model-based method, and the impedance-model-based method. The transfer-function-based method focuses on the relationship between key variables and is therefore incomprehensive compared with the state-space model. The state-space model describes each variable of the system and thus can gain insight into the leading causes of underdamped

or unstable modes. However, the state-space model is a white-box model in nature and requires complete system information, and its abstract form makes it difficult to intuitively clarify the mapping between the oscillation modes and the corresponding factors. The all-in-one impedance model that can be directly measured and verified has less requirements for design details. Hence, it is more suitable for stability evaluation with clear physical meanings. However, the existing impedance model lacks systematic and intuitive insight into the internal roots of underdamped or instability factors, and is essentially a black-box model.

Therefore, an appropriate modeling framework as the bridge between white-box and black-box modeling by combining the advantages of the impedance model and the state-space model is necessary and worth investigating for the LFO mechanism analysis.

(4) *Problem of how to address the state-of-charge imbalance in multi-parallel ESS.*

Multi-parallel ESS is indispensable as the supporting energy source of DC-MG. The parameter mismatches of energy storage units (ESU), such as various series resistances, different self-discharge rates, and uneven operation temperatures across ESU, result in significant divergence of state of charge (SoC) among ESUs. Thus the unbalanced SoC leads to over-charge/-discharge and even explosion, degrades the utilization of some ESUs and decreases the operation lifespan of batteries. Therefore, how to achieve SoC balance under the premise of improved system dynamic stability becomes particularly important. Besides, the optimal design of key parameters should also be considered to address the contradiction between the speed of SoC balancing and system stability.

Aiming at the above problems (1)-(4), this dissertation proposes corresponding solutions, mainly including the following aspects:

(1) *Propose a VIDC to suppress voltage oscillations in islanded DC-MGs.* Without modifying system hardware and increasing system cost and complexity, the proposed VIDC can regulate ESS to release or absorb energy as rotors of DC machines and capacitors do. Thus, inertia can be synthesized by the energy stored in ESS to mitigate the voltage oscillations caused by power disturbances.

(2) *Develop inertia droop controls to simplify the complexity of VIDC*. In order to streamline the control structure of VIDC for easier implementation in engineering applications, inertia droop controls are designed based on the equivalent droop-control-form models of VIDC. Besides, a unified analytical method and related analysis tool should be provided to illustrate the stability mechanism of various inertia controls from multi-views.

(3) *Establish a modeling framework for the LFO mechanism analysis*. The proposed multi-timescale impedance modeling framework can be converted into a white-box or black-box model depending on the need for analysis. Control loops of different timescales are visualized as independent loop virtual impedances, and the impedance properties of control loops/parameters and their impedance-shaping effects can be illustrated at various timescales to explain the LFO in different bandwidths.

(4) *Achieve SoC self-balance of multi-parallel ESS by the inertia-emulation based cooperative control*. Under the premise of ensuring the increased inertia to improve the system stability, the SoC imbalance problem should be solved by the SoC self-balance algorithm and the SoC self-balance rate can be adjusted. Besides, the contradiction between the SoC balancing speed and maintaining system stability should be considered.

To sum up, the overall objective of this dissertation is to propose a stabilization control method for bidirectional DC converters to improve the voltage stability and quality of DC-MG, to establish a suitable modeling framework to explore the LFO mechanism, and to address the hazards of SoC divergence by the proposed inertia-emulation based cooperative control.

1.3 Outlines of the Dissertation

The structure of this dissertation is demonstrated in Figure 1.2 and organized as follows:

In Chapter 2, the state of art about investigations on DC-MG is summarized from four aspects. Firstly, the topologies of DC-MG and their applications are presented, and the main causes of DC voltage fluctuations and their manifestations are reviewed. Then, the basic principle of commonly used stabilization control methods is introduced. Subsequently, the mainstream modeling and stability analysis methods are reviewed. Moreover, the SoC balance methods for multi-parallel ESS are also introduced.

In Chapter 3 [M6], a VIDC strategy is proposed to enable bidirectional DC (bi-DC) converter to dampen voltage oscillations by using the energy stored in ESS to emulate the inertia of DC-MG without modifications of system hardware. Both the inertia part and the damping part are modeled in the VIDC controller, by analogy with DC machines. Droop control is introduced to achieve the multi-parallel operation of ESS. Furthermore, the small-signal model is established and the dynamic characteristics of DC bus voltage under power fluctuations are analyzed. A 2nd-order equivalent model is introduced to simplify the parameter design. By analyzing the control performance indices, the VIDC parameters are optimized. At last, based on the principle

of equivalent machine, an inertia matching method for multi-parallel bi-DC converters is proposed. The simulation results verify that ESS by acting as synthetic inertia can improve the voltage dynamic characteristics and stability in islanded DC-MGs. Compared with other control methods, it has better control effects.

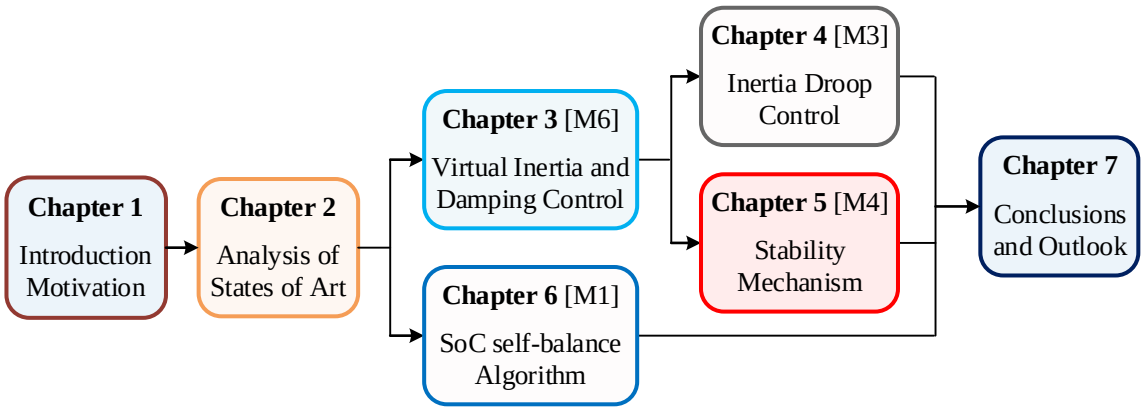


Figure 1.2: Structure of the dissertation.

In Chapter 4 [M3], inertia droop control (IDC) strategies are proposed for a bidirectional DC converter (BiC) to improve dynamic stability and provide high-quality power supply in islanded DC-MG. Compared with VIDC, the proposed IDC can be implemented by easily modifying conventional droop control, which avoids a complex control structure. First, the virtual inertia in the proposed IDC strategies can be achieved in two ways: 1) dynamic virtual impedance, and 2) adaptive droop algorithm. The damping support comes from the redesigned damping term which features secondary voltage regulation to eliminate the voltage deviation. Then, a feedback analytic method is proposed to comprehend the stability mechanism from multiple perspectives, and a double-coordinate-based phasor diagram is developed as its analytical tool to intuitively observe the interaction between variables. Accordingly, the IDC's negative feedback property is revealed, and the impactors of system inertia, stiffness and dissipation properties are explored. Dynamic performance and small-signal stability analysis are also presented to guide parameter selection and optimize transient response. Hardware in the loop (HIL) experiment results verify that IDC strategies have similar effects to VIDC while simplifying the control structure.

In Chapter 5 [M4], the multi-timescale impedance modeling framework is established to clarify the stability mechanism of VIDC and the LFO of VIDC controlled islanded DC-MG. Control loops of different timescales are visualized as independent loop virtual impedance elements to form an impedance circuit considering the CPL, rather than an all-in-one impedance as the

external dynamic representation of power converters. Concrete impedance analysis is performed on loop virtual impedances to reveal the impedance-shaping effect of control loops intuitively, the physical impedance nature of control parameters and the interaction between different timescale, which illustrates the stability mechanism of VIDC. The LFOs (*LC* impedance interaction) in voltage and inertia loops are elaborated by *RLC* circuits of loop virtual impedances. The potential instability factors resulting in poor damping against voltage oscillations are also revealed. Thus, a dynamic stability enhancement method is proposed to compensate for the negative damping caused by the positive feedbacks of VIDC and CPL, and a supercapacitor is added to alleviate rapid voltage changes. Accordingly, the passivity property of the system impedance is strengthened and the stability can be evaluated by Nyquist plot. Finally, the simulation and experiment results have validated the LFO analysis and stability enhancement methods.

In Chapter 6 [M1], an inertia-emulation-based cooperative control strategy for multi-parallel ESS in islanded DC-MG is proposed to address the state-of-charge (SoC) imbalance and voltage deviation problem in steady-state operation and the voltage stability problem caused by inertia-less in transient process, as well as an optimal parameter design is carried out. A SoC self-balance algorithm is developed to dynamically equalize SoC of energy storage units (ESUs). The defined SoC mismatch degree and the balance speed adjustment factor *k* are introduced into the droop resistance to adjust the SoC self-balance rate and eliminate the SoC deviation among ESUs. And the contradiction between SoC balancing speed and maintaining system stability is addressed by this redefined SoC-based droop resistance function. In addition, the inertia emulation loop is constructed by analogy with DC motors to dampen voltage oscillations, while the secondary voltage recovery loop is derived from the circuit equivalence of an inductor to indicate system stiffness and achieve zero-steady-state voltage deviation. The dynamic performance of the SoC self-balance algorithm is analyzed and the small-signal model of the multi-parallel ESS with the proposed strategy is established. Based on the eigenvalue analysis and step response, the system stability is assessed, and the influences of the control parameters on the transient response and stability margin are investigated. Considering the power constraint, the voltage deviation constraint and the stability constraint, the optimal design method of *k* is given. Finally, simulations and HIL experiments prove that the proposed control has better dynamic and static performances without modifying hardware and can equalize SoC in charge and discharge mode.

Finally, Chapter 7 summarizes all the research in the dissertation, points out the remaining

problems in the research process, and gives an outlook for the next research content.

2 Analysis of the State of the Art

Extensive research has been conducted on the stability analysis and stabilization control methods of power electronics systems, such as DC microgrids (DC-MG). This chapter presentes an overview of challenges and problems in the development of DC-MGs, including main topologies of DC-MG and the classification of DC bus voltage fluctuations (DC-BVF), stabilization control methods, low-frequency oscillation (LFO) mechanism analysis methods, and energy management systems. This chapter closes with concluding the reason for the stabilization technique and stability analysis approach pursued in this thesis.

2.1 Review of DC-MG Topologies and Bus Voltage Fluctuation Classification

Driven by practical requirements of certain DC-MG applications, various topologies and their applications have been reported in literatures [8], which are reviewed. Besides, since DC bus voltage stability is the key to the stable operation of DC-MG and needs in-depth study, the leading causes and classification of DC-BVF are analyzed and summarized.

2.1.1 Topologies of DC-MG and its applications

Typical DC-MG topologies and their applications are reviewed here. A number of topologies have been reported in the existing literatures and this section assess of the most prominent representatives. Generally, the DC-MG topologies can be classified into three categories, that is, single-bus topologies, multi-bus topologies, and reconfigurable topologies. Besides, this section also gives an overview of corresponding industrial scenarios.

(a) single-bus topology:

First of all, the single-bus topology is reviewed. As the basis of DC power systems, the single bus DC-MG topology is commonly deployed in industrial applications and a typical topology of single-bus DC-MG integrating RES has been presented in Figure 1.1. An energy storage system (ESS, usually an electrochemical battery pack) can be directly connected to the DC bus to maintain the DC bus voltage [13]. The number of series battery cells depends on the voltage required for the loads. This configuration operating at 48V has been used in telecommunications [14]. However, this configuration has the following drawbacks: (a) uncontrollable voltages, depending on the state of charge (SoC) and current of the battery, and (b) unregulated

battery charging [15]. As well as, ESS can be connected to the DC bus via a converter interface, which provides more flexible control and the possibility of connecting multiple buses to enhance system reliability or supply loads over a wider area [16], while paralleled converters exist circulating current problem which leads to uneven loading and accelerates the wear of the stationary battery [17]. The only one DC bus compels consumers to adapt to this voltage level, thus lacking flexibility. To solve this problem, a bipolar single regulated bus structure is proposed in [18]. This configuration provides load-side DC–DC converters with the option to select source voltages of 340, +170, and −170V. The system reliability is thus increased, since power can be supplied by the other two lines and an auxiliary converter in the event of failures of one line.

In addition, the single-bus DC-MG has been applied in some typical industrial scenarios. For example, a building-integrated microgrid is proposed in [19], and an advanced local energy management is designed to better integrate small photovoltaic plants into power grids. A 380V DC distribution system is built in [20] for test implementation, and the energy saving advantage of DC-MG over AC systems is verified in [21]. The bipolar configuration of DC-MG has also been applied to a residential complex for better system reliability and higher-quality power [22]. Meanwhile, single-bus DC-MG applications also involve renewable energy parks [23], hybrid ESS [24], and electric vehicle (EV) fast charging stations [25, 149]. In [23], a solar power optimizer is proposed for an interface converter to efficiently harvest maximum energy from a photovoltaic panel and then deliver energy to DC-MG. A novel use of superconducting magnetic energy storage (SMES) hybridized with batteries is proposed in [24], and a new power control algorithm is introduced to achieve higher usage efficiency of SMES and longer battery lifetime. In [25], the effective utilization of SMES and the optimal discharge algorithm for lithium-ion batteries are achieved by an optimized integration scheme to extend the battery lifetime in EV charging stations.

(b) multi-bus topology:

Subsequently, multi-bus DC-MG topologies can be composed by the estension of single-bus DC-MG topologies in order to obtain higher reliability and availability. A large number of related academic studies have been carried out and a typical multi-bus DC-MG topology is presented in Figure 2.1 where each DC-MG could absorb or inject power from its neighboring DC-MG in case of shortage or surplus of power. An interesting redundant bus configuration is proposed in [26] to improve system reliability and provide reconfiguration options, and two alternative methods of actively reconfiguring supply buses are presented. Similarly, a game-theory-

based modeling approach for bus selection is studied in [27], thus the optimal operating point of the multi-bus DC system is found by using a payoff table and the influence of nonlinear loads is also considered. In addition to the redundant bus configuration, multiple DC-MG clusters configuration by connecting neighboring DC-MGs can also be an alternative to increase system reliability. Power can be transferred between neighbors to ensure power supply in situations of power shortage or surplus. A distributed hierarchical control is proposed in [28] to regulate power exchange between DC-MG clusters at the expense of voltage deviations. In [29], a simplified equivalent model is established for LFO analysis of multi-bus DC-MG, and the impactors such as the number of inner voltage controllers, the line impedances and the operation mode of interlinking converters on the LFO are investigated. As for the protection system, an event-based protection technique is developed for multi-bus DC power systems in [30]. Without the high-speed communication and synchronization, the type of faults can be classified and the faulted area can be isolated very fast.

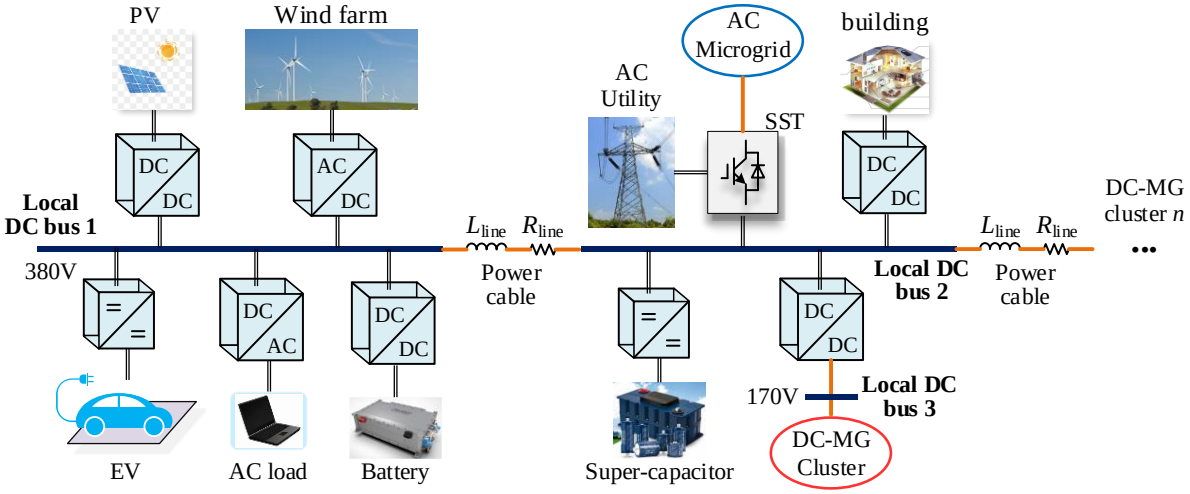


Figure 2.1: Typical topology of multi-bus DC-MG.

As an energy router, the solid-state transformer (SST) can realize the interconnection of DC-MGs of different voltage levels to enable a multi-bus DC-MG architecture. Compared with traditional transformers, the use of semiconductor devices and circuits makes voltage and current regulation possible [31]. In [32], the control strategy for SST is developed to ensure power supply reliability and provide stabilized low voltage DC network ports in both grid feeding and forming modes, and zero circulating power flow operation is also achieved. Based on multi-port DC-DC SST, Ref. [33] proposed a topology for bidirectional photovoltaic/battery-assisted EV charging stations. Further, considering the influence of EV battery capacity, EV battery SoC and EV departure time, an adaptive bidirectional droop control for the EV charging/dis-

charging process is proposed to maintain DC bus voltage with less communication [33]. Recognizing the potential of SST, many academic and industrial projects are launched as testbeds for flexible and modular power electronic interfaces which are able to connect different kinds of sources and loads [34-35]. Simplified forms of the multi-bus DC-MG are derived in [36] by adopting generalized voltage sources, generalized current sources and two-port models. System stability is subsequently assessed with the help of impedances or admittances for each bus port.

(c) reconfigurable DC-MG topology:

Finally, reconfigurable DC-MG topologies such as the ring structure and the zonal architecture have also been proposed in order to further exploit new degrees of freedom with regard to flexibility, reliability and fault tolerance, which are also reviewed here and presented in Figure 2.2. A universal simulation approach for zonal architectures and ring topologies is introduced in [37], which covers all intended variations of hardware configurations and makes it possible to build a fully automated model. Lacking an effective protection system might jeopardize the resilience of DC-MG. Fault detection, location and clearance become complicated because of the absence of natural zero-crossing points, and the need for fast DC circuit breakers is indispensable [39]. To overcome this challenge, extensive studies on the design and implementation of accurate protection schemes have also been conducted. Based on monitoring the modified squared poverty gap index difference, a protection strategy for the ring-bus DC-MG is developed in [38] by employing intelligent electronic devices and solid-state circuit breakers. In [40], a fault protection and location scheme is presented, which can detect the fault current in a bus segment and isolate this segment to avoid the shutdown of the whole system.

Moreover, the zonal architecture of DC-MG features high reliability, and a power management algorithm, which has the advantage of maximum utilization of local distributed resources and smooth transition between different modes, is proposed in [41] based on this configuration. A novel three-port DC-DC interface is designed and a zonal DC-MG architecture is thus proposed in [42] to reduce the energy conversion stage and improve the conversion efficiency. In [43], stability assessment is carried out for a zonal power system with voltage mode droop control, and the impact of droop gain is investigated by the eigenvalue method. The problem of selective protection for zonal DC systems is analysed in [44], and a selective protection based on the coordination between the power electronic fault current limiting and low-voltage protection devices is designed, featuring quick fault response and excellent reliability/continuity. A real-time resistance-based fault detection technique for Zonal DC-MGs is proposed in [45], showing

the advantages of fast fault isolation, communication network less protection, and so on. Besides, this technique can be extended to grid-connected and ring-type DC-MGs.

The multi-terminal DC (MTDC) system can deliver power through multiple paths, which might form a ring structure and also enhances flexibility, although the system structure becomes more complicated. Originally, MTDC is proposed for high-voltage DC (HVDC) transmission and has a meshed architecture [46]. In order to improve the reliability and flexibility of DC-MG, the multi-terminal structure is gradually adopted [151]. This also improves the controllability and security of DC-MG and facilitates the access of large-scale RES to the power system and its interconnection with the utility grid [47]. Maintaining good dynamic stability is the basic premise for the security and stable operation of a MTDC microgrid, the interaction dynamics between multi-controllers and the multi-timescale coupling are investigated in [48], and a reduced-order model is developed for dynamic stability analysis. In order to minimize the DC-MG operation cost, the real-time electricity price is forecast by an adaptive learning algorithm. Therefore, the system profit is maximized by buying energy at low prices and selling it at high prices [49].

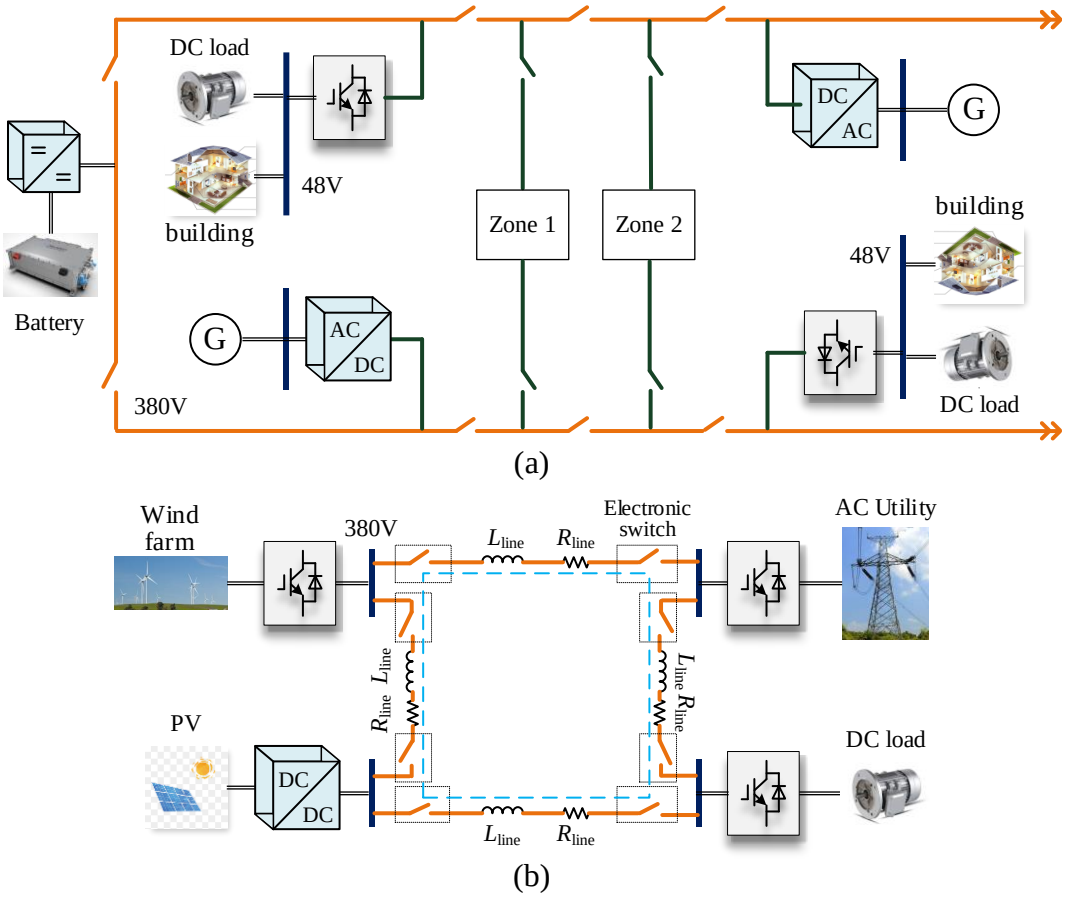


Figure 2.2: Typical reconfigurable topology of DC-MG. (a) Zonal DC-MG architecture. (b) Ring-bus based DC-MG.

The power availability and reliability of DC-MG can be improved by interconnecting with AC infrastructures via a AC/DC converter. In this way, either a hybrid AC/DC microgrid (H-MG) or an AC grid connection is established. As one of the most important devices to realize the interconnection of AC system and DC-MG [32], the SST can provide both AC and DC bus and has flexible voltage and power control. With the help of SST, the large-scale interconnection between DC-MG and AC infrastructures becomes possible and can be realized by zonal architecture. Focusing on the energy management system and coordination control of H-MG, many works have been done in existing literatures. In [50], a new structure of a interlinking converter composed of a converter in series with a static reactive power compensator, is proposed for H-MG and a new droop control method is accordingly developed for the proposed interlinking converter to regulate the fundamental active and reactive power flow, and a fast harmonic control is presented to improve the filtering characteristics. A comprehensive control scheme consisting of the outer loop of flexible power sharing control and the improved-robust inner loop control is developed in [51] to achieve flexible power sharing of distributed generations (DGs) and suppress external disturbances and uncertainties of the system model.

The thorough discussion of the state of the art of the DC-MG topologies and its main applications is summarized in Table 2.1, and the reported voltage levels are also involved. The typical applications of DC-MGs are shown in Figure 2.3.

Table 2.1 Overview of DC bus configuration and applications

DC bus configuration		Reported voltage levels (V)	Remarks	Applications
Single bus DC-MG	• Direct battery connection • Single unipolar regulated bus • Bipolar regulated bus	12, 24, 48, 380 ±170, 340	• Uncontrollable voltage • Unregulated battery charging • Circulating current problem • Only one bus voltage level	Telecommunication High efficiency households Renewable energy parks Hybrid ESS EV fast charging stations Maritime on-board power systems
Multi-bus DC-MG	• Redundant bus configuration • Multiple regulated bus • SST-based MG	48, 380 and higher	• High reliability and flexibility • Higher power availability • Regulated voltage and current	
Reconfigurable DC-MG	• Ring bus configuration • Zonal DC-MG • MTDC MG • Interconnection between DC- and AC-MG (Hybrid-MG)	24V and higher 380 and high 380 or high, and used for HVDC system	• Better flexibility during faults and periodic equipment maintenance periods • High reliability and redundant operation in case of faults • Increased faults tolerance and power availability	

2.1.2 Leading causes and classification of voltage fluctuation

Different from AC systems, DC-MGs have no reactive power fluctuations, so the bus voltage becomes the only indicator for measuring the stability of DC-MG. The instability of DC bus

voltage threatens the stable operation of loads. Therefore, the main task of DC-MG is to maintain the stability of DC bus voltage, which can also be expressed as maintaining the energy balance between the 'source' terminal and the 'load' terminal. In DC-MG, power fluctuations, oscillations or sudden changes and the interaction between the converters connected to DC bus would lead to DC-BVF. Generally, connecting capacitors is a straightforward approach to suppress voltage fluctuations but would bring additional power losses and is limited by certain application scenarios with limited space, such as ship electrical systems [52]. At present, there are a lot of studies on the leading causes, classification, and mechanism analysis of DC-BVF. In this section, DC-BVF is reviewed according to timescales, frequency characteristics and generation mechanisms, and divided into the disturbance-type DC-BVF and the oscillation-type DC-BVF [53]. Table 2.2 summarizes the mechanism classification of DC-BVF.

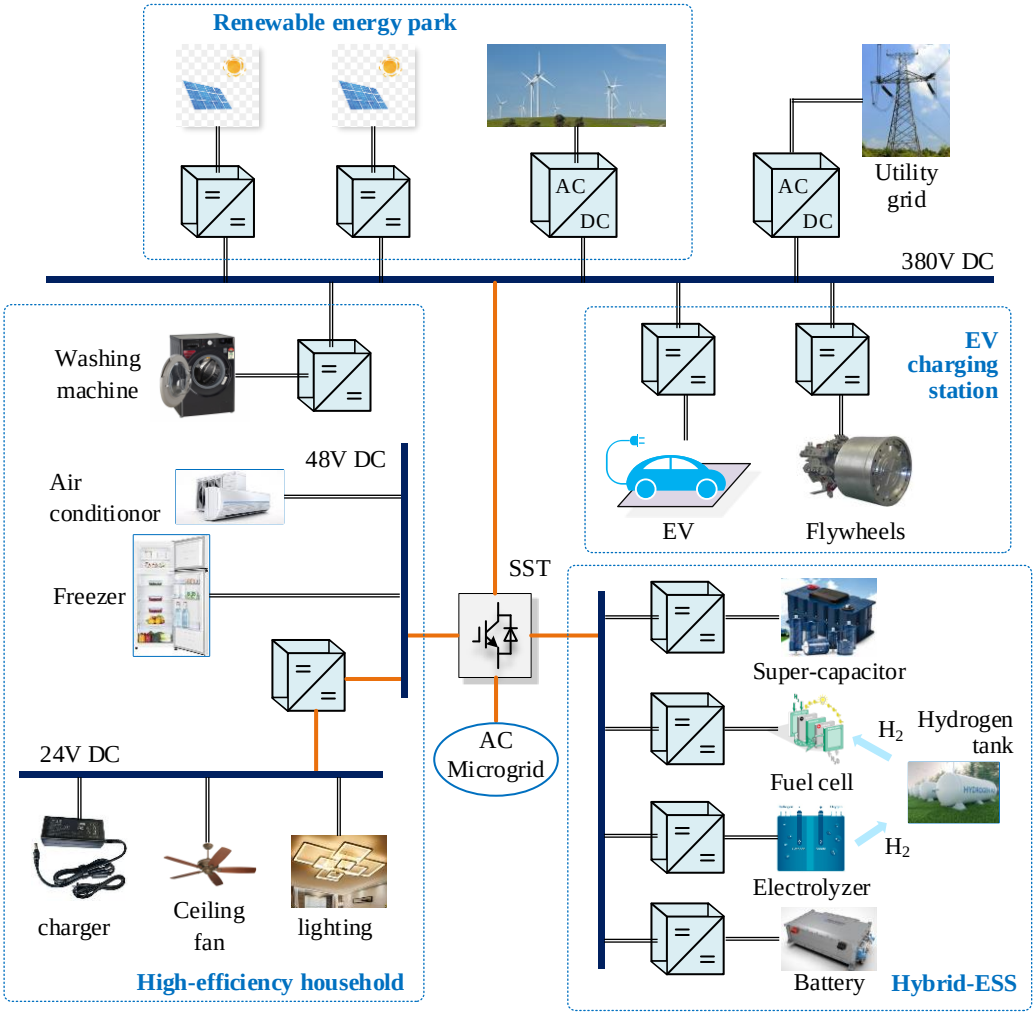


Figure 2.3: Typical applications of DC-MG.

The low-frequency voltage fluctuations caused by the fluctuations/switching of loads/DGs and other factors are defined as disturbance-type DC-BVF. The corresponding phenomena are DC

bus voltage overshoots, low-frequency non-periodic oscillations and underdamped oscillations. The main reason for this type of DC-BVF is the imbalance between the input power and the output power on DC bus. In addition, there is a long-term fluctuation caused by factors such as the dynamic interaction between paralleled converters connected to DC bus, grid faults, harmonics and imbalances, which is referred to oscillation-type DC-BVF. The main reason for the oscillation-type DC-BVF is the changes in system characteristics.

In an islanded DC-MG, the interaction between converters, changes in control parameters and load fluctuations will affect system stability and even lead to system instability. Converters can be divided into bus voltage control units and output power control units. Certain power control units can be equivalent to constant power loads (CPLs) and their negative impedance characteristics introduce negative damping which can reduce the stability margin [54].

Table 2.2 Overview of DC-BVF classification

DC-BVF classification	Disturbance-type DC-BVF	Oscillation-type DC-BVF
Mechanism	• Load fluctuation • Fluctuation of DGs • Switch of load or DGs	• Dynamic interaction between paralleled converters • Grid faults, harmonics, and imbalance
Leading causes	The power imbalance	The change of system characteristics
Phenomenon	• Voltage overshoot • Low-frequency non-periodic oscillation • Low-frequency underdamped oscillation	• Low-frequency underdamped oscillation • High-frequency underdamped oscillation

2.2 Review of Stabilization Control Methods in DC-MG

As the key to the integration of RES into DC-MG, power converters are replacing conventional synchronous generators (SGs) that contribute most of the inertia in the power system. Therefore, the lack of inertia may challenge the operation and control of modern power systems. On the other hand, load converters are generally controlled by high-bandwidth controllers and behave as CPLs whose negative impedance characteristics reduce system damping, decrease stability margin and even lead to voltage instability. To sum up, DC-MG is a typical inertia-less and poor-damping power system. An overview of existing stabilization control methods, which are mainly divided into three categories: passivity-based control methods, virtual inertia and damping control methods, and impedance-reshaping-based control methods, is described as follows.

2.2.1 Passivity-based control method

From the perspective of passivity theory, system passivity can be enforced by controlled active

damping impedances [55]. The DC voltage is indirectly stabilized by passivity-based control with the Brayton–Moser framework, and the series or parallel damping based solutions are used to solve the error dynamics issue [56]. A simplified parallel-damped passivity-based controller is proposed in [57] to maintain its robust output voltage regulation and a complementary PID controller is designed to remove the steady-state error. The classical linear controllers are simple to design and implement, but there are difficulties in dealing with the uncertainty of system parameters, and the right half-plane zero is ignored.

The passivity-based control (PBC), a kind of nonlinear control method, could achieve energy shaping by a damping injection matrix and its control law can be easily implemented by using the structure property of physical systems [71]. The virtual damping injection is realized and the voltage regulation issue is addressed [19]. The port-controlled Hamiltonian (PCH) model describes the energy interaction between modeled systems and external environments via ports. The interconnection and damping assignment-passivity-based control (IDA-PBC) can achieve the active damping control of PCH systems by modifying the energy exchange and dissipation, and the transient response is improved [59-60]. It is worth noting that the arbitrary interconnection of IDA-PBC can remain stable since the passivity is preserved in the resulting system [70].

Based on the passivity theory, Ref. [58] proposes a nonlinear controller to change the energy dissipation property and enhance the voltage regulation ability against the variation of system parameters. The voltage stability challenge of DC-MG is addressed in [70] by applying the IDA-PBC method to the PCH model of a source-side converter. In [61], the IDA–PBC technique is utilized in the voltage outer loop and the damping performance is improved. In addition, an extra integral loop is used to eliminate the voltage error. The PCH model of a power electronics transformer is built in [62] and IDA-PBC is applied to address its voltage regulation issue. Adaptive IDA-PBC can also be used to solve the problem that the bidirectional DC converter (BiC) is non-minimum phase characteristic [63], but the model only considers the buck state. In [64], an improved IDA-PBC scheme is proposed to make the interconnection matrix adaptive. And the PCH model of a DC converter is established and the unique control equations are acquired. The IDA-PBC is utilized in [65] to ensure the stability of a cascaded system by using the Hamiltonian function, and the dynamic instability problem is solved. In [66], a boost converter is modeled as a PCH system and the damping performance is improved by an adaptive IDA-PBC method. Besides, an equivalent circuit is derived and control parameters are determined. In [67], a modified IDA-PBC is proposed to ensure the passivity property of an *LC* input filter-DC/DC converter system, considering the interaction between the *LC* filter and DC/DC

converter. Combined with the modified IDA-PBC, a nonlinear observer is presented in [68] to eliminate the steady-state error and reduce the number of sensors. In [69], an adaptive energy shaping control based on IDA-PBC is developed to guarantee the large-signal stability of power converters with an input filter.

Besides, some improved-PBCs have been developed. In [91], a robust-PBC strategy is presented to mitigate the instability effect of DC–DC boost converters in DC-MG, and a nonlinear disturbance observer is added and works in parallel with the PBC strategy to improve the control robustness against both line and load variations. From the viewpoint of data-driven control, a model-free approach which can set-up passive controllers and is purely based on measured data is proposed to guarantee stability in a deterministic way [92]. An adaptive-PBC strategy is proposed in [93] for buck-boost converters, and an immersion and invariance parameter estimator is introduced to guarantee global convergence and preserve asymptotic stability.

2.2.2 Virtual inertia and damping control

As more SGs are phased out and replaced by power converters, the entire power system becomes more inertia-less, which becomes a major concern for system stability and converter control [72]. In DC-MG, its inertia manifests the ability to prevent sudden changes in DC voltage [73]. More specifically, due to the presence of interface converters with fast response ability, the DC bus voltage may easily oscillate beyond the acceptable range, leading to generation tripping, undesired load shedding, or even system collapse [74]. This means that DC-MGs do not have sufficient inertia to stabilize the DC bus voltage. Therefore, inertia-emulation techniques have already been developed to tackle the issue of lacking inertia.

Originally, virtual inertia and damping control is proposed as virtual synchronous generators (VSGs) or virtual synchronous machines (VSMs) to solve the frequency stability of AC microgrids with a high penetration rate of RES. The basic concept is that, by emulating the moment of inertia of SGs, power converters (synchronverters) can exhibit the swing character and control the frequency within an acceptable range [75]. The inertial dynamics of virtual-synchronous-controlled doubly fed induction generator (DFIG) based wind turbines is investigated in [76]. Thus, DFIG based wind turbines can provide the desired inertial support for power grids. In [77], an oscillation damping approach for DGs is developed to control an inverter to behave like a SG and produce virtual inertia during a short operation time. A derivative control-based virtual inertia is introduced in [78], and the virtual inertia makes a considerable improvement in the initial overshoot response and damping characteristics of HVDC links.

However, none of the above work involves the solution of inertia reduction in DC-MGs. In DC-MGs, connecting capacitors is a straightforward approach but will bring additional power losses, and is limited by certain application scenarios with limited space [79]. In [80], a droop scheme is proposed so that DC sources can be coordinated together with the frequency of AC voltage, like SGs in conventional power systems. Through the AC/DC analogy, virtual inertia emulation techniques have been developed in DC-MGs. The virtual inertia of DC-MGs can be enhanced by the kinetic energy in rotors of permanent magnet synchronous generator based wind turbines, the energy stored in ESS and/or capacitors, and the energy from utility grids [74]. Therefore, the output power of converters can be changed in response to the DC bus voltage in the presence of power fluctuations [76, 81]. In [73], a virtual inertia control strategy for bidirectional grid-connected converters is proposed to enhance the inertia of DC-MGs and the parameter design is discussed. A VSG control strategy is introduced to dampen DC-side oscillations in a wide frequency range and enhance the inertia of DC networks [82]. Another idea is developed in [84], where inertia and damping are emulated by making the external characteristic of ESS interface converters have the charging and/or discharging conversion form of capacitors. In [83], a virtual capacitor control is proposed, which utilizes the energy storage capability of modular multilevel converters to attenuate voltage fluctuations of HVDC systems. By establishing the relationship between the inertia coefficient and the rate of change of voltage (RoCoV), the adaptive adjustment of virtual inertia is realized in [85] to improve system stability. Ref. [86] proposes a virtual inertia control (VIC) for photovoltaic arrays to enhance the inertia of a hybrid photovoltaic array-battery DC-MG. Virtual inertia matching method of parallel VSGs is proposed in [87] to ensure that the transition process remains synchronized. The VIC in previous works mentioned above only simulated the swing equation of SGs or the energy conversion form of capacitors to control the external characteristic of BiC, which is essentially a virtual capacitor control. Moreover, the output of inertia loop is the output voltage reference of BiC, which affects the static characteristics.

Therefore, new control strategies suitable for DC-MGs are needed and the concept of operating BiC of ESS as a DC machine is proposed in [88] to emulate rotor inertia and regulate DC bus voltage fluctuations. A similar concept of virtual DC machine (VDCM) is also developed in [89] to flexibly imitate the rotor inertia characteristics and alleviate voltage fluctuations. Its essence is the systematic combination of VIC, active damping control and virtual resistance control. However, this concept of VDCM is actually not clear, the controller structure and parameter design are complicated and the multi-parallel operation is not analyzed. In [90], the

droop curve swinging in response to transient voltage variations is proposed to provide the necessary inertia power and reduce RoCoV while sufficient damping cannot be ensured.

To sum up, virtual inertia controls have been developed for DC-MGs, but this technique is incomplete in both theoretical and practical regards, and the matching method and parameter design deserve further investigation by researchers and engineers.

2.2.3 Impedance-reshaping-based control method

The stability of DC-MGs can also be improved by impedance-reshaping based control methods, which will reshape the small-signal impedance characteristics to meet impedance stability criteria by parameter adjustment or additional control loops. It is found in [94] that the negative damping characteristic of the output impedance outside the voltage-loop bandwidth makes the traditional virtual resistance stability control fail to mitigate the DC-side oscillation. Therefore, a virtual phase-lead impedance stability control is proposed to correct the output impedance to a positive damping characteristic. Subsequently, a virtual positive damping reshaped impedance stability control is proposed in [95] to maintain a larger positive damping in a wider bandwidth regardless of the variation of DC cable length, which enhances the system stability at a low switching frequency. In [96], a coordinated reshaping control is proposed to simultaneously compensate for the high-frequency negative damping caused by grid impedances and control delay, improving system stability and maintaining the required control performance.

In DC-MGs, power electronic converters (PECs) with feedback loops may behave as CPLs, which have a negative input impedance. And the interaction between CPL and a poorly damped input *LC* filter could make the system prone to instability. In order to eliminate the negative impedance characteristic of CPLs, a feedforward technique is proposed in [100] to create a virtual *RC* impedance, which has only one variable that can be determined by the input filter parameters and is independent of the type of CPLs. As well as, a power adaptive parallel virtual impedance control is achieved in [97] for the load-side converter to improve the stability of a cascaded DC system, and the simplification of the compensation controller is made to be independent of the *LC* and control parameters, which is easy to implement and has high reliability. In addition, various stabilization dampers have been developed to address the instability caused by the interaction between the *LC* filter and CPL, which however would degrade the performance of the original *LC* input filter. In order to overcome this drawback, Ref. [98] proposed a *RLC* damper to stabilize DC-MGs while ensuring the performance of the *LC* input filter. Thus, a virtual *RLC* damper is implemented to avoid the power loss of a physical *RLC* damper.

The active damping solutions in [99] depend on reshaping the impedance of voltage source converters (VSCs) by injecting an internal-model-based active damping signal into the outer, intermediate and inner control loops of voltage-oriented VSC interfaces, and their effects on damping improvement and control performance are also presented. However, the injected stabilization signal may cause undesirable effects on the loads. In Ref. [102], virtual-impedance-based control strategies considering system stability and dynamic performance of load converters are proposed to connect a virtual impedance in parallel or in series with the load converter's input impedance, which is thereby reshaped in a small frequency range. Similarly, two impedance compensation methods are designed in Ref. [103] to enhance the stability of a dual active bridge-based ESS, including the stability-oriented optimization guideline for the feedback controller and the impedance shaping controller which solve the instability issues even under heavy load conditions. For CPLs under voltage mode control, two linear active methods are proposed to design feedforward loops for impedance modification [104]. In order to obtain the optimal performance for stabilization, an additional low-pass filter is designed and added in the feedforward loop, i.e., a larger stability margin can be achieved. Instead of changing the input impedance of CPLs, Ref. [101] proposes an active-damping method that stabilizes the system from the source-side converter to avoid the compromise between stability margin and load performance. A virtual resistance is built in the source-side converter and works around the resonant frequency of the *LC* input filter so that the Middlebrook's stability criterion can be met.

2.3 Review of Modelling and Stability Analysis Method

In order to figure out the oscillation mechanism and its influence, an appropriate framework for dynamic modeling and stability analysis is required. Therefore, the stabilization method can be proposed and improved. At present, three common modeling approaches are used for the small-signal stability analysis of power electronics systems: the impedance-model-based method, the state-space-model-based method, and the transfer-function-based method.

2.3.1 Impedance-model-based stability analysis methods

As an intuitive and effective dynamic representation of PECs, the impedance-based method can illustrate the LFO and evaluate the stability of modern power systems by Nyquist stability criterion [105]. The low-frequency interaction between source-side and load-side VSMs can be revealed by the generalized Nyquist criterion and the generalized inverse Nyquist criterion. The instability caused by the dynamic interaction between the source-side VSG and the load-side

VSM is investigated in [106], and it is found from impedance analysis that the impedance interaction violates the generalized Nyquist criterion and the load-side VSM behaves negative resistance. Thus current feedforward and voltage feedback controls can be designed for VSGs to reshape their impedance and mitigate the low-frequency interaction between a VSG and load-side VSM. Taking the coupling between the AC and DC dynamics into account, the hybrid AC–DC impedance model of a VSM is established in [107] to analyze the LFO mechanism, and a five-dimensional impedance stability criterion based on the established impedance model is proposed to estimate the system stability. The impedance modeling of directly power-controlled VSCs is discussed to study the stability of grid-integration [108]. After transformed into a positive-sequence impedance, the impedance matrix can be analyzed by using single-input single-output (SISO) Nyquist criteria, and the influences of control parameters and the short-circuit ratio of power grids on the system stability are investigated. The mechanism of sub-synchronous oscillation (SSO) in DFIG-based wind farms can also be revealed by the impedance-based analysis. In [109], the impedance model of a DFIG-based wind farm is represented as an *RLC* circuit to quantify the start-SSO condition. From the theoretical analysis results, the DFIGs (which behave as an inductance in series with a negative resistance) and the wind farm side VSC (which is regarded as a resistance–capacitance element) constitute an equivalent *RLC* resonance circuit with a negative resistance, and the negative damping leads to the SSO.

From the point of view of energy dissipation, the passivity-based stability analysis of impedance model can reveal the relationship between unstable resonances and the non-passivity property. The effects of different control loops and operating points in the *dq* frame on the passivity property are analyzed in [110] to assess the system stability in the frequency domain. On this basis, a virtual damping control method is then designed to guarantee passive regions over a wider frequency range. How the digital control delay affects the output impedance of a voltage source inverter and its system stability is studied in [111]. When the control delay is considered in the impedance model, a magnitude drop and a phase rise appear at the high-frequency region, resulting in an impedance mismatch between the grid and the voltage source inverter, and high-frequency oscillations.

In addition, the impedance-model-based method gives an intuitive insight into the physical sense of control parameters [112-114]. In [115], the output impedance model of the DC voltage control system is represented as a parallel *RLC* circuit to give intuitive physical implications of PI parameters, and a dynamic impedance ratio is introduced to obtain the generalized *RLC* parallel impedance model for stability analysis. However, the existing impedance model lacks a

systematic and intuitive insight into the internal roots of underdamped or instability factors and is essentially a black-box model [116]. The impedance nature of each control loops, especially the virtual inertia loop, is seldom understood to clarify the LFO mechanism in more complex DC systems. The relationship between potential instability factors and control loops/parameters cannot be identified intuitively.

2.3.2 State-space-model-based stability analysis method

As a global stability analysis method, the state-space-model-based approach can identify system stability regardless of the location of instability roots and thus has been widely used to analyze the stability of microgrids, VSC-HVDC, modular multilevel converter (MMC) based HVDC systems [123] and interconnected AC power systems with DC grids [124]. The harmonic instability of inverter-fed AC power systems is investigated in [117] by using state-space modeling, and eigenvalue-based stability analysis assesses the influence of controller parameters on harmonic instability. The detailed state-space model of a VSC-based MTDC system is presented in [118] to carry out the stability analysis and define the appropriate range of controller parameters. The interaction between VSC and DC power-flow controllers is further investigated in [119], and the impact of VSC controllers on MTDC grids is then discussed. In addition, the interaction modes in a VSC-based MTDC are systematically identified and classified in [120] based on aggregated participation factors, which provides a fundamental insight into understanding the system dynamics and serves as a framework for analyzing and mitigating such system-wide interactions. In [121], resonance instabilities in VSC-HVDC are investigated by representing this VSC-HVDC as a feedback interconnection of two subsystems. How the commonly used simplifications of the state-space model affect the stability assessment result is studied in [122]. Taking the aggregated effect of internal variables, the circulating currents and the associated control loops into account, an equivalent simplified state-space model of a grid-connected MMC is derived in [123] for stability analysis. In [124], the critical modes of interconnected AC/DC power systems are identified and their interactions with different typical system configurations and controllers are revealed by eigenvalue-based stability analysis. Besides, a modular nonlinear-state-space modelling methodology for power electronics systems is proposed in [150] with the purpose of equilibrium point computation, system-level eigenvalues analysis and nonlinear time-domain simulations. The above stability analysis process can also be applied to identify the oscillation modes of meshed-MTDC systems consisting of multiple power converters.

Based on the above analysis, the state-space model describes each variable of the system and

thus can provide insight into the leading causes of underdamped or unstable modes via participation and sensitivity analysis, and facilitates the derivation of sufficient conditions to guarantee the existence of equilibrium of DC-MGs. However, the state-space model is a white-box model in nature and requires complete system information, including hardware parameters and the control system. Its abstract form makes it difficult to intuitively clarify the mapping between the oscillation modes and the corresponding factors, which is requested by practical engineers.

2.3.3 Transfer-function-based stability analysis method

In order to avoid the multi-variable nature of stability analysis, research has been done to convert a multi-input multi-output (MIMO) model into a SISO model. Due to the advantages of simplicity, convenience in physical interpretation and the ability to identify the stability margin, the transfer-function-based stability analysis method has also been broadly used in stability analysis of power electronics systems. In [125], the equivalent SISO model of a VSC-HVDC system is deduced from its MIMO transfer function model by integrating the main circuit model and the interactive control loops, then an interpretation for the instability of VSC systems under weak AC grid conditions is given from the viewpoint of the coupling degree of different control loops. Similarly, the equivalent SISO model of a MIMO VSC-dominated power system can be used to analyze the mechanisms of voltage amplitude and phase dynamics in the current-control timescale [126], by reserving and converting the interactions between VSC's inner variables. Besides, this SISO equivalent method can also be used to quantitatively study the interaction of multi-VSCs. In [127], the converter–grid interconnection is first considered in MIMO systems which can be resolved into a SISO system with cascaded closed-loop transfer functions. Then the standard SISO Nyquist stability criterion can be applied to stability analysis and optimal design of controller parameters ensuring adequate stability margins [128]. Moreover, the transfer-function-based analysis method can reveal the effect of the interaction between the control loops on the power stability limits of the VSC connected to an AC-grid [129] and the maximum transferable power is assessed by power current sensitivity and affected by the controller parameters. Ref. [130] interprets the instability causes in view of a particular modal resonance within the VSC control, and an approximate multi-modal decomposition approach is adopted to quantify the extent of interaction by the incremental damping and frequency drift superimposed on each mode. It is found that a strong interaction between control loops would force the lower-frequency mode to move toward the decreased frequency and damping direction, while pushing the higher-frequency mode to go to the opposite direction. In Ref. [131], the dynamic characteristics of VSCs integrated with a weak grid are investigated on DC-link

voltage control timescale. And the effects of grid strength, operating points and control loop interactions on the performance of VSCs are studied by employing eigenvalue analysis. Further, the dynamic interaction between multiple VSCs on the DC voltage control timescale has been highlighted in [132].

It is worth noting that the effect of grid strength is taken into consideration in the built MIMO small-signal model. However, it can be seen from the above overview that the SISO transfer-function-based stability analysis [125-130] does not include the effect of grid impedances.

2.4 Review of SoC Balance Method

Multi-parallel ESS is indispensable as the supporting energy source of DC-MG and battery cell are the widely used energy storage unit (ESU) [133]. The ESU parameter mismatches, such as various series resistance, different self-discharge rates, and uneven operation temperatures across ESU, result in significant divergences of SoC among ESUs. The unbalanced SoC leads to over-charge/-discharge and even explosion, degrades the utilization of some ESUs and shortens the operation lifespan of batteries [134]. Besides, the BiC is essential to connect ESS to the DC bus and realize the voltage conversion, making the multi-parallel ESS an inertia-less system. Hence, SoC balance is another issue in DC-MG except for the dynamic stability problem.

The SoC balance of ESUs deserves attention to avoid unexpected hazards, for instance, overheat and explosion. Thus several SoC balance strategies have been explored in many literatures. Based on the current-SoC droop concept, SoC balance for a series-connected battery system is achieved by an adaptive control algorithm [134]. In [135], the concept of "smart cell" is introduced to balance battery cells by using a MMC topology. A battery management system has been developed for the SoC balance of battery cells connected in series in ESU [136]. In addition, the SoC balance of ESUs also deserves attention to avoid unexpected hazards, for instance, over-heat and explosion. A hierarchical control is presented in [137] to equalize SoC at both cell level and ESU level by its modulation scheme for the duty cycle of switches. Refs. [138] and [139] add SoC information into the current deviation factor to modify the current reference and balance SoC of modular multilevel ESS, but this current correction method degrades the current regulation ability. Note that, the above methods focus on the series-connected ESS.

To address the SoC imbalance problem in multi-parallel ESS of DC-MG, the droop coefficient is adjusted by a PI controller according to the SoC level to achieve SoC balance [140], but the extra controller complicates the parameter design, makes the control complex and increases its difficulty in practical applications. Besides, SoC information can be incorporated into droop

coefficients in other forms to redistribute power and remove SoC divergences [141-144]. A distributed secondary level control has been designed in [141]. The SoC imbalance compensation alters the virtual droop resistance according to the difference between ESU SoC and the average SoC, while its defect is the non-adjustable SoC balance speed. The degree of SoC imbalance is added to the armature resistance in [142] to dynamically balance power and SoC simultaneously. And the SoC balance rate can be adjusted by an adjustment coefficient. The SoC information can also be embedded in the droop coefficient in the form of SoC^n and the load sharing speed can be adjusted by changing the exponent of SoC [143-144]. However, the droop coefficient is dependent on SoC and is very small in the initial stage, which may cause instability. An improved distributed cooperative control strategy adopting a hierarchical control structure is proposed in [145] for multi-parallel ESS, and the SoC convergence speed and accuracy can be adjusted by the introduced balance adjustment factor. A multi-agent-based distributed control is proposed for SoC balance in [146] where a SoC-based frequency-power droop is constructed by adding a SoC-related term to all units.

Solutions have been developed for SoC unbalance of multi-parallel ESS of DC-MG, but these methods mentioned above are theoretically incomplete, for example, lacking parameter optimization methods considering various variable constraints and stability constraints. Besides, most studies ignored the voltage support capability of ESS to improve system inertia and stability when balancing the SoC.

2.5 Summary

This chapter presents an overview of the development of DC-MGs, including aspects of hardware topologies, modelling methods, stability analysis methods, and stabilization controls. As well as, the leading causes of bus voltage fluctuations are summarized and classified. As an important element to maintain power balance, ESS is indispensable and the corresponding SoC balance methods are also reviewed.

Generally speaking, a single-bus DC-MG can be regarded as the basic unit of multi-bus and reconfigurable DC-MGs. The controllability and flexibility of PECs bring adaptability to different voltage levels, reliability and higher power availability, which makes it possible for DC-MGs to be broadly applied to various industrial applications, such as high-efficiency households and EV fast charging stations. In addition, the DC bus voltage is the only indicator to measure DC system stability, thus voltage fluctuations are categorized as disturbance-type and

oscillation-type DC-BVF, and their leading causes are summarized. As we all know, PEC regulated by a broadband control makes the DC-MG a typical inertia-less and poor-damping power system, thus destructing the system stability and even leading to voltage instability. To solve this issue, many stabilization control methods have been developed to improve system damping and enhance system inertia, inhibiting DC voltage oscillations and suppressing RoCoV. According to the control principle, these stabilization control methods are divided into three categories: passivity-based control methods, virtual inertia and damping controls, and impedance-reshaping-based control methods. Moreover, a proper framework for dynamic modeling and stability analysis is required to study the mechanism of voltage oscillations and the influence of circuit/control parameters. Therefore, this chapter also provides an overview of the main modeling and stability analysis methods, including impedance-model-based methods, state-space-model-based methods, and transfer-function-based methods.

On the other hand, the unbalanced SoC leads to over-charge/-discharge, degrades the utilization of some ESUs and shortens the battery lifespan. Thus, the SoC balancing method of ESS is also reviewed. According to the different connection methods of ESS, it is divided into the SoC balance algorithms for series-connected battery systems and for multi-parallel ESS.

In summary, suppression of LFO and stabilization mechanism analysis for DC-MGs are more complex research fields, and worth studying to promote the development of DC-MGs in industrial applications.

3 A Virtual Inertia and Damping Control to Suppress Voltage Oscillation in Islanded DC Microgrid

In conventional power systems, synchronous generators (SGs) autonomously slow down or speed up in accordance with the grid frequency. In this way, SGs release/absorb the energy to/from the power grid so that the power mismatch can be compensated partially. This effect is quantitatively evaluated by the per unit kinetic energy, which is defined as the power system inertia. In islanded DC microgrids (DC-MGs), its inertia manifests the ability to prevent sudden changes in DC voltage.

However, as the penetration levels of renewable energy sources (RES) grow, more SGs are phased out and replaced by power electronic converters, because RESs are normally coupled to power grids through power electronic devices without any rotational inertia. Thus the entire power system becomes more inertia-less. More specifically, due to the presence of interface converters with fast response ability, the DC bus voltage may easily oscillate beyond the acceptable range, leading to generation tripping, undesirable load shedding, or even system collapse. This means that islanded DC-MGs do not have sufficient inertia to stabilize the DC bus voltage. Therefore, developing various measures is necessary to improve the dynamic response.

This chapter studies the dynamic voltage support ability of energy storage systems (ESS) and proposes a virtual inertia and damping control (VIDC) strategy. Without modifications of system hardware, inertia can be synthesized by the energy stored in ESS to mitigate voltage oscillations caused by power disturbances. Taking advantage of the high energy density characteristics of batteries, virtual inertia power and damping power are provided for ESS without increasing system cost and complexity, since only the dynamic output characteristics are affected by changing the control loop to compensate for the transient power disturbances. Generally, the power disturbance is much smaller than the load power under normal operation and ESS is always necessary in islanded DC microgrids (DC-MGs) for voltage regulation, so the capacity of ESS need not to be changed. It is worth noting that the proposed VIDC strategy is derived based on the physical model of DC machines, instead of the swing characteristics of synchronous generators (SGs). The concept, implementation, stability analysis, inertia matching

method of the VIDC strategy and parameter design are studied. In addition, based on the principle of equivalent DC machines, it is easier to achieve inertia matching of multi-parallel bidirectional DC (bi-DC) converters controlled by VIDC. The content of this chapter has been published in "*IEEE transaction on energy conversion*" [M6].

3.1 Topology of the Studied DC-MG and its Simplification

From Figure 1.1, a simple islanded DC-MG system studied in this chapter is obtained as shown in Figure 3.1. It composes of a group of renewable energy source (RES), an ESS (i.e. battery) and multiple constant power loads (CPLs). The structure of the bi-DC converter that applied in both the RES and the ESS is shown in Figure 3.2(a). The dual loop control strategy is applied for the ESS control, while the constant power control strategy (where only the current inner loop is reserved) is applied for the RES. The structure of the buck convertor for the CPLs is shown in Fig. 3.2(b). The buck converter attaching to a resistor R also adopts a dual loop control strategy. It regulates its output voltage to simulate a CPL and P_{const} is its consuming power. The corresponding parameters of the above convertors are shown in Table 3.1. The DC voltage source v_s serves as the power source of ESS. i_m is the output current of the source. i_{out} and v_{out} are the output current and output voltage of the bi-DC converter. $Z_s=R_s+sL_s$ is the input filter inductor of bi-DC converter and C_{out} is the output capacitor of bi-DC converter. i_{out_buck} and v_{out_buck} are the output current and output voltage of the buck converter. L_f and R_f are the output filter inductor of buck converter and its parasitic resistance. C_{in} is the input capacitor of buck converter and C_f is the output capacitor of buck converter.

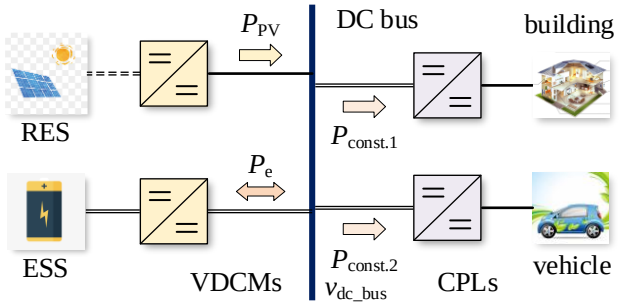


Figure 3.1: Topology of the studied DC-MG in islanded mode.

The state equation of the bi-DC converter and the steady-state operating point equation are shown in (3.1) and (3.2). When the loss of the switching network is neglected, the switching network in the bi-DC converter can be replaced by an ideal transformer. In this case, the switching cycle average model of bi-DC converter can be obtained in Figure 3.3(a). Based on (3.2), the ratio of the ideal transformer is d^*:1. The superscript "" represent the physical quantity of

the primary side derived to the secondary side. At this time, the simplified circuit can be obtained and shown in Figure 3.3(b) where $\Delta v'_s=(\Delta v_s+V_{out}\Delta d^*)/d^*$, $Z_s'=Z_s/d^{*2}$ and $\Delta i'_m=\Delta i_m d^*$. And d is the duty and $d^*=1-d$.

$$\begin{cases} L_s \dfrac{\mathrm{d}\Delta i_m}{\mathrm{d}t} = \Delta v_s - d^*\Delta v_{out} + V_{out}\Delta d^* - R_s\Delta i_m \\ C_{out} \dfrac{\mathrm{d}\Delta v_{out}}{\mathrm{d}t} = d^*\Delta i_m - I_{out}\Delta d^* - \Delta i_{out} \end{cases} \tag{3.1}$$

$$\begin{cases} L_s \dfrac{\mathrm{d}I_m}{\mathrm{d}t} = V_s - d^* V_{out} - R_s I_m \\ C_{out} \dfrac{\mathrm{d}V_{out}}{\mathrm{d}t} = d^* I_m - I_{out} \end{cases} \tag{3.2}$$

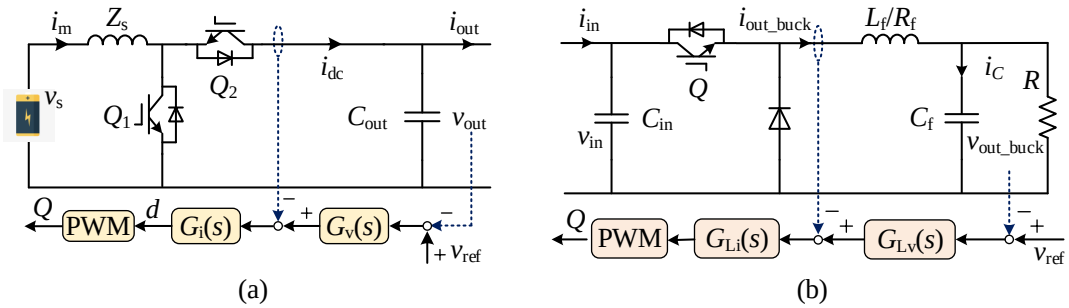


Figure 3.2: Circuit of DC converter. (a) bi-DC converter. (b) Buck converter.

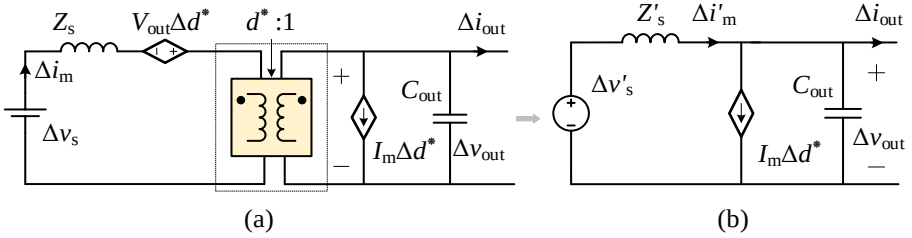


Figure 3.3: The simplified model of bi-DC converter (a) Switching cycle average model. (b) Simplified circuit of bi-DC converter.

Table 3.1 System parameters of the studied DC-MG

Subsystem	Parameters	Magnitude
Bidirectional DC converter	Input voltage v_s	100 V
	Input filter inductor L_s/R_s	5 mH/0.01 Ω
	Capacitance C_{out}	3000 μF
	Switching frequency	10 kHz
Buck converter	Load voltage v_{out_buck}	100 V
	Load power P_{const} (R)	2000 W(5Ω)
	Input capacitance C_{in}	1200 μF
	Filter inductor L_f/R_f	4 mH/0.01 Ω
	Output capacitance C_f	1000 μF
DC bus	DC bus voltage v_{dc_bus}	300 V
	DC bus capacitance C_{bus}	3000 μF
	Line impedance R_{line}/L_{line}	0.01 Ω/0.1 mH

3.2 Inertia Source in DC-MG and VIDC Strategy

3.2.1 Inertia source analysis in DC-MG

1) DC Machine: The DC machine model is shown in Figure 3.4(a). v_{f}, i_{f} and R_{f} are excitation voltage, excitation current, and field winding resistance, respectively. The equivalent circuit equation, torque balance equation and power balance equation are in (3.3) and (3.4). E, $R_{\mathrm{a\_m}}$, $i_{\mathrm{out\_m}}$ and $v_{\mathrm{out\_m}}$ are the internal potential, the winding resistance, the output current and the output voltage of the armature winding. D_{damp} and J_{dc} are damping coefficient and inertia coefficient. ω is the rotor speed and $\omega_{\mathrm{on\_m}}$ is its rated value. $C_{\mathrm{T\_m}}$ and φ_{m} are torque coefficient and magnetic flux. P_{m} and $P_{\mathrm{e\_m}}$ are mechanical power and electromagnetic power, respectively; and T_{m} and $T_{\mathrm{e\_m}}$ are mechanical torque and electromagnetic torque, respectively. v_{on} is the rated output voltage. It can be found in (3.4b) that when the DC machine is disturbed, rotor compensates the power difference by absorbing or releasing kinetic energy, suppressing the fluctuation of v_{out}.

$$\begin{cases} v_{\mathrm{out\_m}} = E - R_{\mathrm{a\_m}} i_{\mathrm{out\_m}} \\ E = C_{\mathrm{T\_m}} T_{\mathrm{e}} = C_{\mathrm{T\_m}} \varphi_m \omega \end{cases} \tag{3.3}$$

$$T_{\mathrm{m}} - T_{\mathrm{e\_m}} - D_{\mathrm{damp}}\left(\omega - \omega_{\mathrm{on\_m}}\right) = J_{\mathrm{dc}} \frac{\mathrm{d}\omega}{\mathrm{d}t} \tag{3.4a}$$

$$\begin{cases} P_{\mathrm{m}} - P_{\mathrm{e\_m}} - \dfrac{\omega_{\mathrm{on\_m}} D_{\mathrm{damp}}}{C_T \varphi}(E - v_{\mathrm{on}}) = \dfrac{\omega_{\mathrm{on\_m}} J_{\mathrm{dc}}}{C_T \varphi} \dfrac{\mathrm{d}(E - v_{\mathrm{on}})}{\mathrm{d}t} \\ P_{\mathrm{d}} = \dfrac{\omega_{\mathrm{on\_m}} D_{\mathrm{damp}}}{C_T \varphi}(E - v_{\mathrm{on}}) \\ P_{\mathrm{iner\_m}} = \dfrac{\omega_{\mathrm{on\_m}} J_{\mathrm{dc}}}{C_T \varphi} \dfrac{\mathrm{d}(E - v_{\mathrm{on}})}{\mathrm{d}t} \end{cases} \tag{3.4b}$$

$$P_{\mathrm{e\_m}} = \omega T_{\mathrm{e\_m}} \approx \omega_{\mathrm{on\_m}} T_{\mathrm{e\_m}} \tag{3.4c}$$

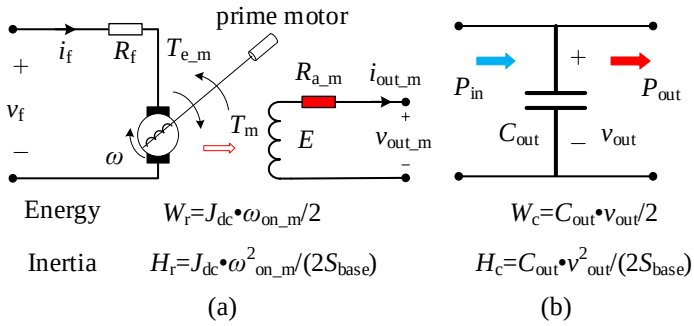


Figure 3.4: Inertia mapping between the DC machine and capacitor. (a) DC machine model. (b) DC capacitor.

2) DC Capacitor: The power balance at the DC capacitor is shown in Figure 3.4(b) and can be expressed in (3.5).

$$P_{\text{in}} - P_{\text{out}} = C_{\text{out}} v_{\text{out}} \frac{\mathrm{d}v_{\text{out}}}{\mathrm{d}t} \approx C_{\text{out}} V_{\text{dcn}} \frac{\mathrm{d}v_{\text{out}}}{\mathrm{d}t} \tag{3.5}$$

where P_{in} is the power output from the converter; P_{out} is the power injected into the DC-MG; v_{out} is the DC output voltage; V_{dcn} is the rated value of DC output voltage; C_{out} is the DC capacitor. When the DC-MG operates in a steady state, the DC voltage maintains constant, P_{in}=P_{out}. Suppose that P_{out} changes by ΔP_{out}, the unbalanced power will cause C_{out} to discharge or charge. When C_{out} is large enough, the change rate and deviation of v_{out} can be reduced. Limited by the actual capacity of C_{out}, the inertia of DC-MG is small, and the DC voltage might fluctuate drastically.

The inertia mapping between DC machine and DC capacitors is shown in Figure 3.4. The inertia constant of the DC machine H_{r} is defined as the ratio of the kinetic energy in the rotating masses ($J_{\text{dc}} \cdot \omega_{\text{on}}^2/2$) to its rated power S_{base}. Similarly, the inertia constant of the capacitor H_{c} can be defined as the ratio of the electrical energy stored in the capacitor ($C_{\text{out}} \cdot v_{\text{out}}^2/2$) to its rated power S_{base}.

3.2.2 VIDC concept model and its implementation

Considering the potential inertia supply ability of ESS, a VIDC strategy for bi-DC converter is proposed based on the voltage inertia characteristics of the DC machine and capacitors. The physical nature of this control is to properly regulate ESS to release or absorb energy in the same way as the rotors of DC machine and capacitors do, and connect a virtual resistance in series with the output port, then alleviate the DC bus voltage oscillation. By comparing (3.4) and (3.5), the control equation is shown in (3.6).

$$\begin{cases} P_{\text{vm}} - P_{\text{e}} - \dfrac{D_{\text{d}}\omega_{\text{on}}}{C_{\text{T}}\varphi}(v_{\text{vir}} - V_{\text{dcn}}) \approx \dfrac{\omega_{\text{on}} J_{\text{vir}}}{C_{\text{T}}\varphi} \dfrac{\mathrm{d}(v_{\text{vir}} - V_{\text{dcn}})}{\mathrm{d}t} \\ P_{\text{vd}} = \dfrac{D_{\text{d}}\omega_{\text{on}}}{C_{\text{T}}\varphi}(v_{\text{vir}} - V_{\text{dcn}}) \\ P_{\text{iner}} = \dfrac{\omega_{\text{on}} J_{\text{vir}}}{C_{\text{T}}\varphi} \dfrac{\mathrm{d}(v_{\text{vir}} - V_{\text{dcn}})}{\mathrm{d}t} = C_{\text{vir}} V_{\text{dcn}} \dfrac{\mathrm{d}(v_{\text{vir}} - V_{\text{dcn}})}{\mathrm{d}t} \end{cases} \tag{3.6a}$$

$$P_{\text{e}} = \omega_{\text{vir}} T_{\text{e}} = i_{\text{out}} v_{\text{out}} \tag{3.6b}$$

$$\begin{cases} v_{\text{out}} = v_{\text{vir}} - R_{\text{a}} i_{\text{out}} \\ v_{\text{vir}} = C_{\text{T}}\varphi\omega_{\text{vir}} \end{cases} \tag{3.6c}$$

where V_{dcn} is the rated output voltage of bi-DC converter. P_{vm} is the input power of converter, which includes P_{vd} (the virtual damping power), P_{e} (the output electromagnetic power) and P_{iner}

(the virtual inertia power). J_{vir} is the introduced inertia coefficient of VIDC and C_{vir} is the equivalent virtual capacitor. D_d is the virtual damping coefficient. v_{vir} is the virtual internal potential in the VIDC strategy, emulating E of DC machine. R_a is a virtual resistance. The physical significance of (3.6) is to transform the relationship between the torque balance and ω_{vir} into the relationship between the power balance and v_{vir}, and it also reflects the inertia and damping characteristics of the bi-DC converter. When there exists power mismatch, the virtual (static) rotor C_{vir} can suppress the voltage oscillation by absorbing or releasing power. The damping power P_{vd} is provided until the power balance is achieved again. The VIDC concept model could be derived in Figure 3.5(a).

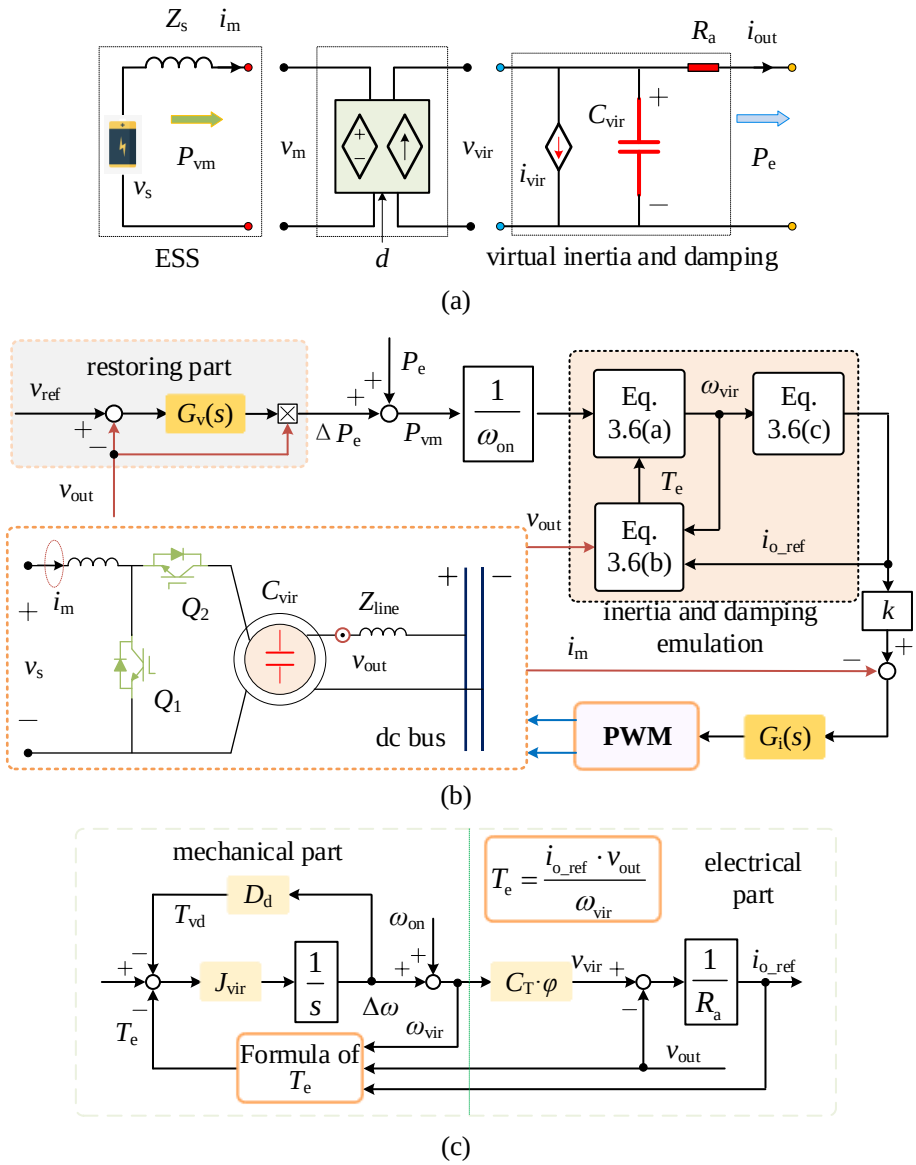


Figure 3.5: Concept model and block diagram of VIDC strategy. (a) Concept model. (b) Control block diagram. (c) Virtual inertia and damping emulation part.

Based on the VIDC concept model in Figure 3.5(a), the analogy between DC machine and the bi-DC converter control system is shown in Table 3.2. The energy of the DC machine is provided by the prime mover, while the inertia power and the damping power of the bi-DC converter come from ESS, and the input filter imitate the excitation winding. The introduction of virtual inertia J_{vir} is equivalent to connecting a virtual capacitor C_{vir} in parallel on the converter output side, which is regarded as the virtual (static) rotor of the bi-DC converter, providing inertia of smoothing voltage fluctuation. R_a is an adjustable parameter that mimics armature winding resistance (the loss of the switching network). D_d is equivalent to a controlled current source i_{vir}, simulating the friction effect. When the voltage rises, the virtual damping current source i_{vir} absorbs the surplus power, and vice versa. Besides, bi-DC converters controlled by VIDC can operate in generator or motor mode, as DC machine can do.

Table 3.2 Analogy between DC machine and VIDC

Physical meaning	DC Machine	Proposed VDCM
Mechanical power	Primary motor	ESS
Moment of inertia	Rotor (J_{dc})	C_{vir} (J_{vir})
Damping source	The friction (D_{damp})	i_{vir} (D_d)
Armature winding	R_{a_m}	R_a
Excitation winding	R_f	R_s
Angular velocity	ω	ω_{vir}
Output voltage	v_{out_m}	v_{out}
Excitation constant	$C_{T\_m}\cdot\varphi_m$	$C_T\cdot\varphi$

Virtual DC machine control has been proposed in [88] to operate bi-DC converter of ESS as DC machine to achieve rotor inertia emulation and regulate the DC bus voltage fluctuations. However, the controller structure and parameters design are complicated and the multi-parallel operation is not analyzed. Besides, the output of the inertia loop is the output voltage, which impact the static characteristic. Different from [88], the rated value of output voltage is added into the VIDC, thus, it only acts in the transient process with a better control performance, the static characteristic (i.e. voltage regulation and power sharing) would not be affected.

The diagram of the VIDC strategy for bi-DC converter is shown in Figure 3.5(b), including restoring part (voltage outer loop, $G_v(s)=k_{vp}+k_{vi}/s$), current inner loop ($G_i(s)=k_{ip}+k_{ii}/s$), and inertia and damping emulation part which includes mechanical part (Eq. 3.6(a-b)) and electrical part (Eq. 3.6(c)).

Voltage restoring part: The objective of restoration controller is to restore v_{out} to its reference value v_{ref}. In the restoring part, a PI controller $G_v(s)$ is adopted to generate deviation power ΔP_e using the error defined between v_{out} and v_{ref}. Due to $G_v(s)$, v_{out} would always track its reference

value v_{ref}, which means the steady-state error can be eliminated, achieving the voltage restoration. The summation of ΔP_e and the feedback power P_e form P_{vm}, i.e. the input signal for VIDC.

VIDC loop: As shown in Figure 3.5(c), the VIDC loop consists of two parts: the virtual inertia control loop (mechanical part) and the armature winding emulation part (electrical part). ***(1)*** In the mechanical part, the virtual speed ω_{vir} of the (static) rotor C_{vir} is controlled according to the power balance equation, achieving the inertia and damping emulation. And its output is the virtual speed ω_{vir}, i.e. the input signal for the electrical part. ***(2)*** In the electrical part, the virtual internal potential v_{vir} is derived and then the output current reference value i_{o_ref} is obtained according to the armature winding circuit equation. $k=V_{dcn}/V_s$ is introduced to achieve the conversion between output current and input current i_{m_ref} (namely, the reference value of the current inner loop).

***Current inner loop*:** The objective of current inner loop is to restore i_m to its reference value i_{m_ref}. In this part, a PI controller $G_i(s)$ is adopted to generate the duty ratio, using the error defined between i_m and i_{m_ref}. Due to the existence of $G_i(s)$, the actual value of i_m would always track its reference value i_{m_ref}, which means the steady-state error of current can be eliminated and the output voltage can be controlled indirectly.

The control system dynamic response is affected by J_{vir} and D_d which provide extra freedom degrees. The VIDC loop is equivalent to connect an adjustable capacitor and controlled current source in parallel at the output side of the converter, and R_a is a virtual resistance in series with the output port. Assuming that P_{vm} changes by ΔP_{vm}, the unbalanced power will be compensated by three parts:

$$\Delta P_{vm} = \Delta P_{vd} + \Delta P_{iner} + C_{out} V_{dcn} \frac{dv_{out}}{dt} \tag{3.7}$$

As can be seen from (3.7), ΔP_{vm} can be balanced by ΔP_{vd}, ΔP_{iner} and the power from capacitor C_{out}. Since ΔP_{vd} and ΔP_{iner}, which is from ESS, are able to take on most unbalanced power, the power from C_{out} will be reduced, i.e. for the same ΔP_{vm}, the change rate and deviation of the v_{out} can be reduced, and the inertia and damping of DC-MG are improved.

3.2.3 Droop control for multi-parallel operation

To achieve multi-parallel operation of bi-DC converters, droop control is added in outer loop, as shown in in Figure 3.6(a) and (b). v_{max}, v_{min}, i_{m_max}, and i_{m_min} are the maximum and minimum values of v_{out}, the maximum discharge current and the maximum charge current of ESS, respectively. And R_d is the droop coefficient. The *V-I* droop control equation is shown in (3.8). Current

sharing between bi-DC converters is inversely proportional to R_d. As shown in Figure 3.6(c), due to the imbalance in the voltage drop across the line resistance, a circulating current would form between the bi-DC converters, which affects the even power sharing. Circulating current Δi_{cir} can be calculated by (3.9). This chapter focuses on the problem of voltage fluctuations, and the suppression method of circulating current is not discussed in detail.

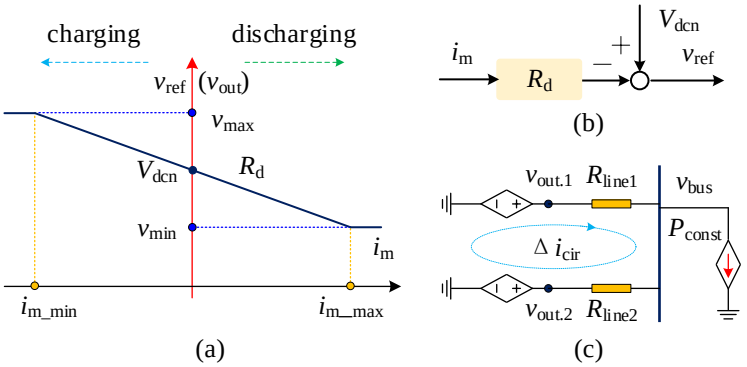


Figure 3.6: Droop control and circulating current analysis. (a) Concept model. (b) Control block diagram (c) Equivalent circuit.

$$v_{out} = v_{ref} = V_{dcn} - R_d i_m \tag{3.8}$$

$$\Delta i_{cir} = \frac{R_{line2} - R_{line1}{}^{R_{d2}}/_{R_{d1}}}{R_{line1} + R_{line2}} i_{out2} \tag{3.9}$$

3.3 Small Signal Model and Dynamic Characteristic Analysis of the VIDC Strategy

To study the relationship between v_{out} and power demand, the small signal model of the bi-DC converter is established. Neglecting the energy loss, there is:

$$v_m i_m = v_{out}\left(i_{out} + C_{out}\frac{dv_{out}}{dt}\right) \tag{3.10}$$

The relation between Δi_m and Δi_{out} is expressed as:

$$\frac{\Delta i_{out}(s)}{\Delta i_m(s)} = \frac{V_s}{V_{dcn}} = A_i(s) \tag{3.11}$$

From (3.6b), the small signal model of ΔT_e is obtained:

$$\Delta T_e = \frac{I_{out}}{\omega_{on}}\Delta v_{out} + \frac{V_{out}}{\omega_{on}}\Delta i_{out} - \frac{V_{out} I_{out}}{\omega_{on}^2}\Delta\omega \tag{3.12}$$

Based on (3.10), (3.11), (3.12) and Figure 3.5, the small signal model of the bi-DC converter control system can be obtained, as shown in Figure 3.7. K_{pwm} is the equivalent gain of pulse width modulator (PWM). Δi_{out} affects Δv_{out} through three loops. The transfer function of Δv_{out}

and Δi_{out} can be split into three parts:

$$TF(s)=\frac{\Delta v_{\mathrm{out}}}{\Delta i_{\mathrm{out}}}=TF_{\mathrm{lp1}}(s)+TF_{\mathrm{lp2}}(s)+TF_{\mathrm{lp3}}(s) \tag{3.13}$$

The transfer functions of these three loops are derived as:

$$TF_{\mathrm{lp1}}(s)=\frac{V_{\mathrm{dcn}}k\cdot C_{\mathrm{T}}\varphi\cdot T_{\mathrm{iv}}(s)\cdot T_{\mathrm{vi}}(s)}{\omega_{\mathrm{on}}\left(R_{\mathrm{a}}+k\cdot H_{\mathrm{vir}}-k\cdot C_{\mathrm{T}}\varphi\cdot T_{\mathrm{iv}}(s)T_{\mathrm{vi}}(s)\right)}=-TF_{\mathrm{lp2}}(s) \tag{3.14a}$$

$$TF_{\mathrm{lp3}}(s)=\frac{\Delta v_{\mathrm{out}}}{\Delta i_{\mathrm{out3}}}=-\frac{T_{\mathrm{vi}}(s)A_{\mathrm{i}}(s)}{1-T_{\mathrm{iv}}(s)\cdot T_{\mathrm{vi}}(s)} \tag{3.14b}$$

where $T_{\mathrm{vi}}(s)$, $T_{\mathrm{iv}}(s)$ $G_{\mathrm{vd}}(s)$, $G_{\mathrm{isd}}(s)$ and $H_{\mathrm{vir}}(s)$ are in (3.15) and (3.16). The influences of Δi_{out1} and Δi_{out2} on the Δv_{out} can cancel each other out as shown in (3.14a). Thus, $TF(s)$=$TF_{\mathrm{lp3}}(s)$. The physical significance of $TF(s)$ is to reflect how v_{out} will change when the output current i_{out} suddenly increases or decreases. As is known to all, i_{out} is relevant to the power demand of the DC-MG and decided by the power consumption of the loads and the output power of RES and ESS.

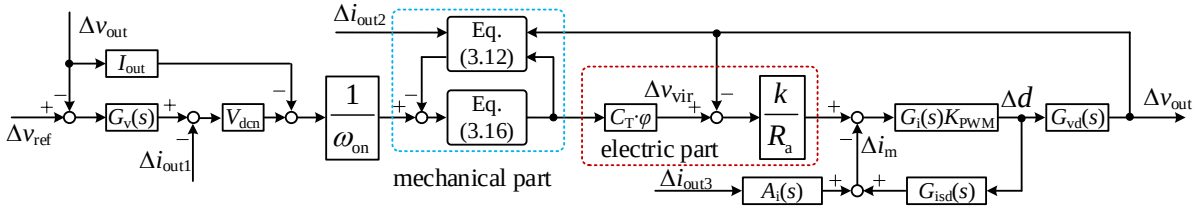


Figure 3.7: Small signal model of the bi-DC converter control system.

$$G_{\mathrm{vd}}(s)=\left.\frac{\Delta v_{\mathrm{out}}}{\Delta d}\right|_{\Delta v_{\mathrm{s}}=0,\Delta i_{\mathrm{out}}=0}=\frac{-i_{\mathrm{m}}(R_{\mathrm{s}}+sL_{\mathrm{s}})+(1-d)v_{\mathrm{out}}}{s^2L_{\mathrm{s}}C_{\mathrm{out}}+sR_{\mathrm{s}}C_{\mathrm{out}}+(1-d)^2} \tag{3.15a}$$

$$G_{\mathrm{isd}}(s)=\left.\frac{\Delta i_{\mathrm{m}}}{\Delta d}\right|_{\Delta v_{\mathrm{s}}=0,\Delta i_{\mathrm{out}}=0}=\frac{sC_{\mathrm{out}}v_{\mathrm{out}}+(1-d)i_{\mathrm{m}}}{s^2L_{\mathrm{s}}C_{\mathrm{out}}+sR_{\mathrm{s}}C_{\mathrm{out}}+(1-d)^2} \tag{3.15b}$$

$$\begin{cases}T_{\mathrm{vi}}(s)=-(T_{\mathrm{vT}}(s)\cdot T_{\mathrm{v\omega}}(s)-1)\dfrac{k}{R_{\mathrm{a}}}\\ T_{\mathrm{vT}}(s)=-\dfrac{2I_{\mathrm{out}}+V_{\mathrm{dcn}}G_{\mathrm{v}}(s)}{\omega_{\mathrm{on}}}\\ T_{\mathrm{v\omega}}(s)=\dfrac{\omega_{\mathrm{on}}^2H_{\mathrm{vir}}(s)}{\omega_{\mathrm{on}}^2+H_{\mathrm{vir}}(s)I_{\mathrm{out}}V_{\mathrm{dcn}}}\end{cases} \tag{3.15c}$$

$$T_{\mathrm{iv}}(s)=\frac{G_{\mathrm{i}}(s)G_{\mathrm{vd}}(s)}{V_{\mathrm{dcn}}+G_{\mathrm{i}}(s)G_{\mathrm{isd}}(s)} \tag{3.15d}$$

$$H_{\mathrm{vir}}(s)=\frac{1}{s/J_{\mathrm{vir}}+D_{\mathrm{d}}} \tag{3.16}$$

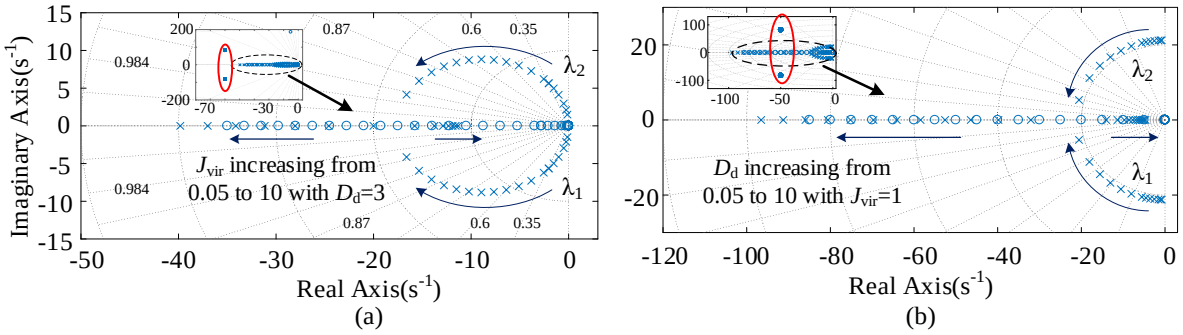


Figure 3.8: Zero and dominant poles distribution of $TF(s)$. (a) Arrow direction: J_{vir} changing from 0.05 to 10. (b) Arrow direction: D_d changing from 0.05 to 10.

Figure 3.8 shows the zeros and dominant poles distribution of $TF(s)$. The symbol "×" represent poles. The symbol "○" represents zero. It can be observed that the pair of poles in the red circle are far away from the point (0, 0) in Figure 3.8 and almost stay constant when J_{vir} or D_d changes. Besides, there is a pair of zeros near this pair of poles, which constitutes dipoles with this pair of poles and neutralizes the influence of this pair of poles. Hence, their influence can be neglected. In Figure 3.8(a), the oscillation frequency firstly increases and then decreases with J_{vir} increasing. When J_{vir}=6, the system becomes overdamped. After that, the dominant poles become two negative real roots. One pole gradually moves away from the imaginary axis, and the other one moves toward the imaginary axis but will not cross the imaginary axis, becoming the only dominant pole. The time constant and the system inertia increase with J_{vir} increasing. The same trend with D_d increasing can be observed in Figure 3.8(b). There is only one pair of dominant poles, which means the high-order system can be estimated by the performance indices of a 2nd-order system.

3.4 Parameter Design

3.4.1 Design of voltage outer loop and current inner loop

With a large control bandwidth, the current loop provides fast tracking performance of i_{out}. The voltage loop ensures accurate reference tracking, with a much slower dynamic response than the current loop. Small signal models of current loop and voltage loop are in Figure 3.9(a) and Figure 3.9(b), respectively. The cut-off frequency of the current loop f_{cc} should be no greater than one-tenth of the switching frequency f_s. Considering K_{PWM}=1, there is:

$$\left|G_i(s)K_{pwm}G_{isd}(s)\right| = 1 \tag{3.17}$$

The bode diagram of current loop is shown in Figure 3.9(c). k_{ip} is chosen as 5 with f_{cc}=636.9Hz and phase margin (PM)=91.1°.

As for the voltage loop, the cut-off frequency f_{cv} should be no greater than one-tenth of f_{cc} to mitigate the coupling between voltage loop and current loop. The phase margin (PM) is designed to be no smaller than $\pi/4$. Since the bandwidth of the voltage loop is much lower than the current loop, the current loop could be simplified to K_c=1 while designing voltage loop. $H_c(s)$ is the sampling loop and equivalent to 1. Then there is:

$$|H_c(s)G_v(s)K_cH_{out}(s)|_{s=j2\pi f_{cv}} = 1 \tag{3.18a}$$

$$\angle H_c(s)G_v(s)K_cH_{out}(s)|_{s=j2\pi f_{cv}} \geq -\frac{3}{4} \tag{3.18b}$$

$$H_{out}(s) = \frac{\Delta v_{out}}{-\Delta i_{out}}\Big|_{\Delta v_s=0,\Delta d=0} = \frac{R_s + sL_s}{s^2L_sC_{out} + sR_sC_{out} + (1-d)^2} \tag{3.18c}$$

H_{out}(s) is the open loop output impedance of bi-DC converter.

The bode diagram of the voltage loop is shown in Figure 3.9(d). k_{vp} and k_{vi} are chosen as k_{vp} =0.3, k_{vi}=50 with f_{cv}=52.7Hz and phase margin (PM)=66.4º.

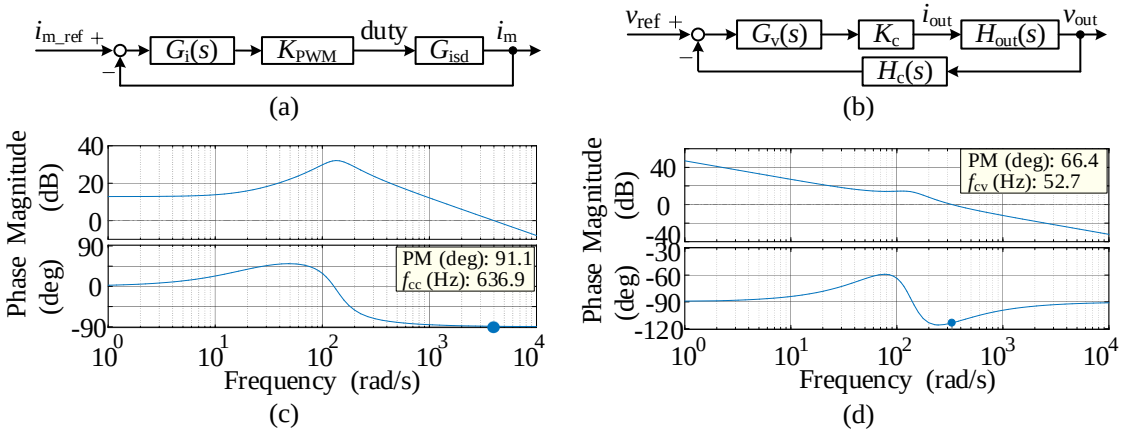


Figure 3.9: Small signal model and Bode diagram. (a) Small signal model of current loop. (b) Small signal model of voltage loop. (c) Bode diagram of current loop. (d) Bode diagram of voltage loop.

3.4.2 Parameters design of VIDC

The rated output voltage V_{dcn} is 300V, the rated current I_{on} is 20A, and the virtual internal potential v_{vir}=325V. The virtual resistance R_a=(v_{vir}-V_{dcn})/I_{on}=1.25Ω. ω_{on} is chosen as 314rad/s, then $C_T \cdot \varphi$ is chosen as 0.955. J_{vir} and D_d are selected according to the requirements of the dynamic characteristic.

When the VIDC regulator is designed, the unity gain block represents the closed-loop gain of current loop with the large bandwidth. The voltage loop with a small bandwidth has slow dynamic response and cannot be ignored. To simplify the parameter design process, a simplified

model of the proposed VIDC strategy is proposed in Figure 3.10. The detailed transfer functions $T_d(s)$ can be obtained in (3.19) which is a 2nd-order system. $k_1=I_{out}V_{dcn}/\omega_{on}$, $k_2=V_{dcn}/(\omega_{on}R_{load})$ and $k_3=V_{dcn}/\omega_{on}$, $g=R_{load}/(R_{load}-R_a)$ and $K= C_T\cdot\varphi$. Its physical meaning is to reflect dynamic characteristic of v_{out} when i_{out} changes suddenly. Thus, several important performance indices in 2nd-order system for can be used to evaluate dynamic.

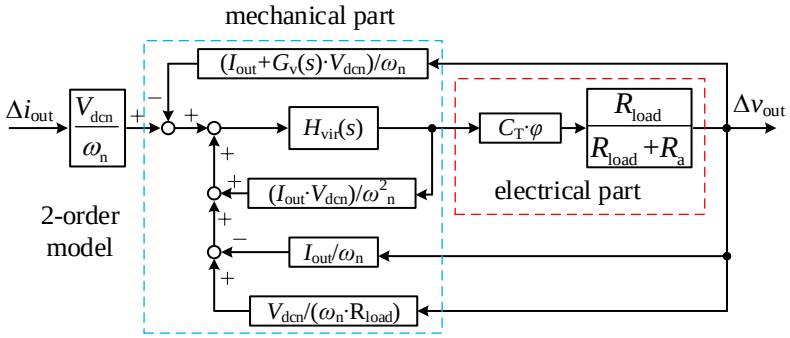


Figure 3.10: Simplified 2nd-order model of the bi-DC converter control system

$$T_d(s)=\frac{\Delta v_{out}}{\Delta i_{out}}=\frac{k_3\cdot g\cdot K\cdot\omega_{on}\cdot s}{\omega_{on}/J_{vir}\,s^2+\left[(D_d+k_1)\omega_{on}+g\cdot K\left(k_2\omega_{on}+2I_{out}+V_{dcn}k_{vp}\right)\right]s+gKV_{dcn}k_{vi}} \tag{3.19}$$

Based on (3.19), damping ratio ξ and the natural oscillation frequency ω_n of the system can be derived as (3.20).

$$\omega_n=\sqrt{\frac{J_{vir}gKV_{dcn}k_{vi}}{\omega_{on}}} \tag{3.20a}$$

$$\xi=\frac{J_{vir}(D_d+k_1)\omega_{on}+gK(k_2\omega_{on}+2I_{out}+V_{dcn}k_{vp})}{\omega_{on}} \tag{3.20b}$$

The voltage response may also be evaluated by the overshoot σ, which can be derived as shown in (3.21).

$$\sigma=\exp(-\frac{\pi\xi}{\sqrt{1-\xi^2}}) \tag{3.21}$$

Additionally, the settling time t_s (time for entering the 2% quasi-steady-state error band) is normally used to evaluate the dynamics of voltage regulation, which can be derived as (3.22).

$$t_s=\begin{cases}\dfrac{4}{\xi\omega_n}, & \xi<1\\ -\dfrac{3}{\mathrm{real}(\lambda_2)}, & \xi>1\end{cases} \tag{3.22}$$

Based on (3.20)−(3.22), the relationships between various performance indices and control parameters (J_{vir} and D_d) are demonstrated in Figure 3.11. In Figure 3.11(a), the increasing of D_d leads to damping ratio increasing. When in overdamped state, the system can be equivalent to

the 1st-order system, meanwhile the system inertia increases gradually with the J_{vir} increasing, In Figure 3.11(b), ω_n is mainly related to the parameter J_{vir}, and gradually increases with J_{vir} increasing. This can be used to guide the designer in how to avoid voltage resonance. In Figure 3.11(c), voltage overshoot σ can well be attenuated by a large value of D_d or J_{vir}. Although being effective in attenuating the voltage overshoot and oscillation, high system inertia will inevitably slow down the dynamics of voltage regulation and extend the voltage restoration process when in overdamped state, as evidenced by Figure 3.11(d). Theoretically, D_d and J_{vir} should be designed according to the comprehensive requirements of the performance indices in (3.20)–(3.22).

The detailed design of the J_{vir} and D_d is illustrated by examples as shown in Figure 3.12.

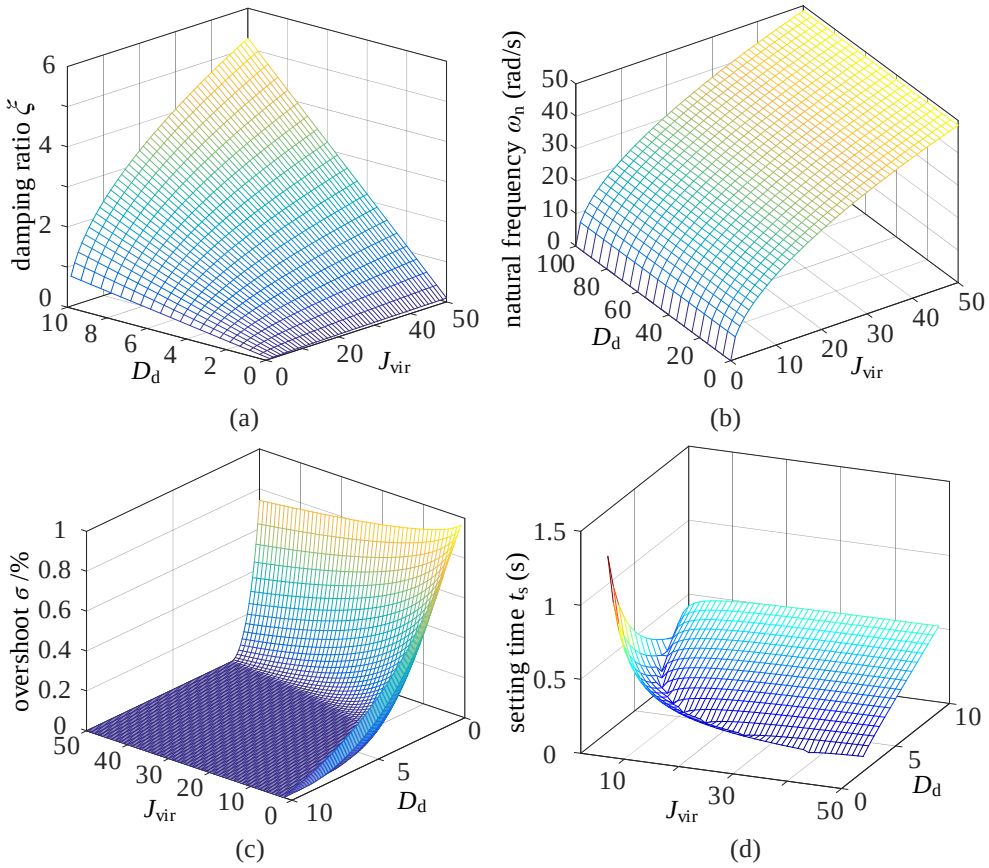


Figure 3.11: Variation range of different performance indices. (a) Damping ratio ξ. (b) Natural oscillation frequency. (c) Overshoot. (d) Setting time.

Case I: When a certain dynamic index is needed to meet some requirements preferentially, the corresponding values of J_{vir} and D_d can be directly obtained according to Figure 3.12(a-c). (***a***) When the damping ratio ξ is required to be over 0.7343. The corresponding parameter set is the green region in Figure 3.12(a). (***b***) When the setting time t_s is required to be less than 0.1s. The corresponding parameter set is the green region in Figure 3.12(b). (***c***) When the overshoot σ is

required to be less than 10%. The corresponding parameter set is the green region in Figure 3.12(c). For the above situations, parameters satisfying these conditions can be obtained from corresponding sets, respectively.

Table 3.3 Control parameters of VIDC strategy

Parameters	Values	Parameters	Values
v_{max}	310 V	v_{min}	290 V
i_{m_max}	40 A	i_{m_min}	-40 A
V_{dcn}	300 V	k_{vp}	0.3
$C_T \cdot \varphi$	0.955	k_{vi}	50
J_{vir}	10	k_{ip}	5.0
D_d	3	R_d	0.5
Switch frequency	10 kHz	Sampling frequency	10 kHz

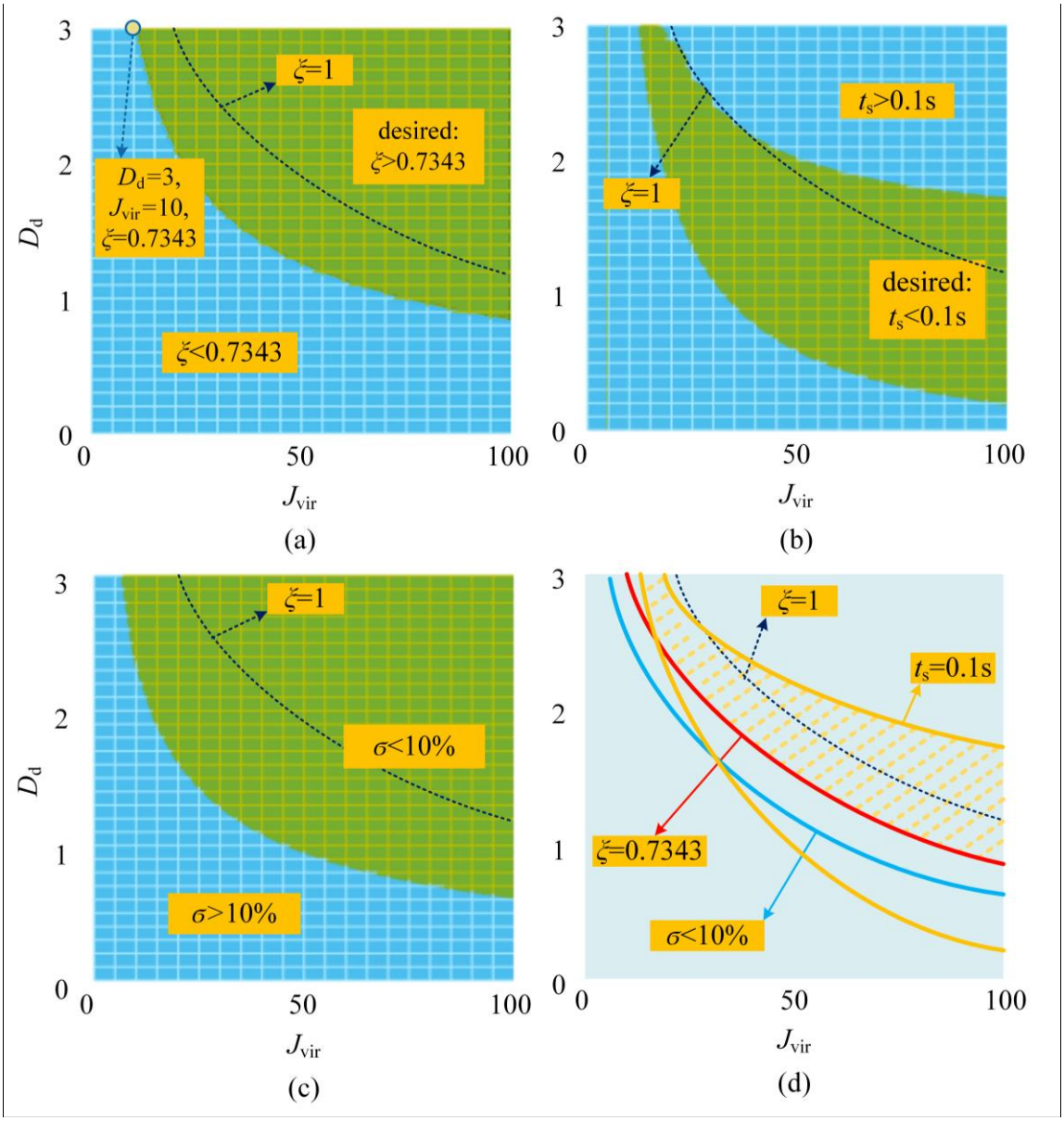


Figure 3.12: Parameters design when performance indices with different requirements. (a) Damping ratio ξ. (b) Setting time t_s. (c) Overshoot σ. (d) Intersection of solutions with different requirements.

Case II: When the three performance indices are required to meet some certain requirements at the same time, the parameters can be obtained from the intersection of their respective solutions. For example, when ξ>0.7343, t_s>0.1s and σ<10% are required at the same time, the solution is the intersection of the green regions in Figure 3.12(a-c), i.e. the shadow region in Figure 3.12(d).

According to (3.20b), when ξ is required to be 0.7343, J_{vir} could be 10 and D_d could be 3 as shown in Figure 3.12(a). The control parameters are shown in Table 3.3.

3.4.3 Inertia matching method

This section will focus on matching the inertia parameter to make the voltage transition process of multi-parallel bi-DC converters consistent and improve their transient stability. Then equation (3.6) will be simplified to:

$$P_{\mathrm{vm}} - P_{\mathrm{e}} \approx \frac{\omega_{\mathrm{on}} J_{\mathrm{vir}}}{C_{\mathrm{T}}\varphi}\frac{\mathrm{d}v_{\mathrm{out}}}{\mathrm{d}t} \tag{3.23}$$

It is assumed that the bi-DC converter operates at the steady-state operating point S_1 before the disturbance occurs, as shown in equation (3.24). After the disturbance occurs, it operates at the steady-state operating point S_2 as shown in equation (3.25). When the system reaches steady state, P_{m1}=P_{e1} and P_{m2}=P_{e2}.

$$P_{\mathrm{m1}} - P_{\mathrm{e1}} \approx \frac{\omega_{\mathrm{on}} J_{\mathrm{vir}}}{C_{\mathrm{T}}\varphi}\frac{\mathrm{d}v_{\mathrm{out}}}{\mathrm{d}t} \quad S_1 \tag{3.24}$$

$$P_{\mathrm{m2}} - P_{\mathrm{e2}} \approx \frac{\omega_{\mathrm{on}} J_{\mathrm{vir}}}{C_{\mathrm{T}}\varphi}\frac{\mathrm{d}v_{\mathrm{out}}}{\mathrm{d}t} \quad S_2 \tag{3.25}$$

According to the droop control principle, when disturbances occur, output power changes from P_{e1} to P_{e2}, and the operating point moves from S_1 to S_2. Inertia configuration principle is obtained, as shown in (3.26). When the disturbance causes voltage fluctuation in DC-MG with multi-parallel bi-DC converters, each inertia parameter must be configured in inverse proportion to the droop factor to obtain the same transition time Δt during the same voltage fluctuation.

$$\frac{\omega_{\mathrm{on}} J_{\mathrm{vir}}}{C_{\mathrm{T}}\varphi}\frac{\mathrm{d}v_{\mathrm{out}}}{\mathrm{d}t} \approx \frac{\omega_{\mathrm{on}} J_{\mathrm{vir}}}{C_{\mathrm{T}}\varphi}\frac{\Delta v_{\mathrm{out}}}{\Delta t} = P_{\mathrm{m1}} - P_{\mathrm{e1}} = -\Delta P \tag{3.26}$$

3.5 Simulation Verification

To test the proposed VIDC strategy, an islanded DC-MG system is modelled in MATLAB, as shown in Figure 3.1. The parameters are in Table 3.3.

3.5.1 Comparison between different control methods

The VIDC strategy is compared with V^2-P-based virtual inertia control (VIC) [74] shown in Figure 3.13 and dual loop control shown in Figure 3.2. Control parameters for dual loop control and V^2-P-based VIC can be obtained from Table 3.4. When t=1.5s, P_{const} increases 500W suddenly and when t=3s, P_{const} decreases 500W. The simulation results are shown in Figure 3.14. When power disturbance occurs, the v_{out} is prone to oscillation with the droop control. In contrast, the DC voltage oscillation is effectively suppressed, when V^2-P-based virtual inertia control or VIDC strategy is utilized, and DC voltage is stabilized within the shortest time when VIDC strategy works. In addition, compared with the V^2-P-based VIC, VIDC strategy has two degrees of freedom (J_{vir} and D_d) to adjust dynamic processes, while V^2-P-based the virtual inertia control only has one control variable C_{vir} affecting the dynamic process.

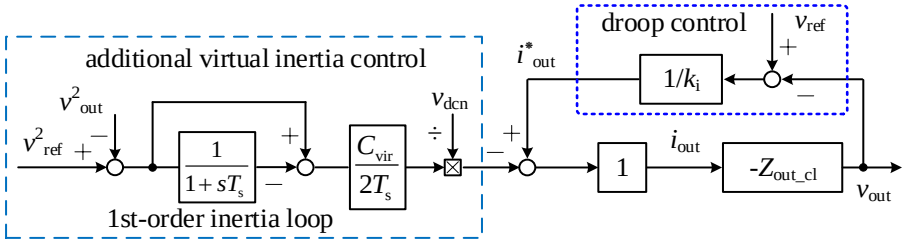


Figure 3.13: Block diagram of V^2-P-based VIC.

Table 3.4 Control parameters of dual loopcontrol and V^2-P-based VIC

Control strategy	Parameters		Magnitude
Dual loop control	Droop coefficient k_i		0.01
	voltage loop	Proportional gain k_{vp}	0.2
		Integral gain k_{vi}	0.02
	current loop	Proportional gain k_{ip}	5
		Integral gain k_{ii}	5
V^2-P-based virtual inertia control	Droop coefficient k_i		2
	Sampling period T_s		10e-4 s
	Virtual capacitance C_{vir}		2 F
	current loop	Proportional gain k_{ip}	0.1
		Integral gain k_{ii}	10

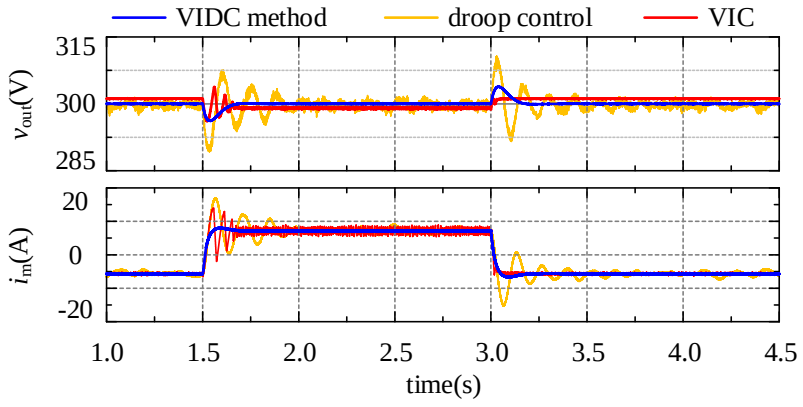


Figure 3.14: Comparison of different control strategies

3.5.2 Stand-alone operation mode of bi-DC converter

Figure 3.15 are the simulation results of DC voltage oscillation caused by power disturbance on RES side and CPL side, respectively. In Figure 3.15(a), When t=1.5s, the output power of RES P_{pv} decreases 300W suddenly, and when t=3s P_{pv} increases 300W. In Figure 3.15(b), When t=1.5s, the power demand of CPL P_{const} increases 500W suddenly, and when t=3s, P_{const} decreases 500W. When D_d and J_{vir} are set as a small value, v_{out} will stabilize after a period of oscillation, indicating system inertia enhancement and damping improvement by the VIDC strategy is not obvious. The oscillation is well damped with a good dynamic response when D_d or J_{vir} is increased.

The converter system is a strongly nonlinear system. Therefore, there are the case where the control parameters need to be changed within a large range to obtain different control effects, and the case where the control effects change greatly when control parameters change with a small interval. Besides, it is proved that the bi-DC converter control system can still maintain stability even if the parameter changes in a large range.

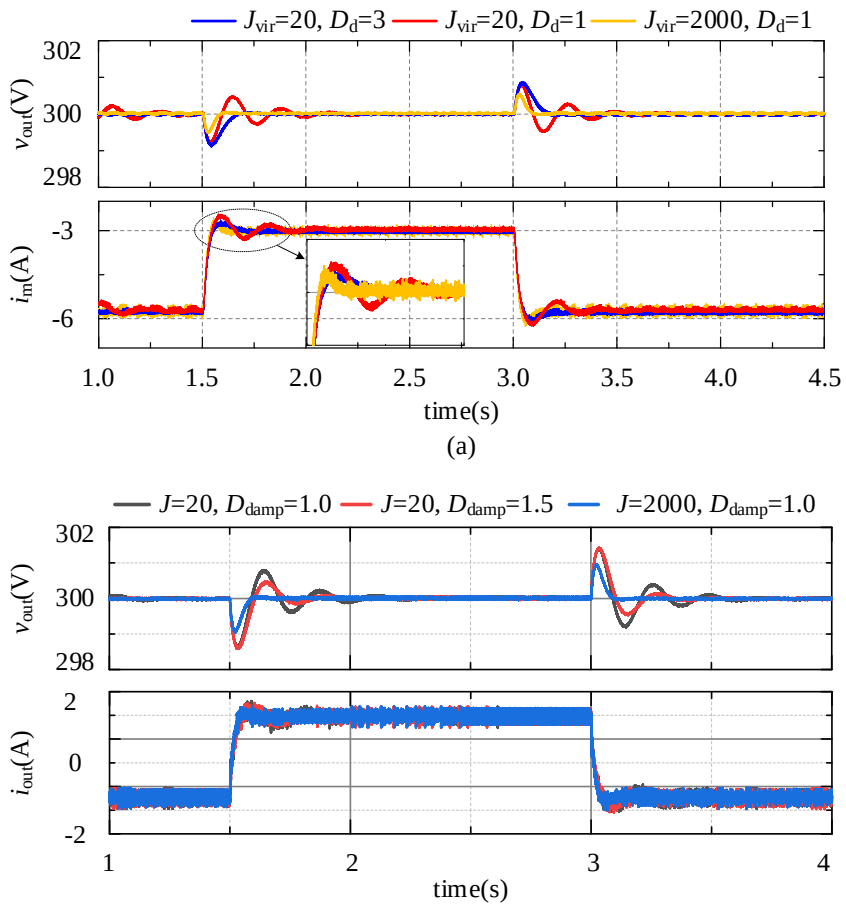


Figure 3.15: The simulation results during sudden power change. (a) RES. (b) CPL.

3.5.3 Multi-parallel operation of bi-DC converters

In order to verify the effectiveness of the proposed inertia matching method, simulation analysis is performed for parallel systems with the same capacity and different capacities. P_{const} increases by 500W at 1.5 s and decreases by 500W at 3.0 s. The simulation results are shown in Figure 3.16. In Figure 3.16(a), R_d and J_{vir} are selected in a 1:1 ratio, the load is evenly shared between the bi-DC converters, and the output voltage transition process remains synchronized. Figure 3.16(b) shows the case where the load is shared between bi-DC converters in a ratio of 1:2. R_d should be selected according to the ratio of 2:1. At the same time, in order to ensure the synchronization of the output voltage transition process, J_{vir} should be selected according to the ratio of 2:1.

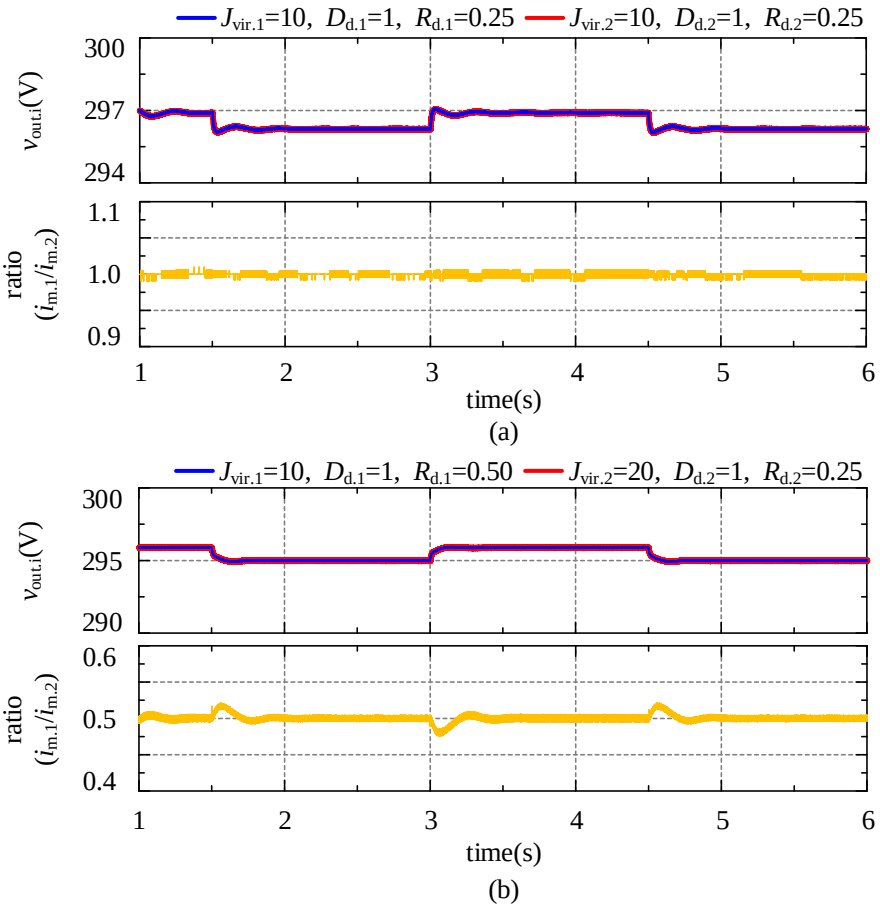


Figure 3.16: The simulation results of parallel operation. (a) Converters with equal capacity. (b) Converters with unequal capacity.

3.6 Summary

In this chapter, a VIDC strategy for bi-DC converters is proposed and its essence is connecting a virtual capacitor and a controlled current source in parallel, and a virtual resistance in series

on the output side of bi-DC converters, which makes the external characteristics of bi-DC converter consistent with the dynamic characteristics of DC machine. Virtual inertia power and damping power are provided by the ESS without increasing system cost and complexity. Combined with droop control, multi-parallel operation of bi-DC converters can be realized. When using zero-pole distribution to analyze the dynamic performance of the VIDC strategy, it is found that the bi-DC converter control system can be equivalent to a 2nd-order model which simplifies the parameter design. Thus, appropriate control parameters can be selected according to the requirements for performance indices, such as damping ratio, overshoot and/or setting time, in 2nd-order systems. Based on the inertia matching method, J_{vir} should be configured according to the capacity ratio to ensure that the output voltage remains synchronized during transient processes. Simulation results show the proposed strategy provides satisfactory inertia and damping effects in islanded DC-MG.

Future work will concentrate on the adaptability of control parameters in a wide range of working conditions and parameter optimization design methods will be studied. The method of suppressing circulating currents caused by line resistances will also be focused on.

4 Inertia Droop Control and its Stability Mechanism Analysis for Energy Storage System in Islanded DC-MG

Although virtual inertia and damping control (VIDC) has been developed in Chapter 3 to deal with the instability issue of an islanded DC microgrid (DC-MG), the extra inertia and damping loops complicate the control system and the voltage deviation caused by droop coeffcient still remains unsolved. Besides, a unified stability mechanism for various VIDC has not been discussed. In order to solve these issues, inertia droop control (IDC) strategies are proposed in this chapter based on the equivalent models of VIDC, to mitigate low-frequency oscillations (LFO), suppress the rate of change of voltage (RoCoV) and remove voltage deviations in islanded DC-MG. A phasor-diagram-based feedback analysis approach is developed to unify the mechanism analysis of IDC and VIDC in an analytic way. The principle of inertia and damping provision, performance evaluation, stability analysis, parameter selection, and a hardware in the loop (HIL) experiment are presented. Accordingly, the stability mechanism becomes clear and the dynamic stability of islanded DC-MG is improved. Under the premise of realizing the same control function as VIDC, the proposed IDC methods omit the inertia loop and simplify the control structure, without adding any auxiliary controller/observer.

The content of this chapter has been published in "*IEEE transaction on transportation electrification*" [M3].

4.1 DC-MG Structure and Discussion about VIDC

4.1.1 System configuration

By neglecting the wind farm of the RES in Figure 1.1, a typical layout of photovoltaics (PV)-integrated DC-MG is shown in Figure 4.1, mainly including three different type of terminals, i.e., the PV unit, constant power load (CPL) and energy storage system (ESS). The PV unit is connected to the DC bus via boost converter and $P_{\mathrm{pv}}(i_{\mathrm{pv}})$ represents its generated power. Buck converter connects to load resistance R to imitate the electric vehicle (EV) charging load and behaves as CPL, and $P_{\mathrm{const}}(i_{\mathrm{const}})$ refers to its consuming power. ESS consists of energy storage unit (ESU) and battery is selected as the ESU. EUSs are linked to the DC bus by bidirectional DC converter (BiC) to compensate the mismatched power between PV unit and CPL. P_{outi} is the output power of ESU and subscript 'i' is the ESU index here. Positive and negative P_{outi}

indicate discharging and charging mode.

Islanded DC-MG is full of power electronic interfaces, resulting in the property of low inertia and poor damping. ESUs take the responsibility for offering ancillary power when DC-MG suffers from power fluctuation. Although VIDC has been proposed to solve the instability risk caused by low inertia and weak damping in the DC-MG, an extra control loop is needed when applying VIDC to droop control, which complicates the control structure. Hence, this chapter proposes two kinds of IDC methods to provide virtual inertia and mitigate the LFO in islanded DC-MG, by simply modifying the droop control without adding any controllers or observers.

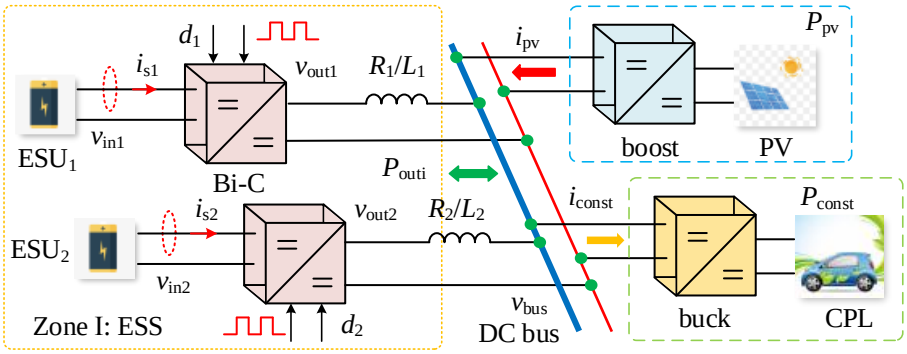


Figure 4.1: The general layout of the studied PV-integrated DC-MG.

4.1.2 Discussion about virtual inertia and damping control

Figure 4.2 shows the circuit of BiC. v_{in} and v_{out} are the input and output voltage of BiC; i_s and i_{out} are the input and output current. L_s, R_s and C_{out} are the filter inductance, resistance, and output capacitor, respectively. i_R=i_{const}-i_{pv} represents the power difference between CPL and PV unit. Droop control is usually adopted as the primary voltage regulation strategy, as shown in (4.1). v_{dcn} is the rated value of v_{out} and R_{d0} is the initial value of droop resistance. i_{set} is the output current reference of the BiC and usually set as 0. The superscript 'ref' refers to the reference values. Normally, dual-loop control (DLC) is also adopted to control the output voltage, with provision of no inertia and poor damping.

$$\begin{cases} v_{out}^{ref} = v_{dcn} - R_{d0} \cdot (i_{out} - i_{set}), \text{voltage mode,} & \text{(a)} \\ i_{out}^{ref} = i_{set} + (v_{dcn} - v_{out})/R_{d0}, \text{current mode,} & \text{(b)} \end{cases} \tag{4.1}$$

VIDC has been proposed with the essence of adding a parallel capacitor at the output side of BiC, as shown in Figure 4.2, to mitigate voltage oscillation by supplying or absorbing mismatched power. Its control equation is shown in (4.2). A inertia current is introduced to suppress RoCoV as in (4.2c). To reduce voltage oscillation amplitude, a damping current is injected as in (4.2b). Thus, an extra inertia loop is introduced, complicating the control system. C_{vir} is the

introduced virtual inertia coefficient, enlarging the equivalent DC capacitor and k_{vd} is damping coefficient. i_{iner} and i_{damp} represent the inertia and damping power supplied by ESS quickly. i_{iner} reduces RoCoV dv_{out}/dt, and i_{damp} restricts the fluctuation amplitude of v_{out} and keeps v_{out} at its reference to achieve power balance.

$$\frac{(v_{dcn}-v_{out})}{R_{d0}}-i_{out}^{'}-i_{damp}=C_{vir}\frac{d\left(v_{out}^{ref}-v_{dcn}\right)}{dt} \tag{4.2a}$$

$$i_{damp}=k_{vd}\left(v_{out}^{ref}-v_{out}\right) \tag{4.2b}$$

$$i_{iner}=C_{vir}\frac{d\left(v_{out}^{ref}-v_{dcn}\right)}{dt} \tag{4.2c}$$

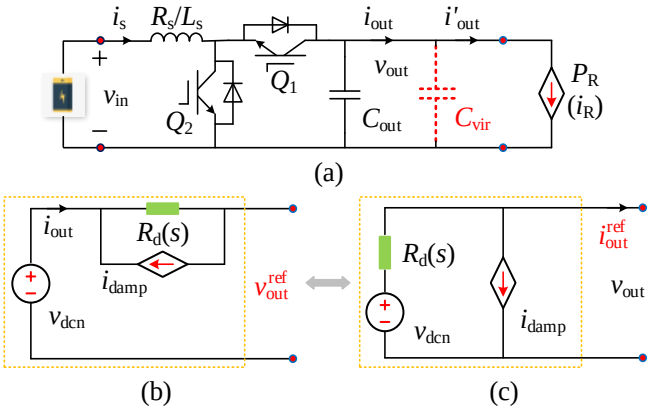


Figure 4.2: Diagram of BiC circuit and the simplified model of VIDC. (a) Circuit of BiC. (b) Voltage source model (c) Current source model.

The bandwidth of DLC is much higher than that of virtual inertia loop, making v_{out} and i_{out} track their reference fast, as shown in (4.3). Combining (4.1), (4.2) and (4.3), VIDC can be deduced as controlled-voltage source model and controlled-current source model, as shown in (4.4) and (4.5), respectively. ω_c is the cut-off frequency of low pass filter (LPF) $G_{lpf}(s)$. $R_d(s)$ is a capacitive impedance of the series connection of R_{d0} and $G_{lpf}(s)$.

$$v_{out}\approx v_{out}^{ref},\qquad i_{out}(i_{out}^{'})\approx i_{out}^{ref} \tag{4.3}$$

$$v_{out}^{ref}=v_{dcn}-\underbrace{R_d(s)\cdot i_{out}}_{\text{inertia term}}-\underbrace{k_{vd}R_d(s)\left(v_{out}^{ref}-v_{out}\right)}_{\text{damping term}} \tag{4.4a}$$

$$i_{out}^{ref}=\underbrace{\frac{(v_{dcn}-v_{out})}{R_d(s)}}_{\text{inertia term}}-\underbrace{k_{vd}(v_{dcn}-R_d(s)i_{out}-v_{out})}_{\text{damping term}} \tag{4.4b}$$

$$\begin{cases}\omega_c=1/C_{vir}R_{d0}\\ R_d(s)=\omega_c/(s+\omega_c)\cdot R_{d0}=G_{lpf}(s)R_{d0}\end{cases} \tag{4.5}$$

Accordingly, the controlled-voltage source and controlled-current source model of VIDC can be obtained, as shown in Figure 2.2(b) and (c). Clearly, the inertia comes from the dynamic

virtual impedance (DVI) $R_d(s)$ and the damping is introduced by the voltage-deviation-based damping term to prevent v_{out} from deviating from its reference. Comparing (4.1) and (4.4), it can be found that there are two differences between conventional droop control and VIDC: *i.* VIDC has a DVI with virtual inertia support ability, *ii.* VIDC has a damping term to suppress voltage oscillation. It can be concluded that VIDC, in nature, is an adaptive droop control with a DVI $R_d(s)$ and a damping term composed of first-order lag unit, which offers new insights into the provision mechanism of inertia and damping by VIDC.

4.2 Inertia Droop Control

According to the established droop-control-form model of VIDC, two kinds of inertia droop control (IDC) are proposed in this section. The specific design process is as follows.

4.2.1 Design of voltage-mode inertia droop control

Voltage-mode inertia droop control (vm-IDC) is shown in (4.6). The DVI is still formed by the product of a droop resistance R_{d0}^{v} and $G_{lpf}(s)$, which can imitate the performance of VIDC with inertia coefficient equal to C_{vir}. The superscript 'v' represents the voltage mode. The original first-order lag unit is replaced by a simple integral unit as the damping term φ_v and k_{damp}^{v} is the introduced damping coefficient, limiting the voltage fluctuation amplitude. Besides, v_{dcn} is used to eliminate steady-state voltage errors. Thus, the damping term φ_v has the essence of secondary voltage recovery (SVR) loop.

$$v_{out}^{ref} = v_{dcn} - R_d^v(s) \cdot (i_{out} - i_{set}) + \varphi \tag{4.6a}$$

$$R_d^v(s) = R_{d0}^v \cdot \frac{\omega_c}{(s + \omega_c)} = R + jX_c \tag{4.6b}$$

$$\varphi_v = k_{damp}^v \int \left(v_{dcn} - v_{out}^{ref}\right) dt \tag{4.6c}$$

To better illustrate the inertia effect of DVI in frequency domain, the Bode diagram and vector diagram of $R_d^v(s)$ with R_{d0}^v= 4 and $\omega_{c1}>\omega_{c2}$ are shown in Figure 4.3(a) according to (4.6b). it can be seen that $R_d^v(s)$ is a capacitive impedance, that is, there is a capacitive component X_c providing inertia support for DC-MG. Figure 4.3(a) also shows the vector diagram of $R_d^v(s)$ with ω=5rad/s. The phases of R_{d1}^v and R_{d2}^v lag behind R_{d0}^v, and their phase lags is less than 90°, which results in *positive* damping. The phase lag and X_c of $R_d^v(s)$ in low-frequency band increase as ω_c reduces, indicating increase of virtual inertia.

The discharging mode of ESU is taken as an example, and i_R increases from 0 at t_1 suddenly. Accordingly, the time-domain explanation of inertia response is in Figure 4.3(b).

1) When the damping and inertia terms are ignored (i.e., only droop control remained without inertia), v_{out}^{ref} would fall to v_0 at t_1 quickly with a large RoCoV, and a voltage deviation Δv occurs. Due to the low-inertia and poor-damping property of BiC, the step change Δv of v_{out}^{ref} might cause voltage oscillations.

2) When only considering the inertia term with $\omega_{c1}>\omega_{c2}$, v_{out}^{ref} will transition to v_0 at t_3 and t_4 smoothly and RoCoV is significantly declined, proving inertia emulation is achieved by $R_d(s)$.

At t_2, the capacitive component $X_{c1,\,2}$ of $R_{d1,\,2}$ provides inertia power and slows down the RoCoV, making v_{out}^{ref} drop to v_1, v_2 respectively. This is equivalent to generating an inertia-related voltage compensation term $\Delta v_{iner1,\,2}$ in real-time. Obviously, decreasing ω_c leads to the inertia rising. The inertia power mentioned above can only reduce RoCoV, but cannot eliminate the voltage deviation Δv inherent in droop control.

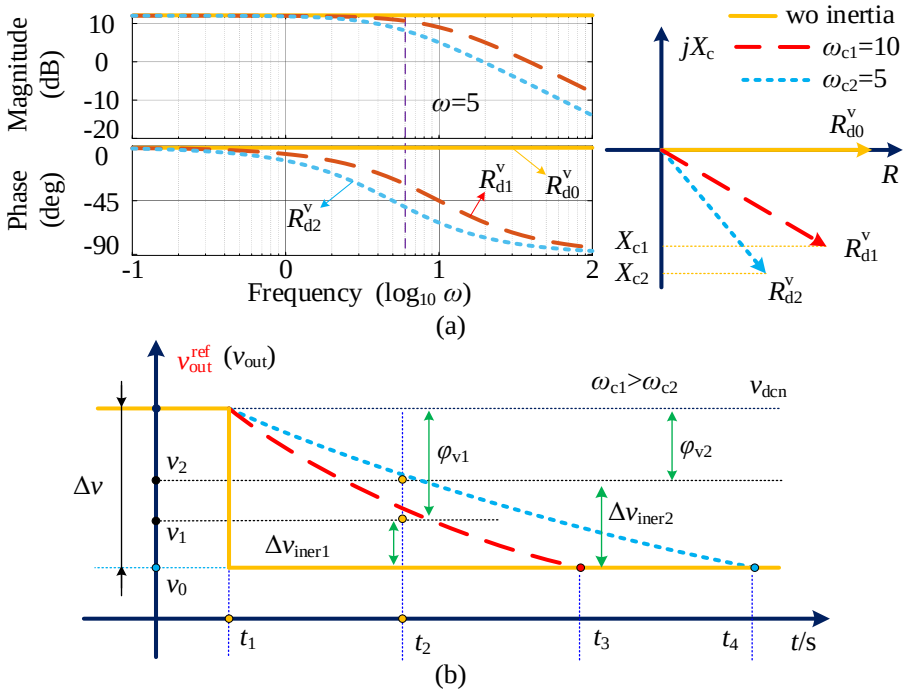


Figure 4.3: Inertia explanation of vm-IDC. (a) Frequency domain. (b) Time domain.

3) On the basis of *2)*, the damping term φ_v is introduced also, which can support a damping current to restrict the voltage fluctuation amplitude. From another perspective, a damping-related voltage compensation term $\varphi_{v1,\,2}$ is produced, making $\Delta v=\varphi_v+\Delta v_{iner}$, to eliminate the voltage deviation from $R_{d1,\,2}$.

The damping term φ_v is equivalent to introducing a Proportional-integral (PI) controller in the feedback loop, forming a SVR loop. The inertia-related and damping-related voltage compensation terms come from the provision of auxiliary power, essentially. The block diagram of vm-

IDC is in Figure 4.4, including DVI loop, SVR loop, and DLC.

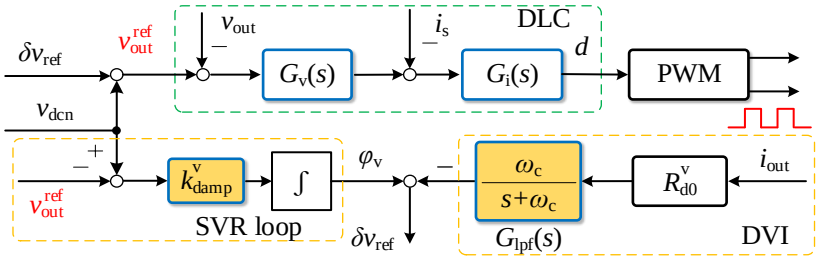


Figure 4.4: Control diagram of voltage-mode inertia droop control.

4.2.2 Design of current-mode inertia droop control

Current-mode inertia droop control (cm-IDC) is developed in this section. In DC-MG, the RoCoV and the voltage deviation scale is related to the unbalanced power and capacitance inertia level. Accordingly, when DC-MG suffers from power disturbance, ESU can change its output level quickly, due to its rapid response capability, to provide inertia power and shrink the power difference between the supplying and the demanding, thus reducing RoCoV. This can be achieved by dynamic swing of droop curve. The control equation of cm-IDC is shown in (4.7). δv_{out} is the transient voltage variation (with unit, V/0.01s). $R_d^i(\delta v_{out})$ is the adaptive droop resistance (i.e., a function of δv_{out}) whose design will be illustrated later and it can achieve the dynamic swing of droop curve. The superscript 'i' represents the current mode here. In the transient process, droop curve would swing, according to δv_{out}, to vary droop resistance and supply inertia power, whereas the droop resistance will be a constant in steady state. φ_i refers to the damping and SVR terms, and k_{damp}^i, and k_{svr}^i are the introduced damping coefficient and SVR coefficient.

$$i_s^{ref} = (v_{dcn} - v_{out} + \varphi_i)/R_d^i(\delta v_{out}) \tag{4.7a}$$

$$\varphi_i = k_{damp}^i(v_{dcn} - v_{out}) + k_{svr}^i \int (v_{dcn} - v_{out})\,dt \tag{4.7b}$$

Figure 4.5(a) and (b) show the principle of the inertia provision by swinging droop curve, the damping and SVR effect from φ_i. At the initial operation point A, there is a power balance i_{out}=i_R=i_a.

1) During the discharging mode of ESU, if i_R increases from i_a to i_b suddenly and only droop control takes effect, power difference Δi will cause a rapid voltage drop (V_a-V_b) to increase i_{out} from i_a to i_b, as in (4.8a).

In this transient process, the operation point moves from A to B along the curve **i** gradually and the power difference declines from Δi to 0, re-establishing the power balance. At this time, if

the variable droop resistance $R_d^i(\delta v_{out})$ mentioned above is used, inertia power can be provided. Specifically, BiC can immediately release more power from i_a to i_c, if reduce the droop resistance $R_d^i(\delta v_{out})$ quickly (i.e., turn **i** to **ii** counter-clockwise) as in Figure 4.5(a). The power difference is shrunk from Δi to i_{vd}, as in (4.8b). (4.8b) can be rewritten into (4.9), and it can be observed that i_{iner} is regarded as the inertia power stored in virtual capacitor C_{vir}, enhancing the equivalent inertia and restricting the RoCoV. $k = i_s/i_{out}$ is the ratio between i_s and i_{out}.

When a reduction of i_R occurs, the droop resistance should be increased quickly (i.e., turn **i** to **iii** clockwise) as in Figure 4.5(a). The scenario where ESU is in the charging mode is shown in Figure 4.5(b). Swinging droop curve reasonably and quickly can create required inertia. However, the voltage deviation caused by droop control are still retained.

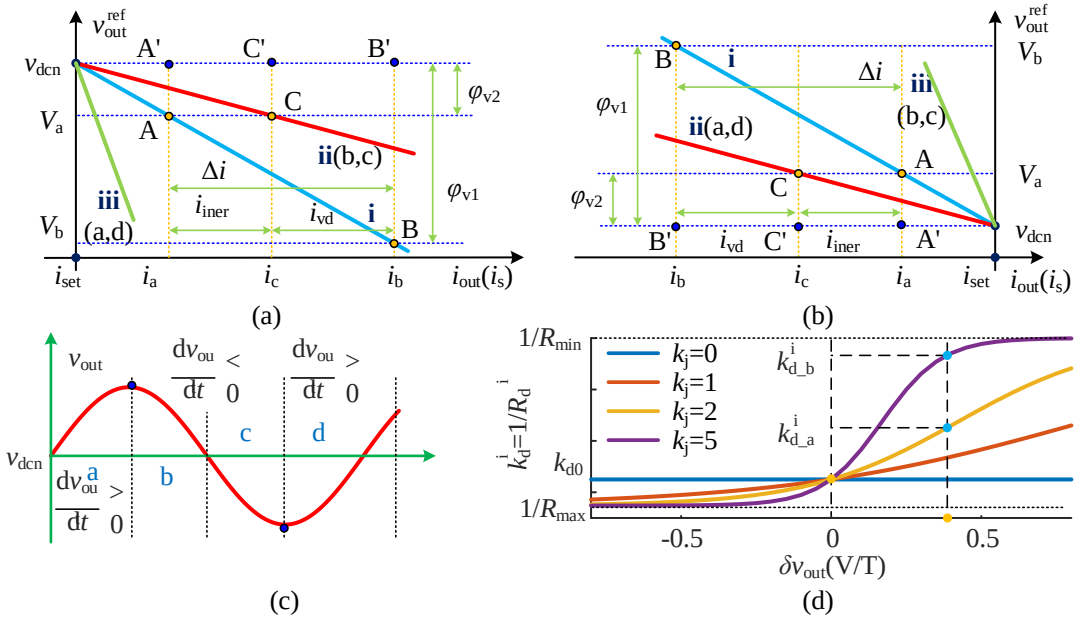


Figure 4.5: Explanation of inertia from cm-IDC. (a) Discharging mode. (b) Charging mode. (c) Transient voltage (d) Variable droop resistance.

2) From Figure 4.5(a) and (b), the damping term φ_i of (4.7b) provides damping power i_{vd}, restricting the voltage fluctuation amplitude during the dynamic process. Due to its integral effect, a voltage compensation term φ_i is produced to cancel the voltage deviation by droop control thoroughly. Thus, the operation points A, B and C will move to their mapping points A', B' and C' on the horizontal dashed line v_{dcn}.

$$\Delta i = k(i_{out} - i_R) = kC_{out}\frac{dv_{out}}{dt}, \quad \text{point A} \tag{4.8a}$$

$$i_{vd} = k(i_{out} - i_R) = kC_{out}\frac{dv_{out}}{dt} = \Delta i - i_{iner}, \quad \text{point C} \tag{4.8b}$$

$$\Delta i = kC_{\text{out}}\frac{\mathrm{d}v_{\text{out}}}{\mathrm{d}t} + i_{\text{iner}} = k(C_{\text{out}} + C_{\text{vir}})\frac{\mathrm{d}(v_{\text{out}} - v_{\text{dcn}})}{\mathrm{d}t} \tag{4.9}$$

The waveform of voltage oscillation is shown in Figure 4.5(c). The design principle of $R_{\text{d}}^{\text{i}}(\delta v_{\text{out}})$ illustrated as follows.

a) In the discharging mode of ESU, when RoCoV is greater than 0, indicating $i_{\text{out}}>i_{\text{R}}$, the droop resistance $R_{\text{d}}^{\text{i}}(\delta v_{\text{out}})$ should be increased to reduce $i_{\text{out}}^{\text{ref}}$. However, when RoCoV is less than 0, indicating $i_{\text{out}}<i_{\text{R}}$, the droop resistance should be reduced to increase $i_{\text{out}}^{\text{ref}}$. In the charging mode of ESU, the adjustment principle of $R_{\text{d}}^{\text{i}}(\delta v_{\text{out}})$ is completely opposite.

b) As mentioned before, RoCoV reflects the scale of power difference. Therefore, the degree of swinging the droop curve (i.e., the amount of provided inertia power) depends on RoCoV.

In practice, δv_{out} would substitute RoCoV and is detected by a washout filter $G_{\text{w}}(s)$. Algorithm of adaptive droop resistance $R_{\text{d}}^{\text{i}}(\delta v_{\text{out}})$ is defined in (4.10). k_{j} is the introduced inertia coefficient for cm-IDC. R_{d0}^{i} is the initial value of droop coefficient, R_{min} and R_{max} are the minimum and maximum respectively.

In discharging mode:

$$\begin{cases} R_{\text{d}}^{\text{i}}(\delta v_{\text{out}}) = R_{\text{d0}}^{\text{i}} + \left(R_{\text{max}} - R_{\text{d0}}^{\text{i}}\right)\tanh\left(k_{\text{j}}\delta v_{\text{out}}\right), \delta v_{\text{out}} > 0 \\ R_{\text{d}}^{\text{i}}(\delta v_{\text{out}}) = R_{\text{d0}}^{\text{i}} + \left(R_{\text{d0}}^{\text{i}} - R_{\text{min}}\right)\tanh\left(k_{\text{j}}\delta v_{\text{out}}\right), \delta v_{\text{out}} < 0 \end{cases} \tag{4.10a}$$

In charging mode:

$$\begin{cases} R_{\text{d}}^{\text{i}}(\delta v_{\text{out}}) = R_{\text{d0}}^{\text{i}} + \left(R_{\text{d0}}^{\text{i}} - R_{\text{min}}\right)\tanh\left(-k_{\text{j}}\delta v_{\text{out}}\right), \delta v_{\text{out}} > 0 \\ R_{\text{d}}^{\text{i}}(\delta v_{\text{out}}) = R_{\text{d0}}^{\text{i}} + \left(R_{\text{max}} - R_{\text{d0}}^{\text{i}}\right)\tanh\left(-k_{\text{j}}\delta v_{\text{out}}\right), \delta v_{\text{out}} < 0 \end{cases} \tag{4.10b}$$

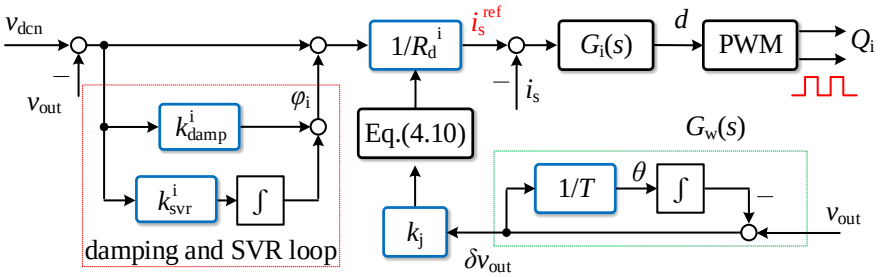


Figure 4.6: Control diagram of current-mode inertia droop control

Take (4.10b) as an example to analyze the inertia response from swinging droop curve, as in Figure 4.5(d). $k_{\text{d}}^{\text{i}}=1/R_{\text{d}}^{\text{i}}(\delta v_{\text{out}})$. A larger k_{j} makes k_{d}^{i} closer to its saturation and droop curve swing faster, indicating that the more inertia power is provided. The larger δv_{out} reflects that the disturbance scale is large and more inertia power is required. From Figure 4.5(d), with δv_{out} increasing, the droop curve swings more violently to support more inertia power, meaning that

the ‘tanh’ function meets the control requirements well. Therefore, the inertia response essentially comes from the dynamic regulation of i_{out}^{ref} due to droop curve swinging, making ESU absorb/release power at a faster speed in the transient process. It is an adaptive droop control.

Figure 4.6 presents the diagram of cm-IDC, including the damping loop, SVR loop and adaptive algorithm of $R_d^i(\delta v_{out})$. T=0.01s is the time constant of $G_w(s)$.

4.3 Stability Mechanism Analysis

In this section, an analytic way, feedback analysis method, is proposed to observe the interaction among variables intuitively, identify the physical sense of parameters and explain the control function of the virtual inertia from multiple perspectives, as well as a double-coordinate-based phasor diagram is constructed as the analytical tool.

4.3.1 Introduction of feedback analysis method

Before discussing the stability mechanism of IDC, a similar physics phenomenon, free vibration, is introduced firstly to illustrate feedback analysis approach. As shown in Figure 4.7(a), the mass-spring-damper (MSD) model is selected. Its dynamics equation is given in (4.11) by the Newton’s law of motion.

$$ma + cv + k_s x = F(t) \Rightarrow v = F(s)M(s) \tag{4.11}$$

$$M(s) = \frac{s}{ms^2 + cs + k} \tag{4.12}$$

where $M(s)$ is its frequency response, determining the state of the model subject to external force $F(t)$ and characterizing the motion behaviour of v. m is the mass, k_s is the stiffness of the spring, and c is the damping coefficient. a, v and x are the acceleration, velocity and displacement, respectively.

Based on conservation of energy, the injected energy E_{in} by F is transferred into kinetic energy E_m and potential energy E_k, and dissipated by the damper (E_d). Hence, $M(s)$ is with positive damping (PD) to attenuate the vibration of MSD model. Feedback analysis approach is developed to explain the PD.

Figure 4.7(d) presents the phasor diagram of v and its feedback F_{fd} at a certain frequency. From the view of motion, the effect of damper F_c is opposite to v and F (a_c<0), consuming E_{in}, featuring PD, and forcing v converging to 0 faster, as shown in Figure 4.7(e). As a conservative force, F_k lags F_c 90° and completes the energy conversion between E_m and E_k. Thus, PD comes

from the negative feedback (NF) formed by F_{fd}, as shown in Figure 4.7(c), weakening the influence of F on this model. DC voltage exhibits similar motion to velocity in dynamic process. Thus, IDC can be comprehended by the above method.

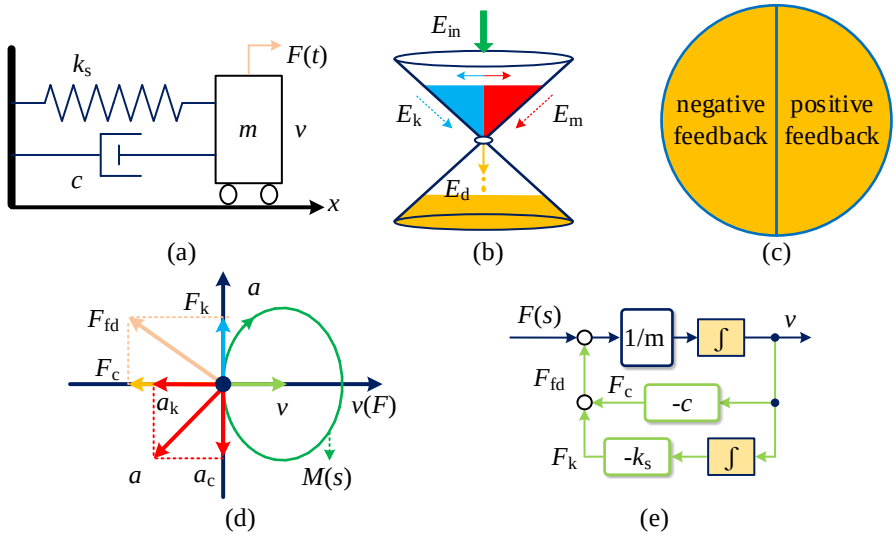


Figure 4.7: Feedback analysis. (a) MSD model. (b) Energy conversion. (c) Illustration of feedback. (d) Phasor analysis. (e) Sketch of feedback control.

4.3.2 Unified model and stability mechanism analysis

The control equations of vm- and cm-IDC can be rewritten into VIDC form. According to (4.6), vm-IDC can be deduced into (4.13a), meanwhile, cm-IDC can be rearranged as (4.13b) based on (4.7) and (4.8). Their unified small-signal model can be derived in (4.14a) and is similar to the VIDC [84]. Δi_{dis} refers to the power disturbance between supplying and demanding, and would be compensated by the virtual inertia and damping currents, as shown in (4.14a). C_v is the virtual inertia, k_{damp} and L_{svr} are the introduced damping and SVR coefficient. Accordingly, the parameter definitions for vm- and cm-IDC are shown in (4.14b). Then, (4.14c) can be obtained easily from (4.14a). $A(s)$ is a phasor with unit of Ohm, describing the motion law of voltage and the dynamic behavior of DC-MG under the effect of Δi_{dis}, and revealing the stability mechanism of IDC. The control goal is that net power disturbance i_{net} in the system becomes zero under the compensation effect of the feedback current i_{fd} from IDC, as shown in equation (4.14d). $Plant(s)$ is the open-loop output-impedance of BiC, as shown in (4.15).

$$\frac{\left(v_{dcn}-v_{out}^{ref}\right)}{R_{d0}^{v}}-i_{out}-\underbrace{\frac{k_{damp}^{v}\left(v_{out}^{ref}-v_{dcn}\right)}{R_{d0}^{v}}}_{\text{damping term}}-\underbrace{\frac{1}{s}\frac{k_{damp}^{v}\left(v_{out}^{ref}-v_{dcn}\right)}{R_{d0}^{v}}}_{\text{SVR}}=\underbrace{\frac{s\left(v_{out}^{ref}-v_{dcn}\right)}{\omega_c R_{d0}^{v}}}_{\text{inertia term}} \quad (4.13a)$$

$$i_{\mathrm{s}}^{\mathrm{ref}}-\frac{(v_{\mathrm{dcn}}-v_{\mathrm{out}})}{R_{\mathrm{d0}}^{\mathrm{i}}}-\underbrace{\frac{k_{\mathrm{damp}}^{\mathrm{i}}(v_{\mathrm{out}}-v_{\mathrm{dcn}})}{R_{\mathrm{d}}^{\mathrm{i}}}}_{\text{damping term}}-\underbrace{\frac{k_{\mathrm{svr}}^{\mathrm{i}}}{s}\frac{(v_{\mathrm{out}}-v_{\mathrm{dcn}})}{R_{\mathrm{d}}^{\mathrm{i}}}}_{\text{SVR}}=\underbrace{skC_{\mathrm{vir}}(v_{\mathrm{out}}-v_{\mathrm{dcn}})}_{\text{inertia term}} \tag{4.13b}$$

$$\text{unified model: } \Delta i_{\mathrm{dis}}=\underbrace{sC_{\mathrm{v}}\frac{\mathrm{d}\Delta v_{\mathrm{out}}}{\mathrm{d}t}}_{\text{inertia term } i_{\mathrm{iner}}}+\underbrace{k_{\mathrm{damp}}\Delta v_{\mathrm{out}}}_{\text{damping term } i_{\mathrm{vd}}}+\underbrace{\frac{\int_0^t \Delta v_{\mathrm{out}}\,\mathrm{d}t}{L_{\mathrm{svr}}}}_{\text{SVR term } i_{\mathrm{svr}}} \tag{4.14a}$$

$$\begin{cases} C_{\mathrm{v}}=\dfrac{1}{\omega_{\mathrm{c}}R_{\mathrm{d0}}^{\mathrm{v}}}, \quad k_{\mathrm{damp}}=\dfrac{k_{\mathrm{damp}}^{\mathrm{v}}}{R_{\mathrm{d0}}^{\mathrm{v}}}, \quad \dfrac{1}{L_{\mathrm{svr}}}=\dfrac{k_{\mathrm{damp}}^{\mathrm{v}}}{R_{\mathrm{d0}}^{\mathrm{v}}}, & \text{for vm}-\text{IDC} \\ C_{\mathrm{v}}=C_{\mathrm{vir}}, \quad k_{\mathrm{damp}}=\dfrac{k_{\mathrm{damp}}^{\mathrm{i}}}{kR_{\mathrm{d}}^{\mathrm{i}}}, \quad \dfrac{1}{L_{\mathrm{svr}}}=\dfrac{k_{\mathrm{svr}}^{\mathrm{i}}}{kR_{\mathrm{d}}^{\mathrm{i}}}, & \text{for cm}-\text{IDC} \end{cases} \tag{4.14b}$$

$$\Delta i_{\mathrm{dis}}\cdot A(s)-\Delta v_{\mathrm{out}}=0 \;\Rightarrow\; A(s)=\frac{L_{\mathrm{svr}}s}{L_{\mathrm{svr}}C_{\mathrm{v}}s^2+L_{\mathrm{svr}}k_{\mathrm{damp}}s+1} \tag{4.14c}$$

$$\text{objective function: } i_{\mathrm{net}}=\Delta i_{\mathrm{dis}}+i_{\mathrm{fd}}=0 \tag{4.14d}$$

$$Plant(s)=\frac{L_{\mathrm{s}}s+R_{\mathrm{s}}}{L_{\mathrm{s}}C_{\mathrm{out}}s^2+R_{\mathrm{s}}C_{\mathrm{out}}s+(1-D)^2} \tag{4.15}$$

Table 4.1 Analogy between the mass-spring-damper model and virtual inertia control

Items (parameter-unit)	mass-spring-damper model	virtual inertia control
Kinetic energy	$mv^2/2$ (m-kg)	$C_{\mathrm{v}}v_{\mathrm{out}}^2/2$ (C_{v}-F)
Potential energy	$kx^2/2$ (k-N/m)	$L_{\mathrm{svr}}i_{\mathrm{svr}}^2/2$ (k_{svr}-H)
Damping source	damper (c-N·s/m)	i_{vir} (k_{damp}-S)
State variable	a, v, x	$s\cdot v_{\mathrm{out}}$, v_{out}, v_{out}/s
External excitation	F	i_{dis}
Inertia	M	C_{v}

Remark 1: From the perspective of circuit theory, IDC can be equivalent to the parallel *RLC* circuit from (4.14a), as shown in Figure 4.8(a). Different from previous works [81], an extra inductor L_{svr} is added due to the SVR loop, to eliminate the voltage deviation.

Comparing (4.12) and (4.14), it is inferred that the negative-feedback structure and positive-damping properties are inherent in $A(s)$. The analogy between the MSD model and IDC is in Table 4.1. Figure 4.8(b) is the closed-loop model of BiC. The superscript 'fd' represents feedback variables from the IDC loop.

Remark 2: From Figure 4.8(b), IDC behaves as a PID controller for Δv_{out} in terms of control theory and (4.14d) is the objective function. $i_{\mathrm{fd}}=i_{\mathrm{iner}}^{\mathrm{fd}}+i_{\mathrm{vd}}^{\mathrm{fd}}+i_{\mathrm{svr}}^{\mathrm{fd}}$ is the feedback current, making the net power disturbance $i_{\mathrm{net}}=0$, i.e., DC-MG always in the non-disturbed state under the compensation effect of IDC. Obviously, IDC is a NF loop.

To observe the interaction among variables intuitively and explain the NF physically, a double-

coordinate-based phasor diagram as the analytical tool for feedback analysis method is constructed. It includes the Δi_{dis}-based current coordinate system (CCS) and the Δv_{out}-based voltage coordinate system (VCS), as shown in Figure 4.8(c) and (d). CCS describes the interaction between variables and explains the negative feedback mechanism from the perspective of control principles and dynamics. VCS describes the energy conversion and explains the dissipation characteristics based on the conservation of energy. Here, the superscripts 'h' and 'v' refer to the horizontal and vertical component. The explanation of Figure 4.8(c) of $\Delta i_{dis}>0$ is as follows.

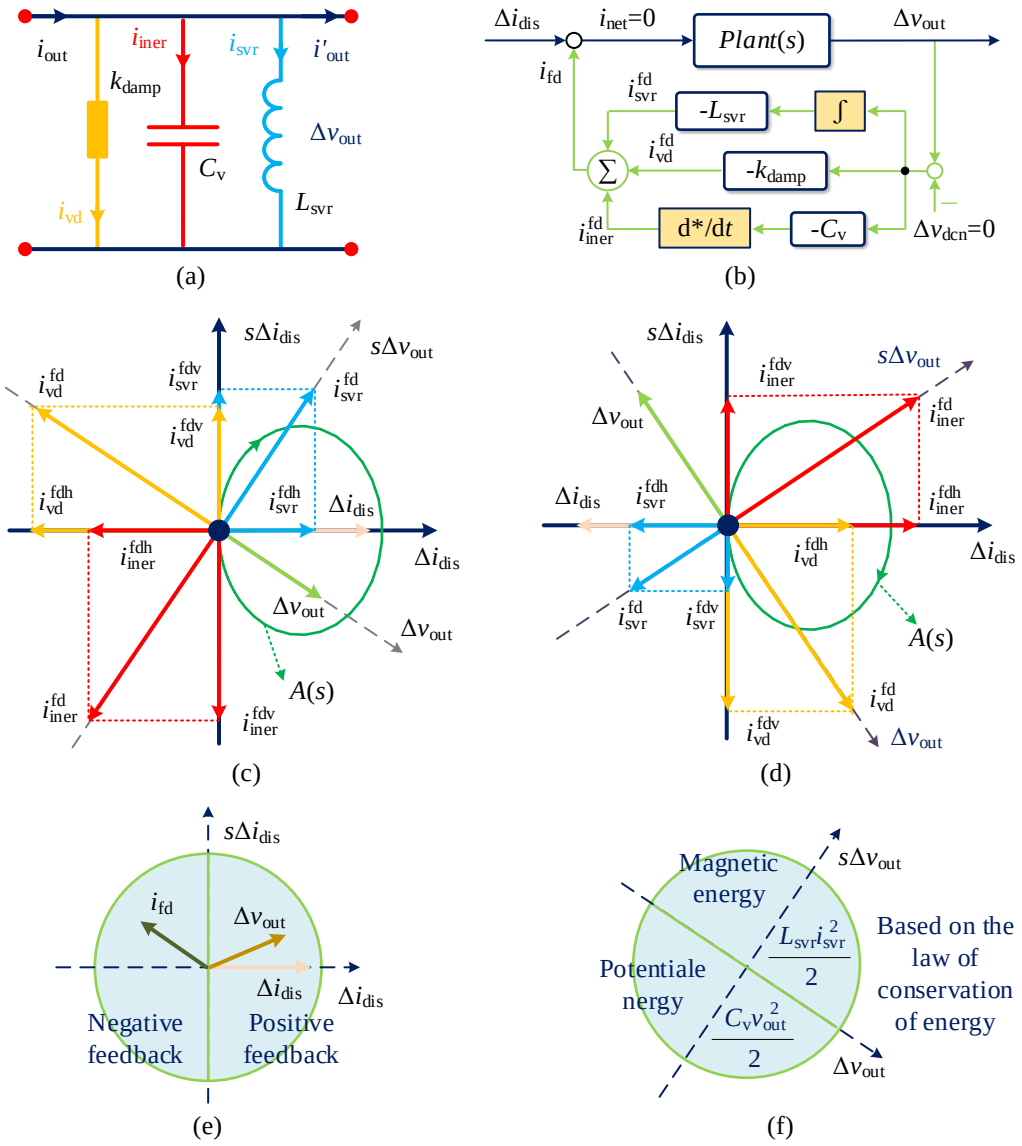


Figure 4.8: Physical interpretation of IDC. (a) *RLC* equivalent model. (b) The equivalent model of BiC with IDC. (c) Phasor diagram when $\Delta i_{dis}>0$. (d) Phasor diagram when $\Delta i_{dis}<0$. (e) Illustrate of feedback control. (f) Sketch of energy.

CCS: After DC-MG is disturbed by Δi_{dis}, Δv_{out} would be generated and locate in the 1st/4th quadrant, under the effect of *plant*(*s*). Usually, v_{out} is prone to oscillate due to the property of

low inertia and poor damping without IDC. Clearly, the horizontal components of Δi_{dis} and Δv_{out} are in same phase, enlarging Δv_{out} continuously and making voltage oscillation hard to dampen spontaneously. This process is similar to positive feedback (PF).

Δv_{out} generates three feedback components i_{iner}^{fd}, i_{vd}^{fd} and i_{svr}^{fd}, via the IDC loop in Figure 4.8(b). Obviously, i_{fd} is opposite to Δv_{out}, which is similar to the relation between damper and speed in dynamics, forcing Δv_{out} to converge to 0 (the function of NF).

From another perspective, after decomposing these three components in CCS orthogonally, it can be observed that i_{iner}^{fdh} and i_{hvd}^{fd} are opposite to Δi_{dis}, reducing the net input from Δi_{dis} and undermining the effect of Δi_{dis}. Hence, i_{hiner}^{fd} and i_{hvd}^{fd} forms a NF to Δi_{dis}, as depicted in Figure 4.8(b). The related illustration of NF and PF is in Figure 4.8(e). *Note that*, it is guaranteed that the strength of NF is stronger than PF when C_v, k_{damp} and L_{svr} are all larger than 0 (the necessary and sufficient condition for ensuring stability of 2nd-order system), though i_{svr}^{fdh} is a PF component. From Figure 4.8(a), i_{svr}^{fdh} will be compensated by i_{vd}^{fdh} completely.

Remark 3: IDC loop is of NF and PD property, and makes feedback variables locate in the NF region. Feedback variables always attenuates the effect of Δi_{dis} and hinders v_{out} changing.

VCS: The injected energy E_{dis} by disturbance current Δi_{dis} is represented by i_{iner}^{fd}, i_{vd}^{fd} and i_{svr}^{fd}. In VCS, i_{iner}^{fd} and i_{svr}^{fd} are perpendicular to Δv_{out}, they correspond to the electrostatic potential energy in C_v and the magnetic energy in L_{svr}, making the injected energy flows between C_v and L_{svr} continuously, as shown in Figure 4.8(f). Thus, i_{iner}^{fd} and i_{svr}^{fd} only represent energy conversion. Eventually, the injected energy will be converted into i_{vd}^{fd} and dissipated by k_{damp} with damping property. This explanation is consistent with Figure 4.8(a). It is suggested in (4.14a) that, when subject to the same Δi_{dis}, the larger C_v leads to the smaller RoCoV. Transient voltage nadir (TVN) will be smaller if k_{damp} is larger and can be eliminated faster if L_{svr} is smaller.

Remark 4: From the point of conservation of energy, IDC can compensate the unbalance power quickly by shaping system dissipation property (k_{damp}), to mitigate voltage oscillation (by active damping). RoCoV and the voltage recovery speed are regulated by the energy transfer rate (adjusting C_v and L_{svr}).

According to the proposed phasor diagram, the interaction between various variables can be clearly observed and their physical significance can be studied, which is convenient for analyzing their influence on the motion trajectory of voltage.

Discussion 1: In the dynamic process, k_{damp}, L_{svr} and C_v represent the primary voltage regulation, secondary voltage regulation and inertia response, respectively. And thus k_{damp} is also of droop

coefficient property. In the steady state, the primary voltage regulation is conducted by droop coefficient and SVR is still carried out by L_{svr}.

Discussion 2: Larger C_v causes stronger stability (inertia) and smaller RoCoV; L_{svr} reflects the grid stiffness (disturbance-rejection ability) and recovery (synchronized) ability, and voltage can recover faster with a smaller L_{svr}. k_{damp} is the damping ability that supplies/absorbs the unbalanced power and adjusts dynamic dissipation property. Remarks are the unified interpretation, applicable to the IDC and other VIDC strategies.

4.4 Dynamic Performance and Stability Analysis

After analytically clarifying the physical meaning of virtual inertia loop from multi-view, this section investigates in detail how the parameters affect the dynamic performance by using pole-zero distribution and step response.

4.4.1 Dynamic performance analysis of IDC

(a) voltage-mode inertia droop control:

Linearizing (4.13a), the relation between Δi_{out} and Δv_{out}^{ref} can be obtained as shown in (4.16). The physical meaning of (4.16) is to illustrate the influence of power disturbance on Δv_{out}^{ref} considering the inertia loop, reflecting the dynamic performance of vm-IDC.

$$\frac{\Delta v_{out}^{ref}}{\Delta i_{out}} = -\frac{\omega_c R_{d0}^{v} \cdot s}{s^2 + \omega_c\left(k_{damp}^{v} + 1\right)s + k_{damp}^{v} \cdot \omega_c} \tag{4.16}$$

The vm-IDC can be equivalent to a 2nd-order system and its damping ratio ξ_v can be calculated by (4.17).

$$\xi_v = \sqrt{\omega_c}\left(k_{damp}^{v} + 1\right)/\left(2\sqrt{k_{damp}^{v}}\right) \tag{4.17}$$

The pole distribution of (4.16) is shown in Figure 4.9(a) and (b), and there are two poles λ_1 and λ_2. There is a zero near λ_2, which constitutes dipoles and reduces the influence of λ_2. Hence, λ_1 becomes the dominant pole. As ω_c decreases, λ_1 moves to the imaginary axis, indicating that its inertia gradually increases. With k_{damp}^{v} increasing, the dominant pole λ_1 become far away from the imaginary axis, suggesting that its related component responds faster and voltage recovery time decreases. All poles are on the left half plane, ensuring vm-IDC stable.

(b) current-mode inertia droop control:

Ignoring damping term of cm-IDC, the inertia power i_{iner} and corresponding virtual inertia C_{vir} can be obtained from (4.8), as in (4.18).

$$i_{\text{iner}} = \frac{(v_{\text{dcn}} - v_{\text{out}})}{R_{\text{d}}^{\text{i}}(\delta v_{\text{out}})} - \frac{(v_{\text{dcn}} - v_{\text{out}})}{R_{\text{d0}}^{\text{i}}} = -kC_{\text{vir}}\frac{\text{d}v_{\text{out}}}{\text{d}t} \approx -kC_{\text{vir}}\frac{\delta v_{\text{out}}}{T} \tag{4.18}$$

The negative sign indicates the charging mode. Their relation is shown in Figure 4.9(c) and (d). The inertia response is related to δv_{out} and controlled by k_{j}. As k_{j} increases, the C_{vir} gets larger and more inertial power is supplied. A larger δv_{out} results in more obvious swing of droop curve and more inertia power, indicating the emulated inertia is time-varying and regulated as required. The droop curve swings to the original value of droop resistance temporarily and no inertia power is provided when δv_{out}=0, as shown in Figure 4.5(c), in the transient process. At this time, the size of C_{vir} no longer has an impact on control effect. The swing of droop curve stops and the droop resistance recovers to the original value after v_{out} stabilizes.

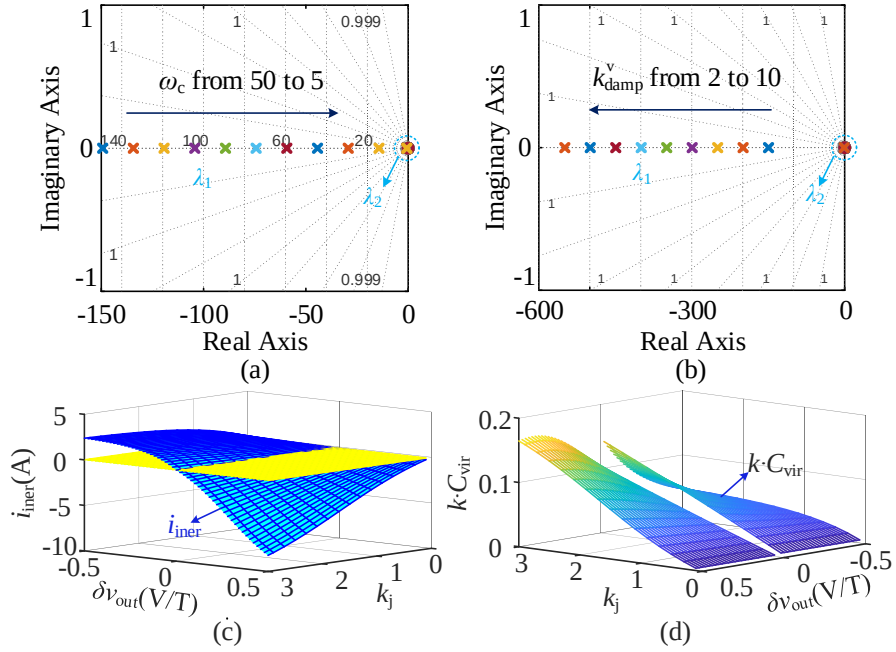


Figure 4.9: Dynamic analysis of inertia droop control. (a) vm-IDC with varying ω_{c}. (b) vm-IDC with varying $k_{\text{damp}}^{\text{v}}$. (c) Inertia power from cm-IDC. (d) Virtual inertia from cm-IDC.

4.4.2 Small-signal stability analysis of voltage-mode IDC

Ignoring the power loss, the power balance between the input and output sides of BiC can be obtained as shown in (4.19).

$$V_{\text{in}}i_{\text{s}} = \left(i_{\text{out}} + C_{\text{out}}\frac{\text{d}v_{\text{out}}}{\text{d}t}\right)v_{\text{out}} \tag{4.19}$$

Perturbing (4.19), there is:

$$V_{\text{in}}\Delta i_{\text{s}} = (I_{\text{out}} + s\cdot 2\cdot C_{\text{out}}V_{\text{out}})\Delta v_{\text{out}} + V_{\text{out}}\Delta i_{\text{out}} \tag{4.20}$$

Therefore, the relation between Δi_{out} and Δi_{s} can be obtained, as shown in (4.21).

$$G_{\mathrm{ii}} = \Delta i_{\mathrm{out}}/\Delta i_{\mathrm{s}} = V_{\mathrm{in}}/V_{\mathrm{out}} \tag{4.21}$$

The state average model of BiC can be acquired as shown in (4.22). d is the control variable, i.e., duty ratio.

$$\begin{cases} L_{\mathrm{s}}\dfrac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} = v_{\mathrm{in}} - R_{\mathrm{s}}i_{\mathrm{s}} - (1-d)v_{\mathrm{out}} \\ C_{\mathrm{out}}\dfrac{\mathrm{d}v_{\mathrm{out}}}{\mathrm{d}t} = (1-d)i_{\mathrm{s}} - i_{\mathrm{out}} \end{cases} \tag{4.22}$$

Linearizing (4.22) and applying the *Laplace* transform, the relationship between Δi_{s} and Δd can be obtained as follows.

$$G_{\mathrm{id}}(s) = \frac{\Delta i_{\mathrm{s}}}{\Delta d} = \frac{C_{\mathrm{out}}V_{\mathrm{dcn}}s + (1-D)I_{\mathrm{s}}}{L_{\mathrm{s}}C_{\mathrm{out}}s^2 + R_{\mathrm{s}}C_{\mathrm{out}}s + (1-D)^2} \tag{4.23}$$

Combining (4.7) and (4.19)-(4.23), the small-signal model of vm-IDC can be obtained as shown in Figure 4.10. Accordingly, the transfer function ($T^{\mathrm{v}}_{\mathrm{vv}}(s)$ and $T^{\mathrm{v}}_{\mathrm{vi}}(s)$) between Δv_{out} and Δv_{dcn}, Δv_{out} and Δi_{out} is derived and shown in (4.24), revealing the performance of v_{out} in tracking its reference and rejecting disturbance.

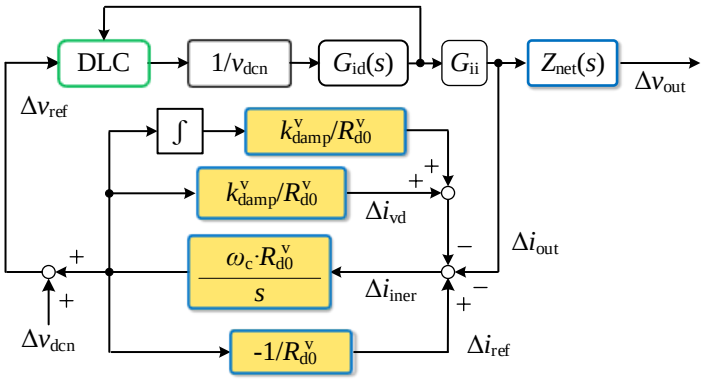


Figure 4.10: Small-signal model of vm-IDC.

$$T^{\mathrm{v}}_{\mathrm{vv}}(s) = \frac{\Delta v_{\mathrm{out}}}{\Delta v_{\mathrm{dcn}}} = \frac{\left(k^{\mathrm{v}}_{\mathrm{damp}} + s\right)G_{\mathrm{v}}G_{\mathrm{i}}G_{\mathrm{id}}G_{\mathrm{ii}}Z_{\mathrm{net}}}{\left(k^{\mathrm{v}}_{\mathrm{damp}} + s\right)\left[v_{\mathrm{dcn}} + G_{\mathrm{i}}G_{\mathrm{id}}(1 + G_{\mathrm{v}}G_{\mathrm{ii}}Z_{\mathrm{net}})\right] + sR^{\mathrm{v}}_{\mathrm{d0}}G_{\mathrm{lpf}}G_{\mathrm{v}}G_{\mathrm{i}}G_{\mathrm{id}}G_{\mathrm{ii}}} \tag{4.24a}$$

$$T^{\mathrm{v}}_{\mathrm{vi}}(s) = \frac{\Delta v_{\mathrm{out}}}{\Delta i_{\mathrm{out}}} = -\frac{\left[s\left(1 + R^{\mathrm{v}}_{\mathrm{d0}}G_{\mathrm{lpf}}G_{\mathrm{v}}G_{\mathrm{ii}}\right) + k^{\mathrm{v}}_{\mathrm{damp}}\right]G_{\mathrm{v}}G_{\mathrm{i}}G_{\mathrm{id}}G_{\mathrm{ii}}Z_{\mathrm{net}}}{\left(k^{\mathrm{v}}_{\mathrm{damp}} + s\right)G_{\mathrm{v}}G_{\mathrm{ii}}(v_{\mathrm{dcn}} + G_{\mathrm{v}}G_{\mathrm{i}}G_{\mathrm{id}}G_{\mathrm{ii}}Z_{\mathrm{net}})} \tag{4.24b}$$

Figure 4.11 depicts their dominant poles (λ_1~ λ_5) of $T^{\mathrm{v}}_{\mathrm{vv}}(s)$ and $T^{\mathrm{v}}_{\mathrm{vi}}(s)$. ξ is damping ratio of poles. It can be observed that there is a zero near λ_1, forming a dipole, thus the influence of λ_1 can be ignored. All the poles are in the left half plane, indicating the system can remain stable always. In Figure 4.11(a), λ_4 and λ_5 move into the poor damping region (PDR, ξ<0.707) and their oscillation frequency rises with $k^{\mathrm{v}}_{\mathrm{damp}}$ increasing, which is caused by the integration of SVR loop. In Figure 4.11(b), λ_4 and λ_5 have the risk of entering the PDR, and $\lambda_{2,3}$ become the oscillation

mode with ω_c declining, while they are always in the desired damping region (DDR, ξ>0.707). From Figure 4.11(c), λ_1 and $\lambda_{3,4,5}$ are impacted slightly, and λ_1 leaves away from the imaginary axis with varying k^v_{damp}, suggesting v_{out} can response faster with a better damping in transient process and the grid stiffness is strengthened to recover to steady state faster. In Figure 4.11(d), $\lambda_{1,2}$ and $\lambda_{4,5}$ are almost unaffected and λ_3 moves toward the imaginary axis with ω_c increasing, indicating longer response time and inertia enhancement. Its realistic meaning agrees with real capacitors, enhancing inertia and making voltage change slower and oscillation disappeared.

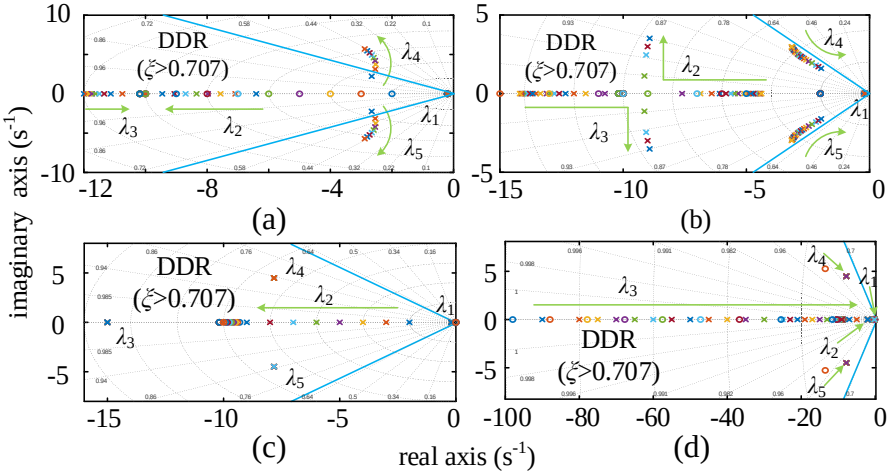


Figure 4.11: The pole distribution of $T^v_{vv}(s)$ and $T^v_{vi}(s)$. (a) $T^v_{vv}(s)$ when k^v_{damp} varying from 2 to 10 with ω_c=15. (b) $T^v_{vv}(s)$ when ω_c varying from 90 to 5, with k^v_{damp}=2. (c) $T^v_{vi}(s)$ when k^v_{damp} varying from 2 to 10 with ω_c=15. (d) T^v_{vi} when ω_c varying from 90 to 5, with k^v_{damp} =2.

4.4.3 Small-signal stability analysis of current-mode IDC

Take stage **b** in Figure 4.5(c) and discharging mode as an example to analyse the stability of cm-IDC. Based on (4.7) and (4.10a), Δi_s^{ref} can be described in (4.25), and initial condition for some variables is in (4.26). The superscript '0' represents the initial value at t=0. θ is an intermediate variable of $G_w(s)$.

$$\Delta i_s^{ref} = \frac{(\Delta v_{dcn} - \Delta v_{out})}{R^i_{d0}} + \frac{\Delta\varphi}{R^i_{d0}} - \frac{\varphi_0 \alpha k_j G_w(s) \Delta v_{out}}{{R^i_{d0}}^2} = \Delta i_s^{ref0} + \Delta i_{vd} + \Delta i_{iner} \tag{4.25a}$$

$$\alpha = \left(R^i_{d0} - R_{min}\right)\left[1 - \tanh^2\left(k_j \delta v^0_{out}\right)\right] \tag{4.15b}$$

$$\begin{cases} \delta v^0_{out} = v^0_{out} - \theta^0/T \\ \theta^0 = v_{dcn}T, R_d^{i,t=0}(\delta v_{out}) = R^i_{d0}, \varphi_0 = i_s^0 \cdot R^i_{d0} \end{cases} \tag{4.26}$$

Integrating (4.23), (4.25) and Figure 4.6, the small-signal model of vm-IDC can be obtained as shown in Figure 4.12. Accordingly, the transfer functions between Δv_{out} and Δv_{dcn}, Δv_{out} and Δi_{out} can be derived, as shown in (4.27) and (4.28).

$$T_{\mathrm{vv}}^{\mathrm{i}}(s)=\frac{\Delta v_{\mathrm{out}}}{\Delta v_{\mathrm{dcn}}}=\frac{\left[\left(1+k_{\mathrm{damp}}^{\mathrm{i}}\right)s+k_{\mathrm{svr}}^{\mathrm{i}}\right]G_{\mathrm{i}}G_{\mathrm{id}}G_{\mathrm{ii}}Z_{\mathrm{net}}}{sR_{\mathrm{d0}}^{\mathrm{i}}\left(v_{\mathrm{dcn}}+G_{\mathrm{i}}G_{\mathrm{id}}\right)+\left[s\left(1+k_{\mathrm{damp}}^{\mathrm{i}}+R_{\mathrm{d0}}^{\mathrm{i}}k_{\mathrm{j}}\varphi_0\alpha G_{\mathrm{w}}(s)\right)+k_{\mathrm{svr}}^{\mathrm{i}}\right]G_{\mathrm{i}}G_{\mathrm{id}}G_{\mathrm{ii}}Z_{\mathrm{net}}} \tag{4.27}$$

$$T_{\mathrm{vi}}^{\mathrm{i}}(s)=\frac{\Delta v_{\mathrm{out}}}{\Delta i_{\mathrm{out}}}=-\frac{sR_{\mathrm{d0}}^{\mathrm{i}}G_{\mathrm{i}}G_{\mathrm{id}}G_{\mathrm{ii}}Z_{\mathrm{net}}}{sR_{\mathrm{d0}}^{\mathrm{i}}v_{\mathrm{dcn}}+\left[s\left(1+k_{\mathrm{damp}}^{\mathrm{i}}+R_{\mathrm{d0}}^{\mathrm{i}}k_{\mathrm{j}}\varphi_0\alpha G_{\mathrm{w}}(s)\right)+k_{\mathrm{svr}}^{\mathrm{i}}\right]G_{\mathrm{i}}G_{\mathrm{id}}G_{\mathrm{ii}}Z_{\mathrm{net}}} \tag{4.28}$$

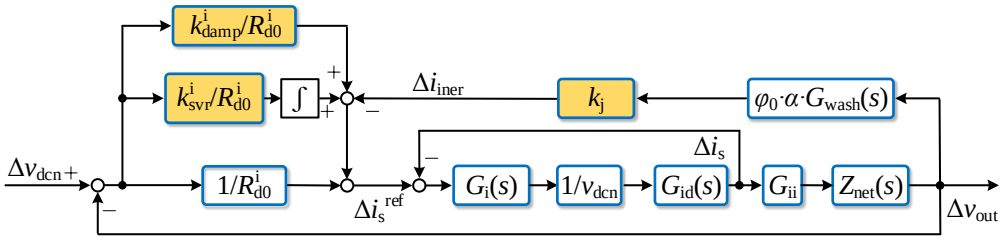


Figure 4.12: The pole distribution of $T_{\mathrm{vv}}^{\mathrm{v}}(s)$ and $T_{\mathrm{vi}}^{\mathrm{v}}(s)$.

The step responses of $T_{\mathrm{vi}}^{\mathrm{i}}(s)$ are in Figure 4.13. As $k_{\mathrm{damp}}^{\mathrm{i}}$ increases in Figure 4.13(a), the dynamic voltage deviation declines gradually, suggesting $k_{\mathrm{damp}}^{\mathrm{i}}$ is of damping and droop coefficient property. From Figure 4.13(b), the recovery speed (grid stiffness) is mainly affected by $k_{\mathrm{svr}}^{\mathrm{i}}$, and larger $k_{\mathrm{svr}}^{\mathrm{i}}$ can strengthen the grid stiffness significantly to shorten the recovery process with the negative effect of reducing damping slightly. In Figure 4.13(c), with the increase of k_{j}, the RoCoV and the overshoot are suppressed, indicating the inertia is enhanced, but v_{out} oscillates longer. Hence, the dynamic response can be optimized by $k_{\mathrm{damp}}^{\mathrm{i}}$, $k_{\mathrm{svr}}^{\mathrm{i}}$ and k_{j} cooperate with each other. Control parameter design can be guided by distributing the pole in a reasonable area or selecting satisfactory step response.

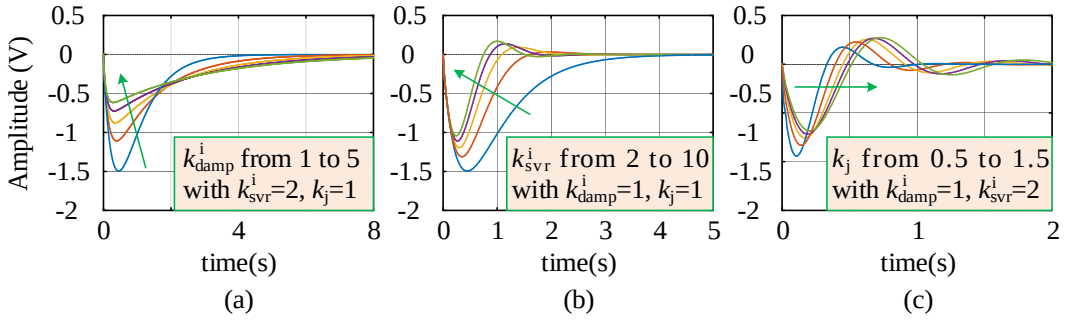


Figure 4.13: The pole distribution of $T_{\mathrm{vv}}^{\mathrm{v}}(s)$ and $T_{\mathrm{vi}}^{\mathrm{v}}(s)$. (a) $k_{\mathrm{damp}}^{\mathrm{i}}$ varying from 1 to 5 with $k_{\mathrm{svr}}^{\mathrm{i}}$=2 and k_{j}=1. (b) $k_{\mathrm{svr}}^{\mathrm{i}}$ varying from 2 to 10 with $k_{\mathrm{damp}}^{\mathrm{i}}$=1 and k_{j}=1. (c) k_{j} varying from 0.5 to 1.5 with $k_{\mathrm{damp}}^{\mathrm{i}}$=1 and $k_{\mathrm{svr}}^{\mathrm{i}}$=2.

4.5 Hardware in the Loop Experiment Verification

The proposed IDC strategies are compared with existing VIDC and validated by dSPACE-based HIL experiment. Referring to the layout of the islanded DC-MG in Figure 4.1, HIL experiment platform is built as shown in Figure 4.14. The control and circuit parameters are listed

in Tables 4.2 and 4.3. It consists of a real time simulator (MicroLabBox), rapid control prototyping module, I/O cables, host computer and an oscilloscope. The DC-MG circuit are deployed in MicroLabBox with a time step of 100μs, while the discrete control algorithm of IDC is implemented by NXP QorlQ P5020 processor to generate the gate signals of all IGBTs and the sampling frequency is 10 kHz. The analog signals and digital signals (state variables and PWM signals) are transferred through I/O interfaces and cables.

Table 4.2 Control parameters of different control strategies

Control strategies	Items	Value
VIDC strategy	Inertia coefficient J_{vir}	10
	Virtual damping D_{damp}	3
	Droop coefficient R_{droop}	2 Ω
Voltage-mode IDC control	Cut-off frequency ω_c	15 rad/s
	Droop coefficient R^v_{d0}	4 Ω
	Virtual damping k^v_{damp}	2
Current-mode IDC control	Inertia coefficient k_j	1
	Virtual damping k^i_{damp}	1
	SVR loop k^i_{svr}	2
	Droop coefficient R^i_{d0} (R_{min}, R_{max})	4 (1.25, 8) Ω
	T	0.01 s
	Time step T_s	100 ns

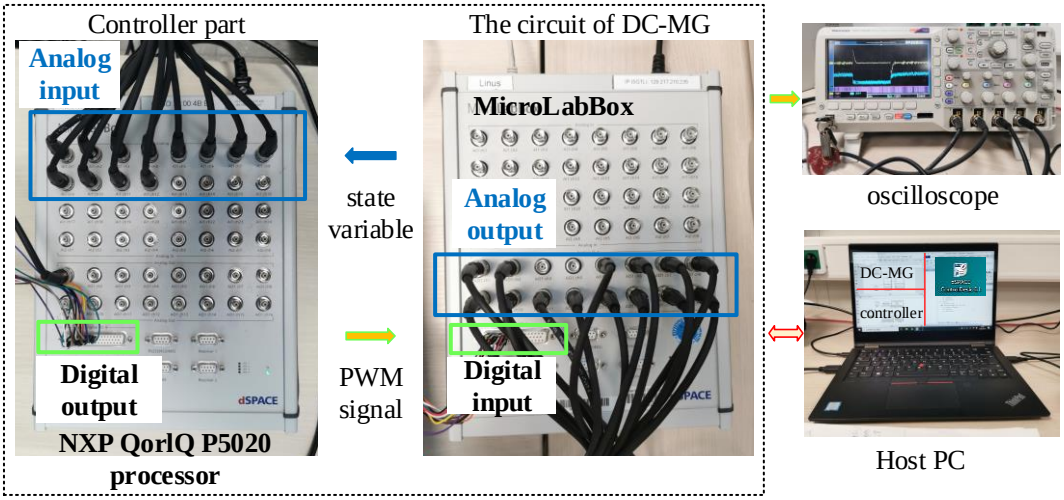


Figure 4.14: The dSPACE-based HIL experiment setup.

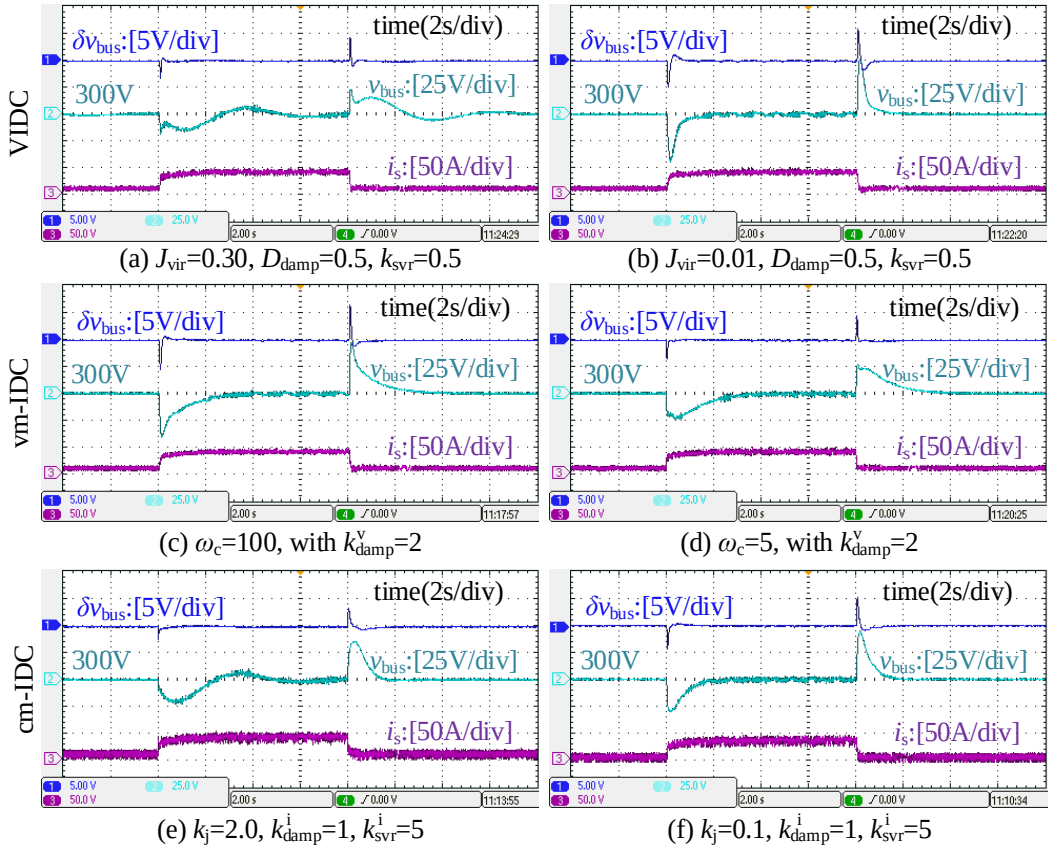
(a) The comparison analysis of IDC methods with VIDC:

The performance comparison analysis of the proposed IDC strategies with the existing VIDC in [84] is considered. When i_{pv}=0A, R=10Ω (P_{const}=1 kW), and EV charging load is changed by P_{dis}=5kW (increasing and then decreasing), corresponding experiment results is shown in Figure 4.15. As observed in Figure 4.15(a) and (b), the RoCoV can be reduced by increasing the J_{vir} in VIDC to improve the inertia and suppress the low-frequency oscillation. Similarly, the

proposed IDC methods has the nature of VIDC by selecting reasonable control parameters according to stability analysis, the inertia and damping are thus enhanced as well as the voltage deviation can be eliminated. Specifically, it can be found from Figure 4.15(c) and (d) that the RoCoV can be also suppressed by decreasing ω_c in vm-IDC. From Figure 4.15(e) and (f), the RoCoV can be reduced by increasing k_j in cm-IDC.

Table 4.3 Circuit parameters of the studied DC-MG

Subsystem	Parameters	Magnitude
Bidirectional DC converter	Input voltage v_{in}	100V
	Input filter inductor L_s/R_s	0.1mH/0.01Ω
	Capacitance C_{out}	3000μF
	Switching frequency	10kHz
Buck converter	Load voltage v_{out_buck}	100V
	Load power P_{const} (R)	2000W(5Ω)
	Input capacitance C_{in}	1200 μF
	Filter inductor L_f/R_f	4 mH/0.01Ω
	Output capacitance C_f	3000 μF
DC bus	DC bus voltage v_{bus}	300 V
	DC bus capacitance C_{bus}	3000 μF
	Line impedance R_{line}/L_{line}	0.01 Ω/0.1 mH



(a) J_{vir}=0.30, D_{damp}=0.5, k_{svr}=0.5 (b) J_{vir}=0.01, D_{damp}=0.5, k_{svr}=0.5

(c) ω_c=100, with k^v_{damp}=2 (d) ω_c=5, with k^v_{damp}=2

(e) k_j=2.0, k^i_{damp}=1, k^i_{svr}=5 (f) k_j=0.1, k^i_{damp}=1, k^i_{svr}=5

Figure 4.15: HIL experiment results of different control strategies. (a) J_{vir}=0.30, D_{damp}=0.5 and k_{svr}=0.5. (b) J_{vir}=0.01, D_{damp}=0.5 and k_{svr}=0.5. (c) ω_c=100 and k^v_{damp}=2. (d) ω_c=5 and k^v_{damp}=2. (e) k_j=2.0, k^i_{damp}=1 and k^i_{svr}=5. (f) k_j=0.1, k^i_{damp}=1 and k^i_{svr}=5.

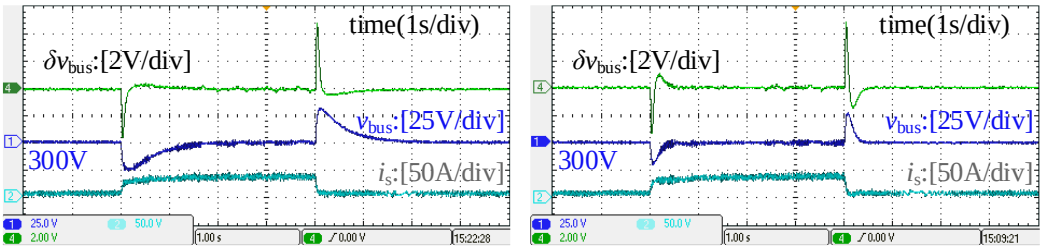
Besides, comparing Figure 4.15(a) with Figure 4.15(d) and (e), it can be observed that VIDC cannot suppress the voltage-loop low-frequency oscillation which lead to the larger RoCoV. An additional compensation control loop is requested to solve this problem. The proposed IDC does not have this problem, which simplifies the control structure even more.

The above experiment results are consistent with the stability analysis. Meanwhile, it is proved that the proposed IDC strategies can achieve the same virtual inertia performance as VIDC by choosing appropriate control parameters to improve inertia and damping.

(b) The power fluctuation form EV charging load:

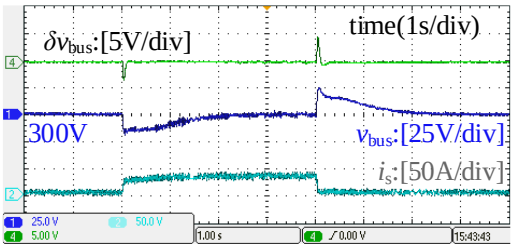
This case aims to study the effect of parameter variation on the dynamic performance in the islanded DC-MG with the proposed IDC methods, when i_{pv}=0A, the initial EV charging load R=10Ω (P_{const}=1 kW), and EV charging load is changed by P_{dis}=5kW (increasing and then de-creasing). Corresponding experiment results of vm-IDC and cm-IDC are shown in Figure 4.16 and 4.17, respectively.

It can be observed from Figure 4.16(c) and (d) that smaller ω_c causes smaller RoCoV and TVN, which indicates the improved inertia and is better for the stability. This is because larger inertia makes v_{out} response slower and thus ESS can supply more inertia power to compensate the unbalanced power. Comparing Figure 4.16(a) and (b), larger k^v_{damp} can obviously decline TVN because of its damping and dynamic droop coefficient properties. And v_{bus} recovers faster and the grid stiffness is enhanced. The static voltage deviation is removed due to the effect of SVR.

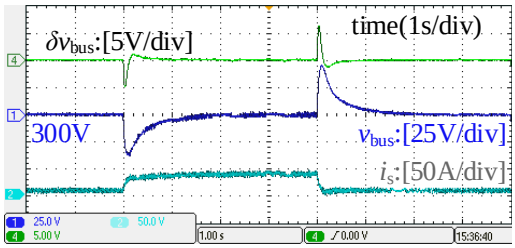


(a) k^v_{damp}=2, with ω_c=10

(b) k^v_{damp}=20, with ω_c=10



(c) ω_c=3, with k^v_{damp}=2



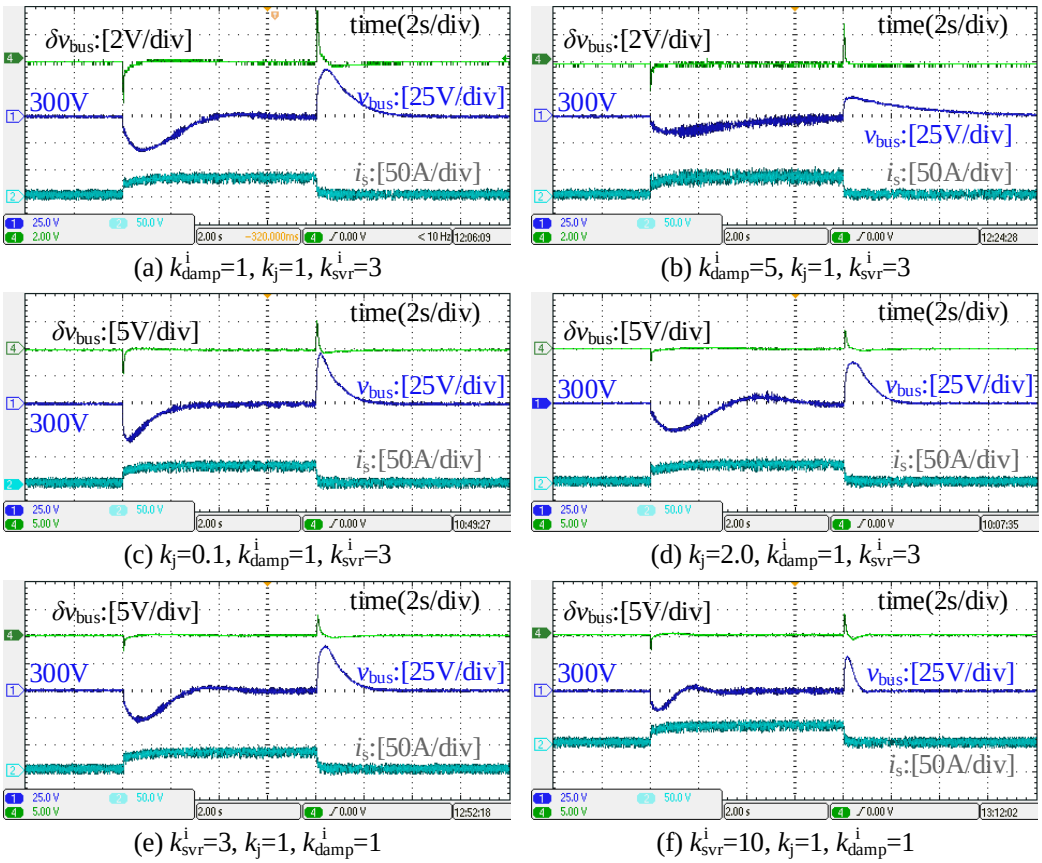
(d) ω_c=70, with k^v_{damp}=2

Figure 4.16: Experiment results of vm-IDC when EV charging load fluctuating. (a) k^v_{damp}=2 and ω_c=10. (b) k^v_{damp}=20 and ω_c=10. (c) ω_c=3 and k^v_{damp}=2. (d) ω_c=70 and k^v_{damp}=2.

From Figure 4.17(c) and (d), larger k_j can increase the system inertia, make v_{out} change slower and reduce oscillation frequency, and thus the oscillation duration is prolonged. It can be concluded from Figure 4.17(a) and (b) that increasing k^i_{damp} can improve the system damping and reduce TVN, revealing its dynamic droop coefficient character. In addition, as depicted in Figure 4.17(e) and (f), growing k^i_{svr} can accelerate the recovery of v_{bus}, representing grid stiffness of rejecting disturbance and eliminating static voltage deviation.

(c) The power fluctuation from PV:

This section studies the effect of parameter variation on the dynamic performance in the islanded DC-MG with the proposed IDC methods, when the initial EV charging load R=10Ω (P_{const}=1 kW), the initial PV output power i_{pv}=25A, and PV is changed by P_{dis}=1kW. Corresponding experiment results of vm-IDC and cm-IDC are shown in Figure 4.18 and 19, respectively. In general, the influence of parameter variations on dynamic performance when the PV generation fluctuates is basically similar to that when the EV charging load fluctuates.



(a) k^i_{damp}=1, k_j=1, k^i_{svr}=3 (b) k^i_{damp}=5, k_j=1, k^i_{svr}=3

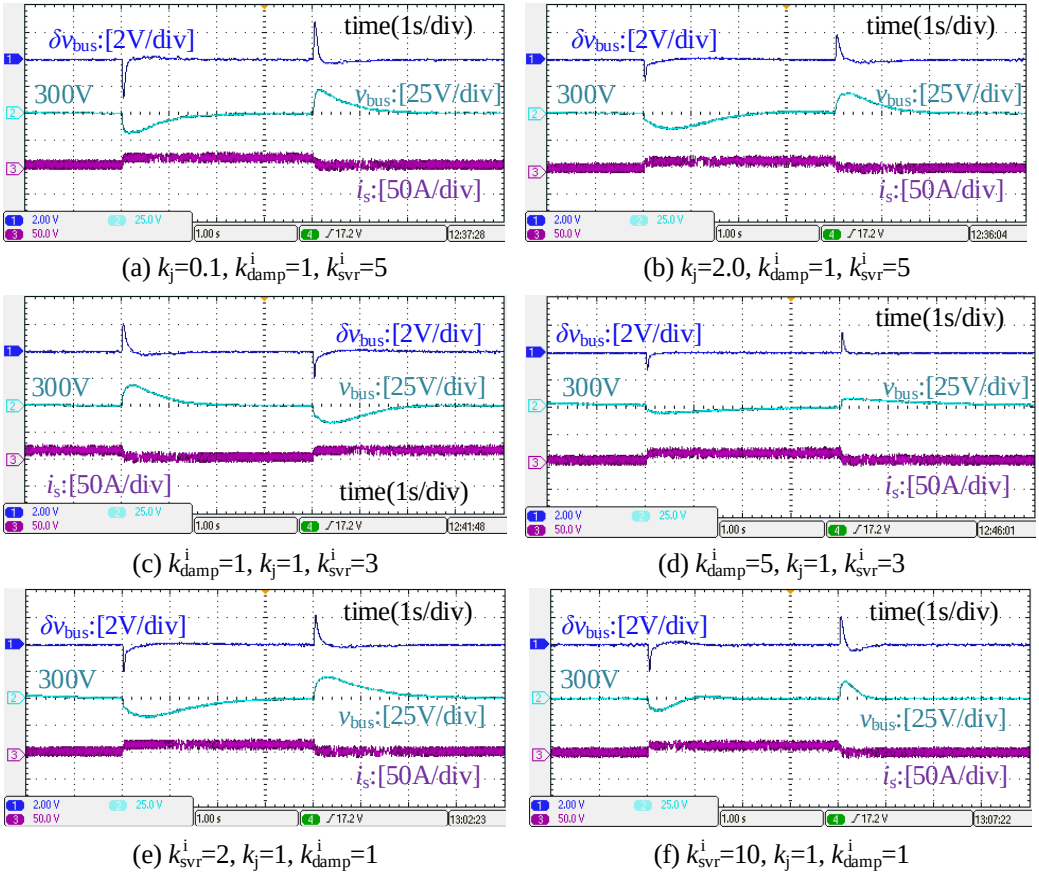
(c) k_j=0.1, k^i_{damp}=1, k^i_{svr}=3 (d) k_j=2.0, k^i_{damp}=1, k^i_{svr}=3

(e) k^i_{svr}=3, k_j=1, k^i_{damp}=1 (f) k^i_{svr}=10, k_j=1, k^i_{damp}=1

Figure 4.17: Experiment results of cm-IDC when EV charging load fluctuating. (a) k^i_{damp}=1, k_j=1 and k^i_{svr}=3. (b) k^i_{damp}=5, k_j=1 and k^i_{svr}=3. (c) k_j=0.1, k^i_{damp}=1 and k^i_{svr}=3. (d) k_j=2.0, k^i_{damp}=1 and k^i_{svr}=3. (e) k^i_{svr}=3, k_j=1 and k^i_{damp}=1. (f) k^i_{svr}=10, k_j=1 and k^i_{damp}=1.

From Figure 4.18(a) and (b), larger k_j can make v_{out} change slower, reduce oscillation frequency and suppress RoCoV (δv_{bus}). It can be seen from Figure 4.18(c) and (d) that increasing k^i_{damp} can improve the system damping and reduce TVN. In addition, as depicted in Figure 4.18(e) and (f), growing k^i_{svr} can eliminate the static voltage deviation and accelerate the recovery of v_{bus}, representing grid stiffness of rejecting disturbance.

It can be obviously seen from Figure 4.19(a) and (b) that larger k^v_{damp} can decline TVN because of its damping properties. In addition, v_{bus} can recover faster to the rated values and the static voltage deviation is removed due to the integral effect of SVR. From Figure 4.19(c) and (d), smaller ω_c can reduce the TVN and make v_{bus} response slower (smaller RoCoV), which indicates the improved inertia and is better for the stability. This is because ESS can supplies more inertia power to compensate the unbalanced power.



(a) k_j=0.1, k^i_{damp}=1, k^i_{svr}=5 (b) k_j=2.0, k^i_{damp}=1, k^i_{svr}=5

(c) k^i_{damp}=1, k_j=1, k^i_{svr}=3 (d) k^i_{damp}=5, k_j=1, k^i_{svr}=3

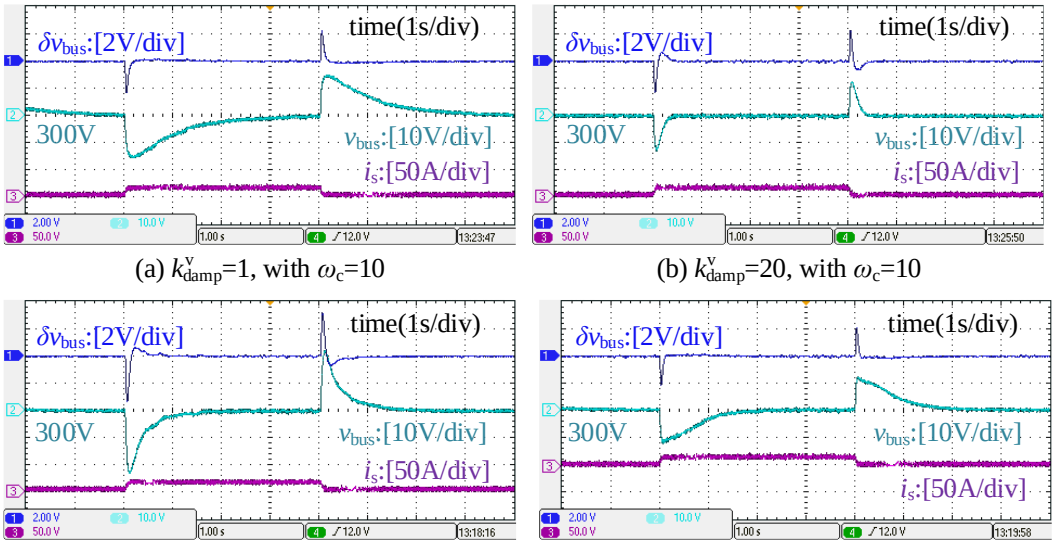
(e) k^i_{svr}=2, k_j=1, k^i_{damp}=1 (f) k^i_{svr}=10, k_j=1, k^i_{damp}=1

Figure 4.18: Experiment results of cm-IDC when PV generation fluctuating. (a) k_j=0.1, k^i_{damp}=1 and k^i_{svr}=5. (b) k_j=2.0, k^i_{damp}=1 and k^i_{svr}=5. (c) k^i_{damp}=1, k_j=1 and k^i_{svr}=3. (d) k^i_{damp}=5, k_j=1 and k^i_{svr}=3. (e) k^i_{svr}=2, k_j=1 and k^i_{damp}=1. (f) k^i_{svr}=10, k_j=1 and k^i_{damp}=1.

(d) The comparison with droop curve swing method:

In this case, the performance comparison analysis of the proposed cm-IDC with the droop curve

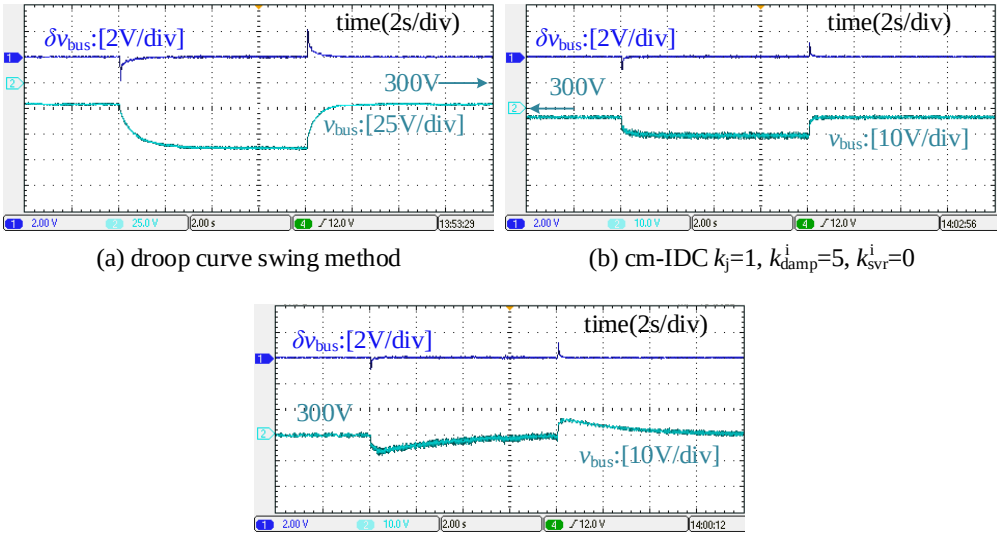
swing method in [90] is carried out, when i_{pv}=0A, the initial EV charging load R=10Ω (P_{const}=1 kW), and EV charging load is changed by P_{dis}=1kW (increasing and then decreasing). The corresponding experiment results is shown in Figure 4.20.



(a) k^{v}_{damp}=1, with ω_c=10 (b) k^{v}_{damp}=20, with ω_c=10

(c) ω_c=100, with k^{v}_{damp}=2 (d) ω_c=3, with k^{v}_{damp}=2

Figure 4.19: Experiment results of vm-IDC when PV generation fluctuating. (a) k^{v}_{damp}=1 and ω_c=10. (b) k^{v}_{damp}=20 and ω_c=10. (c) ω_c=100 and k^{v}_{damp}=2. (d) ω_c=3 and k^{v}_{damp}=2.



(a) droop curve swing method (b) cm-IDC k_j=1, k^{i}_{damp}=5, k^{i}_{svr}=0

(c) cm-IDC, k_j=1, k^{i}_{damp}=5, k^{i}_{svr}=2

Figure 4.20: HIL experiment results of comparison with droop curve swing method. (a) Droop curve swing method. (b) cm-IDC: k_j=1, k^{i}_{damp}=5 and k^{i}_{svr}=0. (c) cm-IDC: k_j=1, k^{i}_{damp}=5 and k^{i}_{svr}=2.

From Figure 4.20(a), the system inertia could be improved to suppress RoCoV by swinging the droop curve with response to the transient voltage variation. However, compared with Figure 4.20(b) and (c), Figure 4.20(a) presents a relatively large steady-state voltage deviation inherent in droop control. According to equation (4.7b), k^{i}_{damp} represents a damping term and has droop

coefficient feature to reduce the voltage deviation, and the SVR loop represented by k_{svr}^{i} can eliminate the steady-state voltage deviation. The corresponding experiment results of cm-IDC are shown in Figure 4.20(b) and (c). It can be concluded from above analysis that the droop curve swing method cannot ensure sufficient damping and remove the steady-state voltage deviation, though the necessary system inertia is provided.

4.6 Summary

In order to enhance the inertia of islanded DC-MG and suppress RoCoV during the occurrence of disturbances, this chapter proposes two types of IDC strategy, based on the conclusion that VIDC is essentially an adaptive droop control with a damping loop, and its inertia and damping come from the DVI and the first-order lag link respectively. Firstly, the principles of inertia response from DVI and variable droop resistance are elaborated, and the damping term is redefined to function as a SVR loop and provide damping. Then, based on the unified modeling of IDC and VIDC, a feedback analysis method is proposed to study stability mechanism from multi-view, and the related analytical tool, i.e., a double-coordinate-based phasor diagram, is developed to identify the influences of feedback variables on control effects and observe the motion of voltage under disturbances. Moreover, dynamic performance is estimated and small-signal stability analysis is given for parameter design. Finally, the dSPACE-based HIL experiment validates the theoretical analysis and proposed methods. The main contributions and findings are summarized as follows.

1. According to the equivalent model of VIDC, vm- and cm-IDC methods are proposed. DVI is remained in vm-IDC to provide inertia while an adaptive droop algorithm is introduced in the cm-IDC for inertia provision by droop curve swing. The damping term is redefined to function as a SVR loop and provide damping.

2. Under the premise of mitigating LFO and reducing RoCoV like VIDC, IDC methods can be more easily implemented on the basis of droop control. And the control structure is thus simplified because there is no need to add a controller or observer.

3. It can be concluded from stability mechanism analysis that IDC is of NF with PD, and C_v, L_{svr} and k_{damp} reflect system inertia, stiffness and dissipation properties in phasor diagram, respectively. In the vm-IDC, the virtual inertia is affected by the LPF bandwidth ω_c, and the damping and stiffness are affected by the damping coefficient k_{damp}^{v}, while in the cm-IDC, the inertia, damping and stiffness are represented by k_j, k_{damp}^{i}, and k_{svr}^{i}.

4. From the experiment analysis, decreasing the LPF bandwidth ω_c in the vm-IDC can increase

the system inertia to mitigate the RoCoV, as well as the TVN decreases and the voltage can recover faster because increasing $k_{\mathrm{damp}}^{\mathrm{v}}$ can improve the system damping. On the other hand, increasing k_{j} in the cm-IDC can reduce RoCoV and suppress LFO, $k_{\mathrm{damp}}^{\mathrm{i}}$ mainly affects the oscillation amplitude, while larger $k_{\mathrm{svr}}^{\mathrm{i}}$ can speed up the restoration of v_{bus} to its nominal value.

5 Low-Frequency Oscillation Analysis of Virtual-Inertia-Controlled DC-MG based on Multi-timescale Impedance Model

In addition to the instability risk caused by the negative impedance characteristic of constant power loads (CPLs), the inertia-less property originating from the replacement of rotational machines by power electronic converters also poses a great challenge to the voltage stability of islanded DC microgrids (DC-MGs). As a promising solution, the virtual inertia and damping control based DC-MG (VIDC-DC-MG) has been developed and studied to solve the problems caused by CPLs and the lack of inertia at the same time. Its essence is adding a virtual capacitance to suppress the rate of change of voltage (RoCoV). However, the stability mechanism of virtual inertia and damping control (VIDC), the influence of CPLs on VIDC, and the low-frequency oscillation (LFO) of VIDC-DC-MG with a clear physical significance are less investigated. Besides, there is a lack of proper analysis tool to identify the potential instability factors (the roots of underdamped and unstable modes) of VIDC-DC-MG although VIDC could maintain the stable operation of islanded DC-MG.

To address the aforementioned problem of lacking suitable modeling tool for LFO analysis in VIDC-DC-MG, this chapter proposes a multi-timescale impedance modeling framework as the bridge between white-box and black-box modeling by combining the advantages of the impedance model and the state-space model. The traditional impedance model is expanded to an *impedance circuit* composed of *loop virtual impedances* (LVIs) that visualize the abstract control loops within different bandwidths. The multi-timescale impedance model with gray-box model property could be converted into a white-box or black-box model, according to the analysis necessity. This multi-timescale impedance modeling method is proposed based on the idea of equating the control loops as virtual impedances, thus, this modeling and analysis method can be extended to AC microgrid, as a universal modeling method.

The interaction stability mechanism and the optimization of stabilization control of VIDC-DC-MG are explored systematically in this chapter. In addition to the establishment and analysis of the multi-timescale impedance model, more comprehensive and in-depth investigation has been

performed on the low-frequency oscillation mechanism, the physical interpretation of the control process, the identification of instability factors, and the stability enhancement methods.

This chapter focuses on the mechanism analysis and mitigation method of low-frequency oscillations. Control loops of different timescales are visualized as independent LVIs in this modeling framework, and the interaction between control loops is interpreted by the interconnection of LVIs. This intuitive impedance model reflects the system dynamics at different timescales. The impedance properties (i.e., resistive, capacitive, inductive) of the control loops/parameters and their impedance-shaping effects are illustrated at different timescales by simplifying the LVIs to *RLC* models in different bandwidths. Hence, the control parameters are given a clear physical meaning. The derived *RLC* circuit reveals the *LC* impedance interaction in different bandwidths and explains the low-frequency oscillation in the voltage-loop and inertia-loop bandwidths emphatically. Moreover, the instability factors are discovered by fully identifying the non-passive region of LVIs. Thus, a dynamic stability enhancement method is proposed to cancel the non-passive impedance and improve the high frequency inertia. The stability of VIDC-DC-MG is assessed by the impedance passivity.

The content of this chapter has been published in "*IEEE transaction on sustainable energy*" [M1].

5.1 DC-MG Description and Discussion about VIDC

5.1.1 System configuration

On the basic of Figure 1.1, a typical diagram of islanded DC-MG is shown in Figure 5.1, mainly including four different types of components, i.e., photovoltaics (PV) unit, one energy storage system (ESS), CPL and constant current load (CCL). It is worth noting that this research focuses on the islanded DC-MG with only one single ESS, and the dynamic stability of multi-parallel ESS will be carried out in the future. PV is connected to the DC bus with boost converter and $P_{pv}(i_{pv})$ is its generation power. CPL and CCL are connected to the DC bus with buck converters. The circuit of boost and buck converters can be obtained from literature [54]. P_{cpl} and P_{ccl} refer to their consuming power. Normally, ESS is composed of battery and employs bidirectional dc converter (BiC, i.e., the b-BiC in Figure 5.1) for charging and discharging [54]. P_{out} is ESS's output power. Positive/negative P_{out} refer to discharging/charging modes. The circuit parameters are from [54].

Most of the terminals are connected to DC bus via power electronic converters, resulting in the system low inertia and poor damping. DC voltage oscillates or becomes unstable when the

islanded DC-MG suffers from power fluctuation from PV or CPL. Therefore, VIDC is proposed to improve the dynamic stability and reduce the rate of change of voltage (RoCoV) by taking full advantage of ESS's inertia support capacity.

In order to take good use of the complementary advantages of battery and super-capacitor (SC) in energy and power density, SC is added in Figure 5.1 to constitute hybrid-ESS (HESS). Hence, the traditional VIDC's shortcoming (i.e., only absorbing low-frequency power fluctuation) is overcome. SC is also connected to the DC bus via BiC (the SC-BiC of Figure 5.1). The control and mathematical model of SC-BiC will be presented later.

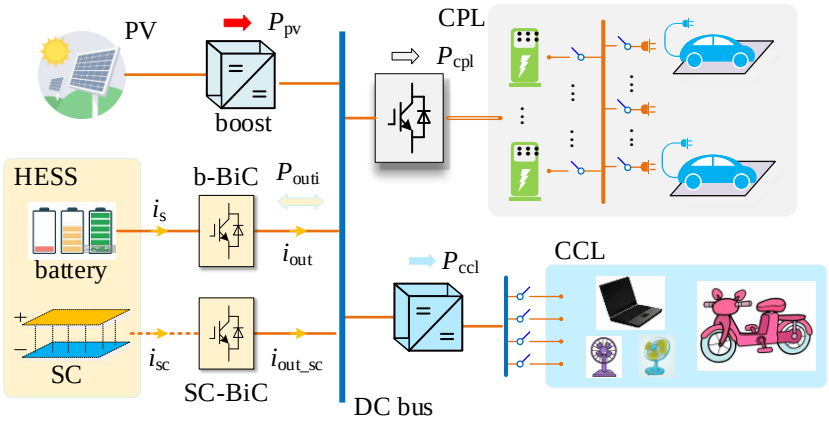


Figure 5.1: The layout of the studied islanded DC-MG.

5.1.2 Virtual inertia and damping control

Figure 5.2 depicts the circuit of b-BiC and the structure of VIDC. It is worth noting that SC-BiC has the same circuit structure as b-BiC, but the control method of SC-BiC is different, which will be introduced in detail in ***Section 5.3***.

v_{in} and i_s are the input voltage and current, v_{out} and i_{out} are the output voltage and current. L_s and R_s are the filter inductor and its parasitic resistance, C_{out} is the filter capacitor. v_{dcn} is the rated value of DC bus voltage.

$$\frac{(v_{\mathrm{dcn}}-v_{\mathrm{out}})}{R_{\mathrm{di}}}-i_{\mathrm{out}}-i_{\mathrm{vd}}-i_{\mathrm{svr}}=J_{\mathrm{vir}}\frac{\mathrm{d}(v_{\mathrm{ref}}-v_{\mathrm{dcn}})}{\mathrm{d}t} \tag{5.1a}$$

$$\text{damping component: } i_{\mathrm{vd}}=k_{\mathrm{vd}}(v_{\mathrm{ref}}-v_{\mathrm{out}}) \tag{5.1b}$$

$$\text{inertia component: } i_{\mathrm{iner}}=J_{\mathrm{vir}}\frac{\mathrm{d}(v_{\mathrm{ref}}-v_{\mathrm{dcn}})}{\mathrm{d}t} \tag{5.1c}$$

$$\text{stiffness component: } i_{\mathrm{svr}}=k_{\mathrm{svr}}\int(v_{\mathrm{ref}}-v_{\mathrm{dcn}})\mathrm{d}t \tag{5.1d}$$

VIDC has been proposed to improve voltage stability, including droop control, virtual inertia

loop and dual loop control [84]. The inertia control equation is in (5.1). R_d is a virtual resistance simulating the droop characteristics. $G_v(s)$ and $G_i(s)$ are the voltage- and current-loop controller. G_{pwm}=1/300 is the modulation gain. d is the duty ratio and v_{ref} is the voltage-loop instruction. J_{vir} and k_{vd} is the introduced inertia coefficient and damping coefficient to enlarge the equivalent DC capacitor and improve dissipation characteristics. Based on the circuit equivalence that inductor behaves as short circuit at long-time scale while open circuit at short-time scale, a secondary voltage recovery (SVR) loop is proposed, as shown in (5.1d), to enhance the system stiffness and remove the steady-state voltage difference caused by R_d. k_{svr} is the stiffness coefficient. The control and circuit parameters are shown in Tables 5.1 and 5.2, which are referred from Ref. [54]. The bandwidth of the current-, voltage- and inertia-loop are set as ω_c= 1160rad/s, ω_v^b=167rad/s, and ω_{iner}≈10rad/s. However, low-frequency oscillation still exists, though VIDC is adopted.

Table 5.1 Control parameters of VIDC strategies

Control loop	Items	Value
VIDC	Inertia coefficient J_{vir}	0.05
	Virtual damping k_{vd}	0.5
	Stiffness coefficient k_{svr}	0.75
voltage-loop controller $G_v(s)$	Proportional gain k_{vp}	1
	Integral gain k_{vi}	10
current-loop controller $G_i(s)$	Proportional gain k_{ip}	5
	Integral gain k_{ii}	20

Table 5.2 System parameters of the studied islanded DC-MG

Subsystem	Parameters	Magnitude
Bidirectional DC converter	Input voltage v_{in}	100V
	Input filter inductor L_s/R_s	0.1mH/0.01Ω
	Capacitance C_{out}	3000μF
	Switching frequency	10kHz
Buck converter	Load voltage v_{out_buck}	100V
	Load power P_{cpl} (R)	2000W(5Ω)
	Input capacitance C_{in}	1200 μF
	Filter inductor L_f/R_f	4 mH/0.01Ω
	Output capacitance C_f	3000 μF
DC bus	DC bus voltage v_{bus}	300 V
	DC bus capacitance C_{bus}	3000 μF
	Line impedance R_{line}/L_{line}	0.01 Ω/0.1 mH

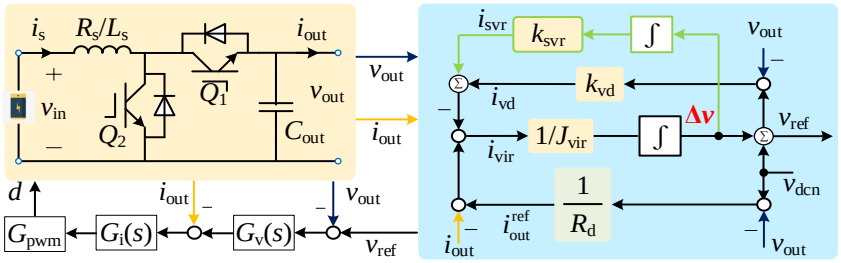


Figure 5.2: The circuit of b-BiC and its VIDC strategy.

5.1.3 Equivalent two-terminal model of islanded DC-MG

It can be observed from Figure 5.1 that the studied islanded DC-MG is composed of four units, i.e., the PV unit, the ESS, the CCL unit and the CPL unit. Generally, this DC-MG can be equivalent to a source-load two terminal system [115]. ***(1)*** 'Load' terminal refers to the PV unit in power control mode, the CCL unit and the CPL unit. ***(2)*** 'Source' terminal refers to the ESS.

(a) the mathematical model of 'load' terminal units:

PV and CCL units: The mathematical models of PV and CCL are current sources i_{pv} and i_{ccl}.

CPL unit: The power characteristic of CPL is

$$P_{\mathrm{cpl}} = v_{\mathrm{out}} \cdot i_{\mathrm{cpl}} \tag{5.2}$$

where i_{cpl} is the input current of CPL.

Using the 1st-order Taylor series, (5.2) is expanded into (5.3).

$$i_{\mathrm{cpl}} = 2 \cdot \frac{P_{\mathrm{cpl}}}{V_{\mathrm{out}}} - \frac{P_{\mathrm{cpl}}}{V_{\mathrm{out}}^2} \cdot v_{\mathrm{out}} \tag{5.3a}$$

$$i_{\mathrm{cpl}} = I_{\mathrm{cpl}} + \Delta i_{\mathrm{cpl}} = \frac{P_{\mathrm{cpl}}}{V_{\mathrm{out}}} - \frac{P_{\mathrm{cpl}}}{V_{\mathrm{out}}^2} \cdot \Delta v_{\mathrm{out}} \tag{5.3b}$$

$$I_{\mathrm{cpl}} = \frac{P_{\mathrm{cpl}}}{V_{\mathrm{out}}}, \quad R_{\mathrm{cpl}} = \frac{\Delta v_{\mathrm{out}}}{\Delta i_{\mathrm{cpl}}} = -\frac{V_{\mathrm{out}}^2}{P_{\mathrm{cpl}}} \tag{5.3c}$$

where I_{cpl} and V_{out} are the steady-state current and voltage. R_{cpl} is the small-signal impedance of CPL, a negative incremental impedance. Define 'Δ' as the small-signal term of each variable.

(b) the mathematical model of 'source' terminal unit:

The 'source' terminal represents the bus voltage regulation, i.e., the b-BiC, which is essentially a controlled voltage source with multi-timescale impedance reshaped by control loops.

According to the small-signal model of b-BiC in literature [84], the transfer function between i_{out} and d can be deduced as shown in (5.4). According to the control diagram of b-BiC shown in Figure 5.2 and equation (5.4), b-BiC can be equivalent to a controlled current source, that is, the mathematical model of the 'source' terminal in Figure 5.3(a).

$$G_{\mathrm{id}}(s) = \frac{\Delta i_{\mathrm{s}}}{\Delta d} = \frac{C_{\mathrm{out}} v_{\mathrm{dcn}} s + (1-D) I_{\mathrm{s}}}{L_{\mathrm{s}} C_{\mathrm{out}} s^2 + R_{\mathrm{s}} C_{\mathrm{out}} s + (1-D)^2} \tag{5.4}$$

Since there is only one ESS in the studied DC-MG to maintain bus voltage balance, according to Kirchhoff's current law, the output current of 'source' terminal (b-BiC) is the sum of the currents of the other three units, that is, $i_{out}=i_{ccl}+i_{cpl}-i_{pv}$.

Subsequently, based on the mathematical model of these four units, the equivalent two-terminal model can be obtained, as shown in Figure 5.3(a). μ=1/3 is the ratio of i_{out} to i_s.

To facilitate the derivation of multi-timescale impedance model, some simplifications have been made to Figure 5.3(a):

- Loop 1 in Figure 5.3(a) is changed into loops i and ii in Figure 5.3(b).
- In order to study the influence of CPL on the 'source' terminal, the small-signal component of CPL Δi_{cpl} is separated from the output current i_{out}. According to equation (5.3b), the current introduction nodes have been modified as shown in the Figure 5.3(b).

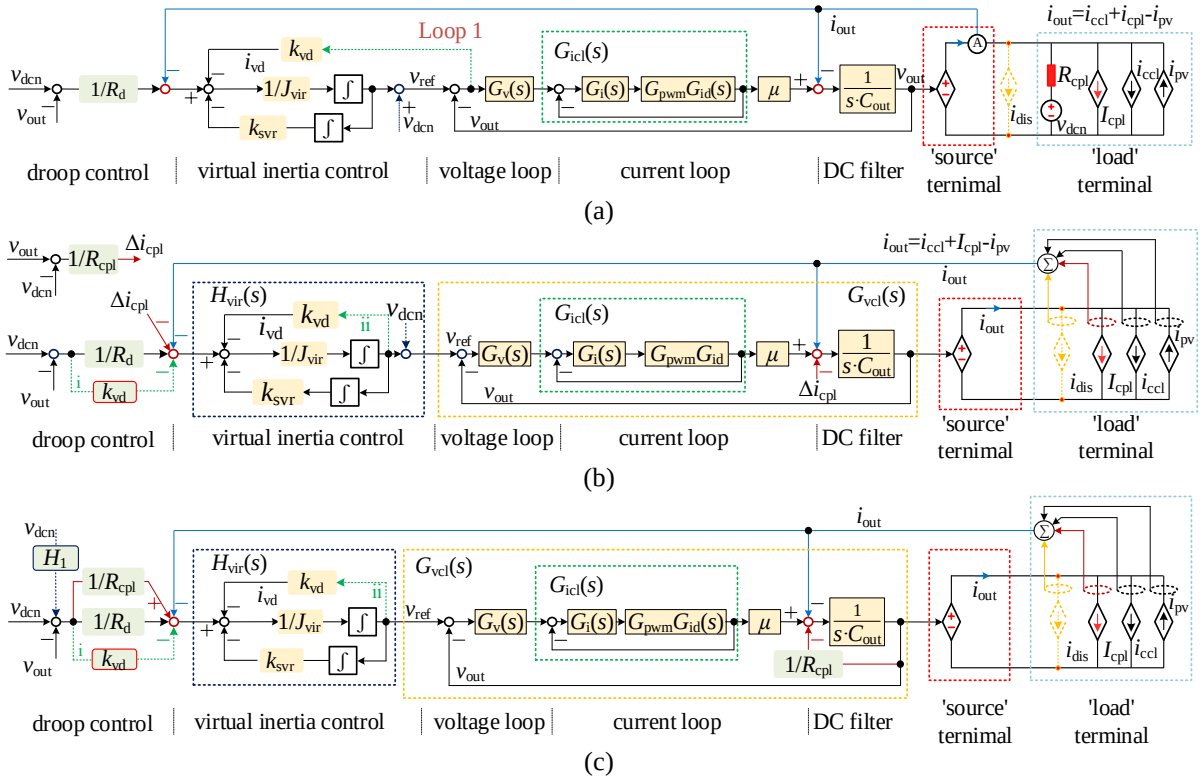


Figure 5.3: Equivalent two-terminal model of DC-MG considering CPL. (a) Original model. (b) Assigning CPL to 'source' terminal. (c) Simplified model.

After the modification, the branch of R_{cpl} is rearranged into the 'source' terminal. Correspondingly, the output current of 'source' terminal is redefined as: $i_{out}=i_{ccl}+I_{cpl}-i_{pv}$. The simplified two-terminal model is shown in Figure 5.3(b).

According to $\Delta i_{cpl}=\Delta v_{out}/R_{cpl}$, Figure 5.3(b) is further simplified Figure 5.3(c). The v_{dcn} branches in the inertia- and current-loop (introduced by R_{cpl}) arranged into the droop loop, thus a transfer function $H_1(s)$ is generated, as expressed in (5.5a).

From Figure 5.3, $H_{vir}(s)$ is the inertia-loop transfer function, as shown in (5.5b) and (5.5c). The inertia loop is changed by SVR from a 1st-order loop into a 2nd-order loop, and its impact on

low-frequency oscillation is analyzed in **Section 5.2**.

$$H_1(s) = \frac{1}{\left(\frac{1}{R_\mathrm{d}} - k_\mathrm{vd} + \frac{1}{R_\mathrm{cpl}}\right) H_\mathrm{vir}} + \frac{1}{\mu \cdot R_\mathrm{cpl} \cdot \left(\frac{1}{R_\mathrm{d}} - k_\mathrm{vd} + \frac{1}{R_\mathrm{cpl}}\right) H_\mathrm{vir} G_\mathrm{v} G_\mathrm{icl}} \tag{5.5a}$$

$$H_\mathrm{vir}(s) = s/(s^2 J_\mathrm{vir} + s k_\mathrm{vd} + k_\mathrm{svr}), \qquad \text{with SVR} \tag{5.5b}$$

$$H_\mathrm{vir}^\mathrm{T}(s) = 1/(k_\mathrm{vd} + s J_\mathrm{vir}), \qquad \text{without SVR} \tag{5.5c}$$

5.2 Multi-timescale Impedance Modelling

In this section, the multi-timescale impedance model is derived and it consists of discrete LVI elements reflecting the impedance-shaping effect of control loops. The non-passive region of LVI is identified and the physical nature of control loops/parameters (stability mechanism) is interpreted by fully analyzing the impedance characteristics of each LVI. The low-frequency oscillation is illustrated by *LC* interaction of different timescales and dynamic coupling among different timescales.

5.2.1 Methodology: mapping between virtual impedance and controlled-source

The essence of b-BiC is a controlled voltage source and its output impedance shaped by control loops describes external dynamics. State variables, fed back to different control loops, would make control loops equivalent to virtual impedances and affect the system stability at various timescales.

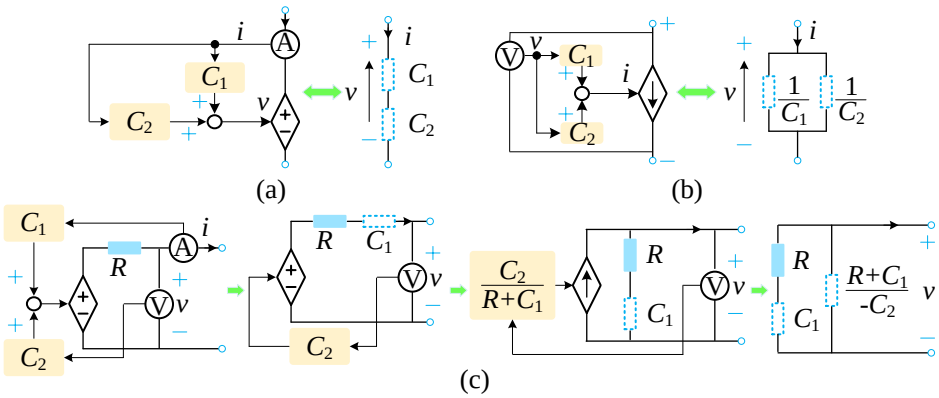


Figure 5.4: Equivalent virtual impedance of controlled source. (a) Self-controlled voltage source. (b) Self-controlled current source. (c) General example.

The virtual impedance of controlled source is discussed firstly, which is regarded as the methodology for multi-timescale virtual impedance modelling. The impedance characteristics of

controlled source is shown in Figure 5.4(a) and (b). On the basis of Ohm's law and Superposition theorem, a self-current-controlled voltage source can be converted into series impedances, while a self-voltage-controlled current source can be equivalent to a parallel admittance. Based on these fundamental cases, a more general example is explained in Figure 5.4(c): the equivalent impedance derivation of an external-voltage-and-current-controlled voltage source. According to Ohm's law, Superposition theorem, Norton's theorem and Thevenin's theorem, it is derived step-by-step into a series-parallel-form impedance. Similarly, the control loops of b-BiC can converted into virtual impedances connected in series or in parallel at the output port and their position depends on the feedback variables. They affect voltage stability at different timescales due to their different origination in control system.

5.2.2 Derivation and analysis of multi-timescale impedance

The accurate multi-timescale impedance model of VIDC-DC-MG is established. Dynamic characteristics of each loop is presented by analyzing relevant LVIs. The significance and function of control parameters are clarified from impedance-reshaping perspective, and the low-frequency oscillation is explained from *LC*-interaction view.

(a) voltage-loop virtual impedance model:

According to the equivalent source-load two-terminal model of DC-MG in Figure 5.3, the voltage-loop mathematical model is shown in Figure 5.5(a). First, the controlled voltage source model of b-BiC in Figure 5.5(a) is transformed to **a controlled current source model**, as shown in Figure 5.5(b). The closed current-loop gain $G_{\mathrm{icl}}(s)$ is derived as (5.6a). It can be seen from Figure 5.5(b) that CPL is equivalent to a negative resistance R_{cpl} in parallel with the output capacitor C_{out}. Subsequently, the derivation of voltage-loop virtual impedance is illustrated in Figure 5.5(c).

From Figure 5.5(c), the voltage-controlled b-BiC is represented as a Norton equivalent source: a current source $v_{\mathrm{ref}}{\cdot}Y_{\mathrm{vl}}(s)$ in parallel with the voltage-loop virtual impedance $Z_{\mathrm{vcl}}(s)$, as represented by (5.6b). It can be concluded from Figure 5.5(c) and (5.6b) that the voltage-loop virtual impedance $Z_{\mathrm{vcl}}(s)$ is the parallel connection of $Y_{\mathrm{vl}}(s)$, C_{out} and R_{cpl}, expressed as (5.6c). In order to facilitate the low-frequency oscillation mechanism analysis, the parallel connection of $Y_{\mathrm{vl}}(s)$ and the output capacitor C_{out} is redefined as the sub-impedance $Z_{\mathrm{v}}(s)$ of $Z_{\mathrm{vcl}}(s)$, as shown in (5.6d), which is a generalized parallel *RLC* model restrained by the $G_{\mathrm{icl}}(s)$. The passive branches of this generalized *RLC* model are R_{v}, L_{v} and C_{v}. Correspondingly, voltage-loop controller $G_{\mathrm{v}}(s)$ is mapped to the virtual admittance component $Y_{\mathrm{vl}}(s)$ of $Z_{\mathrm{v}}(s)$, as shown in (5.6e), adding a

resistor R_v given by k_{vp} and an inductor L_v given by k_{vi}.

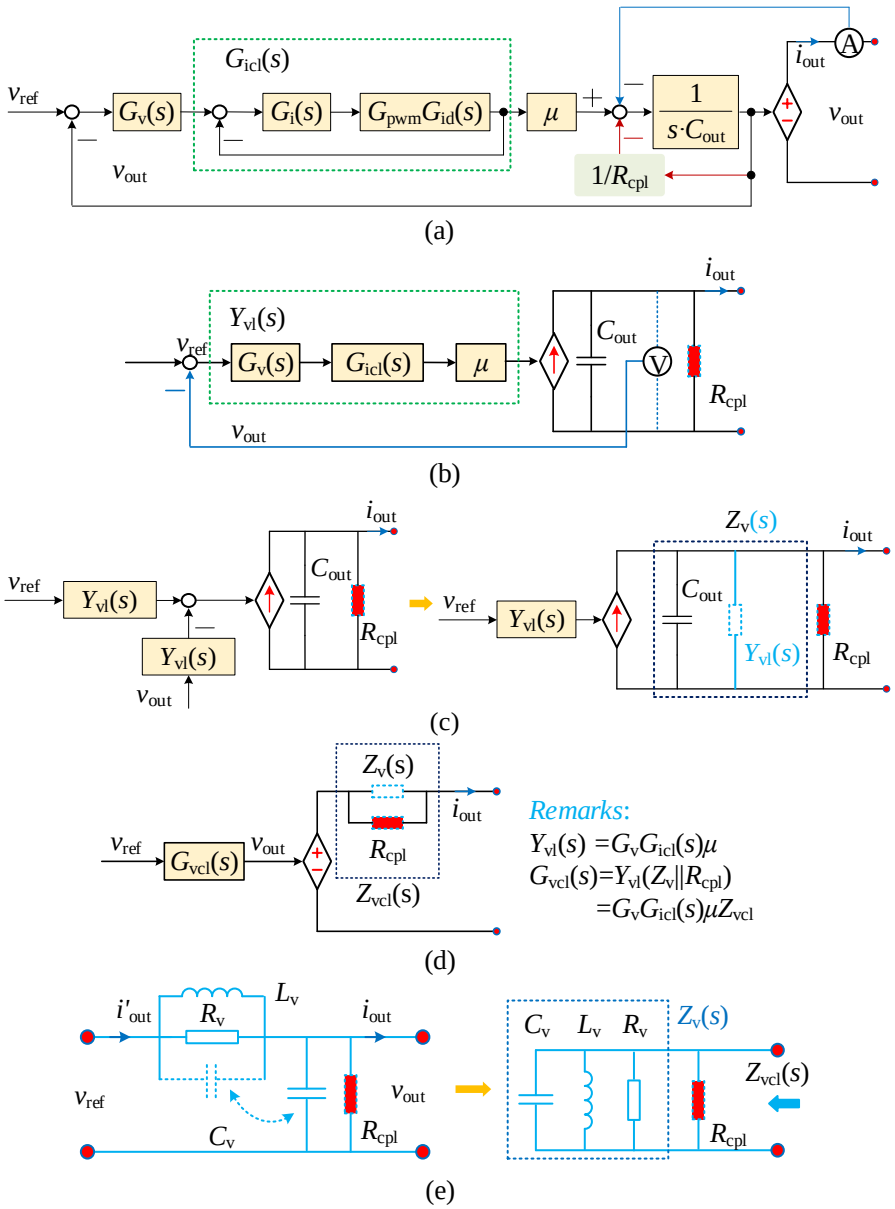


Figure 5.5: Derivation of voltage-loop virtual impedance model and its *RLC* model. (a) Voltage-loop mathematical model. (b) Norton equivalent model. (c) Virtual impedance derivation. (d) Thevenin equivalent model. (e) *RLC* circuit.

$$G_{icl}(s) = \frac{G_i(s)G_{pwm}G_{id}(s)}{1 + G_i(s)G_{pwm}G_{id}(s)} \tag{5.6a}$$

$$i_{out} = v_{ref}Y_{vl}(s) - v_{out}Y_{vl}(s) - C_{out}\frac{dv_{out}}{dt} - \frac{v_{out}}{R_{cpl}} = v_{ref}Y_{vl} - \frac{v_{out}}{Z_{vcl}} \tag{5.6b}$$

$$Z_{vcl} = Y_{vl}(s) \,||\, sC_{out} \,||\, R_{cpl} = Z_v(s)||R_{cpl} \tag{5.6c}$$

$$Z_v(s) = \frac{1}{Y_{vl}(s)||sC_v} = \frac{1}{\mu k_{vp}G_{icl}(s) + \frac{k_{vi}\mu G_{icl}(s)}{s} + sC_v} = \frac{1}{\frac{1}{R_v} + \frac{1}{sL_v} + sC_v} \tag{5.6d}$$

$$Y_{\mathrm{vl}}(s)=\mu k_{\mathrm{vp}}G_{\mathrm{icl}}(s)+\frac{k_{\mathrm{vi}}\mu G_{\mathrm{icl}}(s)}{s}=\frac{1}{R_{\mathrm{v}}}+\frac{1}{sL_{\mathrm{v}}} \tag{5.6e}$$

On the basis of Figure 5.5(c), the voltage-controlled b-BiC is further transformed into a **Thevenin equivalent circuit**: a voltage source in series with voltage-loop virtual impedance $Z_{\mathrm{vcl}}(s)$, as shown in Figure 5.5(d). The output voltage can be represented by (5.7a), where $G_{\mathrm{vcl}}(s)$ is the voltage closed-loop gain as shown in (5.7b).

Within the voltage-loop bandwidth, current loop can be equivalent to a unity-gain loop $G_{\mathrm{icl}}(s)\approx 1$, and $Z_{\mathrm{v}}(s)$ can be thus simplified into a generic parallel *RLC* model. The related passive elements of *RLC* circuit can be expressed as (5.7c). Accordingly, the voltage-loop virtual impedance $Z_{\mathrm{vcl}}(s)$ can be expressed as passive elements, as depicted in Figure 5.5(e).

$$v_{\mathrm{out}}=v_{\mathrm{ref}}G_{\mathrm{vcl}}(s)-i_{\mathrm{out}}Z_{\mathrm{vcl}}(s) \tag{5.7a}$$

$$G_{\mathrm{vcl}}(s)=Y_{\mathrm{vl}}(s)Z_{\mathrm{vcl}}(s)=G_{\mathrm{v}}(s)G_{\mathrm{icl}}(s)\mu Z_{\mathrm{vcl}}(s) \tag{5.7b}$$

$$R_{\mathrm{v}}=\frac{1}{\mu k_{\mathrm{vp}}G_{\mathrm{icl}}(s)}\approx\frac{1}{\mu k_{\mathrm{vp}}},L_{\mathrm{v}}=\frac{1}{k_{\mathrm{vi}}\mu G_{\mathrm{icl}}(s)}\approx\frac{1}{\mu k_{\mathrm{vi}}},C_{\mathrm{v}}=C_{\mathrm{out}} \tag{5.7c}$$

As displayed in Figure 5.5(e) and equation (5.7c), the voltage-loop controller interacts with the output capacitor C_{out} to generate a LFO mode within voltage-loop bandwidth, as well as the parallel negative resistance R_{cpl} given by CPL is of negative damping property, can reduce the voltage-loop damping, and exacerbate LFO. Hence, the interaction between the voltage loop controller and the output capacitor is the leading cause of voltage-loop LFO. The analysis of $Z_{\mathrm{v}}(s)$ is conducted while R_{cpl} is regarded as a reducing-damping factor.

Accordingly, the voltage-loop control effect is elaborated from impedance-shaping perspective, as shown in Figure 5.5(e). The circuit equivalence of inductor is shown in (5.8) that inductor behaves as short circuit in long-time limit and is an open circuit in short-time limit. When i_{out} rises by Δi_{out} due to power disturbance, L_{v} is an open circuit in short-time limit. v_{out} will drop by $\Delta v_{\mathrm{out}}=\Delta i_{\mathrm{out}}\cdot R_{\mathrm{v}}$, so that $i_{\mathrm{out}}^{'}$ will increase to compensate power mismatch. $R_{\mathrm{v}}(1/k_{\mathrm{vp}})$ determines the amplitude of Δv_{out} under the same Δi_{out}. In the long-time limit, L_{v} is short circuit and i_{out} shifts from R_{v} to L_{v} path, so that the voltage deviation is eliminated. Based on (5.9b), decreasing $L_{\mathrm{v}}(1/k_{\mathrm{vi}})$ speeds up the dynamic process with the same R_{v}. Although smaller R_{v} limits the voltage fluctuations amplitude Δv_{out}, it will also extend the adjustment time. Thus, $Z_{\mathrm{v}}(s)$ ensures v_{out} quickly tracks v_{ref}.

$$\begin{cases} t\to\infty\colon \lim\limits_{s\to 0} sL_{\mathrm{v}}=0, & \text{short circuit} \\ t\to 0\colon \lim\limits_{s\to\infty} sL_{\mathrm{v}}=\infty, & \text{open circuit} \end{cases} \tag{5.8}$$

$$\Delta v_{\mathrm{out}}=\Delta i_{\mathrm{out}}\cdot R_{\mathrm{v}} \tag{5.9a}$$

$$\Delta i_{\mathrm{out}} \approx \frac{\int \Delta v_{\mathrm{out}}\,\mathrm{d}t}{L_{\mathrm{v}}} = \frac{\int \Delta i_{\mathrm{out}} \cdot R_{\mathrm{v}}\,\mathrm{d}t}{L_{\mathrm{v}}} \rightarrow \Delta t \approx \frac{L_{\mathrm{v}}}{R_{\mathrm{v}}} \tag{5.9b}$$

The frequency response of $Z_{\mathrm{v}}(s)$, its *RLC* model and $G_{\mathrm{vcl}}(s)$ is shown in Figure 5.6. From Figure 5.6(a), the dashed line represents the generic *RLC* model, i.e., $Z_{\mathrm{v}}(s)$ ignoring the current-loop gain. As shown in Figure 5.6(a), the bode plot of voltage-loop virtual impedance $Z_{\mathrm{v}}(s)$ is consistent with that of its *RLC* model within the voltage-loop bandwidth, which proves the accuracy of the *RLC* model. The theoretical explanation is that $G_{\mathrm{icl}}(s)$ can be ignored at voltage-loop timescale (i.e., $G_{\mathrm{icl}}(s)\approx 1$ holds).

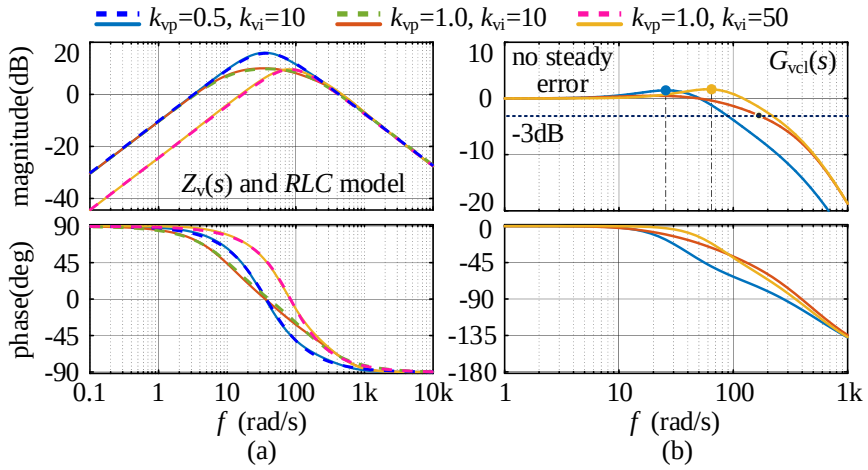


Figure 5.6: Frequency response analysis of voltage loop. (a) $Z_{\mathrm{v}}(s)$ and *RLC* model. (b) $G_{\mathrm{vcl}}(s)$.

From Figure 5.6(a), the $L_{\mathrm{v}}C_{\mathrm{v}}$ impedance interaction induces low-frequency oscillation at voltage-loop timescale. The oscillation frequency ω_{v} can be obtained from (5.10). Increasing k_{vp} can suppress the peak value of $Z_{\mathrm{v}}(s)$, thereby reducing Δv_{out} caused by power disturbance. k_{vi} affects the inductive component of $Z_{\mathrm{v}}(s)$ and reduces the impedance amplitude at low-frequency range, eliminating steady-state voltage deviation. This analysis is consistent with Figure 5.6(b) that the steady-state gain of $G_{\mathrm{vcl}}(s)$ is 1 due to the short-circuit effect of L_{v}. Increasing k_{vi} and k_{vp} can broaden the bandwidth and shorten the adjustment time. Increasing k_{vp} can also suppress Δv_{out}. In addition, the negative resistance characteristic of CPL reduces the voltage-loop damping and aggravate the oscillation. This analysis agrees with *RLC* model analysis of Figure 5.5(e).

$$\omega_{\mathrm{v}} = 1/\sqrt{L_{\mathrm{v}}C_{\mathrm{v}}} < \omega_{\mathrm{v}}^{\mathrm{b}} \tag{5.10}$$

(b) inertia-loop virtual impedance model:

On the basis of the voltage-loop Thevenin equivalent model in Figure 5.5(d), the inertia-loop mathematical model can be represented by Figure 5.7(a). Accordingly, Figure 5.7(b) can be deduced from Figure 5.7(a) by block diagram algebra. As displayed in Figure 5.7(b), the inertia

loop can be also regarded as an LVI.

From Figure 5.7(b), the current-controlled b-BiC is rearranged to a **Thevenin equivalent circuit**: a voltage source $i_{out}^{ref}Z_{vir}(s)$ in series with a virtual impedance (Z_{vcl}+Z_{vir}), as expressed in (5.11a). $Z_{vir}(s)$ is the derived inertia-loop virtual impedance as shown in (5.11b) and its physical essence is a generalized *RLC* circuit influenced by the $G_{vcl}(s)$, as shown in (5.11c). The passive branches of this generalized *RLC* model is R_{vir}, L_{vir} and C_{vir}.

Subsequently, based on Figure 5.7(b), the current-controlled b-BiC is transformed into a **Norton circuit**: a current source $i_{out}^{ref}G_{vir}(s)$ in parallel with virtual impedance (Z_{vcl}+Z_{vir}), as shown in Figure 5.7(c). The output current can be represented by (5.11d), where $G_{vcl}(s)$ is the closed inertia-loop transfer function as shown in (5.11e).

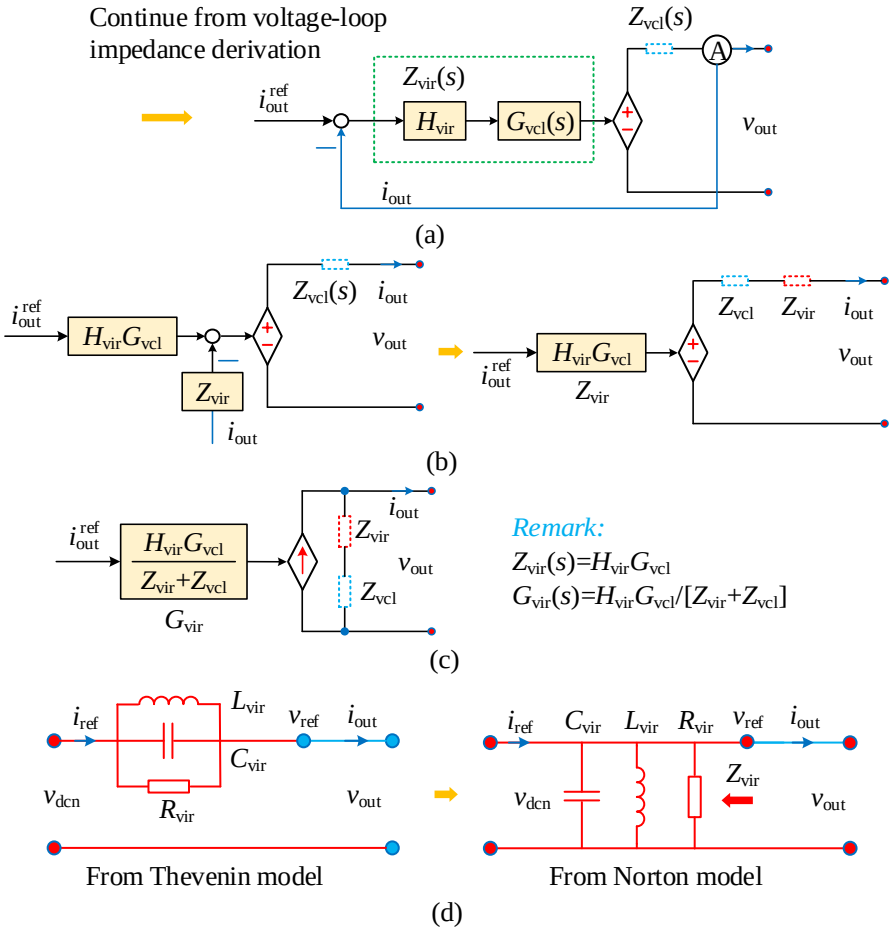


Figure 5.7: Derivation of inertia-loop virtual impedance model and its *RLC* model. (a) Inertia-loop mathematical model. (b) Inertia-loop virtual impedance derivation. (c) Norton equivalent circuit. (d) *RLC* model.

$$v_{out} = i_{out}^{ref}H_{vir}G_{vcl} - i_{out}\left(Z_{vir}(s) + Z_{vcl}(s)\right) \tag{5.11a}$$

$$Z_{vir}(s) = H_{vir}(s)G_{vcl}(s) \tag{5.11b}$$

$$Z_{\mathrm{vir}}(s)=\frac{1}{\frac{sJ_{\mathrm{vir}}}{G_{\mathrm{vcl}}(s)}+\frac{k_{\mathrm{vd}}}{G_{\mathrm{vcl}}(s)}+\frac{k_{\mathrm{svr}}}{sG_{\mathrm{vcl}}(s)}}=\frac{1}{sC_{\mathrm{vir}}+\frac{1}{R_{\mathrm{vir}}}+\frac{1}{sL_{\mathrm{vir}}}} \tag{5.11c}$$

$$i_{\mathrm{out}}=i_{\mathrm{out}}^{\mathrm{ref}}G_{\mathrm{vir}}(s)-\frac{v_{\mathrm{out}}}{Z_{\mathrm{vir}}+Z_{\mathrm{vcl}}} \tag{5.11d}$$

$$G_{\mathrm{vir}}(s)=\frac{H_{\mathrm{vir}}(s)G_{\mathrm{vcl}}(s)}{Z_{\mathrm{vir}}(s)+Z_{\mathrm{vcl}}(s)} \tag{5.11e}$$

At the inertia-loop timescale, voltage loop can be equivalent to a unity-gain loop $G_{\mathrm{vcl}}(s)\approx 1$, because $Z_{\mathrm{vcl}}(s)$ can be regarded as a short circuit due to the equivalent circuit of inductor. From (5.11b), $Z_{\mathrm{vir}}(s)$ can thus be simplified into $H_{\mathrm{vir}}(s)$. The generalized *RLC* model can be reduced into a generic parallel *RLC* model within inertia-loop bandwidth and the passive branches are defined as (5.12). Further, the *RLC* model of $Z_{\mathrm{vir}}(s)$ within inertia-loop bandwidth is depicted in Figure 5.7(d), to illustrate the control effect of inertia loop from the impedance-shaping view.

$$R_{\mathrm{vir}}=\frac{G_{\mathrm{vcl}}(s)}{k_{\mathrm{vd}}}\approx\frac{1}{k_{\mathrm{vd}}},L_{\mathrm{vir}}=\frac{G_{\mathrm{vcl}}(s)}{k_{\mathrm{svr}}}\approx\frac{1}{k_{\mathrm{svr}}},C_{\mathrm{vir}}=\frac{J_{\mathrm{vir}}}{G_{\mathrm{vcl}}(s)}\approx J_{\mathrm{vir}} \tag{5.12}$$

From Figure 5.7(d), the control effect of inertia loop can be also explained from impedance-reshaping perspective. Note that, the control goal of inertia loop focuses on mitigating voltage oscillations and reducing RoCoV, rather than tracking instruction accurately and quickly as voltage loop does. It can be clearly observed from the Norton model that a virtual capacitor C_{vir} is added to suppress voltage oscillation by absorbing or supplying imbalance power. The system inertia is enhanced by exploring the auxiliary power of ESS and thus the voltage stability is improved. Also, it can be concluded from the Thevenin model that R_{vir} limits the voltage fluctuation amplitude Δv_{out} by analogy with (5.9), while L_{vir} behaves as short-circuit and performs as SVR loop to eliminate steady-state voltage error $v_{\mathrm{error}}=v_{\mathrm{dcn}}-v_{\mathrm{ref}}$. k_{svr}, k_{vd}, and J_{vir} characterize system stiffness, dissipation and inertia, which correspond to the abilities of recovery, damping and disturbance rejection at inertia-loop timescale.

$$\omega_{\mathrm{vir}}=1/\sqrt{L_{\mathrm{vir}}C_{\mathrm{vir}}} \tag{5.13}$$

The frequency response of $Z_{\mathrm{vir}}(s)$, *RLC* model and $G_{\mathrm{vir}}(s)$ is shown in Figure 5.8. The frequency response of the inertia-loop virtual impedance $Z_{\mathrm{vir}}(s)$ and that of its *RLC* model $H_{\mathrm{vir}}(s)$, when $k_{\mathrm{svr}}=0.1$, $k_{\mathrm{vd}}=1.5$, and $J_{\mathrm{vir}}=0.2$, is shown in Figure 5.8(a). Their bode plots are basically the same at the inertia-loop timescale, which proves the correctness of the *RLC* model. Notably, J_{vir} shapes $Z_{\mathrm{vir}}(s)$ to capacitive at high frequency, while k_{svr} shapes the $Z_{\mathrm{vir}}(s)$ from resistive to inductive at low frequency. Hence, the SVR loop changes the inertia loop from a 1st-order filter loop to a 2nd-order oscillation loop ($L_{\mathrm{vir}}C_{\mathrm{vir}}$). This will induce low-frequency oscillation at the

inertia-loop timescale. Its natural oscillation frequency is represented as (5.13). Theoretically, this $L_{vir}C_{vir}$ low-frequency oscillation can be suppressed by appropriate k_{vd}, which is however hindered by the positive feedback of k_{vd} in droop loop, (which will be introduced later). SVR loop makes Z_{vir} zero impedance at DC, indicating increased system stiffness and zero steady-state error. The phase lag of G_{vcl} introduces a negative impedance region to $Z_{vir}(s)$ at high frequency (beyond the inertia-loop bandwidth), which might devastate the stability. As displayed in Figure 5.8(b), the inertia-loop bandwidth ω_{iner} is about 10rad/s, and thus inertia loop can be equivalent to a low-pass filter loop with an oscillation modal, indicating battery cannot compensate for high-frequency disturbances (solved by SC in **Section 5.3**).

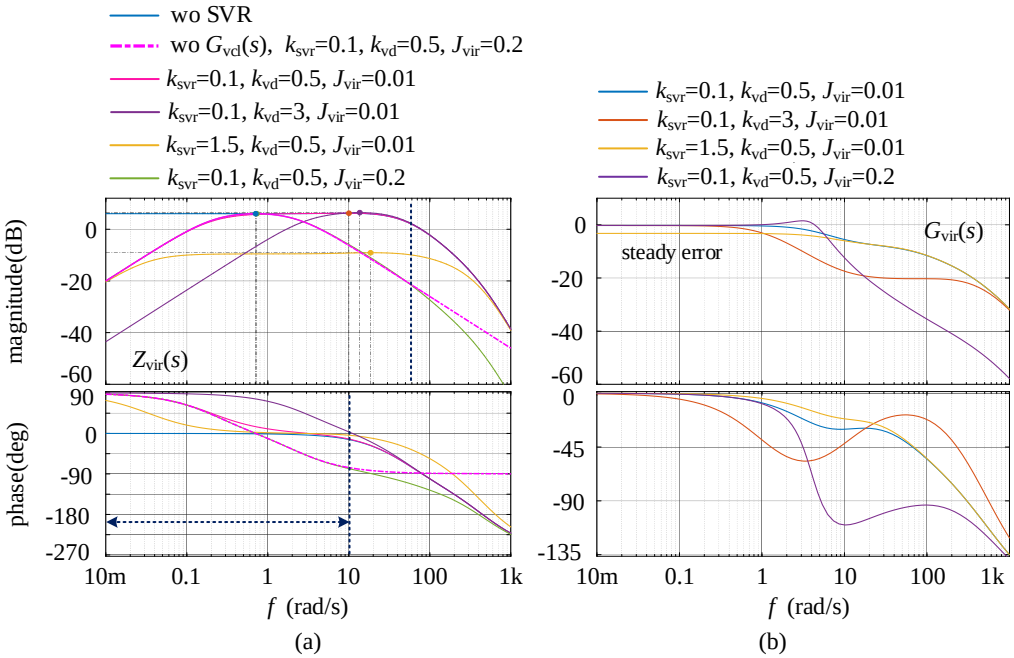


Figure 5.8: Frequency response analysis of inertia loop. (a) $Z_{vir}(s)$. (b) $G_{vir}(s)$.

(c) droop-control virtual impedance model:

As shown in Figure 5.9, the droop control can also be represented by a virtual impedance model. Continuing from the inertia-loop impedance derivation, the droop-loop mathematical model is shown in Figure 5.9(a). By using Block Diagram Algebra, Figure 5.9(a) can be rearranged into Figure 5.9(b), a controlled current source. The source output current is expressed in (5.14a).

Further, based on Ohm's Law and Superposition Theorem, all the droop-loop feedback loops are regarded as virtual admittance as illustrated in Figure 5.9(c), which represents the voltage-controlled b-BiC as a **Norton circuit**: a voltage-controlled current source $v_{dcn}{\cdot}Y_{vi}$ in parallel with admittance $Y_{droop}+Y_{vd}+Y_{cpl}$, as defined in (5.14c-e). From equations (5.14c-e), Y_{vd} is the admittance generated by inertia control, Y_{cpl} represents the interaction between droop control

and CPL, and Y_{droop} is the droop-control virtual admittance.

$$i_{out} = v_{dcn} \cdot Y_{vi} - v_{out}\left(Y_{cpl} + Y_{vd} + Y_{droop}\right) - \frac{v_{out}}{Z_{vir} + Z_{vcl}} \tag{5.14a}$$

$$Y_{vi}(s) = (1 + H_1)\left(\frac{1}{R_d} - k_{vd} + \frac{1}{R_{cpl}}\right)G_{vir} \tag{5.14b}$$

$$Y_{vd}(s) = -k_{vd}G_{vir} \tag{5.14c}$$

$$Y_{cpl}(s) = G_{vir}/R_{cpl} \tag{5.14d}$$

$$Y_{droop}(s) = G_{vir}/R_d \tag{5.14e}$$

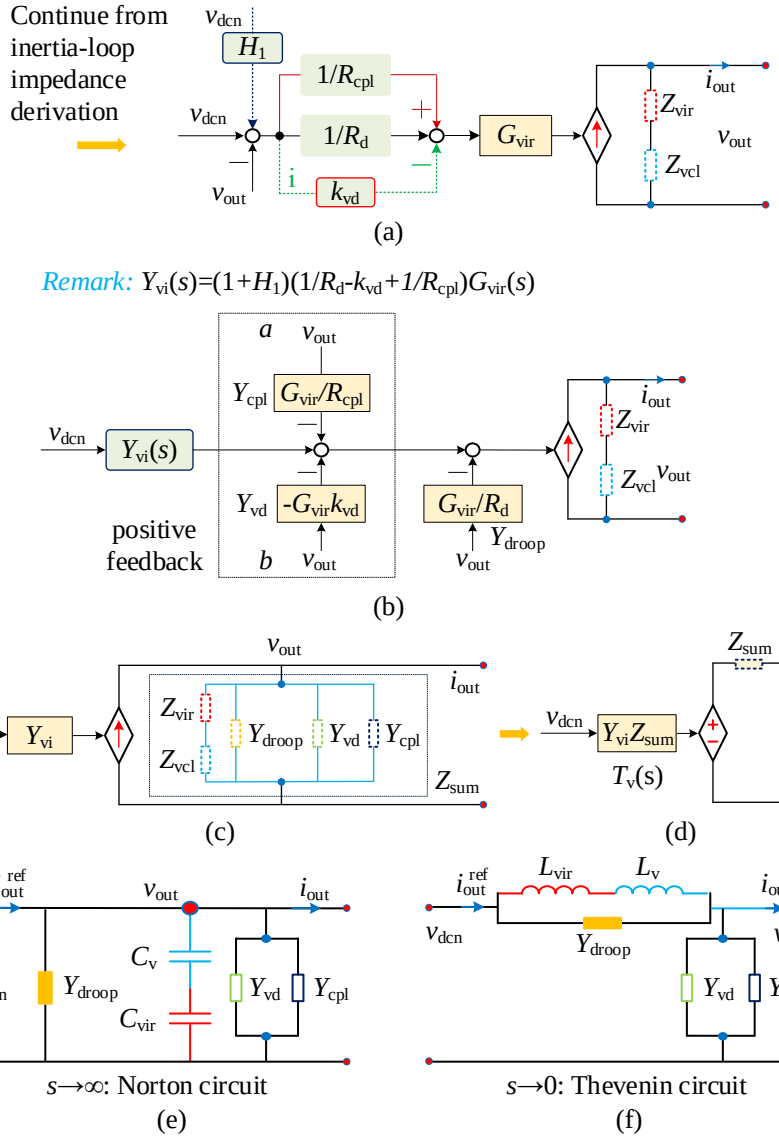


Figure 5.9: Derivation of droop-control virtual impedance model and the *RLC* model of the total system impedance. (a) Droop-loop mathematical model. (b) Droop-loop virtual impedance derivation. (c) Norton equivalent circuit. (d) Thevenin equivalent circuit. (e) *RLC* model in Norton circuit form. (f) *RLC* model in Thevenin circuit form.

Subsequently, the voltage-controlled b-BiC is equivalent to a **Thevenin circuit**: the controlled voltage source $v_{dcn}{\cdot}T_v(s)$ in series with the total source-terminal impedance $Z_{sum}(s)$, as shown in Figure 5.9(d). The voltage-source output voltage is expressed in (5.15a). The total impedance $Z_{sum}(s)$ is expressed in (5.15b), and $T_v(s)$ is the voltage close-loop gain as shown in (5.15c).

$$v_{out} = v_{dcn} \cdot T_v(s) - i_{out} \cdot Z_{sum}(s) \tag{5.15a}$$

$$Z_{sum}(s) = \left(Y_{cpl} + Y_{vd} + Y_{droop}\right)||(Z_{vir} + Z_{vcl}) \tag{5.15b}$$

$$T_v(s) = Z_{sum}(s) \cdot Y_{vi}(s) \tag{5.15c}$$

According to the Final Value Theorem, the *RLC* model of Z_{sum} in Norton circuit and Thevenin circuit form are shown in Figure 5.9(e) and (f). Thus, the control function of VIDC can be explained at multi-timescale physically. In Figure 5.9(e) ($s\to\infty$): C_v and C_{vir} short-circuit the disturbance current, thus the RoCoV is suppressed. The DC-MG's anti-interference ability is enhanced (inertia). In Figure 5.9(f) ($s\to0$): L_v and L_{vir} short-circuit Y_{droop}, and the voltage deviation caused by droop control is zero. The voltage restoration ability is strengthened (stiffness). From impedance-shaping perspective, the stability mechanism and voltage recovery process are intuitively illustrated at voltage-loop and inertia-loop timescales.

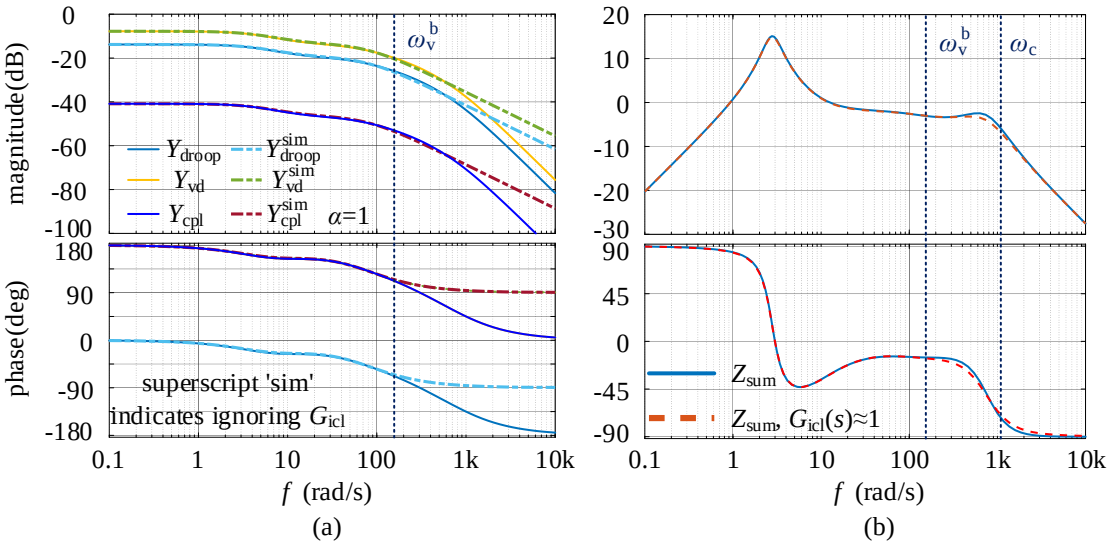


Figure 5.10: Frequency response of droop loop. (a) Y_{droop}, Y_{vd} and Y_{cpl}. (b) Z_{sum}.

The frequency response of each virtual admittance and Z_{sum} is shown in Figure 5.10. Y_{cpl} and Y_{vd} are negative admittances in voltage-loop timescale, weakening the system damping. Thus, the loops *a* and *b* in Figure 5.9(b) are of positive feedback (PFB), exacerbating low-frequency oscillation. Moreover, the phase lag of G_{icl} makes Y_{droop} behaves as negative admittance at high frequency (beyond the voltage-loop bandwidth), endangering high-frequency stability. From Figure 5.10(b), Z_{sum} presents a positive impedance characteristic, suggesting that the VIDC-

DC-MG can still operate stably even though the non-passive region of Y_{droop}, Y_{vd} and Y_{cpl}. Thus, the conventional all-in-one impedance model cannot intuitively explain the physical meaning of control parameters, nor can it visually discover the potential instability factors, such as Z_{vir}, Y_{droop}, Y_{vd} and Y_{cpl}, as the proposed multi-timescale impedance model can do.

5.2.3 Positive-feedback-based instability factor analysis and verification of multi-timescale impedance model

Based on the above virtual impedance analysis, non-passive region exists in Y_{vd} and Y_{cpl}. These loops with non-passive region can be visualized as PFB due to their negative damping.

(a) Positive feedback analysis:

Based on Block Diagram Algebra and the proposed impedance model, source-load two-terminal model of VIDC-DC-MG can be simplified to Figure 5.11(a), which illustrates the interaction between 'source' and 'load' terminal. From Figure 5.11(a), the total source-terminal impedance Z_{sum} is also the system bus-impedance. Virtual admittance Y_{vd} and Y_{cpl} can be replaced by voltage-controlled current sources i_{vd_c} and i_{cpl_c} as shown in (5.16). Thus, Figure 5.11(a) is transferred into Figure 5.11(b). From Figure 5.11(b), the output current of 'source' terminal i_{out} consists of four components, as expressed in (5.16c).

$$i_{vd\_c} = -Y_{vd} v_{out} = k_{vd} v_{out} G_{vir} \tag{5.16a}$$

$$i_{cpl\_c} = -Y_{cpl} v_{out} = -\alpha R_{cpl} v_{out} G_{vir} \tag{5.16b}$$

$$i_{out} = i'_{out} + i_{vd\_c} + i_{cpl\_c} - i_z \tag{5.16c}$$

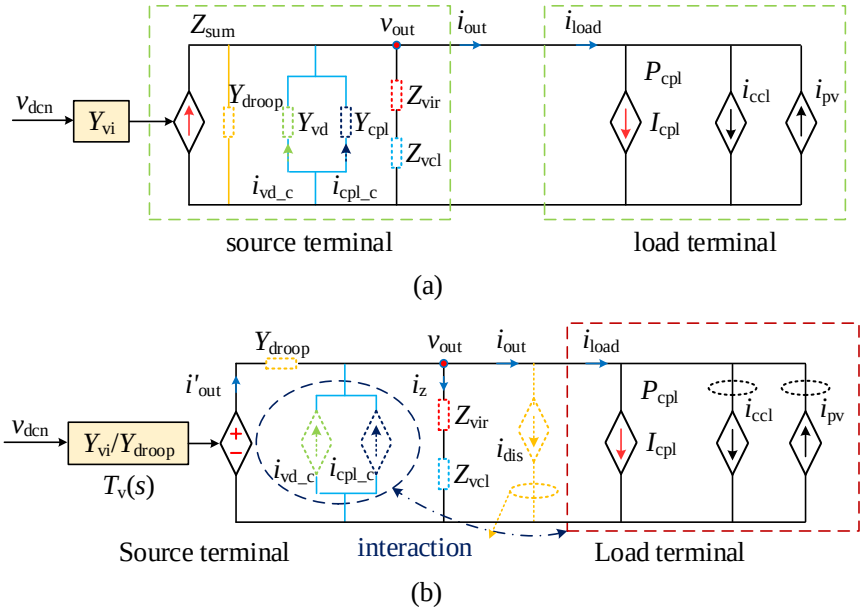


Figure 5.11: Feedback-based instability factor analysis. (a) Current-source. (b) Voltage-source.

Assuming that there is a power disturbance in DC-MG to increase load power by i_{dis} as shown in Figure 5.11(b). The output current of the 'source' terminal i_{out} and the input current of 'load' terminal i_{load} will lose balance and power difference occurs. Thus, the system voltage would drop under the action of C_{vir} and C_v to compensate for power difference. According to (5.16a-b) and Figure 5.11(b), the dropping v_{out} will reduce the power output of i_{vd_c} and i_{cpl_c}, as well as lead to the reduction of i_{out} based on (5.16c). Thus, the power difference between the 'source' and 'load' terminal will be enlarged, which essentially forms PFB leading to further drop of output voltage v_{out}. Based on the above analysis, the negative admittances Y_{cpl} and Y_{vd} introduce positive feedback, making it difficult for the DC voltage to converge to the steady-state value, so Y_{cpl} and Y_{vd} are instability factors. Hence, in addition to CPL, Y_{vd} from virtual inertia control also undermines voltage stability.

According to the detailed impedance analysis, a summary of LVIs is shown in Table 5.3. Note that, VIDC-DC-MG is still stabilized, though there are instability factors leading to voltage oscillation due to the coupling among different timescales.

Table 5.3 Summary of multi-timescale impedance model

Control loops	Sym-bol	Physical Interpretation	Remarks	
Voltage-loop PI	Z_v	A virtual resistor $1/\mu k_{vp}$ and a virtual inductor $1/\mu k_{vi}$, in parallel with C_{out}	limited by current-loop gain $G_{icl}(s)$ voltage-loop timescale LC low-frequency oscillation[1]	
	R_{cpl}	A negative resistance by CPL in parallel with Z_v	Reducing the system damping[2]	
Inertia loop	Z_{vir}	A virtual resistor $1/k_{vd}$, a virtual inductor $1/k_{svr}$ and a virtual capacitor J_{vir}	limited by voltage-loop gain $G_{vcl}(s)$ inertia-loop timescale LC low-frequency oscillation[1] improve system inertia at inertia-loop timescale eliminate steady-state voltage errors (stiffness) equivalent to a low-pass filtering link essentially[3] possible negative damping at high frequency (voltage- and current-loop)[3]	
Droop control	Y_{vd}	Positive feedback/negative virtual admittance	reduce system damping (within voltage loop)[4]	influenced by inertia-loop gain $G_{vir}(s)$
	Y_{cpl}	Positive feedback/negative virtual admittance		
	Y_{droop}	Virtual admittance	negative damping in high frequency (current loop)[3]	

Remarks: 1-*problem 1*, 2-*problem 2*, 3-*problem 3*, 4-*problem 4*.

***Problem 1*:** The LC impedance interactions induce low-frequency oscillation in the voltage- and inertia-loop timescale.

***Problem 2*:** A negative resistance by CPL is introduced to the voltage loop and thus aggravate the voltage-loop LFO, which is essentially 'source'-'load' terminal interaction.

***Problem 3*:** Y_{droop} behaves as negative admittance at voltage-loop and inertia-loop timescale due to the inertia-loop phase lag, while Z_{vir} behaves as negative admittance at voltage-loop timescale due to the voltage-loop phase lag.

***Problem 4*:** Y_{vd} and Y_{cpl} behave as negative damping (ND) at voltage-loop and inertia-loop timescales, and they essentially introduce PFB to VIDC-DC-MG, deteriorating the system robustness and enlarging the oscillation amplitude.

(b) Time-domain validation of the proposed impedance model:

Based on the system topology in Figures 5.1 and 5.2, the studied DC-MG is established in MATLAB. The parameters are listed in Tables 5.1 and 5.2. The switch model is conducted in the following condition: the CPL increases by 1kW at t=6s. The corresponding LVIs of the switch model are also deduced.

The step response of the switch model (SM) and impedance model (IM) are demonstrated in Figure 5.12. It can be observed that the SM results basically coincide with the IM results. In addition, the control effect of each parameter is also consistent with the multi-timescale impedance-model-based analysis. k_{vp} and k_{vi} affect voltage control overshoot and adjustment time at voltage-loop timescale. J_{vir}, k_{svr} and k_{vd} determine oscillation frequency and amplitude in inertia-loop timescale, representing the system inertia, stiffness and dissipation property. It is worth noting that the PFB of Y_{vd} and Y_{cpl} introduces ND. Thus, the multi-timescale impedance model and control-loops impedance-shaping effect are validated.

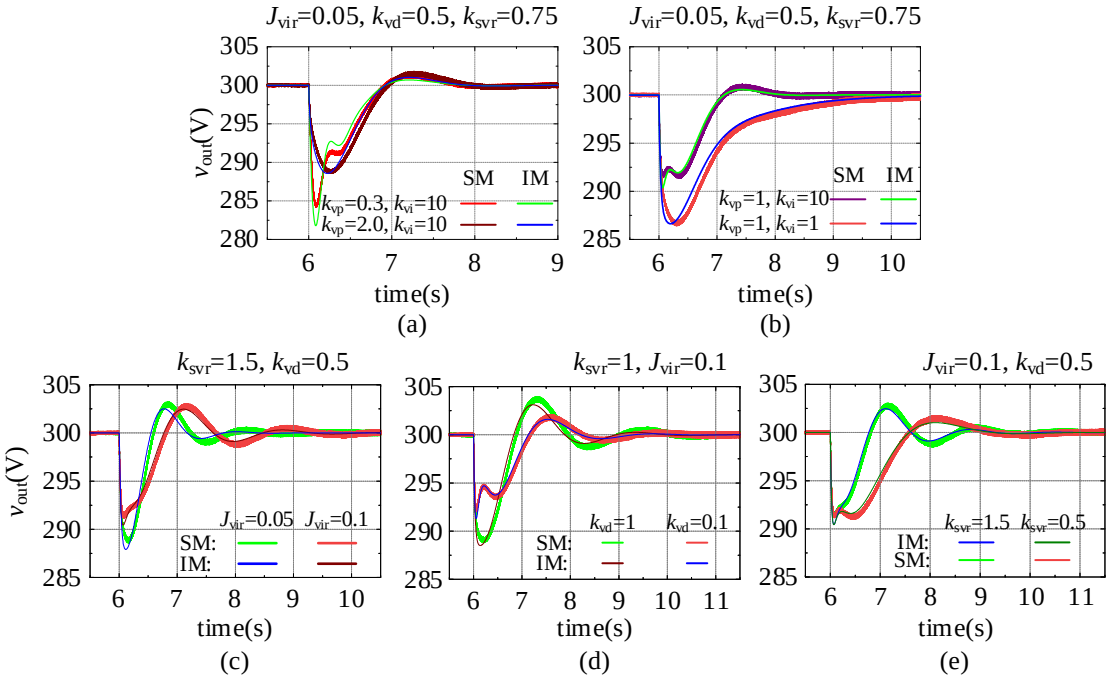


Figure 5.12: Switch model verification of multi-timescale virtual impedance model with different parameters. (a) k_{vp}. (b) k_{vi}. (c) J_{vir}. (d) k_{vd}. (e) k_{svr}.

Note that, the transmission line is considered in the SM, while not in the proposed multi-timescale impedance model for a more conservative analysis. By comparing their step response in

the Figure 5.12, it can be seen that the line impedance has no obvious effect on the accuracy of analyzing low-frequency oscillations, thus it can be ignored in the impedance model.

5.3 Transient Stability Enhancement Method and its Verification

In order to cancel the hidden instability factors and overcome the shortcomings of the battery, positive-damping reshaping loops (PDRLs) are proposed to correct the ND of Y_{vd} and Y_{cpl}, and SC is added to cooperate with virtual-inertia-controlled battery for inertia improvement. The role of SC is shifting the voltage-loop low-frequency oscillation to the inertia-loop timescale, which is then suppressed by PDRLs.

5.3.1 Transient stability enhancement method

(a) positive-damping reshaping loops:

PDRL-*a* and -*b* are added to compensate for the ND caused by Y_{vd} and Y_{cpl} at low frequency due to its PFB nature, as shown in (5.17a-b). i_{cpl}^{c} and i_{vd}^{c} are the CPL compensation current and the damping compensation current, respectively. β is a compensation coefficient. Accordingly, the inertia-loop current command i_{out}^{ref} has also been modified as shown in (5.17c).

It is worth noting that PDRLs can only play a role within the inertia-loop bandwidth and have little suppression effect on the voltage-loop oscillation.

$$i_{vd}^{c} = \frac{v_{dcn} - v_{out}}{k_{vd}} \tag{5.17a}$$

$$i_{cpl}^{c} = \beta \cdot (v_{out} - v_{dcn})/R_{cpl} \tag{5.17b}$$

$$i_{out}^{ref} = \frac{v_{dcn} - v_{out}}{R_{d}} + i_{vd}^{c} - i_{cpl}^{c} \tag{5.17c}$$

(b) SC and its timescale-based coordination control:

Due to the low-pass-filter property of the virtual inertia loop and high-frequency ND of Y_{droop} and Z_{vir}, the battery cannot compensate the high-frequency power disturbance effectively. Thus, SC is added to conceive HESS, as mentioned in Figure 1. Timescale-based coordination control is proposed for SC-BiC as shown in (5.18a) to differentiate the response timescale of battery and SC. The cross-over frequency of high pass filter (HPF) ω_{hp} is selected as 10 rad/s to cooperate with the VIDC. *k* is the compensation coefficient and selected as 3. Different from battery responding to slow and long-term fluctuations, SC only responds to fast and short-term power disturbances.

$$i_{\mathrm{hf}} = k \cdot (v_{\mathrm{ref}} - v_{\mathrm{out}}) \frac{s}{s + \omega_{\mathrm{hp}}} = k(v_{\mathrm{ref}} - v_{\mathrm{out}})\mathrm{HPF}(s) \tag{5.18a}$$

$$i_{\mathrm{vr}} = \left(v_{\mathrm{sc\_ref}} - v_{\mathrm{sc}}\right) G_{\mathrm{v}}(s) \tag{5.18b}$$

$$i_{\mathrm{sc}}^{\mathrm{ref}} = i_{\mathrm{hf}} + i_{\mathrm{vr}} \tag{5.18c}$$

After compensating for high-frequency disturbances, the SC voltage will deviate from its rated value. Thus, the SC voltage recovery loop (SC-VRL) with the slow response is added to stabilize the SC voltage, as shown in (5.18b). Its loop bandwidth $\omega_{\mathrm{v}}^{\mathrm{sc}}$=0.51 rad/s is much smaller than ω_{hp} to avoid SC-VRL conflicts with the compensation of high-frequency disturbances.

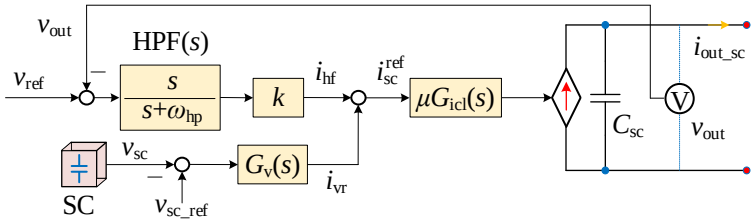


Figure 5.13: The control diagram of SC.

As shown in (5.18c), $i_{\mathrm{sc}}^{\mathrm{ref}}$ is the command of SC output current i_{sc}, including high-frequency compensation current component i_{hf} and voltage recovery component i_{vr}. The control structure is shown in Figure 5.13. $i_{\mathrm{out\_sc}}$ is the output current of SC-BiC. C_{sc} is the output capacitor of SC-BiC.

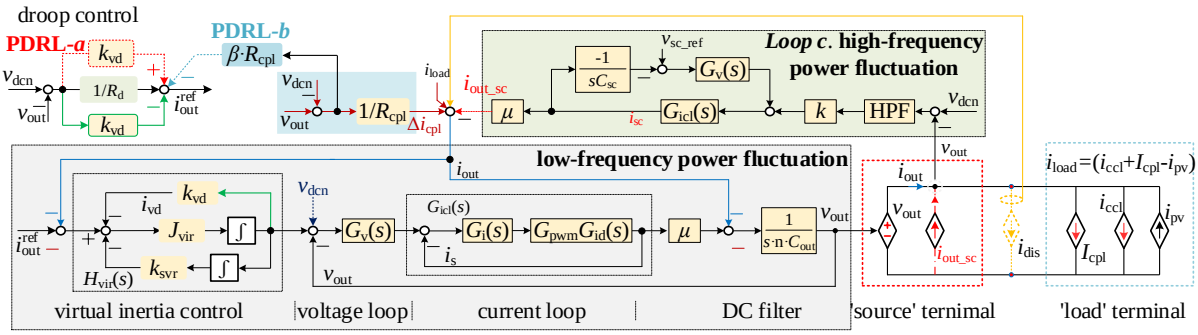


Figure 5.14: Source-load two-terminal model of islanded DC-MG considering the transient stability enhancement method.

(c) LVI analysis of stability enhancement loops:

According to the proposed multi-timescale impedance modelling method, the virtual impedance of PDRL-*a* and *b* are derived as $Y_{\mathrm{vd}}^{\mathrm{a}}$, and $Y_{\mathrm{cpl}}^{\mathrm{b}}$, as shown in (5.19). From Figure 5.13, the output impedance model of the SC unit (Z_{sc}) is derived as shown in (5.20) and integrated to the 'source' terminal. The mathematical model of VIDC-DC-MG considering the stability enhancement loops is shown in Figure 5.14.

$$Y_{\mathrm{vd}}^{\mathrm{a}} = k_{\mathrm{vd}} \cdot G_{\mathrm{vir}}(s) \tag{5.19a}$$

$$Y_{\mathrm{cpl}}^{\mathrm{b}} = -\alpha \cdot \beta \cdot R_{\mathrm{cpl}} \cdot G_{\mathrm{vir}}(s) \tag{5.19b}$$

$$Z_{\mathrm{sc}}(s) = \frac{-\Delta v_{\mathrm{out}}}{\Delta i_{\mathrm{out\_sc}}} = \frac{sC_{\mathrm{sc}} + G_{\mathrm{icl}}(s)G_{\mathrm{v}}(s)}{sC_{\mathrm{sc}}(sC_{\mathrm{sc}} + G_{\mathrm{icl}}(s)G_{\mathrm{v}}(s) + k\mathrm{HPF}(s)G_{\mathrm{icl}}(s)\mu)} \tag{5.20}$$

Combining Figure 5.14 and Eqs. (5.19), (5.20), the multi-timescale impedance of VIDC-DC-MG considering the dynamic stability enhancement method can be obtained, as shown in Figure 5.15. The total virtual impedance $Z_{\mathrm{sum}}^{\mathrm{t}}$ can be re-derived, as shown in (5.21).

$$Z_{\mathrm{sum}}^{\mathrm{t}} = \left(Y_{\mathrm{cpl}} + Y_{\mathrm{cpl}}^{\mathrm{b}} + Y_{\mathrm{vd}} + Y_{\mathrm{vd}}^{\mathrm{a}} + Y_{\mathrm{droop}}\right)||(Z_{\mathrm{vir}} + Z_{\mathrm{vcl}})||Z_{\mathrm{sc}} = Z_{\mathrm{sum}}||\left[\left(Y_{\mathrm{cpl}}^{\mathrm{b}} + Y_{\mathrm{vd}}^{\mathrm{a}}\right)||Z_{\mathrm{sc}}\right] \tag{5.21}$$

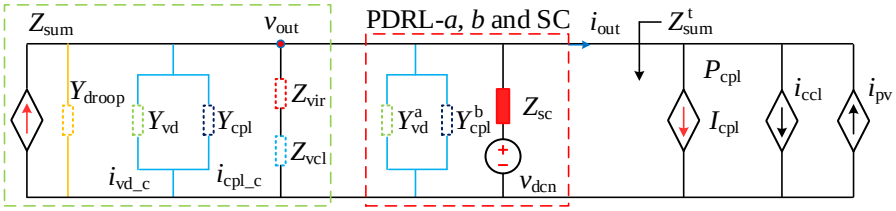


Figure 5.15: Impedance reshaping effect of stability enhancement loops.

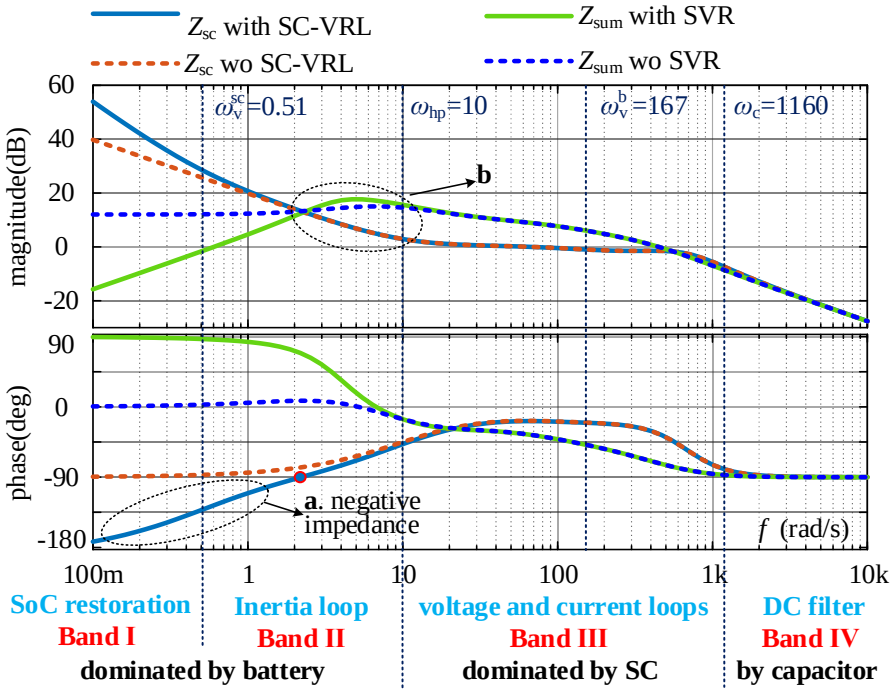


Figure 5.16: Impedance analysis of SC.

The frequency response of Z_{sc} and Z_{sum} is shown in Figure 5.16. The coordination and cooperation between virtual-inertia-controlled battery and SC are clarified in four frequency bands. With the HPF of SC and low-pass characteristics of inertia loop, HESS compensates disturbances according to their response timescale. In band IV, the DC capacitors take care of the high-frequency harmonics. In band III, the system impedance is dominated by capacitive impedance

Z_{sc} and the SC responds to short-term disturbances, while Z_{sum} becomes dominant in bands I and II, and the battery responds to long-term fluctuation. SC and battery cooperate in different timescales, realizing their complementary advantages.

Remark of Fig. 16*:** In circle ***a, SC-VRL leads to negative impedance of Z_{sc} in band I, and its physical meaning can be regarded as a long-term disturbance compensated by battery, which does not bring obvious negative impacts. In circle ***b***, although Z_{sc} is smaller than Z_{sum}, battery would work for this frequency band due to ω_{hp}=10 rad/s, instead of SC.

5.3.2 Time-domain validation of stability enhancement method

Considering the proposed stability enhancement method, simulation verification on the VIDC-DC-MG is provided. The basic parameters are shown in Table 3.1 and 3.2. The step response of SM and IM under the condition of CPL increasing by 1kW at t=6s are shown in Figure 5.17.

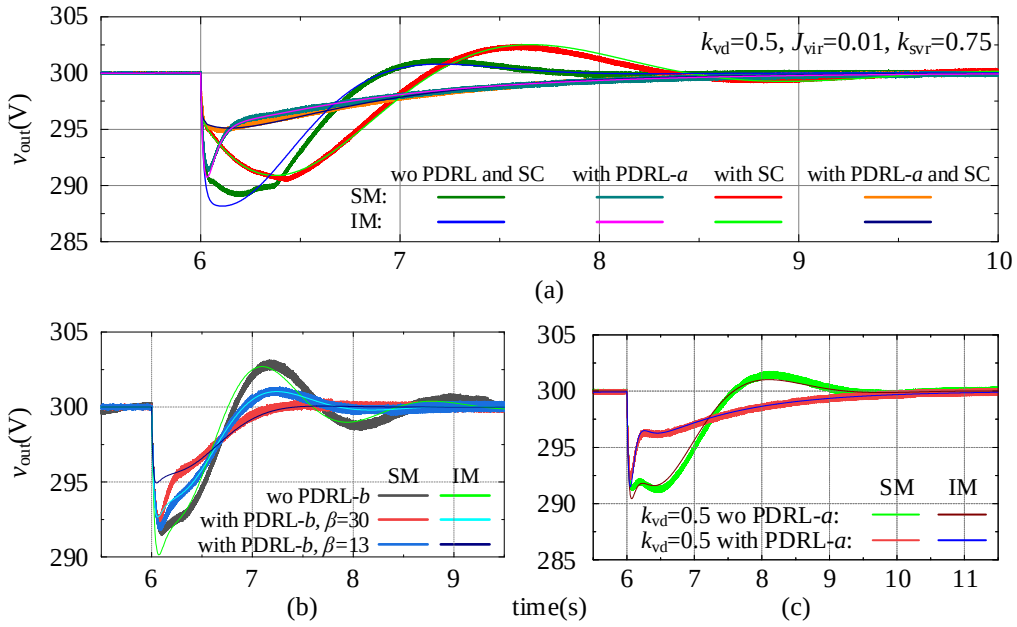


Figure 5.17: SM verification of stability enhancement method. (a) Comparison of different stability enhancement loops. (b) Varying β. (c) Effect of PDRL-a.

From Figure 5.17, the SM step response is almost consistent with IM step response, verifying the effectiveness of the proposed stability enhancement loops. PDRL-a and -b mainly improve low-frequency damping by offsetting the ND caused by PFB and suppress voltage fluctuations caused by long-term disturbances. Obviously, PDRLs suppresses the inertia-loop low-frequency oscillation amplitude and has little effect on the voltage-loop oscillation. Larger β can improve the system damping more obviously. Moreover, SC can enhance the high-frequency

inertia by introducing capacitive impedance Z_{sc} and reduce the voltage-loop oscillation frequency into the inertia loop bandwidth, thus the voltage-loop oscillation can be mitigated by PDRLs as shown in Figure 5.17(a). It can be seen from Figure 5.17(b) that, different from the step response of IM, no special improvement effect is observed in the initial stage of the SM, which is restricted by the battery output characteristics.

From the opposite perspective, the system stability becomes worse without the effect of stability enhancement methods due to the negative damping of the instability factors. Hence, Figure 5.17 also verifies the instability factor analysis in ***Section 5.2.3***.

5.4 Passivity-Based Voltage Stability Assessment

In the previous analysis, a detailed analysis of the impedance characteristics of each control loop has been conducted with the help of the bode diagram, and the LFO of different timescales is studied. In this section, the Nyquist diagram is adopted to evaluate the voltage stability.

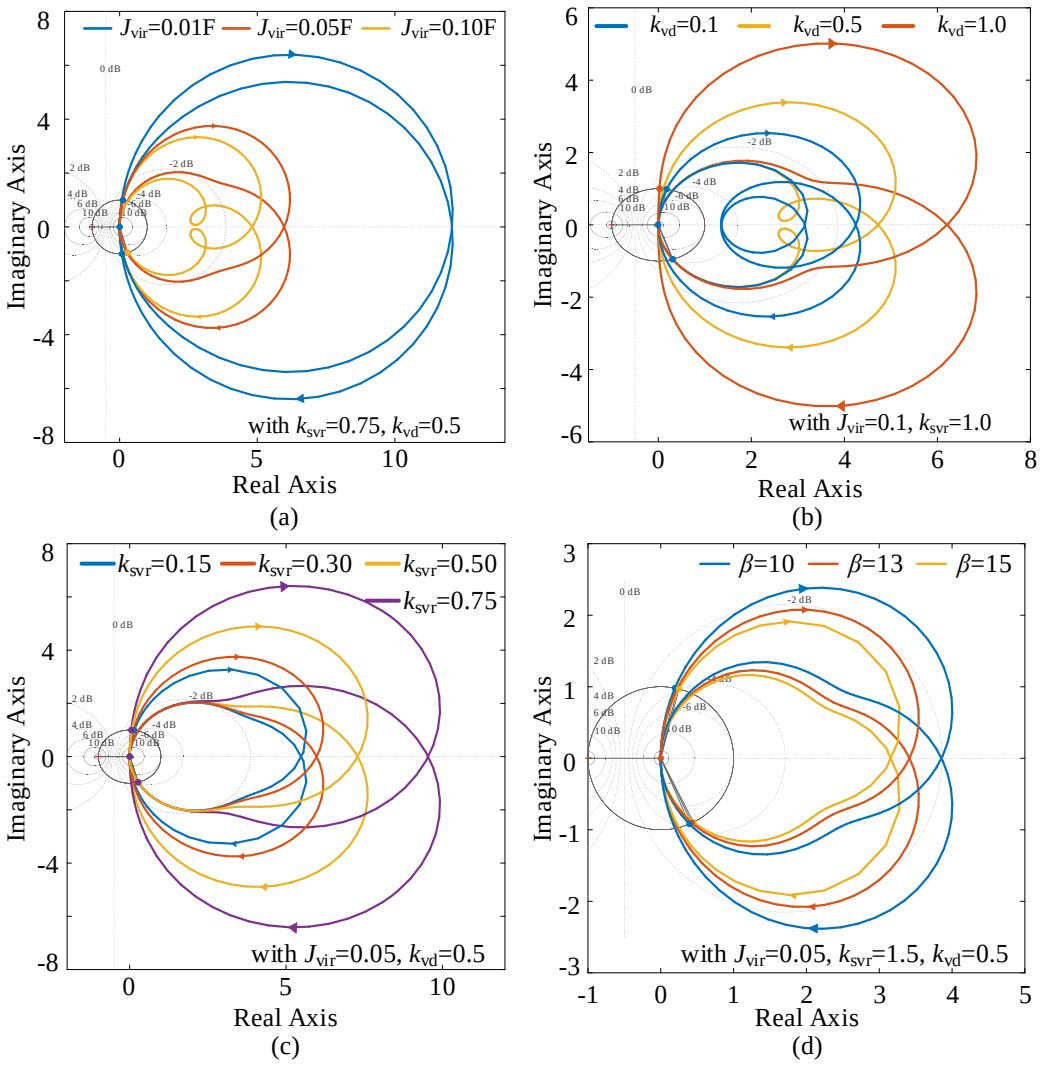


Figure 5.18: Nyquist plot of impedance model Z^{t}_{sum} with various parameters. (a) Varying J_{vir}. (b)

Varying k_{vd}. (c) Varying k_{svr}. (d) Varying β.

From Figure 5.15, the total source-terminal impedance $Z^{t}_{sum}(s)$ also represents the system bus-impedance. Thus, based on passivity-based stability criterion (PBSC), the voltage dynamic stability influenced by control parameters/loops can be assessed by the Nyquist plot of $Z^{t}_{sum}(s)$ [55]. Specifically, the system can guarantee the passivity and the stability, if and only if the system impedance satisfies the following conditions [110]:

1) $Z_{sum}(j\omega)$ contains no right half plane (RHP) poles;
2) $\mathrm{Re}\{Z_{sum}(j\omega)\}\geq 0, \forall\omega$.

It can be concluded from the definition of PBSC that the PBSC gives general insight into small-signal stability of the system; however, it does not give any information regarding the dynamic performance (Low-frequency oscillation). For example, if there is a peak in the bus impedance, even though this impedance peak may not be large enough to violate the PBSC, it can cause an oscillatory behaviour of the bus voltage, thus deteriorating the system dynamic performance [147]. This indicates that PBSC cannot directly observe information such as the low-frequency oscillation frequency, when the bus impedance peak is not very large. Thus, in this section, the PBSC is only used to evaluate the system stability level and the influence of control parameters by observing the Nyquist plot distribution of the total bus impedance. This is different from the effect of bode plot that identifies the detail information of LFO of different timescale.

The influence of control parameters on voltage stability is depicted in Figure 5.18. It can be observed from Figure 5.18(a) that as J_{vir} increases, Nyquist curve shrinks in RHP, indicating voltage stability is improved gradually because of the strengthened inertia. From Figure 5.18(b), the Nyquist plot extends in RHP as k_{vd} increases, suggesting the voltage stability deteriorates due to the ND caused by the PFB of Y_{vd}. Increasing k_{svr} extends Nyquist plot in RHP, indicating deteriorating low-frequency oscillation, which is caused by the increasing interaction between C_{vir} and L_{vir}. In addition, increasing β can offset the ND from the interaction between CPL and VIDC controlled b-BiC, shrinking the Nyquist plot.

The influence of stability enhancement loops on voltage stability is illustrated in Figure 5.19. PDRL-*a*, *b* and SC can shrink the Nyquist trajectory, indicating improved system damping and voltage stability. It is worth noting that although SC-VRL could reduce the system stability, its impact can be ignored as explained in Figure 5.16, because it can essentially be equivalent to a slow and long-term disturbance. The voltage stability can be assessed through the Nyquist plot distribution of the proposed multi-timescale impedance model. The control parameters design

and stability enhancement loop can be determined by selecting a suitable Nyquist contour.

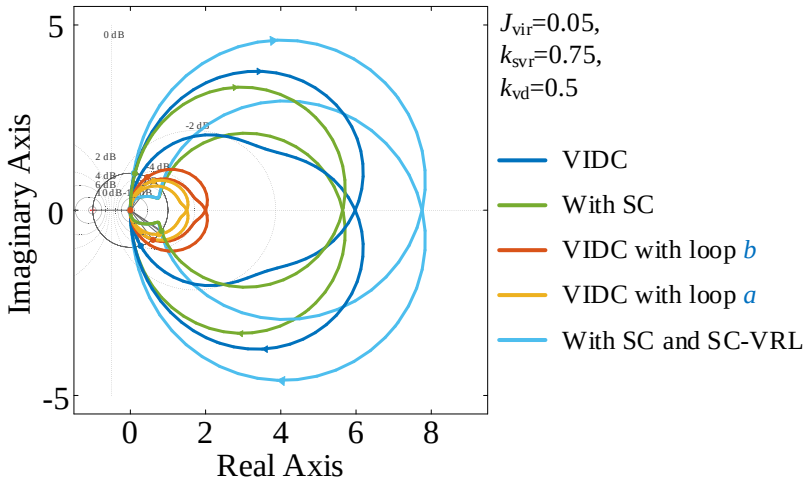


Figure 5.19: Nyquist plot of Z^{t}_{sum} with different stability enhancement loops.

5.5 Experiment Verification

5.5.1 Hardware in the loop experiment

To validate the proposed impedance modelling framework and stability enhancement method, a dSPACE-based hardware in the loop (HIL) platform is established as shown in Figure 4.14, based on the topology of studied DC-MG in Figure 5.1. Control and circuit parameters are listed in Tables 5.1 and 5.2. The HIL experiment is conducted in the following condition: the CPL is changed by 1kW every 8s (increasing and reducing).

The circuit part of DC-MG is built in the power electronics simulation software MATLAB and deployed in compact prototype MicroLabBox with a time step of 100 μs. The discrete control algorithm is implemented in the NXP (Freescale) QorlQ P5020 processor to generate the gate signals of all IGBTs and the sampling frequency is 10 kHz. The analog signals and digital signals (state variables and PWM signal) are transferred through I/O interfaces and cables.

Figures 5.20 and 5.21 illustrate the related experiment results in different scenarios. The SC with timescale-based coordination control responds to the high-frequency component of the power fluctuation, thus RoCoV is significantly reduced in the initial stage of the dynamic process. The decreased oscillation frequency indicates that the system inertia is increased in high-frequency bandwidth, but the oscillation duration are prolonged.

In addition, PDRL-*a* and -*b* are mainly in charge of low-frequency component of power fluctuation to improve low-frequency damping and reduce the oscillations amplitude. The cooperation and coordination of PDRL and SC can not only enhance the system inertia in a wider

frequency band, but also suppress the larger oscillation amplitude caused by the PFB of Y_{vd} and Y_{cpl}. Besides, high-frequency resonance might be observed, which is mainly caused by the ND of Y_{droop} and $Z_{vir}(s)$ at high frequency and tackled by SC.

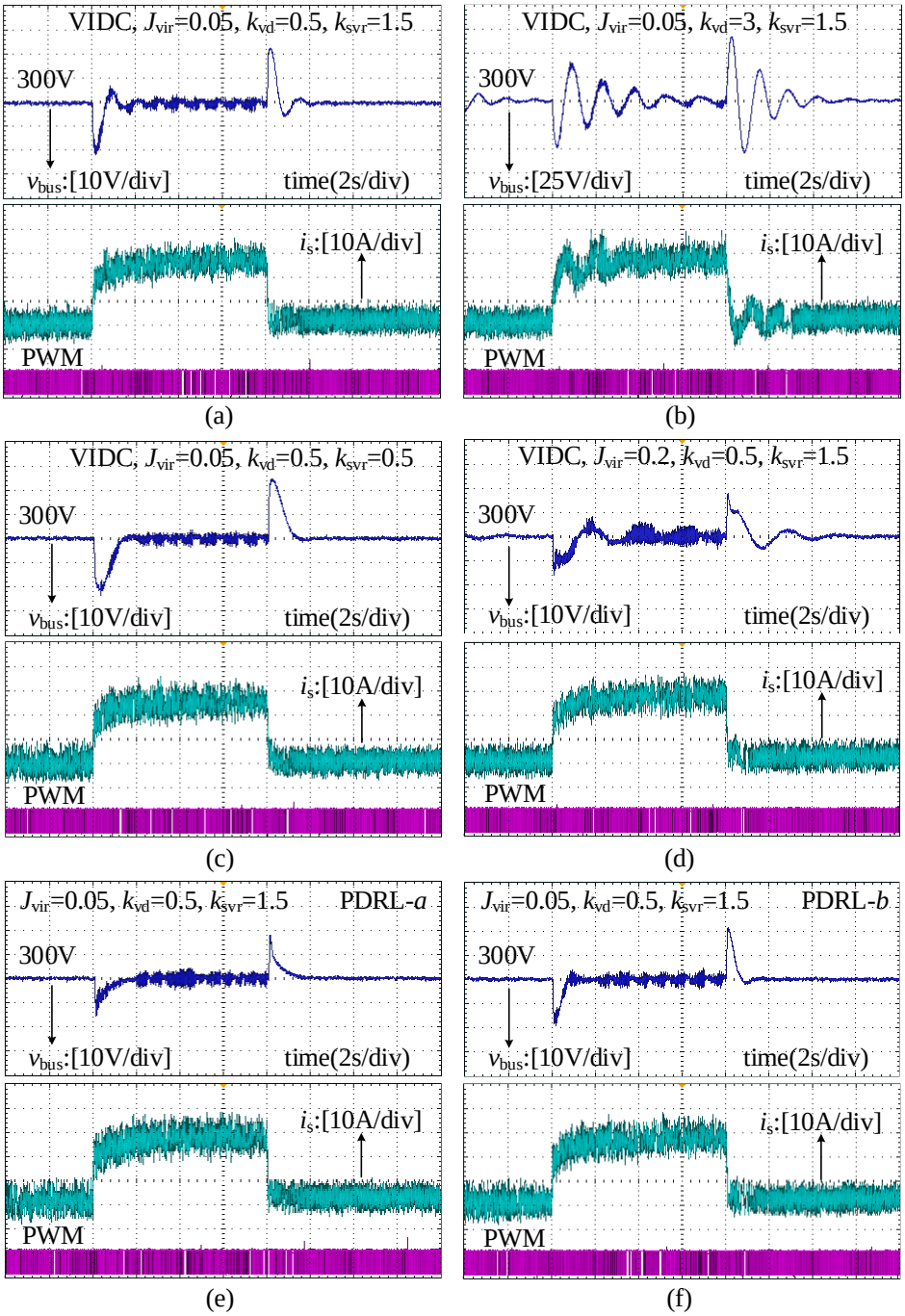
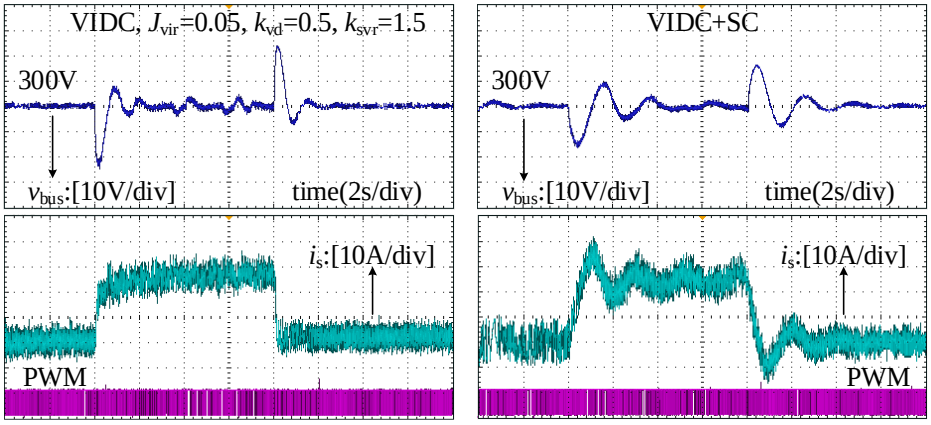


Figure 5.20: Measured waveforms of bus voltage and current with different control method. (a) Effect of VIDC. (b) Varying k_{vd}. (c) Varying k_{svr}. (d) Varying J_{vir}. (e) Effect of PDRL-*a*. (f) Effect of PDRL-*b* with β=11.

5.5.2 Physical experiment verification

To further verify the correctness of theoretical analysis and HIL experimental results, an experiment platform based on the two-terminal system depicted in Figure 5.3 is established and its hardware setup is shown in Figure 5.22. The control algorithm of VIDC is implemented in the MicroLabBox (DS1202) and the sampling frequency is set to be 10 kHz. The parameters are the same as HIL experiment, which are listed in Tables 5.1 and 5.2. The load is perturbed by 1.6 kW of power.



(a) (b)

Figure 5.21: Waveforms of bus voltage and current. (a) VIDC. (b) VIDC+SC.

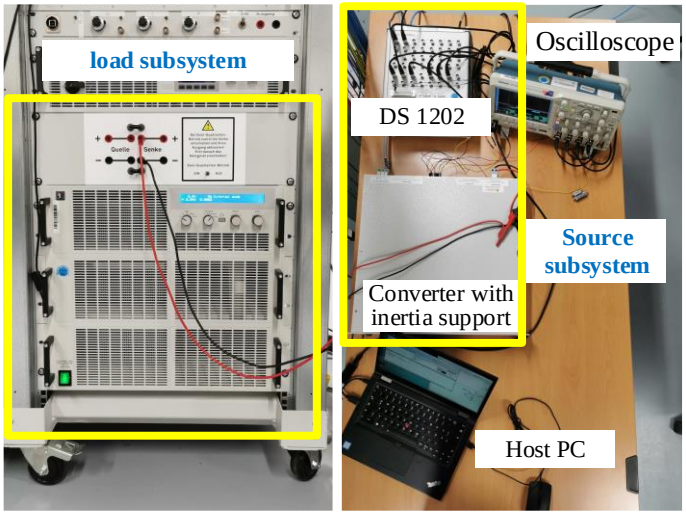
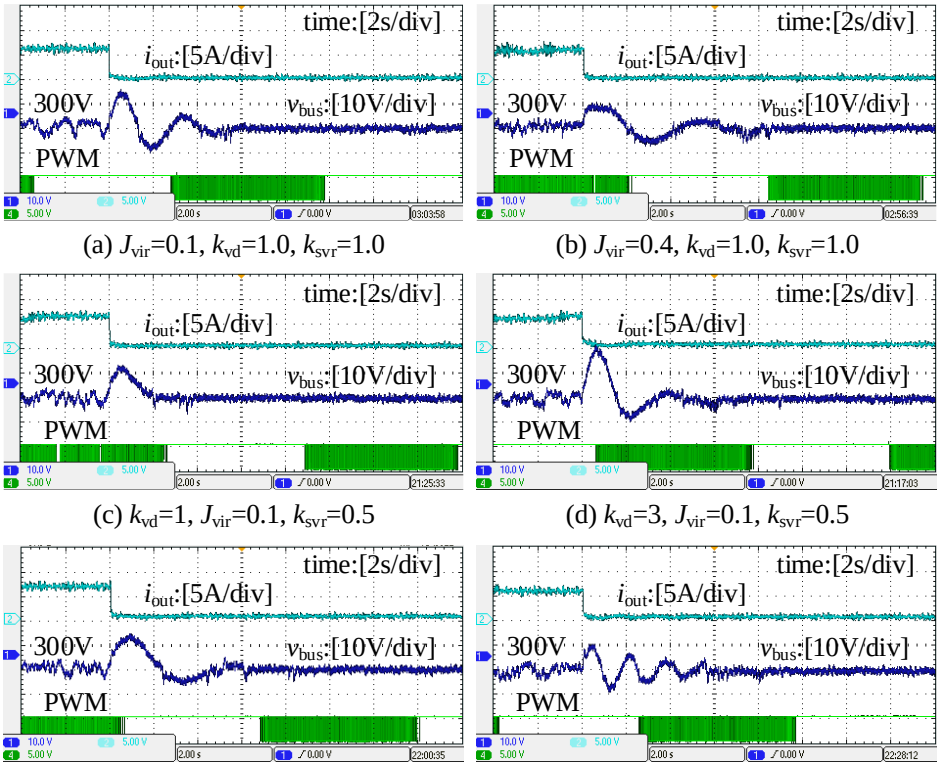


Figure 5.22: Configuration of the experimental setup.

(a) Experiment with different control parameters:

The experimental results with different control parameters are shown in Figure 5.23. It can be seen from Figure 5.23(a) and (b) that increasing J_{vir} can suppress RoCoV apparently, indicating the inertia is enhanced. From Figure 5.23(c) and (d), it can be concluded that the system damping will be reduced and the oscillation amplitude is amplified with the increase of k_{vd}, which is

due to the positive feedback of k_{vd} in the droop loop. From Figure 5.23(e) and (f), it can be observed that the oscillation frequency will increase as k_{svr} becomes larger. Although k_{svr} can accelerate the voltage recovery to the rated value, its interaction with J_{vir} will also exacerbate the voltage-LFO. The above experimental result analysis is in good agreement with the impedance model and the HIL experiment results, the correctness of the proposed multi-timescale impedance modeling method is thus validated.



(a) J_{vir}=0.1, k_{vd}=1.0, k_{svr}=1.0 (b) J_{vir}=0.4, k_{vd}=1.0, k_{svr}=1.0

(c) k_{vd}=1, J_{vir}=0.1, k_{svr}=0.5 (d) k_{vd}=3, J_{vir}=0.1, k_{svr}=0.5

(e) k_{svr}=0.5, k_{vd}=1, J_{vir}=0.2 (f) k_{svr}=5, k_{vd}=1, J_{vir}=0.2

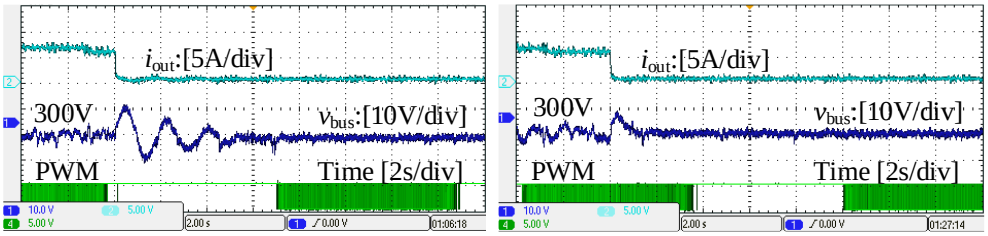
Figure 5.23: Experiment results with different control parameters. (a) J_{vir}=0.1, k_{vd}=1.0 and k_{svr}=1.0. (b) J_{vir}=0.4, k_{vd}=1.0 and k_{svr}=1.0. (c) k_{vd}=1, J_{vir}=0.1 and k_{svr}=0.5. (d) k_{vd}=3, J_{vir}=0.1 and k_{svr}=0.5. (e) k_{svr}=0.5, k_{vd}=1 and J_{vir}=0.2. (f) k_{svr}=5, k_{vd}=1 and J_{vir}=0.2.

(b) Experiment with PDRLs:

The experiment results with the proposed PDRLs are shown in Figures 5.24 and 5.25. It can be seen from Figure 5.24 that PDRL-*a* can effectively counteract the positive feedback introduced by k_{vd} in the droop control loop and enhance the system damping. Therefore, the voltage oscillation is better damped and the oscillation amplitude is significantly reduced. Seen from Figure 5.25, PDRL-*b* can counteract part of the negative damping effect of CPL, the voltage LFO can thus be mitigated. The experiment results are consistent with theoretical analysis that PDRLs can suppress voltage LFO amplitude by improving system damping.

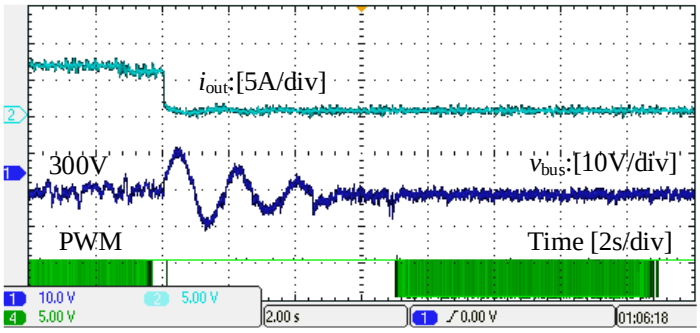
(c) Experiment with SC:

The experiment results of the SC with the proposed timescale-based coordination control are shown in Figure 5.26. Apparently, RoCoV is further mitigated during the dynamic process, due to that SC responds to the high-frequency components of power fluctuations. Both the oscillation amplitude and frequency are reduced, indicating the system inertia is enhanced in a wider bandwidth under the coordination effect of battery and SC. Note: due to the Oscilloscope, the PWM waveform is not fully displayed.

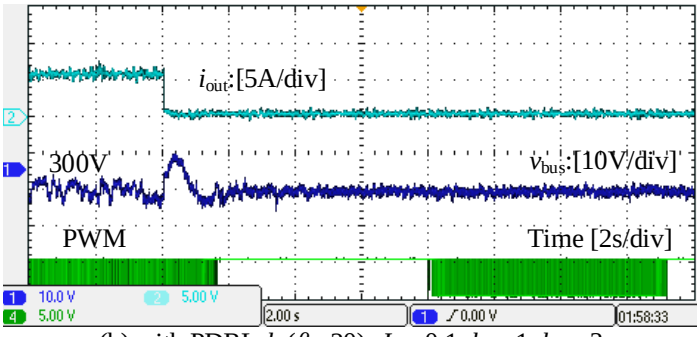


(a) without PDRL-*a*, J_{vir}=0.1, k_{vd}=1, k_{svr}=3 (b) with PDRL-*a*, J_{vir}=0.1, k_{vd}=1, k_{svr}=3

Figure 5.24: Experiment results with PDRL-*a*. (a) Without PDRL-*a*, J_{vir}=0.1, k_{vd}=1 and k_{svr}=3. (b) With PDRL-*a*, J_{vir}=0.1, k_{vd}=1.0 and k_{svr}=3.

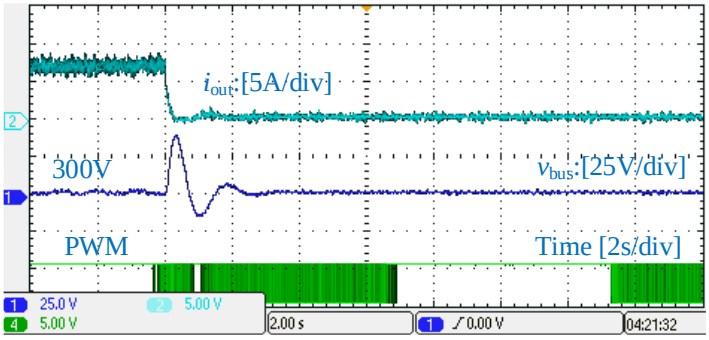


(a) without PDRL-*b*, J_{vir}=0.1, k_{vd}=1, k_{svr}=3

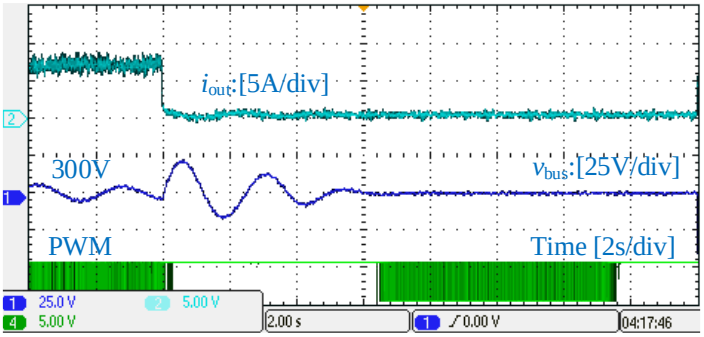


(b) with PDRL-*b* (β =20), J_{vir}=0.1, k_{vd}=1, k_{svr}=3

Figure 5.25: Experiment results with PDRL-*b* (β=20). (a) Without PDRL-*b*, J_{vir}=0.1, k_{vd}=1 and k_{svr}=3. (b) With PDRL-*b* (β=20), J_{vir}=0.1, k_{vd}=1.0 and k_{svr}=3.



(a) without SC, J_{vir}=0.05, k_{vd}=1.5, k_{svr}=1



(b) with SC, J_{vir}=0.05, k_{vd}=1.5, k_{svr}=1

Figure 5.26: Experiment results with SC. (a) Without SC, J_{vir}=0.05, k_{vd}=1.5 and k_{svr}=1. (b) With SC, J_{vir}=0.05, k_{vd}=1.5 and k_{svr}=1.

5.6 Conclusion and Discussion

In order to explore the interaction stability mechanism and stabilization control optimization of the islanded VIDC-DC-MG more systematically, a multi-timescale impedance model is established and analyzed in this chapter. Control loops are visualized as LVIs to form an impedance circuit. The impedance essence and interaction of the control loops/parameters are revealed, providing new insight into the mechanism analysis of low-frequency oscillation. Besides, more comprehensive and in-depth investigation has been performed on the physical interpretation of the control process, the instability factor identification, and stability enhancement methods. Some conclusions are drawn:

1) System stiffness, dissipation characteristics and inertia are characterized by k_{svr}, k_{vd}, and J_{vir}, which correspond to the abilities of recovery, damping and disturbance rejection.

2) The low-frequency oscillations in voltage- and inertia- loops are explained by the *RLC* models of LVIs. The interaction between C_{out} and k_{vi} causes low-frequency oscillation at the voltage-loop timescale. The interaction between k_{svr} and J_{vir} induces low-frequency oscillation at the inertia-loop timescale.

3) Virtual inertia loop and CPL introduce PFB to the DC-MG, deteriorating the low-frequency

oscillation. Y_{droop} and $Z_{vir}(s)$ behave negative admittance at high frequency, which cannot effectively suppress RoCoV at the initial stage of dynamic process.

4) PDRL is proposed to compensate for the ND of Y_{vd} and Y_{cpl} in inertia-loop bandwidth and suppress oscillation amplitude. SC is added to improve high-frequency inertia. Specifically, the voltage-loop oscillation frequency is reduced to the inertia-loop timescale by SC, and is mitigated by PDRLs.

Impedance passivity analysis assesses system stability. Finally, simulation and experiment have validated the proposed impedance modeling and stability enhancement method.

The proposed model has the following characteristics.

a) The impedance calculation is transformed from a multi-variable-coupled algebra problem to a multi-loop block-diagram-algebra problem, that is, a visual block-diagram-simplification process reflecting the impedance-shaping effect of each loop. A series/parallel impedance circuit is obtained to replace the conventional all-in-one impedance transfer function.

b) The conventional all-in-one impedance is expanded into discrete LVIs of a multi-timescale impedance circuit. The stability mechanism and low-frequency oscillation (*LC* impedance interaction) are visualized more intuitively and clearly. Therefore, parameter design can be straightforwardly guided by the passivity evaluation of system impedance.

c) The essence of the proposed multi-timescale impedance model is a gray-box modelling framework, which serves as a bridge between black-box and white-box modeling. It embodies the mapping relationship between parameters and impedance elements. As well as, the derivation process is simplified and the comprehensiveness of system information is not required.

d) When deriving the impedance model, linearization is only applied for CPL and other units do not require linearization, simplifying the calculation process.

6 An Inertia-Emulation based Cooperative Control Strategy and Parameter Design for Multi-parallel Energy Storage Systems in Islanded DC Microgrids

A multi-parallel energy storage system (ESS) is indispensable as the supporting energy source in islanded DC microgrid (DC-MG) and the battery cell is the widely used energy storage unit (ESU). The ESU parameter mismatches, such as various series resistances, different self-discharge rates, and uneven operation temperatures among ESUs, result in divergence of state of charge (SoC) among ESUs significantly. Thus, the unbalanced SoC leads to over-charge/-discharge and even explosions, degrades the utilization of some ESUs and shortens the operation lifespan of batteries. Besides, the bidirectional DC converter (BiC) is essential to connect ESS to the DC bus and realize the voltage conversion, making islanded DC-MG an inertia-less system. Hence, in addition to the dynamic stability problem, another issue in islanded DC-MG is to achieve the SoC balance of multi-parallel ESS.

To address the aforementioned issues, focusing on both the SoC self-balance among ESUs and system stability enhancement, an inertia-emulation based cooperative control strategy is proposed in this chapter. According to the real-time SoC information, the SoC-integrated droop resistance is redefined as an adaptive droop coefficient, and the auxiliary power and voltage regulation of ESS are fully explored to enhance the system inertia and achieve voltage recovery. The proposed SoC self-balance algorithm can dynamically adjust the delivered power to eliminate SoC divergences and a SoC equalization speed adjustment factor k is introduced to regulate the convergence speed. Considering various constraints, the optimal selection of k is carried out in detail. Compared with integrator-based SoC balance methods, the proposed strategy has better extensibility because of its simpler parameter design. Moreover, the inertia emulation loop (IEL) is derived from the physical model of motors, while the secondary voltage recovery (SVR) loop is constructed based on the circuit equivalence of inductors to reflect the system stiffness and achieve zero steady-state voltage errors. Control principle and implementation, stability analysis of each loop and parameter design considering various constraints are presented in detail. Simulation and hardware in the loop (HIL) experiment verify the performance of the proposed control strategy.

The content of this chapter has been published in "*IET Generation, Transmission & Distribution*" [M4].

6.1 Principle of SoC Self-balance Algorithm and IEL

From Figure 1.1, the overall block diagram of islanded DC-MG with multi-parallel ESS is presented in Figure 6.1. Each energy storage unit (ESU, battery usually) is connected in parallel to the DC bus and controlled by the proposed strategy. Zone II, i.e., the load subsystem, consists of other power supply unit and constant power loads (CPL), their output power and consuming power are P_s and P_{const}. Therefore, the net power of zone II is P_{net}=P_{const}-P_s. The positive and negative value of P_{net} indicated the discharging- and charging-mode of ESS.

As shown in Figure 6.1, the front end of BiC is connected with ESU and its back end is linked to DC bus via DC cable. v_{in} and v_{out} are the input and output voltage of BiC; i_b and i_{out} are the input and output current of BiC. L_s, R_s and C_{out} are the filter inductance, resistance, and output capacitor, respectively.

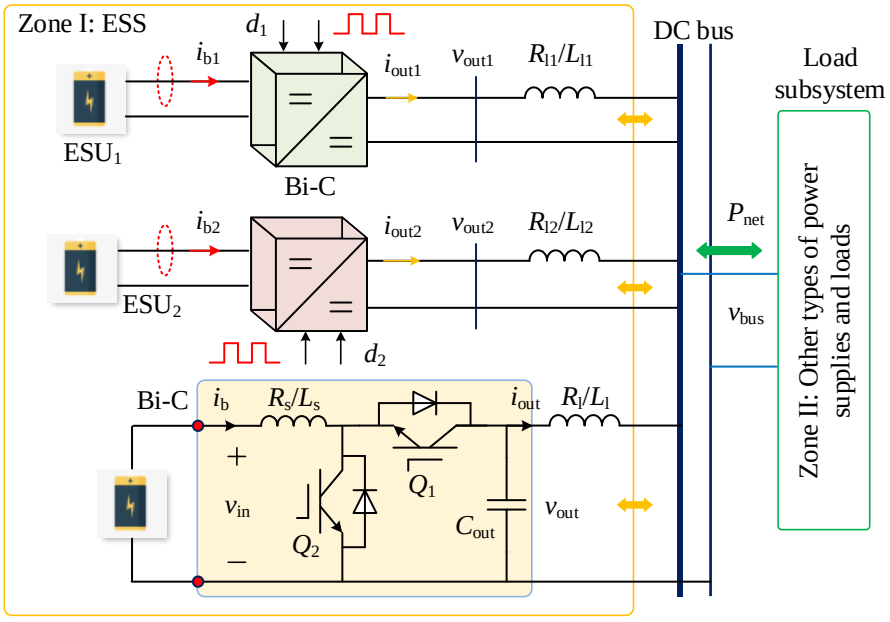


Figure 6.1: The overall block diagram of multi-parallel ESS in islanded DC-MG.

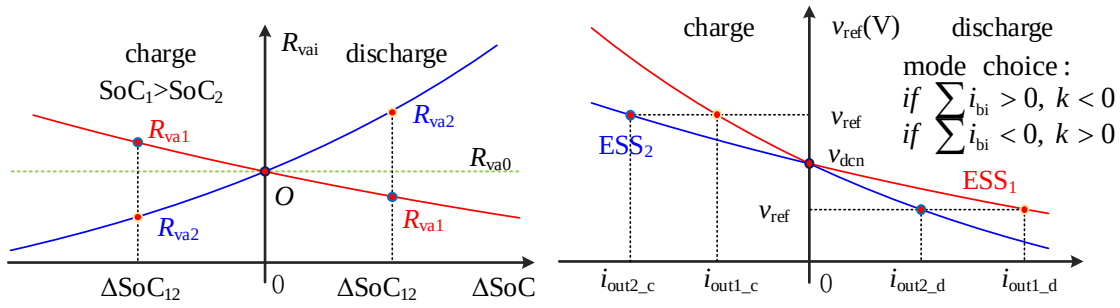
6.1.1 Principle of SoC self-balance algorithm

Droop control is implemented to operate ESS in parallel as shown in (6.1). In order to promote SoC equalization, ESS should operate in the manner that the ESU with higher SoC should release more power in discharge mode and absorb less power in charge mode than the one with lower SoC. Thus, the SoC difference ΔSoC_{ij} (ΔSoC_{ij}=SoC_i-SoC_j) would be removed, avoiding uneven use and expanding their lifespan. Subscripts 'i' and 'j' are the ESU identifier index.

$$i_{\mathrm{outi}} \approx i_{\mathrm{outi}}^{\mathrm{ref}} = (v_{\mathrm{dcn}} - v_{\mathrm{outi}})/R_{\mathrm{vai}} \tag{6.1}$$

$$\begin{cases} R_{\mathrm{vai}}(\mathrm{SoC_i}) = R_{\mathrm{vai}}^{0} \cdot \mathrm{SoC_i}^{-k\lambda_{\mathrm{i}}}, i = 1, 2, \ldots, n \\ \lambda_{\mathrm{i}} = \mathrm{SoC_i} - \mathrm{SoC_{av}},\ \mathrm{SoC_{av}} = \sum_{i=1}^{n} \mathrm{SoC_i}/n \end{cases} \tag{6.2}$$

A SoC-integrated droop resistance $R_{\mathrm{vai}}(\mathrm{SoC_i})$ is redefined in SoC self-balance algorithm, as shown in (6.2). Thus, power would be redistributed to balance SoC in charge and discharge mode. R_{vai}^{0} is the initial value of R_{vai} and is designed based on traditional droop method [138]. k is the SoC equalization speed adjustment factor and selected to be negative in discharge mode and positive in charge mode, affecting the SoC convergence speed. It is worth noticing that λ_{i} is a time-varying parameter indicating the SoC mismatch degree among $\mathrm{SoC_i}$ and the average SoC ($\mathrm{SoC_{av}}$), and also affects the SoC balance speed according to the time-varying $\mathrm{SoC_i}$, which is a novel contribution of this chapter. It can be observed from (6.2) that R_{vai} will return to R_{vai}^{0} and power distribution will become equal, as λ_{i} gradually converges to 0. Note that k and λ_{i} affect the balance speed as exponent forms. Moreover, in order to avoid frequent actions of the SoC self-balance algorithm when there is a slight SoC difference $\Delta\mathrm{SoC_{ij}}$, a small threshold of 0.3% is set to activate this SoC self-balance algorithm, that is, only when $\Delta\mathrm{SoC_{ij}}$ is larger than 0.3%, this algorithm will be activated.



(a) SoC-integrated droop resistance (b) the proposed droop characteristic

Figure 6.2: The illustration of droop characteristics with SoC self-balance algorithm. (a) SoC-integrated droop resistance. (b) The proposed droop characteristic.

This SoC self-balance algorithm is explained in Figure 6.2. For the sake of simple analysis, taking the ESS composed of two ESUs as an example, the relation between R_{vai} and $\Delta\mathrm{SoC_{ij}}$, and the droop characteristic are in Figure 6.2(a) and (b), respectively. In the discharge mode with k<0, $\mathrm{ESU_1}$ with higher $\mathrm{SoC_1}$ would supply more power at $i_{\mathrm{out1\_d}}$ than $\mathrm{ESU_2}$ with lower $\mathrm{SoC_2}$ does at $i_{\mathrm{out2\_d}}$ because of R_{va1}<R_{va2}. This implies that the SoC values of each ESU will move closer to each other to eliminate $\Delta\mathrm{SoC_{12}}$ till λ_{i}=0. Then, all ESUs would charge or discharge at the same rate, maintaining λ_{i}=0. Consequently, SoC self-balance algorithm equalize the SoC gradually and can perform well in SoC-unbalanced scenarios.

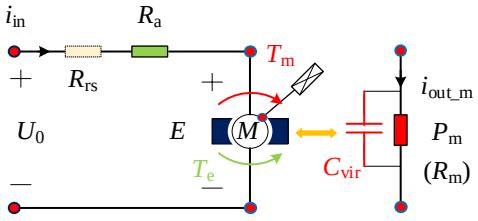
6.1.2 The design of IEL and SVR loop

By analogy with the circuit model of the DC motor, the control equation of IEL is derived for BiC in this section.

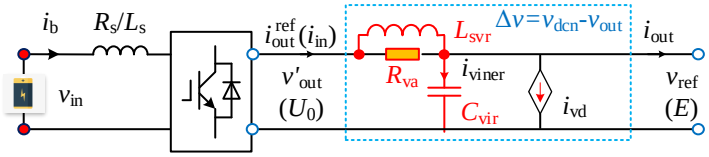
The circuit model of DC motor is shown in Figure 6.3(a). U_0 is the input voltage of motor and E is armature winding induced potential. R_a is armature winding resistance, and R_{rs} is the speed regulating resistance to change the operation point and regulate the output power. M is the mechanical inertia of DC motor, representing the role of rotor kinetic energy in the dynamic process. D_{damp} is the damping coefficient, describing the friction effect. P_m is the introduced electrical power to simulate the mechanical power with respect to load torque T_m. Thus, the mechanical load and the kinetic energy are modelled by an additional resistance R_m and a virtual capacitor C_{vir} storing inertia energy. C_{Tm} and ψ_m are torque coefficient and magnetic flux. ω is the rotor speed and ω_{on_m} is its rated value. The circuit formula is shown in (6.3) and power balance equations is expressed as (6.4). The stored kinetic energy can effectively restrain voltage fluctuation caused by power imbalance. With M increasing, RoCoV becomes smaller.

$$\begin{cases} E = U_0 - i_{in}(R_a + R_{rs}) & (a) \\ E = C_{Tm} \cdot \Psi_m \cdot \omega & (b) \\ P_m = \omega \cdot T_m & (c) \end{cases} \tag{6.3}$$

$$P_e - P_m - \frac{D_{damp} \cdot \omega_{on\_m}}{C_T \Psi}(E - v_{dcn}) = \frac{\omega \cdot M}{C_T \Psi} \cdot \frac{dE}{dt} \approx \frac{\omega_{on\_m} \cdot M}{C_T \Psi} \cdot \frac{dE}{dt} = C_{vir} \frac{dE}{dt} \tag{6.4}$$



(a) DC motor model



(b) the equivalent model of the IEL with SVR

Figure 6.3: Mapping between BiC and DC motor, and equivalent model for IEL. (a) DC motor model. (b) The equivalent model of the IEL with SVR.

Based on the voltage inertia characteristics of DC motor from Figure 6.3(a), the IEL equation is obtained as in (6.5) and (6.6). Its essence is a systematic coordination of virtual capacitor,

active damping and virtual resistance by properly exploring the auxiliary power of ESU to perform inertia and droop feature. The equivalent model of IEL is in Figure 6.3(b).

$$i_{\mathrm{out}}^{\mathrm{ref}} - i_{\mathrm{out}} - i_{\mathrm{vd}} + i_{\mathrm{svr}} \approx \frac{\omega_{\mathrm{on}} M_{\mathrm{vir}}}{v_{\mathrm{dcn}} C_{\mathrm{T}} \Psi} \frac{\mathrm{d}v_{\mathrm{ref}}}{\mathrm{d}t} = J_{\mathrm{vir}} \frac{\mathrm{d}(v_{\mathrm{ref}} - v_{\mathrm{dcn}})}{\mathrm{d}t} = i_{\mathrm{viner}} \tag{6.5}$$

$$\begin{cases} i_{\mathrm{out}}^{\mathrm{ref}} = (v_{\mathrm{dcn}} - v_{\mathrm{out}} + \Delta v_{\mathrm{SVR}})/R_{\mathrm{va}} & (a) \\ i_{\mathrm{vd}} = D_{\mathrm{d}}(v_{\mathrm{ref}} - v_{\mathrm{out}}) & (b) \\ i_{\mathrm{svr}} = \left[k_{\mathrm{s}} \int (v_{\mathrm{dcn}} - v_{\mathrm{out}})\,\mathrm{d}t\right]/R_{\mathrm{va}} = \Delta v_{\mathrm{SVR}}/R_{\mathrm{va}} & (c) \end{cases} \tag{6.6}$$

In Eq. (6.5), v_{dcn} is the rated value of v_{out}. $i_{\mathrm{out}}^{\mathrm{ref}}$ is the output current reference, which mainly includes i_{vd} (the virtual damping current), i_{viner} (the virtual inertia current), i_{svr} (the virtual inductor current), and i_{out}. The physical significance of $i_{\mathrm{out}}^{\mathrm{ref}}$ is to represent energy supply that mimic i_{in}. v_{ref} is the virtual internal potential emulating E. R_{va} is the virtual droop resistance in series on BiC output side, making the BiC present droop feature. Consequently, $i_{\mathrm{out}}^{\mathrm{ref}}$ is obtained by the droop feature, as shown in (6.6a). C_{Tm} and ψ_{m} are the virtual torque coefficient and magnetic flux of IEL. J_{vir} and D_{d} are the introduced virtual inertia and damping coefficient, respectively. The introduced J_{vir} represents the virtual (static) rotor M_{vir}, and can be equivalent to the virtual capacitor C_{vir} as shown in Figure 6.3(b), mitigating voltage oscillation by supplying or absorbing power mismatch. Damping current i_{vd} is added to prevent voltage from deviating its rated value, thus it is defined in proportional to the voltage deviation as shown in (6.6b). i_{vd} is provided till the voltage returns to its reference value.

Based on the circuit equivalence that inductors behave as short circuit at long-time limit while open circuit at short-time limit, virtual-inductor-based SVR is developed and its control law is derived as (6.6c). k_{s} is the stiffness coefficient, revealing the voltage recovery speed. The equivalent model is presented in Figure 6.3(b) and L_{svr} refers to the virtual inductor. At long-time limit, the virtual inductor short-circuits R_{va} and i_{out} is transferred from R_{va} to L_{svr}, thus the voltage deviation Δv is eliminated.

Table 6.1 Analogy between DC motor and IEL with SVR

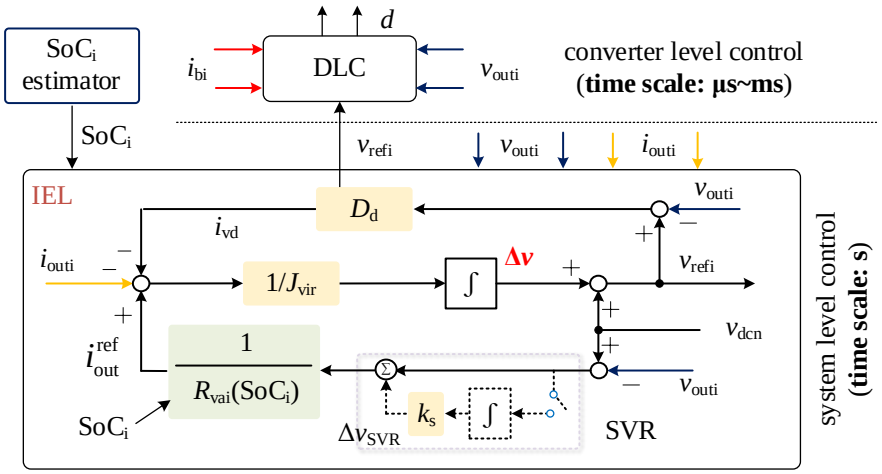
Physical meaning	DC Motor and Inductor	*RLC* model of IEL
Moment of inertia	Rotor (M)	ESS M_{vir} (J_{vir})
Damping source	The friction (D_{damp})	i_{vd} (D_{d})
Stiffness	L	i_{svr} of L_{svr}(k_{s})
Droop characteristic	R_{a}+R_{rs}	R_{va}
Input voltage	U_0	v'_{out} (v_{dcn})
Output voltage	E	v_{ref} (v_{out})
Load	T_{m} (P_{m})	P_{out}
Excitation constant	C_{Tm}·ψ_{m}	C_{T}·ψ
Input current	i_{in}	$i_{\mathrm{out}}^{\mathrm{ref}}$

Accordingly, the analogy between DC motor and BiC is in Table 6.1. The control parameters

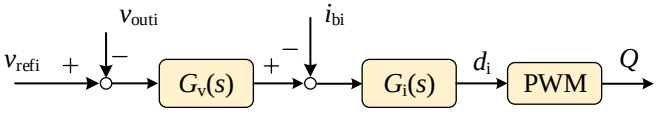
are given a clearer physical meaning. The inertia and damping power of BiC originate from ESS instead of the rotational kinetic energy. i_{viner} will be produced, when the voltage oscillates, to provide inertia and suppress voltage fluctuation, and more inertia current will be produced if oscillation frequency increases. Note that the oscillation frequency declines as J_{vir} increases in the scenario requiring the same inertia current. i_{vd} is generated when voltage deviates from its reference value, indicating voltage deviation is dependent to D_d. In order to attain better performance, larger D_d, leading to smaller voltage deviation, is preferred. The proposed strategy enables BiC to have inertia and damping features, and (self-adaptive) droop characteristics. The detail control diagram is depicted in Figure 6.4.

6.1.3 The illustration of the proposed cooperative control strategy

Combining Eqs. (6.1)-(6.2) and (6.5)-(6.6), the overall block diagram of the inertia-emulation based cooperative control strategy is illustrated in Figure 6.4, mainly including SoC self-balance algorithm, IEL and SVR part, and dual loop control (DLC). The detail explanation of DLC is shown in Figure 6.4(b) [54]. $G_v(s)$ and $G_i(s)$ are the voltage-loop and current-loop regulator. d_i is the duty cycle.



(a) IEL and SVR loop



(b) dual loop control in detail

Figure 6.4: The block diagram of inertia-emulation based cooperative control strategy. (a) IEL and SVR loop. (b) Dual loop control in detail.

***SoC self-balance algorithm*:** SoC evaluator calculates the SoC_i, according to coulomb counting method, as shown in (6.7). C_e is the capacity of ESU. SoC should be within the constraint range in (6.8) to ensure the service life. SoC_{min} and SoC_{max} are the minimum and maximum values,

respectively. Then a central controller is required for SoC_{av}. Each ESU calculates their R_{vai} according to (6.2), regulating their delivered power based on the SoC_i to achieve SoC balance.

$$\mathrm{SoC_i} = \mathrm{SoC_{i,}}_{t=0} - \frac{1}{C_e}\int i_{bi}\,dt = \mathrm{SoC_{i,}}_{t=0} - \frac{1}{C_e}\int \frac{i_{outi}}{1-d_i}\,dt \tag{6.7}$$

$$\mathrm{SoC_{min}} \le \mathrm{SoC_i} \le \mathrm{SoC_{max}} \tag{6.8}$$

***IEL and SVR link*:** The IEL consists of virtual inertia loop and damping loop, which enable BiC to compensate power mismatch by using the energy in ESS, improving the system inertia and restraining the voltage fluctuation. The virtual inductor of SVR loop acts as a short circuit of R_{va} at steady state, and i_{out} is transmitted through the virtual inductor instead of R_{va}. Hence, Δv is eliminated.

***DLC*:** Dual loop control consists of voltage loop tracking v_{ref} accurately and current loop controlling the voltage indirectly, improving the control performance.

From Figure 6.4, the SoC self-balance algorithm are at system level because droop feature is from the redefined R_{va}. The timescale of system level control is second, while the timescale of converter level control is microsecond or millisecond. Therefore, bandwidth of each loop can be coordinated better and easier, enhancing the voltage tracking ability. SoC_i need not be updated fast due to its slow variation and its update cycle is 0.01s. Hence, only low-bandwidth communication is necessary and the impact of communication delay (microseconds usually) is not explicitly considered in this chapter because the communication latency is much less than the time of SoC updating [148].

Normally, the resistance of DC cable is very small, thus the voltage droop across transmission cable can be ignored as (6.9) [144]. Consequently, the power sharing relation among ESUs with the same capacities is in (6.10).

$$v_{out1} \approx v_{out2} \approx \cdots \approx v_{outn} \tag{6.9}$$

$$i_{out1} : i_{out2} : \cdots : i_{outn} \approx i_{b1} : i_{b2} : \cdots : i_{bn} \approx \mathrm{SoC_1^{k\lambda_1}} : \mathrm{SoC_2^{k\lambda_2}} : \cdots : \mathrm{SoC_n^{k\lambda_n}} \tag{6.10}$$

The above analysis is for ESUs with the same capacity. When the ESU capacities differ significantly, R_{vai}^0 is chosen according to their capacity ratio, ensuring that the charge and discharge power can be allocated reasonably. Thus, this SoC self-balance algorithm is also suitable for ESUs with different capacities.

6.2 Dynamic Performance and Stability Analysis

Taking ESS with two ESUs as example, SoC balance speed regulation, stability analysis of SoC

self-balance algorithm and small-signal stability analysis of IEL are presented.

6.2.1 SoC balance speed adjustment

Combining (6.7) and (6.10), it yields (6.11). Selecting C_e=3 Ah, i_{load}=6 A, $SoC_{1,\,t=0}$=50%, $SoC_{2,\,t=0}$=40% and $R^0_{va1,\,2}$=2, the numeric solution of (6.11) in discharge mode is obtained as in Figure 6.5(a). The delivered power and R_{vai} are shown in Figure 6.5(b) and (c). The related data is in Table 6.2 when t=800s. It is shown that, under the same ΔSoC_{12}, larger k would enlarge the differences of R_{vai} and i_{outi}, balancing SoC in shorter time. At t=800s, ΔSoC_{12} is 0.9%, 2.360% and 4.812% when k is -10, -6 and -3, respectively. From Figure 6.5(b) and (c), the delivered power is inversely proportional to R_{vai}. R_{va1} of ESU_1 with higher SoC would be smaller to release more energy. As a result, SoC_1 and SoC_2 balance dynamically, then R_{vai} return to R^0_{vai}.

$$SoC_i = SoC_{i,t=0} - \frac{i_{load}}{C_e}\int SoC_i^{k\lambda_i} \Big/ \sum_{i=1}^{n} SoC_i^{k\lambda_i}\, dt \tag{6.11}$$

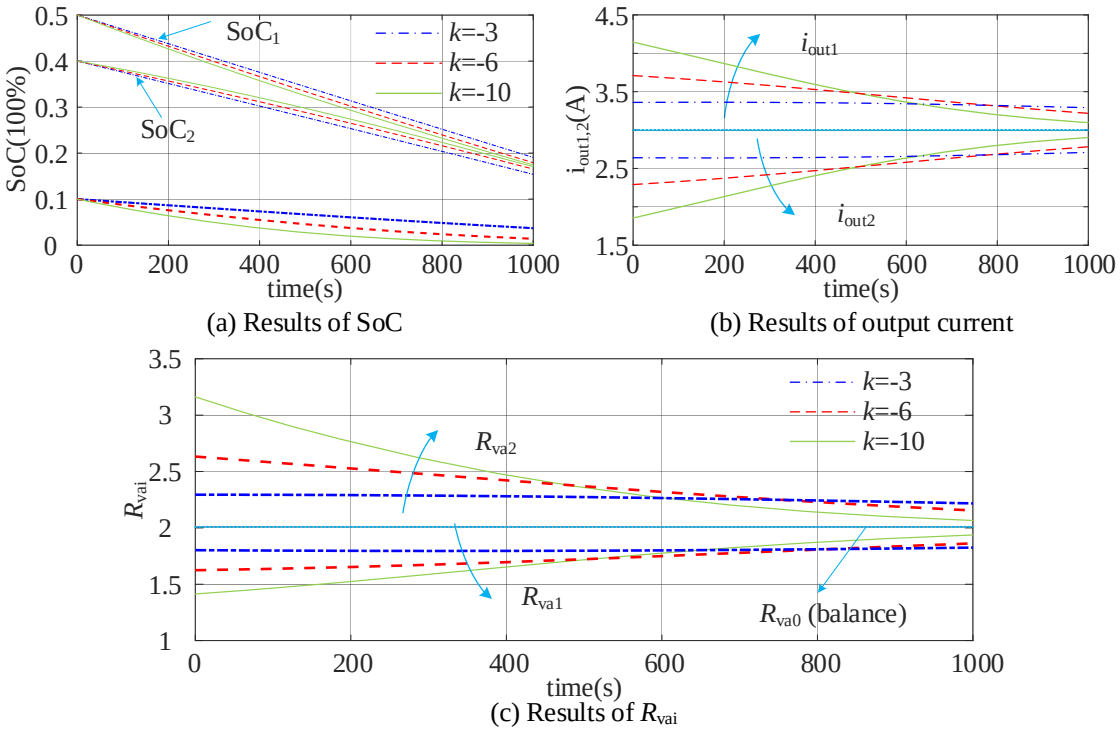


Figure 6.5: SoC balance speed regulation with different k. (a) Result of SoC. (b) Result of output current. (c) Result of R_{vai}.

6.2.2 Stability analysis of the SoC self-balance algorithm

The stability of the SoC self-balance algorithm is evaluated by small signal analysis. Since the DLC bandwidth is much higher than SoC self-balance algorithm, a unity gain block represents the closed-loop gain of DLC. Perturbing (6.1), there is:

$$\frac{-\Delta v_{\mathrm{outi}}}{v_{\mathrm{dcn}}-v_{\mathrm{outi}}}=\frac{-k_{\mathrm{dci}}}{i_{\mathrm{outi}}}\Delta \mathrm{SoC_i}+\frac{\Delta i_{\mathrm{outi}}}{i_{\mathrm{outi}}},\quad \mathrm{i}=1,2 \tag{6.12}$$

$$k_{\mathrm{dc1}}=ki_{\mathrm{out1}}[(\mathrm{SoC_1}-\mathrm{SoC_2})/\mathrm{SoC_1}+\ln(\mathrm{SoC_1})] \tag{6.13a}$$

$$k_{\mathrm{dc2}}=ki_{\mathrm{out2}}[(\mathrm{SoC_2}-\mathrm{SoC_1})/\mathrm{SoC_2}+\ln(\mathrm{SoC_2})] \tag{6.13b}$$

Table 6.2 Numeric solution of SoC balance regulation when *t*=800*s*

k	$\Delta\mathrm{SoC}_{12,\,t=800}$	R_{va1}	R_{va2}	i_{out1}	i_{out2}
-10	0.900%	1.868	2.146	3.208	2.792
-6	2.360%	1.808	2.229	3.313	2.687
-3	4.812%	1.811	2.243	3.320	2.680

Linearizing (6.7), it yields (6.14).

$$\Delta \mathrm{SoC_i}=-\frac{\Delta i_{\mathrm{bi}}}{sC_{\mathrm{e}}}=-\frac{v_{\mathrm{outi}}}{sv_{\mathrm{bi}}C_{\mathrm{e}}}\Delta i_{\mathrm{outi}}=-\frac{\Delta i_{\mathrm{outi}}}{sC'_{\mathrm{e}}} \tag{6.14}$$

Combining (6.11) and (6.14), (6.15) and (6.16) can be obtained. For zone II, the simplified model is shown in (6.17). Based on Kirchhoff's current law, the power balance equation is derived in (6.18).

$$\Delta i_{\mathrm{out1}}=-2si_{\mathrm{out1}}C'_{\mathrm{e}}\Delta v_{\mathrm{out1}}/[(v_{\mathrm{dcn}}-v_{\mathrm{out1}})(2sC'_{\mathrm{e}}+k_{\mathrm{dc1}})] \tag{6.15}$$

$$\Delta i_{\mathrm{out2}}=-2si_{\mathrm{out2}}C'_{\mathrm{e}}\Delta v_{\mathrm{out2}}/[(v_{\mathrm{dcn}}-v_{\mathrm{out2}})(2sC'_{\mathrm{e}}+k_{\mathrm{dc2}})] \tag{6.16}$$

$$\begin{cases} i_{\mathrm{load}}=v_{\mathrm{bus}}/R_{\mathrm{load}}\ ,\text{discharge mode} & (a) \\ i_{\mathrm{load}}=P_{\mathrm{const}}/v_{\mathrm{bus}}\ ,\text{charege mode} & (b) \end{cases} \tag{6.17}$$

$$\Delta i_{\mathrm{out1}}+\Delta i_{\mathrm{out2}}=\Delta i_{\mathrm{load}} \tag{6.18}$$

The state equation can be derived from (6.15) to (6.18) as follows.

$$As^2+Bs+C=0 \tag{6.19}$$

$$\begin{cases} A=4\cdot C'^2_{\mathrm{e}}\cdot(i_{\mathrm{out1}}+i_{\mathrm{out2}}+I_{\mathrm{det}}) \\ B=2\cdot C'_{\mathrm{e}}\cdot(i_{\mathrm{out1}}k_{\mathrm{dc2}}+i_{\mathrm{out2}}k_{\mathrm{dc1}}+I_{\mathrm{det}}(k_{\mathrm{dc1}}+k_{\mathrm{dc2}})) \\ C=k_{\mathrm{dc1}}\cdot k_{\mathrm{dc2}}\cdot I_{\mathrm{det}} \\ I_{\mathrm{det}}=(v_{\mathrm{dcn}}-v_{\mathrm{outi}})/R_{\mathrm{load}} \quad \text{discharge mode} \\ I_{\mathrm{det}}=P_{\mathrm{const}}\,(v_{\mathrm{dcn}}-v_{\mathrm{outi}})/v^2_{\mathrm{bus}} \quad \text{charge mode} \end{cases} \tag{6.20}$$

From (6.19), the dominant poles of SoC self-balance algorithm with different SoC and exponent *k* in charge and discharge mode is presented by using the parameters in Table 6.3, as shown in Figure 6.6. Usually, the SoC self-balance algorithm is an overdamped system, thus only one dominant pole left.

Figure 6.6(a) and (c) show the influences of $\mathrm{SoC_1}$ varying from 0.3 to 0.7 with $\mathrm{SoC_2}$=50% and $|k|$=1 in discharge and charge mode. The increasing of $\mathrm{SoC_1}$ leads to the pole moving away from the imaginary axis firstly, and then toward the imaginary axis, which indicates the stability is

firstly improved and then weakened. When the SoC of two ESUs is close, the stability is approximately the strongest. Figure 6.6(b) and (d) show the influences of $|k|$ varying from 0.1 to 10 in discharge and charge mode. With the increase of $|k|$, the pole moves away from the imaginary axis, improving the stability, because larger $|k|$ makes SoC balance faster. But current difference between ESUs is also greater and ESU_1 undertakes most of the load and is closer to its critical state, therefore an upper limit of $|k|$ is necessary and introduced later. In Figure 6.6, the pole is always on left half plane, so stability of SoC self-balance algorithm is guaranteed.

Table 6.3 System parameters of the studied multi-parallel ESS

	ITEMS	Value
Zone I	Input voltage v_s	100 V
	Input filter inductor L_s/R_s	5 mH/0.01 Ω
	Capacitance C_{out}	3000 μF
	Line impedance R_{li}/L_{li}	0.01 Ω/0.1 mH
	Initial value of R_{vai}/R_{vai}^0	2 Ω
	Sample frequency	10 kHz
Zone II	Bus voltage rating v_{dcn}	300 V
	Net power P_{net} (R)	2900 W
	Equivalent load R_{const}	30 Ω
Variable limitation	Δv_{out_max}	10 V
	Δi_{outi_max}	5 A
	Δi_{bi_max}	14 A

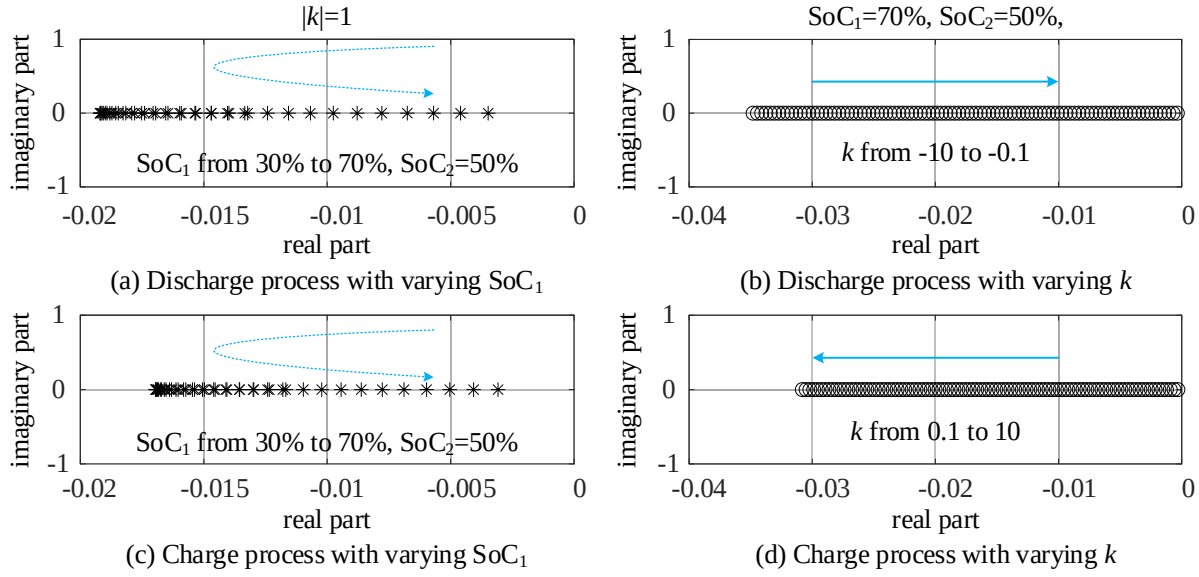


Figure 6.6: The dominant pole distribution of SoC self-balance algorithm. (a) Discharge process with varying SoC_1. (b) Discharge process with varying k. (c) Charge process with varying SoC_1. (d) Charge process with varying k.

6.2.3 Small signal stability analysis of inertia emulation loop

Ignoring the power loss of BiC, (6.21) can be derived from the power balance.

$$V_{\mathrm{s}}\Delta i_{\mathrm{s}} = (I_{\mathrm{out}} + s \cdot 2 \cdot C_{\mathrm{out}}V_{\mathrm{out}})\Delta v_{\mathrm{out}} + V_{\mathrm{out}}\Delta i_{\mathrm{out}} \tag{6.21}$$

Therefore, the relation between Δi_{out} and Δi_{b} can be obtained when virtual-inductor-based SVR is not connected.

$$G_{\mathrm{ii}} = \Delta i_{\mathrm{out}}/\Delta i_{\mathrm{b}} = V_{\mathrm{s}}/V_{\mathrm{out}} \tag{6.22}$$

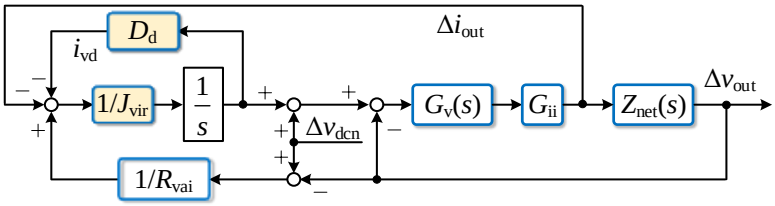


Figure 6.7: Small signal model of BiC with the proposed IEL.

The closed loop gain of current loop is equivalent to unity gain block. Based on (6.21), (6.22) and Figure 6.1, the small-signal model of IEL is established in Figure 6.7. $G_{\mathrm{v}}(s)$ is the voltage PI regulator. $Z_{\mathrm{net}}(s)$ is the small-signal impedance of Zone II and lines. The relation between Δv_{out} and Δi_{out} is in (6.23) and its physical significance is to reflect the dynamic response of v_{out} when i_{out} changes suddenly. The transfer function between Δv_{out} and Δv_{dcn} is in (6.24), reflecting the voltage tracking ability.

$$TF_{\mathrm{i\_id}} = \frac{\Delta v_{\mathrm{out}}}{\Delta i_{\mathrm{out}}} = \frac{-G_{\mathrm{v}} \cdot G_{\mathrm{ii}} \cdot Z_{\mathrm{net}}}{sJ_{\mathrm{vir}} + D_{\mathrm{damp}} + G_{\mathrm{v}} \cdot G_{\mathrm{ii}} \cdot Z_{\mathrm{net}}(1/R_{\mathrm{vai}} + sJ_{\mathrm{vir}})} \tag{6.23}$$

$$TF_{\mathrm{v\_id}} = \frac{\Delta v_{\mathrm{out}}}{\Delta v_{\mathrm{dcn}}} = \frac{(1/R_{\mathrm{vai}} + sJ_{\mathrm{vir}}) \cdot G_{\mathrm{v}} \cdot G_{\mathrm{ii}} \cdot Z_{\mathrm{net}}}{sJ_{\mathrm{vir}}(1 + G_{\mathrm{v}}G_{\mathrm{ii}}Z_{\mathrm{net}}) + D_{\mathrm{damp}} + G_{\mathrm{v}} \cdot G_{\mathrm{ii}} + G_{\mathrm{v}}G_{\mathrm{ii}} \cdot Z_{\mathrm{net}}/R_{\mathrm{vai}}} \tag{6.24}$$

The pole distribution of $TF_{\mathrm{i\_id}}(s)$ and step response of $TF_{\mathrm{v\_id}}(s)$, with varying D_{d} and J_{vir}, are presented, as in Figure 6.8. From Figure 6.8(a) and (b), remarkably, the BiC with IEL can be simplified to a 3rd-order system approximately, including a negative real root (representing the inertia component) and a pair of negative conjugate complex roots (representing low-frequency oscillation mode). In Figure 6.8(a), with D_{d} increasing from 2 to 7, the poles of oscillation mode move to real axis, and the damping increases firstly and then decreases. At about D_{d}=4, the damping is maximum. Besides, the time constant T_{iner} of the inertia component decreases with D_{d} increasing, indicating that system inertia is weakened. The opposite movement trend of poles, with J_{vir} increasing, can be observed in Figure 6.8(b). The damping of oscillation mode is first increased and then decreased, and the poles move away from real axis and oscillation frequency increases. The poles are always on the left half plane, confirming the stability of inertia emulation part. In Figure 6.8(c), with the increase of J_{vir} and D_{d}, the oscillation damping first increases and then decreases, which is consistent with Figure 6.8(a) and (b).

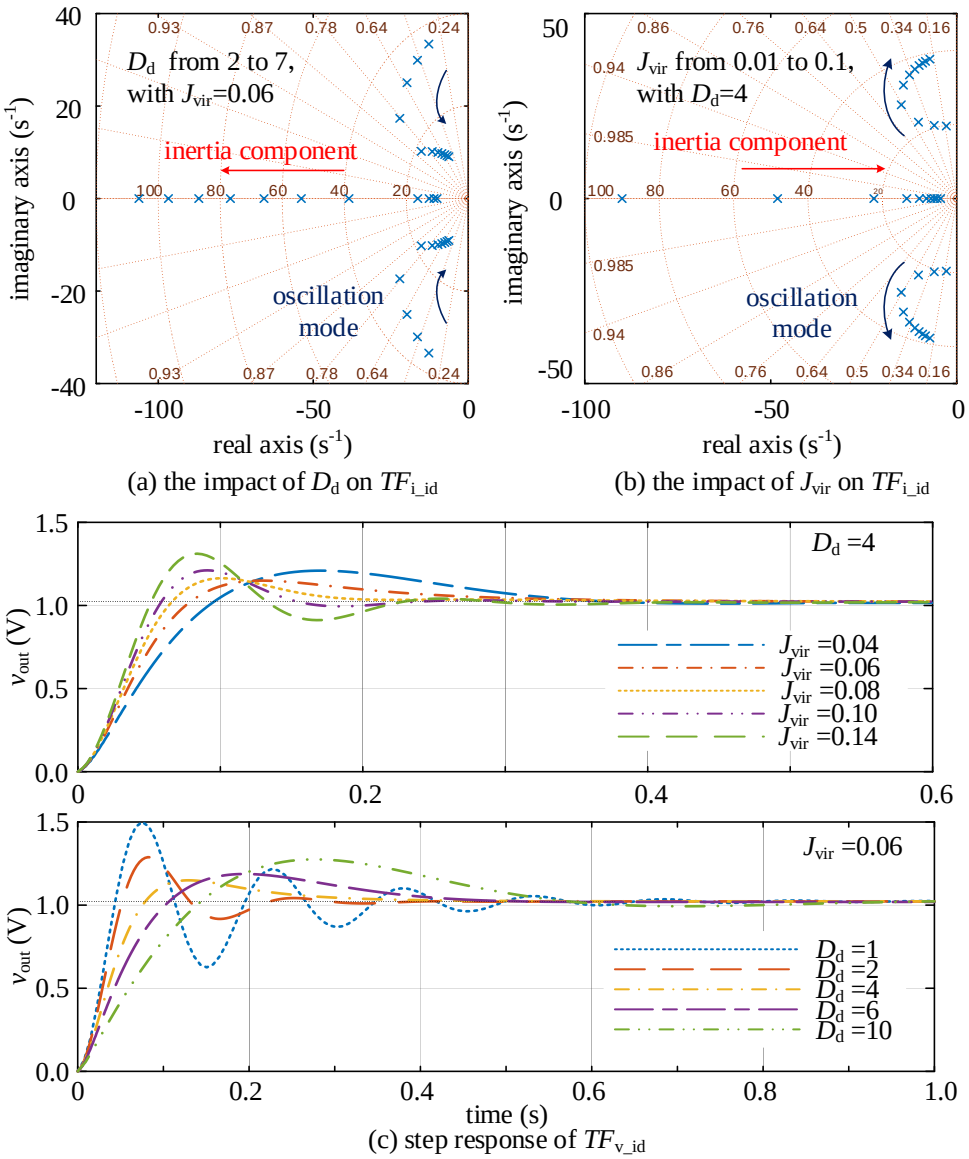


Figure 6.8: Dynamic stability analysis of BiC with the proposed IEL. (a) The impact of D_d on $TF_{i\_id}(s)$. (b) The impact of J_{vir} on $TF_{i\_id}(s)$. (c) Step response of $TF_{v\_id}(s)$.

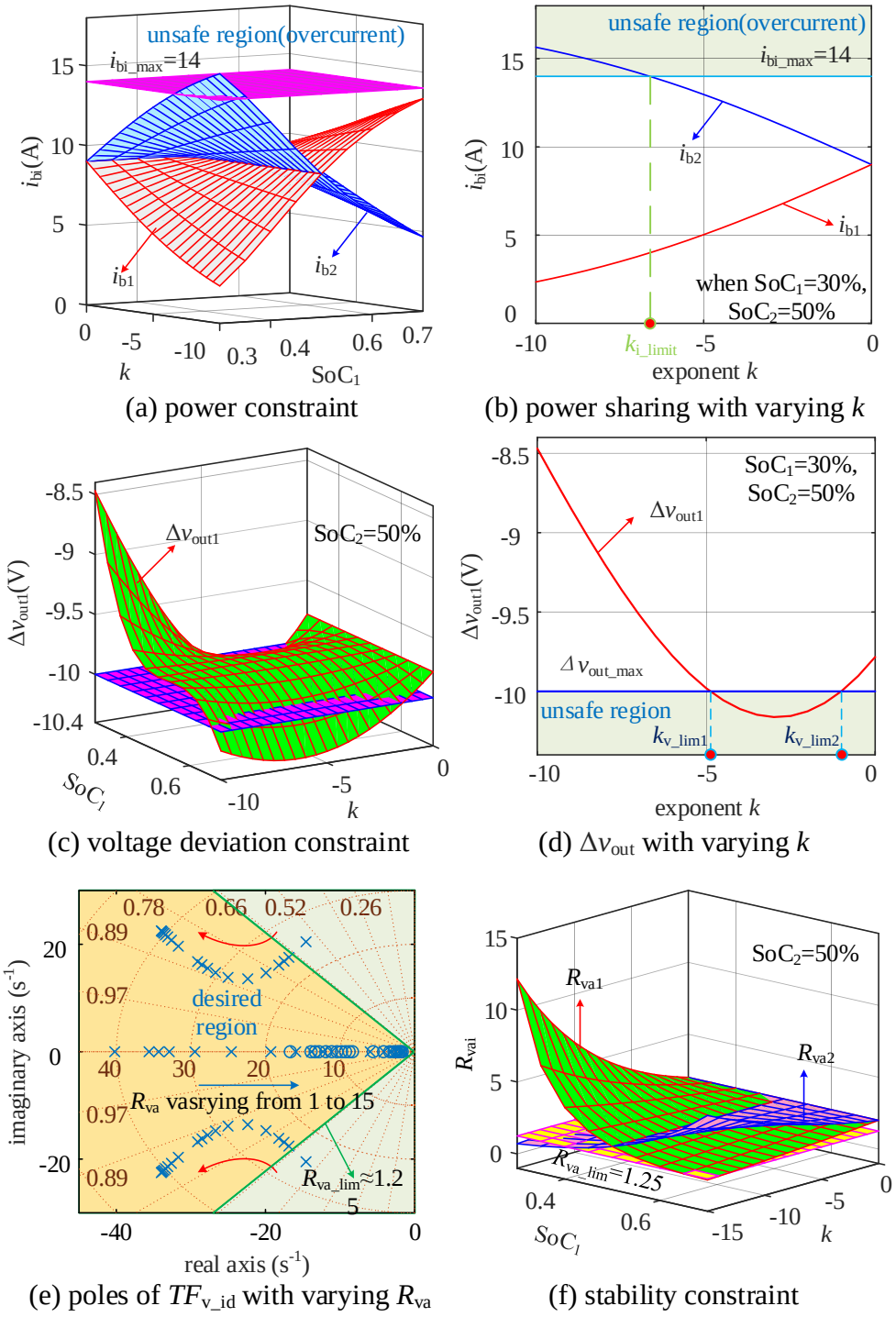
6.3 Parameters Optimal Design

In SoC self-balance algorithm, the exponent k changes the SoC balance speed by adjusting the power allocation. In this process, R_{vai} will be dynamically adjusted according to k and SoC, which would affect i_{outi}, v_{outi} and transient performance. Therefore, power constraint, voltage constraint and dynamic stability constraint should be considered while selecting k. Two ESUs in discharge mode is taken as an example. SoC_1 changes from 30% to 70% and $|k|$ changes from 0 to 10 with $SoC_{2,\,t=0}$ =50%.

6.3.1 Power constraint

The sharing of P_{net} can be derived from (6.10), as shown in (6.25), which is not only related to

k but also related to the ΔSoC_{ij} of ESU. The output/injected current of BiC and ESU should not exceed their maximum value, i.e. i_{outi_max} and i_{bi_max}.



(a) power constraint (b) power sharing with varying k

(c) voltage deviation constraint (d) Δv_{out} with varying k

(e) poles of TF_{v_id} with varying R_{va} (f) stability constraint

Figure 6.9: Different constraints for exponent k. (a) Power constraint. (b) Power sharing with varying k. (c) Voltage deviation constraint. (d) Δv_{out} with varying k. (e) Poles of $TF_{v\_id}(s)$ with varying R_{va}. (f) Stability constraint.

$$\begin{cases} i_{\text{outi}} = \left(\text{SoC}_\text{i}^{k\lambda_\text{i}} / \sum_{i=1}^{n} \text{SoC}_\text{i}^{k\lambda_\text{i}}\right) & i_{\text{load}} \le i_{\text{outi\_max}}(a) \\ i_{\text{bi}} = \left(\text{SoC}_\text{i}^{k\lambda_\text{i}} / \sum_{i=1}^{n} \text{SoC}_\text{i}^{k\lambda_\text{i}}\right) & \frac{v_{\text{outi}}}{v_{\text{si}}} i_{\text{load}} \le i_{\text{bi\_max}}(b) \end{cases} \tag{6.25}$$

Figure 6.9(a) shows how the power sharing would be affected by SoC_i and k. The larger k, with the same $\Delta\text{SoC}_\text{ij}$, enlarges the power allocation difference between ESUs, which might cause the ESU power to exceed its maximum though balancing SoC faster. The relation between i_{outi} and k, when ΔSoC_{12}=-20%, is in Figure 6.9(b). It can be found that the power released by ESU_2 exceeds its acceptable power rating when k exceeds $k_{\text{i_limit}}\approx$6.5, degrading its lifespan. Power constraint is an upper limit to k.

6.3.2 Voltage deviation constraint

The maximum voltage deviation Δv_{outi} caused by droop feature is another constraint of k. R_{vai}^{0} =2 can be obtained from (6.26). Combining (6.10) and (6.25), the quadratic equation of Δv_{outi} can be derived from (6.4a), as shown in (6.27). Δv_{outi} can be acquired by solving (6.27), as shown in (6.28). The other solution of (6.27) is rejected because it exceeds v_{dcn}. From (6.28), Δv_{outi} is affected by SoC_i, k and P_{net}, and their relation is shown in Figure 6.9(c). When $|\Delta\text{SoC}_{12}|$ is large, there would be a set of k making v_{outi} exceed its constraint value. Figure 6.9(d) shows the relation between Δv_{outi} and k, when ΔSoC_{12}=-20%. Δv_{outi} would locate in the unsafe region when $k \in [k_{\text{v\_lim1}}, k_{\text{v\_lim2}}]$, degrading power quality. Therefore, Eq. (6.28) provides a regional limit for k.

$$R_{\text{vai}}^{0} = \Delta v_{\text{outi\_max}} / \Delta i_{\text{outi\_max}} \tag{6.26}$$

$$\Delta v_{\text{outi}} = -\frac{R_{\text{vai}}^{0} i_{\text{load}}}{\sum_{i=1}^{n} \text{SoC}_\text{i}^{k\lambda_\text{i}}} = -\frac{R_{\text{vai}}^{0}}{\sum_{i=1}^{n} \text{SoC}_\text{i}^{k\lambda_\text{i}}} \frac{P_{\text{const}}}{v_{\text{outi}} + \Delta v_{\text{outi}}} \tag{6.27}$$

$$|\Delta v_{\text{outi}}| = \left| \left(-v_{\text{dcn}} + \sqrt{v_{\text{dcn}}^2 - 4\frac{R_{\text{vai}}^{0} P_{\text{const}}}{\sum_{i=1}^{n} \text{SoC}_\text{i}^{k\lambda_\text{i}}}}\right) \Big/ 2 \right| \le \Delta v_{\text{out\_max}} \tag{6.28}$$

6.3.3 Dynamic stability constraint

As mentioned before, R_{vai} is regarded as a virtual impedance connected in series on the BiC output side, affecting the system damping ξ. According to (6.24), the influence of R_{vai} on the system dynamic characteristics is shown in Figure 6.9(e). Note that ξ first increases and then decreases with R_{vai} increasing. To ensure a good dynamic response, ξ should not be less than 0.707, thus from Figure 6.9(e), R_{vai} should not be less than $R_{\text{va\_lim}}$=1.25. Considering (6.6), the dynamic stability constraint is in (6.29).

$$R_{\mathrm{vai}} = R_{\mathrm{vai}}^{0} \cdot \mathrm{SoC_i}^{-k\lambda_{\mathrm{i}}} \geq R_{\mathrm{va\_lim}} \tag{6.29}$$

Figure 6.9(f) shows the influences of SoC and k on R_{vai}. The difference in R_{vai} becomes larger with increase of k, resulting in larger power allocation difference and accelerating the SoC balance speed. However, the ESU releasing more power is with a smaller R_{vai}, degrading the system damping and deteriorating dynamic characteristic. Hence, dynamic stability constraint provides an upper limit for k.

Considering these three constraints, constraints estimation is performed, as shown in Figure 6.10(a). Lower limit of $|k|$ is not required. The power is equally distributed among ESUs when R_{vai}=R_{vai}^{0} and k=0. From Figure 6.9(f), dynamic stability is ensured because R_{vai}^{0} is within the acceptable range. Power and voltage deviation constraints would be obeyed also, when ESUs with R_{vai}=R_{vai}^{0} supply power within rated range. Hence, the above three constraints are upper and region limitations.

The flow of control parameter design and optimized selection range is shown in Figure 6.10(b). The specific process is as follows:

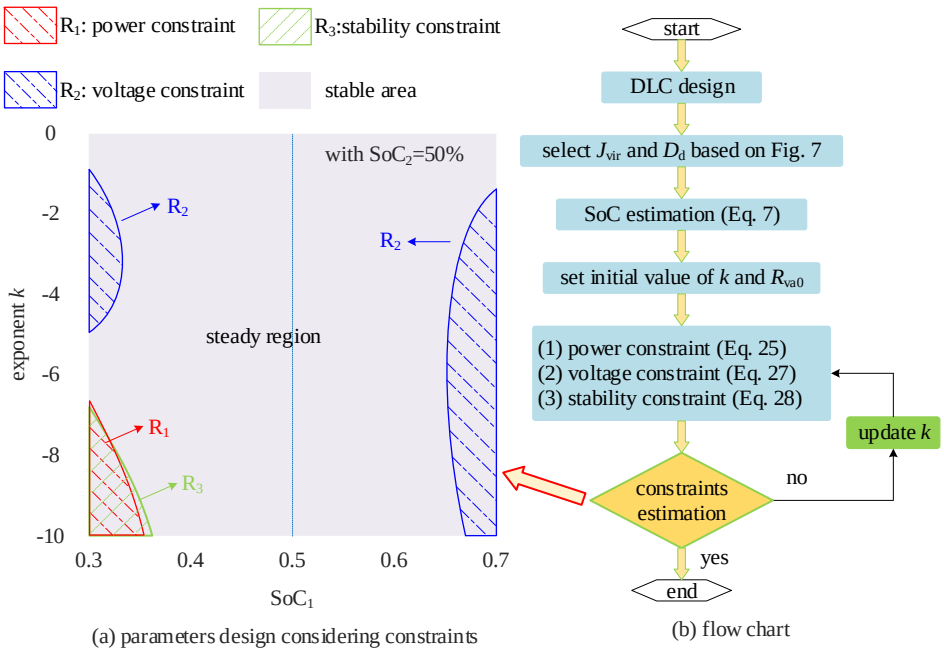


Figure 6.10: Constraint estimation and parameter optimization flow chart. (a) Parameters design considering coonstraints. (b) Flow chart.

1) DLC PI controllers are designed according to the requirements of phase margin and amplitude margin [54].

2) As shown in Figure 6.9, J_{vir} and D_{d} are selected based on the standards of dynamic performance (ξ and T_{iner}). Note that, the impact of oscillation mode should not be ignored.

3) Set R_{vai}^{0} from Eq. (6.26); choose the initial value of k according to the SoC balance speed.

4) Draw Figure 6.10(a) based on Eqs. (6.25), (6.28) and (6.29) for constraint estimation. If these constraints are met, it indicates that the selected k is reasonable, if not, an appropriate k should be chosen according to Figure 6.10(a).

6.4 Simulation and Experiment Verification

Simulation and dSPACE-based HIL experiment is conducted to validate the effectiveness of the proposed control strategy. The multi-parallel ESS similar to Figure 6.1 is tested and P_{net} is changes suddenly to imitate the power disturbance. The control and circuit parameters are in Tables 6.3 and 6.4.

6.4.1 Simulation results

In order to verify the inertia effect and voltage regulation ability of the proposed strategy, it is compared with the droop control and VDCM control [89, 143]. When t=3s and 6s, there are power disturbance of 2 kW. The results are shown in Figure 6.11 and 6.12. The voltage oscillates severely under droop control, indicating that DC-MG lacks of damping and inertia.

Table 6.4 Control parameters of different control

Control strategy	ITEMS	Value
Dual loop control	Droop coefficient R_a	2 Ω
	Voltage loop k_{vp}+ k_{vi}/s	1+10/s
	Current loop k_{ip}+ k_{ii}/s	5+1/s
VDCM control	Droop coefficient R_a	2 Ω
	Virtual armature resistance	1.2 Ω
	Voltage loop k_{vp}+ k_{vi}/s	0.1+50/s
	Virtual inertia J_{vir}	2 F
	Virtual damping D_{damp}	10
Inertia-emulation based cooperative control strategy	Virtual inertia J_{vir}	0.06
	Virtual damping D_d	4
	Speed regulation resistance R_{vai}^{0}	2 Ω
	Voltage loop k_{vp}+ k_{vi}/s	0.1+50/s
	SVR k_s	1
	Switch frequency	10 kHz
	ESU capacity	2.0 Ah
	Net power of Zone II P_{net}	2 kW

It can be seen from Figure 6.11(b) that the dynamic performance is improved significantly when IEL or VDCM works, and v_{out} can move to steady state without oscillation. Since the proposed IEL is in the system level control, it does not destroy bandwidth coordination, thus can eliminate voltage oscillation in the initial stage. The transient behavior is improved and the voltage tracking ability at the startup phase is enhanced, compared with droop control and previous VDCM control. The influences of J_{vir} and D_d are shown in Figure 6.11(c) and (d), respectively. When

J_{vir} or D_d selects a small value, v_{out} would achieve stability after a short period of oscillation. The oscillation will be better suppressed and a good transient behavior would be acquired when larger J_{vir} or D_d is chosen. The damping of oscillation mode would decrease with the increasing of J_{vir} or D_d, which is consistent with Figure 6.8. Therefore, ξ and T_{iner} should be considered together when selecting J_{vir} and D_d.

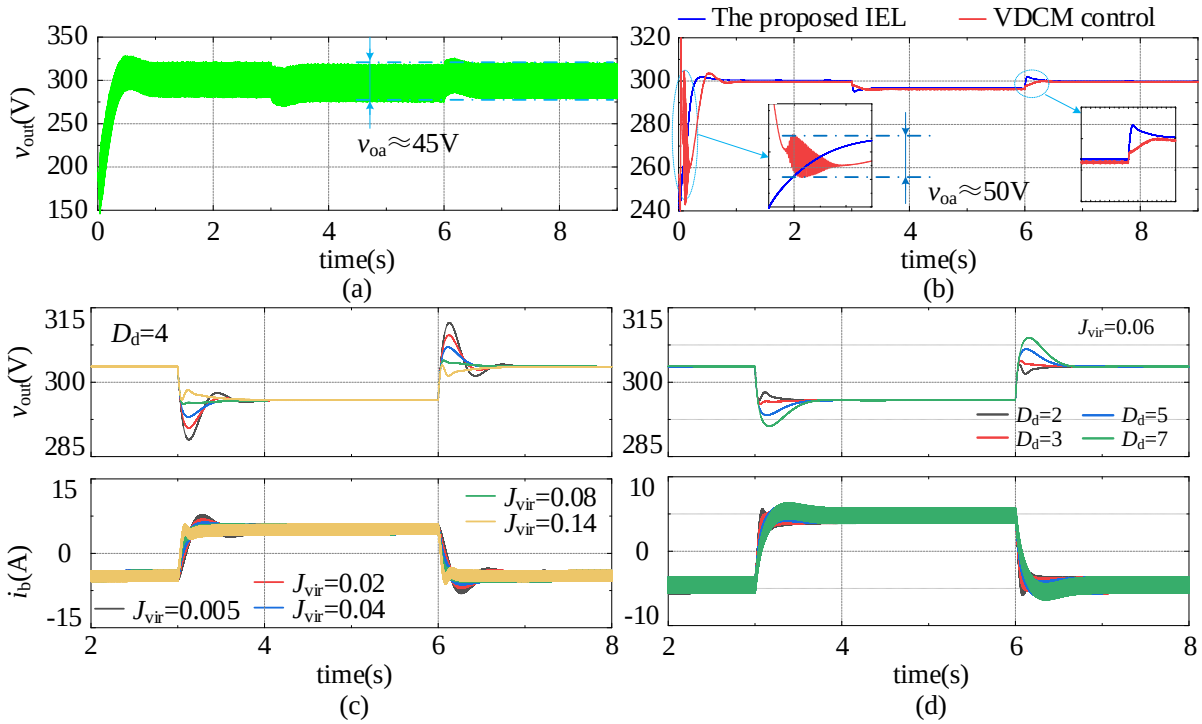


Figure 6.11: Comparison of different control strategies. (a) The v_{out} of droop control. (b) The comparison between the proposed IEL and VIDC. (c) The impact of J_{vir}. (d) The impact of D_d.

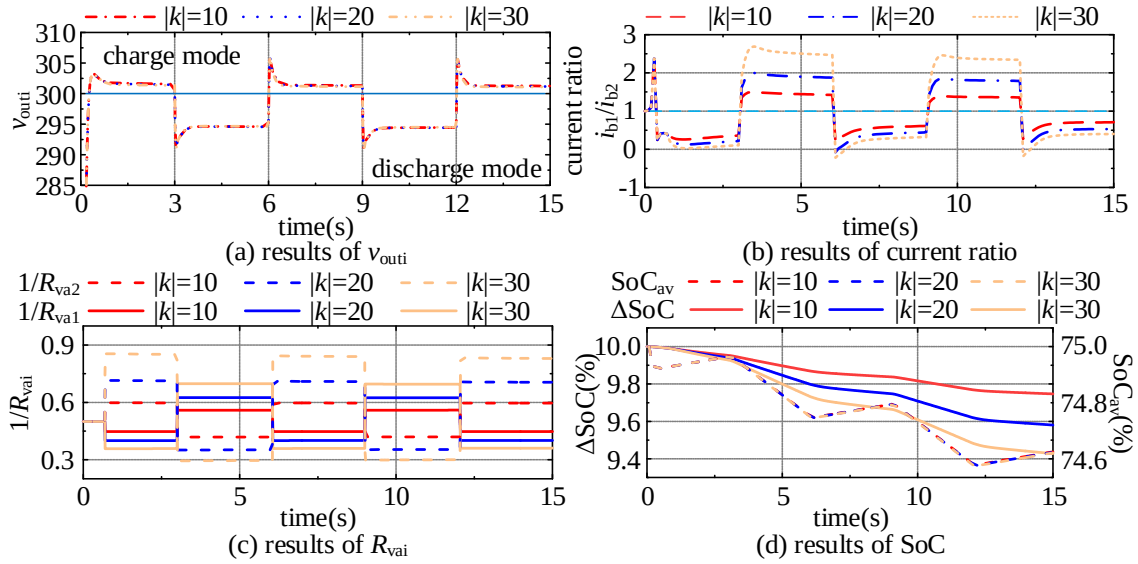


Figure 6.12: The influence of k on SoC balance speed. (a) The result of v_{outi}. (b) The result of current ratio. (c) The result of R_{vai}. (d) The result of SoC.

P_{net} is disturbed by 2kW every 3s and the operation mode of ESS are thus changed. When $t \in$ [0, 0.5s] (the start-up stage), the SoC balance algorithm does not work. After t=0.5s, the SoC self-balance algorithm is activated. The simulation results are in Figure 6.12. From Figure 6.12(b) and (c), R_{va1} of ESU_1 with a larger SoC is smaller in discharge mode, and thus the output current is larger. In the charge mode, R_{va1} is larger and the injected current is smaller. As a result, ΔSoC_{12} is decreased to 0. It can be concluded from Figure 6.12(d) that, after a same time period, the final ΔSoC_{12} with a higher $|k|$ becomes smaller, indicating the SoC equalization rate is enhanced. Meanwhile, although different k would change the SoC balance speed, it would hardly bring a difference in SoC_{av}, indicating that changing k will not affect the overall efficiency of ESS.

6.4.2 Hardware in the loop experiment results

The dSPACE-based HIL platform is built, as shown in Figure 4.14, to verify the performance of the proposed inertia-emulation based cooperative control strategy. The DC-MG is built in the power electronics simulation software MATLAB and simulated by compact prototyping unit MicroLabBox with a time step of 100 μs. The discrete control algorithm is implemented in the NXP QorlQ P5020 processor to generate the gate signals of all IGBTs and the sampling frequency is 10 kHz. The analog signals and digital signals (state variables and PWM signal) are transferred through I/O interfaces and cables.

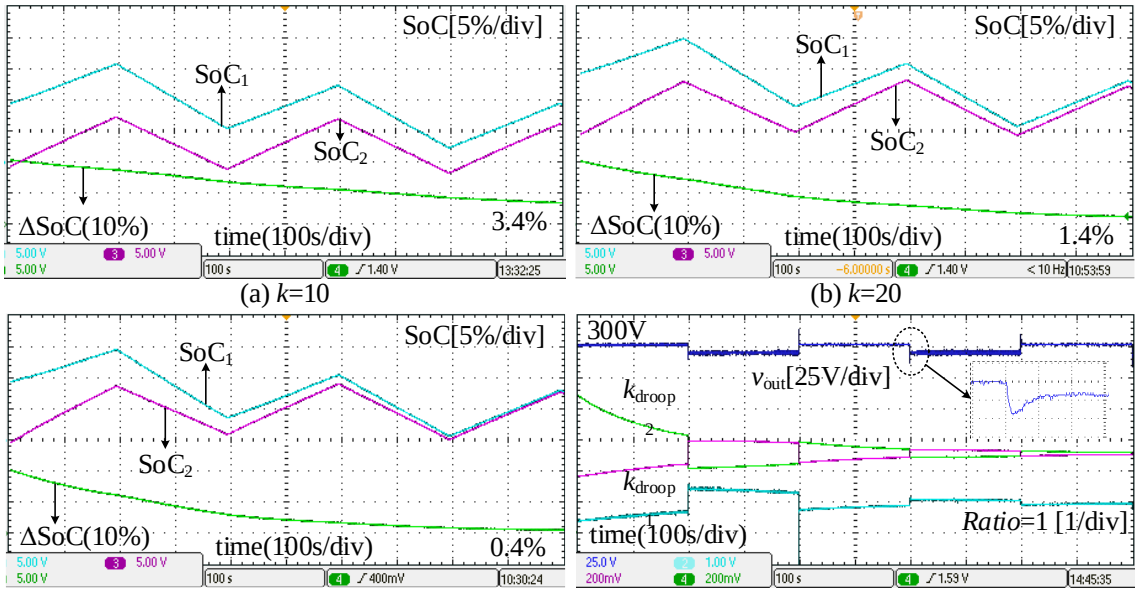
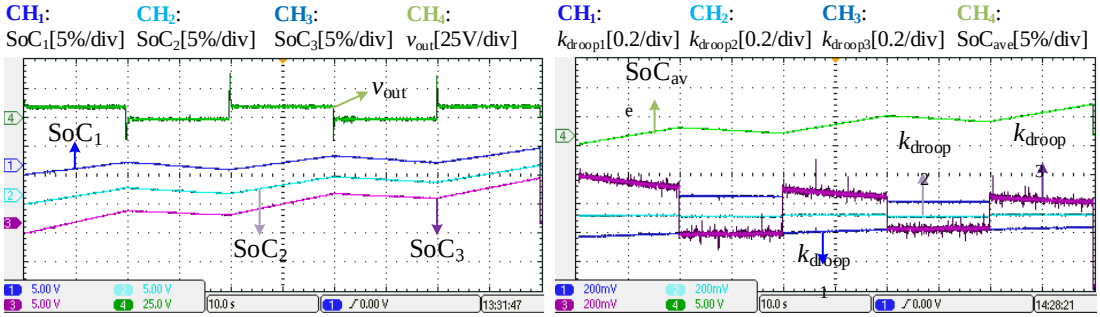


Figure 6.13: The effect of k on the SoC balance when $SoC_{1,\ t=0}$=80% and $SoC_{2,\ t=0}$=70%. (a) k=10. (b) k=20. (c) k=30. (d) State variable when k=30.

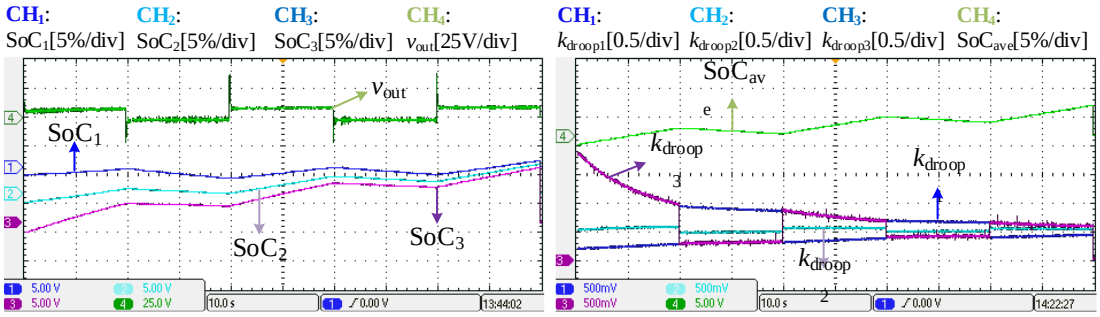
Case A: Performance of the SoC self-balance algorithm with different k and sudden power

fluctuation

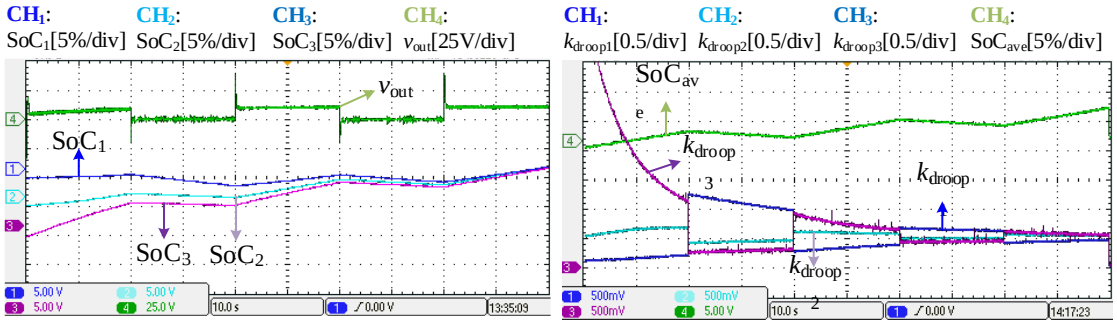
The experimental waveform with varying k is shown in Figure 6.13, when P_s=3kW and P_{const}=2kW. P_{net}(=P_{const}-P_s) is disturbed by 2kW every 200s and the operation mode of ESS are thus changed. The initial SoCs of these ESUs are 80% and 70%. In discharge mode, v_{out} of ESU is lower than v_{dcn}, and v_{out} is higher than v_{dcn} in charge mode, as shown in Figure 6.13(a-c). k_{droop1} of ESU_1 with a larger SoC is larger than k_{droop2} in discharge mode, and thus the output current is larger. In the charge mode, k_{droop1} of ESU_1 is smaller than k_{droop2} and the injected current is smaller. As a result, ΔSoC_{12} converges to 0. From Figure 6.13, the final ΔSoC_{12} with a higher $|k|$ becomes smaller after a same time period. $\Delta SoC_{12,\ t=1000}$ is 3.4%, 1.4% and 0.4% when $|k|$ is 10, 20 and 30. The SoC equalization rate is enhanced by a higher $|k|$.



(a) $|k|$=10, without SVR



(b) $|k|$=30, without SVR



(c) $|k|$=50, without SVR

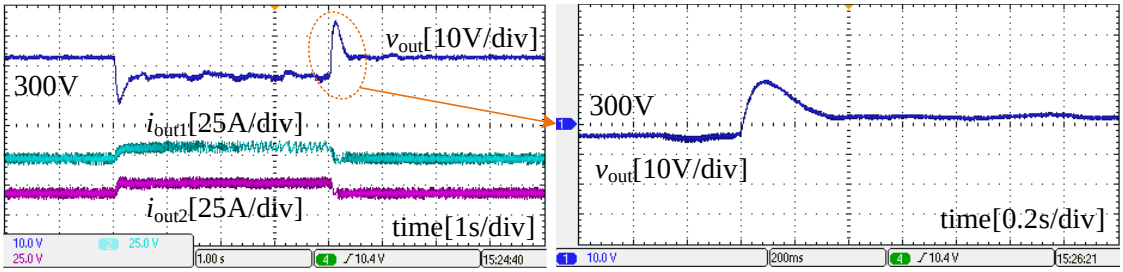
Figure 6.14: The effect of k on the SoC balance when $SoC_{1,\ t=0}$=80% and $SoC_{2,\ t=0}$=70%. (a) k=10. (b) k=20. (c) k=30. (d) State variable when k=30.

Moreover, the experimental waveform of three ESUs in parallel is shown in Figure 6.14. P_{net}(=P_{const}-P_s) is disturbed by 2kW every 20s and the operation mode of ESS are thus changed. The initial SoCs of these ESUs are 55%, 50% and 45%. Similar to the result in Figure 6.13 (two ESUs in parallel), the ESUs regulated by the proposed SoC self-balance algorithm also operate in the manner that the ESU with higher SoC should release more power in discharge mode and absorb less power in charge mode than the one with lower SoC. The SoC unbalance can be removed much faster when choosing a larger |k|.

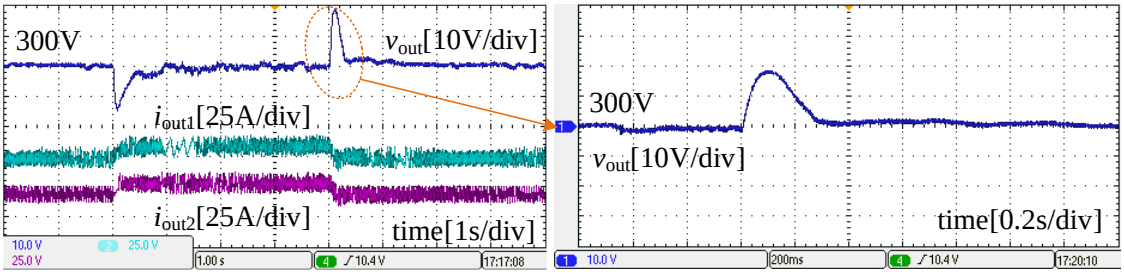
Case B: Performance of SVR loop

Case B verifies the impact of SVR loop, as shown in Figure 6.15. P_s is constant at 3kW. The initial value of P_{const} is 2kW, which increases or decreases by 2kW every 4s.

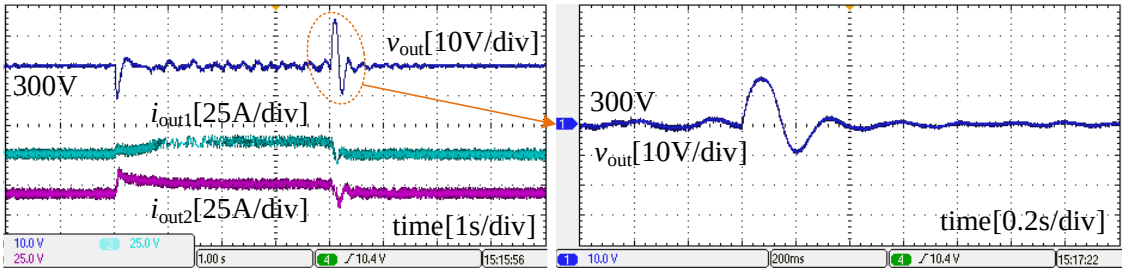
Comparing Figure 6.15(a) and (b), SVR can eliminate steady-state error and ensure better voltage quality. In the transient process, SVR increases the oscillation amplitude, and as k_s increases, the oscillation becomes more severe because of the interaction between SVR and IEL which form a 2nd-order oscillation loop. Thus, k_s should not be too large. In this chapter, k_s=1.



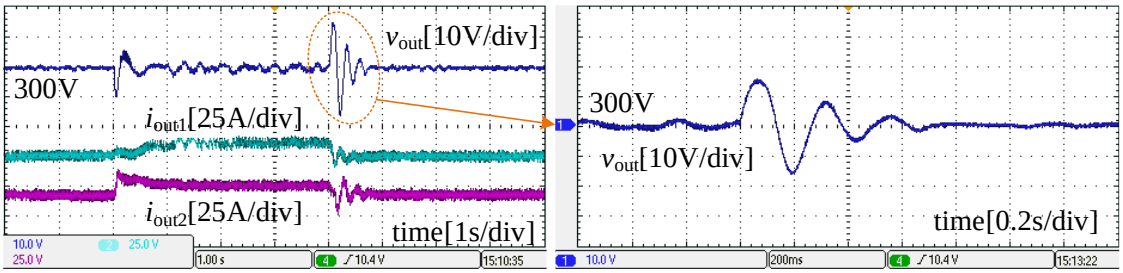
(a) without SVR, k_{damp}=8 and J_{vir}=0.06



(b) k_s=1, and with SVR, k_{damp}=8, J_{vir}=0.06



(c) k_s=5 and with SVR, k_{damp}=8, J_{vir}=0.06



(d) k_s=10 and with SVR, k_{damp}=8, J_{vir}=0.06

Figure 6.15: The influence of SVR loop. (a) Without SVR, k_{damp}=8 and J_{vir}=0.06. (b) k_s=1 with SVR, k_{damp}=8 and J_{vir}=0.06. (c) k_s=5 with SVR, k_{damp}=8 and J_{vir}=0.06. (d) k_s=10 with SVR, k_{damp}=8 and J_{vir}=0.06.

6.5 Summary

An inertia-emulation based cooperative control strategy is proposed to address the SoC imbalance and voltage deviation problem during steady-state operation, and the voltage stability problem caused by inertia-less during the transient process in multi-parallel ESS of islanded DC-MG, which includes a SoC self-balance algorithm, IEL, and a virtual-inductor-based SVR loop.

Specifically, the SoC mismatch degree is defined and the power distribution is regulated by integrating this SoC mismatch degree into virtual droop resistance to achieve dynamic SoC balance. Thus the contradiction between SoC balancing speed and maintaining system stability is addressed by this redefined SoC-based droop resistance function. The SoC convergence speed depends on the introduced adjustment factor k. Besides, IEL and SVR loop are developed based on DC motor model and circuit equivalence of inductors respectively, to improve the dynamic stability and eliminate the steady-state voltage error. The dynamic performance analysis demonstrates that a larger exponent $|k|$ accelerates SoC balance speed. Moreover, the SoC self-balance algorithm is a 2^{nd}-order system and the IEL can be simplified to a 3^{rd}-order system. Thus, appropriate J_{vir} and D_d could be selected based on the requirements of ξ and T_{iner}. The steady region of k is discussed considering the boundaries of various constraints estimation, and the parameter optimal design process is presented. Finally, simulations and dSPACE-based HIL experiments are conducted. It is demonstrated that fast SoC balance, inertia effect, and stiffness can be simultaneously guaranteed in multi-parallel ESS with the proposed method.

7 Conclusions and Future Works

7.1 Conclusions

The promotion of DC microgrid (DC-MG) is one of the most effective ways to improve the penetration of renewable energy sources (RES) and thus would be an indispensable element of the future power system. The characteristics of volatility, intermittency, and randomness will pose challenges to the stability of the DC bus voltage and threaten the stable operation of the islanded DC-MG. A reasonable configuration and control of the energy storage system (ESS) can effectively suppress the fluctuation and oscillation of the DC bus voltage.

This dissertation focuses on the stabilization control and stability mechanism analysis of islanded DC-MG, as well as the state of charge (SoC) unbalance problem of multi-parallel ESS is considered. By making full use of the dynamic voltage support ability of ESS, it aims to improve the voltage stability of islanded DC-MG and the power quality of users by providing sufficient inertia and damping, and the research on low-frequency oscillation (LFO) mechanisms provides theoretical guidances for dynamic stability enhancement methods.

The significant conclusions include the following aspects:

(i) A virtual inertia and damping control (VIDC) for bidirectional DC (bi-DC) converters is proposed and its essence is connecting a virtual capacitor and a controlled current source in parallel, and a virtual resistance in series on the output side of bi-DC converters, which makes the external characteristics of bi-DC converters consistent with the dynamic characteristics of DC machines. Simulation results show that the proposed strategy provides satisfactory inertia and damping effects in islanded DC-MG.

- Based on a simple DC machine model, a VIDC strategy is proposed. It is a systematic combination of active damping control, virtual resistance control and virtual inertia control.
- The analogy between DC machine and bi-DC converter control is addressed and the VIDC concept model is proposed. The control parameters have a clear physical meaning.
- The rated voltage is added into the inertia loop, thus the proposed VIDC strategy only acts in the transient process with a better control performance, the static characteristics (i.e. voltage regulation and power sharing) would not be affected.

- The inertia matching method of multi-parallel bi-DC converters is analyzed to realize dynamic process consistency. Parameter design methods are given and a second-order model is proposed to simplify the parameter design.

(ii) Inertia droop control (IDC) strategies are proposed based on the equivalent models of VIDC to mitigate LFO, suppress the rate of change of voltage (RoCoV) and remove the voltage deviation in islanded DC-MG. The dSPACE-based hardware in the loop (HIL) experiment validates the theoretical analysis and the proposed methods. The major studies and contributions are summarized as follows:

- Equivalent droop-control-form models of VIDC are derived, and it is found that VIDC can be regarded as an improved droop control with a damping term. Thus, the virtual inertia can be realized by a dynamic virtual impedance or an adaptive droop resistance, while the damping results from a first-order lag unit.
- Based on the established voltage-source and current-source models of VIDC, voltage-mode and current-mode IDC strategies are proposed. Compared with conventional VIDC for islanded DC-MG, the inertia and damping can be improved by easily modifying the droop control without adding any auxiliary controllers or observers, simplifying the complex control structure.
- A feedback analytical method is proposed to illustrate the stability mechanism and a phasor diagram is developed as its analysis tool where the interaction among feedback variables can be intuitively observed. Thus the positive damping of IDC is revealed, and the physical significance and control function of parameters are explained explicitly from multi-views.
- Dynamic performance and small-signal stability analysis are conducted to determine appropriate parameters of optimal effect and to ensure better dynamic responses.

(iii) The mechanism analysis and mitigation method of low-frequency oscillations in islanded DC-MG are developed by the established multi-timesacle impedance modeling framework. Specifically, control loops of different timescales are visualized as independent loop virtual impedances (LVIs) and their interaction is interpreted by the interconnection of LVIs, explaining the LFO mechanism. On this basis, dynamic stability enhancement methods are proposed to cancel the non-passive impedances and improve the high-frequency inertia. Simulation and experiment validated the proposed impedance modeling and stability enhancement methods.

- The stability mechanism of VIDC and low-frequency oscillations of VIDC-DC-MG at different timescales are revealed by fully analysing LVIs. The multi-timescale impedance model illustrates the impedance-shaping effects and impedance properties of the different-

timescale control loops/parameters in a generic and intuitive way.

- *RLC* representations of LVIs are derived and their passive circuit elements are expressed by control parameters. Thus the low-frequency oscillations within the voltage- and inertia-loop bandwidths are analyzed by *LC* impedance interaction. Further, the physical interpretation of control process is elaborated by analyzing the behavior of passive circuit elements mapped from control parameters.
- By discovering the non-passive regions of LVIs and investigating their influences on the other LVIs, the positive-feedback loops with negative damping are identified and defined as the instability factors, which deteriorate low-frequency oscillations and reflect the coupling between different timescales.
- Dynamic stability enhancement methods are proposed, including positive-damping reshaping loops to compensate for the negative damping caused by VIDC and constant power load, and a supercapacitor unit enhancing the high-frequency inertia of VIDC-DC-MG.
- The corresponding passivity analysis is conducted on the multi-timescale impedance model to evaluate the voltage stability.

(iv) An inertia-emulation based cooperative control strategy is proposed to solve both the SoC imbalance and voltage deviation problems during steady-state operation, and the voltage stability problem caused by inertia-less in the transient process. Besides, the contradiction between SoC balancing speed and maintaining system stability is addressed. System stability and parameter influences on dynamics are investigated through time-domain modellng and analysis. Simulation and HIL experiment verify the performance of the proposed control method.

- A cooperative control strategy is proposed to balance the SoC of the multi-parallel ESS of islanded DC-MG. The defined SoC mismatch degree and balance speed adjustment factor *k* are integrated into the redefined droop resistance by SoC self-balance algorithm to dynamically balance the SoC and adjust balance rate.
- The contradiction between the SoC balancing speed and maintaining system stability is addressed by the reconstructed SoC-based droop resistance function.
- The optimal design method of *k* is given considering variable constraints and a dynamic stability constraint to ensure that the SoC self-balance algorithm will not affect stability.
- An inertia emuation loop (IEL) is proposed to enable multi-parallel ESS to provide virtual inertia and improve voltage stability. Different from previous inertia control, this IEL is designed based on the detailed DC motor model, giving all the control parameters a clearer physical meaning. And the rated value of the output voltage is added into the IEL, thus the

proposed IEL only acts in the transient process with a better control performance and would not affect the static characteristics (i.e., voltage regulation and power distribution).

- Based on the circuit equivalence of inductances, a secondary voltage recovery loop is constructed to achieve zero steady-state voltage deviation by short-circuiting the droop resistor and to improve the system stiffness.

In summary, this dissertation takes the ESS of islanded DC-MG as the research subject. Focusing on the improvement of system stability, a related virtual inertia control method is proposed and the LFO mechanism of DC voltage is illustrated, and the SoC imbalance problem is solved. This study lays a theoretical and technical foundation for the future large-scale penetration of RES and the application of ESS in islanded DC-MG.

7.2 Future Works

Although VIDC has been proposed to enhance the voltage stability of islanded DC-MG and the low-frequency oscillation mechanism of DC bus voltage has been studied, the dynamic interaction of multi-converters still lacks in-depth investigation and needs to be further explored in future work. Based on this dissertation, there are many aspects worthy of expansion and many works deserve further investigation in follow-up research:

(i) At present, all control parameters are set at a special operation point (generally selected as the rated operation point). When the operation point changes, it is difficult to guarantee sufficient stability margin and better dynamic response of the system. Therefore, future work will concentrate on the adaptability of the designed parameters in a wide range of working conditions, and parameter optimization design methods will be studied.

(ii) The present control methods do not consider the influence of RES and load uncertainties on control performance. Therefore, some advanced nonlinear control methods are also worth studying, such as adaptive sliding mode observer based model predictive control (MPC). MPC is a closed-loop optimization control method with rolling optimization and feedback correction as the core idea, which undermines the influence of RES and load uncertainties to some extent.

(iii) The methods of suppressing circulating current caused by line resistance will also be focused on. Circulating current can lead to uneven power distribution among energy storage units (ESUs), reduce system efficiency, cause SoC divergence among ESUs, and shorten their lifespan. Besides, the system stability would be affected due to the change in the operation point.

(iv) It should be stressed that the proposed LFO analysis and impedance modeling approach are

only restricted to DC-MG with only one ESS. In the future, this impedance modeling framework and LFO analysis would be extended to DC-MG with multi-parallel ESS. Correspondingly, the dynamic interaction and dynamic characteristics of current sharing between multiple converters would be thoroughly investigated.

(v) The research of DC converter topologies should also be paid enough attention to improve their adaptability in medium and high voltage applications. Some key technical issues, such as dynamic voltage equalization and high losses of all series power electronic switches, the zero-current transfer (soft switching) of power electronic switches, and the hazards of extremely high dv/dt and di/dt, will be involved in future research.

Combining the previous research foundations, we will continue to focus on DC-MG stability issues and oscillation damping techniques.

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Gang Lin, born on January 1994 in Shandong, China, had been working as a research associate at the Institute for Energy Sytems, Energy Efficiency and Energy Economics (ie³), at the TU Dortmund University.

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2016.09 – 2019.06 **Hunan University, Changsha, China** **Master**

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Publications

2022:

[M1] **Gang Lin**, J. Liu, P. Wang, C. Rehtanz, Y. Li and S. Wang, "Low-Frequency Oscillation Analysis of Virtual-Inertia-Controlled DC Microgrids Based on Multi-timescale Impedance Model," *IEEE Trans. Sustainable Energy*, doi: 10.1109/TSTE.2022.3157473.

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[M11] Jiayan Liu, Yang Zhou, Yong Li, **Gang Lin**, Wenjing Zu, Yijia Cao, Xuebo Qiao, Chongbo Sun, Yi Cao and Christian Rehtanz, "Modelling and analysis of radial distribution network with high penetration of renewable energy considering the time series characteristics," *IET Generation, Transmission & Distribution*, vol. 14, no.14, pp. 2800-2809 Jul. 2020.

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