2023 IEEE Nanotechnology Materials and Devices Conference (NMDC) | 979-8-3503-3546-0/23/$31.00 ©2023 IEEE | DOI: 10.1109/NMDC57951.2023.10344109

Self-Aligned Formation and Positioning of Nanogap Templates

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***Abstract*— This paper presents a versatile and scalable method for generating sub 20 nm nanogaps based on standard I-line lithography. The nanogaps are self-aligned to lithographically patterned features and make use of a combination of corner lithography, edge retraction, and sidewall oxidization. We demonstrate the flexibility of this approach by extending it to include coaxial holes in the center of the circular nanogaps, and by filling of the nanogaps with platinum silicide to create nanowires.**

I. Introduction

Continual miniaturization is an ever-present aspect of modern nanofabrication, however current approaches of downsizing the lithography wavelength to pattern nanoscale features have resulted in fabrication costs which are prohibitively expensive for many users. Electron beam lithography is typically used when nanoscale features are required on low volume devices, however the serial nature of the process results in both long writing times, and no clear path forward for high throughout production. There is therefore a need to develop alternative fabrication processes for achieving nanoscale features without using extreme ultraviolet or electron beam lithography.

Here we present a method for generating nanoscale features using a combination of edge retraction [1], sidewall oxidation [2], and corner lithography [3] to produce nanogaps at the perimeter of structures defined with standard I-line lithography. This approach is extended to create a perforated membrane where the holes are coaxially centered with the nanogap. Further use of self-aligned machining is demonstrated by filling the nanogap with amorphous silicon and then forming a platinum silicide nanowire inside the gap. Varying the corner lithography and self-aligned processing parameters can enable further customizability of the 3D nanoscale templates. These fabrication methods have possible applications for flow through membranes with incorporated nanofeatures for electrical sensing, filtration, and catalysis.

II. Design and Fabrication

This section is divided into three parts, the first focuses on fabrication of a nanogap following a circular path, the second on a nanogap coaxially aligned around a hole through a silicon membrane, and the third on the platinum silicide nanowire fabrication inside of a nanogap.

A. Self-aligned nanogap fabrication

Figure 1 shows the fabrication flow for producing the self-aligned nanogap structures. The fabrication begins with a monocrystalline 100 oriented silicon wafer followed by 14 nm of silicon nitride deposited by low pressure chemical vapor deposition (LPCVD), then 30 nm of silicon oxide layer grown by decomposition of tetraethyl orthosilicate (TEOS), 30 nm of amorphous silicon by LPCVD, and a layer of native silicon oxide. Olin 907-17 photoresist is then spun onto the wafer, resulting the material stack seen in figure 1A.

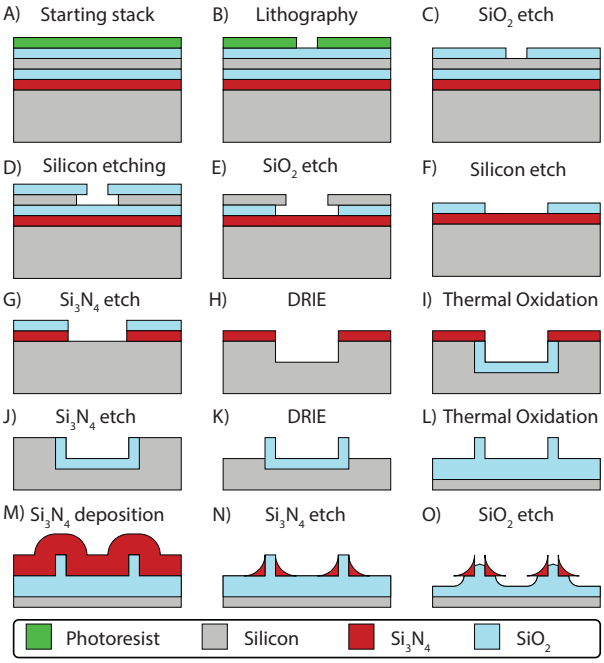

Figure 1: Diagram showing cross-sections of fabrication steps for producing nanogaps.

The final shape of the nanogap will follow the perimeter of the patterned photoresist. While this paper focuses on circles, in principle it is compatible with other geometries. In figure 1B, circles with diameters of 5 µm are patterned into the resist by use of I-Line lithography. The pattern is then transferred into the native oxide by etching in 1% hydrofluoric (HF) acid for 20 seconds, followed by stripping of the photoresist in acetone, figure 1C. The amorphous silicon layer is then etched for 20 seconds using 25% Tetramethylammonium Hydroxide (TMAH) solution at 70°C in figure 1D.

Research supported by Dutch Research Council (NWO) via the NewTDec (NWA.1160.18.200) consortium. All authors are from the Mesoscale Chemical Systems Group, University of Twente, Netherlands.

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Amorphous silicon is used as a hard mask during the buffered hydrofluoric (BHF) acid etching of silicon oxide in figure 1E. Etching is performed for 180 seconds, resulting in an approximate 350 nm retraction. The diameter of the ring will be determined by the photomask used in step 1B and the degree to which the layer stacks are retracted in steps 1D and 1E. The amorphous silicon layer is no longer needed, and so is stripped in figure 1F using TMAH. The mask is then transferred into the silicon nitride by use of 85% phosphoric acid at 140°C for 19 minutes, as shown in figure 1G. Due to their high etching selectivity, silicon oxide and silicon nitride act as a hard mask in the Deep Reactive Ion Etching (DRIE) step. The pattern is transferred into underlying silicon substrate and etched to a depth of approximately 100 nm. The DRIE processing is performed in an Oxford Estrelas system using a cycled pseudo-Bosch process (ICP: 800W, CCP: 41W, SF_6: 23 sccm, C_4F_8: 48 sccm, 18 mTorr, 0°C).

The nanogap width is defined by the silicon oxide thickness formed by thermal oxidation, as seen in figure 1I. Oxidation temperature and duration can be tuned to vary the width of the gap. In this paper we focus on thin oxidations in the range of 10 to 20 nm, achieved by dry oxidation at 900°C. Due to the protective silicon nitride cap, only the side walls of the silicon structure will be oxidized. After oxidation the silicon nitride layer can be removed by wet etching in phosphoric acid as seen in figure 1J. The freshly exposed silicon layer can then be etched in a second DRIE process (ICP: 400W, SF_6: 3 sccm, 18 mTorr, 0°C) with the etch depth being tuned to match that of the first etch, figure 1K. If the etch depth is not matched closely, then there is an asymmetry in the cladding height on either side of the gap. A second thermal oxidation is performed in figure 1L, this time at 1150°C for 1 minute, resulting in an oxide depth of approximately 550 nm.

With the nanogap dimensions defined in silicon oxide, a layer of silicon nitride can be conformally deposited by LPCVD, as seen in figure 1M. The purpose of the silicon nitride is for use in corner lithography, wherein conformal deposition followed by isotopic etching to leave only material in concave corners. During conformal depositions, concave corners will have a layer thickness greater than that of a flat area. In the case of 90-degree corners the thickness will be $\sqrt{2}$ times the deposition thickness on a flat area. Therefore, after isotropically removing the material until there is none remaining on flat areas, only material in concave corners will remain, as seen in figure 1N. Corner lithography is described in greater detail in [3]. In this case after the 74 nm deposition, a retraction of 77 nm was performed, resulting in a protective silicon nitride cladding on the silicon oxide sidewalls, where the height of these structures is slightly less than the original deposition thickness, and the shape follows a circular isotropic etching profile. Finally, the silicon oxide walls are etched back by 25 nm using HF, creating the nanogap as seen in figure 1O.

B. Self-aligned nanogap with coaxial hole fabrication

Figure 2 shows the fabrication flow for producing the self-aligned nanogap structures with coaxial holes. The fabrication begins with the same material stack as in the nanogap fabrication except using a silicon-on-insulator (SOI) wafer as the underlying substrate. The stack is 14 nm of silicon nitride deposited by LPCVD on a SOI wafer (monocrystalline 100 oriented device layer), followed by 30 nm of silicon oxide grown by decomposition of TEOS, 30 nm of amorphous silicon deposited by LPCVD, and a layer of native silicon oxide, followed by Olin 907-17 photoresist, resulting the material stack seen in figure 2A.

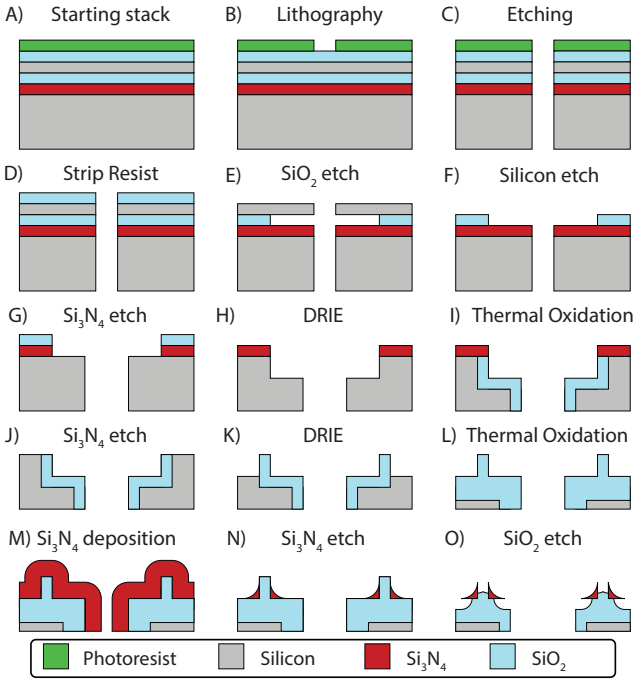

Figure 2: Diagram showing cross-sections of fabrication steps for producing nanogaps with self-aligned hole.

A photomask containing circles with 5 µm diameters are patterned with lithography into the photoresist in step 2B. After lithography and development, DRIE (Passivation using ICP: 1300W, SF_6: 10 sccm, C4F8: 200 sccm, 25 mTorr, 25°C, and etching using ICP: 1600W, CCP: 22W SF_6: 200 sccm, C4F8: 10 sccm, 40 mTorr, 25°C) is used to transfer the pattern into the native oxide, amorphous silicon, TEOS, silicon nitride, and finally into the silicon device layer, as seen in step 2C. The etching continues until reaching the buried oxide layer of the SOI, as illustrated in figure 3A. Any remaining resist can then be stripped in step 2D. The central hole will act as the starting point for defining the self-aligned nanogap. The TEOS layer is retracted approximately 350 nm using hydrofluoric acid, figure 2E, with the retraction distance determining the distance between the nanogap and the hole. It is necessary to have a chemically selective layer above the TEOS, as it prevents etching from the top, constraining the etch to only lateral retraction, this is described in [1].

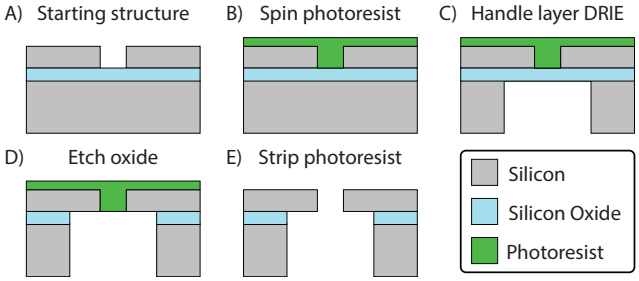

Figure 3: Cross-sectional diagrams for connecting a nanogap with coaxial hole in the device layer of a SOI wafer through the handle layer.

After retraction, the amorphous silicon layer is no longer needed and is etched using TMAH in figure 2F. Phosphoric acid is then used to transfer the pattern from the silicon oxide hard mask into the silicon nitride, figure 2G. A second DRIE etch (ICP: 800W, CCP: 41W, SF_6: 23 sccm, C_4F_8: 48 sccm, 18 mTorr, 0°C) to the desired height of the sidewall is then performed, in this case approximately 100 nm, figure 2H. Thermal oxidation is then performed to desired nanogap width, in this case approximately 19 nm, figure 2I. Oxidation temperature and duration can be tuned to vary the width of the gap and is described in more detail in [2]. The silicon nitride layer which was used to constrain the oxidation is then stripped in phosphoric acid during step 2J, and a third DRIE etch (ICP: 400W, SF_6: 3 sccm, 18 mTorr, 0°C) is then performed to lower the silicon device layer to the base of the oxide sidewall, as seen in figure 2K. The wafer is then thermally oxidized again, figure 2L.

As was done in the nanogap fabrication, a layer of silicon nitride is deposited by LPCVD in figure 2M, which is then used for corner lithography in figure 2N. A hydrofluoric acid etch retracts the silicon oxide sidewalls in step 2O, creating the nanogap coaxially around the hole. Finally, the holes in the device layer of the SOI can be opened from the handle layer. This begins by protecting the device layer with photoresist, as seen in figure 3B, and etching holes into the handle layer up to the buried oxide layer by DRIE, as seen in figure 3C. This results a thin membrane consisting only of the silicon device layer and the buried oxide layer. Hydrofluoric acid can then be used to open the buried oxide layer, as seen in figure 3D, connecting the device layer and handle layer holes. The photoresist is then stripped, resulting in the final structure in figure 3E.

C. Nanogap with platinum silicide nanowire fabrication

Filling of the nanogap can be accomplished by using the same principal of corner lithography used to create the nanogap. Starting with the final nanogap structure in figure 4A, 12 nm of amorphous silicon is then deposited by LPCVD in figure 4B. The silicon is then retracted by 18 nm in figure 4C using an RCA 1 solution (NH_4OH:H_2O_2:H_2O at 1:1:5 vol%). Due to the conformal deposition and isotropic etching, the resulting structures are amorphous silicon nanowires inside the nanogap. Once an amorphous silicon nanowire is formed, a 20 second etch in 1% HF is performed to remove the native oxide, and 5 nm of platinum is sputtered onto the substrate in figure 4D. In this case, platinum is deposited, however a wide range of metals could be used to form metal silicide nanowires. The substrate is then annealed in figure 4E using a rapid thermal annealing system (RTA Solaris) at 520°C for 120 seconds under nitrogen flow of 8 L/min. The remaining excess platinum is stripped using aqua regia (H_2O:HCl:HNO_3 at 8:7:1 vol%) at 80°C for 120 seconds, leaving behind only the platinum silicide nanowire inside the original nanogap, as seen in figure 4F.

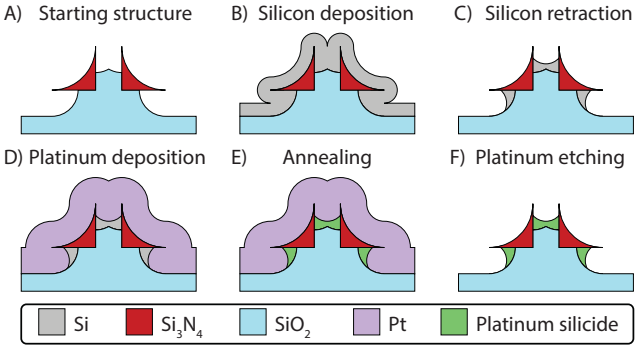

Figure 4: Diagram showing cross-sections of fabrication steps for producing *platinum silicide nanowires inside of nanogaps.*

III. Results and Discussion

The three fabrication flows were imaged by Scanning Electron Microscopy (SEM), and additionally imaged by Scanning Transmission Electron Microscopy (STEM) in the case of the platinum silicide nanowires. Several key steps in the fabrication are shown in the figures in this section.

A. Self-aligned nanogap

Beginning with the first fabrication presented in figure 1, the patterned circles are etched into the substrate by DRIE in figure 5. While there are some nonuniformities in the quality of the sidewall created in this step, these appear to primary result from the lithography. While this could be optimized for in the future, it does not significantly affect the quality of the final fabricated structures.

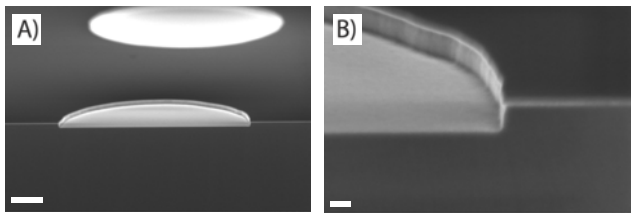

Figure 5: SEM image of a circular pattern etched with DRIE into the starting layer stack at A) Low magnification (1 µm scale bar) and B) High magnification (100 nm scale bar).

After oxidation and removal of the layers in the starting stack, the second DRIE step takes place as illustrated in figure 1K. The resulting silicon oxide sidewall can be seen as SEM images in figures 6A and 6B. While the structure is continuous and follows the shape patterned in previous steps, a small asymmetry in the etching can be seen in figure

6B where the substrate is etched slightly deeper on the inner side of the ring than on the outer side of the time. This is due to the challenges of tuning etch depth during DRIE processing, however, is small enough in this situation that it does not cause any complications in the subsequent steps.

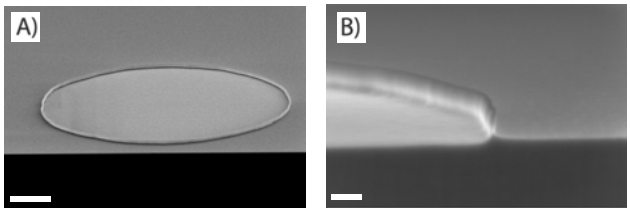

Figure 6: SEM image of the resulting silicon oxide side walls after the second DRIE step at A) Low magnification (1 µm scale bar) and B) High magnification (100 nm scale bar).

Another key step is the oxidation of the substrate after the oxide sidewall is produced. This is done in figure 1L and is required for providing symmetry between the inner and outer sides of the structure during the final HF etching step. There is an additional benefit in that it would provide a tunable electrically isolating layer between the nanostructures and the silicon substrate, which may be required for some applications. The thermal oxidation process was of concern because it was assumed that the oxide sidewall would be fragile, not only because of the sub 20 nm width, but also because of its approximate 5:1 aspect ratio. There are however publications indicating that thick oxidations can be performed without damage to nanostructures [4]. Therefore, a shallow oxidation of only 50 nm was first attempted at 900°C to determine if the structures would survive the processing. Figure 7A shows the resulting structure, which does not appear to show any signs of stress related fracturing or warping of the nanostructures. A deeper oxidation of 500 nm at 1150°C was then attempted on another sample, with the results shown in figure 7B. Once again there was no sign of negative consequences from the thermal oxidation, and so fabrication was continued with the deeper oxidation.

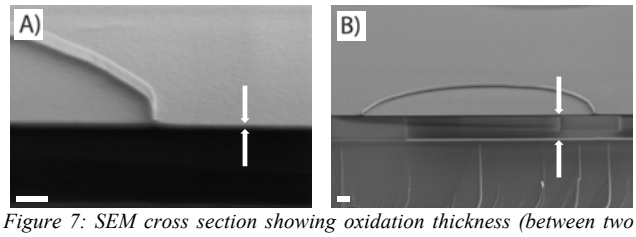

Figure 7: SEM cross section showing oxidation thickness (between two white arrows) after A) 50 nm oxidation at 900°C (200 nm scale bar). B) 500 nm oxidation at 1150°C (300 nm scale bar).

With the sacrificial sidewalls defined, the silicon nitride corner lithography process can begin. The before and after of the silicon nitride LPCVD is shown in figures 8A and 8B respectively. The conformal deposition of the LPCVD process can be clearly seen, and in conjunction with the isotropic etching profile of the next step is essential for the formation of the protective cladding.

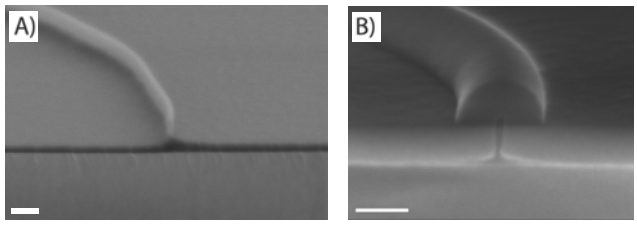

Figure 8: SEM cross section showing the silicon oxide sidewall A) before silicon nitride deposition (100 nm scale bar) and B) After silicon nitride deposition (100 nm scale bar).

A cross sectional image of the nanogap without the central hole can be seen in figures 9A and 9B. SEM data of these structures suggests a gap width of between 10 and 20 nm, which is consistent with the expected thickness of the sidewall oxidation step. While the nanogap can be clearly seen, less obvious is the undercut from the sides of the structure, which results from the same etching step which opened the nanogaps.

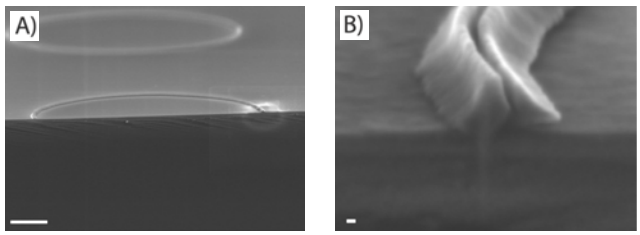

Figure 9: SEM cross section of nanogap without central hole A) Lower magnification (1 µm scale bar) B) Higher magnification (10 nm scale bar).

B. Self-aligned nanogap with coaxial hole

The central hole resulting from the first DRIE step is shown in figures 10A and 10B. The cross-sections are from a test wafer, and therefore does not have the silicon oxide stopping layer found it the SOI wafer used for final fabrication. The etching is performed in cycles, resulting in the repeated scalloping of the side walls. The high selectivity of the hard mask materials result in a high-quality mask transfer in the DRIE step.

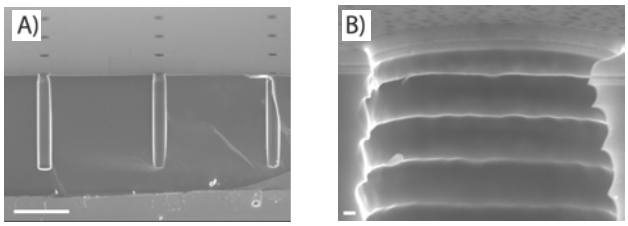

Figure 10*: SEM cross section of* the DRIE *hole A) Lower magnification* (10 µm scale bar) *B) Higher magnification* (100 nm scale bar)

In figure 11A it is possible to see the various layers of the stack at the equivalent of figure 2D. In figure 11B the TEOS layer has been retracted, setting the position of the nanogap as illustrated in figure 2E. While this retraction will also strip the native oxide on exposed any silicon, there is minimal effect on the fabricated structure.

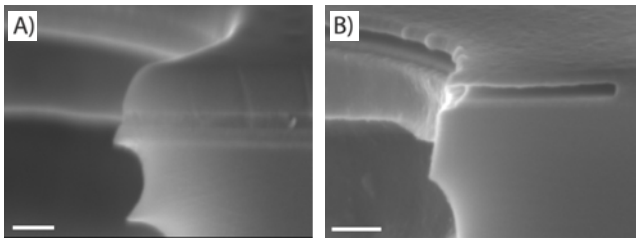

Figure 11: SEM cross section of the DRIE hole A) Before retraction etching (100 nm scale bar) and B) After silicon oxide retraction in BHF (100 nm scale bar).

The amorphous silicon layer, which can be seen in figure 11B suspended above the newly created gap, is no longer needed after the retraction. The amorphous silicon is stripped in 70°C, 25 weight percent TMAH, in 7 seconds, with the resulting structure shown in figure 12. From this point the fabrication closely resembles that of the nanogap without coaxial hole, as presented in figures 5 to 9.

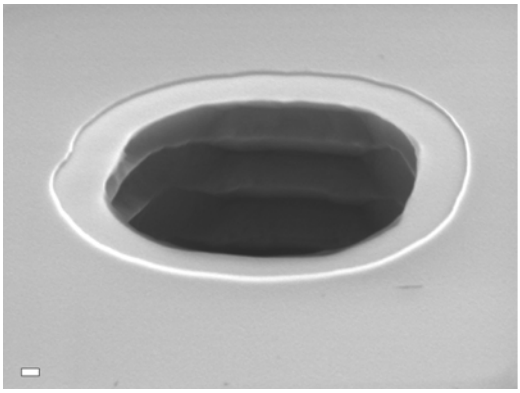

Figure 12: SEM image showing the DRIE hole after amorphous silicon stripping using TMAH (100 nm scale bar).

The final structures can be seen in figures 13A and 13B. The scallops resulting from DRIE can be seen on the sidewalls of the hole, and the hole continues through the device layer of the SOI. The backside etching of the handle layer is not shown, however the hole runs completely through the wafer. There is approximately 200 nm distance between the nanogap location and the edge of the hole, due to the retraction performed after the first DRIE step. In figures 13A and 13B, the nanogap has been filled with amorphous silicon, as was done in figure 3C for the platinum silicide nanowire fabrication.

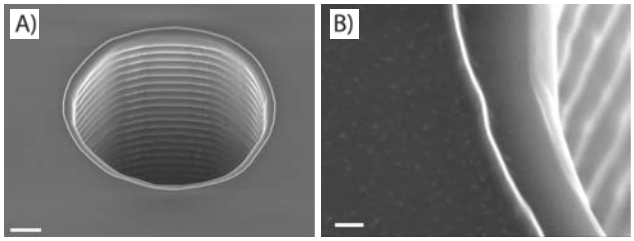

Figure 13: SEM images of a silicon filled nanogap with central hole A) Low magnification (1 μm scale bar)*. B) High magnification* (100 *n*m scale bar)

C. Nanogap with platinum silicide nanowire

The nanogap filled with platinum silicide is shown in figures 14 and 15. For imaging purposes, it was necessary to evaporate aluminium onto the sample as the focused ion beam (FIB) etching to prepare the lamella requires a conductive coating. The STEM images have close resemblance to the expected structures, with notable features including the clear undercut of the silicon oxide substrate, as well as the circular etching profile of the silicon nitride corner lithography.

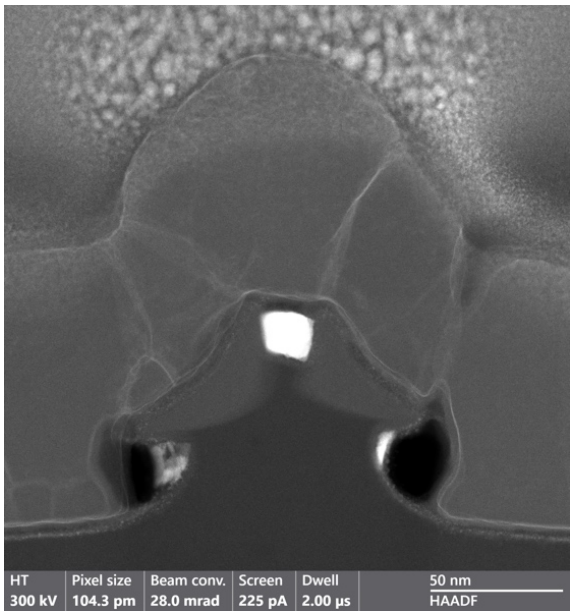

Figure 14: STEM cross sections of the platinum silicide filled nanogap using high-angle annular dark-field imaging (50 nm scale bar)

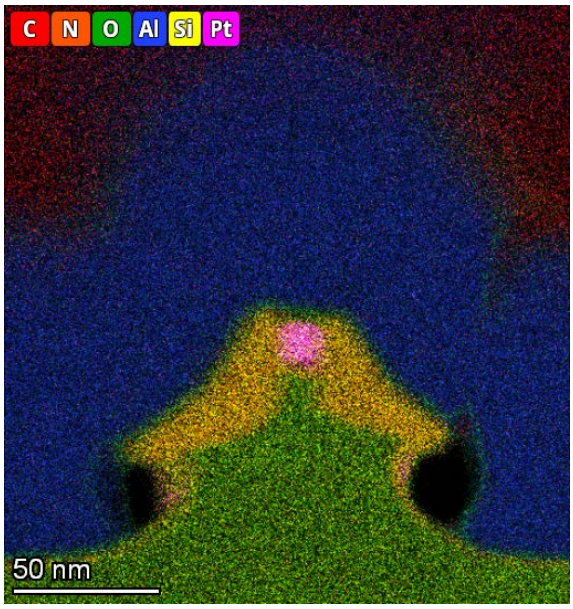

Figure 15: STEM cross sections of the platinum silicide filled nanogap using elemental mapping by energy dispersive X-ray tomography (50 nm scale bar).

Elemental mapping by energy dispersive X-ray tomography shown in figure 15, which shows clear localization of the platinum. Platinum and silicon signatures can be seen in the nanogap and in the undercut region which were not removed by the aqua regia etching, suggesting the presence of platinum silicide. The difference between evaporation and sputtering of metals can be seen by the presence of platinum, which was sputtered, in the undercut region however the aluminium deposition formed a void under the region shadow masked by the silicon nitride. This suggests that it may be possible to localize platinum silicide formation to only inside the nanogap by switching to evaporating platinum in the step at figure 3D. Despite this, the predominant platinum silicide structures remain the nanowire confined by the nanogap.

IV. Conclusion

We present a scalable and versatile approach to creating nanofeature based on microscale I-line lithography by use of self-aligned processing. This allows for complex 3D structures with fine control of nanoscale features by tuning edge retraction, sidewall oxidation, and corner lithography parameters. Additionally, it allows for versatile extension into creating not only nanogaps, but nanowires and coaxially aligned holes compatible with both low volume prototyping and high-volume production. This may serve as a technology to enable flow through membranes with incorporated nanofeatures for electrical sensing, filtration, and catalysis.

Acknowledgment

We would like to thank our consortium partners, in particular Dr. Niels Cornelisse (AmsterdamUMC-location Vrije Universiteit Amsterdam), for discussions leading to pursuing this research. We also thank the technicians and support staff at the MESA+ Nanolab for their tireless efforts in running and maintaining our cleanroom facilities.

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