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Investigation and validation of PV fed reduced switch asymmetric multilevel inverter using optimization based selective harmonic elimination technique

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ABSTRACT

Pulse width modulation for Selective Harmonics Elimination (SHE) is mostly employed in the reduction of lower order harmonics. The PV system in this research provides input voltage to the reduced switch 31-level inverter, which is based on the Artificial Bee Colony algorithm. With a high gain DC-DC single-ended primary-inductor converter (SEPIC), the PV panel output voltage is kept constant. The Grey wolf optimization algorithm (GWO) approach is used to get the most power out PV scheme. Multi Carrier modulation, a high-frequency modulation technology, is also used in this novel design of the inverter to reduce upper order harmonics. The suggested Artificial Bee Colony (ABC) algorithm, harmonics is compared to a SHE technique based on a genetic algorithm. The hardware findings were confirmed using DSPIC30F2010 controller simulation, and the recommended system was validated using Matlab simulation.

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KEYWORDS
Multilevel inverter; SEPIC converter; selective harmonics elimination; MPPT algorithm; GWO algorithm; multi carrier; DSPIC controller

1. Introduction

Solar powered stand-alone voltage source inverters have become increasingly popular in low- and medium-power claims in latest ages. Because of their power electronic circuitry, traditional inverters contain higher order harmonics. The life of electrical and electronic equipment is shortened because of harmonics. A multilevel inverter is used to address the harmonic difficulties [1]. The switching stress and switching loss of power semiconductor circuitry are reduced by using a multilevel inverter (MLI). PV (Photovoltaic) systems have become increasingly important in our daily lives in this century. However, in a PV system, higher order waves are present in the output voltage, as well as in the output power is varied due to natural temperature and irradiance variations. The MPPT method, along with a proper converter, overcomes these limitations. The output voltage of a multilevel inverter is generally regulated by sinusoidal PWM, however, switching losses and Total Harmonic Distortions are slightly higher in high-frequency modulation approaches. The adaptive selective Harmonics Elimination approach overcomes these disadvantages. Here are some existing works of literature that are discussed. The three primary types of multilevel inverters are diode clamped multilevel inverters, capacitor type multilevel inverters, and cascaded H bridge inverters. The Cascaded H-Bridge Multilevel Inverter (CHBMLI) is widely utilized of these three types due to its little capacity, compact interchanging pressure and losses, capabilities, and high efficiency. CHBMLI is divided into two types: symmetrical MLI and asymmetrical MLI. In symmetrical MLI, the number of switches used is extremely high. In paper [1], author discussed about reduced switch symmetrical MLI with different values, this topology achieves output voltage with fewer shifts. But high-frequency variation increases the losses. In paper [2] author discussed about the multi-level inverter that reduces the harmonics level but it is suitable only for low-power applications. The numbers of DC voltage sources are reduced by switched capacitor MLI [3]. But here the capacitor induces a voltage stability problem. The high-frequency modulation drawbacks are overcome by selective harmonics elimination technique [4]. But this inverter is not suitable for nonlinear loads.

The input voltage from switched rectifier requires large amount of capacitor bank and also need EB supply. These drawbacks are overcome by [5], PV based cascaded MLI. But the control technique used in this paper is level shifted and phase shifted PWM techniques. The

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suggested inverter's application regions are reduced using these strategies. Boosting gain inverters is presented in [6,7]. But the number of switches in this topology is large, and the control circuit is likewise complicated.

PV based T-shape inverter has analysed in paper [8]. This inverter is ideal for PV systems that are connected to the grid. MLI with SHE PWM method is used with current source rectifiers in [9]. A current source rectifier, on the other hand, quality while increasing losses. The strategies for removing selective harmonics in general are explained in [10]. This technique will be extremely beneficial in the development of future SHE techniques. To lower the harmonics, various forms of selective harmonics reduction approaches are presented in [11,12]. It is discussed how to remove chosen harmonics using four quadrant operation. in [13–15]. The reduction of selective harmonics with a smaller number of DC source based Multilevel Inverters is described. in [16,17]. A SHE technique based on a parallel resultant elimination procedure is used in [18]. The proposed inverter in this technique features a large number of switches. The use of a SHE system and a DC-DC converter to power an MLI is discussed in [19,20]. However, for the boost converter switch, a low gain DC–DC boost converter utilized.

For the removal of unwanted lower order harmonics in the cascaded H-bridge multilevel inverter, a hybrid asynchronous particle swarm optimization-genetic algorithm (APSO-GA) is proposed (MLI). The APSO-GA is applicable to all MLI levels. The proposed method combines ring topology-based APSO with GA. APSO is used for exploration, while GA is used to extract the best solutions. APSO-GA is used to calculate optimized switching angles for seven-level and nine-level inverters, and the results are compared to GA, PSO, APSO, bee algorithm (BA), differential evolution (DE), synchronous PSO, and teaching-learning-based optimization (TLBO). The performance of APSO-GA is validated experimentally on a single-phase seven-level inverter [21].

A preliminary examination of existing control techniques revealed that selective harmonic elimination pulse-width modulation (SHEPWM) is more capable of removing low-order harmonics. However, the nonlinear transcendental equations used in this technique are difficult to solve, especially for calculus-based methods. Bio-inspired intelligent algorithms (BIAs) appear to be a better approach for solving these complex equations with the advent of powerful and low-cost computers. This review paper explains the basic operation of nine well-known BIAs and discusses their use in inverters for harmonic elimination (HE). The paper covers all of the important information about HE in inverters, which will assist researchers in designing an efficient RE conversion system [22].

Hybrid asynchronous PSO-Newton–Raphson (APSO-NR) algorithm based on selective harmonic elimination pulse width modulation technique for the elimination of undesired harmonics in cascaded H-bridge multilevel inverter. The proposed algorithm works for all levels of MLI with equal and unequal DC sources. The proposed method combines the ring topology-based APSO algorithm with the NR method. APSO was used as a global search technique, while NR was used to refine the best solutions. To eliminate fifth and seventh harmonics, APSO-NR is applied to the seven-level inverter. In simulations, the proposed algorithm's performance is compared to that of the genetic algorithm, the bee algorithm, and particle swarm optimization [23].

The suggested work solves all of the existing issues. The PV system's input voltage converter in this suggested system. The output voltage is fine-tuned using the GWO algorithm-based PI controller. The suggested reduced switch 31-level inverter is provided varied output voltages. High frequency modulation and selective harmonics removal techniques are used to regulate the inverter. In the result and discussion chapter, the THD parameters are shown in the comparison result.

2. Proposed system

Figure 1 depicts 31-level inverter. The PV system's highly oscillated voltage is fed into the DC-DC, which maintains a constant feedback. The GWO method is used to achieve the needed DC output voltage to the multilevel inverter.

The error is sent to the comparator after the reference and actual voltages are compared. The SEPIC Converter's output is used to determine the actual voltage. The PI controller receives the error. decreases the that is used to generate PWM. The GWO algorithm adjusts the proportional and integral gain. To generate a PWM pulse, the reference and carrier signals are compared. The SEPIC Converter receives the PWM pulse. The compact switch multilevel Inverter receives the Converter, which produces four input voltages.

A single H Bridge inverter and a voltage multiplier circuit make up the proposed system's reduced switch multilevel inverter. For a 31-level inverter, the power circuit includes eight MOSFETs and four DC sources.

The multilayer inverter is regulated via Multi Carrier Modulation. High frequency modulation is another name for the MCM technology. THD and considerable techniques. To overcome these challenges, a selective harmonics removal approach based on Artificial BEE colonies is developed, and the results are compared to those of a genetic algorithm.

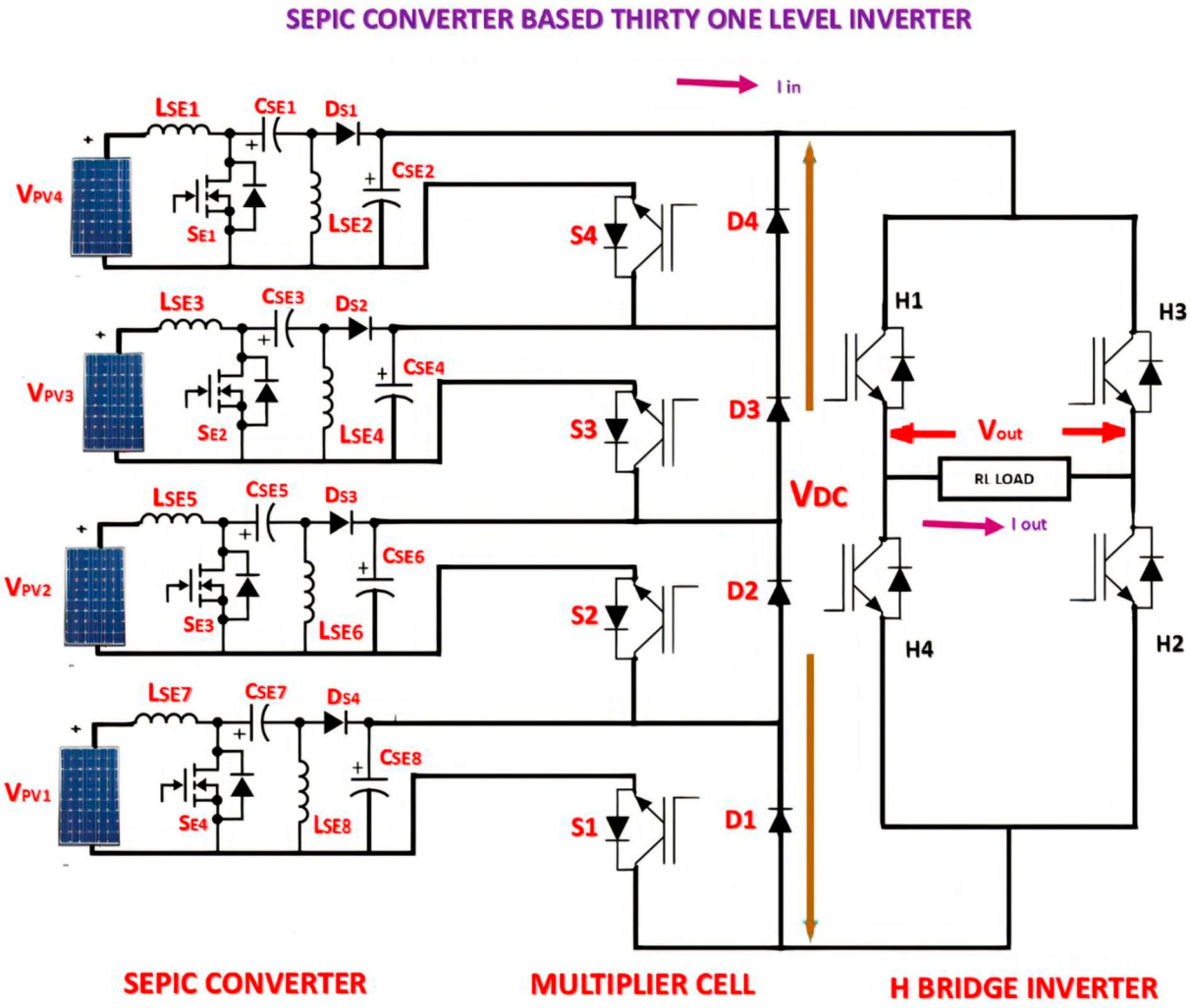


Figure 1. Proposed system circuit diagram.

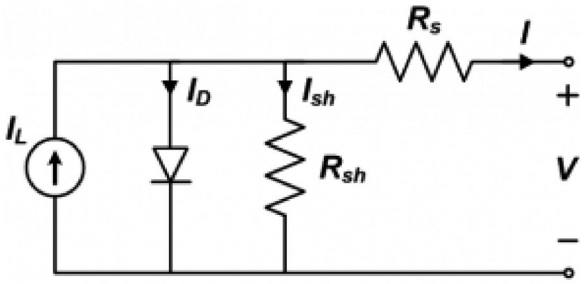


Figure 2. One diode model of the PV system.

3. PV panel modeling

The equivalent circuit which represents one diode model of the PV system is shown in Figure 2. One of the most commonly used solar cell models is the single-diode model, also known as the five-parameter model.

The I–V characteristic of the solar cell is given as follows by the implicit and nonlinear equation.

$$I = I_L - I_0 \left[\exp\left(\frac{V + IR_s}{n V_T} \right) - 1 \right] - \frac{V + I R_s}{R_{sh}} \quad (1)$$

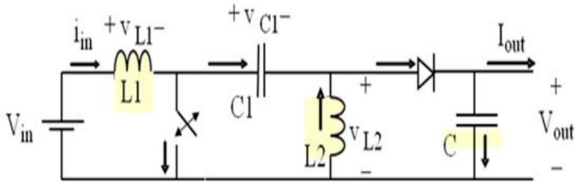


Figure 3. Proposed SEPIC converter circuit diagram.

where I_L, light current (A); I_0, diode reverse saturation current (A); R_s, series resistance (Ω); R_{sh}, shunt resistance (Ω); n, diode ideality factor (unit less).

4. SEPIC converter

SEPIC is a DC to DC converter that can function in either step up or step down mode and is extensively used in battery-powered devices by altering the duty cycle of the gate signal of the MOSFET (see Figure 3). We may change the voltage by stepping up or down. It will step up the voltage if the duty cycle is more than 0.5, and it will step down the voltage if the duty cycle is less than 0.5.

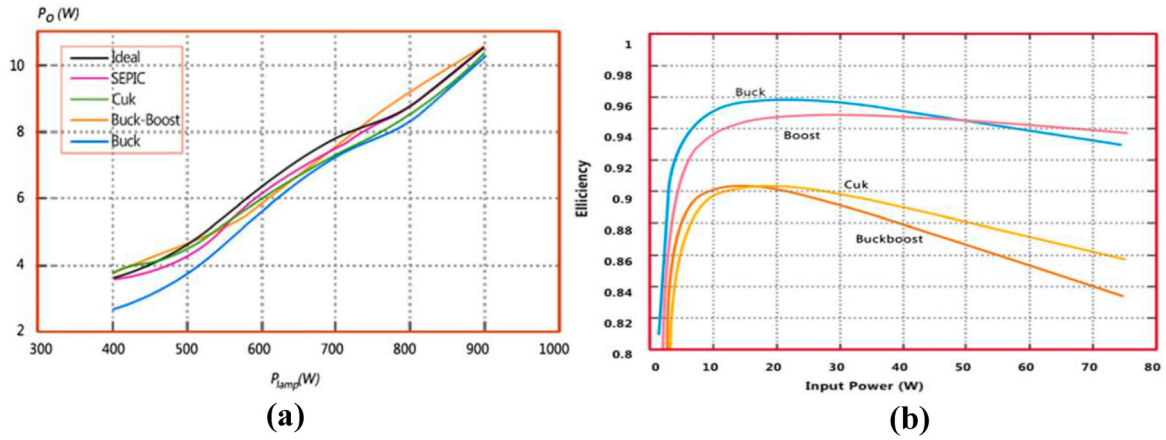


Figure 4. (a) Comparing the tracking capabilities of the different converters. (b) Efficiencies of four DC–DC converter configurations.

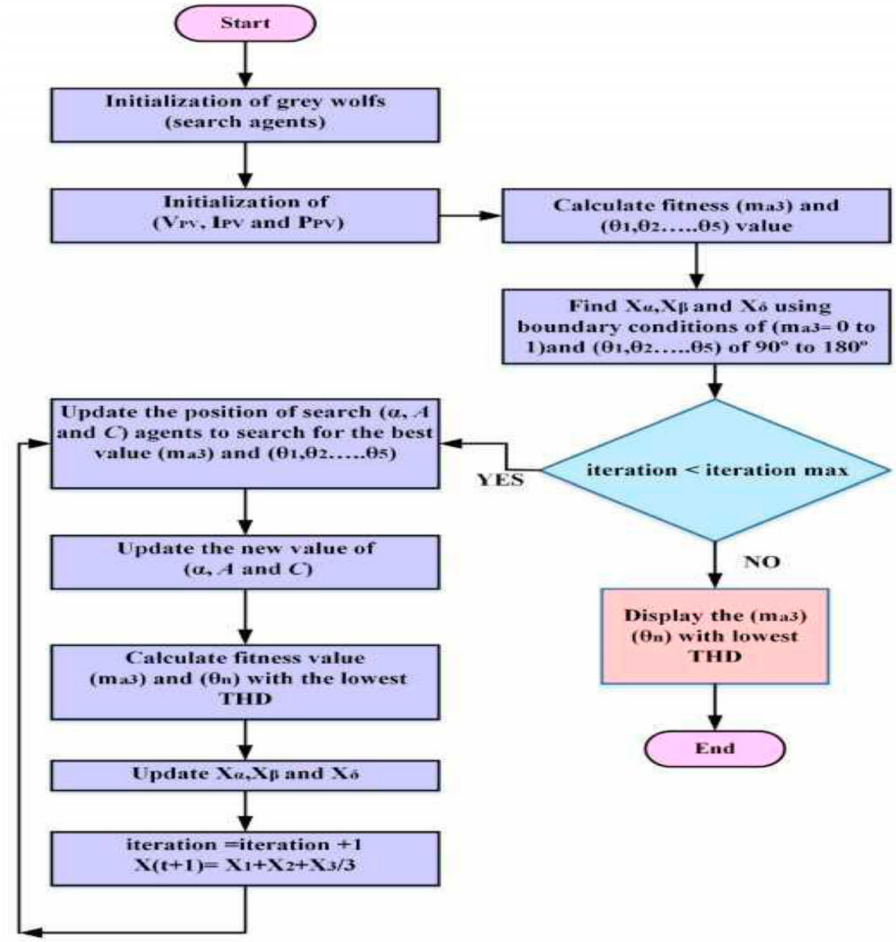


Figure 5. Flow chart for GWO-based optimization algorithm.

A comprehensive comparison of several converters accessible in the literature, such as cuk converter, buck boost, and buck converter, is done in order to verify the suggested sepic converter. Figure 4 shows the parameters such as tracking capabilities and efficiency that are examined using a traditional converter.

SEPIC is not the most efficient or cost-effective, according to the aforementioned assessments.

Buck–Boost and SEPIC converters are excellent for MPPT applications because their operations are not affected by radiation or temperature, allowing them to follow the maximum point.

5. Grey wolf optimization algorithm

The flowchart of Grey Wolf Optimization Algorithmare shown in Figure 5.

Table 1. Firing sequence of proposed 31-level inverter.

Voltage levels	S4	S3	S2	S1	H1	H2	H3	H4
Vin	ON	ON	ON	ON	ON	ON	OFF	OFF
14/15Vin	ON	ON	ON	OFF	ON	ON	OFF	OFF
13/15Vin	ON	ON	OFF	ON	ON	ON	OFF	OFF
12/15Vin	ON	ON	OFF	OFF	ON	ON	OFF	OFF
11/15Vin	ON	OFF	ON	ON	ON	ON	OFF	OFF
10/15Vin	ON	OFF	ON	OFF	ON	ON	OFF	OFF
09/15Vin	ON	OFF	OFF	ON	ON	ON	OFF	OFF
08/15Vin	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
07/15Vin	OFF	ON	ON	ON	ON	ON	OFF	OFF
06/15Vin	OFF	ON	ON	OFF	ON	ON	OFF	OFF
05/15Vin	OFF	ON	OFF	ON	ON	ON	OFF	OFF
04/15Vin	OFF	ON	OFF	OFF	ON	ON	OFF	OFF
03/15Vin	OFF	OFF	ON	ON	ON	ON	OFF	OFF
02/15Vin	OFF	OFF	ON	OFF	ON	ON	OFF	OFF
01/15Vin	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
−01/15Vin	OFF	OFF	OFF	ON	OFF	OFF	ON	ON
−02/15Vin	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
−03/15Vin	OFF	OFF	ON	ON	OFF	OFF	ON	ON
−04/15Vin	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
−05/15Vin	OFF	ON	OFF	ON	OFF	OFF	ON	ON
−06/15Vin	OFF	ON	ON	OFF	OFF	OFF	ON	ON
−07/15Vin	OFF	ON	ON	ON	OFF	OFF	ON	ON
−08/15Vin	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
−09/15Vin	ON	OFF	OFF	ON	OFF	OFF	ON	ON
−10/15Vin	ON	OFF	ON	OFF	OFF	OFF	ON	ON
−11/15Vin	ON	OFF	ON	ON	OFF	OFF	ON	ON
−12/15Vin	ON	ON	OFF	OFF	OFF	OFF	ON	ON
−13/15Vin	ON	ON	OFF	ON	OFF	OFF	ON	ON
−04/15Vin	ON	ON	ON	OFF	OFF	OFF	ON	ON
−Vin	ON	ON	ON	ON	OFF	OFF	ON	ON

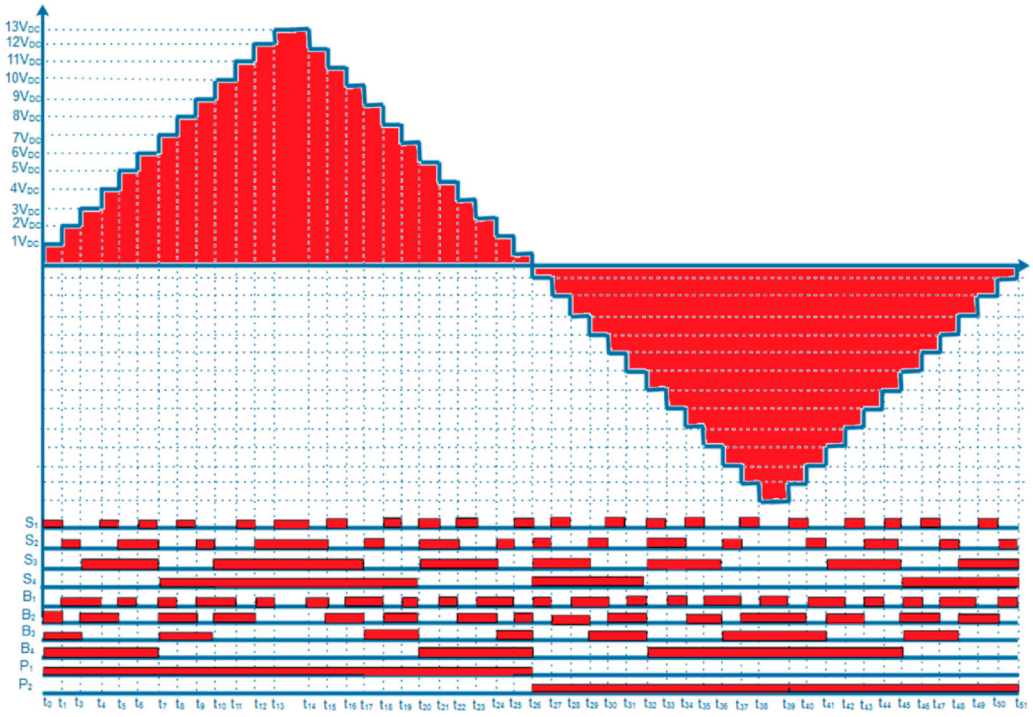


Figure 6. Angle generation for 31-level inverter.

6. Proposed system reduced switch MLI

A suggested 31-level inverter consists of four switches S1–S4, and four diodes D1–D4. In the positive half cycle, 15 levels of voltage are created, and in the negative half cycle, 15 levels of voltage are produced Table 1.

7. PWM generation

(a) **Multi carrier modulation**

Basic multicarrier modulation approach has been at first. The 50 Hz reference sinusoidal signal is compared

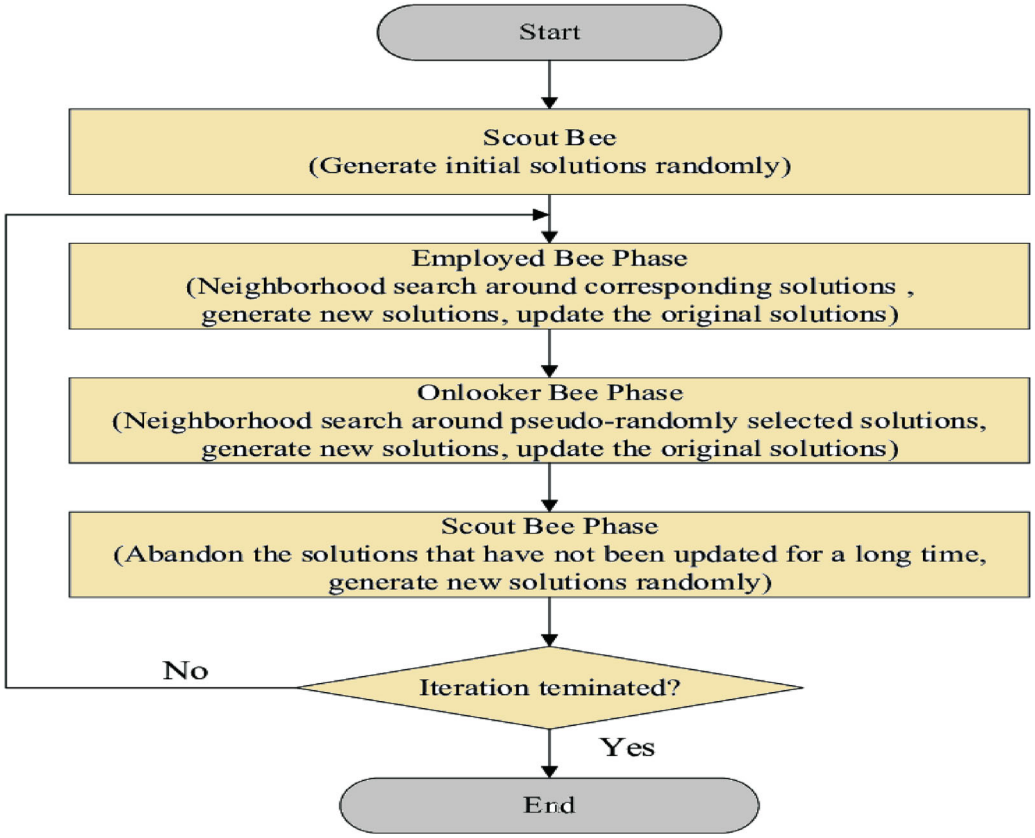


Figure 7. Flow chart for ABC-based optimization algorithm.

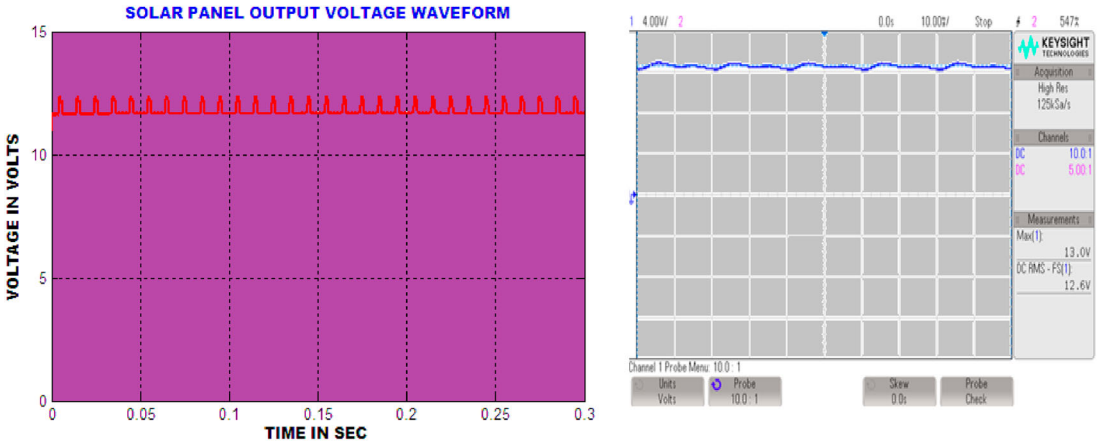


Figure 8. (a) Simulation result of PV panel output voltage waveform (b) Hardware result of PV panel output voltage waveform.

to 15 carrier signals with a switching frequency of 10 kHz. The output voltage levels of the suggested topology are varied using the modulation index M.I.

The angle generation for the suggested reduced switch 31-level multi-level inverter is shown in Figure 6.

Modulation index of the proposed 31-level inverter is,

$$\text{M.I} = \frac{V_{\text{ref}}}{15\,V_{\text{carr}}} \tag{2}$$

V_{carr} – Peak value of the carrier signal amplitude.
V_{ref} – Peak to peak value of the reference signal.

(b) **Selective harmonic elimination technique**

The inverter's output voltage may be stated as follows using harmonic elimination theory:

$$V\omega t = \sum_{n=1}^{\infty} V_n \sin(n\omega t) \tag{3}$$

where

V_n – $(0 < = \theta_i < = \pi/2)$. Since even order to be zero

$$V\omega t = \frac{4}{n\pi}[V_1 \cos(n\theta_1) + V_2 \cos(n\theta_2) \ldots\ldots\ldots\ldots + V_n \cos(n\theta_n)]\ \sin n\omega t \tag{4}$$

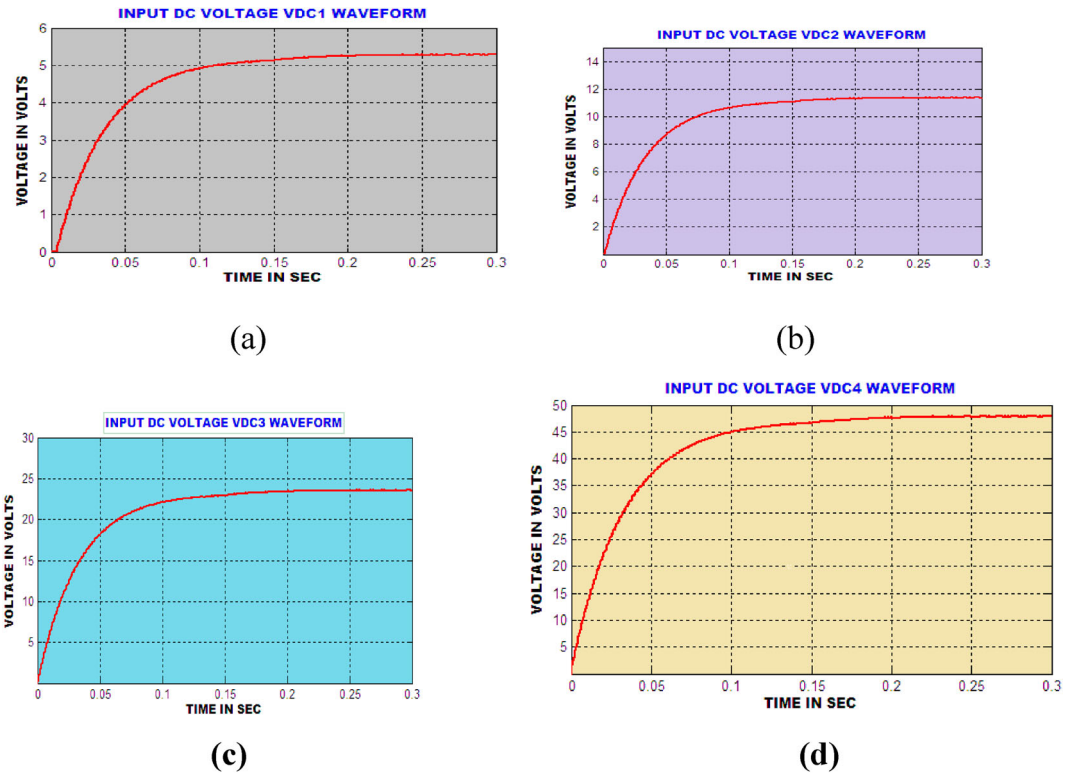


Figure 9. Matlab simulation result (a) 6 V DC voltage to MLI (b) 12 V DC voltage to MLI (c) 24 V DC voltage to MLI (d) 48 V DC voltage to MLI.

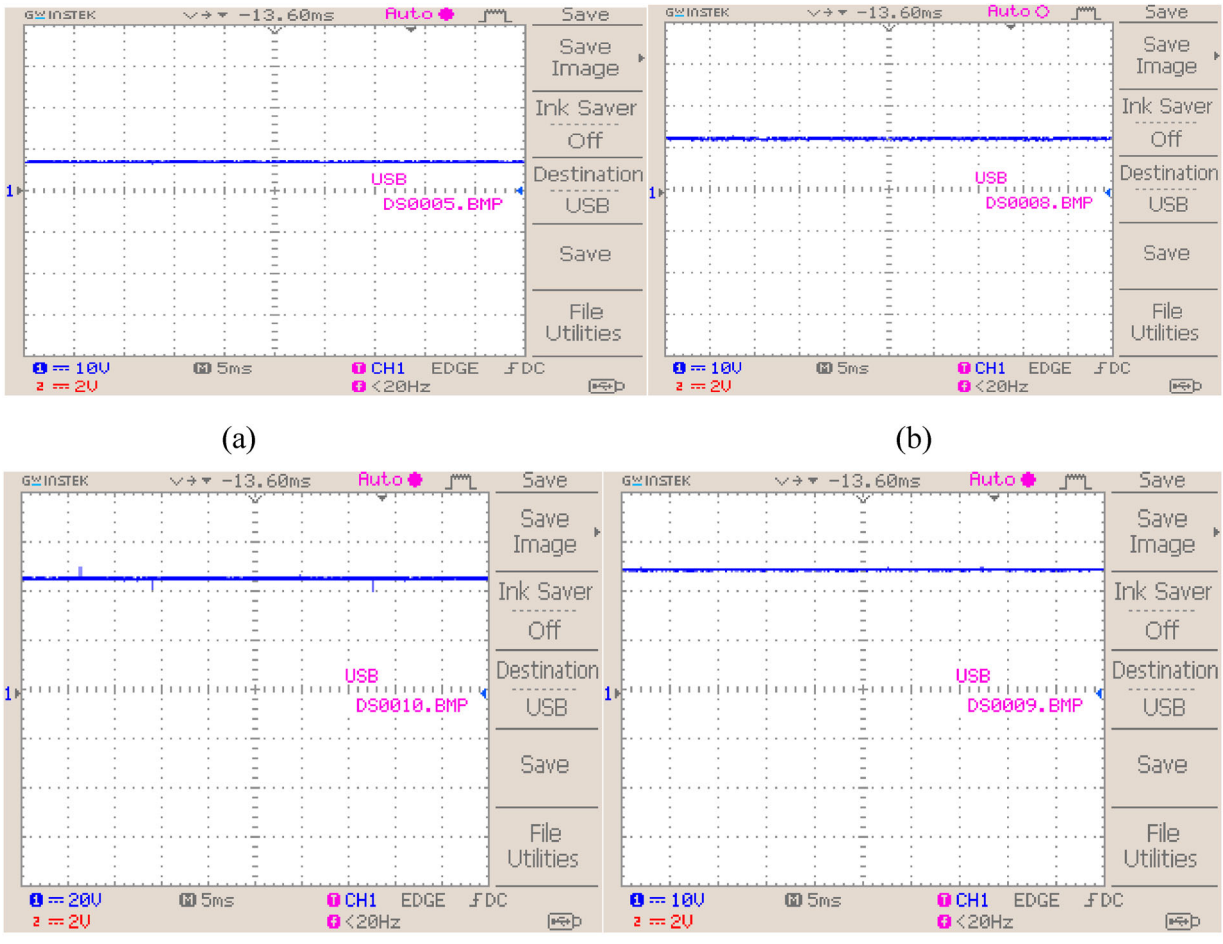


Figure 10. Hardware result (a) 6 V DC voltage to MLI (b) 12 V DC voltage to MLI (c) 24 V DC voltage to MLI (d) 48 V DC voltage to MLI.

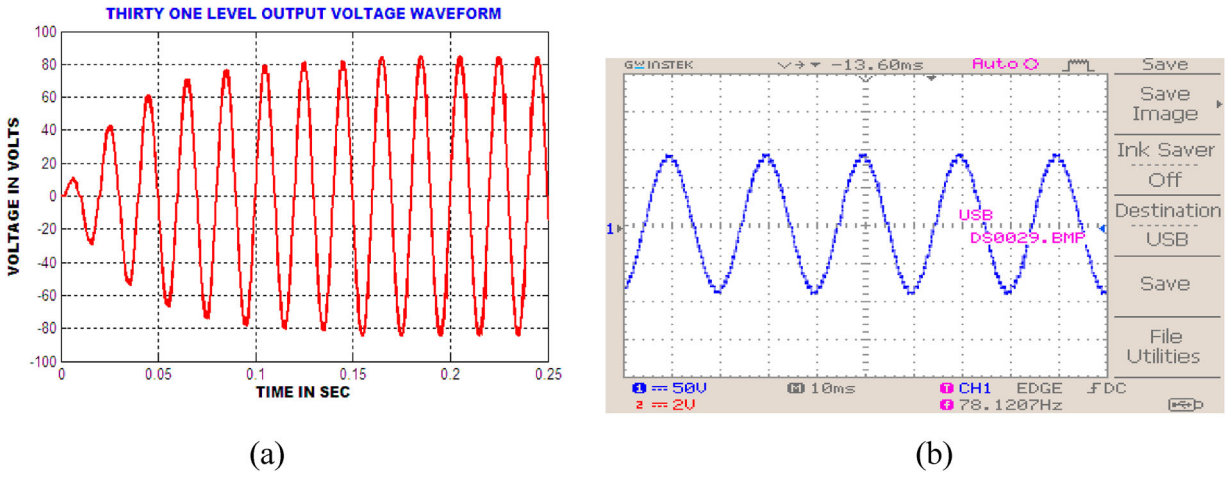


Figure 11. Proposed 31-level inverter output voltage waveform (a) Matlab Simulation (b) hardware implementation.

Table 2. Solar panel rating details.

Components	Specifications
Number of panels	4
Number of cells in series	36
Cell	125 mm × 31.25 mm
Open circuit voltage	21.4 V
Optimum operating voltage	16.8 V
Short circuit current	1.21 A
Optimum operating current	1.19 A
Operating temperature	−40 to +85°C
Maximum system voltage	1000 V DC

Table 3. SEPIC converter elements table.

Components	Symbols	Rating
Source voltage	v_{in}	6–20 V DC.
Source current	i_i	11 A
Capacitors	C_1, C_2	50 uf/100 v
Inductor	$L1$, $L2$	1 Mh
Output load current		1 Amps
Switching frequency	f	10 KHZ
Output power	P_0	200 W
Switching devices (all)		IRF250
Diodes (all)		MUR1560
Driver circuit		TLP 250

where $n = 1, 3, 5, 7$

Shortly

$$Vn = \begin{Bmatrix} \frac{4}{n\pi} \sum_{i=1}^{S} \cos(n\theta_1) & \text{for odd ns} \\ 0 & \text{for even ns} \end{Bmatrix} \quad (5)$$

The planned 31-level inverter is intended to reduce harmonics by up to 15 orders.

$$V_1 = \frac{4}{\pi}[V_1 \cos(\theta_1) + V_2 \cos(\theta_2) \ldots\ldots\ldots\ldots + V_{15} \cos(\theta_{15})]$$

$$V_3 = \frac{4}{3\pi}[V_1 \cos(3\theta_1) + V_2 \cos(3\theta_2) \ldots\ldots\ldots\ldots + V_{15} \cos(3\theta_{15})]$$

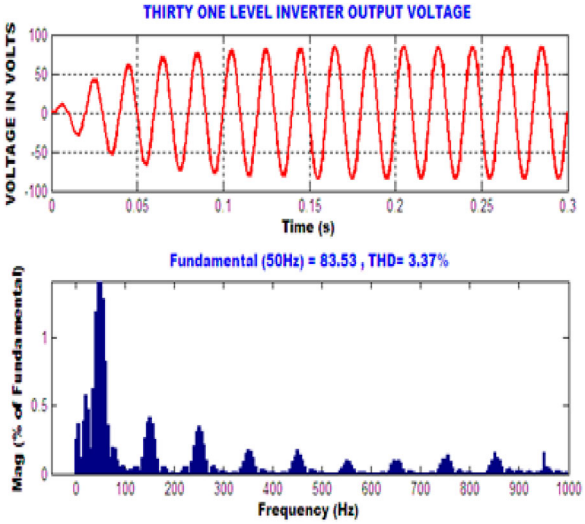


Figure 12. Simulation THD result of 31-level inverter using MCM technique.

$$V_5 = \frac{4}{5\pi}[V_1 \cos(5\theta_1) + V_2 \cos(5\theta_2) \ldots\ldots\ldots\ldots + V_{15} \cos(5\theta_{15})] \quad (6)$$

$$V_{15} = \frac{4}{15\pi}[V_1 \cos(15\theta_1) + V_2 \cos(15\theta_2) \ldots\ldots\ldots\ldots + V_{15} \cos(15\theta_{15})]$$

(C) Artificial Bee Colony Algorithm

The flowchart of Artificial Bee Colony Algorithm (ABC) is shown in Figure 7.

A. SHEPWM based Bee algorithm? <?pag

Rung 1: Initialization of the preliminary parameter θ_i, $i = 1, 2, \ldots\ldots SN$.

Rung 2: estimate the values of a theta

Rung 3: phase $= 1$

Rung 4: replicate

Table 4. Angle generation for 31-level inverter using SHE technique.

Angle	$\alpha 1$	$\alpha 2$	$\alpha 3$	$\alpha 4$	$\alpha 5$	$\alpha 6$	$\alpha 7$	$\alpha 8$	$\alpha 9$	$\alpha 10$	$\alpha 11$	$\alpha 12$	$\alpha 13$	$\alpha 14$	$\alpha 15$
ABC-SHE	5.97	11.02	16.7	22.6	29.1	34.8	41.6	47.6	52.9	58.7	65.2	71.1	77.3	83.1	89.6
GA	5.98	10.97	16.9	23.1	29.3	35.2	40.7	46.8	53.2	57.6	64.3	70.2	77.1	82.8	88.9

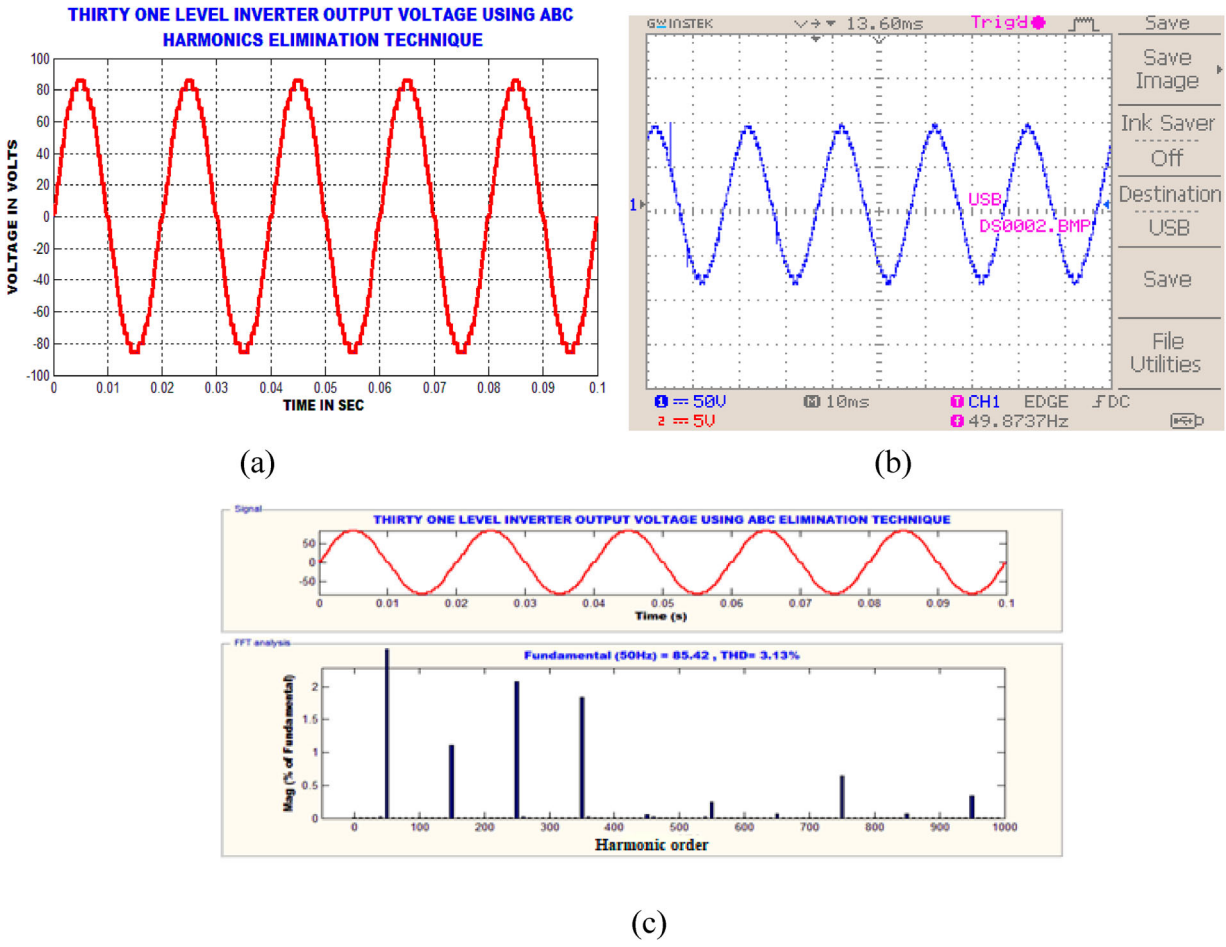


Figure 13. (a) Simulation output voltage 31-level inverter using ABC based SHE technique (b) Hardware output voltage 31-level inverter using ABC based SHE (c) FFT analyse of proposed 31-level inverter using ABC-SHE technique.

Rung 5: Produce and evaluate new Vi solution for the bees employed, using the equation below.

$$V_{ij} = \theta_{ij} + \varphi_{ij}(\theta_{ij} - \theta_{kj})$$

where $k\,e\{1, 2, \ldots\ldots.\text{SN}\}andj\,e\{1, 2, \ldots\ldots D\}$
Rung 6: For the working bees apply the greedy selection method.
Rung 7: Test the Pi chance of the solution θ_i
Rung 8: Produce and evaluate the new Vi solution for onlookers from the θi solution selected depending on Pi.
Rung 9: Apply the onlooker's greedy selection process to bees.
Rung 10: Determine the scout's abandoned solution, if available, and replace it with a new solution produced at random
Rung 11: remember the perfect solution so far found
Rung 12: sequence = sequence +1
Rung 13: until sequence = maximum cycle number (MCN).

8. Results and discussion

In a Matlab simulation, the proposed work has been implemented, with DSPIC30F2010 controller as the hardware.

The characteristics of the solar panel utilized in this system are shown in Table 2.

The Figure 8a shows the Matlab simulation output voltage from the solar PV panel and figure 8b shows the corresponding hardware result of solar PV panel output voltage waveform.

The SEPIC converter produces four DC voltages in the range of 6, 12, 24, and 48 V, The SEPIC converters' ratings are listed in Table 3.

Figure 9 shows the input DC voltages simulated using Matlab software in the ranges of 6, 12, 24, and 48 V.

Figure 10 shows how input DC voltages in the range of 6, 12, 24, and 48 V are created with the aid of a controller for developing a laboratory prototype.

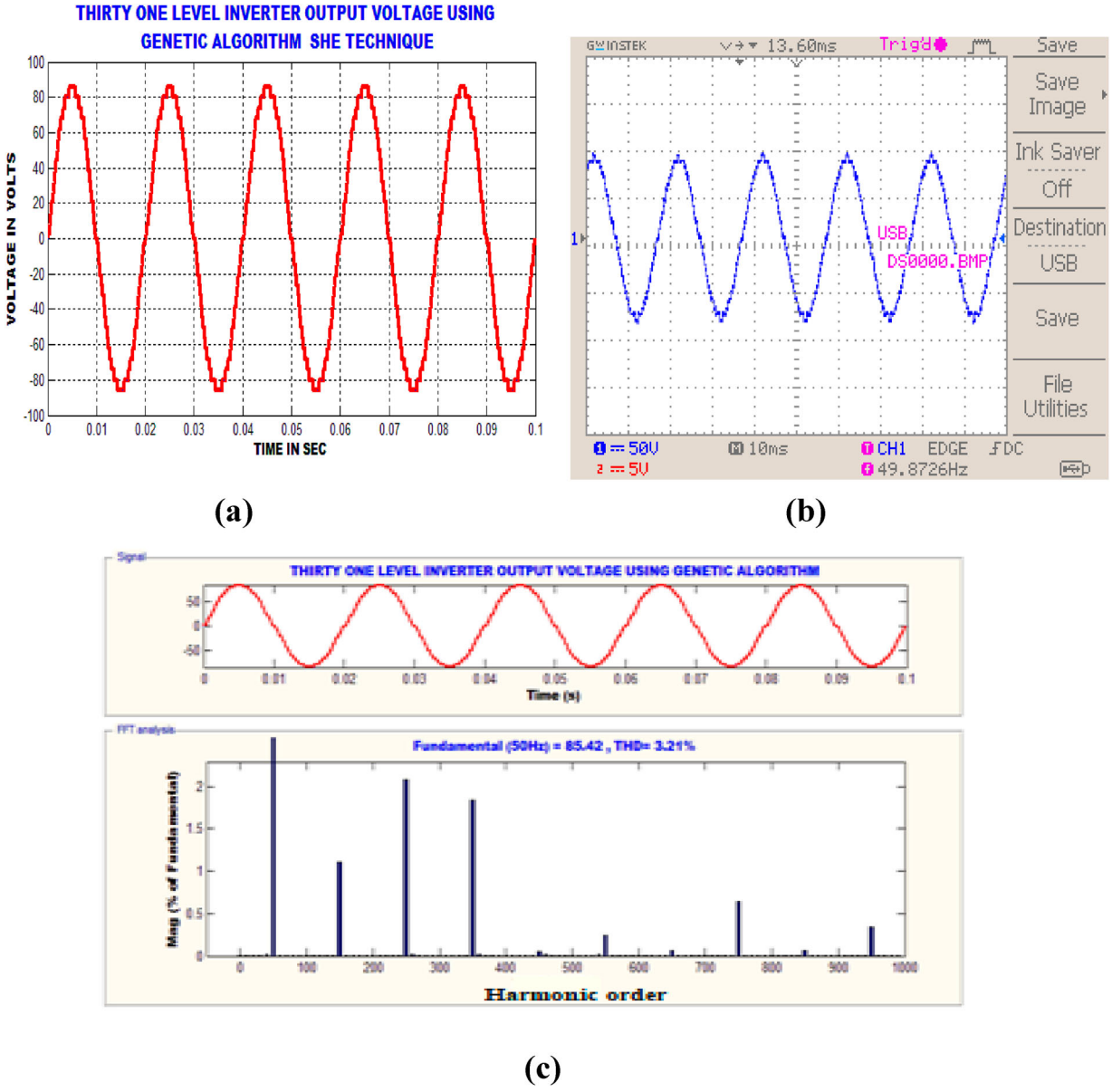


Figure 14. (a) Simulation output voltage 31-level inverter using GA technique (b) Hardware output voltage 31-level inverter using GA (c) FFT analyse of 31-level inverter using GA technique.

Figure 11 depicts the v waveform of a 31-level inverter utilizing the Multi carrier modulation approach with a modulation index of 0.95.

The multilayer inverter is controlled using the multicarrier modulation method (MCM). A PI controller is used to create the reference signal.

Figure 12 presents the Matlab simulation output and corresponding FFT analysis of proposed 31-level inverter by using multi carrier modulation (MCM) technique and FFT analysis are made and total harmonic distortion (THD) 3.37%

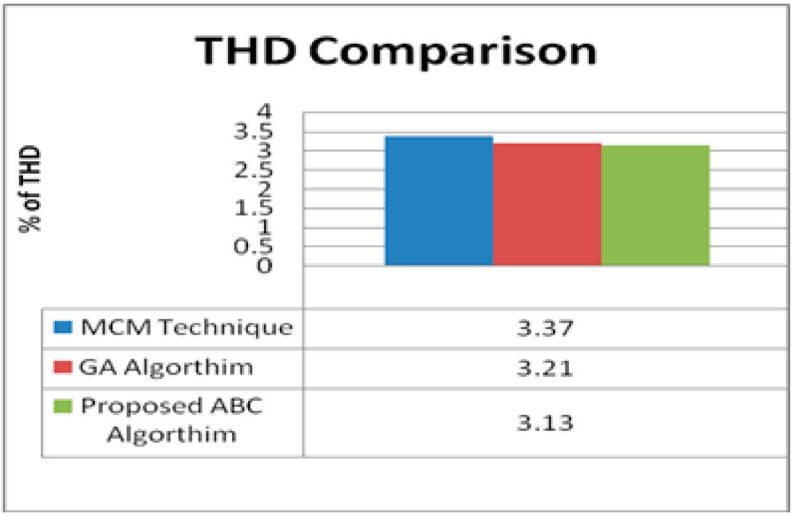
Table 4 shows the various firing angles created by the evolutionary algorithm and the Artificial BEE colony-based selective harmonics removal approach. The proposed Artificial BEE colony based SHE optimization technique gives the best firing angle compared to the genetic algorithm based angle generation approach. Using the DSPIC30F2010 controller, the suggested multilayer inverter is given this firing angle obtained by the ABC- SHE approach.

Figure 13 shows the Matlab simulation and hardware output voltage and FFT analyse of the proposed 31-level inverter using Artificial Bee colony based SHE Elimination technique and FFT analysis are made and total harmonic distortion (THD) 3.13% < 5% THD value which satisfies IEEE519 harmonic standard.

Figure 14 shows the Matlab simulation and hardware output voltage and FFT analyse of the proposed 31-level inverter using Genetic algorithm based SHE Elimination technique and FFT analysis are made and total harmonic distortion (THD) 3.21%.

The hardware experimental laboratory prototype is being carried out to test the system performance with the help of DSPIC30F2010 controller. It is observed that the total harmonic distortion is 5.18% to closely match with the simulation results and proposed ABC

(a) (b)



(c)

Figure 15. Experimental THD analyse of proposed MLI (b) Experimental prototype for proposed 31-level MLI system (c) THD comparison.

algorithm technique THD are compared with Multi carrier modulation and Genetic algorithm are shown in Figure 15.

9. Conclusions

Selective Harmonics Elimination PWM based on the suggested Artificial Bee Colony method is mostly utilized to remove lower order harmonics. Using a high gain DC-DC SEPIC converter, the GW gets the most power from the PV system. Multi carrier modulation is used to design and assess the decreased switch suggested 31-level inverters. Finally, the THD's of the two SHE approaches and the techniques for high-frequency modulation are compared; the ABC SHE technique generates fewer harmonic content other than two procedures. The suggested system has been confirmed by Matlab simulation, and the hardware results have been verified using controller.

Disclosure statement

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References

[1] Babaei E, Laali S, Bayat Z. A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches. IEEE Trans Ind Electron. 2015;62(2):922–929.
[2] Tariq M, Meraj M, Azeem A, et al. Evaluation of level-shifted and phase-shifted PWM schemes for seven level single-phase packed U cell inverter. CPSS Trans Power Elect Appl. 2018;3(3):232–242.
[3] Barzegarkhoo R, Kojabadi H, Zamiry E, et al. Generalized structure for a single phase switched-capacitor multilevel inverter using a new multiple DC link producer with reduced number of switches. IEEE Trans Power Electron. 2016;31(8):5604–5617.
[4] Vijayakumar A, Stonier AA, Peter G, et al. Power quality enhancement in asymmetrical cascaded multilevel inverter using modified carrier level shifted pulse width modulation approach. IET Power Electron. 2022 Nov: pel2.12429. doi:10.1049/pel2.12429.

[5] Chavarria J, Biel D, Guinjoan F, et al. Energy-balance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs. IEEE Trans Ind Electron. 2013;60(1): 98–111.
[6] Lee SS. A single-phase single-source 7-level inverter with triple voltage boosting gain. IEEE J Magazines. 2018;6:30005–30011.
[7] Chavarria J, Biel D, Guinjoan F, et al. Energy-balance control of PV cascaded multilevel grid-connected inverter sunder level-shifted and phase-shifted PWMs. IEEE Trans Ind Electron. 2013;60(1):98–111.
[8] Peter G. A review about vector group connections in transformers. Int J Adv Technol. ISSN: 0976-4860 (Online). 2011;2(2):215–221.
[9] Ni R, Li YW, Zhang Y, et al. Virtual impedance-based selective harmonic compensation (VI-SHC) PW for current source rectifiers. IEEE Trans Power Electron. 2014;29(7):3346–3356.
[10] Wells JR, Nee BM, Chapman PL, et al. Selective harmonic control: a general problem formulation and selected solutions. IEEE Trans Power Electron. 2005;20(6):1337–1345.
[11] Kavousi A, Vahidi B, Salehi R, et al. Application of the Bee algorithm for selective harmonic elimination strategy in multilevel inverters. IEEE Trans Power Electron. 2012;27(4):1689–1696.
[12] Ahmed M, Sheir A, Orabi M. Real-Time solution and implementation of selective harmonic elimination of seven-level multilevel inverter. IEEE J Emerg Sel Top Power Electron. 2017;5(4):1700–1709.
[13] Yang K, Yuan Z, Yuan R, et al. A Groebner bases theory-based method for selective harmonic elimination. IEEE Trans Power Electron. 2015;30(12):6581–6592.
[14] Zhetessov A, Ruderman A. 2017. Simultaneous selective harmonic elimination and total harmonic distortion minimization for a single-phase multilevel inverter with staircase modulation. In 2017 International Conference on Optimization of Electrical and Electronic Equipment (OPTIM) & 2017 Intl Aegean Conference on Electrical Machines and Power Electronics (ACEMP), 729–34. Brasov, Romania: IEEE, 2017. doi:10.1109/OPTIM.2017.7975055.
[15] Zhao H, Wang S. A four-quadrant modulation technique to extend modulation index range for multilevel selective harmonic elimination compensation using staircase waveforms. IEEE J Emerg Sel Top Power Electron. March 2017;5(1):233–243.
[16] Vijayakumar A, Alexander Stonier A, Geno Peter G, et al. A modified seven-level inverter with inverted sine wave carrier for PWM control. Int Trans Elect Energy Sys. 2022;2022:1–12. doi:10.1155/2022/7403079.
[17] Buccella C, Cecati C, Cimoroni MG, et al. Analytical method for pattern generation in five-level cascaded H-bridge inverter using selective harmonic elimination. IEEE Trans Ind Electron. 2014;61(11):5811–5819.
[18] Yang K, Chen L, Zhang J, et al. Parallel resultant elimination algorithm to solve the selective harmonic elimination problem. IET Power Electron. 2016;9(1):71–80.
[19] Filho F, Tolbert LM, Cao Y, et al. Real-time selective harmonic minimization for multilevel inverters connected to solar panels using artificial neural network angle generation. IEEE Trans Ind Appl. 2011;47(5):2117–2124.
[20] Etesami; NaeemFarokhnia MH, Hamid Fathi S. Colonial competitive algorithm development toward harmonic minimization in multilevel inverters. IEEE Trans Ind Inf. 2015;11(2):459–466.
[21] Memon MA, Siddique MD, Mekhilef S, et al. Asynchronous particle swarm optimization-genetic algorithm (APSO-GA) based selective harmonic elimination in a cascaded H-bridge multilevel inverter. IEEE Trans Ind Electron. 2022 Feb;69(2):1477–1487. doi:10.1109/TIE.2021.3060645.
[22] Memon MA, Mekhilef S, Mubin M, et al. Selective harmonic elimination in inverters using bio-inspired intelligent algorithms for renewable energy conversion applications: a review. Renew Sust Energy Rev. 2018;82:2235–2253.
[23] Memon MA, Mekhilef S, Mubin M. Selective harmonic elimination in multilevel inverter using hybrid APSO algorithm. IET Power Electron. 2018;11(10):1673–1680.