RELIABLE DESIGN OF TUNNEL DIODE AND RESONANT TUNNELLING DIODE BASED MICROWAVE SOURCES

BY

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DEDICATION

This thesis is dedicated to my parents Xinxiang Wang & Dongmei Yan and my sister Liwei Wang

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ABSTRACT

This thesis describes the reliable design of tunnel diode and resonant tunnelling diode (RTD) oscillator circuits. The challenges of designing with tunnel diodes and RTDs are explained and new design approaches discussed. The challenges include eliminating DC instability, which often manifests itself as low frequency parasitic oscillations, and increasing the low output power of the oscillator circuits.

To stabilise tunnelling devices, a common but sometimes ineffective approach is the use of a resistor of suitable value connected across the device. It is shown in this thesis that this resistor tunnel diode circuit can be described by the Van der Pol model. Based on this model, design equations have been derived which enable the design of current-voltage *(I-V)* measurement circuits that are free from both low frequency bias oscillations and high frequency parasitic oscillations. In the conventional setup, the I-V characteristic of the tunnelling device is extracted from the measurement by subtracting from the measured current the current through the stabilising resistance at each bias voltage. In this thesis, also using the Van der Pol model, a circuit for the direct measurement of I-V characteristics is proposed. This circuit utilises a series resistor-capacitor combination in parallel with the tunnelling device for stabilisation. Experimental results show that I-V characterisation of tunnel diodes in the negative differential resistance (NDR) region free from oscillations can be made.

A new test set-up suitable for radio frequency (RF) characterisation of tunnel diodes over the entire NDR region was also developed. Initial measurement results on a packaged tunnel diode indicate that accurate characterisation and subsequent small-signal equivalent circuit model extraction for the NDR region can be done.

To address the limitations of low output power of tunnel diode or RTD oscillators, a new multiple device circuit topology, incorporating a novel design methodology for the DC bias decoupling circuit, has been developed. It is based on designing the oscillator specifically for sinusoidal oscillations, and not relaxation oscillations which are also possible in tunnel diode oscillators. The oscillator circuit can also be described by the Van der Pol model which provides theoretical predictions of the maximum inductance, in terms of the tunnel diode device parameters, that is required to resonate with the device capacitance for sinusoidal oscillations. Each of the tunnel diodes in the multiple device oscillator circuit is decoupled from the others at DC and so can be stabilised independently. The oscillator topology uses parallel resonance but with each tunnel diode individually biased and DC decoupled making it possible to employ several tunnel diodes for higher output power. This approach is expected to eliminate parasitic bias oscillations in tunnel diode oscillators whilst increasing the output power of a single oscillator. Simulation and experimental oscillator results were in good agreement, with a two-tunnel diode oscillator exhibiting approximately double the output power as compared to that of a single tunnel diode oscillator, i.e. 3 dB higher.

Another method considered for the realisation of higher output power tunnel diode or RTD oscillators was series integration of the NDR devices. A new method to suppress DC instability of the NDR devices connected in series with all the devices biased in their NDR regions was investigated. It was successfully employed for DC characterisation with integrations of 2 and 5 tunnel diodes. Even though no suitable oscillator circuit topology and/or methodology with series-connected NDR devices could be established for single frequency oscillation, the achieved results indicated that this approach may be worthy of further investigation.

The final aspect of this project focussed on the monolithic realisation of RTD oscillators. Monolithic oscillators in coplanar waveguide (CPW) technology were successfully fabricated and worked at a fundamental frequency of 17.5 GHz with -21.83 dBm output power. Finally, to assess the potential of RTD oscillators for high frequency signal generation, a theoretical analysis of output power of stabilised RTD oscillators was undertaken. This analysis suggests that it may be possible to realise RTD oscillators with high output power ($\backsim$ 0 dBm) at millimetre-wave and low terahertz (up to 1 THz) frequencies.

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CHAPTER 1

INTRODUCTION

Millimetre-wave and submillimetre-wave signal sources are widely required for a variety of applications, such as medical imaging and radio astronomy [1], upper atmosphere study [2], [3], plasma diagnostics [4], security and surveillance [5], adaptive cruise control systems [6], biological imaging [7], and pollution monitoring and disease detection [8]. Several electronic devices may be used to build millimetre-wave and submillimetre-wave sources. These include impact avalanche transit-time (IMPATT) diodes [9], [10], Gunn diodes [10], [11], tunnel injection transit-time (TUNNETT) diodes [12], [13], heterojunction bipolar transistors (HBT) [14], [15], high electron mobility transistors (HEMT) [16], [17], Schottky diode multiplier chains [18], [19] and resonant tunnelling diodes (RTD) [20], [21]. Fig. 1.1 summarises published RF power levels from the devices mentioned above. As can be seen, besides TUNNETT diodes, Schottky multiplier diode chains and RTDs are two of the sources that can provide RF signals above 500 GHz. The RF signals that can be achieved by Schottky diode multiplier chains range from 14.8-15.4 dBm[1] at 200 GHz [19], -2 dBm at 920 GHz [22] to -30 dBm - -25.2 dBm

[1] To express an arbitrary power P as x dBm, or vice versa, the following equations may be used: $x = 10\log_{10} P$ or $P = 10^{(x/10)}$ where P is the power in mW and x is the power ratio in dBm.

at 1.8-1.9 THz [23] and -40 dBm at 2.55 THz [24]. The multiplier chains have been broadly used in the last two decades. However, they require input signals that largely depend upon the development of solid-state sources, some of which are shown in Fig. 1.1, and power amplifiers [18]. Moreover, to date the power conversion efficiency of the input signal to the output signal is below 10% above 600 GHz [18].

Three-terminal devices, whose performance is also shown in Fig. 1.1, have higher DC-to-RF conversion efficiency compared to two-terminal devices. For example, the DC-to-RF conversion efficiency for HEMT and HBT devices was reported to be up to 36% in the Ka-band [25], [26]. However, three-terminal devices have higher phase noise values compared to two-terminal devices [27], including RTDs [28]. IMPATT diodes, Gunn diodes and TUNNETT diode based millimetre-wave sources can provide higher RF output power levels compared to three-terminal devices. IMPATT-diode based sources were reported to achieve 18.9 dBm and 8.8 dBm at 115 GHz and 285 GHz, respectively [9]. Gunn diode based sources were also reported to achieve 24.9 dBm and 5.4 dBm at 82.4 GHz and 315 GHz, respectively [29]-[31]. TUNNETT-diode based sources, on the other hand, were reported to achieve 20 dBm and 10 dBm at 100 GHz and 200 GHz, respectively [13]. According to published results on Gunn diodes, IMPATT diodes and TUNNETT diode based sources, the DC-to-RF conversion efficiency is normally below 3% [13], [32]. To date, the highest operating frequencies for the HBT,

HEMT, IMPATT diode, TUNNETT diode and Gunn diodes based sources are 311 GHz, 480 GHz, 394 GHz, 706 GHz and 480 GHz, respectively [15], [16], [33]-[35].

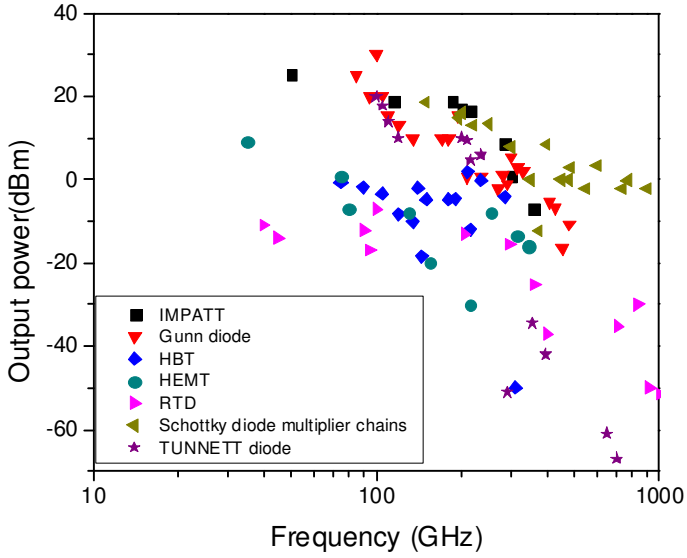

Figure 1.1: Published state-of-the-art RF power levels for IMPATT diodes, Gunn diodes, HBTs, HEMTs, RTDs, Schottky diode multiplier chains and TUNNETT diodes in the frequency range of 10 – 1000 GHz [9]-[38].

RTD based sources can also provide RF power above 500 GHz. Fundamental oscillations at 712 GHz from an RTD oscillator were demonstrated by Brown and co-workers in 1991 [21]. Recently, fundamental frequency oscillations of an RTD oscillator close to (831 GHz, 915 GHz) and above a terahertz (1.04 THz) at room temperature were reported by Asada and co-workers [36], [37]-[39]. Compared to Schottky diode multiplier chains which require RF input signals, RTDs only require a DC source to produce an RF output signal. The DC power consump-

tion of RTDs is extremely low ($\backsim$1.2 mW [40]) compared, for instance, to that of Gunn diodes ($\backsim$5 W [6] but is considerably less for submillimetre-wave operation), IMPATT diodes or TUNNETT diodes. The DC-to-RF conversion efficiency for Gunn diode oscillators is approximately 1-3% [32]. Planar Gunn diodes [41] have lower DC consumption of about 70 mW but with still very poor DC-to-RF conversion efficiency ($\sim$ 0.3%) and are therefore limited by Joule heating. An excellent review by Eisele of the state of the art and future of electronic sources at terahertz frequencies is provided in Ref. [42].

RTD oscillators are the only solid state oscillators to have demonstrated room temperature oscillations above 500 GHz. The theoretical DC-to-RF device conversion efficiencies of RTDs, which can be estimated from the I-V characteristic ($P_{max} = 3\Delta I \Delta V/16$ and $P_{DC} = I_{DC}V_{DC}$)[2], can reach as high as 20% [40]. However, DC-to-RF conversion efficiency of published millimetre-wave or terahertz RTD oscillators is less than 1% [32]. The low efficiency is attributed to parasitic bias oscillations and inefficient oscillator circuit topologies (as will be explained later in this thesis). RTDs may therefore be used to realise millimetre-wave and submillimetre-wave sources if the known problems of parasitic oscillations and low output power (which is also related to inefficient oscillator topologies) can be solved.

A two-terminal device with terminal DC electrical characteristics similar to an

[2] ΔV and ΔI are the peak-to-valley voltage and current differences, respectively. P_{max} is the theoretical maximum RF output power for a single RTD oscillator [100] and will be derived and discussed in chapter 8 on output power analysis. I_{DC} and V_{DC} are the RTD bias current and voltage, while P_{DC} is the DC power consumption.

RTD is the Esaki tunnel diode [43]. Both the tunnel diode and the RTD exhibit a negative differential resistance (NDR) region in their I-V characteristics, but RTDs are faster devices because of the faster tunnelling process that causes the NDR region and so have a much larger bandwidth. The NDR region in both device types is the reason they are well-suited to oscillator realisation. The electrical circuit design challenges such as parasitic oscillations and low oscillator output power limitations are common to both device types [44], [45], [46]. Therefore circuit concepts developed for tunnel diodes are applicable to RTDs so long as suitable circuit implementation technologies are used (suitable for the frequency of operation). Unlike RTDs, packaged tunnel diodes are commercially available and so can be used for prototyping oscillator circuits in hybrid form at low frequency to demonstrate new circuit concepts that could be applicable to RTDs.

The approach of using tunnel diodes to assess the potential of RTD circuits has been used by previous researchers [45], [46]. It is best suited only for prototyping planar RTD integrated oscillators, but clearly not for (rectangular) waveguide RTD oscillators due to the similar and dissimilar circuit implementations, respectively. Also, at high frequencies accurate modelling of the RTD to account especially for parasitic effects would be required. As will be described in subsequent chapters, many of the circuit concepts developed on this project were implemented using tunnel diodes. A brief description of the principle of operation of the tunnel diode and the resonant tunnelling diode is provided in the next sub-section.

1.1 Review of tunnel diode and RTD theory

1.1.1 Esaki Tunnel diodes [43], [46] - [49]

Tsu and Esaki [43] first proposed the resonant tunnelling structure. Heavily doped p-type and n-type semiconductors are used to build tunnel diodes. A p-type semiconductor is doped with acceptor impurities and an n-type semiconductor is doped with donor impurities. The Fermi-level (energy level where the probability of an available state being occupied by an electron is equal to 50 percent) of the intrinsic semiconductor is at the centre of the band gap [46]. However, for the doped semiconductors, the Fermi-level moves towards the valence band edge with increasing acceptor concentration or moves towards to the conduction band edge with increasing donor concentration [46]-[48].

A cross section of a tunnel diode is shown in Fig. 1.2(a), which is a p-n junction structure made of heavily doped semiconductors (carrier concentrations of 10^{19} per cm^3 to 10^{20} per cm^3) [47], [49]. The n-type semiconductor contains so many donor impurities that all of the states near the bottom of the conduction band are occupied by electrons so that the Fermi-level moves up into the conduction band instead of being located in the band gap (right side of Fig. 1.2). On the other hand, the p-type semiconductor contains so many acceptor impurities that all of the states near the top of the valence band are emptied of electrons so that the Fermi-level moves into the valence band instead of being located in the band gap (left side of Fig. 1.2).

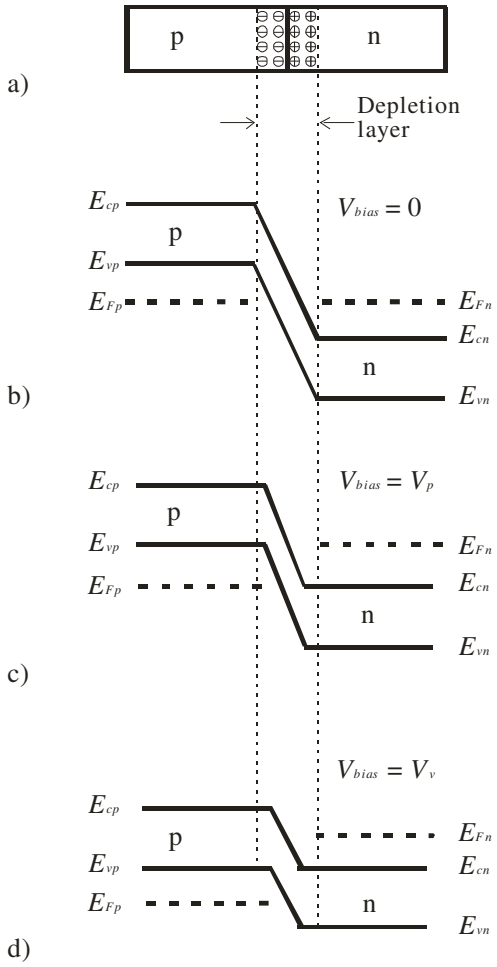

Figure 1.2: Cross-section of a tunnel diode and the corresponding band diagram. E_{cp}, E_{vp} and E_{Fp} are the conduction band, valence band and Fermi-level of the p-type semiconductor, respectively, and E_{cn}, E_{vn} and E_{Fn} are the conduction band, valence band and Fermi-level of the n-type semiconductor, respectively, and V_{bias} is the forward bias voltage. a) The cross-section of a tunnel diode, b) band diagram without forward bias $V_{bias} = 0$, c) band diagram with forward bias at peak voltage $V_{bias} = V_p$, d) band diagram with forward bias at valley voltage $V_{bias} = V_v$. [46], [48].

With no applied forward bias, no current flows through the junction (Fig. 1.2(b)). Then if a small forward (positive on the p-type semiconductor) bias is applied, it causes a large number of the electrons at the bottom of the conduction band of the n-type semiconductor to tunnel through to the top of the valence band of the p-type semiconductor. With increasing forward bias, a larger forward current flows through the junction because the overlap between the region between the Fermi-level and valence band of p-type semiconductor (E_{Fp} and E_{vp}) and the region between the Fermi-level and conduction band of n-type semiconductor(E_{Fn} and E_{cn}) increase. When the forward bias reaches the peak voltage (V_p) which means the overlap reaches maximum, the tunnelling current reaches its peak current I_p (Fig. 1.2(c)). When the forward voltage is further increased, there are fewer available unoccupied states in the p-type semiconductor. Therefore the current decreases with the increasing forward bias and negative differential resistance (NDR) region is produced. When the forward bias reaches the valley voltage (V_v), the bands are almost "uncrossed" and there are almost no unoccupied states in the p-type semiconductor available for tunnelling. Therefore, the tunnelling current reaches its valley current I_v (Fig. 1.2(d)). With still further increase of the voltage the normal thermal current will flow [46], [48]. Fig. 1.3 shows a typical current-voltage (I-V)characteristic of tunnel diode with forward bias. The depletion layer introduces a junction depletion capacitance, which is bias dependent

and it is given by [49]

$$\frac{1}{C_n^2} = \frac{2(V_{bi} - V_j - 2V_T)}{A^2 q \varepsilon_r n^*} \tag{1.1}$$

where C_n is the junction capacitance of tunnel diode, V_{bi} is the built-in potential voltage, V_j is the voltage across the p-n junction, V_T is the thermal voltage, A is junction area, q is the elementary charge and ε_r is the relative permittivity of the material used to form the tunnel diode. The n^* is the effective carrier concentration [50], [51].

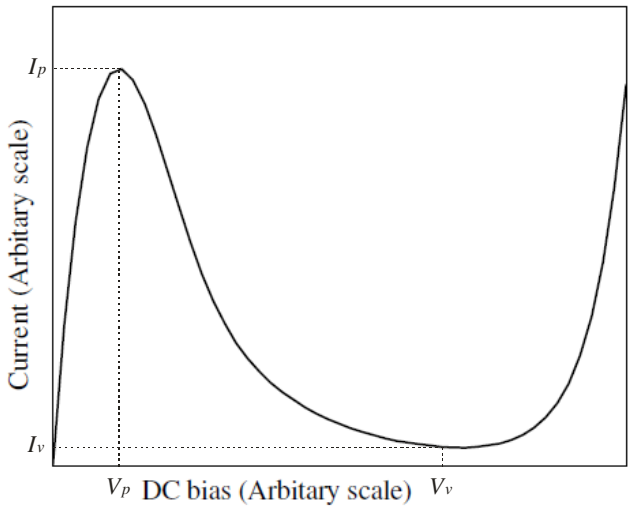

Figure 1.3: Typical current-voltage characteristic of a tunnel diode [46].

1.1.2 Resonant tunnelling diodes [46], [52]

A resonant tunnelling diode (RTD) consists of three parts: 1) an emitter region, which is the source of electrons, 2) a double-barrier quantum-well (DBQW) structure which consists of a low band-gap quantum-well material sandwiched between two barriers of high band-gap material, 3) a collector region to collect the electrons tunnelling through the double-barrier structure. The emitter and collector regions are made of heavily doped n-type semiconductors. The cross-section and the corresponding conduction band diagram of an RTD are given in Fig. 1.4. The double-barrier structure is designed such that resonant energy levels are present in the quantum-well. Electrons from the emitter can tunnel through the barriers if their longitudinal energy is equal to one of the resonant energy levels in the quantum-well.

As shown in the band diagram of Fig. 1.4, if the forward bias (positive on the collector) is zero, there is no current because the electrons from the emitter cannot quantum mechanically tunnel through the double-barriers structure (Fig. 1.4(b)). When the forward applied bias is small, electrons from the emitter form an accumulation layer near the barrier and a small fraction of electrons reach the first resonant energy level and then can tunnel through the double-barriers structure, leading to a small current. As the voltage increases, the first resonant energy level (E_1) of the quantum-well is moved downwards to the Fermi level of the emitter (E_{FE}). A great number of electrons from the emitter can tunnel

through the double-barriers structure into the collector, which leads to an increasing current with the forward bias. This continues until the maximum current I_p is reached when the first resonant energy level reaches (E_1) the bottom of the conduction band of emitter (E_{cE}) which means that the overlap between the region of incident electrons from the emitter and the first resonant level region reaches a maximum (Fig. 1.4(c)). When a larger voltage is applied, fewer electrons from the emitter can go across the double barriers and the diode current rapidly drops and a negative differential resistance (NDR) region is produced. For even larger applied voltages, thermal emission over the barrier and tunnelling through the non-resonant energy levels of the well become important and the diode current rises rapidly (Figure 1.4(d)).

Since the double barrier structure is an undoped region sandwiched between two heavily doped regions, the device capacitance can be given approximately by

$$C_n = \frac{A\varepsilon_0\varepsilon_r}{d} \tag{1.2}$$

where, ε_0 is the permittivity of free space, ε_r is the relative permittivity of the barrier and well materials, A is the area of the device and d is the width of the double barriers quantum well structure, i.e. consists of the width of the barrier layers, the quantum well and any spacer layers [53]. Unlike the tunnel diode junction capacitance which varies with bias, the RTD capacitance is largely bias independent.

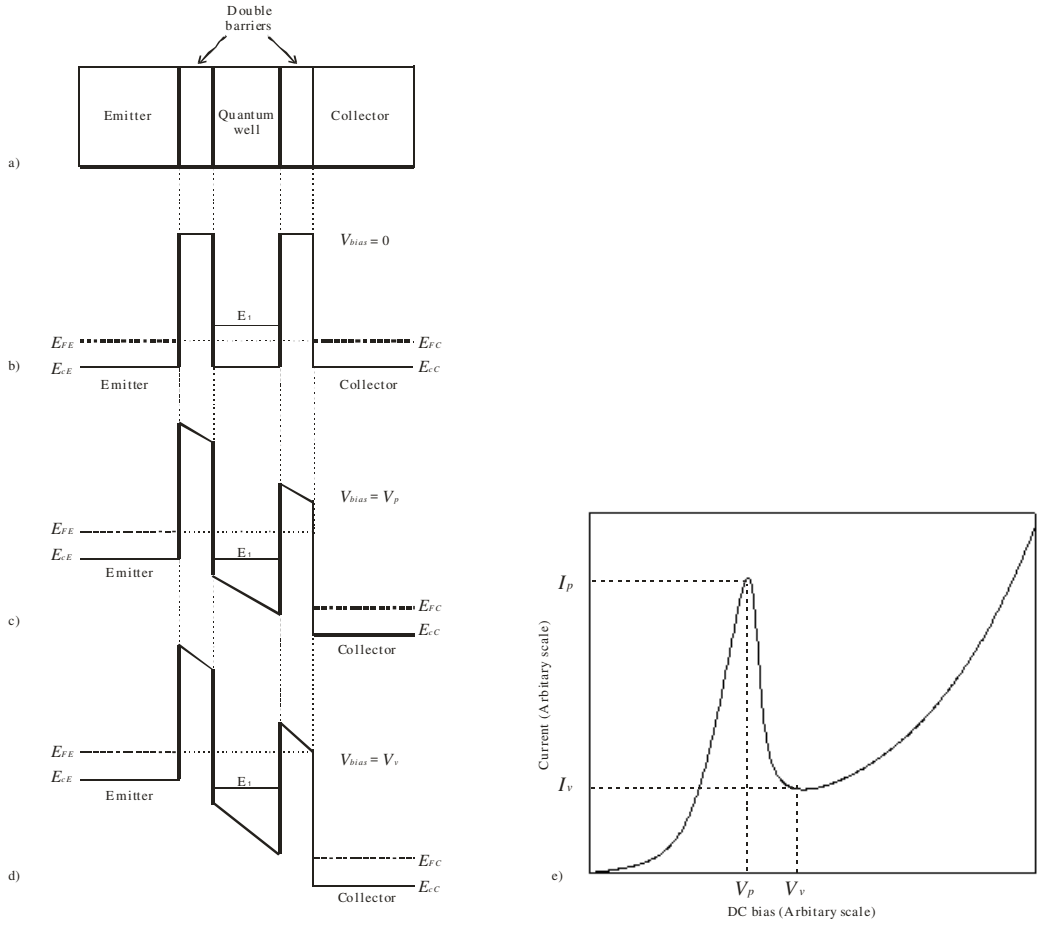

Figure 1.4: A cross-section of a resonant tunnelling diode and the corresponding conduction band diagram under forward bias, and the corresponding I-V curve. E_{cE} and E_{FE} are the conduction band and Fermi-level of the emitter, respectively, and E_{cC} and E_{FC} are the conduction band and Fermi-level of the collector, respectively, and V_{bias} is the forward bias voltage. a) The cross-section of a resonant tunnelling diode, b) conduction band diagram without forward bias $V_{bias} = 0$, c) conduction band diagram with forward bias at peak voltage $V_{bias} = V_p$, d) conduction band diagram with forward bias at valley voltage $V_{bias} = V_v$. e) Typical current-voltage characteristic of a tunnel diode [46], [52].

1.2 NDR device characterisation and NDR oscillator circuits

1.2.1 DC (in)stability and equivalent circuit modelling

Accurate DC characterisation of the negative differential resistance (NDR) region of tunnel diodes or RTDs is often hindered by parasitic oscillations in the bias circuit making it difficult to determine the static characteristics of these devices in this very critical region [54]-[57] correctly. A common method to solve the bias instability problem is to employ a stabilising resistor connected directly across the tunnelling diode [46], [58]-[60]. The stabilising resistor is chosen such that the combined resistance (at DC and low frequencies) is positive when the tunnelling diode is biased in the NDR region. The diode characteristic is then determined indirectly. Another previously proposed method uses a large capacitor connected across the device [61], but the inductance of the interconnect between the capacitor and the tunnel diode must be kept very low for this to work [63]. The former method yields accurate results so long as the stabilising resistance value suppresses all oscillations in the circuit. This shunt resistor stabilisation method is to date the most accurate and robust method for DC characterisation of tunnel diodes. It is, however, known that either too large or too small a shunt resistor cannot suppress oscillations effectively [58], [60], [64], [65] and the oscillations present in the bias circuit modify the measured characteristics of the NDR region. Therefore as method to resolve this uncertainty and enable robust characterisation of the entire NDR region is desirable.

An RF model for RTDs is also required for circuit design, especially for high frequency analogue circuits such as submillimetre-wave oscillators. A few direct RF measurements have been reported from which the device equivalent circuit elements can be extracted, but these have been performed under very restricted bias conditions [66], [67], [68] or for small size devices for which the circuit was stable under measurement conditions. This is possible for some parts of the NDR region [70], [71] or the entire NDR region when the magnitude of the effective diode negative differential conductance is smaller than the conductance of the measurement set-up (which is usually 0.02 S) [62], [69]. Note that small area RTDs (corresponding to a negative differential resistance of say -100 Ω) exhibit DC stability and so have no problem of low-frequency bias oscillations. DC stability is easily achieved here because of the sufficiently small negative conductance in small area devices (approx. $1\,\mu m^2$) [62]. However, because of the small size of the RTDs the output power of oscillators employing these is limited [63], [72].

For larger NDR devices, more robust characterisation techniques are required. One such technique uses an RTD in parallel with a resistor for circuit stability (similar to the technique for DC stabilisation), with this setup being characterised with s-parameter measurements [73]. The RTD small-signal equivalent model was fitted to the measured data to determine the individual element values. In this method, errors will occur in determining and de-embedding the stabilising resistance at high frequencies and this limits the modelling accuracy. Clearly

more robust methods for both DC and RF characterisation of tunnel diodes and RTDs are required. Some new characterisation methods will be described in this thesis.

1.2.2 Parasitic bias oscillations and low oscillator output power

This section summarises the methods previously used to realise RTD oscillators. The problems/limitations of each of the approaches are highlighted, and details of how each of these problems are solved will be described in the thesis. Due to the existence of a negative differential resistance (NDR) in the device current-voltage (I-V) characteristic which can extend from DC to terahertz (THz) frequencies, the RTD has been carefully analysed and employed in several high frequency applications. Trigger circuits employing fast switching have been realised up to 110 GHz [74] and waveguide oscillators were realised up to 712 GHz [21], [75]. However, the output power levels at high frequency (millimetre-wave) were all low. For example, RF power of -15.5 dBm (28 μW) was measured at 290 GHz [76], and the highest power of -7 dBm (200 μW) at 100 GHz and at 443 GHz, respectively [77], [78]. The efficiency of these oscillators was below 1%. The reasons for the very low output power of the RTD-based oscillators include the low-frequency parasitic bias oscillations [79] and/or the inefficient oscillator circuit topologies employed as will be explained in this thesis.

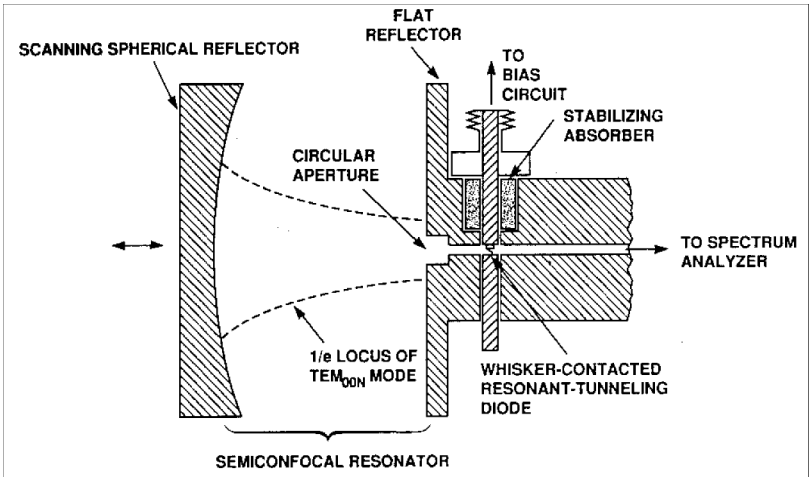

Figure 1.5: Schematic cross-sectional diagram of a quasioptical waveguide resonant tunnelling diode oscillator, after [40].

1.2.2.1 Waveguide RTD oscillators

RTD oscillators have been implemented in either waveguide technology in planar technology. Waveguide RTD oscillators have employed a lossy transmission line section along the DC bias line to minimise the parasitic oscillations [40], [80]. Fig. 1.5 shows the schematic diagram of a quasi-optical oscillator designed for the 100 GHz region. The RTD is mounted in a in a rectangular waveguide (WR-6) that opens abruptly to a round diameter coupling hole within the middle of a flat metallic plate. This plate forms one reflector of a semiconfocal open resonator. The waveguide portion of the oscillator is typical of RTD waveguide oscillators. The diode is dc biased by a coaxial circuit that suppresses spurious oscillations by means of a very lossy section of transmission line placed in close proximity to

the diode chip. The lossy material is an iron-loaded epoxy. Waveguide oscillators achieve efficiencies of approx. 1.6% well below the theoretical predictions. The lossy line diminishes the signal level of parasitic oscillations so that they do not significantly interfere with the main oscillations, but the presence of bias oscillations means that there is less power available from the device for conversion into an RF signal. This RTD oscillator implementation is limited by the inductance of gold bond wire (whisker) required to connect the device in the circuit. A detailed analysis of this circuit is described in chapter 8.

1.2.2.2 Planar RTD oscillators

Planar RTD oscillators, on the other hand, eliminate parasitic bias oscillations in an oscillator circuit by employing a shunt resistor to the NDR device [81], [82]. A non-linear (diode) resistor [81] was first used instead of a linear resistor to reduce the DC power consumption of the stabilizing resistor. Later on Schottky diodes [82], [83] were employed for the same purpose. Fig. 5.14 shows the schematic diagram of a planar RTD oscillator in which S_d and R_e are a Schottky diode and a resistance, respectively, and form the stabilising resistance. C_e is a decoupling capacitor (is an RF short circuit), while "TML" is said to be quarter-wave transmission line. The decoupling circuit at the other end of the "quarter-wave" transmission line, consisting of Schottky diodes, resistor and a capacitor behaves as a RF short circuit at the oscillation frequency. This "quarter-wave" long trans-

mission line presents an open circuit to the RTD oscillator circuit at the oscillation frequency. Even though impressive experimental results, mainly with regards to frequency, were achieved by this approach, it will be shown in this thesis that the "quarter-wave" transmission line in fact does not act as a RF open circuit but together with the RTD capacitance and any resonator used combine to determine the frequency of the oscillation. As a consequence the oscillator would operate at a different (lower) oscillation frequency and so the "quarter-wave" line will no longer be quarter-wavelength long but would act as a short stub (inductor). The output power of such an oscillator would also be lower since any impedance matching at the design frequency would no longer be valid at the actual oscillation frequency.

At millimetre-wave and low terahertz frequencies ($<$ 1 THz), planar RTD oscillators have been integrated in slot antennas [83], [36]. The RTD devices are usually integrated at the centre of the slot antenna, a location at which the antenna input impedance is infinity! Therefore the device is mismatched with the antenna load and so the oscillator efficiencies have remained low, under 1%. In recognition of this problem, recent work has used devices offset from the slot antenna centre with improved results [78].

In order to increase the output power of planar RTD oscillators, both Professor Mark Rodwell's group at University of California, Santa Barbara, and Professor Masahiro Asada's group at Tokyo Institute of Technology proposed RTD oscilla-

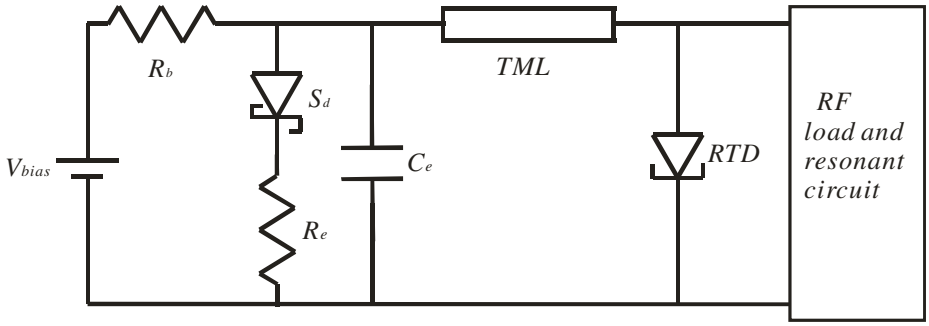

Figure 1.6: Reddy's bias stabilization scheme for sub-mm-wave RTD oscillators. R_b is the resistance of the bias line. S_d, R_e and C_e are the Schottky diode, external resistor and external capacitor, respectively, which form the stabilising circuit. TML is the quarter-wave length transmission line at the oscillation frequency [83].

tor arrays [76], [84]. In their approaches, a single RTD oscillator each employing a single device is loaded by slot antenna and the radiated power from the individual oscillators combines in space. Mutual coupling between the individual oscillators is employed to achieve coherent oscillation. A shunt resistor [84] or Schottky stabiliser (non-linear resistor) [76] is used to suppress low-frequency bias circuit oscillations in each individual oscillator of the array. Very high oscillation frequencies is up to 650 GHz were achieved using this approach, however, the output power is still low and the highest output power was -15.5 dBm (28 $\boldsymbol{\mu}$ W) at 290 GHz [76]; Recently, Suzuki et al achieved the highest output power around -7 dBm (200 $\boldsymbol{\mu}$ W) at 443 GHz [78]. At the moment, there is no procedure for placing the oscillators geometrically to achieve power combining in a given direction. Even if such a procedure were in place, the locations of individual oscillators

might be such that the required mutual coupling between neighbouring oscillators to achieve coherent oscillation would be compromised. This spatial power combining technique is also limited in applicability, for instance if a mixer stage is to be driven by an RTD oscillator (requiring higher power than a single device can provide) this would not be possible. Also, because of the many antennas required (one for each individual oscillator in the array) the size of the required circuit is large (the slot length of a slot antenna is approximately half a wavelength which corresponds to about 580 on semi-insulating (SI) indium phosphide (InP) substrate at 100 GHz). Therefore this technique has only been applicable to terahertz (>500GHz) frequencies at which the antenna size is small enough to allow integration of many RTD oscillators.

Another example of an inefficient planar RTD oscillator topology is the 50 GHz RTD oscillator circuit described in Reference [85] where the RF power is taken across the DC stabilising resistor. The circuit used is similar to that described above in Fig. 1.6, but with no Schottky diode S_d i.e. a linear resistor R_e is used for stabilisation. The circuit also has no decoupling capacitor C_e and no explicit RF load or resonant circuit. In their circuit, the stabilising resistor R_e was 5 Ω, which also acted as the load resistance. With the generated RF power being taken across the stabilising resistance, large losses occur due to impedance mismatch to a 50 Ω load.

1.2.2.3 Quasi-optical power combining

Another technique that has been attempted to improve the radiated power of RTD oscillators is power combining in a quasi-optical resonator [86]. A Fabry-Perot resonator with a metallic grating mounted with an array of RTDs is used as a quasi-optical power combiner at millimetre and sub-millimetre wave frequency regions. Figure 1.7 shows the configuration of the resonator. The resonator consists of a concave output mirror and a grating (grooved mirror) with RTDs. In the experimental demonstration described in Ref. [86], two RTDs in parallel were fed a bias by a single DC supply. Each diode was mounted in the groove and contacted with a whisker antenna. The backshort was insulated by a Teflon sheet to feed a bias current to the diodes. A tapered structure at front of the grooved mirror was introduced to improve impedance matching between the groove circuit and free space. The output power of the oscillator with two RTD's increased by about 6 dB compared to that with single RTD, but at -64 dBm ($\sim 0.4\,nW!$) for 2 diodes this is extremely low output power. The circuit configuration does not provide opportunities for eliminating bias oscillations, and as such this approach has not received much attention.

1.2.2.4 Series or parallel device integration

Further attempts have been made to increase the tunnel diode or RTD oscillator output power at circuit level. These include series-connected tunnel diodes

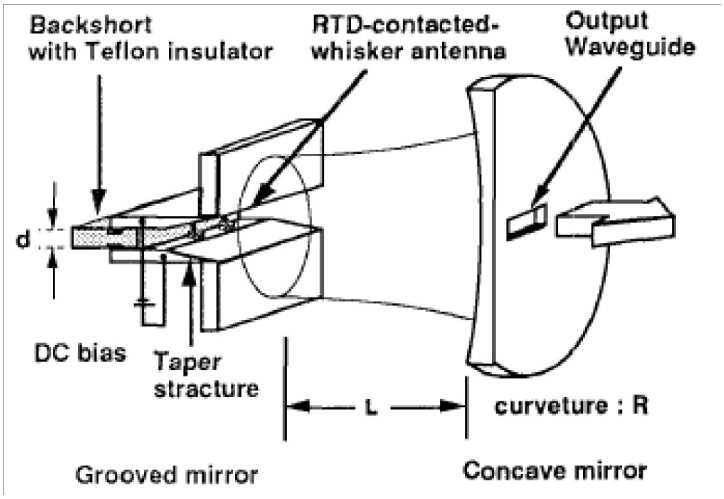

Figure 1.7: Configuration for RTD power combining in a quasi-optical resonator, after [86].

[44], [45] or parallel-connected RTDs [87], [88] in oscillator circuits. For the former design, the main problem is DC instability whereby it is not possible to simultaneously bias the tunnel diodes or RTDs in their NDR regions. Previously proposed solutions to this biasing problem include fast electric pulse excitation [89] and RF excitation [44], [45], but both techniques are involving and only RF excitation has been experimentally validated for two tunnel diodes [45]. Due to the lack of suitable trigger sources, pulse excitation has, to date, not yet been experimentally demonstrated. On the other hand, for parallel-connected devices the problem of low-frequency parasitic oscillations is exacerbated. The peak current of parallel-connected tunnel diodes or RTDs is higher and so the effective negative differential resistance of the parallel-connected devices is small making

it more difficult to suppress the low-frequency parasitic oscillations (this will be discussed in chapter 5). The small negative differential resistance can also cause circuit bistability if its value is smaller than the series resistance of the bias line [79]. Therefore this design approach is also hardly used. Common RTD oscillator design and implementation methods are therefore far from optimal with the target frequency often not achieved [82] and the output power is very low [28].

1.2.2.5 Power combining for other two terminal devices

The problem of limited output power at millimetre-wave and THz frequencies is not limited to RTD oscillators. Other solid-state two terminal devices such as Gunn diodes or IMPATT diodes have also required the development of a variety of combining techniques. One such technique with demonstrated success was described by Rucker [90] and later analysed by Kurokawa [91]. This technique has a number of coaxial transmission lines, each approximately one-quarter-wavelength long, terminated by a device and arranged radially about a common bias network and a common output network. Even though the devices are located physically far apart from each other, the behaviour of the oscillator becomes identical to that of an oscillator with parallel connected devices. Another technique employed for other solid-state two terminal devices is using waveguide cap resonators [92]. It was shown that power addition of three individual active devices (GaAs IMPATT diodes) under a common resonant cap was possible. Despite these techniques be-

ing known for many years now, to the best of the author's knowledge there have been no reported RTD circuit implementations using them. They are however included in this thesis for completeness.

1.3 Project aims and thesis layout

According to the discussion above, the main challenges for this project are building an equivalent circuit model for a tunnel diode or RTD and developing an oscillator design approach which can achieve high output power using either of these devices. This thesis is organised in nine chapters. The next chapter discusses the Van der Pol oscillator model, the basis for predicting oscillations in tunnel diode or RTD circuits. The next chapter also establishes the required circuit conditions for the DC characterisation of the tunnel diodes/RTDs employing the widely employed shunt resistor stabilisation method. It is shown that, high frequency oscillations can exist in the bias circuit (depending on the circuit elements) and if present these oscillations also modify the measured I-V characteristics. This problem is analysed using the Van der Pol oscillator model, and on this basis I-V measurement circuits can be designed to be free from both low frequency *bias* oscillations and high frequency *parasitic* oscillations[3] [93]. In addition, a direct I-V measurement approach which utilises the stabilisation resistor in series with a capacitor is proposed. Experimental results show that I-V char-

[3]Low frequency bias oscillations are determined by the whole circuit including the bias network, while high frequency oscillations are determined by only a section of the circuit usually excluding the bias network. This will be explained in detail in chapter 3.

acterisation of tunnel diodes in the NDR region can now be performed free from oscillations. These results are described in chapter 3.

Chapter 4 describes a new measurement set-up suitable for RF characterisation of NDR devices over the entire NDR region. As will be detailed in that chapter, the measurement results for the NDR device are independent of the set-up used to achieve circuit stability. First measurement results on a packaged tunnel diode indicate that accurate characterisation and subsequent small-signal equivalent circuit model extraction for the NDR region can be done. It is worthy already noting here that following the publication of this technique [94], it has now also been successfully applied to the characterisation of RTDs [95] and thereby also demonstrating the close similarity between tunnel diodes and RTDs.

Having described the DC and RF characterisation techniques of tunnelling devices in previous chapters, oscillator design with these devices will be discussed in chapters 5 and 6. In chapter 5, a new multiple device power combining circuit topology, incorporating a new design methodology for the DC bias decoupling circuit, will be described [96]. The oscillator is designed specifically for sinusoidal oscillations by proper choice of the inductance to resonate the tunnel diode capacitance (based on the Van der Pol model of the circuit). The oscillator topology uses parallel resonance but with each tunnel diode individually biased and DC-decoupled making it possible to employ several tunnel diodes in a single oscillator circuit for higher output power. This approach seems to eliminate parasitic bias

oscillations. Simulation and experimental oscillator results are in good agreement, with a two-tunnel diodes oscillator exhibiting approximately double the output power as compared to that of a single tunnel diode oscillator. Chapter 6, on the other hand, explores the potential of series integration of NDR devices. A simple way to suppress DC instability of the NDR devices connected in series with all the devices biased in their NDR regions is proposed and experimentally validated using tunnel diodes.

The design and fabrication processes for monolithic RTD oscillators will be discussed in chapter 7. Monolithic RTD oscillators were successfully fabricated and they operated at the designed fundamental frequency. In chapter 8, output power analysis of an optimal RTD oscillator topology is carried out. One this basis, predictions on the output power and device size of RTD oscillators/devices in various material systems/designs can be made. The chapter also critically reviews the waveguide RTD oscillator configuration as well as a planar RTD oscillator topology in which the RF power is taken across the stabilising resistor.

CHAPTER 2

VAN DER POL OSCILLATOR ANALYSIS

2.1 Introduction

In this chapter, the basic differential equation for a typical tunnel diode circuit will be derived. The equation is found to be similar to the Van der Pol equation in the general case (and reduces to the Van der Pol equation for special circuit conditions), which is a widely understood equation for describing non-linear oscillatory processes [97]. As will be indicated here and shown in subsequent chapters, the Van der Pol oscillator model forms the foundation for the reliable design of stable DC test fixtures and NDR-based oscillators. This chapter also establishes circuit stability conditions for a typical tunnel diode circuit from small-signal analysis.

2.2 Van der Pol oscillator theory

The Van der Pol oscillator which was proposed by Balthasar van der Pol in 1920 is an oscillator model with nonlinear damping governed by the second-order differential equation as shown in equation (2.1) [97], [98]

$$\frac{d^2x}{dt^2} - \varepsilon(1 - x^2)\frac{dx}{dt} + x = 0 \tag{2.1}$$

where x is the dynamical variable and the waveform of x versus t depends on the value of the parameter ε.

If the value of ε is very small ($\varepsilon << 1$) the solution to equation (2.1) is sinusoidal as shown in Fig. 2.1(a) and if the value of ε is large ($\varepsilon > 1$) the solution is a square-like (switching) waveform as shown in Fig. 2.1(b) [98]. The simulation results in Fig. 2.1 and Fig. 2.2 were generated by programming equation (2.1) in a mathematical software tool, MATLAB [99].

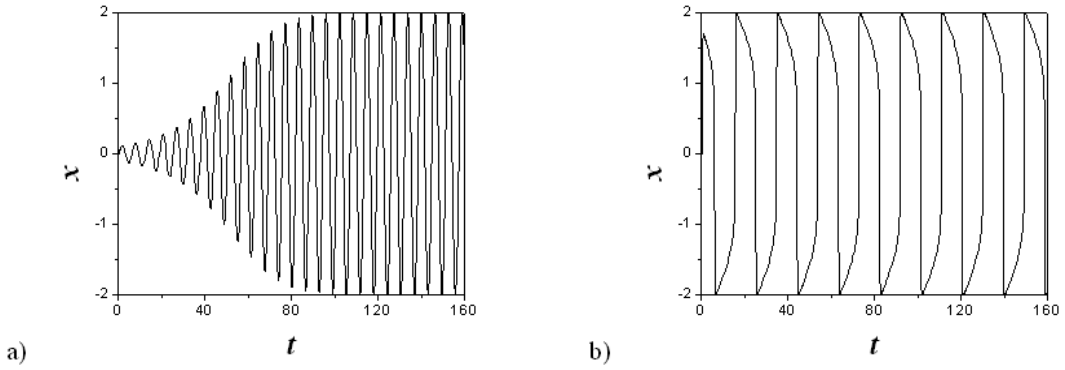

Figure 2.1: Solutions to the Van der Pol equation (2.1) for positive values of ε. (a) Oscillation waveform with $\varepsilon = 0.1$, (b) Oscillation waveform with $\varepsilon = 10$.

For conventional Van der Pol analysis, the constant ε is usually positive. For applications in which no oscillations are desired ε should not be positive. In this case, negative values of ε should be chosen because oscillations are not sustained as illustrated by simulation results in Fig. 2.2(a and b). The simulation results for $\varepsilon = -0.1$ and $\varepsilon = -0.5$ in Fig. 2.2 show that large negative ε results in faster damping.

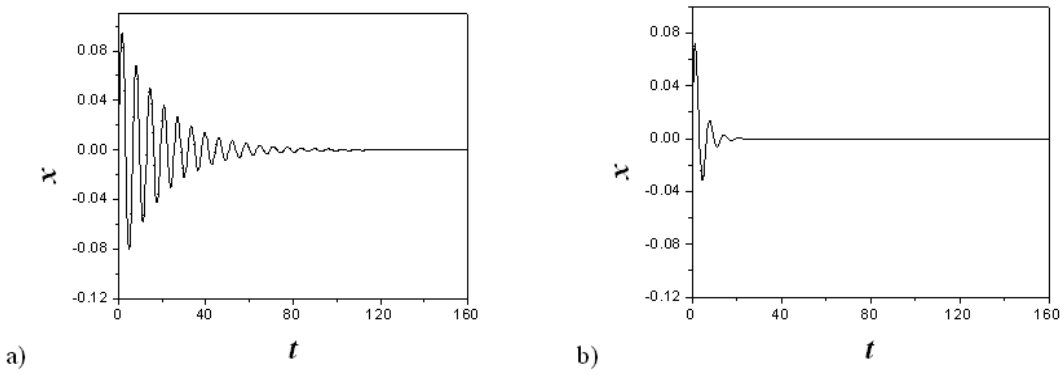

Figure 2.2: Solutions to the Van der Pol equation (2.1) for negative values of ε. (a) Oscillation waveform with ε = -0.1, (b) Oscillation waveform with ε = -0.5.

2.3 Negative differential resistance based Van der Pol oscillator

Fig. 2.3(a) shows a typical NDR device such as a tunnel diode or an RTD with DC bias, and Fig. 2.3(b) shows the NDR device modelled as a voltage controlled current source, $I(V)$: I_p and I_v are the peak current and valley current, respectively; V_p and V_v are the bias voltages when the device reaches the peak current I_p and valley current I_v, respectively; and ΔV and ΔI are the peak to valley voltage and current differences, respectively. R_b is the resistance of the DC supply and the bias line, L_b is the bias line inductance, and Q_n the charge at the junction of the device (tunnel diode) when it is biased in the NDR region. In a small-signal model, the voltage controlled current source $I(V)$ is replaced by a small-signal negative conductance, -G_n, while the charge Q_n by a capacitance C_n. The bias dependent small signal model for the 1N3717 tunnel diode used in this work is described in detail in Chapter 4 and any of the assumptions made

on model elements within an oscillator setup is on the basis of these experimental results and the datasheet of the device (Appendix D). Some element values to bear in mind at this stage include the inductance of the diode leads ($\backsim$1.6 pH), series resistance of the diode ($\backsim$ 1Ω), and variation of the diode capacitance with bias (varies between 12 - 14 pF in the NDR region). The device datasheet gives the diode capacitance as 25 pF, a value that may have been extracted from a device biased the second positive differential resistance (PDR) region of the I-V characteristics as the experimental results in chapter 4 suggest.

Fig. 2.4(a) shows the small-signal RF equivalent circuit of Fig. 2.3(a) (R_b ($\backsim$1 Ω) and the series resistance R_s ($\backsim$1 Ω) of the device are typically small therefore they are ignored in the RF equivalent circuit[1], and the series inductance L_s ($\backsim$1.6 nH) of the device is also small compared to L_b ($\backsim$60 nH) therefore it is also ignored. Low frequency ($\backsim$100 MHz) oscillations mainly determined by L_b and the device capacitance will be present in this circuit. Fig. 2.4(b) shows the large-signal RF equivalent circuit in which the current source of the RTD is represented by a cubic polynomial. Shifting the origin of the axis to the DC bias point (middle of the NDR region) for the sake of convenience, the I-V characteristics can be represented by a cubic polynomial $I(V) = -aV + bV^3$ where a and b are both positive constants [83], [98], [100] [101]. These constants can be related to ΔV and ΔI which represent the extent of the NDR region. By equating the slope of

[1]Note that the series resistance R_s can be considered as being part of the current source *I(V)*. This is the case for the work described in this and the next chapter where the stabilising resistance is determined from estimates of the NDR region from measured "un-stabilised" I-V characteristics.

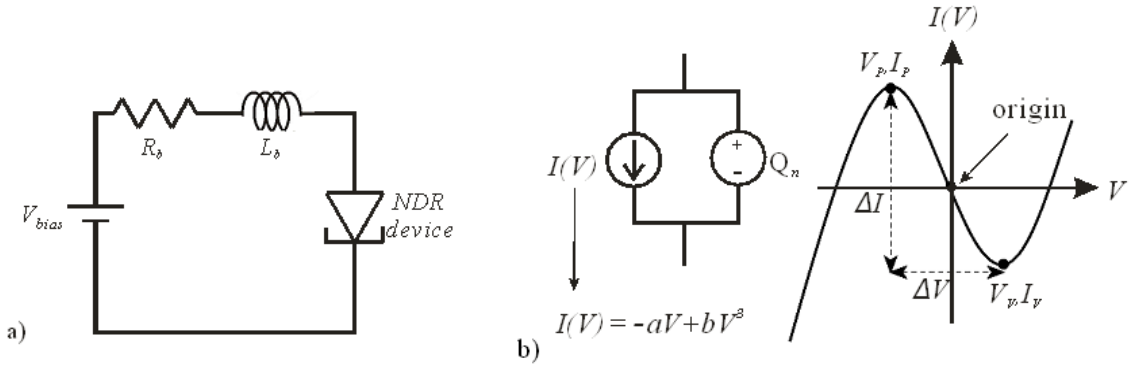

Figure 2.3: (a) A NDR device with DC bias, (b) A large-signal model for the NDR device biased in the NDR region. The voltage controlled current source $I(V)$ is modelled by a cubic polynomial. The charge an the pn junction is modelled by a charge source $Q_n\,(V)$.

the I-V curve to zero at the peak and valley points, the constants a and b can be determined to be $a = (3\Delta I)/(2\Delta V)$ and $b = (2\Delta I)/(\Delta V^3)$ [83], [98], [101]. The maximum absolute value of small-signal negative conductance G_n is obtained at the origin of the cubic polynomial and it is equal to the constant a.

The cubic model captures the main attributes of the I-V characteristics of actual devices and it has previously been employed for generic nonlinear analysis of circuits containing tunnel diodes or resonant tunnelling diodes [83], [98], [100]. For instance, the maximum RF output power when the devices are employed in oscillator circuits has been estimated using this model [100]. This approach is adopted here but with the focus on circuit stability. Note that accurate modelling of the I-V characteristic of the tunnel diode used in this work requires a 9th order polynomial (details about this in Chapter 6).

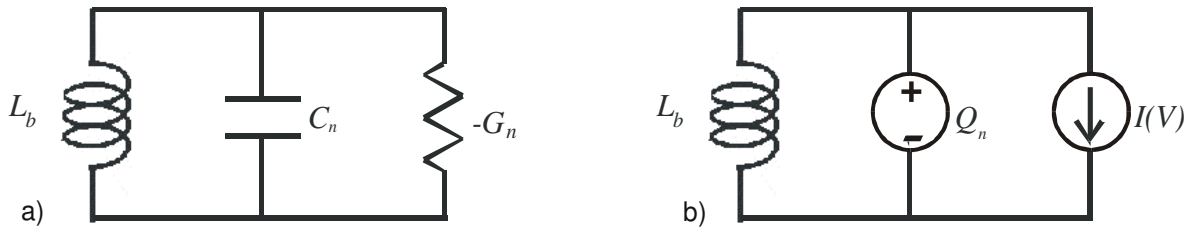

Figure 2.4: (a) A small-signal equivalent circuit of Fig.2.3(a). R_b, R_s and L_s are typically small therefore they are ignored in the RF equivalent circuit, (b) A large-signal RF equivalent circuit of Fig. 2.3(a).

When the device is biased in the NDR region using the set up of Fig.2.3(a), the circuit has oscillations present when the net resistance in the circuit is negative. Due to the large equivalent inductance L_b of the biasing cables, the oscillation frequency is usually low. In order to eliminate these bias oscillations, a shunt resistor R_e is commonly used in the oscillator circuit set up, as shown in Fig. 2.5. The inductance L models the connection between R_e and the NDR device and it includes the external inductance L_e in series with the inductance L_s introduced by the connection leads. The DC bias stability of this circuit can be determined by considering the real part of the admittance looking into the stabilising resistor R_e, i.e. Re(Y_{in}).

$$Y_{in} = \frac{1}{R_e} + [j\omega L + \frac{1}{-G_n + j\omega C_n}]^{-1} \tag{2.2}$$

and

$$\mathrm{Re}(Y_{in}) = \frac{1}{R_e} - G_n \frac{1}{(1-\omega^2 LC_n)^2 + (\omega L G_n)^2} \tag{2.3}$$

where the NDR device has been replaced by the small-signal conductance –G_n and

self capacitance C_n. If $\mathrm{Re}(Y_{in}) > 0$, the circuit will be stable [81], [82]. However, there are two cases to consider here, at DC and low frequencies and then at high frequencies. Considering the DC and low frequency case first, from equation (2.3)

$$\mathrm{Re}(Y_{in}) \approx \frac{1}{R_e} - G_n \tag{2.4}$$

Therefore for DC and low frequency stability

$$R_e < \frac{1}{G_n} \tag{2.5}$$

That is, R_e should be chosen small enough such that the combined DC characteristic of R_e in parallel with the NDR device is positive in the negative differential resistance region of the tunnel diode or RTD. This is the same condition as established in Refs.[81] and [82].

At high frequencies ($\omega \approx 1/\sqrt{LC_n}$), assuming large L_b as earlier indicated), the second term of equation (2.3) can become greater than the first term, i.e.

$$\frac{G_n}{(1-\omega^2 LC_n)^2 + (\omega L G_n)^2} > \frac{1}{R_e} \tag{2.6}$$

in which case $\mathrm{Re}(Y_{in}) < 0$ making the circuit potentially unstable. In this case, high frequency oscillations could exist in the circuit.

The DC and low frequency stability criterion derived in equation (2.5) is used to suppress the low-frequency bias line oscillations. However, there could be high frequency oscillations between the shunt resistor, the inductance L, and the NDR device as mentioned above. In this section we derive equations that

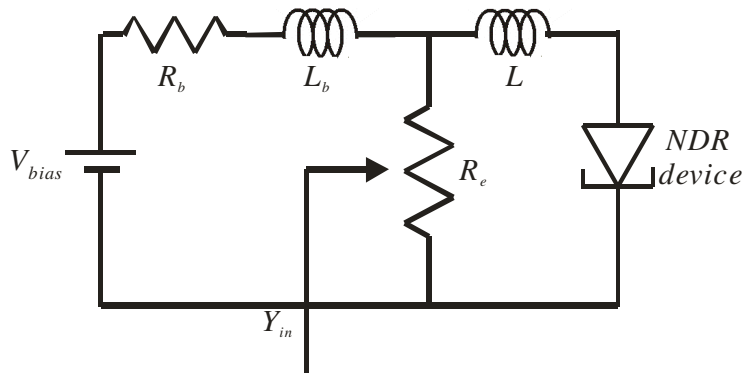

Figure 2.5: A NDR device oscillator topology with the DC decoupling circuit (R_e). R_b and L_b model the resistance and inductance of the DC power supply and the bias line, respectively. The inductance L and self-capacitance of the NDR device can lead to high frequency oscillations in the circuit.

relate R_e and L to such high frequency oscillations. Fig. 2.6 shows the RF equivalent circuit of Fig. 2.5. Here, the bias line inductance L_b is assumed large and so acts like an open circuit at the high frequencies of oscillation, decoupling the DC power supply. The RF equivalent circuit can be described by equations below according to Kirchhoff's current law where the current source is represented by a cubic polynomial as previously stated [83], [100], [101]. The variation of the junction charge Q_n with voltage (the device capacitance $C_n = dQ_n/dV$) is assumed constant in this analysis because it is for establishing conditions for no oscillations i.e. no large signal variations will be present. Any present transient oscillations will be small and will decay rapidly to zero (for a circuit designed to achieve DC stability). For the device used in experimental work, the actual

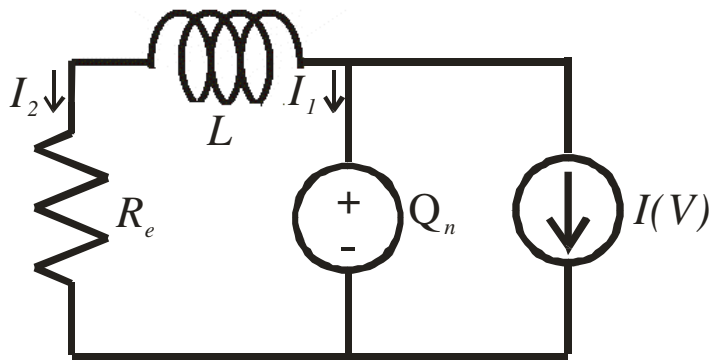

Figure 2.6: Large-signal RF equivalent circuit of Fig. 2.5. The bias line inductance L_b in Fig. 2.5 is assumed large and so decouples the RF signal from the DC supply.

variation of C_n within the NDR region is $13 \pm 1pF$ as will be shown in Chapter 4. Thus

$$I + I_1 + I_2 = 0 \tag{2.7}$$

$$I_1 = \frac{dQ_n}{dt} = \frac{dQ_n}{dV}\frac{dV}{dt} = C_n\frac{dV}{dt} \tag{2.8}$$

$$I_2 = \frac{V - L\frac{dI_2}{dt}}{R_e} \tag{2.9}$$

$$I_2 = -(I + \frac{dQ_n}{dt}) = -\left(I + C_n\frac{dV}{dt}\right) \tag{2.10}$$

where I is the current source of the NDR device, I_1 and I_2 are the currents through the capacitor of the NDR device and external decoupling circuit R_e, respectively. V is the voltage across the NDR device and L is the total inductance between the decoupling circuit and NDR device.

Combining Eqs. (2.7)-(2.10) gives

$$I + C_n \frac{dV}{dt} + (V - L\frac{dI_2}{dt})/R_e = 0 \tag{2.11}$$

By substituting the cubic polynomial $I(V) = -aV + bV^3$ into equation (2.11), it can be re-written as shown in equation (2.12) and simplified as shown in equation (2.13)

$$LC_n \frac{d^2V}{dt^2} + (C_nR_e - aL + 3bLV^2)\frac{dV}{dt} + (1 - aR_e)V + bR_eV^3 = 0 \tag{2.12}$$

$$\frac{d^2u}{d\tau^2} - \varepsilon(1 - u^2)\frac{du}{d\tau} + u + \beta u^3 = 0 \tag{2.13}$$

where $\tau = \sqrt{\frac{1-aR_e}{LC_n}}t$, $u = \sqrt{\frac{3bL}{aL-C_nR_e}}V$, $\beta = \frac{R_e(aL-C_nR_e)}{3L(1-aR_e)}$ and $\varepsilon = \frac{aL-C_nR_e}{\sqrt{LC_n(1-aR_e)}}$.

Equation (2.13) is similar to Van der Pol equation ($\beta = 0$) which is the special case of the Liénard equation, which can be used to describe simple circuits that include NDR components [102], [103]. The type of the limit cycle solution depends on ε. For a given device/circuit the waveform of the signal is determined by the value of ε:

$$\varepsilon = \frac{aL - C_nR_e}{\sqrt{LC_n(1 - aR_e)}} \tag{2.14}$$

The discussion about the value of ε in the Van der Pol second order differential equation in section 2.1 shows that if the value of ε is very small ($\varepsilon << 1$) then the solution to equation (2.13) is sinusoidal and if the value of ε is large ($\varepsilon > 1$) then the solution is a square-like (switching) waveform [98]. For negative values of ε, on the other hand, oscillations are not sustained.

It therefore means that high-frequency oscillations do not exist in the circuit if ε is chosen to be negative. From equation (2.14), this can be achieved if

$$R_e < \frac{1}{a} \tag{2.15}$$

for ε to be real, and

$$R_e > \frac{aL}{C_n} \tag{2.16}$$

Therefore the condition for stability (no oscillations in the circuit) can be expressed as

$$\frac{aL}{C_n} < R_e < \frac{1}{a} \tag{2.17}$$

2.4 Small-signal analysis

The Van der Pol approach described in the preceding section provides analysis for RF stability using a large-signal model for the diode current from which the design equation (2.17) was derived. Another approach to understanding RF stability is to do small-signal analysis. In this case, the current source as shown in Fig. 2.6 is replaced with a conductance $-G_n$, and from the admittance of the circuit the characteristic equation as a function of the complex frequency, $s = \sigma + j\omega$, is given by

$$-G_n + sC_n + \frac{1}{R_e + sL} = 0 \tag{2.18}$$

Equation (2.18) can be re-written as

$$LC_n s^2 + (C_n R_e - LG_n)s + 1 - G_n R_e = 0 \tag{2.19}$$

The solutions to the equation (2.19) are given by

$$s = \frac{(LG_n - C_nR_e) \pm \sqrt{(LG_n - C_nR_e)^2 - 4LC_n(1 - G_nR_e)}}{2LC_n} \tag{2.20}$$

Case 1: the solutions are complex and therefore

$$(LG_n - C_nR_e)^2 - 4LC_n(1 - G_nR_e) < 0 \tag{2.21}$$

Equation (2.21) can be re-written as

$$R_e < 2\sqrt{\frac{L}{C_n}} - \frac{LG_n}{C_n} \tag{2.22}$$

If the solutions to the equation (2.19) fall in the left half of the complex frequency plane, it means that the circuit is stable [60], [104]. From equation (2.20) the circuit will be stable if

$$R_e > \frac{LG_n}{C_n} \tag{2.23}$$

Combining the conditions for Case 1 as shown in Eqs. (2.22) and (2.23), the condition to achieve circuit stability becomes

$$\frac{LG_n}{C_n} < R_e < 2\sqrt{\frac{L}{C_n}} - \frac{LG_n}{C_n} \tag{2.24}$$

Case 2: the solutions are real and so

$$(LG_n - C_nR_e)^2 - 4LC_n(1 - G_nR_e) > 0 \tag{2.25}$$

Equation (2.25) can be re-written as

$$R_e > 2\sqrt{\frac{L}{C_n}} - \frac{LG_n}{C_n} \tag{2.26}$$

For these solutions to fall in the left half of the complex frequency plane, equation (2.23) should be satisfied as well as

$$(LG_n - C_nR_e) \pm \sqrt{(LG_n - C_nR_e)^2 - 4LC_n(1 - G_nR_e)} < 0 \tag{2.27}$$

The first term $(LG_n - C_nR_e)$ in equation (2.27) is negative. The magnitude of the term under the square root sign has to be smaller than the magnitude of the first term if the "+" solution is taken for the solution to be negative. Since the square term $((LG_n - C_nR_e)^2)$ is identical to the first term, $1 - G_nR_e$ has to be positive or

$$R_e < \frac{1}{G_n} \tag{2.28}$$

Combining the conditions for Case 2 as shown in Eqs. (2.26) and (2.28), the condition to achieve circuit stability becomes

$$2\sqrt{\frac{L}{C_n}} - \frac{LG_n}{C_n} < R_e < \frac{1}{G_n} \tag{2.29}$$

Combining conditions for both Case 1 and Case 2 as shown in Eqs. (2.24) and (2.29), the final condition for the circuit to achieve stability is

$$\frac{LG_n}{C_n} < R_e < \frac{1}{G_n} \tag{2.30}$$

Eqs. (2.17) and (2.30) are identical since the diode parameter a equals with the small signal conductance $G_n = a$ at the point of highest negative differential conductance in the NDR region (which corresponds to the origin of cubic polynomial model for the NDR device).

2.5 Summary

The differential equation for an NDR device oscillator topology has been derived in this chapter. For the special case of eliminating oscillations in the circuit during DC characterisation conditions on the circuit elements have been established. The same conditions were also established from small-signal analysis.

CHAPTER 3

DC CHARACTERISATION OF TUNNEL DIODES

3.1 Introduction

As briefly discussed in chapter 1, accurate DC characterisation of the negative differential resistance (NDR) region of tunnel diodes or RTDs is often hindered by parasitic oscillations [54]-[57]. A common method to solve the bias instability problem is to employ a stabilising resistor connected directly across the tunnelling diode [58]-[60]. It is however known that either too large or too small a shunt resistor cannot suppress oscillations effectively [58], [60], [64], [65] and the oscillations present in the bias circuit modify the measured characteristics of the NDR region.

In this Chapter, it is shown that using conditions established from the Van der Pol model as discussed in the Chapter 2, the shunt resistance can be chosen correctly (equation (2.17)) to eliminate all oscillations and hence obtain the correct I-V characteristics of the device. On this basis, a practical design methodology for the DC characterisation circuit of tunnel diodes has been developed, details of which are given in the following sections.

3.2 Simulation results of un-stabilised and stabilised tunnel diodes

The circuit for the measurement of I-V characteristics of NDR device is the same as the one shown in Fig. 2.5 and the condition for eliminating all oscillations in the circuit is given in equation (2.17) or (2.30). To verify this design guideline for DC measurements, transient/time domain simulations of the circuit of Fig. 2.5 were done using a commercial circuit simulation software, Advanced Design System (ADS) from Agilent Technologies [105]. The model of an Esaki tunnel diode that is commercially available, the 1N3717 packaged Germanium tunnel diode supplied by American Microsemiconductors was used in the simulations. The datasheet of tunnel diode 1N3717 is given in Appendix D. The diode was modelled by its measured I-V characteristic (Fig. 3.7) in parallel with a 13 pF capacitance extracted from RF measurements [94]. Details of extraction of the equivalent circuit elements of the tunnel diode will be described in chapter 4. A series inductance L of $\backsim$2 nH was used and it represents the external inductance L_e and device inductance L_s. For the 1N3717 diode, equation (2.17) gives the values of the shunt stabilising resistor to be in the range 7.5 $\Omega < R_e <$ 21 Ω (details in section 3.4).

The transient or time domain simulation tool within ADS provides the basic simulation results directly, i.e. signal amplitude versus time. The software provides the user with an in-built function named "fs(x)" that returns the frequency spectrum of the time domain signal (vector x) by using a chirp-z transform by

default [105]. By setting the available options, one could also apply a desired type of window e.g. Hamming, Hanning, etc. to the time domain data. For conversion of transient simulation data for oscillators, the default setting that uses the chirp z-transform with no window function applied to the data is recommended and was therefore used in all simulation results presented in this thesis. Transient simulation uses a variable time step and variable order algorithm. The user sets an upper limit on the allowed time step, but the simulator will control the time step so that the local truncation error of the integration is also controlled. The non-uniformly sampled data are uniformly re-sampled for function "fs", with the number of points being determined by increasing the original number of points to the next highest power of two. The data to be transformed by default is all of the data. The user may specify *start* and *stop* times to transform a subset of the data. Further information about this can be found via the online documentation of ADS [105]. It is useful to re-state here that the basic data from the time domain simulator is a time domain signal which can be analysed/ displayed as a spectrum using mathematical techniques (chirp z-transform in this case) and not vice versa.

3.2.1 Unstable circuit at low frequency

The circuit of Fig. 2.5 was simulated using the transient/time domain simulator with the following circuit elements and bias conditions: $R_b = 1\ \Omega$, $L_b = 56\ nH$, $L = 2\ nH$, $R_e = 50\ \Omega$, and $V_{bias} = 145\ mV$ (the DC voltage across the tunnel

diode is 140 mV). Here $R_e > 1/G_n$ and therefore the circuit is potentially unstable. Fig. 3.1 shows the time domain signals and corresponding spectrum of the signals across the tunnel diode. The results show that the oscillation frequencies are low ($\backsim$137 MHz) and mainly determined by $L_b(= 56\,nH)$ and $C_n(= 13\,pF)$, which indicate that low-frequency parasitic oscillations occur through the bias line. In this circuit, the net resistance at DC (and low frequencies) is negative and this causes circuit instability and hence the bias oscillations. This result will be discussed further in chapter 5 where an external decoupling capacitor is added in parallel with R_e since this is required for oscillator circuits in which bias oscillations are to be eliminated. The large number of harmonics seen in Fig. 3.1b are due to the switching (square-like) nature of the oscillations.

3.2.2 Stable circuit at low frequency

The simulation in the preceding section was repeated with the stability condition $R_e < 1/G_n$ is satisfied. Here $R_e = 5\ \Omega$ while the other circuit elements were left unchanged. Fig. 3.2 shows the time domain signals and corresponding spectrum of the signals across the tunnel diode. The time domain signal is shown over a longer (Fig. 3.2a) and shorter (Fig. 3.2b) time span. Poor resolution in Fig. 3.2a may erroneously suggest that there are two signals mixing, but the same signal over a shorter time span indicates there is no such mixing. The spectrum of the signal shown in Fig. 3.2c shows the presence of a high frequency signal

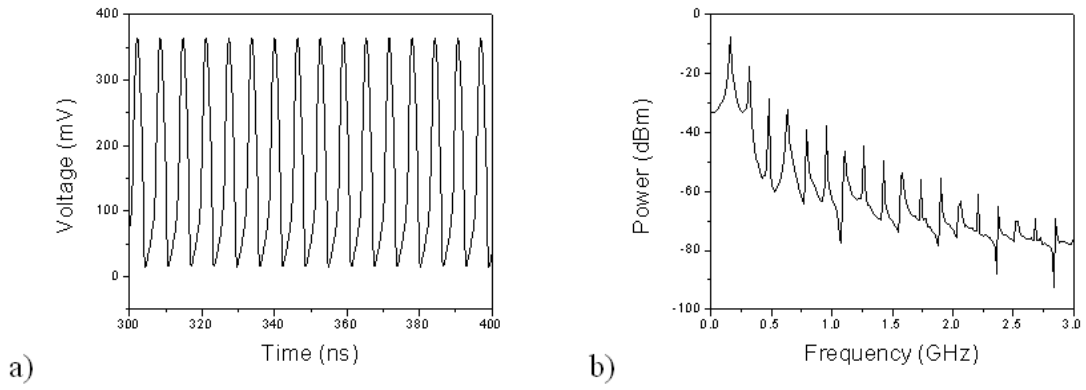

Figure 3.1: Simulation results of the tunnel diode bias circuit with $R_e > 1/G_n$. $R_b = 1\ \Omega$, $L_b = 56$ nH, $L = 2$ nH, $R_e = 50\ \Omega$, and $V_{bias} = 145$ mV (the DC voltage across the tunnel diode is 140 mV). (a) Time domain signal of the voltage across the NDR device (b) The spectrum of the voltage across the diode. The circuit oscillates at a low frequency (137 MHz) as determined by the bias line ($L_b = 56$ nH) and the tunnel diode capacitance characteristics ($C_n = 13$ pF).

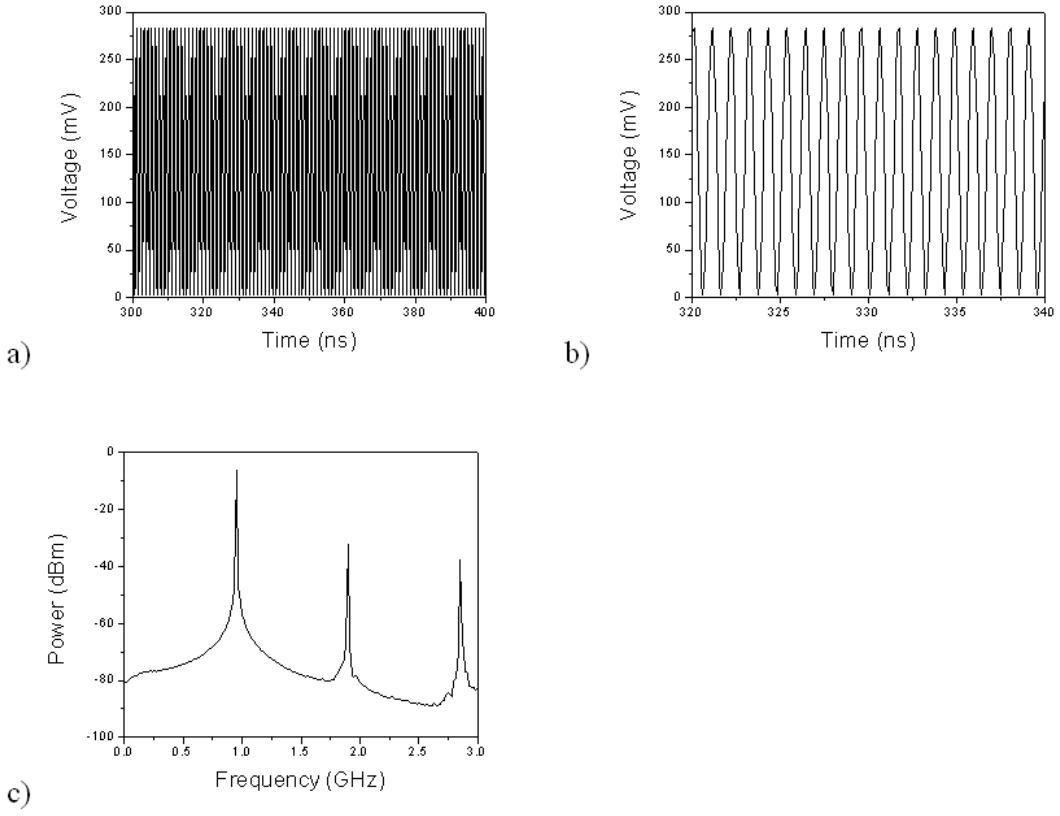

Figure 3.2: Simulation results of the tunnel diode bias circuit with $R_e < 1/G_n$. $R_b = 1\ \Omega$, $L_b = 56$ nH, $L = 2$ nH, $R_e = 5\ \Omega$ and $V_{bias} = 170$ mV (the DC voltage across the tunnel diode is 140 mV). (a) Time domain signals of the voltage across the load R_L over a 100 ns time span, (b) Time domain signals of the voltage across the load R_L over a 25 ns time span, (c) The spectrum of the diode voltage.

only, and no low frequency signal as would be expected in this case (this will be discussed further in chapter 5). It indicates fundamental oscillations of approximately 935 MHz and so this are clearly determined by the inductance $L(= 2\,nH)$ and capacitance $C_n(= 13\,pF)$. The value of $R_e = 5\ \Omega$ is small (it does not satisfy the first inequality in equation (2.17)) and hence high frequency oscillations exist in the circuit.

3.2.3 Stable circuit at low and high frequencies

Now consider the case when both the DC and low frequency stability condition and also the high frequency stability condition are satisfied, equation (2.17), $R_e = 15\ \Omega$. The other circuit elements were left unchanged as in the preceding two sub-sections. Transient simulation results for the circuit of Fig. 2.5 over a time span of $1\,ms$ for this case are shown in Fig. 3.3. The voltage across the device when biased in the NDR region remains constant with time as would be expected. This simulation result shows that both low-frequency bias oscillations and high-frequency oscillations are eliminated, and the circuit is stable. Therefore by proper choice of the stabilising resistance, the circuit for DC characterisation of tunnel diodes can be free from both low frequency bias oscillations and high frequency parasitic oscillations and so enabling distortion-free device characteristics in the NDR region to be determined.

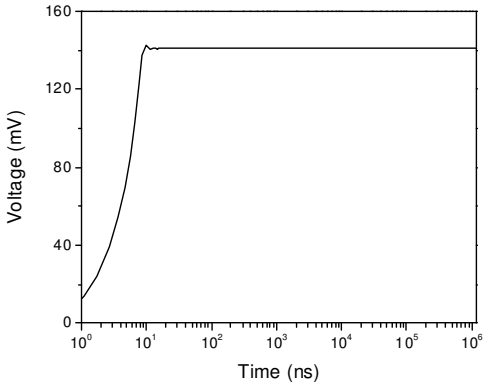

Figure 3.3: Time domain simulation results of the tunnel diode bias circuit with $aL/C_n < R_e < 1/a$. $R_b = 1\ \Omega$, $L_b = 56$ nH, L = 2 nH, $R_e = 15\ \Omega$, and $V_{bias} = 155\ mV$ (the DC voltage across the tunnel diode is 140 mV). It shows that neither low-frequency bias oscillations nor high frequency oscillations are present.

3.3 Direct characterisation of I-V characteristics

Using the circuit of Fig. 2.5, the diodes I-V characteristics can be measured indirectly. If direct I-V characterisation is desired, then a capacitor C_e can be introduced in the circuit as shown in Fig.3.4. In this case, the high frequency analysis is still the same as described in chapter 2 and equation (2.17) has still to be satisfied because C_e acts as an RF short circuit. At low frequencies, however, stability can no longer be established via (2.5) but needs to be re-analysed. In this case, the inductance L can be assumed as a short circuit and R_e can be ignored due to large C_e which adds to the device capacitance C_n. Fig. 3.5 represents the low frequency equivalent circuit and its similarity to Fig.2.6 should be apparent.

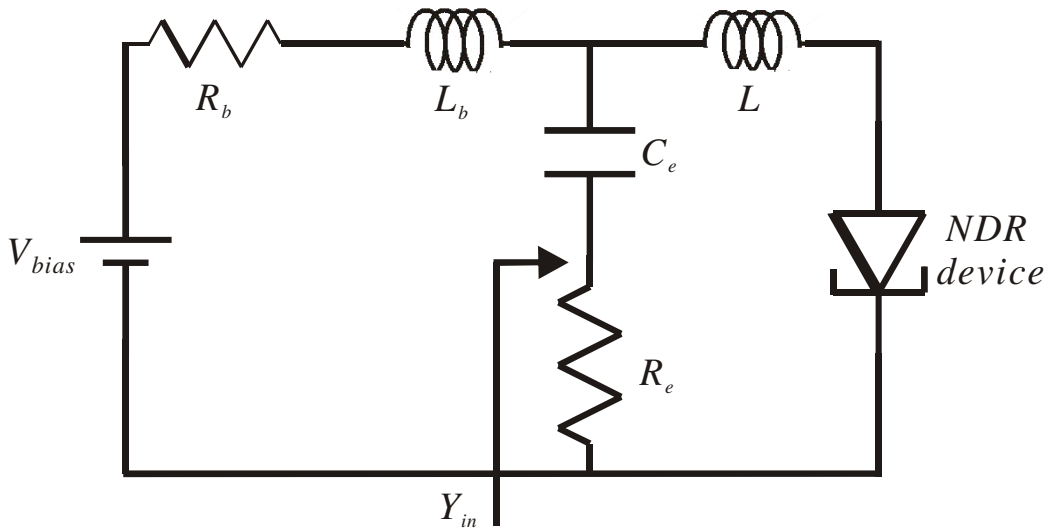

Figure 3.4: A circuit for direct I-V measurement of tunnel diodes or general NDR devices. An external capacitor C_e is introduced in series with R_e. Circuit stability is determined by equation (3.1). Transient simulations showed stability with $C_e = 6$ nF.

Therefore in addition to the condition on R_e in (2.17), R_b, L_b and C_e should satisfy (2.17) but with R_e, L and C_n replaced as follows

$$\frac{aL_b}{C_e + C_n} < R_b < \frac{1}{a} \tag{3.1}$$

The small-signal analysis is as the same as that discussed in section 2.4 only with R_e, L and C_n replaced by R_b, L_b and C_n+C_e, respectively. This condition is similar to that derived by Hines using small-signal analysis [61].

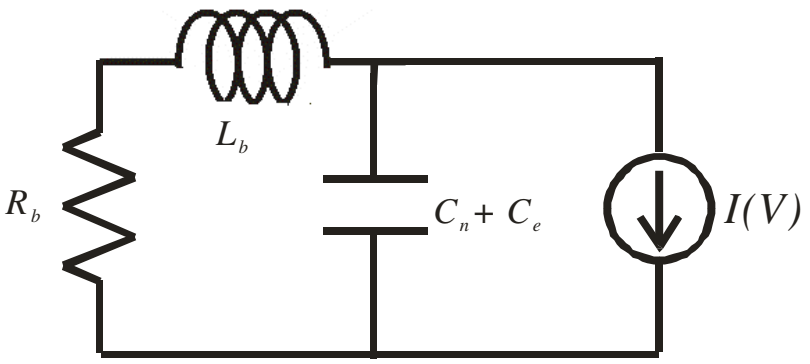

Figure 3.5: Low frequency equivalent circuit of Fig. 3.4. R_b and L_b model the resistance and inductance of the DC power supply and the bias line, respectively. $I(V)$ and C_n model the voltage controlled current source and capacitance of the NDR device, respectively. C_e is the external capacitor in series with R_e in Fig. 3.4.

3.4 Experiment Results

Commercially available 1N3717 and 1N3714 tunnel diodes from American Microsemiconductors were used in the experimental work. The I-V characteristics of the tunnel diodes were measured by Agilent B1500 semiconductor device analyzer (SDA) in steps of 5 mV. Measured I-V characteristics without bias stabilisation are shown in Fig.3.6. These measurements show the characteristic "plateau" distortion due to bias oscillations, but ΔI and ΔV values of 4 mA and 250 mV, and of 2 mA and 250 mV, for the 1N3717 and 1N3714 tunnel diodes, respectively, could be noted. The parameter G_n $(= a)$ was estimated from $3\Delta I/2\Delta V$ (see section 2.3). In practise. however, half the measured ΔV is used to compute the parameter a (reason for this given below), i.e. $a \backsim 0.048\,S$. The parameter a

of tunnel diode 1N3714 was calculated in the same way, i.e. ΔV is only about half the actual peak-to-valley voltage difference. Therefore, from the measured un-stabilised I-V characteristics the constant $a \backsim 0.024$ for tunnel diode 1N3714.

For the experimental tests, a series inductance L of $\backsim 2$ nH (realised from a microstrip line and lead inductance), and a tunnel diode capacitance of 13 pF extracted from RF measurements [94] were used. Therefore, from equation (2.17), the shunt stabilising resistor should satisfy the condition $7.5\ \Omega < R_e < 21\ \Omega$ for 1N3717 and $4\ \Omega < R_e < 42\ \Omega$ for 1N3714. Measured I-V results for tunnel diode 1N3717 employing different bias stabilisation, $R_e = 8\ \Omega$ and $R_e = 15\ \Omega$ are shown in Fig. 3.7. Clearly the I-V characteristic in Fig. 3.7a is distorted in the NDR region with oscillations while that in Fig. 3.7b seem to be free from oscillations (detailed analysis of these measurements is provided in the next sub-section).

The generic cubic polynomial has been compared to the measured I-V data in the NDR region as shown in Fig. 3.7(b). It approximates the crucial NDR region well but does not reproduce the broad valley region. Therefore designing the DC test fixture to satisfy (2.30) or (3.1), half the actual ΔV from un-stabilised measurements is used. Fig. 3.8 shows the measured I-V characteristic for tunnel diode 1N3714 and it seems to be free from bias oscillations (analysis in next sub-section). Note that, as already noted in section 2.3, the purpose of the cubic model is not to reproduce the I-V characteristics of an actual tunnel diode. In fact, a 9th order polynomial is required to accurately model the I-V characteristics of

the 1N3717 tunnel diode as will be shown in chapter 6. Nonetheless, it may be possible to improve the fit of the "cubic" model (*which features a shifted origin to the middle of the NDR region*) to actual data by using a higher order polynomial such as $I(V) = -aV + bV^3 + cV^5$ that also employs a shifted origin to the middle of the NDR region (this was not attempted in this work but worthy doing in the future).

The I-V characteristics of the tunnel diode 1N3717 were also measured by employing different shunt resistors, $R_e = 4\ \Omega$ and $R_e = 36\ \Omega$. The former does not satisfy the condition in equation (2.17) although it satisfies the condition in equation (2.5), i.e. $R_e < 1/G_n$. The latter neither satisfies the condition in equation (2.5) nor the one in (2.17). Measured I-V results are shown in Fig. 3.9, which show the presence of oscillations.

For direct I-V measurements, a test fixture was built using a series lumped inductance L_l of 56 nH (bias resistance R_b was estimated of 1 Ω), and $C_e = 6$ nF to satisfy (3.1). The stabilising resistances R_e were 8 Ω and 15 Ω, the same values used in the indirect I-V measurement setup. Measured I-V characteristics were practically identical for the two approaches.

3.5 Discussion

The second derivative of measured I-V curves can be used to detect the presence of oscillations even when the oscillation frequency is high (hundreds of MHz,

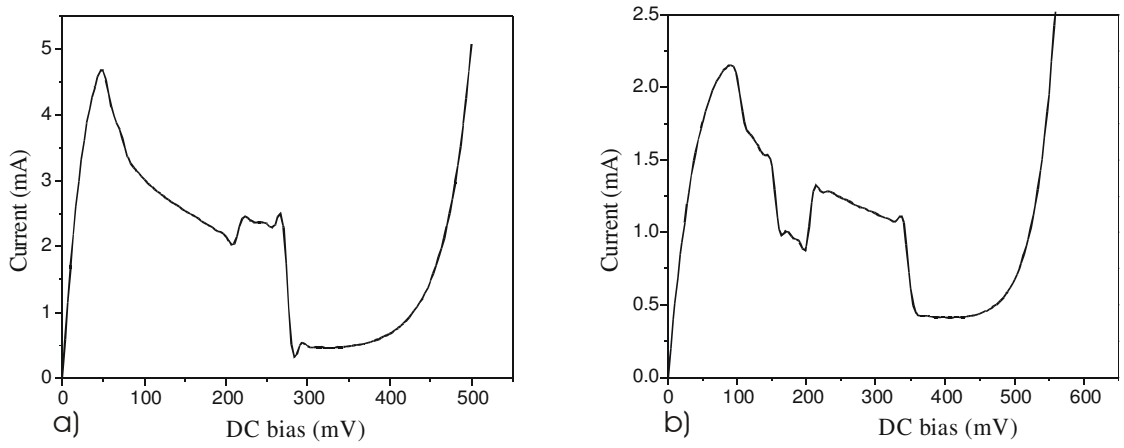

Figure 3.6: Measured I-V characteristics for a) tunnel diode 1N3717 and b) tunnel diode 1N3714 without bias and high frequency stabilisation. The curves in the NDR region have the characteristic 'plateau' distortion due to bias oscillations.

e.g. >100 MHz) or the oscillation amplitude is very small, e.g., below 10 mV [65]. As can be seen from Fig.3.6 for unstabilised devices, there is a fast decrease of current around the peak current area if the oscillations are present. This fast decease of current results in a valley in the first derivative of I-V curve, and therefore, the second derivative curve will show a sharp valley immediately followed by a sharp peak. The oscillations will be quenched around the valley current area where the negative conductance is small. The quenching of oscillations lead to a sharp decrease of current since the average current is larger if the oscillations are present. The second derivative will shows the characteristics of same a sharp valley immediately followed by a sharp peak. This pair of the oscillation characteristics in the second derivative curve can be used to detect whether there are

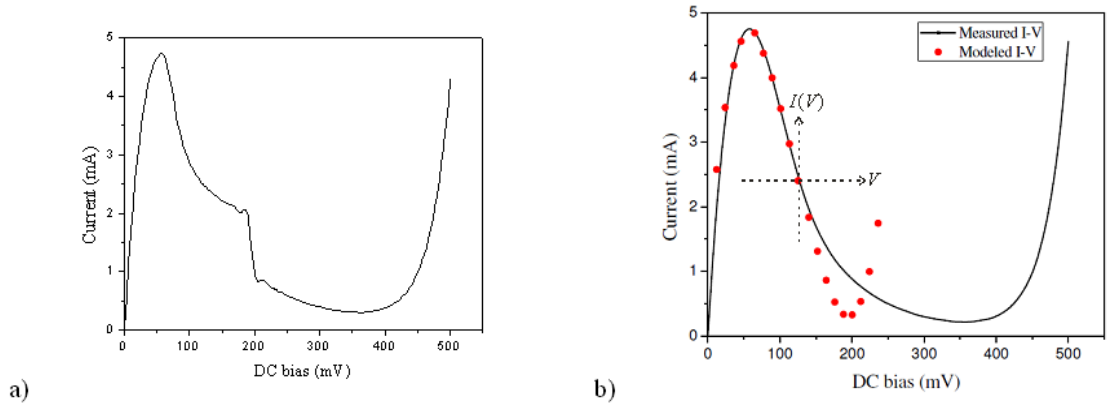

Figure 3.7: Measured current-voltage (I-V) characteristics for tunnel diodes 1N3717 using the circuit in Fig. 3.4: a) tunnel diode 1N3717 with $R_e = 8\ \Omega$, $C_e = 6$ nF, b) tunnel diode 1N3717 with $R_e = 15\ \Omega$, $C_e = 6$ nF. (a) contains oscillations while (b) is free from oscillations. The measured I-V curve in (b) has also been fitted with the cubic polynomial, showing a good fit (dots) to measured data (solid line) in the NDR region (except the broad valley region).

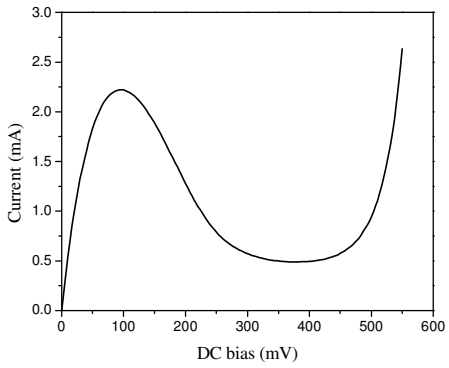

Figure 3.8: Measured current-voltage (I-V) characteristics for tunnel diode 1N3714 using the circuit in Fig. 3.4 $\mathrm{R}_e = 20\,\Omega$, $\mathrm{C}_e = 6\,nF$. The measured I-V curve seems free from oscillations.

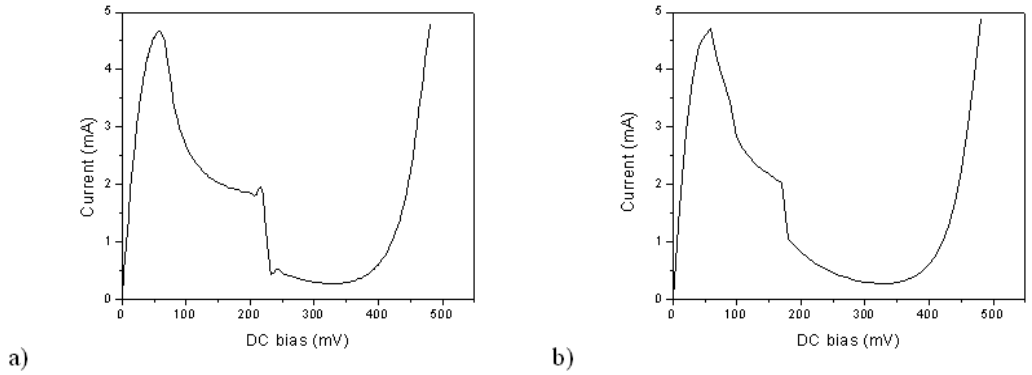

Figure 3.9: Measured current-voltage (I-V) characteristics for tunnel diodes 1N3717: a) tunnel diode 1N3717 with $R_e = 4\ \Omega$, b) tunnel diode 1N3717 with $R_e = 36\ \Omega$. Both I-V characteristics were modified by oscillations during the measurement.

oscillations present in the measurement [65].

Figs. 3.10 and 3.11 show derivatives for stabilized tunnel diode I-V measurements for the 1N3717 for $R_e = 8\ \Omega$, and $R_e = 15\ \Omega$, respectively. The second derivative confirms the presence of oscillations in the measurement shown in Fig. 3.7(a) ($R_e = 8\ \Omega$) while none for those shown in Fig. 3.7(b) ($R_e = 15\ \Omega$). For $R_e = 8\ \Omega$ only the conventional stability criterion (2.5) is satisfied (errors in estimating the element values for the test fixture meant (2.17) was not satisfied and oscillations were present during the measurement), while for $R_e = 15\ \Omega$, equation (2.17) is satisfied and the measurements are free from oscillations. Fig. 3.12 shows derivatives for stabilised 1N3714 tunnel diode I-V measurements for $R_e = 20\ \Omega$. Tunnel diode 1N3714 with is large negative differential resistance seems to be easily stabilised as expected from theoretical considerations. A wider range of

resistance values ($4\ \Omega < R_e < 42\ \Omega$ for 1N1714) can provide a stable circuit while a much narrower range ($7.5\ \Omega < R_e < 21\ \Omega$ for 1N3717) for the small negative differential resistance tunnel diode 1N3717 device.

The accuracy of the values of L and C_n is limited for the hybrid microstrip test fixture with packaged tunnel diodes employed in the experimental results described here. The proposed method should prove vital for the on-wafer characterisation of RTDs, for which C_n can be accurately estimated from the layer structure and L from the layout. For direct I-V characterisation, the bias cables modelled by L_b must be kept short so that a small value for C_e can be used to satisfy (3.1) (since R_b, the bias cable resistance, is small, approx. 1 Ω). Requirements on L_b and C_e could be relaxed by using an additional series resistance R_b (but not large enough as to cause bi-stability) which is then de-embedded from the measurements.

3.6 Summary

The criteria for designing test fixtures for the DC characterisation of tunnel diodes was developed and experimentally verified. The developed approach can also be used to accurately measure the current-voltage characteristics of RTDs on-wafer. Although the capacitance of a RTD (10 -100 fF range) which is much smaller than the capacitance of a tunnel diode (10 - 100 pF range), it is still

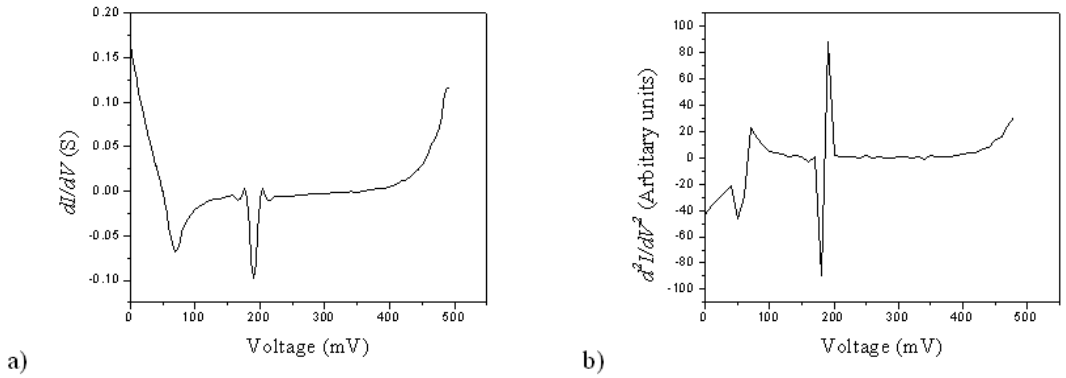

Figure 3.10: First (a) and second (b) derivatives of the I-V curve of the 'stabilised' 1N3717 tunnel diode (Fig. 3.7(a)). Here $R_e = 8\ \Omega$. The valley/peak in the second derivative shows the presence of oscillations in the 90 mV to 180 mV range of the NDR region.

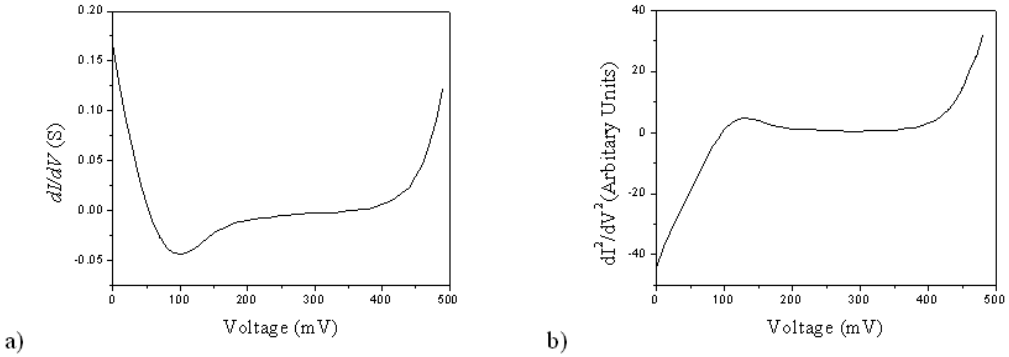

Figure 3.11: First (a) and second (b) derivatives of the I-V curve of the stabilised 1N3717 tunnel diode (Fig. 3.7(b)). Here $R_e = 15\ \Omega$. There are no sharp valleys followed immediately by sharp peaks in the second derivative showing no oscillations are present during measurement.

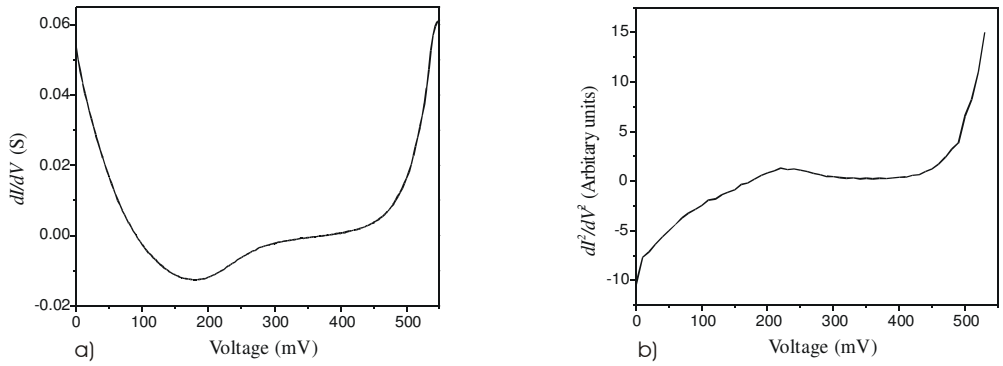

Figure 3.12: First (a) and second (b) derivatives of the I-V curve of the stabilised 1N3714 tunnel diode (Fig. 2.14(c)). There are no valleys/peaks in the second derivative showing no oscillations present during measurement.

possible to measure the I-V characteristics of the RTDs if the inductance between the shunt resistor and the RTD on-wafer can also be reduced to a few pico Henries, say10 pH (which corresponds to about 100 μm of a 50-Ω coplanar waveguide transmission line on a semi-insulating InP substrate, similar to that used for RTD integrated oscillators described in Chapter 8).

CHAPTER 4

RF CHARACTERISATION OF TUNNEL DIODES

4.1 Introduction

To aid in circuit design, especially for high frequency analogue circuits such as oscillators for which tunnel diodes and especially RTDs are ideally suited, an equivalent circuit model for the device in the NDR region is essential. This chapter describes a new measurement set-up suitable for RF characterisation of NDR devices with high peak currents (negative differential resistance of approx. $-20\ \Omega$) over the entire NDR region. First measurement results on a packaged tunnel diode indicate that accurate characterisation and subsequent small-signal equivalent circuit model extraction for the NDR region can be done, and they are independent of the set-up used to achieve circuit stability. The approach described here was first published in a conference paper by the author of this thesis [94]. A research group at the University of Duisburg-Essen followed the same approach, citing Ref. [94], for RTDs in monolithic form [95].

4.2 RF test fixture: theory and experiment

For RF characterisation of an NDR device, a stabilising pi-network in which the NDR device was embedded was employed. Fig. 4.1 shows a schematic diagram for the pi-network. The admittances Y_1 and Y_2 are the stabilising components (resistors), and the admittance Y_3 is that of the NDR device. The terminal currents and voltages can be described by

$$I_1 = Y_1 V_1 + Y_3(V_1 - V_2) \tag{4.1}$$

$$I_2 = Y_2 V_2 + Y_3(V_2 - V_1) \tag{4.2}$$

Combining Eqs. (4.1) and (4.2) gives

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_1 + Y_3 & -Y_3 \\ -Y_3 & Y_2 + Y_3 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{4.3}$$

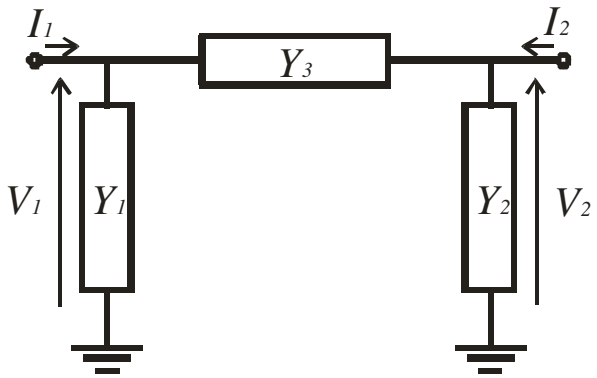

Figure 4.1: A diagram for a typical pi-network.

To establish stability conditions for this network, one can first consider the input impedance when the output node is grounded. Using equation (2.5) gives

the stability condition as

$$\mathrm{Re}(Y_1) > \mid \mathrm{Re}(Y_3) \mid \tag{4.4}$$

and then considering the output impedance when the input node to be grounded gives

$$\mathrm{Re}(Y_2) > \mid \mathrm{Re}(Y_3) \mid \tag{4.5}$$

In actual RF measurements (s-parameter characterisation), an elaborate circuit configuration as shown in Fig. 4.2 was used. The RF test-fixture consists of the NDR device and stabilising resistors R_1 and R_2 in a pi-network configuration terminated in two short sections of transmission line (Z_0 and l are the transmission line's characteristic impedance and length, respectively). The resistors are chosen to ensure circuit stability. At DC or low frequencies, the right hand terminal of the NDR device is grounded through the bias-T inductance. Here, the interconnects between the NDR device and the two stabilising resistors was reduced to a minimum (as was practically feasible) and the inductance associated with this was included in the diode lead inductance. R_1 is effectively in parallel with the NDR device and suppresses bias oscillations from the left hand terminal. The inductance from the bias-T that connects the tunnel diode to the ground would also cause oscillations. Therefore, another resistor R_2 was used to suppress the oscillations at the right hand terminal. Using this setup, s-parameter characterisation of the NDR device can be done. Note that R_1 and R_2 are connected to the microstrip ground (back side of the substrate) through holes (vias), and therefore

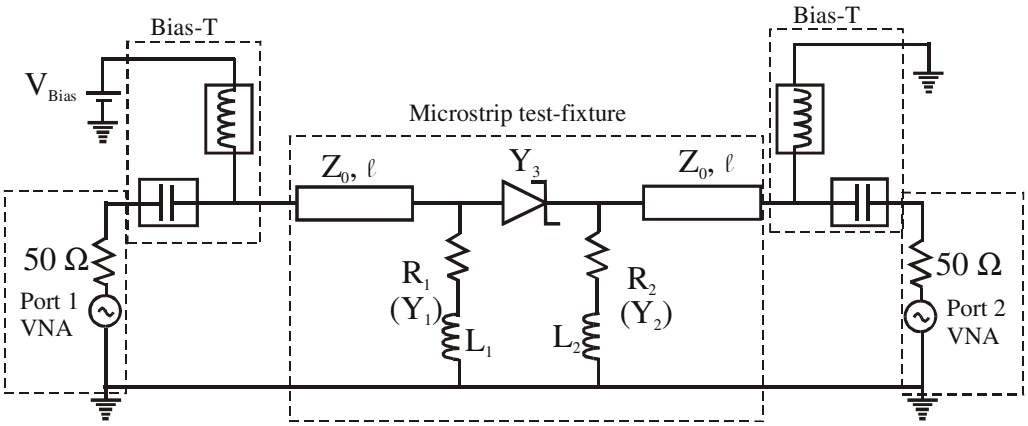

Figure 4.2: Schematic of the measurement set-up for s-parameter characterisation of an NDR device. Resistors R_1 and R_2 are chosen to cancel the negative conductance of the NDR device and so ensure circuit stability during characterisation.

this connection would act as a (small) inductance. This inductance adds to the shunt stabilising admittances Y_1 and Y_2 (is in series with the resistance) as illustrated in Fig.4.2 and therefore can be separated from the tunnel diode admittance Y_3 using the admittance matrix (equation (4.3)).

The measured -Y_{21} or -Y_{12} gives the admittance parameters (Y_3) of the NDR device. After measurement of the scattering parameters (s-parameters) of the complete test-fixture, the transmission line sections are de-embedded from the measurements and then the parameters converted into Y-parameters by the equations (4.6) and (4.7) [106].

$$Y_{12} = \frac{-2S_{12}Z_0}{(Z_0 + S_{11}Z_0)(Z_0 + S_{22}Z_0) - S_{12}S_{21}Z_0^2} \tag{4.6}$$

$$Y_{21} = \frac{-2S_{21}Z_0}{(Z_0 + S_{11}Z_0)(Z_0 + S_{22}Z_0) - S_{12}S_{21}Z_0^2} \tag{4.7}$$

where S_{11}, S_{12}, S_{21} and S_{22} are the s-parameters and Z_0 is the port impedance, usually 50 Ω. The s-parameters of the tunnel diode can be obtained from the Y-parameters of diode by the equation (4.8) [107]

$$S_{TD} = \frac{1 + Y_{12}Z_0}{1 - Y_{12}Z_0} \tag{4.8}$$

where S_{TD} are the s-parameters of the tunnel diode.

4.3 Experimental results

The equivalent circuit elements of the NDR device can be extracted from the measured Y_{12} or Y_{21}. A microstrip test-fixture was constructed using a microwave substrate of permittivity 3.48 and thickness 0.762 mm. The NDR device was a 1N3717 packaged tunnel diode from American Microsemiconductors, and both R_1 and R_2 were 10-Ω chip resistors chosen according to Eqs. (4.4) and (4.5), with maximum value of $|Re(Y_3)|$ estimated from the device's measured I-V characteristic. The transmission lines were of 50-Ω characteristic impedance and 10 mm long. This arrangement was characterised in a universal test-fixture from 40 MHz to 3 GHz using an Anritsu MS4624B vector network analyser (VNA). Test power was set to -15 dBm. A TTi QL 355 DC supply was connected through the network analyser bias-T to provide port 1 (left hand terminal) DC bias from 0 mV to 500 mV, and port 2 (right hand terminal) was connected to ground.

The measured parameters of the resistive branches to ground, Y_1 and Y_2, can be examined to verify if they indeed correspond to the used resistive elements. Fig.

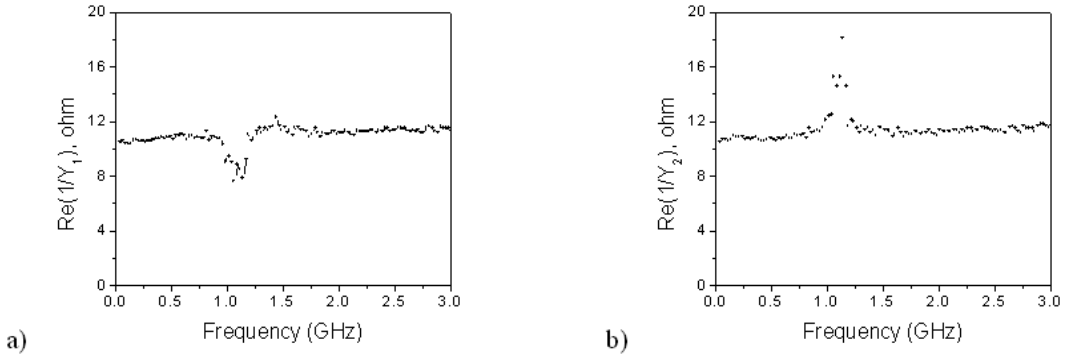

Figure 4.3: Real part of the stabilising resistive elements R_1 and R_2. The peak and trough in the measurement are assumed to be due to resonance caused by the inductance of the microstrip lines and the diode package capacitance.

4.3 shows the real part of the reciprocal of the measured Y_1 and Y_2, and demonstrates the expected frequency independence of the resistive elements. The via inductance to the ground of these elements could also be examined, and as shown in Fig. 4.4, this also shows the expected frequency independence. The results also show that there was resonance at about 1 GHz. This resonance was assumed to be caused mainly by the inductance of microstrip lines and the capacitance of the diode package.

4.4 Extracted RF model for the NDR region

The small-signal equivalent circuit model employed is shown in Fig. 4.5. It consists of the differential conductance (resistance), G_n (R_n), in parallel to capacitance, C_n. The inductance, L_s, and the resistance, R_s, model the passive extrinsic

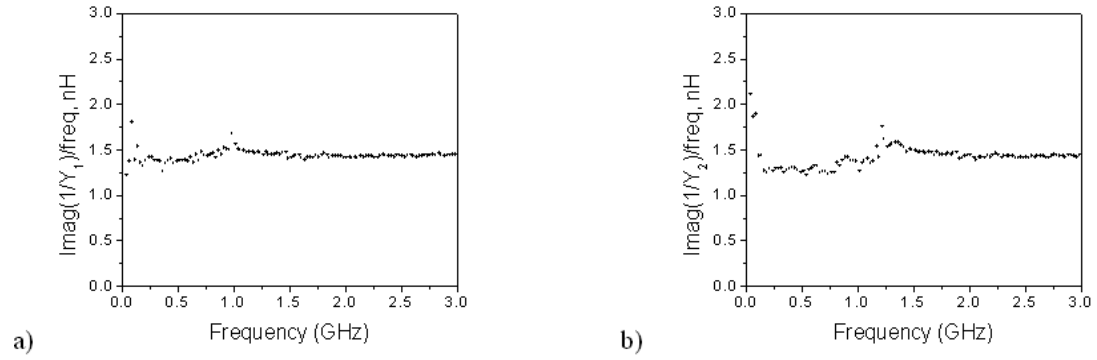

Figure 4.4: Imaginary part of the stabilising resistive elements R_1 and R_2, which corresponds to the via hole inductance.

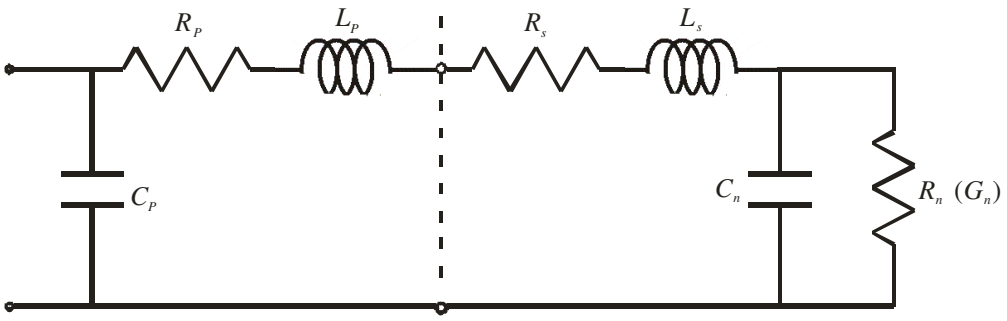

Figure 4.5: Small-signal equivalent circuit of an NDR device (including the package parasitic) with $L_s + L_p = 1.61$ nH, $R_p + R_s = 1.09\ \Omega$, $C_p = 0.41$ pF, $C_n = 12.42$ pF and $-G_n =$ -0.035 S when it was biased at 140 mV.

device. The package is modelled by the elements L_p, R_p and C_p [100]. Equivalent circuit parameters were extracted by fitting the measured Y-parameters data over the entire frequency range. Agilent's Advanced Design System (ADS) was used to do the fitting/optimisation. The Gradient optimizer in ADS was used for this. It uses the Gradient search method to arrive at new parameter values using the gradient information of the network's error function. The gradient of the error function indicates the direction to move a set of parameter values in order to reduce the error function. For each iteration, the error function and its gradient is evaluated at the initial point. Then the set of parameter values is moved in that direction until the error function is minimized. The Gradient optimizer uses the Least-Squares error function (see section 6.2.1 for details) to minimize the average weighted violation for the desired responses. So the value for the error function represents the average weighted violation for the desired responses and a value of zero indicates that all of the intended performance goals have been reached. The optimisation goal was to minimise the difference between the measured and modelled s-parameters over the measured frequency range.

For this step, the series inductances L_p and L_s were lumped together, as well as the series parasitic resistances R_p and R_s. Fig. 4.6(a) and (b) show the measured and modelled s-parameters of the tunnel diode in the NDR region at 140 mV (where is in the middle of NDR region of the tunnel diode 1N3717). The extracted equivalent circuit model accurately reproduces the measured data. At

a bias voltage of 140 mV, the extracted element values were: $L_s + L_p = 1.61\ nH$, $R_p + R_s = 1.09\ \Omega$, $C_p = 0.41\ pF$, $C_n = 12.42\ pF$ and $-G_n = -0.035\ S$. Note that the value of G_n from DC characterisation at the same bias point was $-0.048\ S$. This difference may be attributed to the two different devices actually used even though they were both of the same type, and to the inaccuracies in the extraction procedure (e.g. errors in de-embedding the transmission line sections) that hamper accurate determination of the equivalent circuit elements.

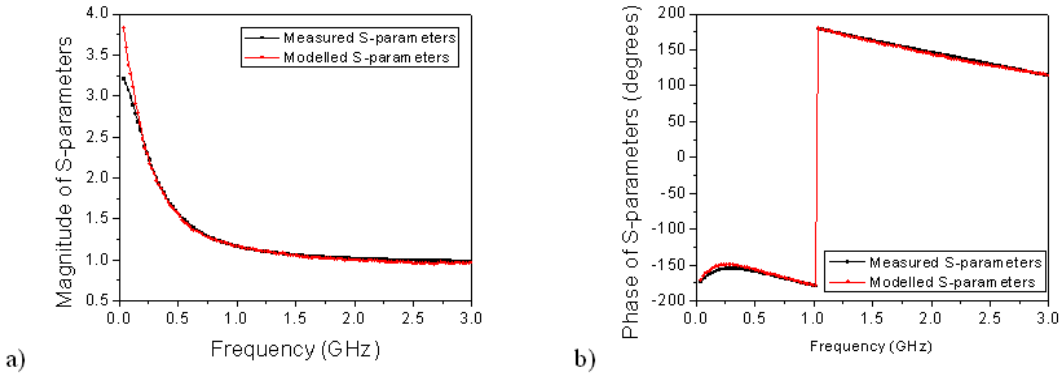

Figure 4.6: The measured (converted from measured Y-parameters, Y_{12} or Y_{21}) and modeled s-parameters of the tunnel diode in the NDR region at 140 mV, a) Comparison between measured and modelled magnitude of the s-parameters, b) Comparison between measured and modelled phase of the s-parameters.

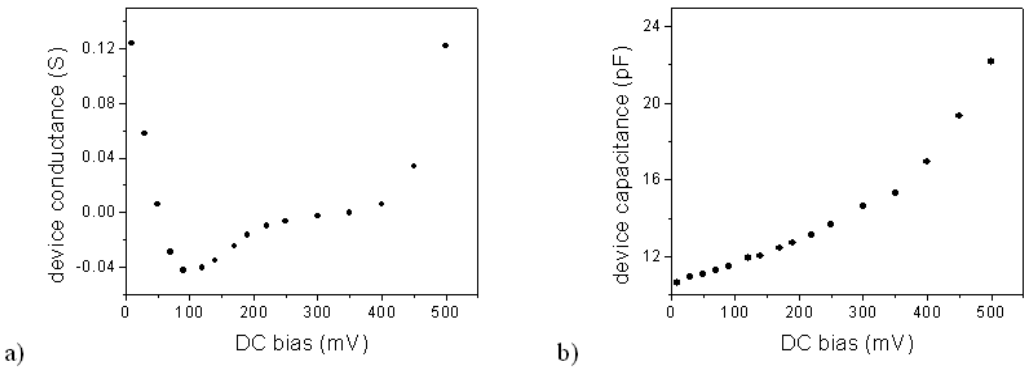

Figure 4.7: Extracted device conductance and capacitance of a tunnel diode (1N3717) with different DC bias voltages: a) The extracted device conductance, b) the extracted device capacitance.

4.4.1 Variation of G_n and C_n with bias

The extrinsic elements of the small-signal equivalent circuit of the 1N3717 tunnel diode were determined in the previous section to be $L_s + L_p = 1.61$ nH, $R_p + R_s = 1.09\ \Omega$, $C_p = 0.41$ pF. These elements are considered to be constant with bias. The intrinsic elements C_n and G_n were extracted as a function of bias and are shown in Fig. 4.7. The device capacitance increases with bias and the device differential conductance varies as expected. The extracted conductance graph, Fig. 4.7a, is very similar to that extracted from the I-V characteristics of a similar device, see Fig. 3.11(a). The capacitance varies from 11 pF at 0 V to 22 pF at 500 mV. In the critical NDR region the diode capacitance varies from 12 - 14 pF.

4.5 Summary

A method for RF characterisation of tunnel diodes has been described. Stability in the NDR region is achieved by embedding the tunnel diode in stabilising resistors in a pi-network topology. The device parameters were extracted from the measured s-parameters by de-embedding the circuit elements in which the tunnel diode is embedded, and from these, the small signal equivalent model of the device at any bias point could be extracted. Results obtained using a microstrip test-fixture and a packaged tunnel diode demonstrate that RF measurements can be made but small errors may occur in the measurement from the de-embedding of the transmission line. The proposed methodology lends itself well to monolithic implementation for RF characterisation of high speed RTDs, and it has been successfully employed for on-wafer RTDs characterisation by a research group at the University of Duisburg-Essen, Germany [95]. For a monolithic implementation and on-wafer characterisation, the length of transmission line can be reduced and it is expected that the de-embedding of the transmission line sections would be a lot more accurate.

CHAPTER 5

OSCILLATOR DESIGN WITH TUNNEL DIODES

5.1 Introduction

In this chapter a new oscillator design methodology employing tunnel diodes will be discussed. The method results in oscillators without the issues of parasitic oscillations and when two diodes instead of one are used in an oscillator circuit, the output power doubles. The method for suppressing the low-frequency bias oscillation has been discussed in chapter 2, and it will be demonstrated here how it is implemented in an oscillator circuit. This design method is expected to be applicable to RTD-based oscillators [44], [45]. This chapter also discusses previously published planar RTD oscillator circuits in comparison to the topology developed here.

5.2 Requirements for tunnel diode sinusoidal oscillator design

As discussed in Chapter 2, when the elements of the circuit in Fig. 2.5 satisfies the condition of equation (2.17), there can be no oscillations in the circuit. The only way to produce high frequency oscillations in this circuit whilst ensuring DC and low frequency stability is to reduce the resistance of the external shunt resistor

R_e, which would increase the DC power consumption, or increase the inductance L so that the lower inequality of (2.17) is not satisfied. To avoid reducing R_e to low values, an external capacitor C_e was connected parallel with this resistor as shown in Fig. 5.1 with the capacitor chosen to act as an RF short circuit. The short circuited resistor R_e now no longer stops RF oscillations which are decoupled from the bias circuit by C_e and R_e. The large-signal RF equivalent circuit of Fig.5.1 is similar to the Fig.2.6 with $R_e = 0$ and current source parallel with the load R_L, with the total current through the current source and the load given by $I(V) = -(a - G_L)V + bV^3$, where $G_L = 1/R_L$. Therefore, equation (2.12) can be re-written as (with the diode capacitance C_n assumed constant for the RF oscillation signals to simplify analysis; ideally, C_n should be replaced with a voltage controlled (non-linear) charge source Q_n)

$$LC_n\frac{d^2V}{dt^2} + L(-(a - G_L) + 3bV^2)\frac{dV}{dt} + V = 0 \tag{5.1}$$

$$\frac{d^2u}{d\tau^2} - \varepsilon(1 - u^2)\frac{du}{d\tau} + u = 0 \tag{5.2}$$

where $\tau = \frac{t}{\sqrt{LC_n}}$, $u = \sqrt{\frac{3b}{a-G_L}}V$ and $\varepsilon = (a - G_L)\sqrt{\frac{L}{C_n}}$.

Equation (5.2) is the Van der Pol equation, which can be used to describe simple circuits that include NDR components [102], [103]. For a given device/circuit the waveform of the signal is determined by the value of L (or equivalently ε):

$$\varepsilon = (a - G_L)\sqrt{\frac{L}{C_n}} \tag{5.3}$$

If the small value of ε is very small ($\varepsilon << 1$) the solution to equation (5.2) is

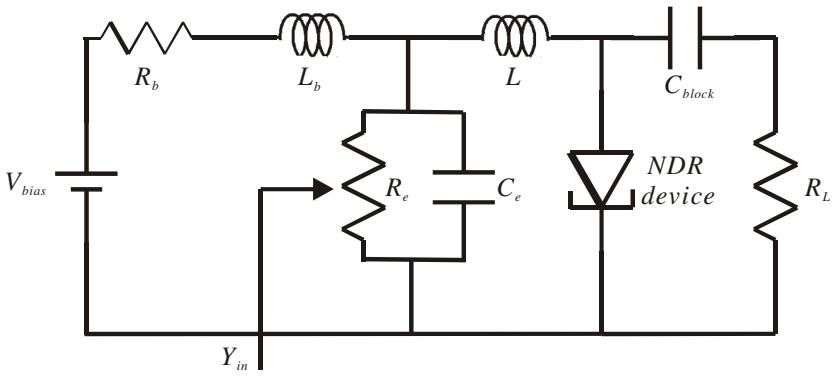

Figure 5.1: A NDR device oscillator topology with the DC decoupling circuit (R_e, C_e). R_b and L_b model the resistance and inductance of the bias line. C_{block} and R_L are DC block and load, respectively. The total inductance L and capacitance of the NDR device determine the frequency of oscillation.

sinusoidal [98]. Therefore if ε is chosen such that $\varepsilon << 1$, the oscillator would produce a sinusoidal waveform as long as

$$L \leqslant \frac{\varepsilon^2 C_n}{(a - G_L)^2} \tag{5.4}$$

For this parallel oscillator topology, to obtain the maximum output power the load should satisfy the condition, $G_L = G_n/2$ (This condition will be derived and discussed in chapter 8). Since $G_n = a = 3\Delta I/2\Delta V$ at the bias point, equation (5.4) can be re-written as

$$L \leqslant \frac{4\varepsilon^2 C_n}{G_n^2} \tag{5.5}$$

Equation (5.5) gives the maximum inductance value for the lowest frequency (sinusoidal) oscillations for a given NDR device (as determined by the device

characteristics and ε). For large values of L, ε becomes large and the waveform becomes non-sinusoidal (relaxation oscillations). In this case L will be larger than that given by equation (5.5) and the power produced is distributed over a larger frequency range. Therefore, to concentrate most of the power at the fundamental frequency it is necessary to design a circuit that achieves the desired oscillation frequency f_0 ($f_0 = 1/(2\pi\sqrt{LC_n})$), and also satisfies equation (5.5) so as to simplify the bias circuit design.

To establish the design guideline derived above (equation (5.5)) for an actual oscillator circuit, the circuit of Fig. 5.1 with a 50 Ω load R_L was simulated in Advanced Design System (ADS) circuit simulation software with the model of a tunnel diode, the 1N3717 packaged tunnel diode. These diodes are commercially available from American Microsemiconductors and so are suitable for experimentally testing NDR circuit concepts. The diode was modelled by its measured I-V characteristic (Fig. 3.7(b)) in parallel with a 13 pF capacitor extracted from RF measurements [94]. A table-based model[1] represents the measured, and (spline) interpolation used to approximate the currents between measurement points. For this diode, the difference between the peak and valley currents ΔI is 4 mA, and the difference between the peak and valley voltages ΔV is 250 mV.

Table 5.1 shows detailed simulation results of the voltage across the tunnel diode for various values of ε (or equivalent inductance L). The magnitudes of the

[1]Note that the cubic model described in chapters 2 and 3 is not suitable for circuit design. Measured data in a table-based model or modelled with a 9th order polynomial (see Ch.6) is required to model I-V characteristics of the tunnel diode for circuit simulation.

ε	L (nH)	f_0 (MHz)	P(f_0) (dBm)	P($2f_0$) (dBm)
2	90	129	-9.3	-21.6
1	22.6	260	-9.1	-27.7
0.5	5.6	568	-8.8	-34.8

Table 5.1: Simulation results of the power delivered to a 50-Ω load for various values of ε. f_0 is the fundamental frequency, P(f_0) is the power at fundamental, and P($2f_0$) is the power at the first harmonic.

fundamental and first harmonic frequency (both normalised to power dissipated in a 50 Ω load) are given. The other harmonics, such as 2nd and 3rd harmonics, are even weaker than the 1st harmonic, they are therefore ignored in the power analysis. It can be seen that for $\varepsilon = 0.5$, the 1st harmonic is more than 26 dB below the fundamental and so the oscillations are essentially sinusoidal. The 2nd and 3rd harmonics are both 12 dB below the 1st harmonic. Therefore inductance values of 5.6 nH or lower would be required to realise (quasi-) sinusoidal oscillators with these tunnel diodes.

5.3 Simulation results of oscillator circuits

5.3.1 Oscillators with bias stabilisation

Transient simulations of the circuit of Fig. 5.1 was carried out in ADS for the cases in which the condition for bias stabilisation was and was not satisfied. In the first case, the stabilising resistance R_e was chosen such that $R_e < 1/G_n$, i.e.

the circuit should have DC and low frequency stability. The circuit elements and biasing voltage were as follows: $R_b = 1\ \Omega$, $L_b = 56\ nH$, $R_e = 15\ \Omega$, $C_e = 2.5\ nF$, $R_L = 50\ \Omega$, $C_{block} = 2.\ nF$, and $V_{bias} = 180\,mV$. In this case, the net circuit conductance at DC and low frequencies is positive, and there should be no low frequency oscillations in the circuit. Fig. 5.2 shows the time domain signal of the voltage across the shunt resistor R_e which settles to the desired DC bias point after initial oscillation. The simulation was carried out over a 1 ms time span. The results that the tunnel diode is always biased at the desired DC bias point in the NDR region. However, high frequency oscillations would be expected to occur in the circuit since the lower inequality of equation (2.17) is not satisfied. Fig. 5.3 shows the simulated voltage across the load resistance R_L that indicates the presence of oscillations of about 625 MHz. Fig.5.3a and b show the time domain signal of the voltage across the load R_L over a longer and shorter time span of 100ns and 20 ns, respectively, while Fig. 5.3 shows the spectrum of the voltage this time signal. These simulation results show that the circuit oscillates at high frequency (625 MHz) determined by series inductor ($L = 4\ nH$) and tunnel diode capacitance C_n. This oscillation frequency is determined by only the inductance L and the tunnel diode capacitance C_n. Here, the capacitance C_e is chosen large enough, $(2\pi f_0 C_e)^{-1} < 0.1$, to act as a RF short circuit, where f_0 is the oscillation frequency determined by the inductance L and the tunnel diode capacitance C_n.

The appearance of Fig.5.3a may seem to suggest that there may be mixing

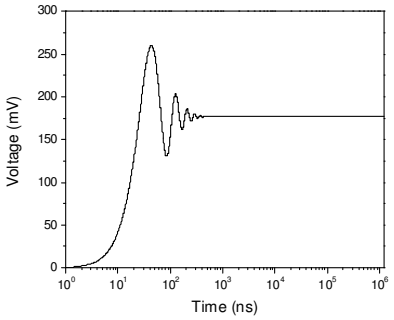

Figure 5.2: Simulation result of the tunnel diode oscillator with $R_e < 1/G_n$. $R_b = 1\ \Omega$, $L_b = 56$ nH, $L = 4$ nH, $R_e = 15\ \Omega$, $C_e = 2.5$ nF, $R_L = 50\ \Omega$, $C_{block} = 2.5$ nF and $V_{bias} = 180$ mV. It shows the time domain signal of the voltage across the shunt resistor R_e. The voltage across R_e, which is the same as across the bias line, is constant with time indicating that no bias oscillations are present.

or "beating" of a low frequency signal with the high frequency one. This is not the case as may be seen from the same Fig.5.3b which is identical to Fig.5.3a but over a shorter time span. It is thought that the resolution of the image gives this wrong optical impression. This appearance of Fig.5.3a is certainly not a result of the power spectrum acquisition method. The simulation results shown in Fig.5.3a comes directly from the time domain simulation, i.e. the time domain signal is the basic output from a time domain simulator [105]. This basic signal can be analysed/displayed as a spectrum using mathematical techniques (chirp z-transform in this case) as explained in section 3.2. Therefore Fig.5.3c is obtained from the time domain signal in Fig.5.3a and not vice versa.

5.3.2 Oscillators without bias stabilisation

The other case is that the condition $R_e < 1/G_n$ is not satisfied. The circuit elements and biasing voltage were as in the preceding case but with $R_e = 50\,\Omega$. Therefore, the net conductance at DC (and low frequencies) is negative which would cause the circuit to be unstable. Fig. 5.4 shows the time domain signal and corresponding spectrum of voltage across the shunt resistor R_e for this condition. Instead of maintaining the device at the desired DC bias point as shown in Fig. 5.2, the voltage across the resistor R_e oscillates around the desired bias point (see Fig. 5.4(a)) and the oscillations frequency is mainly determined by L_b and C_e (in this simulation $L = 0\ nH$). The frequency of oscillation ($\backsim$12 MHz) is mainly determined by L_b, and C_e. Here, the voltage across R_e, which is the same as across the bias line, varies with time and clearly indicates that bias oscillations are present.

The simulation was repeated with $L = 4\ nH$. Note that here the net circuit resistance at DC is negative and hence bias oscillations could be expected. Because of the varying bias voltage, the desired high frequency oscillations (determined by L and C_n) occur only when the DC voltage across the tunnel diode is within NDR region. Otherwise there would be no oscillations. Therefore there are two oscillations across the load R_L, see Fig. 5.5(a). Fig. 5.5(b) shows the oscillations over a narrow time range, 350-410 ns, while Fig. 5.5(c) is the spectrum of the signal. The spectra in Fig. 5.3(b) and 5.5(c) over a 1 μs timeframe, but only

a shorter time span for the time domain signal is shown for clarity. Clearly C_e does not decouple the bias supply and the frequency of oscillation ($\backsim$12 MHz) is determined by all the reactive components of the circuit: L_b, C_e, L_e and C_n. The circuit occasionally oscillates at a high frequency (see Fig. 5.5(a)).

For this case when both low-frequency and high frequency oscillations were present (Fig. 5.5), the RF output power was low. It should be apparent from Fig. 5.5 that high frequency oscillations are intermittent, only present when the low frequency signal is within the NDR range. Therefore the RF output power is low. The simulation results presented here suggest that the tunnel diode or RTD oscillator circuits not employing the R_e (and C_e) bias stabiliser, e.g. Ref. [88], are likely to suffer from (parasitic) bias oscillations and consequently will have low RF output power. It is useful to note here that tunnel diode or RTD oscillators may be designed specifically as (low frequency) relaxation oscillators, e.g. Ref. [108].

5.4 Oscillator topology and design

Figure 5.6 shows the new topology for a single device tunnel diode oscillator and its large signal RF equivalent circuit. Unlike in the basic NDR oscillator studied in the previous sections, Figure 5.1, here the frequency determining inductance L is located after the NDR device. This way several devices could be connected to at node A, all utilising the same inductance to achieve oscillation, see e.g. Fig.5.7

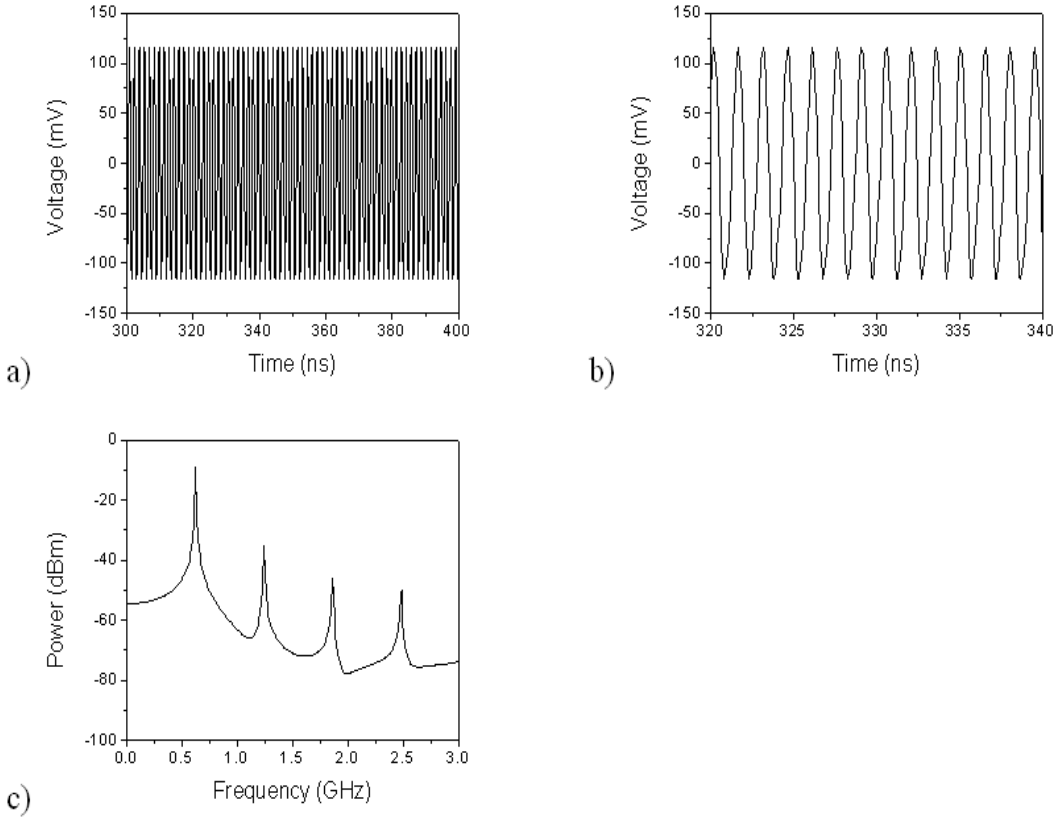

Figure 5.3: Simulation results of the tunnel diode bias circuit with the same conditions as shown in Fig. 5.2. (a) Time domain signal of the voltage across the load R_L. (b) The voltage across the load R_L between 320 ns and 340 ns. (c) The spectrum of the voltage across the R_L. The circuit oscillates at high frequency (625 MHz) determined by series inductor ($L = 4\,nH$) and tunnel diode capacitance C_n.

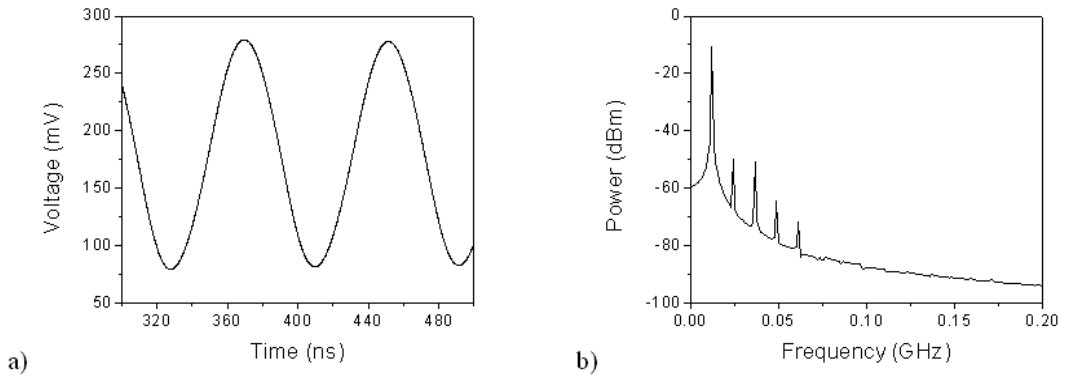

Figure 5.4: Simulation results of the tunnel diode oscillator with $R_e > 1/G_n$. $R_b = 1$ Ω, $L_b = 56$ nH, $L = 0$ nH, $R_e = 50$ Ω, $C_e = 2.5$ nF, $R_L = 50$ Ω, $C_{block} = 2.5$ nF and $V_{bias} = 180$ mV. (a) Time domain signal of the voltage across the shunt resistor R_e. (b) The spectrum of the voltage across R_e.

with its large signal RF equivalent circuit for an oscillator employing two tunnel diodes together .

At DC or low frequencies, the individual NDR devices in an oscillator employing two or more tunnel diodes are decoupled since inductance L acts as a short circuit. Therefore, each NDR device can be individually biased in this case. The DC decoupling circuits are designed as described in section 5.3. The required decoupling resistor R_{ei} chosen according to equation (2.5) is independent of the number of NDR devices in the circuit. The capacitor C_{ei} is used to short circuit the RF signal from the NDR device to ground, which further improves the DC stability and eliminates RF power dissipation by resistor R_{ei}. Capacitor C_{ei} short circuits bias resistor R_{ei} at the oscillation frequency. Because there are

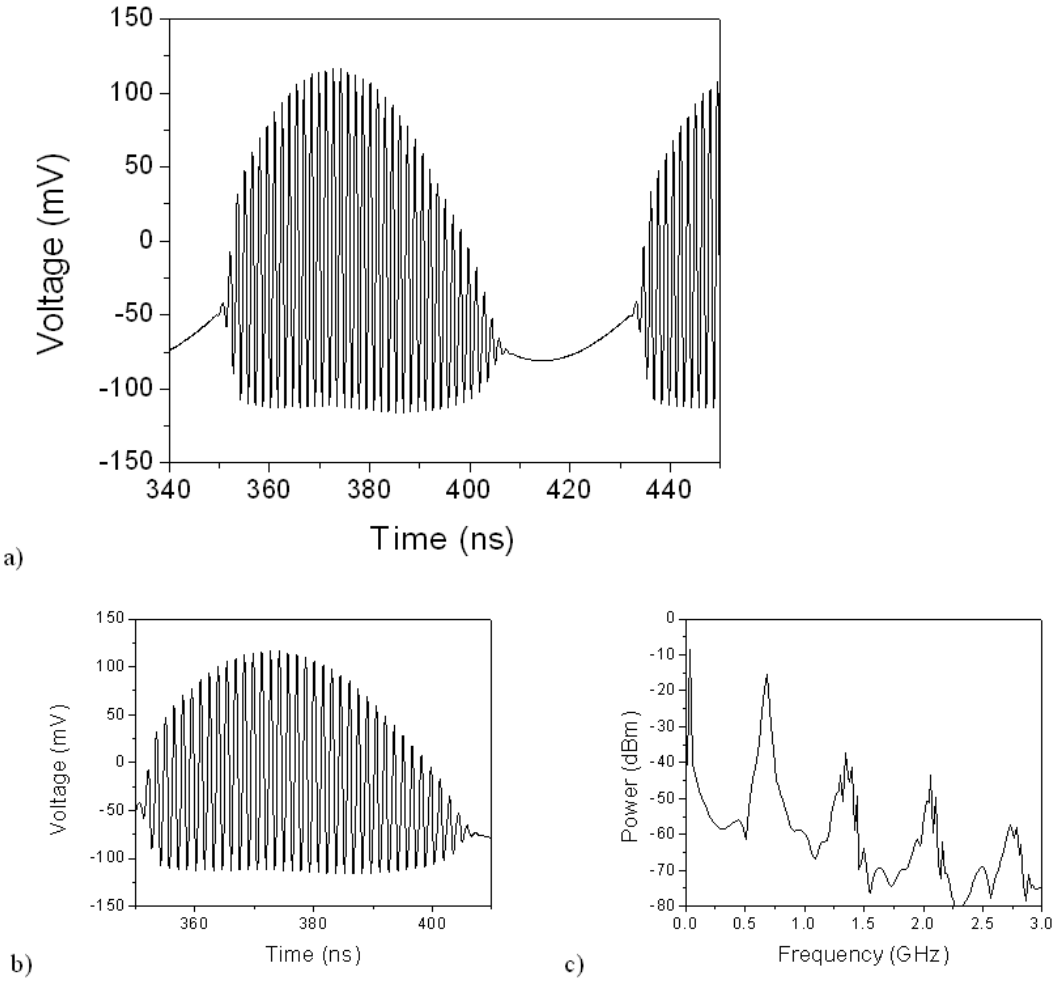

Figure 5.5: Simulation results of the tunnel diode bias circuit with the same conditions as shown in Fig. 5.4. (a) Time domain signal of the voltage across the load R_L. (b) Time domain signal of the voltage across the load R_L between 350 ns and 410 ns. (c) The spectrum of the voltage across R_L.

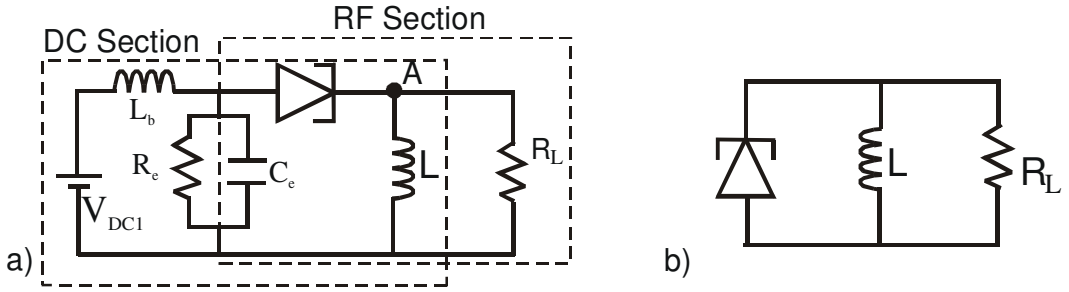

Figure 5.6: a) A single NDR device oscillator topology with DC stabilisers C_e and R_e ($R_e < 1/G_n$), oscillation frequency determining inductance L, and load resistance R_L. b) RF equivalent circuit

no bias line oscillations with this topology and design methodology, larger area RTDs ($\Delta V/\Delta I \approx -50\ \Omega$) can be employed [63], [72] in oscillator circuits. The small-signal RF equivalent circuits of these oscillator circuits are shown in Fig. 5.8. For the oscillators employing two tunnel diodes, the total conductance is $-(G_{n1} + G_{n2})$ and the total capacitance is $C_{n1} + C_{n2}$, where subscripts 1 and 2 refer to NDR device 1 and NDR device 2, respectively.

5.5 Experimental results

The 1N3717 tunnel diode was used in circuit design and implementation. The parameter ε was chosen as 0.5 (or $L \backsim 5.6$ nH) to realise oscillation frequencies easily achievable by the packaged tunnel diodes. In the design of both the single and two tunnel diode oscillators, an inductance value of approximately 5.6 nH was used. With the 1N3717 diode biased in the NDR region ($C_n \sim 13$ pF) the

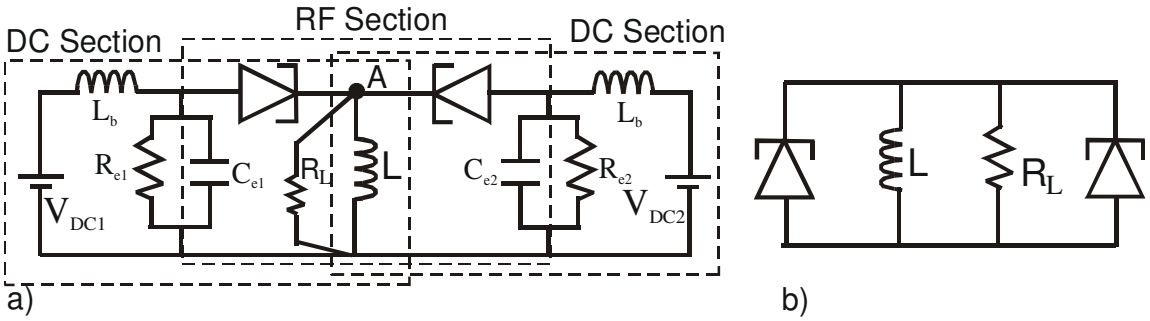

Figure 5.7: a) A two tunnel diode parallel-connected oscillator topology with DC stabilisers C_{e1}, R_{e1}, C_{e2} and R_{e2} ($R_{e1} < 1/G_n$ and $R_{e2} < 1/G_n$), the inductance L, DC block C_{block} and 50 Ω load R_L. In both circuits the output power is taken from node A thereby establishing a parallel resonant circuit. b) RF equivelent circuit.

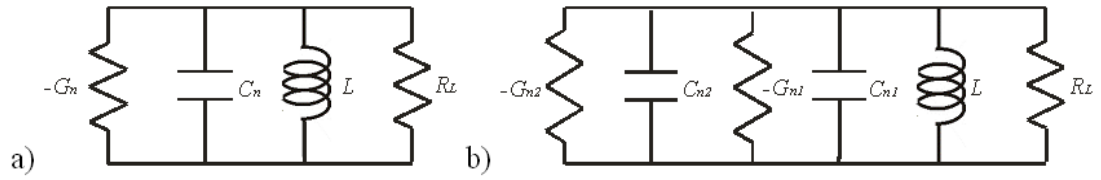

Figure 5.8: (a) RF equivalent circuit of a single NDR device oscillator (Fig. 5.6): -G_n and C_n are the negative differential conductance and the capacitance of the NDR device based in the NDR region, (b) RF equivalent circuit of a two NDR device parallel-connected oscillator (Fig. 5.11): -G_{n1}, and -G_{n2} are the negative differential conductance, and C_{n1} and C_{n2} are the capacitances of the NDR device 1 and NDR device 2 biased in the NDR region, respectively.

oscillators were expected to operate at about 600 MHz and 450 MHz for the single diode and two-diode oscillator, respectively. The difference in oscillation frequencies is due to the increased total capacitance ($\sim$26 pF) of the two-diode circuit, as should be clear from the small signal equivalent circuit (Fig. 5.8).

The circuits were realized in microstrip hybrid technology using a microwave substrate with a dielectric constant of 3.48 and a thickness of 0.762 mm. A picture of the fabricated two tunnel diode oscillator is shown in Fig. 5.9. A 15 mm 50-Ω microstrip line ($\backsim$4 nH) was used to realise the inductor in the circuit, and so the design oscillation frequency was around 450 MHz (taking into account the series inductance of each tunnel diode of 1.6 nH). At the output, a 50-Ω microstrip line was used to connect to the 50-Ω cable that was connected to the spectrum analyser. The load resistance was fixed to 50 Ω[2]. The DC bias voltage was supplied by a TTi QL355 power supply, and the oscillation signal was measured by an Agilent RF spectrum analyzer E4448A.

A single tunnel diode oscillator was measured as a reference in the same set-up, and it provided an output power -10.17 dBm (0.096 mW) at 618 MHz when it was biased at 180 mV (Fig. 5.10) and -9.42 dBm (0.114 mW) at 621 MHz when as biased at 250 mV. The smaller span spectrum around the fundamental oscillations frequency (618 MHz biased at 180 mV) is shown in Fig. 5.11(b) which also indicates that no low-frequency bias oscillation occur in the single tunnel diode

[2]Ideally, a quarter-wave transmission line required to transform 50 Ω to the optimum load ($R_L = 2/G_n \approx 40\,\Omega$ for the 1N3717 tunnel diode) to obtain the maximum output power should have been employed, and should be considered in future circuit implementations following this approach.

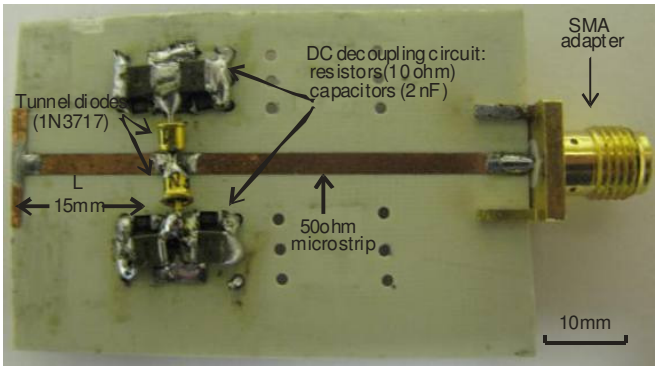

Figure 5.9: A picture of a two tunnel diodes (1N3717) parallel-connected oscillator realized in hybrid microstrip technology.

oscillator circuit. If bias oscillations were present, they would appear as smaller peaks about the fundamental frequency. Simulated output power and frequency for the single tunnel diode oscillator was -9.73 dBm (0.106 mW) and 615 MHz when biased at 180 mV, and -8.97 dBm (0.127 mW) and 627 MHz when biased at 250 mV, respectively.

As may be noted from the selected experimental data given above, the diode was not biased at the point of highest absolute negative differential conductance, approx. at 140 mV on Fig. 3.7b. Previous work by the author [94] had shown that biasing the tunnel diode midway between the peak and valley voltage resulted in the highest RF output power. This is the reason for illustrating the diode performance at the bias voltages of 180 mV and 250 mV, with the latter voltage roughly midway between the peak and valley voltages. The variation of oscillator RF output power with bias will also be given below (for the two-diode oscillator,

Fig. 5.12) and corroborates this observation.

The measured oscillation frequency and output power for the two tunnel diode oscillator were 437 MHz and -7.83 dBm (0.165 mW) respectively (biased at 180 mV, Fig. 5.11), around 2 dB higher than for a single-tunnel diode oscillator. The smaller span spectrum around the fundamental oscillation frequency as shown in Fig. 5.11(b) indicates that no low-frequency bias oscillation occur in the circuit. As earlier noted, if bias oscillations were present they would appear as smaller peaks about the fundamental frequency. The maximum measured output power of -6.5 dBm (0.224 mW) was obtained at the bias point 250 mV which is around the valley of the NDR region (Fig. 3.7(b)), and more than 3 dB higher than for a single tunnel diode oscillator (Fig. 5.10). Fig. 5.13 shows the measured and simulated oscillation frequencies for the two tunnel diode oscillator. For both the single and two-diode oscillators, no low frequency oscillations were detected by the spectrum analyser with bandwidth DC - 50 GHz. Note that oscillator frequency of the two-diode oscillator was lower because of the larger combined device capacitance as indicated earlier. This is a disadvantage of this approach, but high oscillation frequencies can still be attained by reducing the inductance.

Fig. 5.12 and Fig. 5.13 show simulated and experimental output power and frequency of the designed two-tunnel diode oscillator as a function of bias. Overall, good agreement between simulation and experimental results was achieved, and double the RF output power was produced by using two tunnel diodes in a

practical oscillator topology. These experimental results demonstrate that small variations in device characteristics do not affect the circuit performance. This conclusion follows from the fact two commercial tunnel diodes of the same type (1N3717), which invariably would not be identical, were used in the working circuit. It may therefore seem that problems of instability in multiple device oscillators such as in the oscillator topology proposed by Rucker [90] do no affect the oscillator circuit described here.

5.5.1 Oscillator efficiency

Since the stabilising resistance is isolated from the RF signal, it may provide more insight to define the DC-to-RF conversion efficiency for the NDR device separately from that of the complete oscillator circuit in which the DC power consumption of the stabilising resistors is also considered. A single device oscillator draws 1 mA when biased at 180 mV, i.e. DC power consumption of the device of 0.18 mW, and delivers -10.17 dBm (0.096 mW), therefore the *device* DC-to-RF conversion efficiency can calculated to be $(0.096/0.18) \simeq 53\%$. On the other hand, if the complete circuit is considered, the efficiency is expected to drop significantly because of the DC power dissipated in the resistor. At a bias voltage of 180 mV, the power dissipated in the 10-Ω resistor is 3.24 mW. Therefore circuit DC-to-RF conversion efficiency in this case is $(0.096/\left(0.18 + 3.24\right)) \times 100 \simeq 2.8\%$. The *device* efficiency is far better than what is typical of two-terminal NDR device oscillator

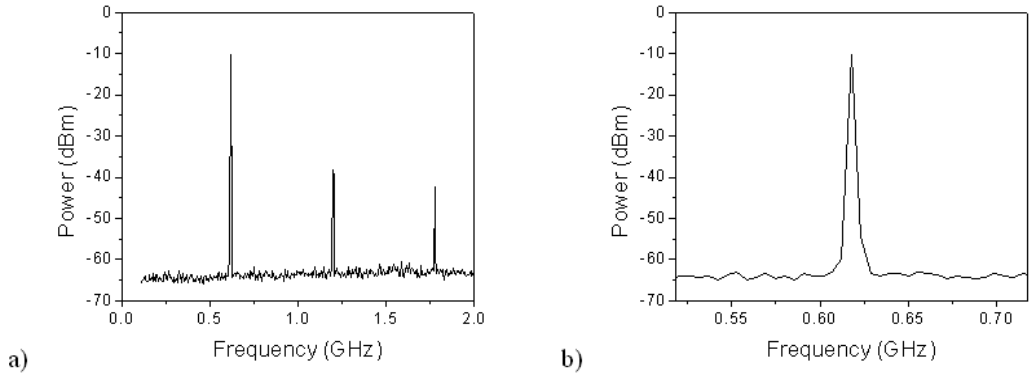

Figure 5.10: a) The measured spectrum of a single tunnel diode oscillator with fundamental oscillations at 618 MHz with -10.17 dBm output power. b)An expanded spectrum of Fig. 5.10(a) around the fundamental oscillations frequency.

circuits though the circuit efficiency is low. This high device efficiency can be attributed to the parallel oscillator topology employed which makes it possible to generate the maximum possible RF power. Therefore, the oscillator design approach demonstrated here could be attractive despite limitations in the overall circuit efficiency imposed by the stabilising resistors

5.6 Discussion

The oscillator topology described in this chapter, both for the single and two-diode oscillator circuits, is a parallel resonant circuit. The total device capacitance of two-diode oscillator circuit is double that of the single diode oscillator circuit, therefore the oscillation frequency of the former circuit is lower than that of the latter if the inductance L as shown in Figs. 5.6 and 5.7 is the same (see Fig.

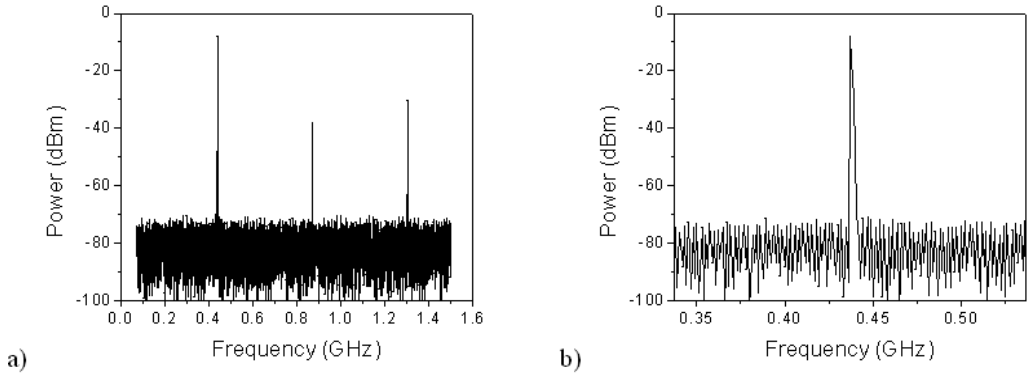

Figure 5.11: a) The measured spectrum of a two tunnel diode parallel-connected oscillator with -7.83 dBm fundamental oscillations at 437 MHz. b) An expanded spectrum of Fig. 5.11(a) around the fundamental oscillations frequency.

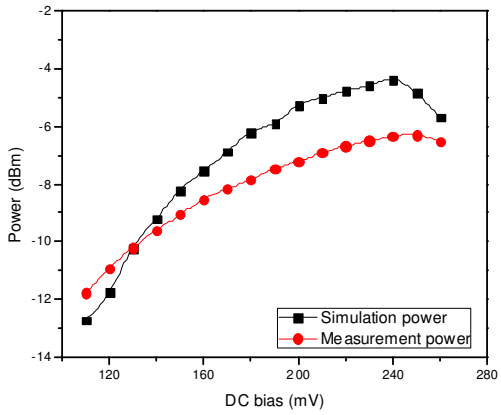

Figure 5.12: The measured and simulated output power of the two tunnel diode parallel-connected oscillator as a function of bias voltage.

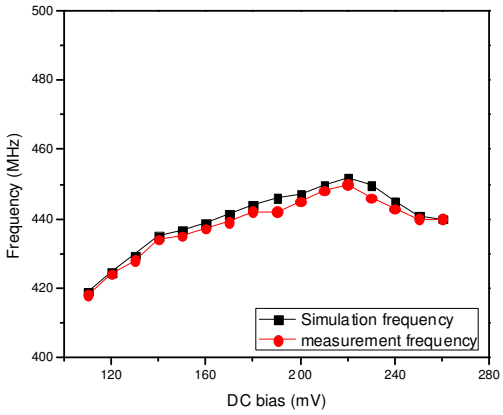

Figure 5.13: The measured and simulated oscillation frequencies of the two tunnel diode parallel-connected oscillator as a function of bias voltage.

5.8 to see how the device capacitances add up). By proper choice of the load resistance the circuits can be designed to deliver the maximum output power ($3\Delta I \Delta V/16$) possible by the NDR device(s) [83], [100]. This way, the maximum DC-to-RF conversion efficiency of an individual NDR device can be achieved. This means that heat dissipation within the device can be significantly reduced. However, since this approach relies on employing a stabilising resistor to eliminate bias oscillations, there is additional heat dissipation (by the resistor) as well as substantial lowering the DC-to-RF conversion efficiency of the oscillator circuit (under 3% for the hybrid circuits described here) due to DC power dissipation by the resistor. The low bias voltages required by tunnel diodes or RTDs ($< 2.5\,V$) mitigate this a little and therefore the absolute power consumption is still low. In the circuit layout, the capacitance C_e can be located between the stabilising

resistance R_e and the RTD to minimise the impact of the power dissipation in the resistor (heating) on RTD performance (similar to the layout in Fig.5.15 [36] shown in the next sub-section).

5.6.1 Comparison to other planar RTD oscillator circuits

An RTD oscillator circuit using a topology similar to Fig. 5.1 is described in Reference [82], [83] in which the inductance L is replaced by a quarter-wave transmission line and the RTD is loaded by a resonator and load. The circuit from Reference [83] is re-drawn in Fig. 5.14 for ease of comparison. A non-linear resistor (Schottky diode) is used for bias stabilisation. As discussed in chapter 1, it is claimed in Ref. [83] that the quarter-wave transmission line acts as an open circuit at the frequency of oscillation. However, from the work described in this chapter, the transmission line and the RTD will form a parallel resonant circuit, i.e. there is no reason why the transmission line should not influence the circuit operation. Therefore the oscillation frequency of this circuit is likely to be lower than the resonance frequency of the load circuit. This observation may explain why the oscillator circuit described in References [82] and [83] designed at 10 GHz worked at 6.9 GHz. The (incorrect) assumption about the transmission line being quarter-wavelength long means that the circuit cannot be designed optimally, i.e. both the oscillation frequency and so impedance matching to the load will be incorrect.

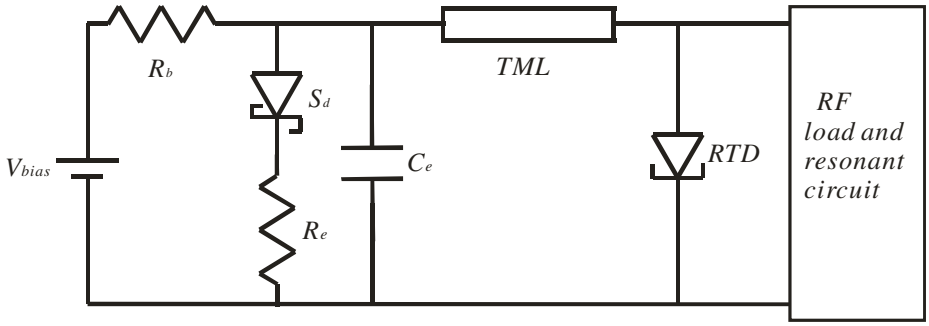

Figure 5.14: Reddy's bias stabilization scheme for sub-mm-wave RTD oscillators. R_b is the resistance of the bias line. S_d, R_e and C_e are the Schottky diode, external resistor and external capacitor, respectively, which form the stabilising circuit. TML is the quarter-wave length transmission line at oscillation frequency [83].

The work of Asada and co-workers [36] also employs a stabilising resistor to eliminate low-frequency bias oscillations. Figures 5.15 and 5.16 show an illustration of the fabricated structure of an RTD oscillator integrated with slot antenna and its equivalent circuit, respectively [36]. The RTD is located at the centre of the slot. The electrodes of the RTD are connected to the left and right electrodes of the antenna. At both edges of the antenna, the electrodes are overlapped with a $SiO_{\mathbf{2}}$ layer between them forming a metal-insulator-metal (MIM) capacitor across which a stabilising resistor is connected. The equivalent circuit of this oscillator is identical to that of Figure 5.1. The oscillation frequency is determined by the parallel resonance of L and C (Fig.5.16), where the inductance L is produced by the antenna (corresponding to L in Fig.5.1) and the capacitance C produced by the RTD and the antenna. The $SiO_{\mathbf{2}}$ MIM capacitor plays the same role as $C_{\mathbf{e}}$ in

Fig. 5.1. The antenna inductance L could also be viewed as the inductance of the metallisation (connection) between C_e and the RTD, and looking at it this way the circuit is identical to that shown in Fig. 5.1. Note that at millimetre-waves and THz frequencies, the circuit of Fig. 5.14 is identical to that in Fig. 5.15 [76]. Thus the suitability of the resistor stabilisation technique for RTD oscillators has been demonstrated at the highest frequencies (despite the reducing circuit size) [36], [83].

The circuits by Asada [36] and Rodwell [83] can only employ one RTD device in a single oscillator circuit. Therefore, only spatial and not circuit based power combining techniques are possible with these circuits. In spatial power combining, arrays of individually oscillators, each with its own antenna, are used to achieve higher emitted output power. Using arrays has implications on circuit size as antenna size is approximately half a wavelength and so only very higher frequency oscillators can be implemented in this way. Indeed, to date RTD oscillators employing arrays have been implemented at 330 GHz for two oscillators [36] and 650 GHz [76]. Note also that, spatial power combining is not useful in a case where higher oscillator power is required to, for instance, drive a mixer stage. But the real downside of the integrated planar oscillators proposed by Asada [36] and Rodwell [83] is the poor impedance matching to the slot antenna. The input impedance of a slot antenna at the centre of the slot is infinity and therefore mounting the RTD in this location as done in the work described in Refs. [36],

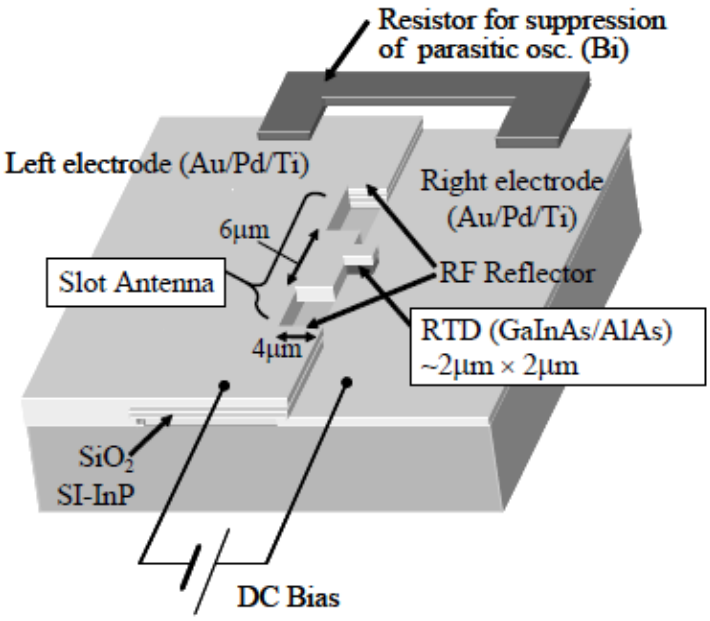

Figure 5.15: A planar resistor-stabilised millimetre-wave and THz RTD oscillator integrated with a slot antenna load [36].

[83] invariably results in impedance mismatch. This may explain the very low efficiencies achieved by the published circuits.

In contrast to the Rodwell and Asada circuits, the oscillator topology developed here can employ more than one RTD. Impedance matching to, for instance, a coplanar waveguide (CPW) fed slot antenna load can be easily realised for an oscillator employing two RTDs. Thus, the new oscillator circuits described in this chapter can be realised as monolithic microwave integrated circuit (MMIC) using RTDs. An illustration of a CPW RTD oscillator circuit is described in the section 9.2 on future work.

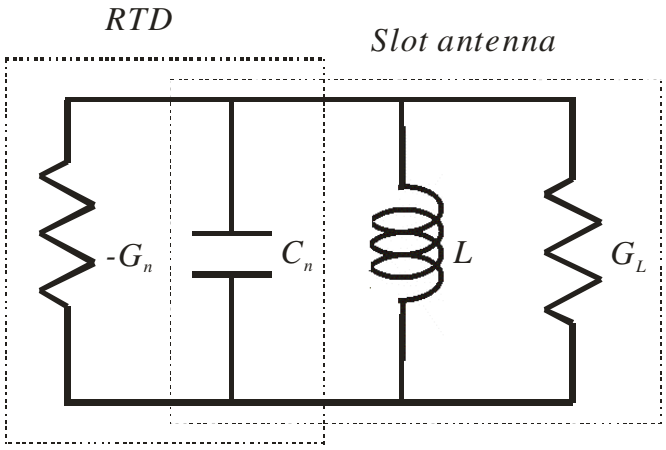

Figure 5.16: RF equivalent circuit of Figure 5.15 [36].

5.7 Summary

A criterion for designing sinusoidal tunnel diode oscillators was derived in this chapter. Further, an oscillator topology employing two tunnel diodes for higher output power was proposed and experimentally verified. The circuit used parallel resonant circuit topology making it possible to design oscillators delivering close to the theoretical output powers, but at the cost of high DC consumption by the stabilising resistors. It is expected that RTD based oscillators could employ the same design methodology as described in this chapter for better performance, i.e. high output power at the design frequency.

CHAPTER 6

SERIES INTEGRATION OF TUNNEL DIODES

6.1 Introduction

Besides the parallel oscillator design method discussed in Chapter 5, there may be another method for power combining which is by connecting several NDR devices in series. Series device integration is known to have the potential to suppress the spurious oscillations and enhance the output power at RF and millimetre wave frequencies [89], [109]. According to the theoretical analysis by Yang et al, 10 series integrated RTDs can theoretically provide 20 dBm (100mW) at 100 GHz [89]. The analysis assumes that all the RTDs are biased in their NDR regions and that the DC instability problems of this configuration are overcome. In practice, however, a circuit using several NDR devices connected in series suffers from severe DC instability [44], [45].

Theoretically, series connected NDR devices can behave like a single NDR device with an *I-V* characteristic that is similar to the one of a single NDR device, but one which is stretched by N times along the voltage axis, and its capacitance is N times smaller than the one of a single NDR device [109], [110]. Therefore N times more output power for an oscillator realised from such series connected

devices can be expected. The combined capacitance reduces which on its own would increase the device cut-off frequency. However, the contact resistance will increase with the number of devices which would limit the device cut-off frequency (see e.g. equation 8.28 in chapter 8 for variation of cut-off frequency with device parameters).

Series-connected tunnel diodes have been employed in oscillator circuits [44], [45]. The main problem is the DC instability whereby it is not possible to simultaneously bias the tunnel diodes or RTDs in the NDR region. Previously proposed solutions to this biasing problem include fast electric pulse excitation [89] and RF excitation [44], [45], but both techniques are involving and only RF excitation has been experimentally validated for two tunnel diodes [45]. Due to the lack of suitable trigger sources, pulse excitation has, to date, not yet been experimentally demonstrated. In this chapter, a new method of achieving DC stability of series connected tunnel diodes will be described. A possible oscillator topology which utilises this method was investigated and will be described.

6.2 DC stability of series connected tunnel diodes

Fig. 6.1 shows the topology of two NDR devices connected in series. In order to obtain higher output power in an oscillator circuit, both of the NDR devices are expected to be biased in the NDR region. Therefore, the ideally combined I-V characteristic is expected as shown in Fig. 6.2(b), in which the I-V

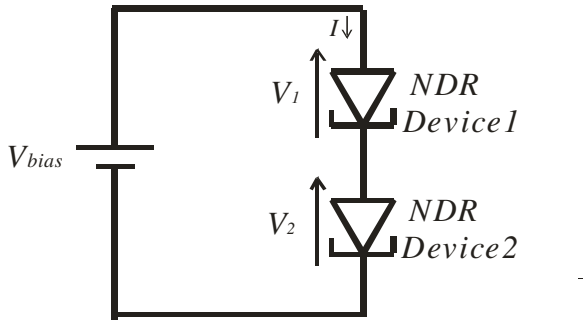

Figure 6.1: A diagram of two NDR devices connected in series

characteristic is stretched by 2 times along the voltage axis compared to that of single NDR device (1N3717, Fig. 6.2(a)). Fig. 6.2(c) is the simulated I-V for 5 series connected NDR devices, in which the I-V characteristic is stretched by 5 times along the voltage axis compared to that of single NDR device. Here it is assumed that the devices are identical and the voltage division between them is the same. The I-V characteristic of a single device is from measured data of the 1N3717 tunnel diode. The combined characteristic is easily generated using MATLAB or ADS software.

In practice, however, due to DC instability, it is difficult to bias both devices in the NDR region simultaneously [44], [45]. Fig. 6.3 shows the measured I-V characteristic of two NDR devices (1N3717) connected in series. The bias voltage is not evenly split between the devices but it is divided such that either one or both of the devices are in the positive differential resistance (PDR) region [44], [89]. This behaviour is captured by the measurement shown in Fig. 6.4 which shows the voltages across each individual tunnel diode versus the DC bias. These

measurements show that either one or both diodes are in the positive PDR region for all bias points. Clearly, without the devices being biased in their NDR regions no oscillator design would be possible.

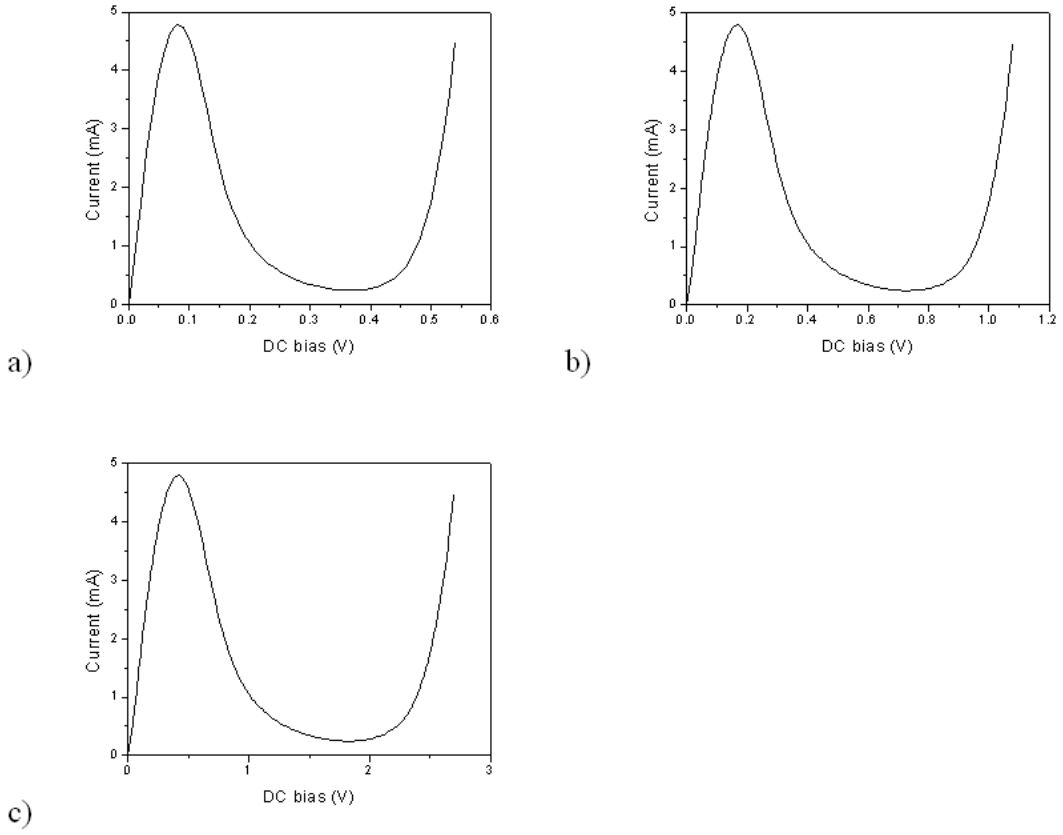

Figure 6.2: a) Measured I-V characteristic of single NDR device (1N3717), b) Simulated ideal I-V characteristic of 2 NDR devices (1N3717) connected in series, c) Simulated ideal I-V characteristic of 5 NDR devices (1N3717) connected in series. Note that in b) and c), the voltage is expanded by 2 and 5 times, respectively, compared to the single device.

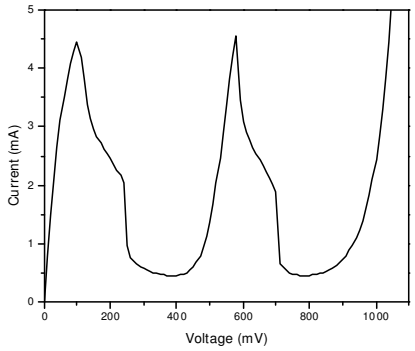

Figure 6.3: Measured I-V characteristics of two NDR devices (1N3717) connected in series. The I-V characteristic is not stretched along the voltage axis as expected due to DC instability.

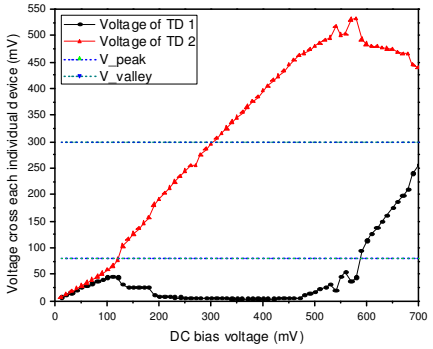

Figure 6.4: Measured voltages across two individual tunnel diodes (1N3717) in the series integration as shown in Fig. 6.1. The voltage range between two dashed lines V_peak and V_valley is the NDR region for a single device. It shows that the bias voltage is not evenly split between the two devices but is divided such that either one or both of the devices are in the positive differential resistance (PDR) region.

6.2.1 Analytical model for the tunnel diode

In order to investigate the DC instability problem, the measured I-V curve of the tunnel diode (1N3717) was modelled using a ninth-order polynomial fit. The 9th order polynomial is used to replace the cubic polynomial used in chapter 2 and 3, and the table-based model in chapter 5. The analysis in chapters 2 and 3 focussed mainly on the NDR region of the tunnel diode and the cubic polynomial (with the origin shifted to the middle of the NDR region) was adequate for this. For the analysis of the DC instability of series-connected tunnel diodes, a good model for both the NDR and PDR regions is required and therefore a higher order polynomial must be used.

A curve fitting tool in MATLAB, *cftool*, employing the method of least squares was used to generate the 9th order polynomial fit for the I-V characteristic of the NDR device (1N3717). The model could be expressed as

$$I(V) = k_0 + k_1 V + k_2 V^2 + k_3 V^3 + k_4 V^4 + k_5 V^5 + k_6 V^6 + k_7 V^7 + k_8 V^8 + k_9 V^9 \quad (6.1)$$

where k_0 to k_9 are the polynomial coefficients. To determine the model, i.e. the coefficients k_0 to k_9, with the *cftool* the order of the polynomial and the measured data are required. With this information, the constants k_0 to k_9 (for a 9th order polynomial) are determined from the sum of squares of the difference between the measured and modelled currents using the method of least squares [111], [112]. To find the least square error, the sum of the squares of the differences between the

polynomial fit and the actually data must be evaluated. Specifically, the quantity

$$Error = \left(\frac{1}{n} \sum_{k=1}^{n} |I(V_k) - y_k|^2 \right)^{1/2} \tag{6.2}$$

is calculated where y_k is the measured data (n data points) and $I(V_k)$ is the modelled data (equation (6.1)). To solve this equation for the unknown coefficients k_0 to k_9, a system of simultaneous linear equations in the ten unknowns is generated. Because the least-squares fitting process minimizes the summed square of the residuals, the coefficients are determined by differentiating $S\,(= n * Error^2)$ with respect to each parameter, and setting the result equal to zero. This way, the coefficients k_0 to k_9 can be estimated analytically [111], [112]. Equation (6.2) also provides a quick and easy calculation which allows for an evaluation of the fitting procedure. In general, the error will continue to drop as the degree of polynomial is increased. This is because every extra degree of freedom allows for a better least-squares fit to the data. The measured and calculated/simulated I-V curves of the 1N3717 tunnel diode are shown in Fig. 6.5b. The following coefficients were determined: $k_0 = 0.1134$, $k_1 = 0.0607$, $k_2 = 0.0018$, $k_3 = -4.49 \times 10^{-5}$, $k_4 = 3.866 \times 10^{-7}$, $k_5 = -1.756 \times 10^{-9}$, $k_6 = 4.66 \times 10^{-12}$, $k_7 = -7.275 \times 10^{-15}$, $k_8 = 6.201 \times 10^{-18}$, $k_9 = -2.227 \times 10^{-21}$. The error between measured and calculated currents was 0.01. This error may be reduced as noted above by using a higher order polynomial fit but the fit by the 9th order polynomial was deemed good (visually).

It may be worthy to note here that lower-order polynomials were first tried

to fit the measured I-V but were found to be less accurate. This is illustrated in Fig. 6.5(a) that shows that an eighth-order polynomial does not fit the data in the 280 - 500 mV bias voltage range. The error for of 8th polynomial was 0.0877, while for the 9th polynomial was 0.0096. The ninth-order polynomial fit as shown in Fig. 6.5(b) produced a far better (visually) fit to the measured I-V characteristic across the whole bias range. The measured I-V characteristic was therefore modelled by equation (6.1).

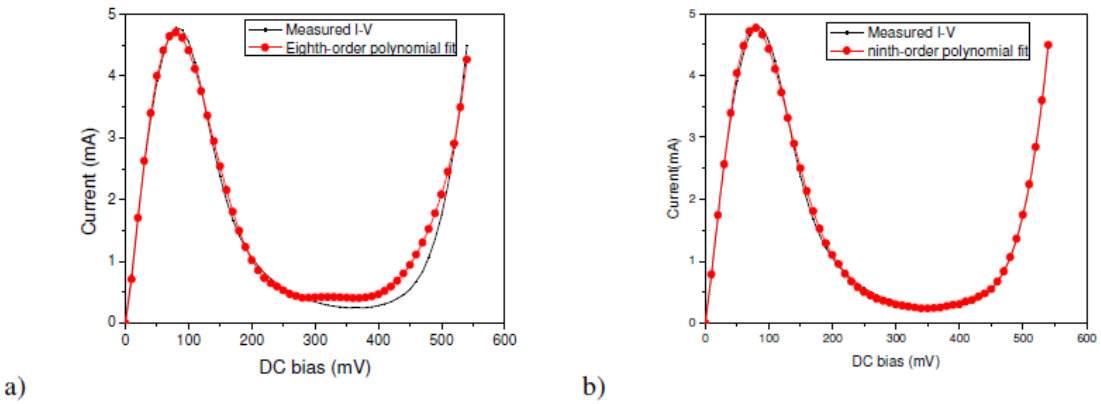

Figure 6.5: a) Measured I-V characteristic (continuous trace) of the tunnel diode (1N3717) and an eighth-order polynomial fit (dotted trace). b) Measured I-V characteristic of the tunnel diode (1N3717) and a ninth-order polynomial fit.

6.2.2 Analysis of DC stability of series connected tunnel diodes

6.2.2.1 Theoretical analysis

The analysis presented here assumes that the individual devices are identical. The circuit with two NDR devices in series (Fig. 6.1) can be described by

$$I(V_1) = I(V_2) \tag{6.3}$$

$$V_1 + V_2 = V_{bias} \tag{6.4}$$

where I is the current through the NDR devices 1 and 2, V_1 is the voltage across the NDR device 1 and V_2 is the voltage across the NDR device 2.

There can be more than one solution for V_1 and V_2 for equations (6.1), (6.3) and (6.4). For example, the circuit as shown in Fig. 6.1 was biased at 340 mV. From equations (6.1), (6.3) and (6.4), there are only three solutions for V_1 and V_2 ($V_1 = 3\ mV, V_2 = 337\ mV$, $V_1 = 337\ mV, V_2 = 3\ mV$ or $V_1 = 170\ mV, V_2 = 170\ mV$). The desired solution would be to have both devices biased in their NDR regions, i.e. $V_1 = 170\ mV, V_2 = 170\ mV$. The measurement results (Figs. 6.3 and 6.4) however show that the NDR devices prefer being biased such that one device is in the PDR region and the other in NDR region. DC instability causes the bias voltage not to be evenly split between the devices if it is applied gradually, although the DC bias voltage is sufficient to bias both NDR devices in their NDR regions [89], [109].

Consider equations (6.1), (6.3) and (6.4) again: it may be possible to si-

multaneously bias both of the diodes in their NDR regions if an external biasing network is introduced such that solutions $V_1 = 3\ mV, V_2 = 337\ mV$ or $V_1 = 337\ mV, V_2 = 3\ mV$ are not possible and that the only possible solution is $V_1 = 170\ mV, V_2 = 170\ mV$. That is, external circuit conditions are introduced such that the possible solutions to equations (6.1), (6.3), (6.4) for V_1 and V_2 are only in the NDR region.

In order to bias all of the NDR devices in the NDR region, external stabilizing resistors (R_e) were introduced into the series integration circuit and the external inductors (L_e, the interconnection between the tunnel diodes and the external resistors) are used to connect the external resistors (R_e) and the NDR devices as shown in Fig. 6.6. Consider two NDR devices of the N-order series integration as shown in Fig. 6.6(b). If $I_{NDR\_device1}$ and $I_{NDR\_device2}$ are the currents going through the NDR devices 1 and 2, V_1 and V_2 are the voltages across the NDR devices 1 and 2, respectively, with $V_2 > V_1$ then applying Kirchoff's current law at the node between devices 1 and 2 gives:

$$I_{NDR\_device1} = I_{NDR\_device2} + \frac{V_2 - V_1}{R_e} \tag{6.5}$$

Now assume that the two series-connected NDR devices are biased at $2 \times V_{NDR}$, where V_{NDR} is any voltage point within the NDR region of a single device. In this case, it is impossible to bias both devices either in the first PDR regions (the total voltage across the NDR devices will be less than the bias voltage) or both of them in the second PDR regions (the total voltage across the NDR devices

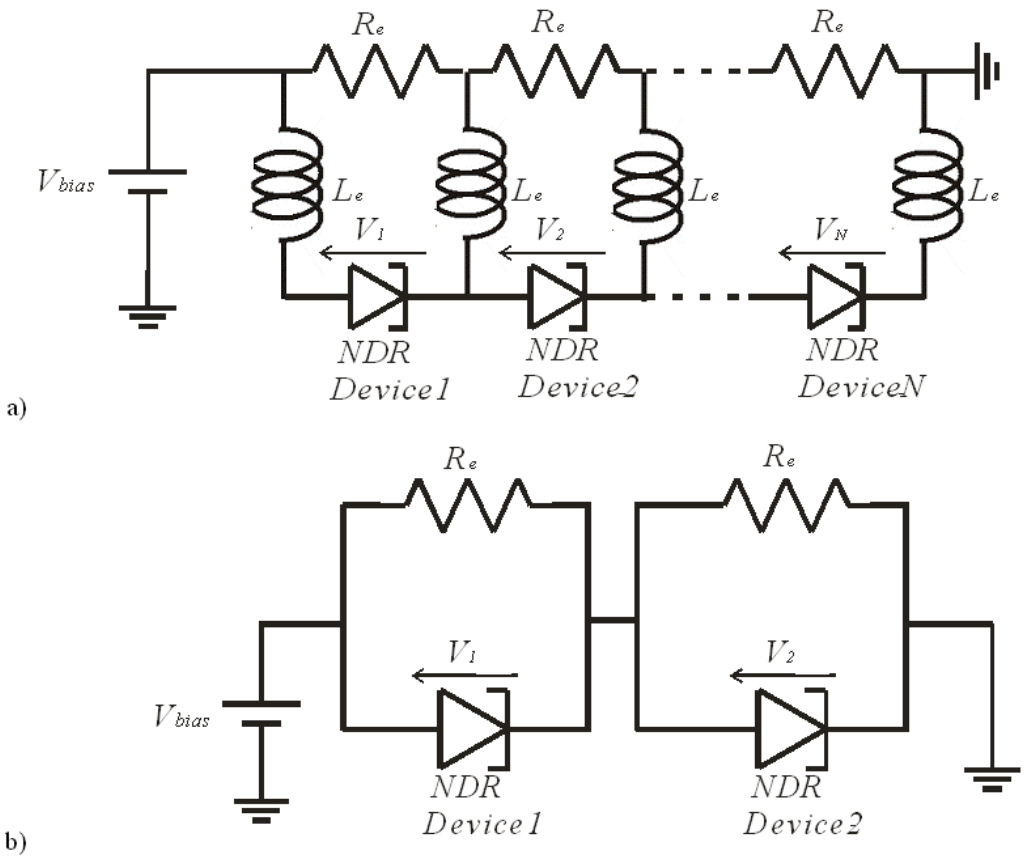

Figure 6.6: a) Circuit diagram of the series integration of N NDR devices and external stabilizing resistors (R_e) that are connected to the NDR devices through external inductors (L_e), b) Two series-connected NDR devices with external stabilising resistors (R_e).

will greater than the bias voltage). Therefore, one of the diodes will be biased in the first PDR region while the other one will be biased in the second PDR region or vice versa. This behaviour has been experimentally verified, e.g. Fig. 6.4, in which device 1 in the first PDR region while device 2 in the second PDR region. Therefore the minimum voltage difference $|V_2\text{-}V_1|$ is the peak to valley voltage difference (ΔV) of the I-V characteristic of the NDR device.

Equation (6.5) shows that voltage difference $|V_2\text{-}V_1|$ depends on the values of resistor R_e and that the current goes through the NDR device 1, $I_{NDR\_device1}$, must be greater than the one that goes through the NDR device 2, $I_{NDR\_device2}$. Therefore the maximum current difference ($I_{NDR\_device1}$ - $I_{NDR\_device2}$) is the peak to valley current difference (ΔI) of the I-V characteristic of the NDR device. This means that to avoid biasing the NDR devices such that one of them is biased in the first PDR region and the other in the second PDR region, then the condition below must be satisfied

$$\Delta I \times R_e < \Delta V \tag{6.6}$$

i.e. the maximum voltage drop across the stabilising resistor for the second device ($\Delta I \times R_e$) should be such that V_2 cannot possibly be in the second PDR region. This way, at least one of the devices will be biased in the NDR region. Therefore, R_e could be chosen as

$$R_e < \frac{\Delta V}{\Delta I} \tag{6.7}$$

In this case, it is possible that the other device is biased either in the first or second

PDR region. To guarantee that both devices are biased in their NDR regions, a more detailed analysis is required.

Now consider the case when the bias voltage is changed to 2 $\times V_{NDR\_M}$, where V_{NDR_M} is the bias point at the middle of the NDR region of a single device. In this case, one of the devices will be biased in the NDR region while the other in either the first or second PDR region as illustrated in Fig. 6.7. For instance, if device 1 is in the NDR region and $V_1 > V_{NDR\_M}$ then device 2 will be biased in the first PDR region if it is also not in the NDR region (Fig. 6.7(a)). On the other hand, if device 1 is in the NDR region and $V_1 < V_{NDR\_M}$ then device 2 will be biased in the second PDR region if it is also not in the NDR region (Fig. 6.7(b)).

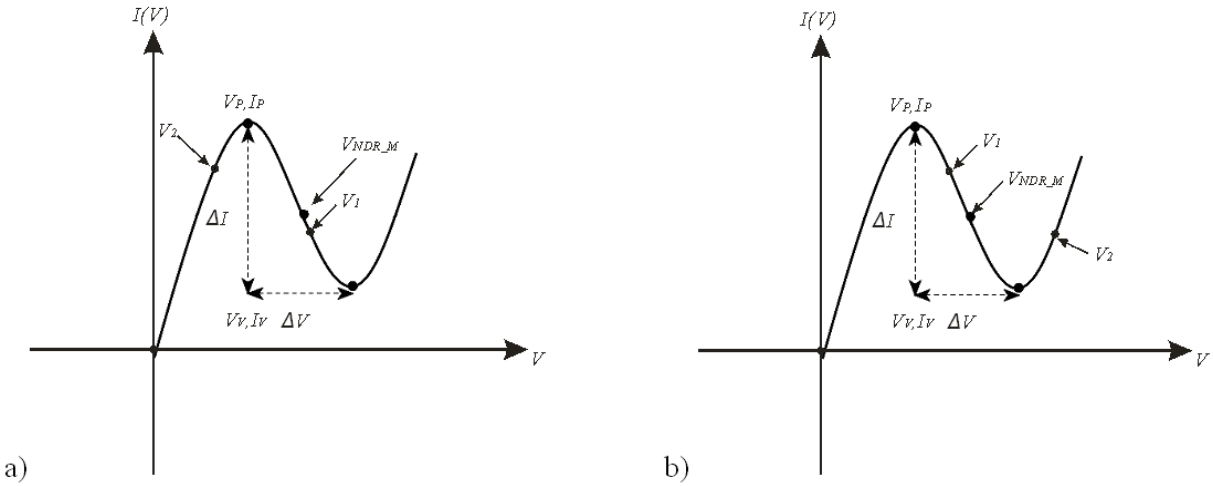

Figure 6.7: Possible bias points for two series-connected NDR devices having a bias supply capable of biasing both in the mid-points of the NDR regions. a) $V_1 > V_{NDR\_M}$ b) $V_1 < V_{NDR\_M}$.

Therefore the minimum voltage difference dropped across the devices, $|V_2$ -

$V_1|$, is $\Delta V/2$ and the maximum current difference is ΔI. Thus to ensure that both devices are biased in their NDR regions, the stabilising resistance must satisfy

$$R_e < \frac{\Delta V}{2\Delta I} \tag{6.8}$$

Finally, having biased both devices in their NDR regions, it is now desirable to have both devices with the same DC bias point, i.e $V_2 = V_1$. Now assume that $V_2 > V_1$. In this case the condition in equation (6.5) should be satisfied, i.e.

$$R_e = \frac{V_2 - V_1}{I_{NDR\_device1} - I_{NDR\_device2}} \tag{6.9}$$

Equation (6.9) gives the value of the resistance R_e which actually corresponds to the slope of the NDR region since both voltages and both currents are within this region. Therefore if the R_e is chosen smaller than the minimum value of the negative differential resistance, then equation (6.9) cannot be satisfied. The only possible solution in this case is for both NDR devices to be at identical points within the NDR region, with the same current flowing through both NDR devices. In summary, the stabilising resistance R_e should therefore be chosen such that

$$R_e < R_{n\_Min} \tag{6.10}$$

where R_{n_Min} ($= 1/G_n \approx 22\ \Omega$ for the 1N3717 tunnel diode) is the minimum absolute value of negative differential resistance in the NDR region.

6.2.2.2 Experimental results

Fig. 6.8 shows the measured voltages across each of the two tunnel diodes (1N3717) connected in series. The resistor R_e was set to 10 Ω according to equation (6.10), with $R_{n\_Min} \approx 22\ \Omega$. The results show that both of the tunnel diodes were biased in the NDR region when the DC bias was sufficient to bias them in the NDR region. The bias voltages across the NDR regions were almost identical and not just at the mid-point of the NDR region. Thus, with the proposed scheme, series connected NDR devices can be biased at identical bias points along their *I-V* characteristics even within their NDR regions.

The *I-V* characteristics of the series connected devices can be extracted from the measurements by subtracting the current through the stabilising resistors. Fig. 6.9 shows that extracted/measured *I-V* characteristics of 2 and 5 tunnel diodes (1N3717) connected in series, respectively. As expected the characteristics are expanded on the voltage axis by 2 and 5 times, respectively, while the current through them is the same as for a single tunnel diode. It is also clear from Fig.6.9 that there were oscillations present during the measurement - this is not surprising because of the existing negative differential resistance region. Note that the resistors in the circuit of Fig. 6.6 are for ensuring an equal split of the DC voltage between individual devices and not for suppressing an RF oscillations that may be present due to the negative differential resistance. Note also that since the two/five diodes are only nominally identical (as they are of the same type),

the experimental results suggest that the procedure described here is robust.

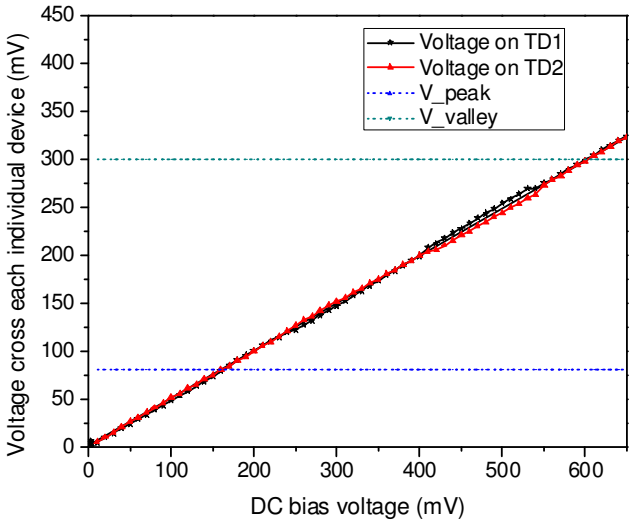

Figure 6.8: Measured voltages across two individual tunnel diodes (1N3717) in the series integration as shown in Fig. 6.6(b). The measurements show that the bias voltage is almost evenly split between the two devices.

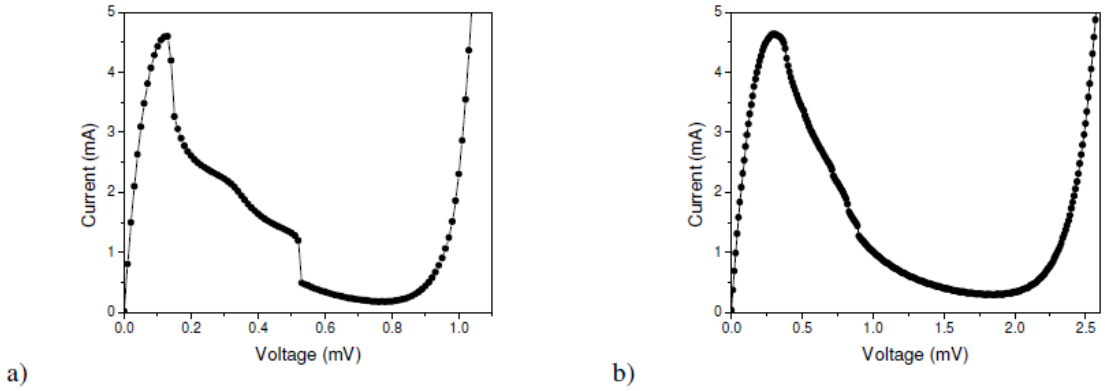

Figure 6.9: Extracted I-V characteristics of a) 2 and b) 5 tunnel diodes (1N3717) connected in series. Compared to the I-V characteristics of a single device as shown in Fig. 3.7(b), the voltage axis is expanded 2 and 5 times, respectively.

6.3 Oscillator design with series connected tunnel diodes

Having established how to bias all the series connected tunnel diodes in their NDR regions as described in the previous section (albeit with oscillations present), a suitable oscillator topology is needed to utilise this. One topology investigated was based on the extended resonance technique [113]-[115]. Fig. 6.10 shows a NDR device based oscillator circuit using extended resonance power combining. Capacitors C_{block} are short circuits at the expected frequency of oscillation. The admittance of the each device is assumed to be Y_1 = -G_{n1} + jB_1. The length of the transmission line (TML1) can be chosen such that the admittance of the first device is transformed to only its conductance, namely -G_{n1}. After adding the second device, the total admittance seen by looking at the terminal of second device is Y_2 = -G_{n2}+ jB_2. The length of transmission line 2 (TML2) can now be

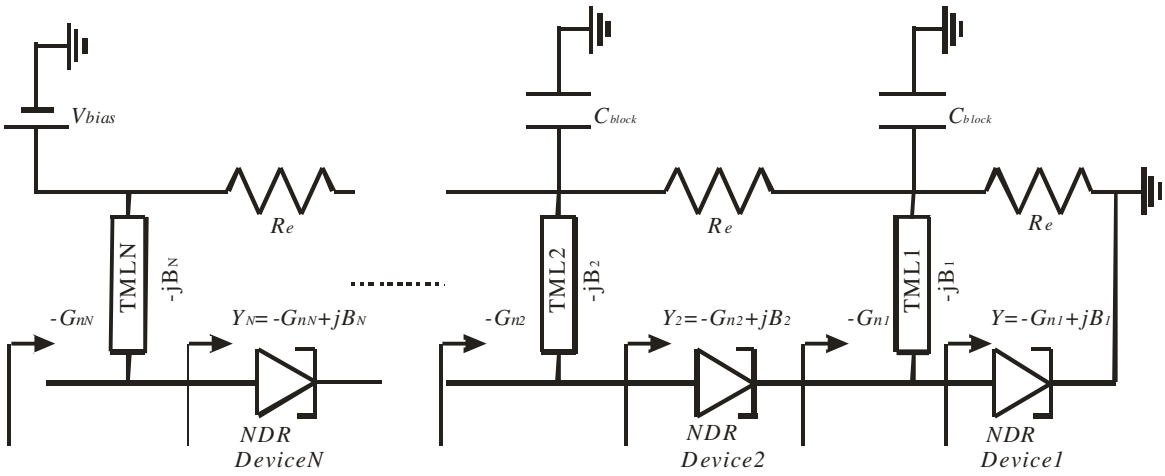

Figure 6.10: An extended resonance power combining circuit topology with N NDR devices connected in series. TML are transmission lines.

chosen to convert Y_2 = -G_{n2} + jB_2 to -G_{n2}. This process is repeated N times. Finally, the admittance seen at the terminals of the Nth device is -G_{nN}. Then a load network is selected to connect to that point and the oscillator design is completed.

To verify this design method, the circuit of Fig. 6.10 was simulated in ADS using *Harmonic Balance*[1] analysis for three 1N3717 tunnel diodes connected in series. The admittance of the single device biased at 170 mV is $-0.0025 + j0.082\ S$ at 800 MHz. Therefore the length of the transmission line (TML1) can be chosen such that the admittance of the first device is transformed to only its conductance, namely $-0.0025\ S$. The length of the transmission line can be determined by the

[1]In this simulation, the non-linear devices are simulated in the time domain while all the passive circuitry is simulated in the frequency domain. Convergence is achieved when the terminal voltages and current of the non-linear devices (after being converted to frequency domain) equal the terminal voltages and currents of the passive circuitry at common terminal points.

equation (6.11) [107], [116]

$$G_{TML} = j\frac{1}{Z_0}\cot(\beta l) \tag{6.11}$$

where, Z_0 is the characteristic impedance of the transmission line, β is the wave coefficient, $\beta = 2\pi/\lambda$ (λ is the wave length of the signal), and l is the length of the transmission line.

In the simulation, an ideal transmission line with 50-Ω characteristic impedance was employed in the circuit, and three resistors are used for DC stability components. 3 nF capacitors are used for the RF short circuits. According to the method discussed above, the electrical lengths of the transmission lines are calculated as 39.8°, 73.3° and 81.5°. The Harmonic Balance simulation results are shown in Fig. 6.11 which show that the circuit should work at the design frequency of 800 MHz with an output power of -4.259 dBm.

6.3.1 Experimental results

To test the simulated results, three 1N3717 tunnel diodes were used in the circuit design and implementation. The load resistance was fixed to 50 Ω. The circuit of the three tunnel diodes oscillator was realised in microstrip hybrid technology using a microwave substrate with a dielectric constant of 3.48 and thickness of 0.762 mm as shown in Fig. 6.12. Three 50-Ω microstrip lines with lengths 20.13 mm, 37.08 mm and 41.22 mm were used to realise the transmission lines in the circuit, and so the design oscillation frequency was to be around 800 MHz from

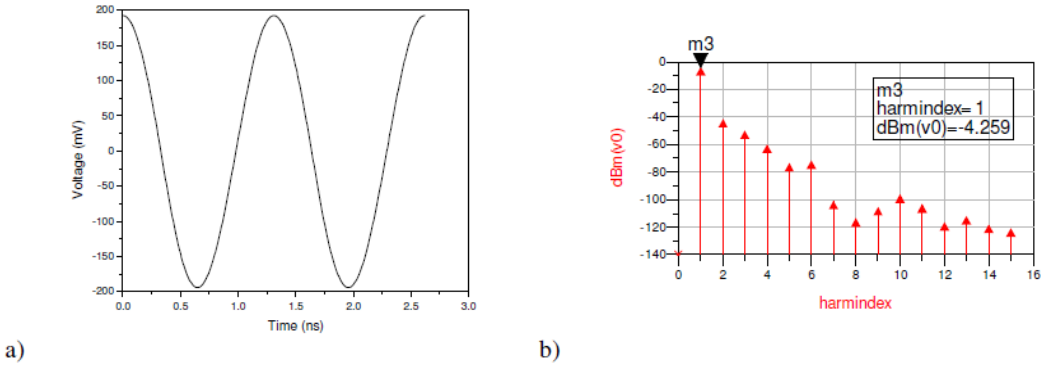

Figure 6.11: Harmonic Balance simulation results for an oscillator with 3 tunnel diodes connected in series using the extended resonance technique. (a) Time domain signal of the voltage across the 50-Ω load. (b) The spectrum of the voltage obtained using a in-built function "fs" in ADS shows an output power of -4.259 dBm at the fundamental frequency.

Harmonic Balance analysis. The n-shaped microstrip lines were used to realise 41.22 mm (on the top in Fig. 6.12) and 37.08 mm (in the middle in Fig. 6.12) for the circuit layout to work. These two microstrip lines were designed and modified to have the same electrical characteristics as that of the microstrip lines with 41.22 mm and 37.08 mm length at desired frequency (800 MHz). ADS has models for all the microstrip discontinuities e.g. the 90-degree bends, T-junctions etc. Three 10-Ω resistors were used to ensure equal splitting of the applied bias across the three diodes in their NDR regions, and three 3 nF capacitor were used as the RF short circuits. At the output, a 50-Ω microstrip line was used to connect to the 50-Ω cable that connected to the spectrum analyser.

The DC bias voltage was supplied by a TTi QL355 power supply. The waveform of the output signal was measured by an Agilent mixed signal oscilloscope MSO6104A and the spectrum of the output signal was measured by Agilent RF spectrum analyser E4448A. The waveform and the spectrum of the output signal are shown in Fig. 6.13 and Fig. 6.14, respectively. Clearly, the circuit did not work as predicted by the Harmonic Balance simulation results and so further investigation into the operation of this circuit was done.

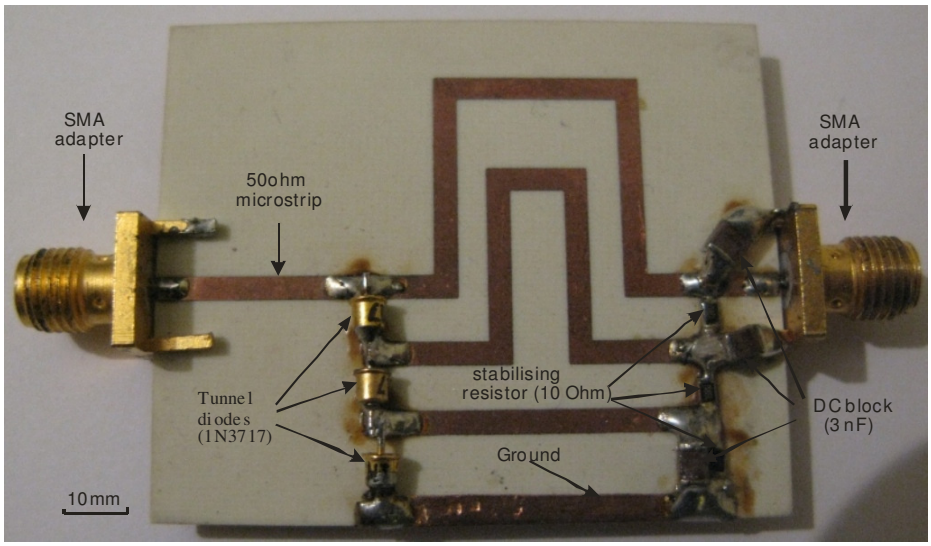

Figure 6.12: A picture of the three series-connected tunnel diodes (1N3717) oscillator realised in hybrid microstrip technology.

6.3.2 Time domain simulations

It is important to point out here that the practical circuit implementation was carried out on the basis of the design done by Harmonic Balance (HB) simulations

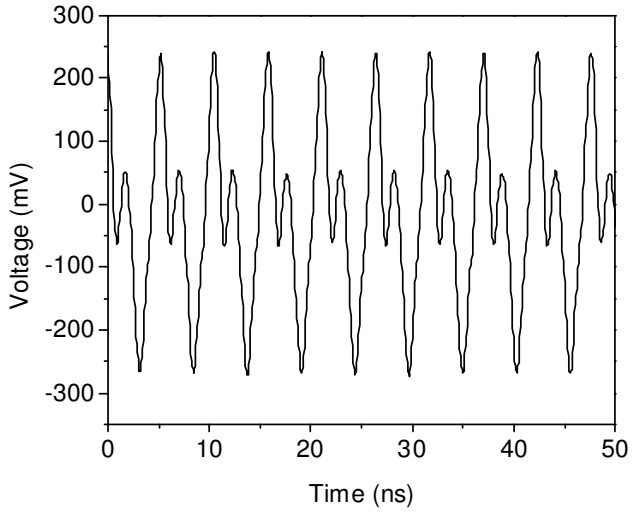

Figure 6.13: Measured waveform of the three series-connected tunnel diodes (1N3717) oscillator.

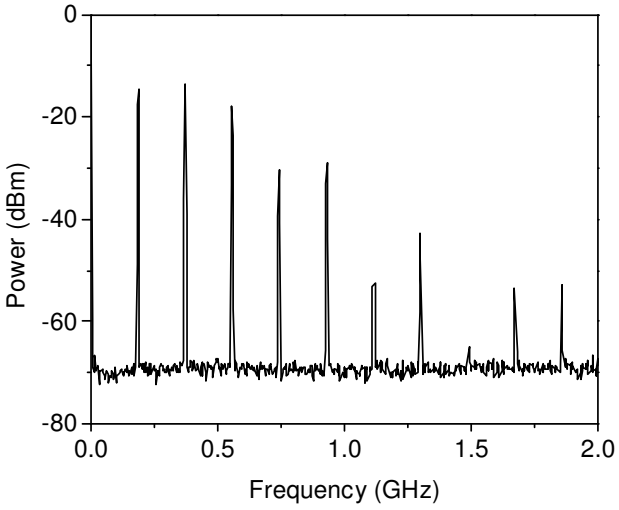

Figure 6.14: Measured spectrum of the three series-connected tunnel diodes (1N3717) oscillator.

alone. As the experimental results were different from theoretical Harmonic Balance predictions, further investigation into the circuit operation was carried out. In particular, time domain simulations were carried out on the designed circuit in an attempt to understand its operation. Fig. 6.15 shows the transient/time domain simulation results and the corresponding signal spectrum of the output voltage of the designed circuit. The results show that the circuit should oscillate at ∼250 MHz and the oscillation amplitude varied - more or less as in the experimental results. Note that in Harmonic Balance analysis, an estimate of the frequency is required to run the simulation and therefore using the Harmonic Balance tool alone, the lower frequencies of oscillation could be predicted.

The observed circuit operation, both experimentally and from time domain simulations, indicates that maybe the transmission lines behaved as lumped elements (inductances) in this circuit and therefore caused low-frequency oscillations. It is well known that time domain simulators solve differential equations describing any given circuit [105], [117]. It is also known that a transmission line cannot be described by differential equations and so equivalent circuit approximations are made if it is used in the simulation [105]. Nonetheless, attempts to optimise the design on the basis of time domain simulations did not reveal any useful design methodology to achieve single frequency oscillations and so this approach to possible power combining was not explored further.

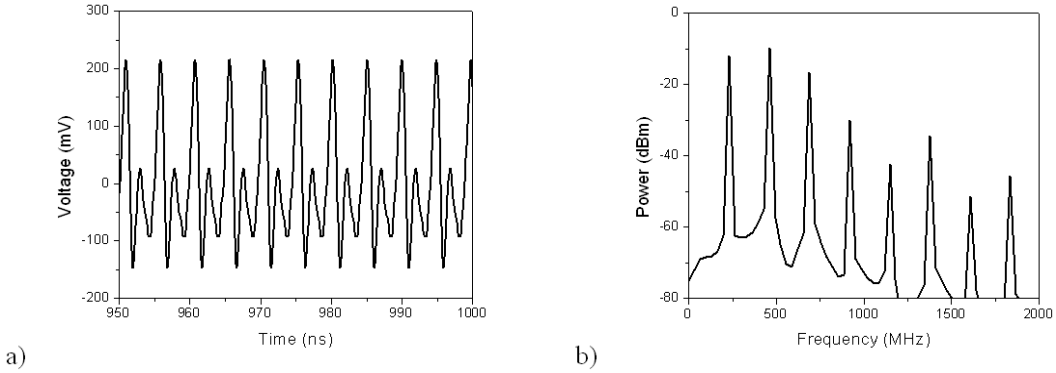

Figure 6.15: Transient/time domain simulation results for oscillator with three tunnel diodes connected in series using the extended resonance technique. (a) Time domain signal of the voltage across the 50-Ω load. (b) The spectrum of the voltage across the 50 Ω load obtained using a in-built "fs" function in ADS.

6.4 Summary

A new method to suppress DC instability of the NDR devices connected in series with all the devices biased in their NDR regions was investigated. It was successfully employed for DC characterisation with integrations of two and five tunnel diodes connected in series. The measured I-V characteristics exhibited the typical "chair-like" signature for bias oscillations when the devices were biased in the NDR region. Note that the resistors used in the circuit were for ensuring equal splitting of the DC voltages between the series-connected devices and were not for suppressing any RF oscillations that may be present due to the negative differential resistance. Low frequency oscillations seemed to reduce with the number of series integrated tunnel diodes (see Fig.6.9). For an increasing number of diodes, the

effective conductance in the NDR region reduces making stability easier to achieve.

Experimental results for oscillators designed using the extended resonance technique were different from predictions by Harmonic Balance analysis. They were, however, similar to predictions by time domain simulations. The measured output signal was non-sinusoidal and very similar to the simulation in Fig. 6.15(a). It would seem that the transmission lines may have behaved as equivalent inductances, with each inductance and tunnel diode producing an oscillation. This is not surprising since time domain simulators, e.g. SPICE simulator, solve differential equations governing the circuit. Transmission lines being distributed elements cannot be analysed this way and are therefore approximated by equivalent inductances [117]. The discrepancy between the measured and simulated time domain signals can be attributed to the inaccurate device model, e.g. the device capacitance was assumed constant and the contact resistance ignored. Future work should be based on optimising the oscillator circuit using time domain simulations since they seem to have predicted the circuit behaviour more accurately.

CHAPTER 7

MONOLITHIC RTD OSCILLATORS

7.1 Introduction

In this chapter, the design and fabrication processes to realise resonant tunnelling diode (RTD) oscillators in monolithic form, i.e. as monolithic microwave integrated circuits (MMIC) will be described. The MMIC circuits were designed and simulated using ADS with the RTD model from Ref. [103]. A DC decoupling circuit (R_e, as discussed in chapter 2 and 5) was employed to suppress the low-frequency bias oscillations and a coplanar waveguide (CPW) was designed to connect the RTD and DC decoupling circuit (R_e). The RTD oscillators were fabricated in the James Watt Nanofabrication Centre (JWNC), an interdisciplinary research facility run by the School of Engineering at the University of Glasgow.

7.2 Components of RTD MMIC oscillators

The designed RTD MMIC oscillators consisted of three components namely the resonant tunnelling diode, the decoupling circuit (resistor) and the coplanar waveguide. These will be described next.

7.2.1 Resonant tunnelling diode

The epitaxial wafer used on this project was designed for resonant tunnelling diode-optical waveguide (RTD-OW) applications [118]. This material was used in the work described in this thesis because it had reliable and known RTD characteristics and was freely available. The RTD-OW epitaxial structure was designed to enable operation over a wide bandwidth, require a low drive voltage, give a large absorption change and introduce a low insertion loss, i.e. the RTD-OW I-V characteristic must show considerable negative differential conductance, and at the same time provide efficient light guidance with low optical background loss [118]. The structure for the wafer used is illustrated in Fig. 7.1, while Table 7.1 shows the detailed specification of the layer structure. The RTD-OW core employing the $In_{1-x-y}Ga_xAl_yAs$ composition was designed to have an absorption bandedge below 1550 nm. The RTD-OW wafer was grown by Molecular Beam Expitaxy on an SI InP substrate by IQE Ltd. The structure consists of InGaAs quantum well sandwiched by two AlAs barriers (that forms the double barrier quantum well RTD structure) embedded in an InAlGaAs waveguiding core and doped InAlAs cladding. In the 1300/1600 nm optical transmission windows, the InGaAlAs quaternary material system can be used to form the waveguide core and the quantum well, with AlAs and $In_{0.48}Al_{0.52}As$/InP being employed in the barriers and in the waveguide cladding layers, respectively.

The high frequency performance of the RTD-OW is improved by increasing

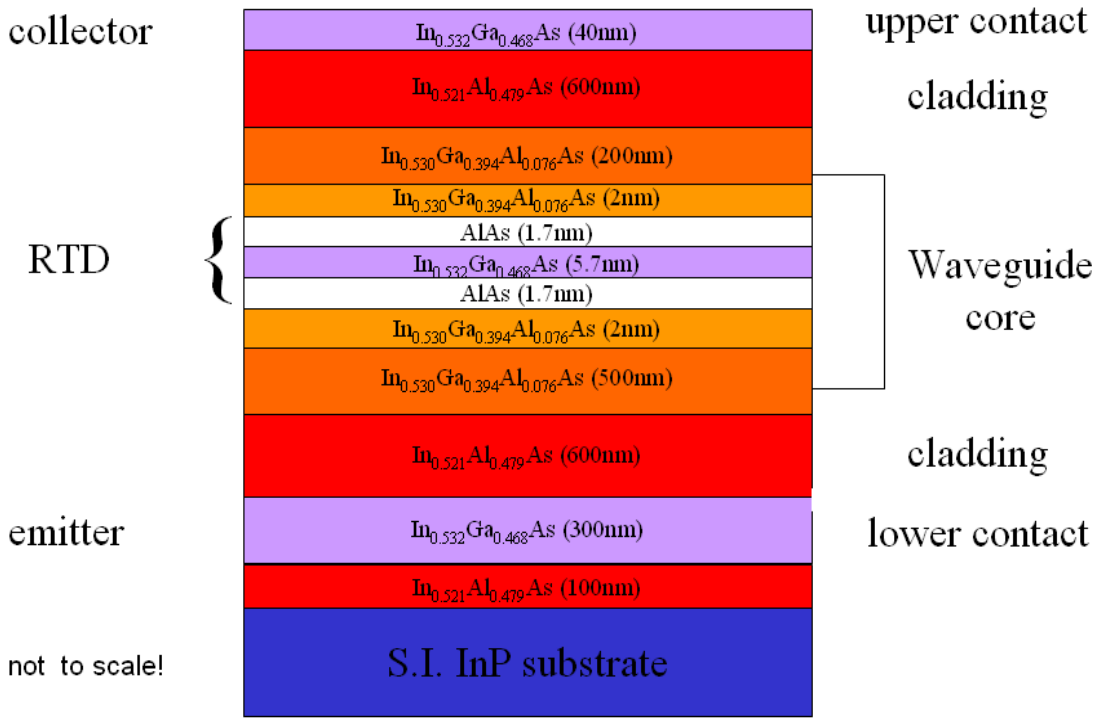

Figure 7.1: The heterolayer structure specification for the RTD-OW wafer. It was grown by Molecular Beam Expitaxy in a Varian Gen II system on a semi-insulating InP substrate by IQE, Ltd.

Layer no.	**Material**	**Thickness**	**Doping**	**Doping conc.**
1	$In_{0.532}Ga_{0.468}As$	40 nm	n	Si: 2×10^{19} cm^{-3}
2	$In_{0.521}Al_{0.479}As$	600 nm	n	Si: 2×10^{18} cm^{-3}
3	$In_{0.530}Ga_{0.394}Al_{0.076}As$	200 nm	n	Si: 5×10^{16} cm^{-3}
4	$In_{0.530}Ga_{0.394}Al_{0.076}As$	2 nm	undoped	
5	$AlAs$	1.7 nm	undoped	
6	$In_{0.532}Ga_{0.468}As$	5.7 nm	undoped	
7	$AlAs$	1.7 nm	undoped	
8	$In_{0.530}Ga_{0.394}Al_{0.076}As$	2 nm	undoped	
9	$In_{0.530}Ga_{0.394}Al_{0.076}As$	500 nm	n	Si: 5×10^{16} cm^{-3}
10	$In_{0.521}Al_{0.479}As$	600 nm	n	Si: 2×10^{18} cm^{-3}
11	$In_{0.532}Ga_{0.468}As$	300 nm	n	Si: 2×10^{19} cm^{-3}
12	$In_{0.521}Al_{0.479}As$	100 nm	undoped	
subst.	SI InP	350 μm		

Table 7.1: The hererolayer structure specification for the RTD-LD wafer. It was grown by Molecular Beam Expitaxy in a Varian Gen II system on a semi-insulating InP substrate by IQE Ltd.

the negative differential conductance, G_n, or by decreasing the device series resistance. To obtain a larger value of G_n, it is necessary to achieve a high peak current density, J_p, and a high peak-to-valley current ratio (PVCR), J_p/J_v. The small electron effective mass in the $In_{0.53}Ga_{0.47}As$ ($0.041m_0$) gives rise to high peak current densities due to the large broadening of the resonant levels. And, because of the high energy energy seperation between the Γ and upper (X and L) satellite valleys (Γ_{InGaAs}-X_{AlAs} barrier height of 0.65 eV) non-resonant tunnelling parasitic Γ-X mediated transport current flow is reduced, resulting in smaller current. This gives rise to a RTD-OW with a large peak-to-valley current ratio, resulting in high negative differential conductance. The conduction band discontinuities between $In_{0.48}Al_{0.52}As$ and the core material ($\simeq$ 0.47 eV), and between the core and the InP substrate ($\simeq$ 0.26 eV), can act as "ballistic launching ramps", injecting electrons into the lower bandgap material with high forward momentum, reducing the transit time considerably [120].

The waveguide core was formed by two moderately doped (Si: 5×10^{16} cm^{-3}) $In_{0.530}Ga_{0.394}Al_{0.076}As$ layers with 200 nm and 500 nm thick, respectively. The upper and lower claddings were implemented with 200 nm and 600 nm thick heavily doped (Si: 2×10^{18} cm^{-3}) $In_{0.521}Al_{0.479}As$ layers, respectively. The heavily doped (Si: 2×10^{19} cm^{-3}) 40 nm $In_{0.532}Ga_{0.468}As$ contact layers (on the top) and 300 nm (below the lower cladding layer) were used for formation of n-type Ohmic contacts using an $AuGeNi$-based metallisation.

The peak and valley voltages of the RTD-OW are slightly higher compared to a normal RTD wafer without an optical waveguide, because the waveguide cladding and core layers increase the device series resistance. As a consequence of the higher peak and valley voltages, the valley current will be increased due to enhancements of the non-resonant effects induced by the higher voltage/electric field across the structure [118]. The peak current does not change significantly but the valley current will increase, which leads to lower peak to valley current ratio (PVCR).

7.2.2 Coplanar waveguide

In the fabrication of RTD oscillators, a coplanar waveguide (CPW) is designed to connect the RTD to the decoupling circuit (R_e). It is also employed here as the inductor to determine the frequency of the oscillation by resonating with the self-capacitance of the RTD. A coplanar waveguide consists of a strip of a thin metallic film deposited on the surface of a dielectric slab, with two ground electrodes running adjacent and parallel to the strip on the same surface. A cross-section of the CPW is shown in Fig. 7.2. The most important parameters are the central conductor width w, the substrate thickness h, and its relative permittivity ϵ_r. The width of the ground planes should be larger than the gap width s to ensure single mode operation, and is usually set to at least three times the gap spacing [121]. The thickness of the metallic film strips is generally of less importance and is

often neglected in the analysis. However, to ensure good operation, the minimum thickness recommended is at least four times the skin depth in the metal at the lowest frequency of interest [123].

CPWs have been analysed using quasi-static as well as full-wave methods [123], [124]. The quasi-static methods provide information about the characteristic impedance Z_0 and the effective line permittivity ϵ_{eff} neglecting the frequency dependence of these elements. A full-wave analysis of coplanar waveguides provides information regarding frequency dependence of phase-velocity and characteristic impedance. The following closed form design equations can be used in most of the practical implementations of CPW circuits [125]

$$Z_0 = \frac{30\pi}{\sqrt{\epsilon_{eff}}} \frac{K(k')}{K(k)} \tag{7.1}$$

$$\epsilon_{eff} = 1 + \frac{\epsilon_r - 1}{2} \frac{K(k')\,K(k_1)}{K(k)\,K(k_1')} \tag{7.2}$$

where $K(k)$ represents a complete elliptic function of the first kind, and $K'(k)$ its complementary function $[K'(k) = K(k')]$, with $k_1 = \sinh(\pi w/4h) / \sinh[\pi(w+4s)/4h]$, $k = w/(w+2s)$, and $k' = \sqrt{1-k^2}$; $K(k)/K(k')$ can be approximated as

$$\frac{K(k)}{K(k')} \simeq \left[\frac{1}{\pi} \ln\left(2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right)\right]^{-1} \qquad 0 \le k \le 0.7 \tag{7.3}$$

$$\frac{K(k)}{K(k')} \simeq \frac{1}{\pi} \ln\left(2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right) \qquad 0.7 \le k \le 1 \tag{7.4}$$

These closed form equations are used in a software tool called *LineCalc* within Agilent's Advanced Design System (ADS) software to support the design of CPW

lines. On this project, the CPW was fabricated on the InP substrate with a dielectric constant of 12.56 [122] and a thickness of 320 μm. For a CPW with characteristic impedance of 50 Ω, the widths of the signal line and the gap space are W = 60 μm and S = 40 μm, respectively. The width of the ground planes were set to 120 μm .

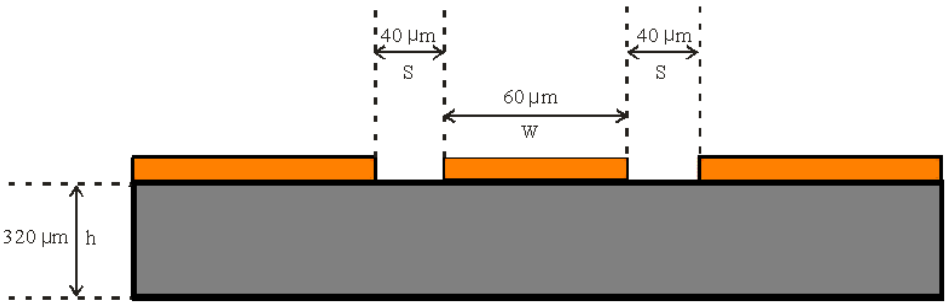

Figure 7.2: Cross-section of a CPW on an InP substrate with a dielectric constant of 12.56 and a thickness of 320 μm. The signal line width W = 60 μm, and the gap space S = 40 μm.

7.2.3 Nickel chromium resistor

In the fabrication of RTD oscillators, an integrated resistor as illustrated in Fig. 7.3 was used as the decoupling circuit (R_e). The integrated resistor was made of a thin film of nickel chromium (NiCr) with a uniform thickness of 33 nm. Its sheet resistance is 50 Ω/square. The resistance of the resistor can be calculated from

$$R = R_{sh}\frac{L}{W} \tag{7.5}$$

where, R_{sh} is the sheet resistance, L and W are the resistor's length and width, respectively.

The shunt resistor R_e was chosen to be 10 Ω to satisfy $R_e < 1/G_n$. In the actual circuit, two resistors in parallel were required for the CPW implementation, and so each resistor had a value 20 Ω (see illustration of the oscillator circuit in Fig. 7.4). The length of the resistor is equal to the gap (S = 40 μm) between the signal line and the ground plane of the CPW line. Therefore using equation (7.5) the width is the only dimension of the resistor that should be determined. For a 20-Ω resistor, the width should be 100 μm.

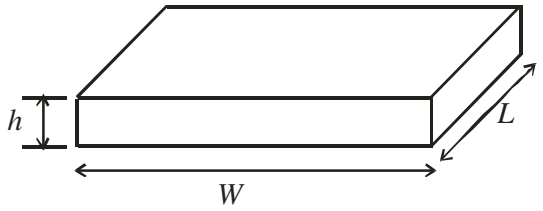

Figure 7.3: The layout of the NiCr resistor. L, W and h are the length, width and thickness of the resistor, respectively.

7.3 Monolithic RTD oscillator topology

The MMIC RTD oscillator circuit described here was designed in a similar way to that published by Raytheon Inc. [85]. A layout of the designed oscillator is shown in Fig.7.4. The MMIC RTD oscillator (Fig. 7.4) consists of an RTD and a DC decoupling circuit (two resistors in parallel) placed in a CPW line with

characteristic impedance, $Z_0 = 50\ \Omega$. The RTD area is covered by a passivation layer, polyimide. The CPW is fabricated on the semi-insulating InP substrate and connects through the vias in the polyimide passivation layer, which covers the device mesa, to the collector and emitter Ohmic contacts. The circuit is similar to that discussed in chapter 5, Fig.5.1 but without the decoupling capacitor C_e. The work described in this chapter was done prior to establishing the importance of the decoupling capacitor C_e in parallel with R_e as discussed in Chapter 5, therefore the decoupling capacitor C_e was not included in this circuit. The inductor (L formed by the CPW length between the resistor R_e and the diode) and the self-capacitance of the NDR device determine the frequency of the oscillation. The resistor (R_e) is employed as a DC decoupling circuit and was chosen, as earlier established, to satisfy $R_e < 1/G_n$, in order to obtain DC and low frequency stability in the circuit. The load (spectrum analyser or power meter) could be connected via a ground-signal-ground (G-S-G) probe to the right of the RTD.

To establish the design guideline of the circuit shown in Fig. 7.4 for an actual oscillator circuit, the circuit was simulated in ADS simulation software with the model of the resonant tunnelling diode from Ref. [103]. The wafer used in this project was from the same growth runs and of similar structure as that used in Ref. [103]. The diode, with 400 μm^2 cross-sectional area, was modelled using the fitted I-V characteristic in parallel with a 3.6 pF capacitor [119], [118]. Fig. 7.5 shows the experimental I-V characteristic and fitted model. For this diode, the

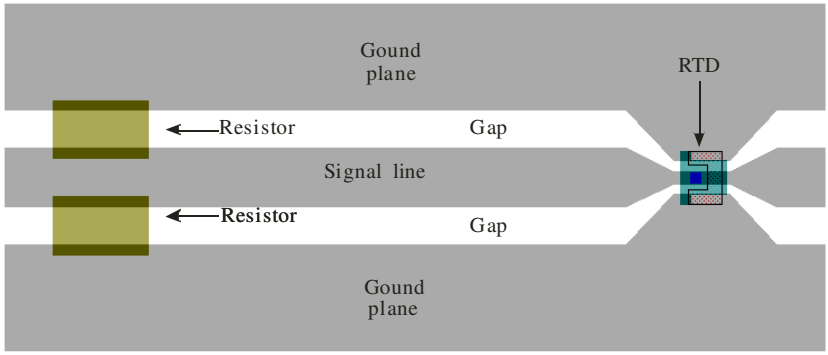

Figure 7.4: Layout of MMIC RTD oscillator comprising an RTD and a DC decoupling circuit (two resistors in parallel) embedded in a coplanar waveguide (CPW) line. The characteristic impedance of the CPW is 50 Ω and its series inductance per unit length is 90 pH/mm. The output power can be measured from the right hand side using a 50-Ω CPW probe.

difference between the peak and valley currents ΔI is 30 mA, and the difference between the peak and valley voltages ΔV is 500 mV [103]. The CPW was designed with characteristic impedance $Z_0 = 50\ \Omega$ and with inductance of $L = 45$ pH. Two 20-Ω resistors in parallel formed a 10-Ω shunt resistor as the DC decoupling circuit and placed across the CPW line as illustrated in Fig. 7.4, 500 μm from the RTD. Given that the fundamental frequency of the RTD oscillator is mainly dependent on the values of the inductance (L) and the self-capacitance of the NDR device, simulations were also carried out using the same I-V characteristic but a smaller capacitor (2 pF) in order to predict the oscillation frequency of an oscillator with a smaller active area ($\backsim$225 μm^2).

Fig. 7.6 shows simulation results with different RTD oscillator circuits. The RTD oscillator designed with the I-V model parallel with a capacitor (3.6 pF, estimated capacitance for a RTD with an area of 400 μm^2) is predicted from simulation to oscillate at 11.26 GHz with -18.27 dBm output power (Fig. 7.6(a)). The other oscillator designed for a RTD with an area of 225 μm^2 had a simulated oscillation frequency of 16.07 GHz with -14.32 dBm output power (Fig. 7.6(b)). The 1st harmonic was 20 dB below the fundamental and the larger harmonics were even lower. The I-V characteristic for the smaller device was scaled accordingly from the peak current density (10 kA/cm^2), peak-to-valley current ratio (4) but with the same peak-to-valley voltage difference (0.5 V), and an estimated capacitance of 2 pF.

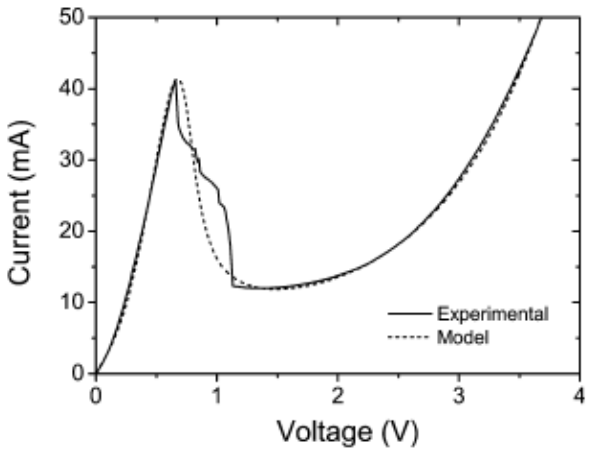

Figure 7.5: Experimental and modelled I-V characteristics for the RTD (400 μm^2) with capacitance C_n = 3.6 pF [103].

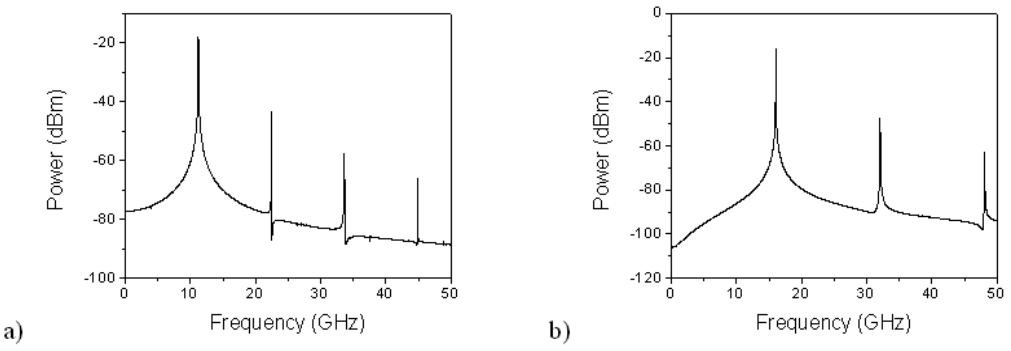

Figure 7.6: Simulated spectrum of a single RTD oscillator (400 μm^2, device size) using a fitted I-V characteristic: a) Fundamental oscillations are at 11.26 GHz with -18.27 dBm output power with a 500 μm long CPW and 3.6 pF capacitor. b) Fundamental oscillations are at 16.07 GHz with -14.32 dBm output power with a 500 μm long CPW and 2 pF capacitor.

7.4 Basic fabrication processes

This section provides a description of the main steps for the fabrication of RTD integrated circuit oscillators. Details of the actual process steps are given in Appendix C.

7.4.1 Sample preparation

Before the RTD oscillator fabrication, the wafer is cleaved into small samples and they are cleaned in an ultrasonic water bath. 10×10 mm^2 samples were used in the RTD oscillator fabrication. Before cleaving, the epilayer side of the sample must be identified, and this side should not directly touch the cleaving machine.

The samples were first cleaned in acetone (CH_3COCH_3), methanol (CH_3OH) and isopropyl alcohol (IPA, C_3H_8O) in the ultrasonic water bath. The small bubbles formed on the sample surface collapse at high speed providing a physical mechanism for particles and contaminant removal [126]. Acetone is an ideal solvent to clean the organic contaminants on the semiconductor substrate, and methanol is used to remove the possible oily contaminants on the sample surface. These are organic solvents and hence will not react with any of the materials used in III-V device fabrication. Since acetone may leave a residue when it evaporates, a transfer to IPA will remove the potential for residue formation. Finally, a de-ionised water rinse is used to remove all contaminants followed by a rinse in IPA.

7.4.2 Photolithography

Photolithography is used to create a pattern in photo resist on a semiconductor sample with a photolithography mask and ultraviolet (UV) light. First of all, a photolithography mask should be made by electron beam (e-beam) lithography. L-Edit software (Tanner Research, Inc., California, USA), was used to design the desired patterns, and then converted into the universal GDSII file. Another commercial application, CATS (Synopspy, Inc., California, USA) then fractured the patterns into trapezia that is the format required by the e-beam tool. Another software, Belle, developed in the University of Glasgow, was used to register the fractured patterns with a given sample size, dose, beam size and resolution. Fi-

nally, technical staff in the JWNC would write the masks using a Leica Electron Beam Pattern Generator 5 (EBPG5).

Once the photolithography masks were produced, the photolithography process started with the spinning of a positive resist on the sample. First, the sample was attached onto a spinner in a laminar air flow (LAF) cabinet by the means of vacuum. Then, the photo resist (Shipley S1818) was applied on the sample surface without bubbles, and rapidly accelerated to the desired rotational speed for a pre-determined time. The thickness of the uniform layer of photo resist is determined by the fluid properties of the resist and the spin speed [127].

Once the photo resist was spun onto the sample, a pre-patterned mask was placed over the sample. When the sample was correctly aligned to the pattern on the mask, the sample was moved into contact with the mask directly and a UV lamp illuminated the resist in regions where the mask is transparent. The photo resist used for this project was Shipley S1818. This is a positive resist which is photosensitive from 350 nm to 450 nm [128]. The UV light used to expose the resist is at 365 nm, therefore the polymer in the photo resist is broken down and then can be developed by Shipley Microposit(R) Developer Concentrate (a metal ion containing developer) resulting in the exposed areas being removed by the developer solvent [129]. A Sűss mask aligner (MA6) was used to conduct this work, providing good alignment and contact between sample and mask, achieving high resolution ($\backsim$0.5 μm) in pattern definition. In this machine, the UV light output

of the mercury lamp is continuously monitored to maintain constant intensity. All of the exposure processes of lithography were carried out in a sterile and dust-free environment (clean room class 100 – there are only one hundred or less particles that are 0.5 μm or greater in diameter in a cubic foot of air in this class of clean room [130]).

7.4.3 Lift-off metallisation

The lift-off technique was used for patterning the Ohmic contacts. Using this technique, windows are defined in a layer of resist(s) where the contacts will be formed. In the exposed regions, the metal is deposited on the substrate; in the masked areas, the metal is deposited on the resist. Then by soaking the sample in a solvent, the resist can be dissolved, removing the metal deposited on top of the unexposed regions. In general, a lift-off process requires that the layer of the resist(s) be thicker than the metal to be deposited and that the resist profile have a negative slope or undercut along the edge of the resist. This ensures that metallisation on top of the resist is disconnected from that on the substrate and so this can be easily "lifted-off" by dissolving the resist.

There are two different methods usually used for lift-off in the JWNC. In one of the methods, two different resist types - bi-layer lift-off metallisation - are used. A lift-off resist, Michrochem LOR-10A, is first spun onto the sample on top of which a second photo resist layer, S1818, is spun. The LOR-10A is not photosensitive

and provides an undercut which is useful for the lift-off process. However, this method produces thicker bead at the edges of the sample due to two layers of resist being employed, and this could lead to poor pattern reproduction. The other lift-off technique employed in the JWNC uses only the S1818 photoresist. The sample is coated with S1818 photo resist and pre-baked at $65\,^{\circ}C$ for 2 minutes. It is then soaked in 1:1 Shipley Microposit(R) Developer Concentrate: H_2O for 60 seconds before exposure [131]. Upon development, the resist edges have a negative slope which is suitable for lift-off metallisation. This latter method was used on this project.

7.4.4 Metallisation

Before metal deposition, a step to remove the surface oxide of the sample surface is carried out. This is because the oxide layer which can be found on the surface of III-V semiconductor presents a barrier to electrons from the metal to the semiconductor. A standard process of a short dip in a dilute solution of hydrochloric acid (HCl) and then in de-ionised water was used [132].

Depositing metal onto the semiconductor samples can be carried out in several different ways, such as thermal evaporation, electron beam evaporation and sputtering. Electron beam evaporation was employed on this project, using both a Plassys MEB 450 Electron Beam Evaporation (Plassys I) and a Plassys MEB 550S (Plassys II). First of all, the sample is carefully clamped to the holder which

was specially designed for the evaporator. Once the sample is loaded upside down into the vented load lock and the system is pumped down to the process pressure (Plassys I is an older model with a base pressure of 1×10^{-7} Torr maintained by a diffusion pump, whereas Plassys II has a lower base pressure by a factor of 10 which is generated by its cryogenic vacuum pump [133]) the desired metal scheme is chosen from the PC control software, and the metal in the crucible is heated past the melting point by a beam of electrons. Once the deposition rate is steady, the shutter that blocks the holder and sample is opened. The vapourised metal evaporates up onto the sample where it deposits. Metal is thus deposited everywhere on the sample, and the metal on the regions without resist would adhere onto the sample, while the metal on the areas covered by resist will be easily and completely removed in a warm acetone bath during the lift-off process. The metals available for deposition by evaporation in JWNC are gold (Au), germanium (Ge), nickel (Ni), titanium (Ti) and nichrome (NiCr).

On this project, only n-type Ohmic contacts were required for device fabrication. For n-type InGaAs contact/cap layers, the gold-germanium (Au/Ge) based contact scheme is commonly used [134]. The Au/Ge scheme is usually employed with an overlay of another metal, such as nickel. Gold-germanium is evaporated in proportions that represent a eutectic alloy (88% Au, 12% Ge by weight), whose melting point is at 360°C. Germanium is an n-type dopant in InGaAs, and high quality Ohmic contacts are achieved because germanium diffuses into the semi-

conductor and gallium diffuses towards to the metal layer, then creating heavily doped ($>10^{19}$ /cm^{-3}) layer at the semiconductor surface [130], [135]. An optimum atomic ratio Ge:Ni of 0.8-1.0 was reported to yield contact resistances in the range 10^{-2}-10^{-1} Ω-mm [136]. An optimised recipe of this n-type Ohmic contact Au/Ge/Au/Ge/Au/Ni/Au (10nm/10nm/10nm/10nm/20nm/10nm/80nm) was developed in the JWNC [133] and was used on this project. After the deposition of the metal stack, annealing was carried out in a Jipelec rapid thermal annealer (RTA). A computer was used to control the RTA to quickly heat the sample to a desired temperature for 60 seconds in an inert nitrogen environment. The annealing temperature was at 380°C in order to achieve minimum contact resistance (0.031 Ω-mm) extracted from transmission line measurements (TLM) [133].

7.4.5 Etching

There are two different methods used to etch III-V semiconductor samples, wet etching and dry etching. Wet etching III-V semiconductors involves liquid chemical etchants, usually acid solutions in water. In the etching process, firstly, an oxidising agent creates an oxide layer at the semiconductor surface and then a etching agent removes the oxide in a reduction reaction [130]. Oxides of GaAs derived alloys are amphoteric, which means that an acid can be used to remove them [137]. The whole etching rate, including oxidation and dissolution processing, can be adjusted to the desired one by properly allocating the amounts of the

agents in the solution.

A 1:1:38 H_3PO_4: H_2O_2: H_2O solution which can etch both InGaAs and InAlAs at a rate of $\backsim$100 nm/min [134] and a 3:1 HCl:H_2O solution that can etch the InAlAs layer at a rate of $\backsim$600 nm/min were used in this project. An oxide layer measuring approx. 5 nm remains on the surface after removal from the etchant [138]. Agitation of the sample in the solution is necessary in order to obtain constantly replenished etchant on the sample surface rather than a diffusion-rate limited etch. Although wet etching could provide a comparatively higher etching rate and better selectivity between $In_{0.53}Ga_{0.47}As$ and InP than that of dry etching [140], it can also cause serious under-cut (sample is horizontally etched) problems. This is because there are favoured crystallographic directions (and the resulting etch profiles) during the wet etching of InGaAs [139] and InP [140]. In the first attempts to fabricate RTDs, the under-cut would remove half of the collector for larger size device (30×30 μm^2) and almost the whole collector for the smaller one (15×15 μm^2). Fig. 7.7a shows a collapsed collector metallisation after wet etching.

To avoid the serious under-cut problem from the wet etching recipe, dry etching was introduced to etch some of the device layers. Dry etching processes are a combination of a physical process, in which the energetic ion beam or particles bombard the semiconductor surface, and a reactive process, a plasma-driven chemical reaction. Ions in the plasma are accelerated towards to the surface using

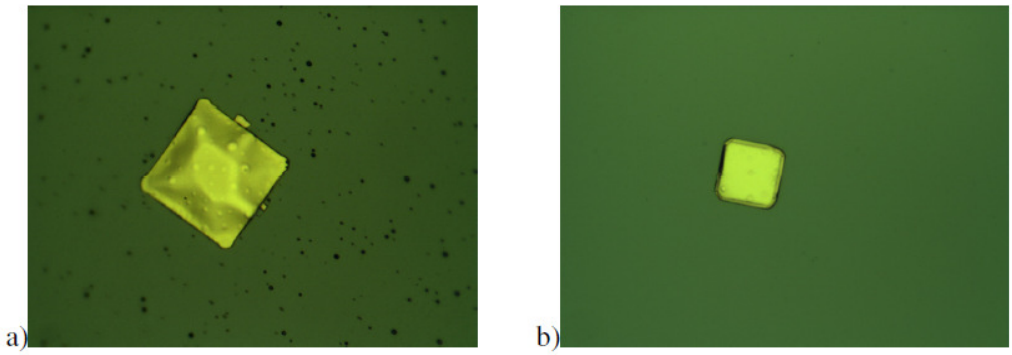

Figure 7.7: The collector after the etching process. a) a broken collector after only wet etching from the collector layer to the emitter layer, b) a good collector after both wet & dry etching from the collector to emitter layer.

the DC self-bias in the system or, in the case of a remote plasma, by an applied bias to the sample. The particles that are etched away are pumped out avoiding re-deposition by the vacuum. Dry etching can be used to fabricate nearly vertical sidewalls over large $\backsim 2$ μm scales, with high aspect ratios [141]. The dry etching process used on this project was developed by the Dry Etch group at the University of Glasgow and is based on reactive ion etching (RIE) using methane/hydrogen (CH_4/H_2) in an Electrontech SRS Plasmafab 340 RIE machine (ET340). It requires a DC bias of around 650 V. This is likely to introduce considerable material damage, such as hydrogen passivation of dopants and degradation of the material mobility [142]. But as dry etch chemistries that selectively etch indium containing alloys are not common [143], both wet and dry etchings were used in the project to achieve vertical sidewalls and good selectivity as well as low damage to the ma-

terial. Fig. 7.7b shows the collector metallisation after both wet and dry etching using the developed recipe (details on this process will be provided in the next section).

7.4.6 Passivation

Generally, silicon dioxide (SiO_2) or silicon nitride (Si_3N_4) is used as a passivation layer and as an insulator to separate different parts of the device, such as the collector and emitter metallisation. However, as the mesa height was high, around 2 μm, polyimide (PI2545) [144] was chosen for passivation and planarisation. The process of coating a sample with polyimide is similar to the one for photo resists such as S1818, and it can be etched by most alkaline positive resist developers [144]. In order to pattern the polyimide, a positive photo resist should be spun on the top of it. A 1:41 Tetramethylammonium Hydroxide (TMAH):H_2O solution is recommended to develop the photoresist and etch the polyimide as well [144]. The patterning removes the spun polyimide from all areas of the sample (the exposed SI InP substrate) except on the device mesas in which windows/vias are opened in the polyimide for the collector, emitter contacts.

7.5 RTD oscillator fabrication

Based on the steps described in the preceding section, this section describes the whole fabrication process for the RTD oscillator. Before the RTD oscillator

fabrication process, the samples needed to be thoroughly cleaned. This consisted of 5 minutes in ultrasonic water bath in a beaker containing first acetone followed by methanol and then isopropyl alcohol (IPA). A softer plastic beaker was used in this processing step because a harder glass beaker could possibly lead to the sample breaking, especially for very fragile InP substrate sample used on this project. It is important not to leave the sample to dry when it is transferred from one solution to another. This avoids any particles in the solution from adhering to the sample surface which would lead to undesirable effects in the later fabrication processes. Finally, de-ionised water was used to rinse the samples in the beakers for at least 2 minutes.

The first step of the fabrication was to define the collector patterns and the alignment markers on the sample using photolithography. After this, a process to remove the surface oxide of the sample surface was carried out. And following this step, the collector metal (*Au/Ge/Au/Ge/Au/Ni/Au*, 10 nm/10 nm/10 nm/10 nm/20 nm/10 nm/80 nm) was deposited on the sample surface using Plassys I or II (Fig. 7.8(a)). After the collector Ohmic contact was deposited on the sample using lift-off. 200 nm of silicon dioxide (SiO_2) was deposited to act as a hard mask, to protect the collector metal and alignment makers during the dry etching step. This etching process consisted of three steps:

1. The collector cap was etched first by using a 1:1:38 H_3PO_4:H_2O_2:H_2O solution which etched at a rate of $\backsim$100 nm/min. Here H_2O_2 was the oxidising

agent and the H_3PO_4 was the etching agent. Then, a 3:1 HCl:H_2O solution was used to etch the InAlAs layer at a rate of $\backsim$600 nm/min.

2. The InGaAlAs layer was etched by CH_4/H_2 in ET340 at rate of $\backsim$17 nm/min.

3. After the dry etching, a 3:1 HCl:H_2O solution was used to etch the InAlAs layer to the emitter layer (InGaAs). The wet etching is selective and stops on the InGaAs layer (Fig. 7.8(b)).

The next step was to define the emitter metal pattern on the sample by photolithography, after which the Ohmic contact to the emitter contact layer was deposited. The same metallisation scheme as for the collector was used. After this step, annealing was required for both collector and emitter Ohmic contact to improve the contact resistance (Fig. 7.8(c)). Following the annealing step, individual devices were isolated by etching the extrinsic emitter layer down to the substrate using the 1:1:38 H_3PO_4:H_2O_2:H_2O solution which stops on the substrate (InP) due to the selectivity of the etchant on InP (Fig.7.8(d)). After etching down to the substrate, a passivation and insulation layer, polyimide (PI2545), was spun on the semiconductor surface and removed from all areas except around the RTD mesa areas where vias were opened for the collector and emitter contacts. The polyimide passivates the surface, provides a positive slope (slants away from the developed/exposed regions) for the bond pad to connect the collector and emitter contacts to the coplanar waveguide (CPW) on the semi-insulating InP substrate, and acts as a dielectric/insulation between metal connections to the collector and

emitter metal contacts. Some of the RTDs were fabricated with 100 μm long CPW RF pads. Fig. 7.9 is a picture of one of the fabricated devices. Other RTDs were fabricated with 500 μm long CPW RF pads connected to 10-Ω stabilising resistor to realise integrated RTD oscillators. In this case, before depositing the CPW, a pair of 20-Ω integrated resistors (33 nm NiCr) were first deposited on the substrate to form the DC stabilising resistor. A labelled optical picture of one of the fabricated RTD oscillators is shown in Fig. 7.10. The full fabrication process is given in Appendix C.

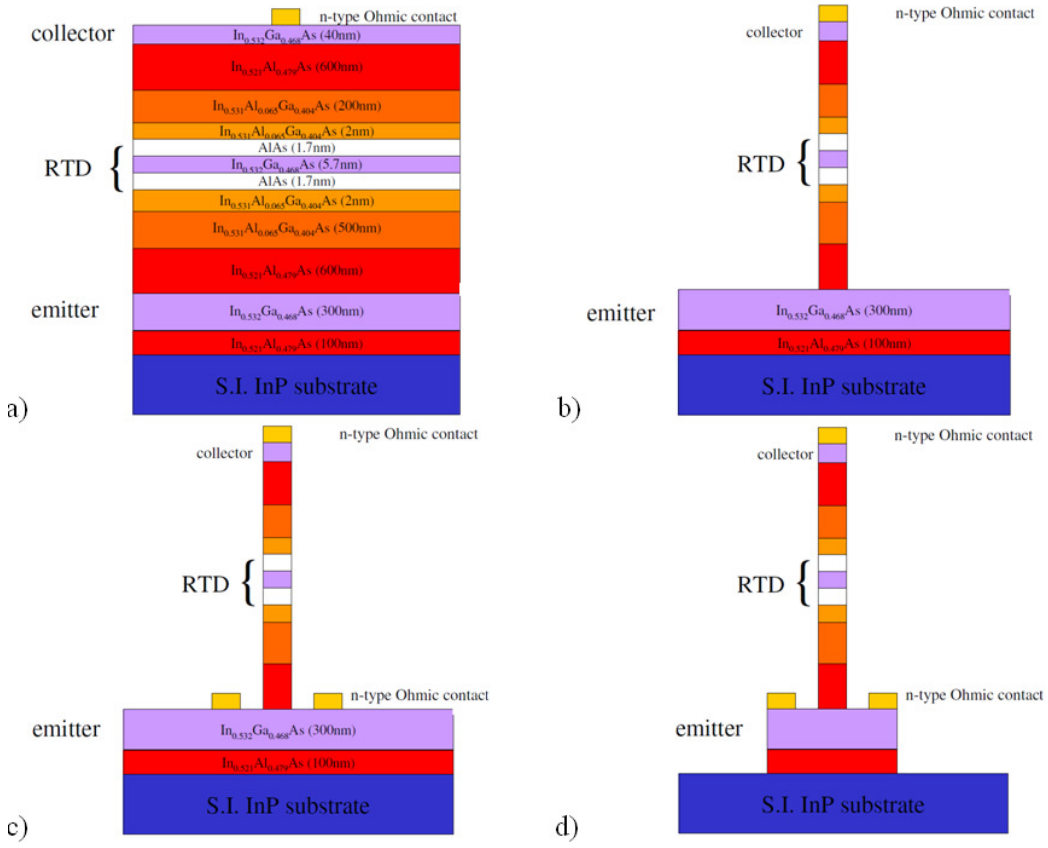

Figure 7.8: Cross-sectional views of the main fabrication steps for the RTD.

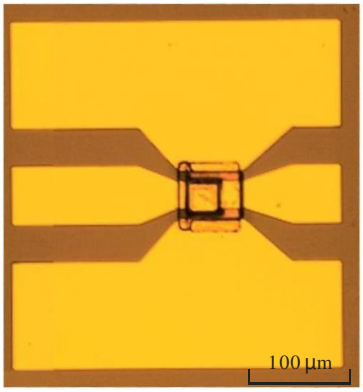

Figure 7.9: A fabricated RTD with 15×15 μm^2 active area and 100 μm CPW metal pads.

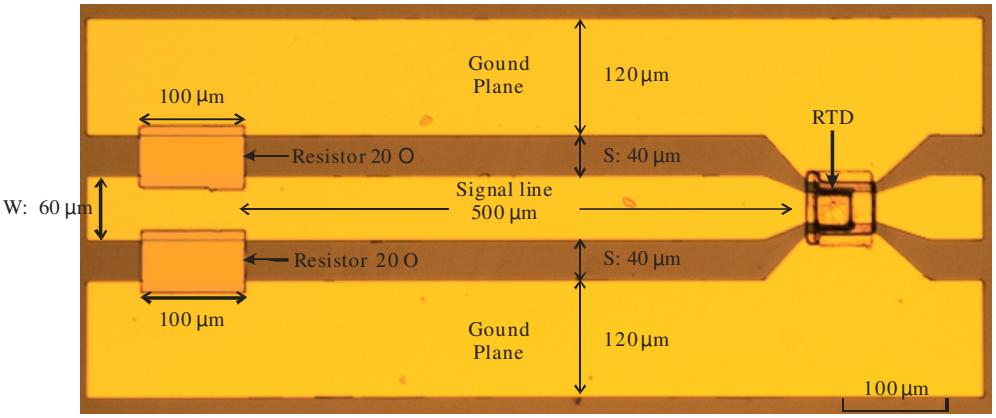

Figure 7.10: An optical picture of a fabricated MMIC RTD oscillator: a RTD with 15×15 μm^2 active area and a DC stabiliser (two 20-Ω resistors with width = 100 μm, length = 40 μm and thickness = 33 nm in parallel) placed in a coplanar waveguide (CPW) line on an InP substrate with a dielectric constant of 12.56 and a thickness of 320 μm. Signal line width, W = 60 μm, gap space, S = 40 μm and width of the ground planes, 120 μm.

7.6 Experimental results

RTD oscillators were designed and fabricated with 500 μm long CPW lines and RTDs with collector cross-section areas of 15×15 μm^2 and 20×20 μm^2, respectively. Individual RTDs were fabricated with 100 μm long CPW RF pads as shown in Fig. 7.9. The *I-V* characteristics of the fabricated RTDs were measured by using an Agilent B1500 semiconductor device analyzer (SDA) through Cascade CPW probes. The measured *I-V* characteristics of RTDs with an area of 15×15 μm^2 and 20×20 μm^2 are shown in Fig. 7.11(a) and (b), respectively. Both RTD characteristics show that the peak current density is up to 10 kA/cm^2 and the peak to valley ratio is around 3, with valley-to-peak voltage difference (ΔV) of 1 V and peak-to-valley current difference (ΔI) of 12 mA for the RTD with 15×15 μm^2 active area, and 1 V and 27 mA for the 20×20 μm^2 device, respectively. Compared with the *I-V* model as shown in Fig. 7.5, the measured *I-V* characteristics of the RTDs with an area of 400 μm^2 have similar peak-to-valley current difference (ΔI) but the valley-to-peak voltage difference (ΔV) is higher. Therefore, the fabricated RTDs oscillators with an area of 400 μm^2 RTD could provide higher maximum output power ($P_{max} = 3\Delta I \Delta V/16$) than that was provided by the model (Fig. 7.5) because of the larger voltage difference.

The oscillator circuits were designed so that the RF output signal could be measured across a 50-Ω load (spectrum analyser) connected directly to the 50-Ω CPW pad of the RTD (the pad to the right of the RTD in Fig. 7.9). However,

as there was only one CPW probe available during the measurement (the other probe was faulty and so unavailable), the output signal was measured across the 10-Ω stabilising resistor, in a similar way to Ref. [85]. The probe was therefore connected via a bias-T so that it carried both the DC and RF signals; the DC to bias the RTD while the RF was the oscillator output. In the bias-T, the DC and RF ports are isolated with a large inductor (from the RF signal) and capacitor (from the DC signal), respectively. Therefore if very low frequency bias oscillations were present, they may not have been detected by this measurement technique.

Fig. 7.12 shows the measured oscillation frequency and output power as 17.5 GHz and -23.12 dBm, respectively. The measurement was done using an Agilent RF spectrum analyzer E4448A with the device biased at 1.80 V for the RTD oscillator with 15×15 μm^2 active area and with 500 μm length between the shunt resistors and the RTD. Bearing in mind the discussion on bias-T above, the choice of 0 - 30 GHz measurement span was unwise. A small span about the oscillation frequency would have provided more useful information such as level of oscillator noise and presence of low frequency up-converted signals.

The unconnected RF pads in the oscillator circuit act as a short open stub. Since the stub has a characteristic impedance of 50 Ω and a length of 100 μm, the open stub acts a capacitor of value 17.4 fF at the oscillation frequency of 17.5 GHz. This is significantly smaller that the 2 pF device capacitance and so influences only very slightly the oscillator performance. For oscillators with 20×20

μm^2 RTDs, no oscillations were observed. This may have been due the complete circuit (including the stabilising resistor) being stable.

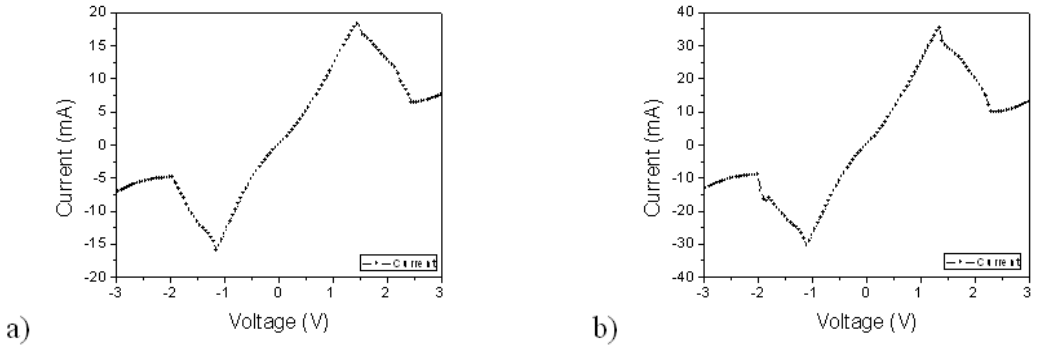

Figure 7.11: Measured RTD I-V characteristics with: a) 15×15 μm^2 active area, b) 20×20 μm^2 active area.

7.7 Discussion

The fabricated RTD oscillators had a measured fundamental frequency (17.5 GHz) which was slightly higher than the simulated fundamental frequency (16.02 GHz). This discrepancy may be due to the areas of the fabricated RTDs in the oscillators being slightly reduced due to undercut during the wet etching process. Therefore the capacitances of the RTDs are slightly smaller than the estimated value of 2 pF and therefore the oscillation frequency is slightly higher than the simulated frequency. The measured RF output power is lower than the simulated results. There are several possible reasons for the low output power. First of all, the stabilising resistors consumed most of the power delivered from the RTD. As

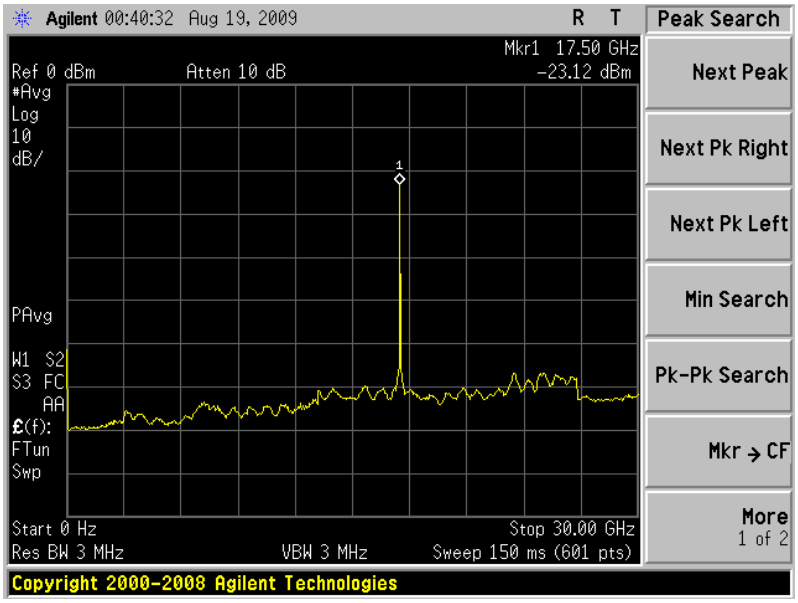

Figure 7.12: Picture of measured spectrum of the fabricated oscillator with 15×15 μm^2 RTD active area and 500 μm long CPW lines. Spectrum shows fundamental oscillation frequency is 17.5 GHz and output power is of -23.12 dBm.

will be shown in the next chapter, only 1/6th ($R_e/(R_e + R_L)$, with $R_e = 10\ \Omega$ and $R_L = 50\ \Omega$) of the generated power reaches the load and 5/6th ($R_L/(R_e + R_L)$ is consumed by the stabilising resistor. The RTDs in the fabricated oscillators had smaller current difference (ΔI) compared with the I-V model as shown in Fig. 7.5 although the voltage difference (ΔV) was higher. But according to equation ($P_{max} = 3\Delta I \Delta V/16$) used to calculated the maximum theoretical output power, a maximum of 3.5 dBm for the $15 \times 15\ \mu m^2$ device could be achieved (Note that the equation assumes that all power is at the fundamental frequency and that the oscillator is impedance matched to load, none of which may have been true for this circuit).

7.8 Summary

RTD MMIC oscillators in coplanar waveguide operating at 17.5 GHz were successfully fabricated on this project. However, the output power is low mainly because of the power consumed by the stabilising resistor. The total loss including load mismatch was 20 dB. It is expected that using the oscillator topology discussed in chapter 5 would lead to more efficient oscillators (reduced harmonics) with higher output power.

CHAPTER 8

OUTPUT POWER ANALYSIS OF RTD OSCILLATORS

8.1 Introduction

For tunnel diodes or RTD oscillators, it is known that the maximum RF output power can be obtained if a parallel oscillator topology is employed [83], [100], [101]. In this topology, an inductor can be chosen to resonate with the device capacitance and also an optimum load can be chosen to match the negative differential conductance of the device. The derivation of the maximum RF output power that can be delivered by a parallel RTD oscillator circuit in terms of the I-V characteristics of the device is given. The output power analysis is based on the cubic polynomial model for the RTD I-V characteristics. As earlier noted, the purpose of the cubic model is not to reproduce the I-V characteristics of an actual tunnel diode. As a matter of fact, a 9th order polynomial as discussed in chapter 6 is required to accurately model the I-V characteristics of the tunnel diode used on this project. However, because the cubic model captures the main attributes of the I-V characteristics of actual devices researchers have previously employed it for generic non-linear analysis of circuits containing tunnel diodes or resonant tunnelling diodes [98], [100], [102]. It has for instance been widely

used in estimating the RF output power of actual RTD oscillators [36], [40], [100], and is used for the same purpose here. It is also shown how such an oscillator is realisable in planar technology (similar to the topologies discussed in chapter 5).

Due to the known problems of parasitic bias oscillations and to a lesser extent improper circuit topologies, the output power of the RTD-based oscillators is very low, in the microWatt range [40], [85], [82]. For instance, the oscillator topology employed in reference [85] taking the output signal across the stabilising resistor dramatically reduces the RF output power as will be shown in this chapter. High frequency RTD oscillators are often realised in waveguide technology. Analysis of this implementation in Reference [63] shows how difficult it is to achieve DC and low frequency stability. This problem is highlighted in almost all reported RTD-based waveguide oscillators, see e.g. [40], [80] in which a lossy bias transmission line section is used to suppress the problem. A review of this oscillator circuit is presented in this chapter. The chapter concludes with an analysis of the variation with frequency of the RF output power of a tunnel diode or RTD parallel oscillator.

8.2 Output power analysis for parallel RTD oscillators

In this section, expressions for the maximum power achievable from parallel RTD oscillators are derived for the typical large-signal RF equivalent circuit of parallel RTD oscillators as shown in Fig.8.1 [100]. This equivalent circuit is similar to that of Fig. 5.1; the circuit of Fig. 5.1 illustrates how the DC biasing of the

RTD is made for the parallel topology - it is supplied to the RTD across the parallel stabilising resistor and capacitor, with the capacitor acting as a short circuit at RF frequencies.

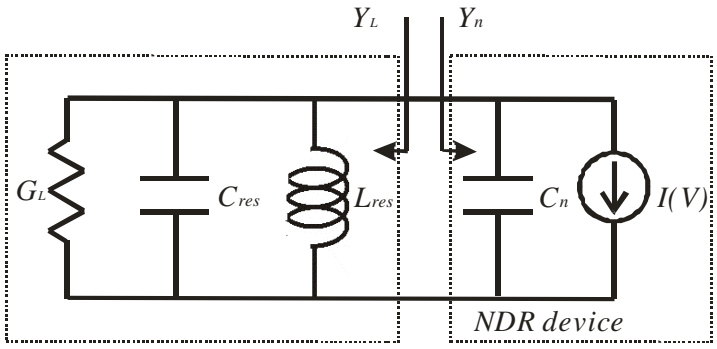

Figure 8.1: A large-signal RF equivalent circuit of parallel RTD oscillator with load conductance G_L and resonant circuit (inductance L_{res} and capacitance C_{res}).

In the RF equivalent circuit shown in Fig. 8.1, G_L is the load conductance, L_{res} and C_{res} are the resonant circuit elements used to determine the frequency of the circuit and C_n is the device capacitance (adds to C_{res}). This circuit can be described by equation (8.1) according to Kirchhoff's current law where the current source is represented by a cubic polynomial with a and b both positive parameters, $a = (3\Delta I)/(2\Delta V)$ and $b = (2\Delta I)/(\Delta V)^3$ and ΔI is the difference between peak and valley currents, and ΔV is the difference between valley and peak voltages [83], [100]

$$L_{res}C\frac{d^2v}{dt^2} + L_{res}(G_L - a + 3bv^2)\frac{dv}{dt} + v = 0 \tag{8.1}$$

where capacitance $C = C_n + C_{res}$.

Equation (8.1) is similar/identical to equations (5.1) and (5.2) and therefore, as discussed in section 5.2, if L_{res} is chosen such that $\varepsilon \ll 1$ (from equation (5.3)) then the solution to equation (8.1) for the voltage v will be sinusoidal. For such sinusoidal oscillations, the voltage v across the NDR devices is

$$v = V\cos(\omega t) \tag{8.2}$$

where $\omega = 1/(\sqrt{L_{res}C})$. The instantaneous power dissipated in load G_L is

$$P_L = G_L v^2 = G_L(V\cos(\omega t))^2 \tag{8.3}$$

and average power (integrating equation (8.3) over a period) is

$$P_L = G_L\frac{V^2}{2} \tag{8.4}$$

The instantaneous power generated by the NDR device (the bias point is moved to the origin, therefore generated power should be given as in equation (8.5)) is

$$P_{NDR} = -i \times v = (av - bv^3)v = av^2 - bv^4 \tag{8.5}$$

and average power (integrating equation (8.5) over a period) is

$$P_{NDR} = \frac{av^2}{2} - \frac{3bv^4}{8} \tag{8.6}$$

If the DC bias point is chosen at the origin, the constant a becomes G_n (the conductance of the NDR device at the bias point), therefore equation (8.6) can be re-written as

$$P_{NDR} = \frac{G_n v^2}{2} - \frac{3bv^4}{8} \tag{8.7}$$

By equating the average power dissipated in the load during one cycle to the average generated ac power, it gives

$$\frac{G_n v^2}{2} - \frac{3bv^4}{8} = \frac{G_L}{2} V^2 \tag{8.8}$$

Equation (8.8) can also be calculated by substituting equation (8.2) to equation (8.1) [100]. The solution of equation (8.8) is

$$V = 2\sqrt{\frac{G_n - G_L}{3b}} \tag{8.9}$$

Power to the load (G_L) is

$$P_L = 2(G_n - G_L)\frac{G_L}{3b} \tag{8.10}$$

And the maximum power can be obtained when

$$G_L = \frac{G_n}{2} \tag{8.11}$$

Combining Eqs. (8.10) and (8.11), the maximum power is

$$P_{\max} = \frac{G_n^2}{6b} = \frac{3}{16}\Delta I \Delta V \tag{8.12}$$

Equation (8.12) gives the theoretical maximum RF output power that can be generated by an NDR device such as a tunnel diode or an RTD in terms of its I-V characteristic. For instance, for the fabricated $15 \times 15\,\mu m^2$ RTD described in chapter 8 with $\Delta I = 12\,mA$ and $\Delta V = 1\,V$ the expected maximum RF output power in an oscillator circuit will be 3.5 dBm from equation (8.12).

8.3 Power limitation of the Chahal RTD oscillator topology

The RTD oscillator topology proposed by Chahal [85] will be analysed here. This topology was used to implement a 50 GHz RTD oscillator. Fig. 8.2(a) shows an RTD oscillator topology with the load connected via a bias-T as in Ref [85]. A small shunt resistor is used as a DC stabiliser to suppress bias oscillations. For high frequency oscillation signals, the inductor L_b works like open circuit and capacitor C_{block} acts like short circuit, therefore, the RF equivalent circuit as shown in Fig. 8.2(a) can be re-drawn as shown in Fig. 8.2(b). Y_{ext} and Y_n are the admittances of the external load network and the NDR device, respectively. The external admittance Y_{ext} can be described as

$$Y_{ext} = G' + \frac{1}{j\omega L'} \equiv \frac{1}{R + j\omega L} = \frac{R - j\omega L}{R^2 + (\omega L)^2} \tag{8.13}$$

i.e.

$$G' = \frac{R}{R^2 + (\omega L)^2} \tag{8.14}$$

$$L' = \frac{R^2 + (\omega L)^2}{\omega^2 L} \tag{8.15}$$

where $R = R_e \,//R_L$ (R_e in parallel with R_L), ω is the operating frequency in the circuit, L is the total inductance that includes the device series inductance L_s and the external inductance L_e between the stabilising resistor R_e and the NDR device and G' and L' are the equivalent conductance and inductance of the external load network.

The equivalent circuit of Fig. 8.2(b) is the same as Fig. 2.6 if R_e is replaced by R, where $R = R_e//R_L$ (R_e in parallel with R_L). This circuit is also as the

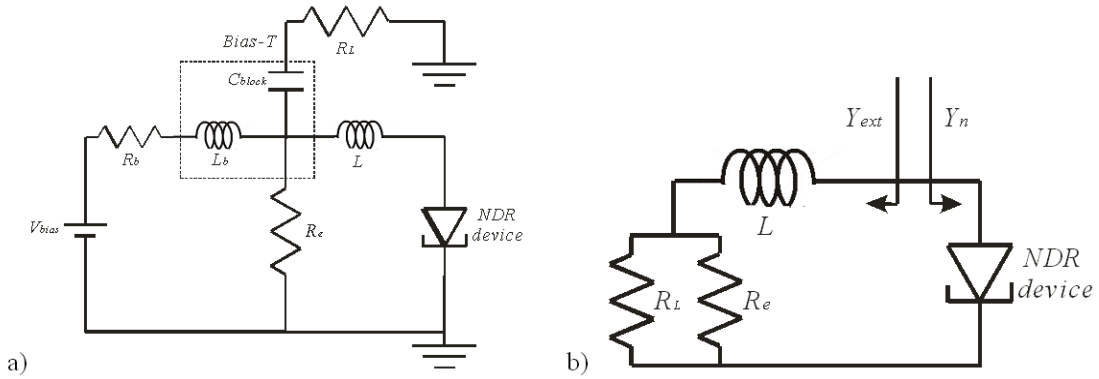

Figure 8.2: A typical RTD oscillator with load (R_L) and external DC decoupling circuit (R_e). a) R_b and L_b model the resistance and inductance of the bias line. The inductance L (the total inductance that includes the device series inductance L_s and the external inductance L_e between the stabilising resistor R_e and the NDR device), resistor R_e and self-capacitance of the NDR device determine the frequency of the oscillation, R_L is the load and C_{block} is a DC block. b) Equivalent circuit of Fig. 8.2(a) when L_b and C_{block} act as an RF open circuit and RF short circuit, respectively.

same as the one as shown in Fig. 8.1 if G_L is replaced by G', L is replaced by L' and C_{res} is removed. G' and L' are the equivalent conductance and inductance of the external circuit (R and L). They are given by Eqs. (8.14) and (8.15). Since the equivalent load conductance G'_L is function of R_L, R_e and ω, clearly only a fraction of the generated power can be delivered to R_L, e.g. for the fabricated MMIC oscillator $R_e = 10\ \Omega$ and $R_L = 50\ \Omega$, the stabilising resistor (R_e) will also consume power P_r given by

$$P_r = \frac{R_L}{R_e + R_L} P'_L = \frac{5}{6} P'_L \tag{8.16}$$

and the power deliver to the load (R_L) is only

$$P_L = \frac{R_e}{R_e + R_L} P'_L = \frac{1}{6} P'_L \tag{8.17}$$

where P'_L is the power delivered to the external load network. Therefore, only a small fraction (1/6th for the fabricated example oscillator) of the theoretical maximum power ($3\Delta V \Delta I/16$) of the RTD oscillator as shown in Fig. 8.2(a) can possibly reach the load R_L.

8.4 Comparison between the Chahal and the parallel RTD oscillator topology

The oscillator topology discussed in the preceding section will be compared to another a planar integrated RTD oscillator topology similar to the circuits in Ref. [36], [37], [38]. This other topology is also similar to that developed in chapter 5.

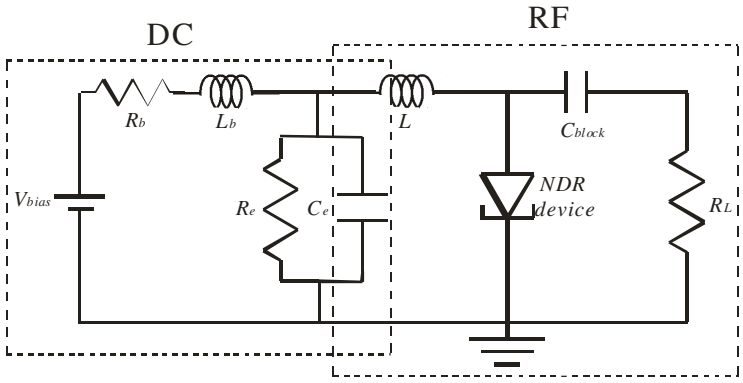

Figure 8.3: RTD oscillator with RF and DC separated by DC decoupling circuit (R_e, C_e). R_L is the load of the RTD oscillator. The inductance L and self-capacitance of the NDR device determine the frequency of oscillation.

A generic equivalent circuit is shown in Fig. 8.3 in which the DC and RF sections of the RTD oscillator circuit are clearly separated by a decoupling circuit, R_e and C_e. R_e is used to suppress the low-frequency parasitic oscillation from the DC bias and C_e is employed as a RF short circuit at the oscillation frequency. Fig. 8.4 shows the equivalent circuit of the Fig. 8.3. From Fig. 8.4, the admittance of NDR device part (Y_n) and external load network part (Y_L) at the design frequency (f_0) can be described by

$$Y_n = -G_n + jB_n \tag{8.18}$$

$$Y_L = G_L - jB_L \tag{8.19}$$

where $jB_n = j2\pi f_0 C_n$ and $jB_L = j/(2\pi f_0 L)$ are the susceptances of the NDR device part and load network part at the design frequency (f_0), respectively. $-G_n$ and $G_L = 1/R_L$ are the conductance of the NDR device and load network, re-

spectively.

This circuit can achieve maximum RF output power, if $G_L = G_n/2$, and $B_n = B_L$ at the desired frequency. Details have been discussed in section 8.2. The circuits shown in Figs. 8.2 and 8.3 were simulated in Advanced Design System (ADS) circuit simulation software with the model of a tunnel diode, the 1N3717 packaged tunnel diode to assess RF performance. The total inductance L was set as 2 nH. Fig. 8.5 shows the simulations results. The circuit of Fig. 8.3 provides -10.52 dBm output power compared to -17.6 dBm for the circuit in Fig. 8.2, i.e. 7 dB higher output power, and clearly the circuit of Fig. 8.3 is the better oscillator topology.

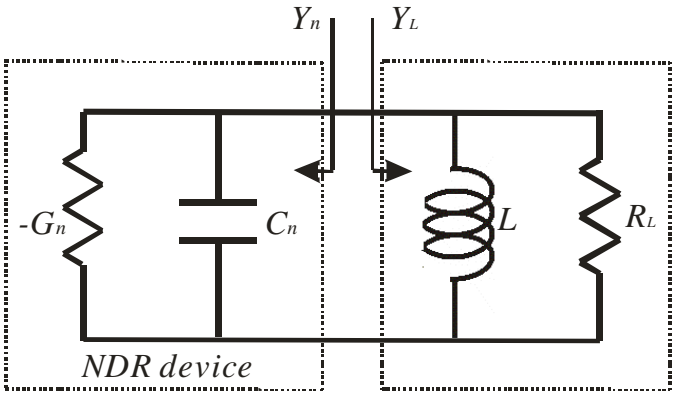

Figure 8.4: A small-signal RF equivalent circuit of Fig.8.3. The circuit can deliver maximum power to the load (G_L) if the conductance of the load is equal to half conductance of the NDR device at the bias point.

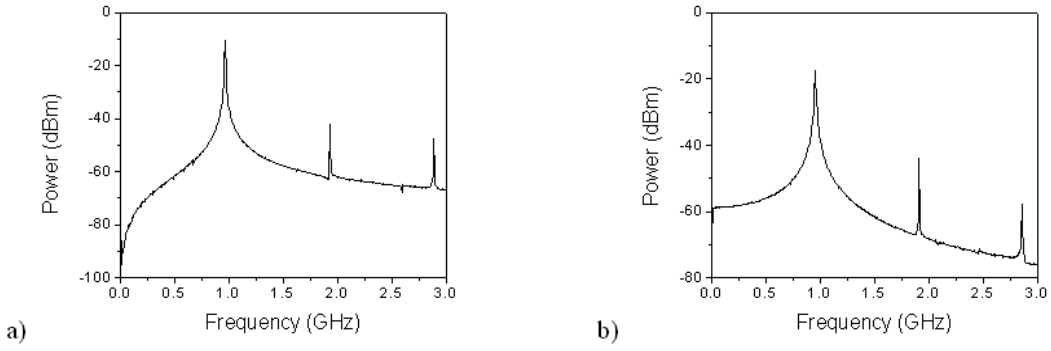

Figure 8.5: Simulation results of the tunnel diode oscillator with $R_e < 1/G_n$. $R_b = 1\ \Omega$, $L_b = 56$ nH, $L = 2$ nH, $R_e = 10\ \Omega$, $C_e = 2.5$ nF, $R_L = 50\ \Omega$, $C_{block} = 2.5$ nF and V_{bias} = 180 mV. a) The power delivered to the load (R_L) at 935 MHz is -10.8 dBm with an RF short circuit via $C_e = 2.5$ nF. b) The power delivered to the load (R_L) at 935 MHz is -17.6 dBm without C_e.

8.5 Limitations of the RTD waveguide oscillator

A brief description of the RTD waveguide oscillator was provided in section 1.2.2. The section summarises the analysis of such an oscillator as described in Ref.[63] and discusses this circuit from the perspective of the work described in this thesis. Fig. 8.6(a) shows the equivalent circuit for an RTD waveguide oscillator including the bias circuit [63]. $-R_n$ and C_n are the negative differential resistance and capacitance of the RTD, R_s is the series (contact and access) resistance of the device. The resistance R_c within the waveguide cavity is connected in series to the RTD in the oscillator circuit in order to improve the device stability, and L_w is the inductance of the whisker contact. The RF signal is isolated from the

DC bias by a low-pass filter (LPF). R_e, L_e and C_e are the circuit elements outside the oscillator cavity. R_b and L_b are the resistance and inductance from the DC source and bias line. C_{block} acts like a short circuit for RF signal but open circuit for the DC source.

At frequencies low enough to neglect the impedance of the RF load, and with a voltage source connected to the diode through the low pass filter (LPF), the circuit of Fig. 8.6(a) reduces to the circuit of Fig. 8.6(b). Several of the circuit elements in Fig. 8.6(a) are in series and so are combined as follows: $L = L_w + L_e + L_b$ and $R = R_s + R_c + R_e + R_b$. In Ref. [63], the circuit stability was analysed by considering the circuit of Fig. 8.6(b) from which it was found that for a given device, the stability criterion is

$$L < R_n^2 C_n \tag{8.20}$$

For RTD's with peak currents in the mA range (10-50 mA), typical values of R_n are tens of Ohms (15-40 Ω) and C_n are tens of femto-Farads (10-50 fF). This constrains L to a few picoHenrys (2-80 pH). Thus, very small bias inductances are required for stability [63]. There are therefore several disadvantages for the RTD waveguide oscillator:

a) Although the resistance R_c can be used for improving the device stability, it would, however, reduce the maximum frequency (cut-off frequency) that the device can achieve;

b) A large proportion R_c/R_n of the power generated by the RTD will be lost to the stabilising resistance, i.e. R_c [63];

c) Either the inductance from the DC bias line and the LPF or the RTD area (device size) needs to be minimised in order to achieve device stability [63]. However, the inductance of the bias lines is usually around a few hundred Henries ($\approx 200\ pH$) and may not be reduced further. Therefore, reducing the RTD area of the device is the only way to achieve circuit stability, which leads to low output power [63]; and

d) The LPF can be an inductor in which case the DC stability is very difficult to establish as discussed in chapter 2.

The reported RTD waveguide oscillators by Brown et al [40], [80] employed a lossy transmission line section along the bias line to minimise the parasitic oscillations. To the best of the author's knowledge, none of the published oscillators to date have utilised resistor R_c for stabilisation.

8.6 Power limitation of a single RTD oscillator

8.6.1 RTD devices for waveguide oscillators

As discussed in section 8.5, the inductance L (including bias inductance and contact pad inductance) of the RTD waveguide oscillator must satisfy equation

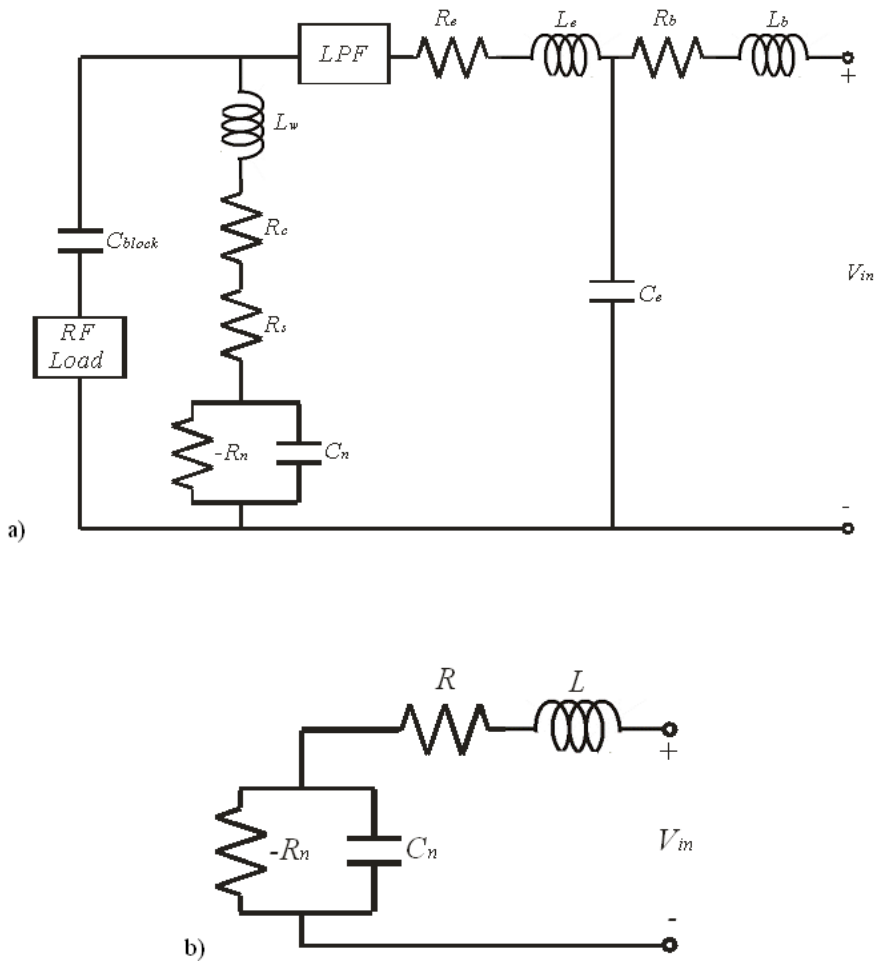

Figure 8.6: a) The equivalent circuit for a resonant tunnelling diode waveguide oscillator including the bias circuit. b) The equivalent circuit where series elements have been combined without an external capacitor [63].

(8.20) in order to achieve DC stability. Equation (8.20) can be re-written as

$$L < \left(\frac{2\Delta V}{3\Delta J\, A}\right)^2 AC_d \tag{8.21}$$

where ΔV is the peak-to-valley voltage difference, ΔJ is the current density difference between the peak and valley currents, A is the device area and C_d is the capacitance per unit area of the device. The cubic model for I-V characteristics has been used in equation (8.21). For the cubic model for the I-V characteristic of an RTD, $G_n = 3\Delta I/2\Delta V$. Therefore from the equation (8.21), the maximum device area can be given by

$$A_{\max 1} = \frac{4C_d}{9L}\left(\frac{\Delta V}{\Delta J}\right)^2 \tag{8.22}$$

where $A_{\max 1}$ is the maximum device area for the model of Kidner et al [63].

For the RTD waveguide oscillator, there is another expression for maximum device area given by Eisele et al [72], which is derived from the stability conditions derived by Hines [61], and can be expressed as

$$A_{\max 2} = \frac{2\rho_s C_d}{3L}\frac{\Delta V}{\Delta J} \tag{8.23}$$

where $A_{\max 2}$ is the maximum device area and ρ_s is the specific contact resistance. The cubic model for the I-V characteristics is used in equation (8.23) instead of the piece-wise linear model used in Ref. [72].

8.6.2 RTD devices for planar oscillators

Having given the maximum device area of waveguide RTD oscillators, the maximum device area of planar RTD oscillators will also be derived. As discussed in chapter 2 and 5, a stabilising resistor R_e should be used in the planar RTD oscillator design topology in order to suppress the low-frequency bias oscillations and it should satisfy the condition in equation (2.5), i.e. $R_e < 1/G_n$. Note that the device series parasitic resistance R_s can be considered part of the I-V characteristic (i.e. modifies the I-V characteristic) and does not have to be explicitly accounted for in the estimation of the device area to be derived below. For the cubic model for the I-V characteristic of an RTD, $G_n = 3\Delta I/2\Delta V$ and so

$$R_e < \frac{2\Delta V}{3\Delta I} \tag{8.24}$$

Equation (8.24) can be re-written as

$$R_e < \frac{2\Delta V}{3\Delta J A} \tag{8.25}$$

From equation (8.25) the maximum area of the RTD device used to form an oscillator can be approximated by

$$A_{\max 3} = \frac{2\Delta V}{3\Delta J\, R_e} \tag{8.26}$$

8.6.3 Estimation of RTD oscillator power from device sizes

The maximum output power can be obtained from the NDR device is given in equation (8.12) and it can be written as

$$P_{\max} = \frac{3}{16}\Delta I \Delta V = \frac{3}{16}\Delta J A_{\max} \Delta V \tag{8.27}$$

For any given material, according to equation (8.27), since the voltage difference ΔV and current difference between the peak current and valley current per unit area of the device ΔJ are fixed, the maximum RF output power depends on the maximum device area $A_{\max}$. The estimation of output power described here assumes that the parasitic series resistance R_s does not change with device size (actually reduces with increasing size).

Table 8.1 shows the calculated maximum device areas $A_{\max 1}$, $A_{\max 2}$, and $A_{\max 3}$ using equations (8.22), (8.23) and (8.26) respectively for different published InP-based AlAs/InGaAs/AlAs double-barrier quantum-well RTD structures (actual areas should be smaller that that give by these equations to ensure DC stability). The typical voltage differences ΔV of InP-based RTDs are between 0.2 V to 0.5 V [36], [38], [40], [83]. The peak and valley voltages (V_p and V_v) were estimated from the RTD I-V characteristics in the published papers, and the current density differences (ΔJ) were calculated from the given peak current density and peak to valley current ratio (PVCR). Specific contact resistances (ρ_s) given in the table are quoted from the referenced papers. The capacitances per unit area of the device (C_d) were calculated by using equation (1.2) for some published

RTD oscillators. The cut-off frequencies (f_c) given in the table are quoted from the referenced papers.

For the calculation of the maximum areas of the NDR devices used in waveguide RTD oscillators ($A_{\max 1}$ and $A_{\max 2}$), a value of inductance L is required. In practical waveguide RTD oscillators, this inductance L cannot be reduced beyond a certain value [63], and was set to 100 pH, which is the same value as that was used to calculate the maximum device areas ($A_{\max 1}$ and $A_{\max 2}$) in Ref. [72]. For the calculation of the maximum area of the NDR device used to form a planar RTD oscillator ($A_{\max 3}$), a value of resistance R_e is required. According to equation (8.26), the smaller the resistance R_e is the larger the maximum device area $A_{\max 3}$. However, the minimum value of R_e in a MMIC circuit is limited since very small values (a few Ohms) would consume higher DC power (essentially short circuit the DC supply), and as discussed in section 5.5.1, the oscillator DC-to-RF conversion efficiency would drop significantly (was $< 3\%$ for the hybrid circuits described in chapter 5 which used $R_e = 10\,\Omega$). Therefore R_e could be (and was) set to 10 Ω from which the maximum area (actual area should be smaller than that given by equation (8.26)) of an RTD in a planar RTD oscillator can be calculated. For commonly used Nichrome resistors in integrated circuit realization corresponds to a size of 40 $\mu m \times 100 \mu m$ for a typical sheet resistance of $50\Omega/\square$.

From the estimations of maximum device areas for stabilised RTD oscillators tabulated in Table 8.1, it is clear that RTD devices for planar RTD oscillators

($A_{\max 3}$) can be much larger (ranging from 3 to 1600 times) than those that could be used in waveguide RTD oscillators ($A_{\max 1}$ and $A_{\max 2}$). This means the planar RTD oscillators can deliver significantly more power than waveguide RTD oscillators. Note that some required device areas for waveguide oscillators are too small to be practically feasible. The estimation of output power described here assumes an ideal NDR device without parasitic elements. In the next section, the variation of output power with frequency which results from the device's parasitic elements will be discussed.

In earlier work by Kidner et al [63] and Eisele et al [72] on output power analysis of RTD waveguide oscillators, theoretical analysis showed that high output powers ($\backsim$10 dBm) at frequencies in excess of 100 GHz could be achieved if the oscillator circuits had no DC stability problems [28], [63], [72]. The analysis was based on a piece-wise linear model for the RTD I-V characteristics. In their approach, a load resistance of 1 Ω was assumed. Clearly, a load resistance of 1 Ω was unrealistic (alternatively such a normalised load was only suitable for analysis or making comparisons), and it is not surprising that to date no RTD oscillators with performance close to those predictions have been experimentally demonstrated. Also, the derived stability criteria for these RTD waveguide oscillators was not amenable to circuit implementation because of the difficulty in realising the required low inductance contact as highlighted in section 8.5, see equation (8.20).

Ref.	V_p	V_v	ΔJ	ρ_s	C_d	f_c	$A_{\max 1}$	$A_{\max 1}$	$A_{\max 3}$
	(V)	(V)	$\left(\frac{mA}{\mu m^2}\right)$	$\Omega\mu m^2$	$\left(\frac{fF}{\mu m^2}\right)$	(THz)	(μm^2)	(μm^2)	(μm^2)
[36]	1.4	0.9	3	3	5.86	2.7	0.72	0.02	11
[37]	0.95	1.35	9	3	3.52	1.1	0.03	0.003	2.1
[40]	0.5	0.75	0.75	48	12.35	0.9	6.1	1.32	21.9
[83]	0.9	1.30	2.75	2.2	3	2.2	0.28	0.006	9.7

Table 8.1: Calculated maximum device areas for some published RTD InP-based AlAs/InGaAs/AlAs double barrier quantum-well RTD structures. The resistance R_e is set to 10 Ω and L is set to 100 pH. V_p and V_v are the peak and valley voltages, ΔJ is the current density difference, C_d is the capacitance per unit area of the device and $f_{cut-off}$ is the cut-off frequency [36],[37], [40], [83]. A_{max1} and A_{max2} are the maximum device areas for the waveguide RTD oscillators from the models of Kidner et al [63] and Eisele et al [72], respectively. A_{max3} is the maximum device area of planar RTD oscillators derived here.

8.6.4 Output power and frequency

In the derivation of the RTD oscillator output power presented in section 8.2, the RTD equivalent circuit model did not include the device series resistance, R_s, and pad/contact inductance, L_s. Here, the limitation of these parasitic elements on cut-off frequency and output power will be discussed. The equivalent circuit model of an RTD including the parasitic series resistance R_s and inductance, L_s is shown in Fig. 8.7. The (equivalent) total resistance of the RTD is given by

$$R_s - \frac{G_n}{G_n^2 + \omega^2 C_n^2} \tag{8.28}$$

where R_s is the device series resistance, G_n is the magnitude of the conductance of he device ($G_n = 3\Delta I/2\Delta V$), C_n is the capacitance of the device and ω is the operating frequency. The frequency at which equation (8.28) is equal to zero is the cut-off frequency ω_c of the device and is given by [36], [63].

$$\omega_c = \frac{G_n}{C_n}\sqrt{\frac{1}{R_s G_n} - 1} \tag{8.29}$$

The RF equivalent circuit of a planar RTD parallel oscillator in which the RTD device model also includes the parasitic elements is shown in Fig. 8.8. This circuit can be re-drawn as shown in Fig. 8.9, where the total equivalent impedance (Z'_L) of the inductance L and the load G_L can be described by

$$Z'_L = \frac{\omega^2 L^2 G_L}{1 + \omega^2 L^2 G_L^2} + j\frac{\omega L}{1 + \omega^2 L^2 G_L^2} \tag{8.30}$$

The equivalent resistance R'_L and reactance X are described by

$$R'_L = \frac{\omega^2 L^2 G_L}{1 + \omega^2 L^2 G_L^2} \tag{8.31}$$

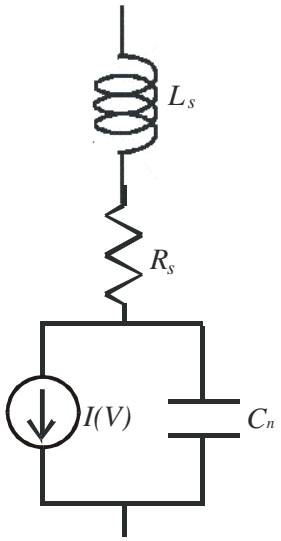

Figure 8.7: RTD model with series resistance R_s. C_n is the device capacitance and $I(V)$ is the voltage controlled current source.

$$X = \frac{\omega L}{1 + \omega^2 L^2 G_L^2} + \omega L_s \tag{8.32}$$

And the total impedance (as seen by the RTD), including the parasitic resistance, R_s, and inductance, L_s, inductance L and load G_L is given by

$$Z_{total} = R_s + R'_L + jX \tag{8.33}$$

Therefore, the cut-off frequency ω_{c_osc} of the oscillator circuit can be obtained from

$$R_s + \frac{\omega_{c\_osc}^2 L^2 G_L}{1 + \omega_{c\_osc}^2 L^2 G_L^2} - \frac{G_n}{G_n^2 + \omega_{c\_osc}^2 C_n^2} = 0 \tag{8.34}$$

Comparing equations (8.28) and (8.34), the circuit cut-off frequency ω_{c_osc} is lower than the device ω_c since the second term (on the left hand side) in eqn. (8.34) is positive. It is clear that the inductance L and load G_L affect the circuit cut-off

frequency besides the series resistance R_s, device capacitance C_n and the device conductance G_n.

Having discussed the cut-off frequency limitation for a parallel RTD oscillator, the limitation on the output power will now be discussed. Fig. 8.9b can be re-drawn as shown in Fig. 8.10, where the total admittance Y_{total} of series resistance R_s inductance L and load G_L can be given by

$$Y_{total} = \frac{1}{R_s + R'_L + jX} \tag{8.35}$$

Combining equations 8.31, 8.32 and 8.35, the equivalent conductance G'_L and susceptance B can be described as

$$G'_L = \frac{R_s + \frac{K}{1+KG_L}}{\left(R_s + \frac{K}{1+KG_L}\right)^2 + \left(\frac{\omega L}{1+KG_L} + \omega L_s\right)^2} \tag{8.36}$$

$$B = \frac{\frac{\omega L}{1+KG_L} + \omega L_s}{\left(R_s + \frac{K}{1+KG_L}\right)^2 + \left(\frac{\omega L}{1+KG_L} + \omega L_s\right)^2} \tag{8.37}$$

where $K = \omega^2 L^2 G_L$.

The resonant frequency ω_{res} of the equivalent circuit shown in Fig. 8.10 is given by

$$\omega C_n = B \tag{8.38}$$

with $\omega_{res} = \omega$.

For integrated monolithic RTD oscillators using this parallel topology, the parasitic series inductance L_s (which models the connection to the device) adds to the resonating inductance L (and so can be set to zero in the equations in this

section). With this simplification, it can be shown using equation (8.38) that

$$\omega_{res} = \frac{\sqrt{(L - C_n R_s^2)\, C_n}}{LC_n\,(1 + R_s G_L)} \tag{8.39}$$

From equation (8.39), it is clear that

$$L > C_n R_s^2 \tag{8.40}$$

if the resonant frequency is to be real. This means that if L is chosen to be less than $C_n R_s^2$ then the circuit becomes stable, i.e. equation (8.40) also provides an expression for the smallest possible inductance to realise an oscillator.

The circuit of Fig. 8.10 is identical to that in in Fig. 8.1 and so using the analysis in section 8.2, the power delivered to equivalent load G'_L (i.e. the power generated by the diode) can be given from equations (8.10) and (8.36) as

$$P'_L = \frac{2\,(G_n - G'_L)\, G'_L}{3b} \tag{8.41}$$

Referring to Fig. 8.9, since R'_L is an apparent load resistance due to the external circuit, and R'_L is in series with R_s, the power delivered to the load in terms of the power generated by the diode can be expressed by

$$P_L = \frac{2\,(G_n - G'_L)\, G'_L}{3b} \frac{R'_L}{R'_L + R_s} \tag{8.42}$$

The apparent load G'_L changes with increasing frequency and so does not present an ideal load for maximum output power, i.e. output power drops with increasing frequency. At any given frequency, an optimum value of the oscillator load G_L of may be found.

Approximate analysis of output power with frequency of tunnel diode oscillators was first provided in Reference [101] in which the equivalent resistance and inductance in equations (8.31) and (8.32) were assumed constant in the neighbourhood of the oscillation frequency. In the analysis presented here, no such assumptions are made. This analysis, however, does not include the effect of the tunnelling and transit times which modify the negative differential conductance G_n and and capacitance C_n of the device with increasing frequency [20], [36]. These are thought to manifest themselves as reactive components in the equivalent circuit, a so-called quantum-well inductance in series with the negative differential conductance [40] and additional device capacitance [36]. Therefore the maximum output power predicted by equation (8.42) should be considered as an upper limit on the maximum available output power. This is also because, to date, the intrinsic G_n is only an estimate as it has been impossible to determine it from the measured I-V curves which are usually distorted by oscillations (this may soon change with the introduction of the DC and RF characterisation techniques described in this thesis, chapters 3 and 4).

8.6.4.1 Simulated output power for some NDR devices

For the 1N3717 tunnel diode and the single device oscillator described in section 5.4, $G_n = a = 0.048\,S, C_n = 13\,pF$, $R_s = 1.09\ \Omega$, $L_s = 1.6\,nH$, $b = 2\frac{\Delta I}{(\Delta V)^3} = 4.09$ and $G_L = 0.02\,S$. The predicted output power versus frequency according

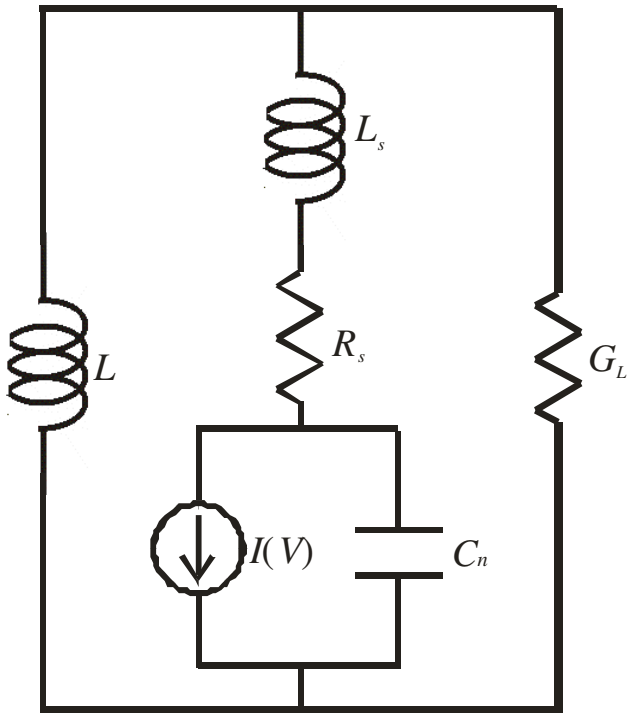

Figure 8.8: RF equivalent circuit of Fig. 8.3.

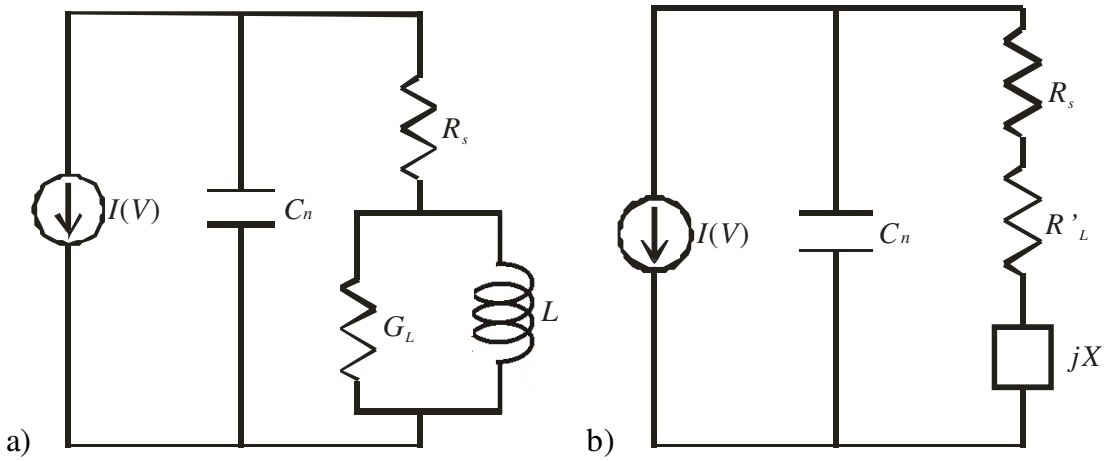

Figure 8.9: Re-drawn RF equivalent circuit of the circuit of Fig.8.8.

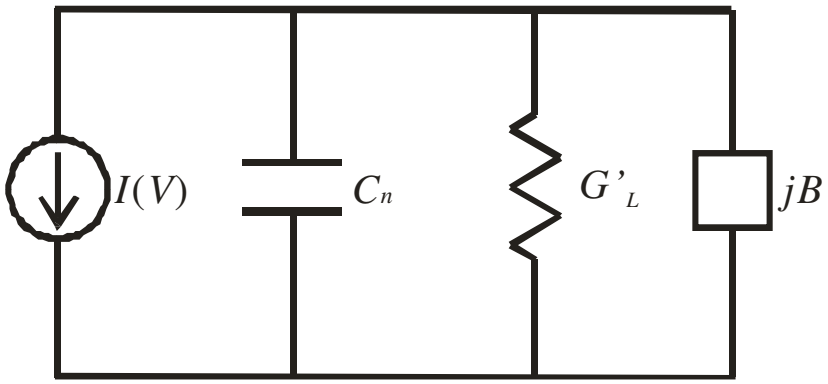

Figure 8.10: Parallel RTD oscillator with equivalent load conductance G'_L and equivalent parallel susceptance B.

to equation (8.42) is shown in Figure 8.11. For the simulation, the inductance L is first fixed, from which the frequency of oscillation ω calculated. R'_L and G'_L are then computed using (8.31) and (8.36), respectively. Here, L ranges from $0.1 - 100\ nH$. The simulation shows that the output power drops with frequency as expected. In comparison with the measured output power ($-10.17\,dBm$) of the 617 MHz oscillator using the 1N3717 tunnel diode, the predicted output power ($-11\,dBm$) is approximately 1 dB lower. This discrepancy may be due to the cubic model used to approximate the I-V characteristics of the tunnel diode. Note also that G_n (i.e. the I-V characteristic) was not modified to account for the explicit R_s, but the results should still be representative.

For the RTD used in the MMIC oscillators described in Chapter 7, the simulated output power versus frequency for the largest area RTD, i.e. resistor stabilised according to equation (8.26), is shown in Fig. 8.12. For this material,

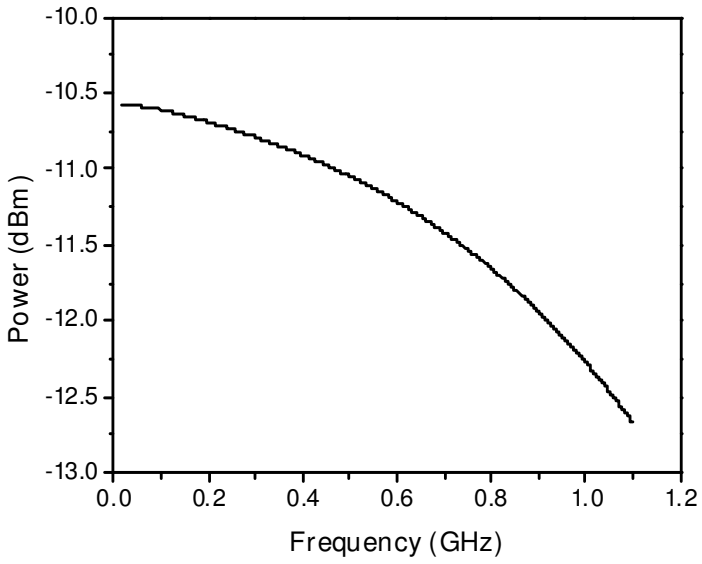

Figure 8.11: Simulated output power versus frequency for the 1N3717 tunnel diode.

$\Delta V = 1\,V$, $J_p = 10\,kA/cm^2$, $PVCR = 3$, and so with the stabilising resistance set to $R_e = 10\,\Omega$, the maximum device area, $A_{\max} = 1000\,\mu m^2$. For this device, $G_n = 0.1\,S, C_n = 9\,pF$, $R_s = 0.04\,\Omega$, $L_s = 0\,nH$, $b = 2\,(\Delta I)\,/\,(\Delta V)^3 = 0.067$ and $G_L = 0.05\,S$. R_s is estimated from the specific contact resistance of the AuNiGe-Ohmic contacts on n^+ InGaAs ($\rho_c = 3.5 \times 10^{-7}\,\Omega cm^2$) and the device area, while L_s is approximately zero (L_s becomes part of the resonating inductance L) in the MMIC implementation for the parallel oscillator topology. In the simulation, the resonating inductance L ranges from $5 - 1000\,pH$. The simulation results show that high RF output powers above 8 dBm ($> 6\ mW$) for frequencies up to 12 GHz are possible in this material system.

Output power analysis of recently published planar RTD MMIC oscillators

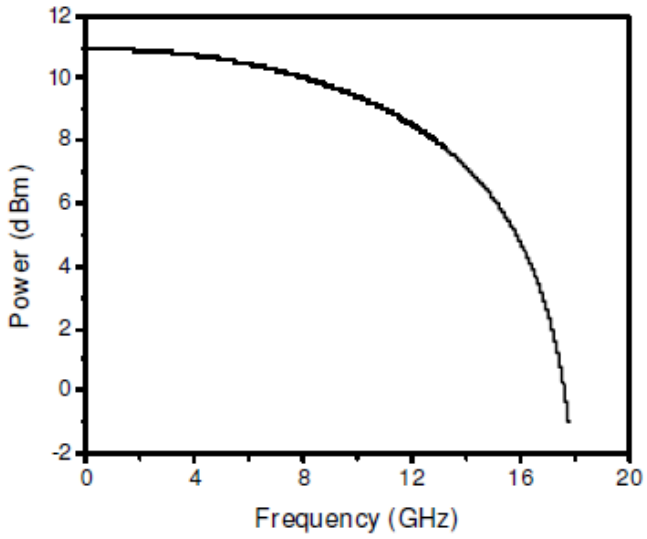

Figure 8.12: Simulated output power versus frequency for RTD layer structure used in the MMIC oscillators described in Chapter 7, Table 7.1.

employing resistor stabilisation was also carried out. For the oscillators described in Ref. [36], the layer structure had been grown on a semi-insulating InP substrate and was as follows (from top of the material): n^+ -GaInAs (30 nm), n -GaInAs (50 nm), GaInAs (undoped, 5 nm), AlAs, (undoped, 1.5 nm), GaInAs (undoped,4.5 nm), AlAs, (undoped, 1.5 nm), GaInAs (undoped, 5 nm), n-GaInAs (50 nm), n^+ -GaInAs (400 nm). The material had a peak current density a 400 kA/cm^2 and a current peak to valley ratio of $3.5 \backsim 4$. The peak-to-valley voltage difference (estimated from published I-V characteristics) was $0.5\,V$. From these parameters, the maximum device area was estimated to be $11\,\mu m^2$ (using equation (8.26)) and the device capacitance calculated to be $64.5\,fF$ (using equation (1.2)). R_s was estimated from the specific contact resistance of the Ti/Pd/Au-

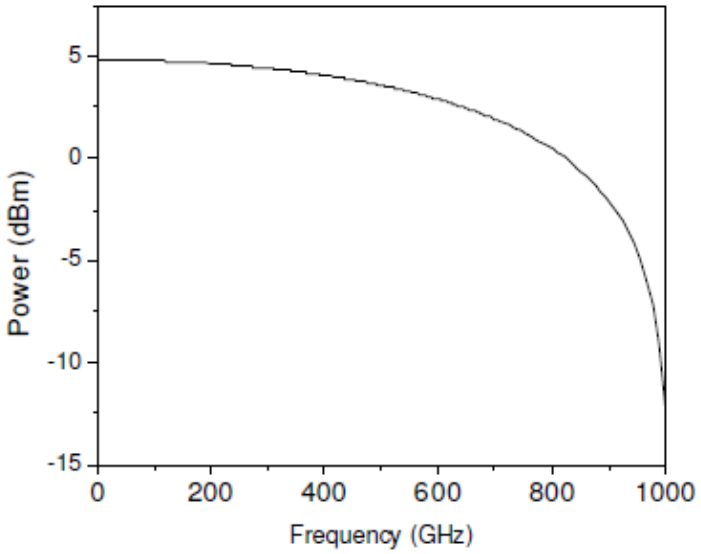

Figure 8.13: Simulated output power versus frequency for RTD layer structure in Ref. *[36].*

Ohmic contacts on n^+ InGaAs ($\rho_c = 3 \times 10^{-8}\,\Omega cm^2$, [145]) and the device area. The simulated output power versus frequency is shown in Fig. 8.13. Here, L ranges from $0.4 - 1000\ pH$. The simulations show that $\sim 0\ dBm$ ($\sim 1\ mW$) could be achieved at 800 GHz for a single diode oscillator in this material system. To achieve higher output powers, the power combining planar RTD oscillator design methodology discussed in chapter 5 could be employed. For instance, employing 2 RTDs with this material could provide 10 dBm (10 mW)output power up to 200 GHz! Fabricated oscillators in this material system employing $2 \times 2\ \mu m^2$ devices delivered $-22.2\ dBm$ ($6\ \mu W$) at around 600 GHz [36]. This performance could be significantly improved upon by proper device sizing and oscillator design.

In addition to neglecting the transit-time effects for the RTD structures analysed above (especially the structure of Ref. [36]), it was also assumed that each of the circuit elements in the model (Fig. 8.7 except for L_s) scales linearly (or inversely) with area. This is a good assumption for all the elements except the series resistance R_s, which usually has a component that depends sub-linearly on area because of current-spreading effects [146]. Therefore the predicted maximum output power should be considered as an upper limit on the maximum available output power at any given frequency.

8.7 Summary

Output power analysis of the parallel RTD oscillator topology has been discussed in this chapter. This oscillator topology can be stabilised resistively to eliminate bias oscillations. For a stabilised oscillator at low frequencies, an optimum load can be chosen for maximum output power. At high frequencies, the influence of parasitic elements start to dominate the oscillator performance and the output power reduces (if the low frequency load remains fixed). Analytical expressions derived for the variation of output power with frequency make it possible to optimise the oscillator load with increasing frequency, and so maintain a higher output power over a larger frequency range. The actual load to the oscillator can be matched to the optimal load by using impedance matching techniques. The chapter also summarised deficiencies of the waveguide RTD oscillator topology as

well as those of the planar RTD oscillator topology in which the output power is taken across the stabilising resistor.

CHAPTER 9

CONCLUSIONS AND FUTURE WORK

9.1 Conclusions

This thesis explored the stability of tunnel diodes and resonant tunnel diodes (RTD) and their application in realising high frequency oscillators. The following results were achieved:

a) Design equations for realising a stable test circuit that can be used in the accurate determination of the current-voltage (I-V) characteristics of tunnel diodes or RTDs were derived. The proposed approach eliminates both low frequency bias oscillations and high frequency oscillations which would otherwise distort the measured characteristics. Measured tunnel diode I-V characteristics confirmed the validity of the design criteria. No special circuit conditions (apart from the stabilising resistance R_e) such as minimising inductance in the circuit are required.

b) A method for the RF characterisation of negative differential resistance (NDR) devices was developed in which the NDR devices were embedded in a resistive stabilising pi-network topology. Measured device parameters were found by de-embedding the circuit elements in which the NDR device

was embedded, and from these, the small-signal equivalent model of the device at any bias point could be extracted. Experimental results obtained with this approach using a microstrip test-fixture and a packaged commercial tunnel diode demonstrated that accurate measurements could be made. The proposed methodology lends itself well to monolithic implementation for RF characterisation of high speed RTDs.

c) To address the problem of limited output power of tunnel diodes and RTDs, a novel oscillator design approach with two tunnel diodes in parallel but with each individually decoupled from the DC supply, was demonstrated. Experimental results showed that the output power of a two tunnel diode oscillator was double that of a single tunnel diode oscillator. Design guidelines for tunnel diode or RTD sinusoidal or quasi-sinusoidal oscillators were established from the Van der Pol model of the oscillator. In addition, a clear approach to biasing tunnel diodes or RTDs in oscillator circuits was presented. The fabricated circuits exhibited no low-frequency parasitic bias oscillations and no bias instability.

d) The series integration of NDR devices was also investigated. A method to suppress the DC instability in the network with several tunnel diodes or RTDs connected in series was proposed and experimentally validated. However, more effort is required to develop oscillator circuits employing series connected tunnelling devices.

e) MMIC RTD oscillators were designed and fabricated. The frequency and output power of the oscillators seem predictable although the output powers were very low ($\backsim$-20 dBm). As discussed in chapter 8, the oscillator topology employed was inefficient with the stabilising resistors consuming most of the power generated by the RTD.

9.2 Future work

The results obtained show that reliable RTD oscillator circuits can be designed to realise high frequency sources. The basic limitations to conventional design techniques were discussed in the thesis and new design approaches proposed. Further research is however required to investigate the reliability of the proposed techniques at millimetre-wave and submillimetre-wave frequencies.

The stabilised DC and RF characterisation circuit topologies developed in the thesis for tunnel diodes will make it possible to develop accurate small and large-signal models for RTDs. Such models will be invaluable to the future reliable design of RTD-based circuits.

The oscillator circuit topology discussed in Chapter 5 can easily be extended to use three or more NDR devices in order to scale up to higher output power. Fig. 9.1 illustrates the connection of several tunnelling devices to a common node that is grounded through an inductor. The technique lends itself to monolithic realisation of RTD oscillator circuits. Fig. 9.2 shows the top view and cross-section

of the MMIC layout of an oscillator employing two RTDs in coplanar waveguide technology. The resonating inductor is realised by the CPW short stub. Each RTD is located in the CPW slot and biased individually as illustrated. The RF output can be matched to the load. Based on the work described in this thesis, integrated circuits similar to this are currently being designed and fabricated by the High Frequency Electronics Group, University of Glasgow.

The proposed device sizing approach described in Chapter 8, section 8.6, together with circuit based power combining technique described in Chapter 5 can be used to realize high output power oscillators (say $\sim 0\,dBm$) which could be employed as local oscillators in very high frequency receiver circuits [147], [148]. The realisation of such signal sources in the $100 - 1000\,GHz$ frequency range would find use in many emerging areas such as imaging [149]. As a first step towards this, the predictions on the output power capability of planar RTD oscillator MMICs using suitably sized devices should be experimentally tested.

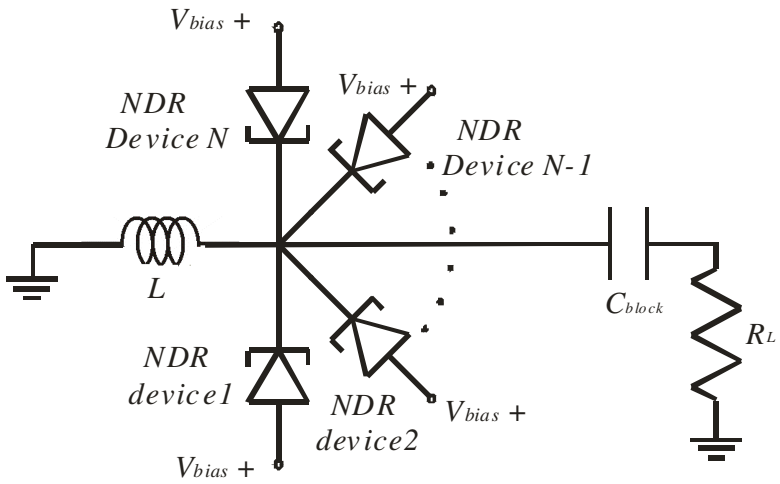

Figure 9.1: A N tunnel diodes/RTDs parallel-connected oscillator topology with individual DC decoupling circuit for each device.

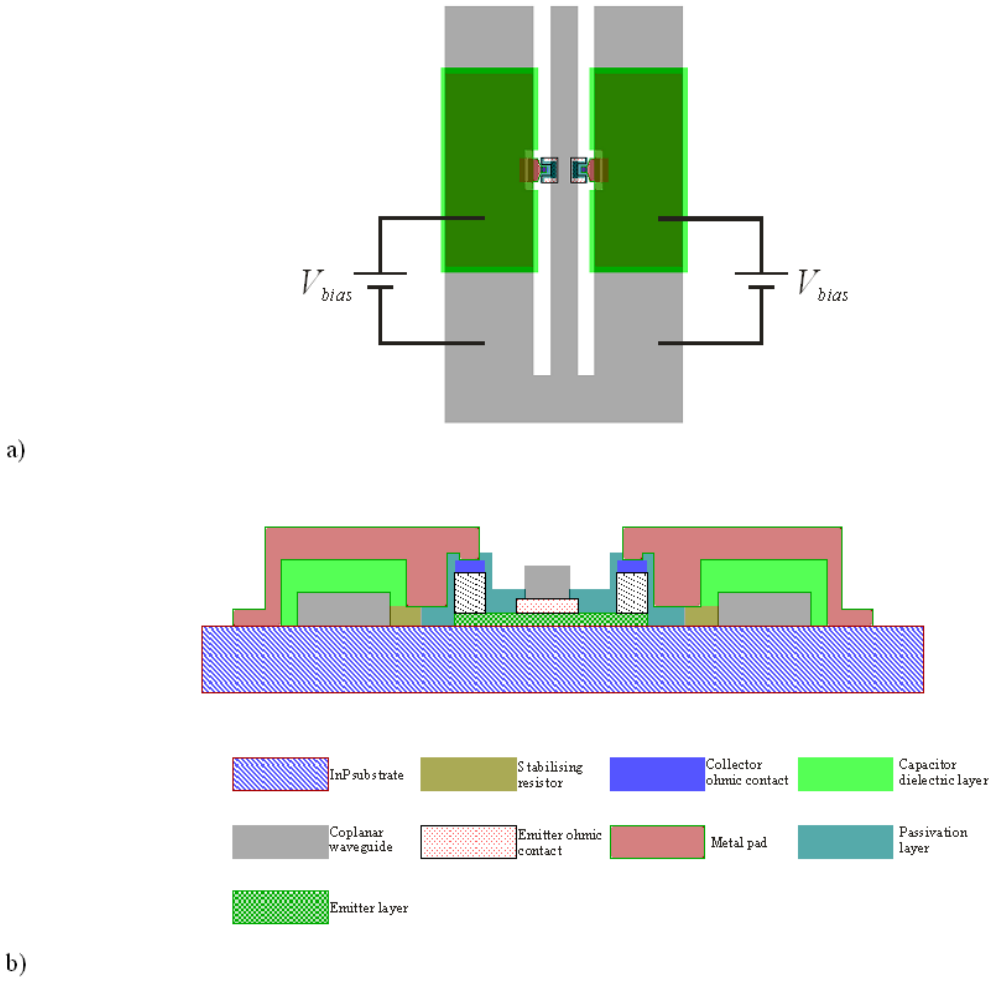

Figure 9.2: Top view (a) and the cross-section (b) of an illustration of a MMIC oscillator employing two RTDs.

APPENDICES

A. List of Abbreviations and Acronyms

ADS: advanced design system

Al: aluminum

AlAs: aluminium arsenide

Au: gold

Ar: argon

CH_4: methane

CHF_3: trifluoromethane

CPW: coplanar waveguide

DBQW: double-barrier quantum-well

DC: direct current

e-beam: electron-beam

GaAs: gallium arsenide

Ge: germanium

H_2: hydrogen

HBT: heterojunction bipolar transistor

HCl: hydrofluoric acid

HEMT: high electron mobility transistor

H_2O: water

H_2O_2: hydrogen peroxide

H_3PO_4: phosphoric acid

IMPATT: impact avalanche transit-time

InAlAs: indium aluminium arsenide

InAlGaAs: indium aluminium gallium arsenide

InGaAs: indium gallium arsenide

InP: indium phosphide

IPA : isopropyl alcohol

I-V: current-voltage

LAF : laminar air flow

LPF: low pass filter

MMIC: monolithic microwave integrated circuit

N_2: nitrogen

NDR: negative differential resistance

Ni: nickel

NiCr: nichrome

PCB: printed circuit boards

Pd: palladium

PDR: positive differential resistance

PECVD: plasma enhanced chemical vapour deposition

Pt: platinum

PVCR: peak to valley current ratio

q: the elementary charge, q$\approx 1.60\times 10^{-19}$C

RF: radio frequency

RTA: rapid thermal annealer

RTD: resonant tunnelling diode

RTD-LD: resonant tunnelling diode - laser diode

S-parameters: scattering parameters

SDA: semiconductor device analyzer

Si_3N_4: silicon nitride

SiO_2: silicon dioxide

SPA: semiconductor parameter analyzer

TML: transmission line

TMAH: tetramethylammonium hydroxide

Ti: titanium

TUNNET: tunnel injection transit-time

UV: ultraviolet

VNA: vector network analyser

Y-parameters: admittance parameters

ε_0: the permittivity of free space, $\varepsilon_0 \approx 8.854\times10^{-12}$ F/m

B. List of Symbols

C_{block}: DC block

C_e: external capacitance

C_n: device capacitance

C_p: package capacitance

C_{res}: capacitance of an external resonator

E_1: first resonant energy level

E_{cC}: conduction band of collector

E_{cE}: conduction band of emitter

E_{cn}: conduction band of n-type semiconductor

E_{FC}: Fermi-level of collector

E_{FE}: Fermi-level of emitter

E_{Fn}: Fermi-level of n-type semiconductor

E_{Fp}: Fermi-level of p-type semiconductor

E_{vp}: valence band of p-type semiconductor

G_L: load conductance

G_n: absolute value of device negative differential conductance

G_{nc}: absolute value of combined device conductance (in power combing circuit

topology)

I_p: peak current

I_v: valley voltage

$I(V)$: voltage controlled current source of an NDR device

L: total inductance between the external inductance and the NDR device

L_b: inductance associated with the bias line and supply

L_e: external inductance

L_l: series lumped inductance

L_p: package inductance

L_{res}: inductance of an external resonator

L_s: device series inductance

L_w: inductance of a whisker contact

R: total resistance between the external inductance and the NDR device

R_b: Resistance associated with the bias line and supply

R_c: resistance within the waveguide cavity

R_e: external resistance

R_L: load resistance

R_n: absolute value of device negative differential resistance

R_{n_min}: the minimum absolute value of device negative differential resistance

R_p: package resistance

R_s: device series resistance

R_{sh}: sheet resistance

V_{NDR_M}: bias point mid-way between peak and valley voltages

V_p: peak voltage

V_v: valley voltage

Y_{ext}: external circuit admittance

Y_L: load network admittance

Y_n: device admittance

C. RTD Oscillator Fabrication Process

Sample cleaning

Ultrasonic bath in acetone for 5 minutes.

Ultrasonic bath in methanol for 5 minutes.

Ultrasonic bath in IPA for 5 minutes.

Rinse in de-ionised water for 5 minutes.

Blow dry with N_2.

Alignment makers and collector contacts

Spin S1818 at 4000 rpm for 120 seconds.

Bake on hotplate at 65°C for 120 seconds.

Post-develop in 1:1 Microposit(R) Developer Concentrate: H_2O for 60 seconds.

Expose using MA6 for 5 seconds.

Develop with 1:1 Microposit(R) Developer Concentrate: H_2O for 75 seconds.

Rinse in de-ionised water for 30 seconds.

Blow dry with N_2.

Ash at 80W for 3 minutes.

Remove the surface oxide in 1:10 HCl:H_2O for 60 seconds.

Rinse in de-ionised water.

Blow dry with N_2.

Deposit n-type ohmic contact using electron beam metal evaporator (Plassys I or II).

Soak in acetone at 50°C for 30 minutes.

Transfer to IPA.

Blow dry with N_2.

Etch to emitter layer

Deposit 200 nm of PECVD SiO_2.

Spin S1818 at 4000rpm for 30 seconds.

Bake on hotplate at 115°C for 90 seconds.

Expose using MA6 for 5 seconds.

Develop with 1:1 Microposit(R) Developer Concentrate: H_2O for 75 seconds.

Rinse in de-ionised water for 30 seconds.

Blow dry with N_2.

Etch by CHF_3/Ar in 80 plus RIE for 10 min

Agitate in 1:1:38 H_20_2:H_3PO_4:H_2O for 40 seconds.

Rinse in de-ionised water for 2 minutes.

Blow dry with N_2.

Agitate in 3:1 HCl: H_2O for 60 seconds

Rinse in de-ionised water for 5 minutes.

Blow dry with N_2.

Etch by CH_4/H_2 in ET340 for 40 minutes.

Agitate in 3:1 HCl: H_2O for 60 seconds

Rinse in de-ionised water for 2 minutes.

Blow dry with N_2.

Agitate in 1:10 HCl: H_2O for 2 minutes.

Rinse in de-ionised water for 2 minutes.

Blow dry with N_2.

Emitter contacts

Spin S1818 at 4000 rpm for 120 seconds.

Bake on hotplate at 65°C for 120 seconds.

Post-develop in 1:1 Microposit(R) Developer Concentrate: H_2O for 60 seconds.

Expose using MA 6 for 5 seconds.

Develop with 1:1 Microposit(R) Developer Concentrate: H_2O for 75 seconds.

Rinse in de-ionised water for 30 seconds.

Blow dry with N_2.

Ash at 80W for 3 minutes.

Remove the surface oxide in 1:10 HCl:H_2O for 60 seconds.

Rinse in de-ionised water.

Blow dry with N_2.

Deposit n-type ohmic contact using electron beam metal evaporator (Plassys I or II).

Soak in acetone at 50°C for 30 minutes.

Transfer to IPA.

Blow dry with N_2.

Anneal sample in RTA at 380°C for 1 minute.

Etch to substrate

Spin S1818 at 4000rpm for 30 seconds,

Bake on hotplate at 115°C for 90 seconds

Expose using MA 6 for 5 seconds.

Develop with 1:1 Microposit(R) Developer Concentrate: H_2O for 75 seconds.

Rinse in de-ionised water for 30 seconds.

Blow dry with N_2.

Ash at 80W for 3 minutes.

Agitate in 1:1:38 H_2O_2:H_3PO_4:H_2O for 4 minutes.

Rinse in de-ionised water for 2 minutes.

Blow dry with N_2.

Passivation

Pour 5:1 VM651: H_2O on the sample and wait for 20 seconds.

Spin 5:1 VM651: H_2O at 4000rpm for 5 seconds.

Bake on hotplate at 120°C for 60 seconds.

Spin polyimide at 500 rpm for 5 seconds.

Spin polyimide at 4000 rpm for 30 seconds.

Bake on hotplate at 140°C for 20 minutes.

Spin S1818 at 4000 rpm for 30 seconds,

Bake on hotplate at 115°C for 90 seconds

Expose using MA 6 for 11 seconds.

Develop in 1:41 Tetramethylammonium Hydroxide (TMAH):H_2O solution for 20 seconds.

Strip resist in Acetone

Post bake on hot plate at 140°C for 5 minutes

Post bake in oven at180°C for 30 minutes

Shunt resistor

Spin S1818 at 4000 rpm for 120 seconds.

Bake on hotplate at 65°C for 120 seconds.

Post-develop in 1:1 Microposit(R) Developer Concentrate: H_2O for 60 seconds.

Expose using MA 6 for 5 seconds.

Develop with 1:1 Microposit(R) Developer Concentrate: H_2O for 75 seconds.

Rinse in de-ionised water for 30 seconds.

Blow dry with N_2.

Ash at 80W for 3 minutes.

Remove the surface oxide in 1:10 HCl:H_2O for 60 seconds.

Rinse in de-ionised water.

Blow dry with N2.

Deposit 33 nm NiCr using electron beam metal evaporator ((Plassys I or II).

Soak in acetone at 50°C for 30 minutes.

Transfer to IPA.

Blow dry with N_2.

Bond pad and CPW

Spin S1818 at 4000 rpm for 120 seconds.

Bake on hotplate at 65°C for 120 seconds.

Post-develop in 1:1 Microposit(R) Developer Concentrate: H_2O for 60 seconds.

Expose using MA 6 for 5 seconds.

Develop with 1:1 Microposit(R) Developer Concentrate: H_2O for 75 seconds.

Rinse in de-ionised water for 30 seconds.

Blow dry with N_2.

Ash at 80W for 3 minutes.

Remove the surface oxide in 1:10 HCl: H_2O for 60 seconds.

Rinse in de-ionised water.

Blow dry with N_2.

Deposit metal pad using electron beam metal evaporator (Plassys I).

Soak in acetone at 50°C for 30 minutes.

Transfer to IPA.

Blow dry with N_2.

D. Fundamental constants

Elementary charge, $q = 1.6 \times 10^{-19}\ C$

Permittivity of free space, $\varepsilon_0 = 8.854 \times 10^{-12}\ F/m$

E. Datasheet of tunnel diodes 1N3717 and 1N3714

The typical specifications of 1N3717 and 1N3714 packaged Germanium tunnel diodes from American Microsemiconductors are shown in Tables 9.1 and 9.2, respectively [150], [151].

Property	**Typical value**
Maximum peak current	4.7 mA
Peak current tolerance	0.12 mA
Total capacitance	25 pF
Minimum peak to valley current ratio	7.6
Peak voltage	65 mV
Valley voltage	355 mV
Cut-off frequency	3.4 GHz
Series inductance	0.5 nH
Series resistance	0.52 Ohms
Negative resistance	24 Ohms
Semiconductor material	Germanium
Package style	DO-17

Table 9.1: Typical specifications of tunnel diode 1N3717

Property	**Typical value**
Maximum peak current	2.2 mA
Peak current tolerance	0.20 mA
Total capacitance	25 pF
Minimum peak to valley current ratio	4.2
Peak voltage	65 mV
Valley voltage	350 mV
Cut-off frequency	2.2 GHz
Series inductance	0.5 nH
Series resistance	1.0 Ohms
Negative resistance	55 Ohms
Semiconductor material	Germanium
Package style	DO-17

Table 9.2: Typical specifications of tunnel diode 1N3714

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