UNIVERSITY OF GLASGOW

AlN/GaN MOS-HEMTs Technology

by

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Abstract

The ever increasing demand for higher power devices at higher frequencies has prompted much research recently into the aluminium nitride/gallium nitride high electron mobility transistors (AlN/GaN HEMTs) in response to theoretical predictions of higher performance devices. Despite having superior material properties such as higher two-dimensional electron gas (2DEG) densities and larger breakdown field as compared to the conventional aluminium gallium nitride (AlGaN)/GaN HEMTs, the AlN/GaN devices suffer from surface sensitivity, high leakage currents and high Ohmic contact resistances. Having very thin AlN barrier layer of $\sim 3\,\text{nm}$ makes the epilayers very sensitive to liquids coming in contact with the surface. Exposure to any chemical solutions during device processing degrades the surface properties, resulting in poor device performance. To overcome the problems, a protective layer is employed during fabrication of AlN/GaN-based devices. However, in the presence of the protective/passivation layers, formation of low Ohmic resistance source and drain contact becomes even more difficult.

In this work, thermally grown aluminium oxide (Al_2O_3) was used as a gate dielectric and surface passivation for AlN/GaN metal-oxide-semiconductor (MOS)-HEMTs. Most importantly, the Al_2O_3 acts as a protection layer during device processing. The developed technique allows for a simple and effective wet etching optimisation using $16H_3PO_4$:HNO_3:$2H_2O$ solution to remove Al from the Ohmic contact regions prior to the formation of Al_2O_3 and Ohmic metallisation. Low Ohmic contact resistance ($0.76\,\Omega$.mm) as well as low sheet resistance ($318\,\Omega/\square$) were obtained after optimisation.

Significant reduction in the gate leakage currents was observed when employing an additional layer of thermally grown Al_2O_3 on the mesa sidewalls, particularly in the region where the gate metallisation overlaps with the exposed channel edge. A high peak current $\sim 1.5\,\text{A/mm}$ at $V_{GS} = +3\,\text{V}$ and a current-gain cutoff frequency, f_T, and maximum oscillation frequency, f_{MAX}, of 50 GHz and 40 GHz, respectively, were obtained for a device with $0.2\,\mu$m gate length and $100\,\mu$m gate width. The measured breakdown voltage, V_{BR}, of a two-finger MOS-HEMT with $0.5\,\mu$m gate length and $100\,\mu$m gate width was 58 V.

Additionally, an approach based on an accurate estimate of all the small-signal

equivalent circuit elements followed by optimisation of these to get the actual element values was also developed for AlN/GaN MOS-HEMTs. The extracted element values provide feedback for further device process optimisation. The achieved results indicate the suitability of thermally grown Al_2O_3 for AlN/GaN-based MOS-HEMT technology for future high frequency power applications.

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List of abbreviations/symbols

AFM atomic force microscope

AlN aluminium nitride

AlGaN aluminium gallium nitride

Al aluminium

Al_2O_3 aluminium oxide

Ar argon

BCl_3 boron trichloride

Cat-CVD catalytic chemical vapor deposition

CAD computer-aided design

CATS computer aided transformation software

CH_4 methane

CMU capcitance measurement unit

Cl_2 chlorine

CPW co-planar waveguide

CV capacitance-voltage

DC direct-current

D-mode depletion mode

DI de-ionised

DUT device under test

e-beam electron beam

EBL electron beam lithography

EBPG5 electron beam pattern generator 5

ECR-RIE electron cyclotron resonance reactive ion etching

E-mode enhancement mode

FET field effect transistor

FE Field Emission

f_{MAX} maximum oscillation frequency

f_T current-gain cutoff frequency

4**H-SiC** 4 hexagonal silicon carbide

G_{max} maximum extrinsic transconductance

GaAs gallium arsenide

GaN gallium nitride

GHz gigahertz

GSG ground signal ground

HCl hydrochloric

HFET heterostructure field effect transistor

HEMT high electron mobility transistor

HPSI high purity semi-insulating

HR high resistivity

I_{DSmax} maximum drain current

ISS impedance standard substrate

ICP inductively coupled plasma

ICP-RIE inductively coupled plasma reactive ion etching

InP indium phosphide

IPA Isopropyl alcohol

IV current-voltage

L_G gate length

LOR Liftoff resist

L_T transfer length

MBE molecular beam epitaxy

MIBK methyl isobutyl ketone

MIS-HEMT metal-insulator-semiconductor high electron mobility transistor

MOCVD metal organic chemical vapour deposition

MOS metal-oxide-semiconductor

MMICs monolithic microwave integrated circuits

MOS-HEMT metal-oxide-semiconductor high electron mobility transistor

MW molecular weight

n_s 2DEG sheet carrier concentration

P_{Dmax} maximum power density

P_{PE} piezoelectric polarization

P_{SP} spontaneous polarization

PAMBE plasma assisted molecular beam epitaxy

PAE power added efficiency

PECVD plasma enhanced chemical vapor deposition

PMMA poly methyl methacrylate

R_C contact resistance

RF radio-frequency

RPM revolution per minute

R_{sh} sheet resistance

RT room temperature

RTA rapid thermal annealing

RIE reactive ion etching

SBH Schottky barrier height

sccm standard cubic centimeters per minute

SCUU SMU CMU unify unit

SEM scanning electron microscope

SOLT short-open-load-thru

Si silicon

SI semi-insulating

SiC silicon carbide

$SiCl_4$ silicon tetrachloride

SMU source monitor unit

SPA semiconductor parameter analyser

TE Thermionic emission

TFE Thermionic field emission

TLM transmission line method

2**DEG** two-dimensional electron gas

UID unintentionally doped

UV ultraviolet

V_{TH} threshold voltage

W_G gate width

Chapter 1

Introduction

1.1 GaN-based HEMT Technology

Gallium nitride (GaN) -based high electron mobility transistors (HEMTs), and in particular aluminium gallium nitride (AlGaN)/GaN devices, have become one of the most promising solid-state microwave power devices due to their ability to produce higher power densities at higher frequencies as compared to silicon (Si) and gallium arsenide (GaAs)-based devices. This is attributed to a unique combination of GaN material properties, including wide bandgap (3.4 eV of GaN to 6.2 eV of AlN), large electric breakdown field strengths ($\sim 3 \times 10^6$ V/cm) and high saturation electron drift velocity ($> 2 \times 10^7$ cm/s). These properties are given in Table 1.1, including a wide range of common semiconductor materials for comparison to GaN. Semiconductors featuring a large energy bandgap can be used to build transistors which operate at much higher temperatures, sustain greater voltage levels, and handle higher signal power levels than is possible with smaller bandgap conventional materials such as Si, GaAs and indium phosphide (InP).

GaN-based HEMTs are attracting considerable attention for amplifiers operating at higher power levels, high temperatures and in robust environments. Example application areas include radar, missiles, satellites, as well as in low-cost compact

TABLE 1.1: Semiconductor Properties [3],[4]

Parameter (Units)	Si	GaAs	InP	4H-SiC	GaN
Energy bandgap (eV)	1.12	1.43	1.34	3.2	3.4
Relative dielectric constant, ε_r	11.9	12.5	12.4	10.0	9.5
Thermal conductivity (W/Kcm)	1.5	0.54	0.67	4	1.3
Breakdown electric field (MV/cm)	0.3	0.4	0.45	3.5	3.3
Saturated electron velocity (10^7 cm/s)	1	1	1	2	2.5
Electron mobility (cm^2/Vs)	1500	8500	5400	700	900

amplifiers for wireless base stations. More applications areas for GaN-based electronics are illustrated in Fig. 1.1, which include automotive industry, defence and millitary applications, high frequency Monolithic Microwave Integrated Circuits (MMICs), radar and space applications, high power amplifiers for wireless base stations, and high voltage electronics for power transmission lines.

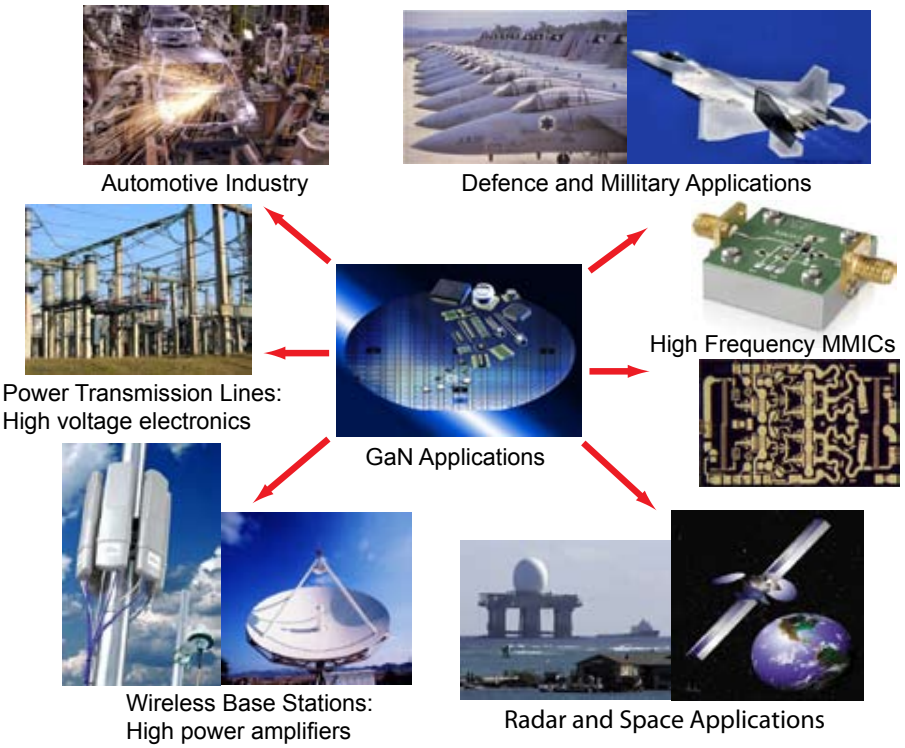


FIGURE 1.1: Example applications areas of GaN-based transistors.

1.2 GaN-based HEMT Theory

1.2.1 Basic HEMT Structure

A device structure of particular interest for high power and/or high frequency applications is the GaN-based HEMT. In contrast to other conventional III-V HEMTs which require n-type doping, polarization doping related to the piezoelectric and spontaneous polarization induced electric fields in nitride-based (III-N) HEMTs and large conduction and valence band discontinuities at the heterointerfaces in this material system enables extremely high sheet carrier densities in GaN device channels.

Typical $Al_xGa_{1-x}N$/GaN and all-binary AlN/GaN HEMT basic structures are shown in Fig. 1.2 and Fig. 1.3, respectively. Two common methods used for the epitaxial material growth are molecular beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD) (as reported in Table 1.4). The typical epitaxial structure for both heterostructures consists of (from top to bottom) the following layers;

Cap layer Usually a thin GaN layer (1-2 nm) is deposited on top of the barrier layer to prevent the epitaxial surface from the oxidation and to form low resistance Ohmic contact on the heterostructures. It also lowers the surface electric field.

Barrier layer This is the most critical layer in HEMT structure. It is a material with a wider bandgap than the channel layer. In this case $Al_xGa_{1-x}N$ or binary AlN. The bandgap depends on the aluminium mole fraction, x, in the material.

Channel/buffer layer This is the material with the lower bandgap than the barrier layer, a semi-insulating (SI) or high resistivity GaN layer to ensure proper drain-source current saturation, complete channel pinch-off, low loss at high frequencies, and low cross-talk between adjacent devices.

Nucleation layer The insertion of this layer depends on the material of substrate and the choice of epitaxial growth technique (e.g., MBE or MOCVD) used to grow the epitaxial layers. Usually very thin AlN, AlGaN or GaN is grown before growing a thicker semi-insulating (SI) GaN buffer layer. The purpose of this interlayer is to reduce stress and lattice mismatch to the non-native substrate.

Substrate Due to the lack of a native substrate, GaN epitaxy is grown on a non-native material substrate such as SI SiC [5], c-plane sapphire (Al_2O_3) [6] or Si(111) [7] (as reported in Table 1.4).

Upon growth of the HEMT structure, three metal contacts, source (S), gate (G), and drain (D) are made to the top AlGaN or AlN barrier layer as shown in shown in Fig. 1.2 or Fig. 1.3. Both the source and drain terminals are Ohmic contacts; they provide the means of controlling the carriers in the direction parallel to the heterointerface. The source is typically grounded while a positive bias is applied to the drain, thus forcing the electrons in the 2DEG to flow from source to drain. The applied voltage between the drain and source is called V_{DS}, while the gate-source voltage is called V_{GS}.

The gate terminal is a metal-semiconductor rectifying contact (Schottky barrier contact). The Schottky gate controls the potential distribution of heterostructure below the contact and can reduce the carrier concentration in the channel through the application of a negative bias. By applying a large negative gate bias, the channel becomes depleted of carriers, and thus, no current can flow between the drain and source. The gate bias required to pinch-off the channel is called the threshold voltage (V_T). If the threshold voltage is negative, then the device is called a depletion-mode (D-mode) HEMT. When it is positive the device is then called an enhancement-mode (E-mode) device. Conventional AlGaN/GaN HEMTs are D-mode transistors.

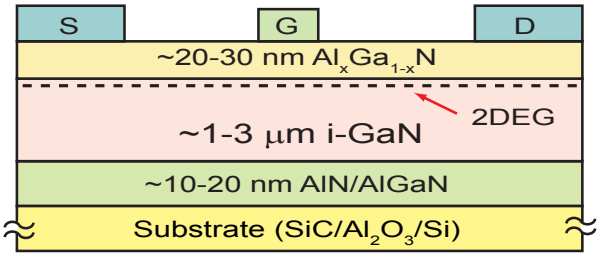


FIGURE 1.2: Basic structure of AlGaN/GaN HEMT.

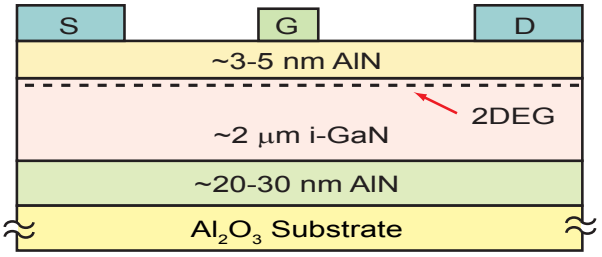
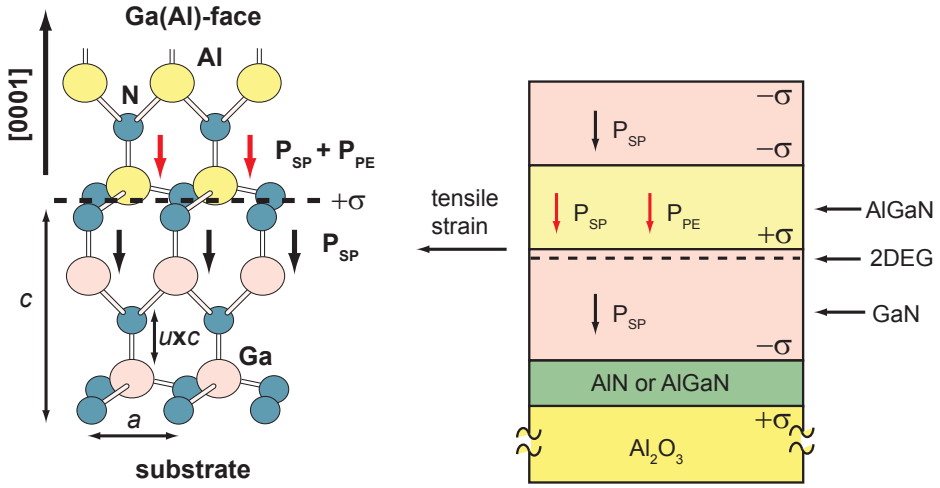


FIGURE 1.3: Basic structure of AlN/GaN HEMT.

1.2.2 Spontaneous and Piezoelectric Polarization Effects

The crystal structure of GaN is hexagonal or wurtzite, where the bilayers consist of two closely spaced hexagonal layers, one formed by Ga atoms and the other formed by N atoms as shown in Fig. 1.4(a). The lack of inversion symmetry with the strong ionicity of the covalent bonds leads to the polarization vectors, and these polarization vectors are additive along the *c*-direction, resulting in a macroscopic polarization. This polarization effect is referred to as spontaneous polarization, P_{SP}, since it occurs without any external field. When a thin AlGaN barrier layer is grown on the GaN buffer layer, both layers experience strain caused by lattice mismatch. This strain yields a well-known piezoelectric polarization, P_{PE}, by increasing non-ideality of the crystal lattice [1].

Increasing the Al-content in the strained AlGaN leads to an increase in piezoelectric polarization, P_{PE}. Fig. 1.4(b) shows polarization induced sheet charge and direction of the spontaneous and piezoelectric polarization in Ga-face strained AlGaN/GaN structure. The polarization induced charge density, σ (C/cm^2), is



(a) (b)

FIGURE 1.4: (a) Crystal structure of wurtzite Ga(Al)-face GaN and (b) Polarization induced sheet charge and direction of the spontaneous and piezoelectric polarization in Ga-face strained AlGaN/GaN heterostructures [1].

related to polarization vectors by Eqn. 1.1

$$\sigma(x) = P_{SP,AlGaN}(x) + P_{PE,AlGaN}(x) - P_{SP,GaN} \tag{1.1}$$

By increasing the Al-content of the AlGaN layer, the overall polarization induced charge density increases. An energy band diagram of the AlGaN/GaN structure is shown in Fig. 1.5, where the bandgap difference between AlGaN and GaN creates a large conduction band offset, $\triangle E_C$. The conduction band offset effectively forms a potential well at the AlGaN/GaN interface.

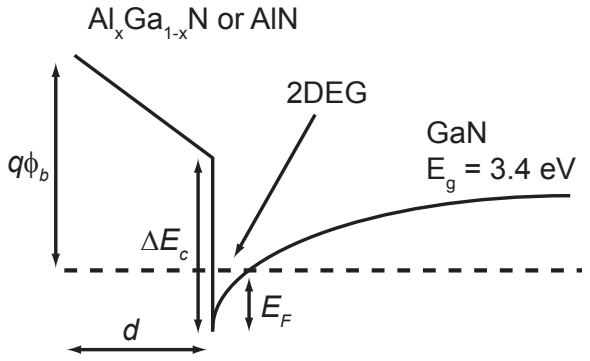


FIGURE 1.5: Band diagram of the $Al_xGa_{1-x}N$/GaN or AlN/GaN heterojunction. Electron accumulation and 2DEG formation at the interface.

Free electrons tend to compensate a positive polarization induced sheet charge ($+\sigma$) which is bound at the lower AlGaN/GaN interface for Ga(Al)-face structures as shown in Fig. 1.4(b). The value of the total polarization induced sheet charge is the same in heterostructures of different polarities for a given Al concentration and strain of the barrier. For undoped Ga-face AlGaN/GaN structures, the sheet electron concentration $n_s(x)$ can be calculated by using the total bound sheet charge $\sigma(x)$ and is given by the Eqn. 1.2 [1]:

$$n_s(x) = \frac{\sigma(x)}{q} - (\frac{\epsilon_0\epsilon_r(x)}{d_{AlGaN}q^2})[e\phi_b(x) + E_F(x) - \triangle E_C(x)] \tag{1.2}$$

where q is the electron charge, ϵ_0 is the vacuum permittivity, ϵ_r is the relative dielectric constant of the AlGaN layer, d_{AlGaN} is the thickness of the barrier layer, $q\phi_b(x)$ is the Schottky barrier height, E_F is the Fermi level with respect to the GaN conduction-band-edge energy, and $\triangle E_C$ is the conduction band offset at the AlGaN/GaN interface where a 2DEG forms.

As the electrons are confined in a two-dimensional (2D) quantum well, bulk scattering effects such as ionized impurity scattering are reduced, resulting in much higher mobility than for bulk GaN. As the quantum well is formed at the AlGaN/GaN interface, the main factors influencing 2DEG mobility are interface, alloy and dislocation scattering. Modified AlGaN/AlN/GaN structures, which employ a thin AlN interfacial layer between AlGaN and GaN layers, show higher 2DEG mobilities than those of conventional AlGaN/GaN structures [8]. This high performance is achieved due to the increased $\triangle E_C$, which effectively suppresses the electron penetration from the GaN channel into the AlGaN layer, and so reduces alloy disorder scattering.

As mentioned earlier, the 2DEG concentration in the unintentionally doped AlGaN/GaN structure has a strong dependence on the Al-content of the AlGaN barrier and, to a lesser extent, its thickness [9]. Numerical simulations of the AlGaN/GaN heterostructure demonstrate this clearly. Fig. 1.6 shows simulated 2DEG sheet charge density as a function of Al-content in the barrier layer using Eq. 1.2 [1]. Note that the number of electrons in the 2DEG (sheet charge density)

increases rapidly once a critical barrier thickness is exceeded, then gradually flattens out. Therefore, in order to achieve high power densities for RF/microwave devices, high current handling capability or low on-state resistance (for switching devices), it seems effective to use AlGaN/GaN heterostructures with high Al-content [9], [10]. However, difficulties in making good quality ohmic contacts and in the growth of high Al-content barrier devices have hampered this approach, but devices of 40 - 50 % Al-content have been reported [9].

As illustrated in Fig. 1.6, for a given 2DEG sheet charge density a thinner AlGaN barrier layer is required if the Al-content in the barrier is higher. In fact, the highest 2DEG sheet density can be achieved with the thinnest barrier layer for 100 % Al-content. For instance, for a 2DEG sheet density of $2 \times 10^{13}\,\mathrm{cm}^{-2}$ only $\sim 3.5\,\mathrm{nm}$ thick of AlN barrier layer is needed. This seems like an ideal combination for the realisation of normally-off (or E-mode) devices since a thin barrier would make it possible to deplete the channel with a Schottky gate, and since the large conduction band offset ($\triangle E_C$) at the AlN/GaN interface guarantees the existence of a 2DEG channel elsewhere between the source and drain contacts. Indeed, using the analytical HEMT model described in Ref. [11], normally-off operation for AlN/GaN HEMTs is predicted for AlN thicknesses $\leq 35\,\mathring{A}$. Another reason for investigating this heterostructure is the fact that compared to high Al-content ($> 30\,\%$) barriers, it is easier to grow AlN layers [12], [13]. The schematic cross-section of AlN/GaN HEMT was shown in Fig. 1.3.

1.2.3 HEMT Operation Theory

The current flowing between the drain and source contacts can be written as follows (rate at which the 2DEG charge moves across the gate):

$$I_D = q n_s v_{eff} W_G \tag{1.3}$$

where v_{eff} is the effective velocity of the electrons in the channel, n_s is the 2DEG charge density and W_G is the gate width. The sheet carrier density can vary from

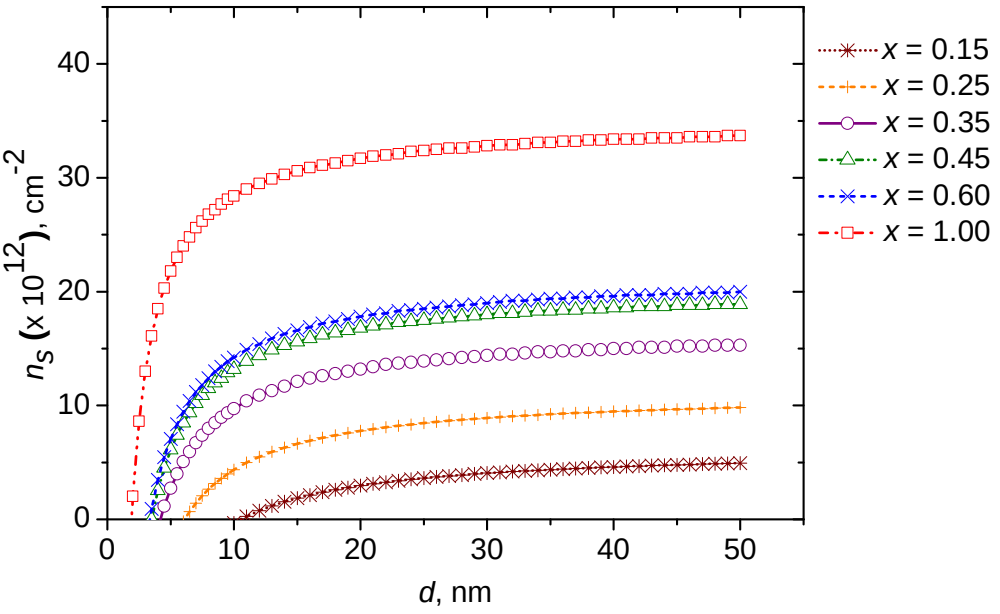


FIGURE 1.6: Simulated sheet charge density, n_s, as a function of barrier thickness, d, for various Al mole fractions, x, in AlGaN barrier layers.

a maximum value of n_{s0} to a minimum value of zero depending on the gate bias. Assuming that for $0 \leq n_s \leq n_{s0}$, the n_s is given by (modelling the gate metal and 2DEG channel as a capacitor)

$$n_s = \frac{\epsilon_{AlGaN}}{q(d_{AlGaN} + \triangle d)}(V_G - V_T) \tag{1.4}$$

where d_{AlGaN} is the thickness of the AlGaN Schottky barrier layer, $\triangle d$ is the effective distance of the 2DEG from the heterointerface, and V_G is the gate bias. So, when the gate bias is equal to V_T, n_s equal to zero, and no current can flow between the drain and source.

When HEMTs are biased at low drain voltages so that $V_D < V_G$ - V_T, the devices are said to be operating in a linear regime, where the electron velocity is linearly related to the electric field strength. However, at high drain biases ($V_D > V_G$ - V_T), the effective electron velocity saturates and becomes independent of bias or the electric field strength. Velocity saturation (v_{sat}) occurs due to scattering of electrons with the semiconductor lattice. For practical purposes, devices are

typically operated at high drain biases, i.e. in the saturated regime. The drain current in the saturated regime is given by

$$I_D = \frac{\epsilon_{AlGaN} v_{sat} W}{(d_{AlGaN} + \triangle d)} (V_G - V_T) \tag{1.5}$$

Notice that I_D is independent of V_D due to the assumption that electrons are moving at their saturated velocities. In reality, I_D is not totally independent of V_D. At high values of V_D, high electric fields exist between the drain and gate contacts and may cause electrons to be injected into the GaN buffer or captured by electron traps. A parallel conduction path may exist between the drain and source contacts. The high drain-to-gate field may also result in an increase in parasitic gate leakage current into the channel. The I_D - V_D curves may also exhibit negative differential resistance at high drain bias voltages, which is characteristic of self-heating effects. These effects cause I_D to be slightly dependent on V_D.

The physical basis of HEMT equivalent circuit is shown in Fig. 1.7 and its corresponding small-signal model is shown in Fig. 1.8. The intrinsic elements are R_{in}, C_{gs}, C_{gd}, R_{ds}, g_m, τ, and C_{ds} while the extrinsic elements are R_d, R_s, and Rg. The descriptions for each circuit elements is given in Table 1.2. In addition, parasitic inductances L_d, L_s, and L_g could be added in series with R_d, R_s, and R_g in the equivalent circuit to account for the effects of device pads. In a HEMT, the conductive channel is controlled by the Schottky barrier gate potential and intrinsic gain is provided by the device transconductance, g_m. The g_m is a figure of merit value that measures the effectiveness of the gate in modulating the drain current and is defined by Eqn. 1.6

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \tag{1.6}$$

The transconductance in the saturated regime is given by Eqn. 1.7

$$g_m = \frac{\epsilon_{AlGaN} v_{sat} W}{(d_{AlGaN} + \triangle d)} \tag{1.7}$$

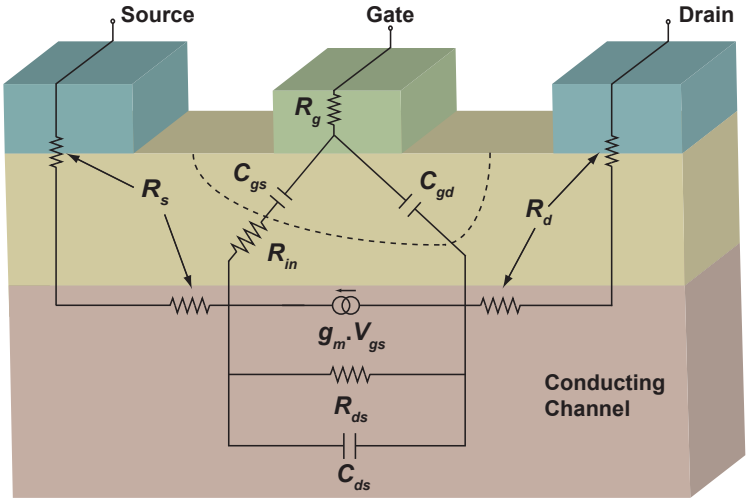


FIGURE 1.7: Physical basis of HEMT small-signal equivalent circuit model.

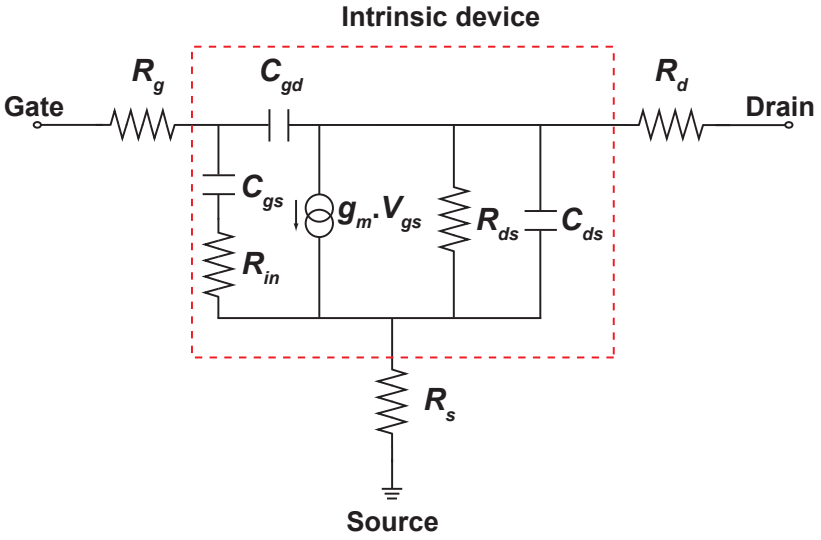


FIGURE 1.8: Equivalent circuit of HEMT.

It is interesting to note that g_m is independent of the gate length (L_G) and V_G. However, in actuality, g_m as well as I_D is dependent on L_G. Velocity overshoot and ballistic effects become important at small L_G and as a result increase v_{sat}. Therefore, higher g_m and I_D are obtained for short gate length devices. The actual transconductance is also dependent on V_G. At gate voltages near V_T, the electrons in the 2DEG are pushed away from the heterointerface and thus increase the value of $\triangle d$. As V_G is increased away from V_T, $\triangle d$ decreases and causes g_m to increase.

At large V_G, n_s in the channel saturates, and g_m peaks at this point. A further

TABLE 1.2: HEMT small-signal equivalent circuit elements

Circuit Element	Description
R_{in}	input (channel) resistance
C_{gs}	gate-source capacitance
C_{gd}	gate-drain feedback capacitance
R_{ds}	drain-source resistance
g_m	transconductance
τ	phase delay due to carrier transit in channel
C_{ds}	drain-source capacitance
R_d	drain-channel resistance, including contact resistance
R_s	sourc-channel resistance, including contact resistance
R_g	gate metal resistance

increase in V_G beyond this point results in carriers residing in the AlGaN layer instead of in the GaN channel. Carriers in the barrier layer suffer a reduced mobility and, as a consequence, reduced velocity. The overall effective velocity of the carriers degrades and causes g_m to decrease with high V_G.

The g_m as given by Eqn. 1.7 is called intrinsic transconductance ($g_{m,int}$), since the expression does not take into account parasitics such as series source resistance (R_s). The measured transconductance is called extrinsic transconductance ($G_{m,ext}$), since it includes parasitic effects. The $G_{m,ext}$ is related to $g_{m,int}$ as follows [14]:

$$G_{m,ext} = \frac{g_{m,int}}{1 + g_{m,int} R_s} \tag{1.8}$$

In general, the series source and drain resistances limit the current drive capabilities of FETs. These parasitic resistances lead to lower values of the drain current and higher values of the knee voltage at which the transistor current saturates.

Another important parameter in determining the performance of the devices is the transit time (τ_t) of the electrons. This transit time is related to the unity-current gain cut-off frequency (f_T)

$$f_T = \frac{1}{2\pi\tau_t} = \frac{v_{eff}}{2\pi L_G} \tag{1.9}$$

the f_T can be derived using a simple small-signal model (Fig. 1.8 without access resistances) as

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{1.10}$$

where C_{gs} is the capacitance between gate and source and C_{gd} is the capacitance between gate and drain.

Eqns. 1.9 and 1.10 do not include parasitic source and drain resistances (i.e. R_s and R_d) from small-signal model. A more rigorous derivation for the f_T of a FET gave a better approximate expression for the extrinsic f_T [15]:

$$f_T = \frac{g_m/2\pi}{[C_{gs} + C_{gd}].[1 + (R_s + R_d)/R_{ds}] + C_{gd}g_m(R_s + R_d)} \tag{1.11}$$

where R_{ds} is the output resistance. The maximum oscillation frequency (f_{MAX}) is the maximum frequency that power can be extracted from the device. It is related to the Mason′s unilateral power gain (U) [16]

$$U = \left(\frac{f_{MAX}}{f}\right)^2 \tag{1.12}$$

and the f_{MAX} can also be derived using a simple small-signal model as [17]

$$f_{MAX} = \frac{f_T}{2\sqrt{\frac{R_{in}+R_s+R_g}{R_{ds}} + 2\pi f_T R_g C_{gd}}} \tag{1.13}$$

where R_{in} is the input resistance and R_g is the metal gate resistance. To maximise f_{MAX}, the f_T and the resistance ratio $\frac{R_{in}+R_s+R_g}{R_{ds}}$ must be optimised in the intrinsic HEMT. The extrinsic resistances R_g and R_s and the feedback capacitance (C_{gd}) have aslo to be minimised.

1.2.4 GaN-Based MOS-HEMT

As already mentioned in section 1.3, GaN-based HEMTs are expected to be widely used for high frequency power applications due to their outstanding properties, for instance, high 2DEG charge density. However, one critical issue that limits the performance and reliability of GaN-based HEMTs is their relatively high gate leakage current. The gate leakage current reduces the breakdown voltage, the power added efficiency and the output-power stability for GaN-based HEMTs. To overcome these problems, MIS- and/or MOS-HEMTs have been employed for fabrication of AlGaN/GaN-based devices.

The MOS-HEMT design incorporates a thin dielectric layer such as Si_3N_4 [18], Al_2O_3 [19] and gate metal stacks (HfO_2/Al_2O_3) [20] under the gate (Fig. 1.9). The theory and concepts behind the MOS-HEMTs operation are nearly identical to the HEMTs. In the case of MOS-HEMTs, the current which is entering the gate (I_{GS}) would be smaller than the Schottky gate due to the existing of the oxide/dielectric layer. This significantly reduces the gate leakage current of GaN-based devices thereby improving their performance and reliability. The gate oxides/dielectrics also acts as a surface passivation which reduces current collapse in the devices [20],[21].

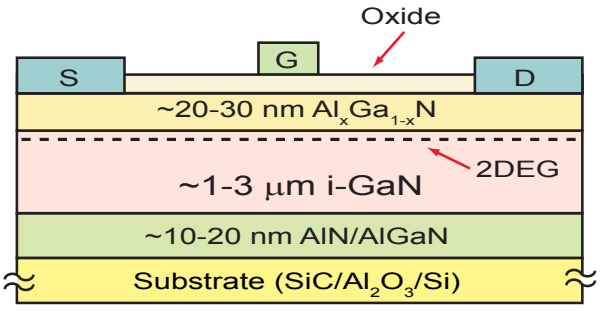


FIGURE 1.9: Basic structure of AlGaN/GaN MOS-HEMT.

1.2.5 Basic MOS Structure

The metal-oxide-semiconductor (MOS) diodes (also known as a MOS capacitors) are the heart of silicon MOSFET transistors. Its operation is briefly summarised

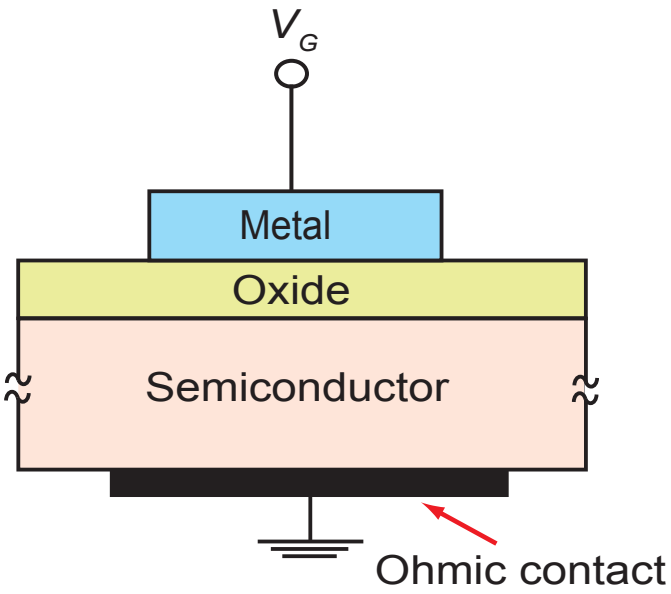


FIGURE 1.10: Schematic cross-section of an MOS diode.

here because of its similarity with the gate capacitance of the GaN MOS-HEMT that is described in this thesis. The MOS capacitor is just an oxide layer located between a semiconductor and a metal gate. The semiconductor and the metal gate are two plates of the capacitor. The oxide layer acts as a dielectric. Silicon dioxide, SiO_2, is commonly used as a gate dielectric/oxide for conventional Si MOS diode. The area of the metal gate defines the area of the capacitor.

The most important characteristic of the MOS capacitor is that its capacitance (C) changes with an applied DC voltage. The capacitance can be determined from the following equation (of a parallel plate capacitor)

$$C = \frac{\varepsilon_0 \varepsilon_r A}{t} \tag{1.14}$$

where ε_0 is the permittivity of free space, ε_r is the relative permittivity of the material, A is the area of the metal contact, and t is the thickness of the dielectric material. Fig. 1.10 shows the schematic cross-section of an MOS structure. The procedure for C-V measurements involves the application of DC bias voltages across the capacitor while making the measurements with an alternating current (AC) signal. Commonly, AC frequencies from about 10 kHz to 10 MHz are used

for these measurements. The bias is applied as a DC voltage sweep that drives the MOSCAP structure from its accumulation region into the depletion, and then into inversion. A typical high-frequency C-V curve for MOSCAP structure formed on n-type Si substrate is shown in Fig. 1.11 [2]. Details of these three modes of operation are described below:

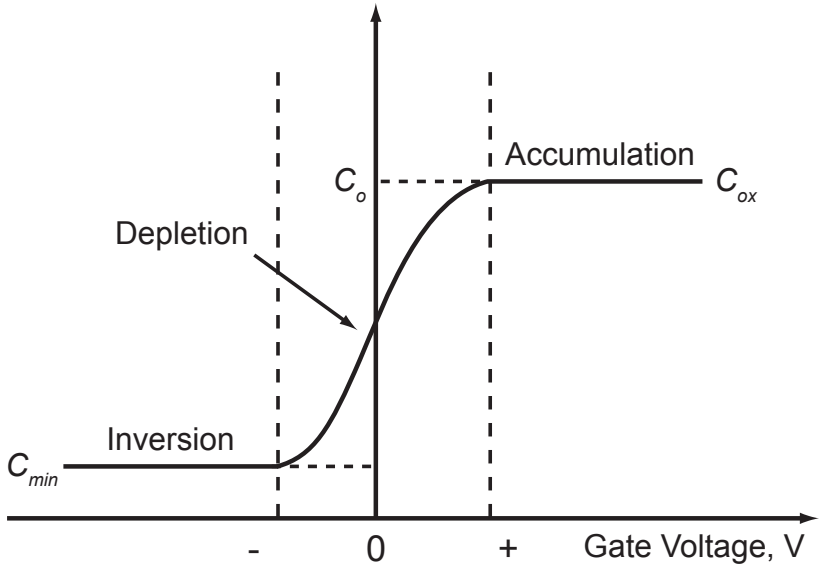


FIGURE 1.11: High-frequency C-V curve of an ideal MOSCAP (n-type Si substrate) at room temperature [2].

Accumulation: When a positive voltage ($V_G > 0$) is applied to the gate metal, the majority carriers (electrons) will be attracted to the oxide-semiconductor interface. The energy bands at the semiconductor surface are bent downward and the conduction band edge becomes closer to Fermi level, which in turn gives rise to an enhanced electrons concentration near the oxide-semiconductor interface. This is called the accumulation and it is illustrated in Fig. 1.12(a). The oxide capacitance (C_{ox}) is measured in the strong accumulation region. This is where the voltage is positive enough that the capacitance is essentially constant and the C-V curve is almost flat. The oxide capacitance (t_{ox}) can also be extracted from the oxide capacitance (Fig. 1.11).

Depletion: When a small negative voltage ($V_G < 0$) is applied, the energy bands are bent upward, and the majority carriers (electrons) are depleted. This is called

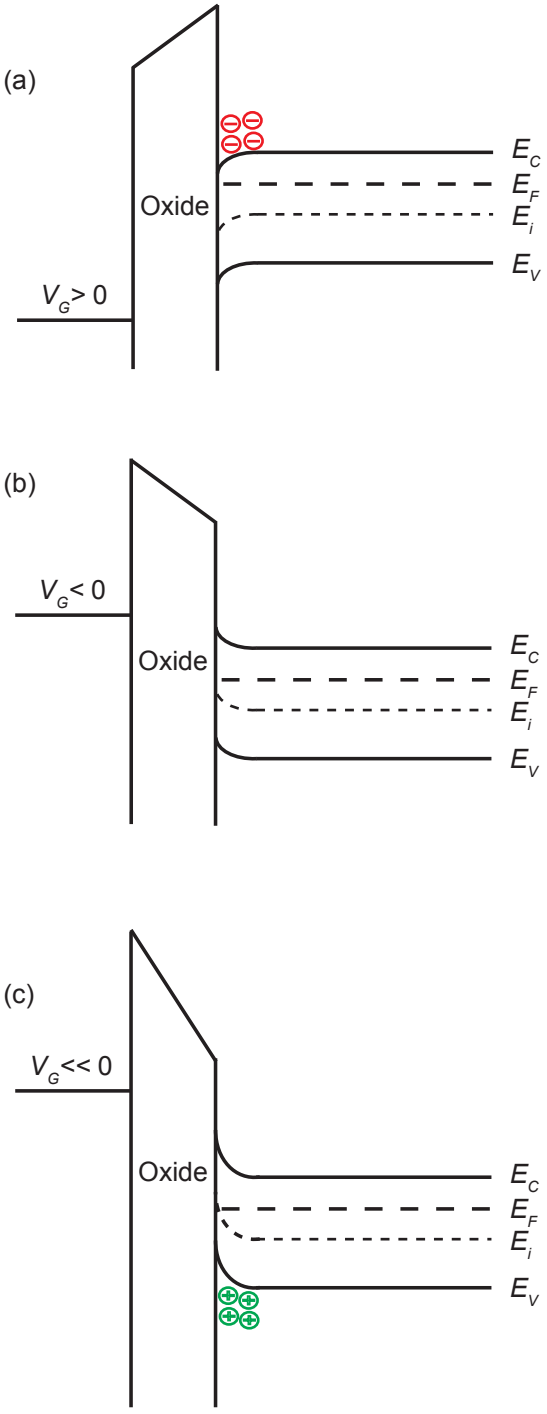


FIGURE 1.12: The energy band diagrams of MOSCAP (n-type semiconductor) at different biases:(a) accumulation, (b) depletion and (c) inversion. *Note*: E_C is the conduction band, E_F is the Fermi level, E_i is the intrinsic level and E_V is the valence band [2]

depletion and it is illustrated in Fig. 1.12(b). The depleted area acts as a dielectric/insulator because it can no longer contain or conduct charge. The total

measured capacitance now becomes C_{ox} and the depletion layer capacitance (C_s) in series, and as a result the measured capacitance decreases. This decrease in capacitance is illustrated in Fig. 1.11 in the depletion region. As a more negative voltage is applied, the depletion region moves away from the gate, increasing the effective thickness of the dielectric between the gate and the substrate, thereby reducing capacitance.

Inversion: When a larger negative voltage ($V_G << 0$) is applied, the energy bands are bent upward even more so that the intrinsic level at the surface crosses over the Fermi level. The number of minority carriers (holes) at the oxide-semiconductor interface can become larger than the number of majority carriers (electrons). This is called the inversion and it is illustrated in Fig. 1.12(c). Initially, the surface is in a weak inversion condition since the hole concentration is small. As the bands are bent further, eventually the valence band edge comes close to the Fermi level. The onset of strong inversion occurs when the hole concentration near the oxide-semiconductor interface is equal to the substrate doping level i.e. n-type Si substrate [2].

The important thing to notice is that the behaviour of the device in inversion under high frequency and low frequency conditions is different. In the case of n-type substrate, the holes (the minority carriers) in the inversion layer must be generated somehow, as there are not sufficient free holes in a n-type Si substrate to form an inversion layer without some excitation. For a MOSCAP (as shown in Fig. 1.11) the holes are generated slowly by thermal excitation. For a high frequency signal, though, there is not sufficient time for this generation to occur so the measured capacitance is equal to C_{min}.

If, however, the measurement frequency is low enough so that generation-recombination rates in the surface depletion region are equal to or faster than the voltage variation, then the hole concentration can follow the AC signal and lead to charge exchange with inversion layer in step with the measurement signal. As a result the capacitance in strong inversion will be that of the oxide layer alone, C_o. Commonly, the onset of the low-frequency curves occurs at $f \leq 100\,\text{Hz}$ [2].

At a certain negative gate voltage, most available minority carriers are in the inversion layer, and further negative gate-voltage bias do not further deplete the semiconductor. That is, the depletion region reaches a maximum depth. Once the depletion region reaches a maximum depth, the minimum capacitance that is measured using high frequency signal is the oxide capacitance in series with the depletion capacitance. This capacitance is referred to as minimum capacitance (C_{min}) and is illustrated in Fig. 1.11 in the inversion region. The C-V curve slope is almost flat.

In the case of GaN-based MOS capacitors (i.e. wide bandgap semiconductor), the situation is different. When the n-type GaN MOSCAP is biased from accumulation to depletion, the inversion layer cannot form due to a very low generation rate of minority carriers. Thus, the GaN MOSCAP's depletion region has to compensate and continue becomes wider. The capacitance continues to drop below the value of C_{min}, as illustrated in Fig. 1.13. This region is called as deep depletion [22]. The deep depletion feature with no inversion capacitance characteristics is typical for wide bandgap semiconductor MOS structures. In addition, deep depletion behaviour was also observed even at the low frequency (10 kHz) [23].

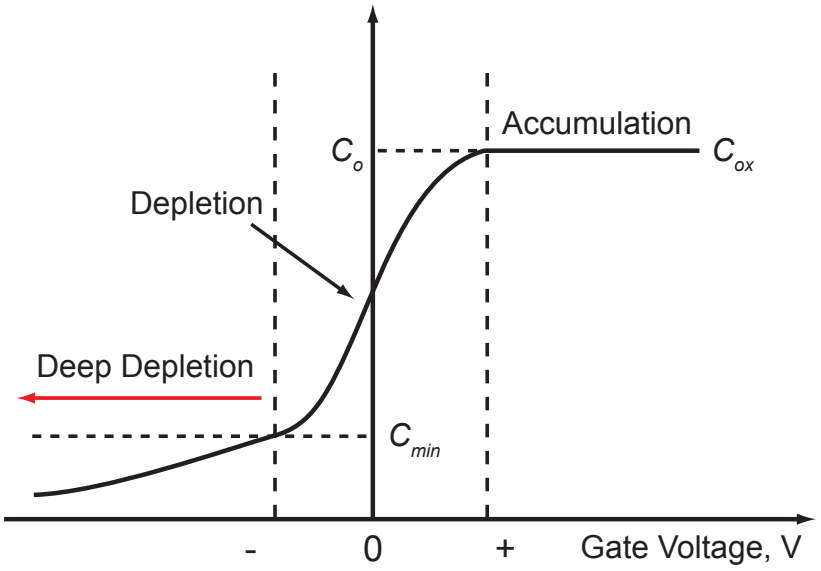


FIGURE 1.13: Typical high-frequency C-V curve for GaN MOSCAP formed on n-type GaN substrate at room temperature.

1.3 Conventional AlGaN/GaN-Based HEMT Technology

AlGaN/GaN HEMTs offer operational advantages under a number of circumstances because a two-dimensional electron gas (2DEG) is formed at the heterojunction of two semiconductor materials with different bandgap energies. It has the ability to achieve a 2DEG with sheet carrier concentrations (n_s) of $\sim 1 \times 10^{13}\,\mathrm{cm}^{-2}$ or higher close to the interface without intentional doping, well in excess of those achievable in other III-V material systems. Furthermore, electrons that originate in the wider bandgap material (i.e. AlGaN) transfer to the smaller bandgap material (i.e. GaN) to form 2DEG, allowing a high electron mobility (μ) over $1000\,\mathrm{cm}^2/\mathrm{V.s}$ at room temperature (RT) due to reduced scattering effect. In order to produce a high gain microwave- and/or millimetre-wave power amplifier featuring high reliability, it is important to simultaneously realise transistors with high current-gain cutoff frequency (f_T), maximum oscillation frequency (f_{MAX}), and high breakdown voltages. Having high electron velocities which is achieved under high electric fields and high breakdown voltage properties, GaN-based HEMTs have the potential to meet this requirement.

Excellent GaN-based HEMTs performance in terms of current and cutoff frequency have been reported since the first demonstration of AlGaN/GaN devices in 1993 [24]. State of the art direct-current (DC), radio-frequency (RF) and power performances of AlGaN/GaN-based devices are summarised in Tables 1.3 and 1.4, given at the end of this chapter. As can be seen, the optimal values of maximum drain currents (I_{DSmax}), maximum extrinsic transconductance (G_{max}), f_T, f_{MAX} and maximum power density (P_{Dmax}) reported in the literature are varied because of the various factors affecting the device performances. These include the quality of the epitaxial layers (e.g. 2DEG and μ), process maturity in growing materials using metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE), Ohmic contact resistances (R_C), sheet resistance (R_{sh}), device dimensions (e.g. gate length and gate width), advanced processing (e.g. Ohmic and

gate recessing), advanced device design (e.g. sub-T-gate and field plate), type of substrates used i.e. silicon carbide (SiC), sapphire (Al_2O_3) or silicon (Si) and surface passivation. Major breakthroughs which have been achieved for this material system are summarised below:

1. Improvement of the AlGaN/GaN HEMTs grown on sapphire substrates by MOCVD, produces high $n_s \times \mu$ (2.4×10^{16}/V.s) product which leads to reduction in a sheet resistance (R_{sh}) in the range of $\sim 250\,\Omega/\square$. Record current densities up to 2.1 A/mm under 200 ns pulse condition has been achieved [25].

2. Reduction in R_C. Very low of R_C (0.15 Ω.mm) was achieved by Ohmic recess technique. The AlGaN barrier was slowly etched using a low-power electron cyclotron resonance reactive ion etching (ECR-RIE) with Cl_2/BCl_3 gas mixture [26].

3. The use of thin AlGaN barrier layer (6 nm), high Al mole fraction (40 %), surface passivation using silicon nitride (SiN) catalytic chemical vapor deposition (Cat-CVD), heterostructures grown on 4H-SiC substrates, leads to very high $n_s \times \mu$ (3.4×10^{16}/V.s) product, and lower R_{sh} (220 $\Omega/\square$). Fabricated devices demonstrated a high I_{DSmax} of 1.6 A/mm, a record G_{max} of 424 mS/mm, high f_T of 190 GHz and f_{MAX} of 251 GHz [18].

4. The insertion of very thin AlN (0.5 - 2 nm) between AlGaN and GaN layers, leads to improvement in 2DEG mobilities to over 2000 cm^2/V.s [18],[8]. The AlN interlayer increases the effective conduction band offset and reduces the alloy disorder scattering from the AlGaN barrier layer, which improves the 2DEG mobility in the channel, thus enhancing the high frequency characteristics of the device.

5. Incorporating sub-0.1 μm T-gate technology and optimised reduced parasitic resistances, AlGaN/GaN HEMTs with a record f_T of 194 GHz with a gate length of 0.045 μm [27] and a f_{MAX} of 300 GHz with a gate length of 0.06 μm [26] have been demonstrated.

6. The use of high thermal conductivity of SiC substrate makes heat in AlGaN/GaN HEMT sink through the substrate promptly, allows realisation of very high power density in the devices [8].

7. With increasing process maturity, the highest ever achieved for f_T and f_{MAX} of 107 GHz and 150 GHz respectively of AlGaN/GaN HEMTs grown on silicon is comparable to those grown on SiC [28]. The first power performance of AlGaN/GaN HEMTs on silicon substrate with an output power density of 7 W/mm at 10 GHz has been achieved [7].

8. Optimised surface passivation using Si_3N_4 plasma enhanced chemical vapor deposition (PECVD) reduces the DC and RF dispersion by suppressing/removing the surface defects and traps [5],[29].

9. The metal-insulator-semiconductor HEMT (MIS-HEMT) and/or metal-oxide-semiconductor (MOS-HEMT) design combines the advantages of the MOS structure, which suppresses the gate leakage current, and provides high 2DEG density [18],[30].

10. Sub-0.1 μm recess gate technology in order to maintain excellent gate control of the channel in short-gate-length devices and to reduce gate access resistances (i.e. thinning the AlGaN barrier layer under the gate foot). A gate recess was performed using very low-voltage and low-damage Cl_2-based inductively coupled plasma RIE (ICP-RIE) process for 70 nm gate length devices. The unpassivated devices exhibited a high I_{DSmax} of 1.5 A/mm, G_{max} of 374 mS/mm, an f_T of 160 GHz and f_{MAX} of 200 GHz [31].

11. The use of field plate technologies has dramatically improved the power performances of AlGaN/GaN-based devices. With the double field-plated devices, a record microwave power performances of 41.4 W/mm at 4 GHz with power added efficiency (PAE) as high as 60% was achieved in Ref. [32]. The first field plate integrated with the gate for both reduced gate resistance and minimisation of electron trapping, while the second field plate which electrically connected to the source is to minimise feedback capacitance.

Power performances in millimeter-wave applications, from Ka-band up to W-band also have been reported and show very promising results [33],[34],[35]. There are still opportunities to extend the power capabilities of this technology. As can be seen clearly in Tables 1.3 and 1.4, there is a trade off between DC, RF and power performances of AlGaN/GaN HEMTs. Higher drain current densities, transconductances, current-gain cutoff frequency and maximum oscillation frequency were observed for scaled devices, while higher power densities were observed for larger gate periphery devices.

1.4 Emerging AlN/GaN-Based HEMT Technology

AlGaN/GaN HEMT technology has matured significantly over the past few years, and offers significant advantages in power density and total power over other competing material technologies such as Si, GaAs, and InP-based transistors. With the impressive achievements on the device level, high-power amplifier monolithic microwave integrated circuits (MMICs) up to Ka-band have also been realised [58],[59]. Today, the demand for higher power devices at higher frequencies is very strong. Therefore the performance of GaN-based HEMTs is being pushed to achieve maximum power and speed levels possible.

The 2DEG in the unintentionally doped AlGaN/GaN structure is formed largely as a result of piezoelectric and spontaneous polarisation effects which arise in the AlGaN layer. For this heterostructure, the typical 2DEG value of $\sim 1 \times 10^{13}$ with Al mole fraction is ~ 20 - $30\,\%$ as can also be seen in Table 1.3.

In order to further increase the 2DEG density as well as the breakdown field in the AlGaN/GaN structure, high Al mole fraction is desirable to increase the strength of polarization. However, from a growth perspective, it is difficult to grow high-quality $Al_xGa_{1-x}N$ layers with high Al content which results in poor

transport properties of $Al_xGa_{1-x}N$/GaN structures with x > 0.5 [12]. To overcome this problem, the ultra-thin all binary AlN/GaN material system, which can be grown reliably, has become an alternative candidate for future high-frequency power applications [60].

Due to the large difference in spontaneous and piezoelectric polarizations between the GaN and AlN layers, the 2DEG which forms near the AlN/GaN interface can reach over $3 \times 10^{13}\,\mathrm{cm}^{-2}$ for an extremely thin AlN barrier layer thickness ($d < 5\,\mathrm{nm}$) along with high mobility ($> 1000\,\mathrm{cm}^2/\mathrm{V.s}$) and very low sheet resistance ($R_{sh} < 150\,\Omega/\square$) [60],[61]. In addition, AlN with its relatively high dielectric constant (8.5) and wide band gap (6.2 eV), provides better carrier confinement and has the potential to be an excellent choice for the gate dielectric. Compared to the AlGaN/GaN structure, the AlN/GaN structure offers a big reduction in alloy disorder scattering and roughness scattering (by removing Ga from the barrier) [62].

From a circuit design point of view, the use of very thin AlN barrier layer ($\sim$3-5 nm) increases the intrinsic transconductance and decreases the short channel effects by placing the gate much closer to the 2DEG channel [63]. Having these superior properties makes this material system have potentially the highest performance HEMTs in the III-V nitrides. Table 1.5 at the end of this chapter summarises DC and RF AlN/GaN-based HEMTs performances which have been reported to date. In the early years, it was difficult to grow high quality material AlN/GaN heterostructures due to large lattice mismatch between AlN and GaN ($\approx 2.4\,\%$) [64]. With the advanced improvement in AlN/GaN material growth, outstanding record performances have been demonstrated for its epitaxial layers and devices such as (details are given in Table 1.5):

1. Record very high f_T of 220 GHz, f_{MAX} of 400 GHz and high G_{max} of 723-mS/mm (these values were the highest reported in the III-nitride HEMTs), resulting from vertical scaling in AlN/GaN/AlGaN double heterojunction

HEMT structure, reduction of access resistance using MBE re-growth of n^+-GaN Ohmic contacts, incorporating sub-40-nm T-gate technology and fully passivated devices [65].

2. Record very high current densities up to 2.9 A/mm (the highest reported in the III-nitride HEMTs) and high G_{max} of 430 mS/mm, resulting from high $n_s \times \mu$ ($\sim 3.7 \times 10^{16}$/V.s) product with low R_{sh} (165 $\Omega/\square$). The HEMT structures have 3.5 nm thin AlN barrier layer and utilised 3 nm Al_2O_3 gate dielectric. Device dimensions were very small, gate length of 0.15 μm and gate width of 10 μm [66].

3. Record high transconductance up to 480 mS/mm and high I_{Dmax} of 2.3 A/mm, resulting from high $n_s \times \mu$ ($\sim 3.76 \times 10^{16}$/V.s) product with low R_{sh} (165 $\Omega/\square$). The HEMT structures have 3.5 nm thin AlN barrier layer and also utilised 3 nm Al_2O_3 gate dielectric. Device dimensions were very small, gate length of 0.25 μm and gate width of 12 μm [67].

4. Impressive f_T of 107 GHz and f_{MAX} of 171 GHz utilising AlN/GaN metal-insulator-semiconductor high field effect transistors (MIS-HFETs) with very thin 2.5 nm AlN barrier layer and 3 nm SiN passivation by Cat-CVD. Cat-CVD SiN increased the electron density of AlN/GaN HFETs by compensating the surface depletion of the 2DEG [68].

5. Low defect AlN/GaN HEMTs with very high values of n_s ($> 3 \times 10^{13}$ cm^{-2}) and μ (> 1800 cm^2/V.s), resulting a record R_{sh} as low as $\sim 100\,\Omega/\square$. Devices demonstrated high I_{Dmax} of ~ 1.3 A/mm and G_{max} of ~ 260 mS/mm with large device dimensions, gate length of 1.2 μm and gate width of 200 μm [60]

6. An optimised AlN/GaN HEMT structure with 4.5 nm thin AlN barrier layer exhibited very high $n_s \times \mu$ ($\sim 4.32 \times 10^{16}$/V.s) product with very low R_{sh} (144 $\Omega/\square$). Devices with large gate length (1 μm) exhibited record very high drain current densities up to 1.8 A/mm and transconductance of 400 mS/mm [69].

These results clearly demonstrate the potential of ultra-thin AlN/GaN-based devices for high power frequency applications. However further reduction in Ohmic contacts resistances is required to fully exploit advantages offered by the ultra-thin AlN barrier. As can be seen in Table 1.5, Ohmic contact resistances R_C values are still very high ($\sim 1\,\Omega$.mm) as compared to conventional AlGaN/GaN HEMTs technology.

The ultra-thin barrier layers under gate have been of increasing interest also for developing enhancement-mode (E-mode) or normally off devices which exhibit a positive threshold voltage. To date, most of the development in conventional AlGaN/GaN HEMTs technology has been focused on depletion-mode (D-mode) devices that feature negative gate threshold voltage. Power switching devices with normally off characteristics are required since they prevent device destruction due to short circuit should the gate signal become ground and so they offer increased safety [70]. Also, normally off devices require only a single-polarity voltage supply, which reduces circuit complexity (D-mode devices which require a negative gate bias). For AlGaN/GaN HEMTs, the most commonly used approaches to realise E-mode devices is by thinning/etching the AlGaN layer by low-damage ICP-RIE which can selectively reduce 2DEG density under the gate contact. However this technique has low uniformity and reproducibility due to difficulty in obtaining a precise etching depth and damage free surface [71]. Therefore, the ultra-thin barrier AlN/GaN HEMTs seems to be an ideal way to realise E-mode devices since a thin barrier makes it possible to deplete the channel with a Schottky gate.

At the beginning of this project, the initial effort was to develop E-mode AlN/GaN-based devices. However, the AlN/GaN devices suffered from surface sensitivity and high leakage currents if the epilayers were not protected during processing. It was therefore necessary to protect the AlN/GaN epitaxial layers during device processing. These problems/issues will be discussed further in the following section.

1.5 Research Problem

The aim of this project was to develop a robust AlN/GaN transistor technology. Despite the excellent progress of AlN/GaN devices to date, there are still significant problems/challenges to be overcome before the potential of this material system can be fully realised. These problems are surface sensitivity, high leakage current and high contact resistance, which currently limit the device performance. Details of the specific problems/challenges are described below:

1. **Surface sensitivity and high leakage current:** Devices suffer from surface sensitivity and high leakage currents if the epilayers are not protected during processing [79],[82]. Having a very thin AlN barrier layer, 3 - 4 nm thick, makes the structure very sensitive to liquids coming in contact with the surface. Exposure to developer solutions or solvents such as acetone and isopropanol during device processing degrades the surface properties, resulting in poor device performance. In addition to this, the thin barrier is prone to gate leakage through tunneling and surface defects. Also, unlike other nitrides, AlN is easily attacked/etched by common alkaline processing solutions, e.g AZ400K photoresist developer [76]. To overcome these problems, a protection layer such as Al_2O_3 or Si_3N_4 is needed to protect the AlN surface during device processing and also to minimise the gate leakage current. This protection layer also can be used as a gate dielectric and surface passivation for the devices.

2. **High contact resistance:** The formation of low Ohmic contacts resistance on wide bandgap AlN barrier layer, 6.2 eV, is difficult as compared to AlGaN or GaN, 3.4 eV, layer. This problem is even more challenging with the existence of the protection/passivation layers on the AlN surface. To be able to form Ohmic contacts, these protection/passivation layers need to be removed from areas where the contacts are to be formed. Since the 2DEG is very near to the surface, a low damage process is preferred to etch/remove these protection/passivation layers [78],[83].

1.6 Research Goal and Objectives

In this project, the main focus of the research is to develop a reliable processing technology for AlN/GaN-based devices for future high frequency power applications. As previously mentioned, AlN/GaN material system has superior properties as compared to conventional AlGaN/GaN material system. However, problems such as surface sensitivity, high leakage currents and high Ohmic contacts currently limits the expected device performance. Hence, the objectives of the research are described below;

1. To optimise the Ohmic contacts and device processing for AlGaN/GaN HEMTs since its technology is a well established as compared to the AlN/GaN HEMTs. The techniques employed for AlGaN/GaN devices serve as a foundation for the work on AlN/GaN devices.

2. To find a suitable protection or passivation layer for fabrication of AlN/GaN devices. A protection layer such as Al_2O_3 or Si_3N_4 is needed to protect the AlN/GaN epilayer surface during device processing and to minimise the gate leakage current. This protection layer also can be used as a gate dielectric and surface passivation for the devices.

3. With the existing of protection/passivation layer on the AlN/GaN epilayers, develop an alternative Ohmic contact processing recipe to obtain low resistance Ohmic contacts.

4. To extract the small-signal equivalent circuit model values for both AlN/GaN MOS-HEMTs and AlGaN/GaN MOS-HEMTs. The extracted element values provide feedback for further device process optimisation.

1.7 Thesis Structure

This thesis is divided into seven (6) chapters. **Chapter** 1 (this chapter) describes basic transistor structure, piezoelectric and spontaneous polarization effects, 2DEG formation, and the operation of GaN-based HEMT devices. The chapter also gave an overview on the state of the art GaN-based HEMT technology in particular for AlGaN/GaN-based HEMT technology and the new AlN/GaN-based HEMT technology. The recent development of AlN/GaN-based devices was also presented and reviewed, along with issues and problems which currently limit the expected device performance. The aim and objectives of the research project were also presented and discussed briefly.

Chapter 2 describes the material structures and the processing techniques used for fabrication of AlGaN/GaN HEMTs and AlN/GaN HEMTs grown on sapphire substrates. The processing techniques include sample preparation, lithography, mask plate production, metallisation, mesa isolation and annealing.

Chapter 3 gives an overview of Ohmic metal to semiconductor formation for GaN-based heterostructures, and state of the art Ohmic contacts on the conventional AlGaN/GaN as well as AlN/GaN HEMT structures. Ohmic contact processing for both heterostructures will be described and discussed.

Chapter 4 focuses on the processing and characterisation of AlN/GaN MOS-HEMT devices which employ thermally grown Al_2O_3 as a gate dielectric, and for surface protection and passivation. The discussion covers a simplified gate wrap-around method which was initially used for process development on the devices, and processing for conventional AlGaN/GaN structures to provide comparative data with the new barrier AlN/GaN structures. Process development for fabrication of RF devices (which employ mesa isolation) will be also presented and discussed.

Chapter 5 discusses the extraction of the small-signal equivalent circuit model values for AlN/GaN MOS-HEMTs as well as AlGaN/GaN MOS-HEMTs to provide feedback for further device process optimisation.

Finally, **Chapter** 6 provides summary of the research project as well as the discussion for the potential future work.

TABLE 1.3: State of the art DC and RF AlGaN/GaN-based HEMTs performances

L_G, W_G, μm	Material Growth/ Substrate	Al mole fraction, %	2DEG, cm^{-2}	μ, $cm^2/V.s$	R_{sh}, $\Omega/\square$	R_C, $\Omega.mm$	I_{DSmax}, mA/mm	G_{max}, mS/mm	f_T, GHz	f_{MAX}, GHz	Ref.
0.7, 2×75	MOCVD/Al_2O_3	34	$\sim1.45\times10^{13}$	1650	250	0.3	2100	-	~24	~45	[25]
0.06, 2×25	MBE/SiC	-	8×10^{12}	2200	356	~0.15	1200	410	70	300	[26]
0.06, 2×50	MOCVD/4H-SiC	40	1.7×10^{13}	2000	220	0.3	1600	424	190	251	[18]
0.35, 1000	MOCVD/6H-SiC	-	1.044×10^{13}	2215	251	0.4	1300	314	28	60	[8]
0.045, 2×50	MOCVD/SiC	26	9.1×10^{12}	1710	-	-	1263	274	194	-	[27]
0.07, 2×75	-/HR Si	26	1×10^{13}	~1500	600	0.55	750	310	107	150	[28]
0.3, 2×50	MBE/Si	25	-	1500	530	-	850	220	24	47	[7]
0.3, 2×125	MOCVD/SiC	30	1.4×10^{13}	1200	450	0.3	1200	360	39	51	[5]
0.07, 100	PAMBE/6H-SiC	23	1×10^{13}	1900	350	0.2	1500	374	160	200	[31]
0.1, 2×75	MOCVD/HR Si	27	8.5×10^{12}	~1500	640	0.46	~600	195	104	125	[36]
0.12, 100	MOCVD/4H-SiC	25	1.1×10^{13}	1300	-	0.35	1230	314	121	162	[37]
0.25, 45	-	20	-	-	-	0.45	1710	222	-	-	[38]
0.05, 200	MBE/SiC	-	1.1×10^{13}	1100	-	-	1200	-	110	>140	[39]
0.25, 100	MOCVD/6H-SiC	30	-	-	380	~0.15	1280	310	51	115	[40]
0.25, 100	MOCVD/4H-SiC	25	1.1×10^{13}	1300	-	~0.35	1300	275	65	110	[41]
0.15, 100	MBE/Al_2O_3	24	1.5×10^{13}	1170	330	0.7	1100	213	79	125	[42]
0.03, 2×50	PAMBE/Al_2O_3	40	2.07×10^{12}	827	364	-	1490	402	181	186	[43]
0.1, 150	MOCVD/SiC	32	1.5×10^{13}	1240	-	-	1400	~380	153	230	[44]
0.14, 2×150	MOCVD/4H-SiC	34	1.14×10^{13}	1883	295	~0.24	1481	338	91	122	[45]
0.125, 2×50	MOCVD/HR Si	26	7.05×10^{12}	2160	410	0.28	655	332	75	125	[46]

TABLE 1.4: State-of-the-art power performance AlGaN/GaN-based HEMTs

L_G, W_G, μm	Material Growth/ Substrate	Power Density (P_{Dmax}), W/mm	Frequency, GHz	PAE %	Ref.
0.3, 4×50	MBE/Si (111)	7	10	52	[7]
0.3, 150	OMVPE/SiC	10.7	10	40	[5]
0.25, 100	MOCVD/6H-SiC	9.1	18	23.7	[29]
1.1, 200	LPMOCVD/4H-SiC	20	2	-	[30]
0.55, 246	Cree HPSI SiC	41.4	4	60	[32]
0.1, 4×37.5	PAMBE/SiC	2.1	80.5	14	[33]
0.16, 2×75	MOCVD/-	10.5	40	34	[34]
0.16, 2×75	MBE/-	8.6	40	32	[34]
0.18, 100	MOCVD/4H-SiC	2.8	40	10	[35]
0.25, 100	MOCVD/SI 6H-SiC	6.7	18	26.6	[40]
0.25, 100	MOCVD/SI (0001)SiC	4	30	20	[41]
0.25, 100	MOCVD/SI (0001)SiC	6.4	20	16	[41]
0.14, 300	MOCVD/4H-SiC	4.6	10	46	[45]
0.35, 2000	MOCVD/6H-SiC	9.05	8	36.4	[47]
0.7, 150	PAMBE/SiC	7.3	10	36	[48]
0.7, 2×75	MOCVD/Al_2O_3	12	4	58	[6]
0.55, 500	MOCVD/SI SiC	20.5	4	60	[49]
0.7, 2×50	MOCVD/HR Si	12	2.14	52.7	[50]
0.35, 150	MOCVD/SiC	16.5	10	47	[51]
0.55, 246	MOCVD/SI SiC	30.6	8	49.6	[52]
0.55, 246	MOCVD/SI SiC	32.2	4	54.8	[52]
0.18, 2×75	-	5.7	30	45	[53]
1.1, 200	LPMOCVD/SI SiC	20	2	74	[54]
0.8, 1000	MOCVD/6H-SiC	4.1	5.4	36.4	[55]
0.4, 1000	MOCVD/HR Si	5.1	2	35	[56]
0.25, 300	MOCVD/4H-SiC	4.13	35	23	[57]

TABLE 1.5: DC and RF AlN/GaN-based HEMTs performances

L_G, W_G, μm	Material Growth/ Substrate	2DEG, cm^{-2}	μ, $cm^2/V.s$	R_{sh}, $\Omega/\square$	R_C, $\Omega.mm$	I_{DSmax}, mA/mm	G_{max}, mS/mm	f_T, GHz	f_{MAX}, GHz	Ref.
1.2, 200	PAMBE/Al_2O_3	$>3\times10^{13}$	>1800	~100	-	~1300	~260	-	-	[60]
0.04, 80	MBE/SiC	1.3×10^{13}	1200	440	-	1610	723	220	400	[65]
0.15, 10	MBE/Al_2O_3	$\sim2.7\times10^{13}$	~1370	~165	~1.1	2900	430	52	60	[66]
0.25, 12.5	PAMBE/Al_2O_3	2.75×10^{13}	1367	~165	~1.1	2300	480	-	-	[67]
0.25, 60	PAMBE/Al_2O_3	$\sim2.75\times10^{13}$	~1367	~165	~1.1	-	-	52	60	
0.06, 50	PAMBE/Al_2O_3	2.33×10^{13}	365	1144	-	~920 - 950	185	107	171	[68]
1, 50	RF-MBE/Al_2O_3	3.6×10^{13}	~1200	144	0.93	1800	400	-	-	[69]
1.4, 40	MOCVD/Al_2O_3	1.5×10^{13}	340	176	-	475	220	-	-	[72]
3, 40	PAMBE/Al_2O_3	8.25×10^{13}	150	-	0.72	600	130	-	-	[73]
0.25, 48	PAMBE/Al_2O_3	3.5×10^{13}	1185	~150	~1.5	2100	360	60	50	[74]
2, 24	PAMBE/Al_2O_3	3.5×10^{13}	1185	~150	~1.5	1700	270	3.5	-	
0.5, 15						-	300	-	-	
0.25, 30	PAMBE/Al_2O_3	$\sim1.4\times10^{13}$	1600	~350	~1.5	1600	-	-	-	[75]
0.15, 30						-	-	24	52	
1, 200	MOCVD/Al_2O_3	0.98×10^{13}	900	569	1.75	380	85	5.8	10.47	[76]
1, 200	MOCVD/Al_2O_3	6.8×10^{12}	948	709	0.64	403	206	10.2	32.3	[77]
0.25, 200	MBE/Al_2O_3	3.25×10^{13}	>1000	~161	0.46	~1100	246	25	22	[78]
0.38, 200	PAMBE/Al_2O_3	2.8×10^{13}	>1800	~167	-	1300	330	19.6	30.9	[79]
0.4, 200	PAMBE/Al_2O_3	3.5×10^{13}	1300 - 1900	230 - 140		1250	-	-	-	[80]
0.2, 100	PAMBE/Al_2O_3	2.2×10^{13}	1250	318.00 ± 59.73	0.76 ± 0.26	1460	303	50	40	[81]

Chapter 2

Fabrication Techniques

2.1 Introduction

Since this was the first project on GaN-based HEMTs at the University of Glasgow, earlier work was spent on developing and optimising the basic process modules of this technology. This chapter describes the material structures and the processing techniques used for fabrication of AlGaN/GaN HEMTs and AlN/GaN HEMTs grown on sapphire substrate. The processing techniques include sample preparation, lithography, mask plate production, metallisation, mesa isolation and annealing.

2.2 Material Structure

The AlGaN/GaN and AlN/GaN HEMT structures used in this study were grown by SVT Associaties, USA, using molecular beam epitaxy (MBE) on sapphire substrate (0001). The electrical properties of the heterostructures were characterised by SVT Associaties using Hall measurements at room temperature (RT). The

2DEG concentration (n_s) and mobility (μ) for both structures are given in Table 2.1. As-grown sheet resistances (R_{sh}) are calculated using the following equation

$$R_{sh} = \frac{1}{qn_s\mu} \tag{2.1}$$

where q is the electron charge with value of 1.602×10^{-19} C.

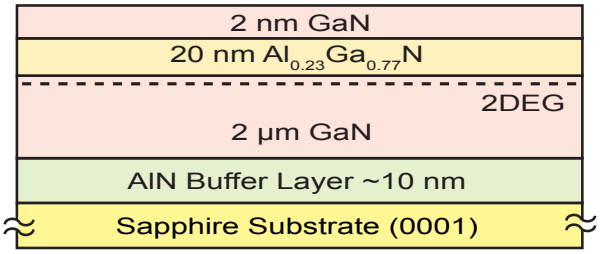
TABLE 2.1: Electrical Properties

Wafer Structure	2DEG (n_s), cm^{-2}	Mobility (μ), $cm^2/V.s$	As-grown R_{sh}, $\Omega/\square$
AlGaN/GaN HEMT	1.08×10^{13}	1450	399
AlN/GaN HEMT	2.20×10^{13}	1250	227

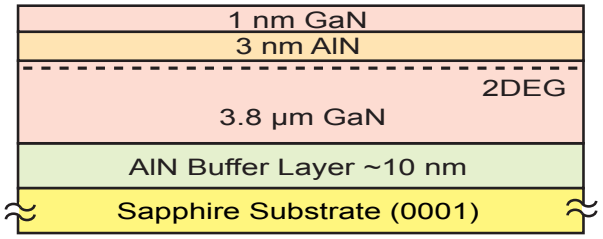
For the $Al_{0.23}Ga_{0.77}N$/GaN HEMT structure, the epitaxial layers consisted of (from top to bottom), a 2 nm GaN cap layer, 20 nm $Al_{0.23}Ga_{0.77}N$, 2 μm GaN, and a thin AlN buffer layer as shown in Fig. 2.1(a).

For the all-binary AlN/GaN HEMT structure, the epitaxial layers consisted of (from top to bottom), a 1 nm GaN cap layer, 3 nm AlN, 3.8 μm GaN, and a thin AlN buffer layer as shown in Fig. 2.1(b). All of the layers for both structures were undoped (or unintentionally doped).

In this work, two different device layout concepts, namely (i) a gate wrap-around and (ii) a conventional HEMT employing mesa isolation step, were used for process development and device optimisation. A gate wrap-around technique is used to simplify device processing and is good for evaluating DC performance of new material structures. While a conventional HEMT technique is used for evaluating not only DC but also radio-frequency (RF) of HEMT structures. Device processing techniques, wafer structures as well as device dimensions investigated in this work are summarised in Table 2.2.



(a) $Al_{0.23}Ga_{0.77}N$/GaN HEMT



(b) AlN/GaN HEMT

FIGURE 2.1: Schematic cross-section for both the AlGaN/GaN and AlN/GaN epitaxial wafer structures.

2.3 Sample Preparation

During the fabrication, surface treatment and cleaning procedures of the sample are very important and unavoidable. Two main reasons why sample preparation is required prior to any processing, are (1) to remove native oxides which form from the exposure of the semiconductor surface to air or other ambients, and (2) to remove residues or debris which formed during the wafer cleaving. Due to the high price of wafers, only a small piece/sample of wafer was used during the processing. The price for a single 50.8 mm diameter wafer of AlGaN/GaN HEMT and AlN/GaN HEMT is approximately £ 2500 and £ 3000 respectively. Therefore, a single 50.8 mm diameter wafer was cleaved into 10 mm × 10 mm samples.

In this project, different sample preparation procedures were used for AlGaN/GaN and AlN/GaN HEMT structures. For the AlGaN/GaN wafer sample, a standard procedure cleaning was used. The wafer sample was placed in a beaker which contained of acetone, followed by isopropyl alcohol (IPA). All the organic solvent cleanings were conducted in an ultrasonic water bath for 5 mins to remove and

TABLE 2.2: Summary of structures/device geometries investigated in this project

Device Concept	Device Processing Technique	Wafer Structure	Device Dimension (L_G, W_G) μm
Gate Wrap-around HEMT	Unprotected HEMT	AlGaN/GaN AlN/GaN	3, 100
Gate Wrap-around HEMT	Protected MOS-HEMT	AlN/GaN	3, 100
Mesa MOS-HEMT	Unprotected mesa sidewall	AlN/GaN	3, 2×100
Mesa MOS-HEMT	Protected mesa sidewall	AlN/GaN	3, 2×100
Mesa MOS-HEMT	Protected mesa sidewall	AlN/GaN	0.5, 2×100
Mesa MOS-HEMT	Protected mesa sidewall	AlN/GaN	0.5, 2×200
Mesa MOS-HEMT	Protected mesa sidewall	AlN/GaN	0.2, 2×100
Mesa MOS-HEMT	Protected mesa sidewall	AlN/GaN	0.2, 2×200
Mesa MOS-HEMT	Protected mesa sidewall	AlGaN/GaN	0.5, 2×200
Mesa MOS-HEMT	Protected mesa sidewall	AlGaN/GaN	0.2, 2×200

clean any organic contaminants from the sample surface. Then, the cleaning procedure was completed with rinsing the sample with the de-ionised (DI) water and blown dry with nitrogen, N_2, gun. While for AlN/GaN structure, only DI water was used during the cleaning procedure due to surface sensitivity of its epilayer surface which will be explained detail in sub-section 4.2.2. De-oxidation process was then done on the AlN/GaN HEMT sample using HCl:$4H_2O$ prior to deposition of aluminium (Al). The need for Al will be explained in sub-section 4.2.3.

2.4 Lithography

Lithography is a fundamental process in the fabrication of any semiconductor device. It involves the process of transferring patterns on a mask to a thin layer of resist, covering the semiconductor wafer surface. The lithography process can be done either by using optical or electron beam (e-beam) lithography. In this project, optical lithography was used for process development of GaN-based devices because it is fast and has the required alignment accuracy for the large gate length ($> 1\,\mu$m). The use of e-beam lithography on the other hand was only for the fabrication of submicron devices later in the project after good device performance had been obtained for larger gate devices.

2.4.1 Optical Lithography

Optical lithography is also known as a photolithography. The process involves transferring of patterns on the mask plate to the wafer surface. The process steps involved are wafer cleaning, photoresist coating, soft baking, mask exposure, photoresist development, oxygen ashing, and post baking.

Photoresist is a radiation-sensitive compound. There are two types of resist, positive or negative photoresist depending on how they react to the ultraviolet (UV) light/radiation. For positive photoresists, the exposed regions become more soluble in developer solutions and thus more easily removed during the development process. As a result, the patterns formed in the positive resist are the same as those on the mask. For negative photoresists, the exposed regions become less soluble in developer solutions and thus more difficult to be removed during the development process. The patterns formed in the negative resist are the reverse of the mask patterns.

The photoresist used for this project was Shipley S1818. It is a positive photoresist and was chosen because of its well developed process in the JWNC. The

optical lithography processing starts with the sample cleaning prior to the photoresist coating. The mask plate is also cleaned prior to the mask exposure. To form a good patterning, the original mask (the chrome mask plate) was used in this project. After cleaning, the photoresist is applied to the wafer surface with constant spinning speed at 4000 rpm for 2 mins. The purpose of this was to ensure that the photoresist coating was uniform on the wafer surface. This results in a thickness of 1.8 μm. After the spinning step, the sample is baked at 65 °C for 2 mins on the hotplate to remove the solvent from the resist film and to increase resist adhesion to the wafer. Then, the sample is aligned with respect to the mask in Karl Suss MA6 mask aligner machine.

When the sample is correctly aligned to the pattern on the mask, the sample is brought into contact with the mask and the photoresist is exposed to the UV light for 5 secs. The exposed resist is dissolved in the developer solution which contained of Shipley Microposit Developer Concentrate:H_2O. The sample is then rinsed with the DI water and dried with N_2 gun.

2.4.2 Electron Beam Lithography

Electron beam lithography (EBL) is primarily used for mask plate production. However, due to submicron or deep submicron patterning requirements, the technique can be used to write a direct pattern onto the resist covering the wafer surface by a focused electron beam without a mask plate. The advantages of this technique include patterning of submicron and deep submicron features, highly automated and precisely controlled operation, positioning/alignment accuracy, ultra high resolution, direct patterning on a semiconductor wafer without using a mask plate, and can be easily accessible for corrections since the layout design for EBL are stored and used electronically in the machine tool system. The disadvantages include low throughput, high of cost operation, complicated and time consuming processing.

The resists used for electron beam (e-beam) lithography are polymers. The behaviour of an e-beam resist is similar to the photoresist, that is, a chemical or physical change is induced in the resist by irradiation which allows the resist to be patterned. For a positive electron resist, the polymer-electron interaction causes chemical bonds to be broken to form shorter molecular fragments which are more easily dissolved by the developer solution during development process. For a negative electron resist, the irradiation causes radiation-induced polymer linking which creates a complex three-dimensional structure and makes the irradiated resist more difficult to be dissolved during the development process as compared to the nonirradiated resist.

Fig. 2.2 shows the summary of data prosesing flow for e-beam submission job used in this project. After creating a pattern file in L-Edit computer-aided design (CAD) software, it is exported in the GDSII file format. Then the pattern is fractured in Computer Aided Transformation Software (CATS), and the final fractured pattern layout with a given substrate size, dose, beam size and resolution is done in Belle software [84]. The Leica VB6 Ultra High Resolution Extremely Wide Field (UWF) machine tool writes the pattern directly onto the resist covering the wafer sample.

In this project, the poly methyl methacrylates (PMMA) was used as a e-beam resist for the ohmic and gate metal liftoff processes during submicron device fabrication. PMMA is a positive resist. PMMA is supplied as powders which are dissolved in solvents (mainly ethyl lactate) to provide different concentrations. Details of the e-beam lithography process using PMMA bilayers will be discussed in sub-section 2.7.

2.4.3 Alignment

It is well known that almost any microscale device or structure requires more than one pattern or level step of fabrication. For example, the fabrication of completed HEMT devices may involve six or more of different processing steps.

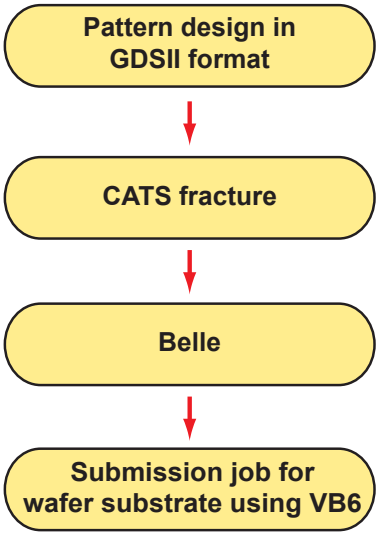


FIGURE 2.2: Data processing flow for e-beam submission job.

In order to make functional devices the patterns for different lithography steps that belong to a single device structure must be aligned to one another. The first pattern transferred to a wafer usually includes a set of alignment marks which are used as a reference when aligning the subsequent patterns to the first pattern. It is important for each alignment mark on the wafer and the subsequent mask/pattern to be labelled so it is more easier to be identified during the alignment/positioning. Alignment accuracy of the MA6 is 0.25 μm and the VB6 is 0.5 nm [85]. Fig. 2.3 shows an example of complete transistor layout design in L-Edit with a set of photolithography and e-beam markers.

2.5 Mask Plate

As previously mentioned, the mask plate is required for patterning the photoresist during photolithography process. After creating a pattern file in L-Edit CAD software, it is exported in the GDSII file format. The pattern is then fractured in CATS, and the fractured pattern with a given substrate plate/mask size, dose and resolusion is handled in Belle software [84]. Technical staff of JWNC are responsible for the processing of mask plates beyond the CAD design and e-beam job submission. The submitted pattern is written using Leica Electron Beam

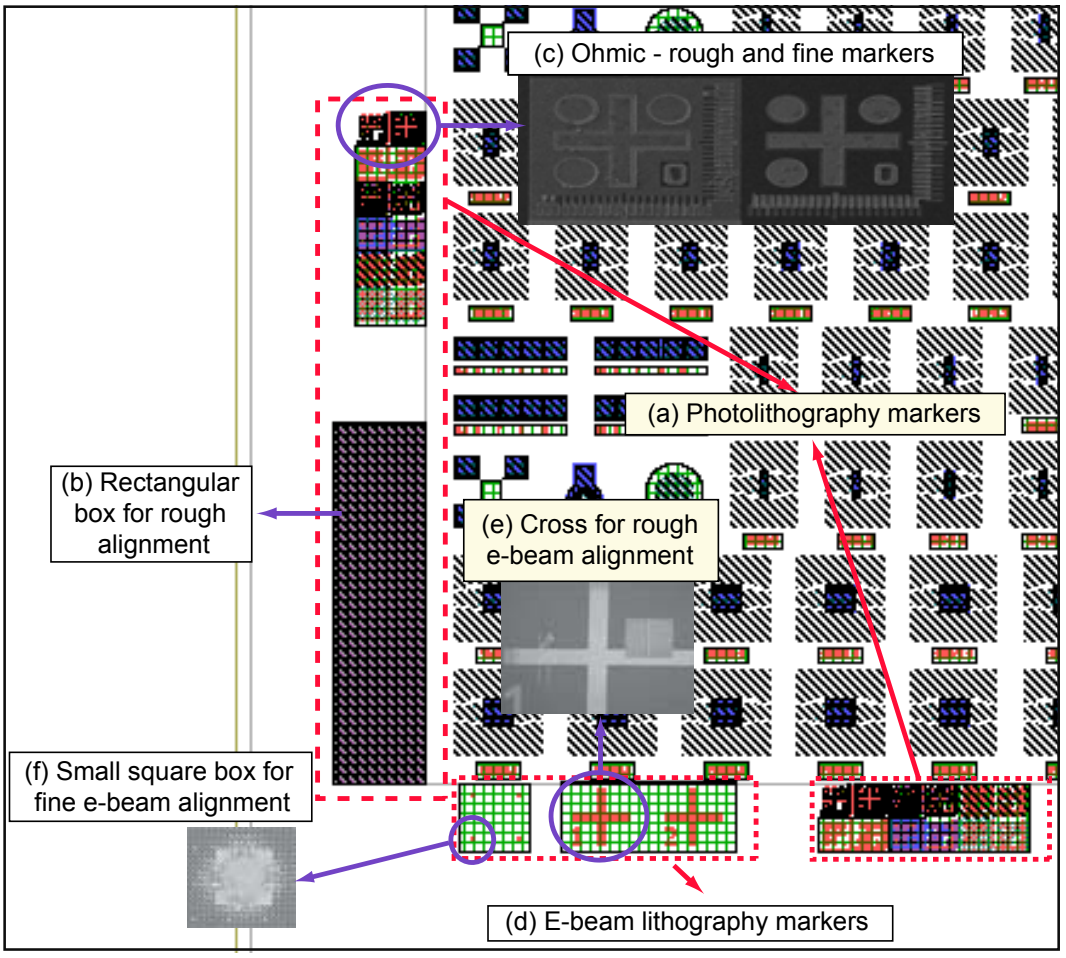


FIGURE 2.3: An example of complete device layout design in L-Edit with a set of photolithography and e-beam markers. (a) A set of photolithography markers, (b) A big rectangular box for rough alignment during photolithograpy processing, (c) Fine and rough alignment for Ohmic step, (d) A set of e-beam markers, (e) A big cross for rough e-beam alignment, and (f) A small box for fine e-beam alignment.

Pattern Generator 5 (EBPG 5) on the specified size of mask plate. The process consists of patterning a quartz mask with chrome on one surface and e-beam resist on top of the chrome. The chrome is then etched away using a chemical wet etch and then the remaining resist removed in a barrel asher leaving the original pattern transferred into the chrome. Fig. 2.4 shows the summary of data prosesing flow for mask plate job submission.

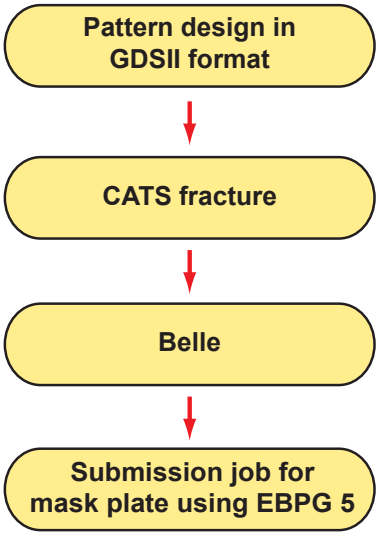


FIGURE 2.4: Data processing flow for mask plate job submission.

2.6 Metallisation

Metal deposition onto semiconductor wafers or samples can be carried out in several different ways including thermal or electron beam evaporation and sputtering. In this project, electron beam evaporation was employed for metallisation process either by using a Plassys MEB 450 electron beam evaporator (Plassys I) or a Plassys MEB 550S (Plassys II). The liftoff technique is commonly employed for metallisation process. This technique is simple and easy for patterning metals that are deposited. A pattern is defined on a substrate using photoresist or e-beam resist. A metal is blanket-deposited all over the substrate covering the photoresist/e-beam resist and areas in which the photoresist/e-beam resist has been cleared. During the liftoff process, the photoresist/e-beam resist under the metal is removed with solvent (e.g. acetone), taking the metal with it, and leaving only the metal which was deposited directly on the substrate. In this work, two different processes for liftoff were developed, which are (1) liftoff using S1818 photoresist for optical lithography, and (2) liftoff using PMMA e-beam resist for electron beam lithography.

2.6.1 Liftoff technique using S1818 photoresist

A chlorobenzene soak prior to exposure of S1818 photoresist is a very well developed technique used for lift-off process but it is not really recommended to use since it has potential hazards to the user. Basically, the sample is soaked in chlorobenzene either prior to UV exposure or just after, but prior to process development. In either case, the sample is rinsed with DI water, and dried with N_2 gun. During the chlorobenzene soak, the top surface of the photoresist is chemically modified to develop at a slower rate than the underlying resist. After the development, the photoresist result should be an undercut profile.

In this project, a new process for metal liftoff was developed to avoid using the chlorobenzene soak. The standard optical lithography process as described in sub-section 2.4.1 was used but in this case the sample is soaked in the developer solution for 1 min prior to the UV exposure. The sample is then rinsed with the DI water and dried with the N_2 gun. Then, the sample is exposed with UV light using MA6 machine. This technique is illustrated in Fig. 2.5.

The exposed resist is dissolved in the developer solution, Shipley Microposit Developer Concentrate:H_2O. The soak in developer solution step causes a hardening of the upper layer of the un-exposed photoresist (i.e. similar effect done by the chlorobenzene soak). Once developed the photoresist profile exhibits an undercut created by an increased development time as shown in Fig. 2.5(b). The sample is then rinsed with the DI water and dried with N_2 gun.

After the development, the sample is ashed in the Oxygen Barrel Asher at 40 W for 3 mins to remove the resist residues. The metal contacts are then formed by evaporation either using Plassys I or Plassys II. After the metal evaporation, the sample is placed in a beaker which is filled with warm acetone. The liftoff process is done in warm water bath at 50 °C. Fig. 2.5 shows the new liftoff process in which a key step is for the coated sample to be soaked in the developer solution. The method is simple and with less hazards as compared to the conventional S1818

liftoff process using chlorobenzene. An example of the top-view inspection under optical microscope after metallisation liftoff is shown in Fig. 2.6.

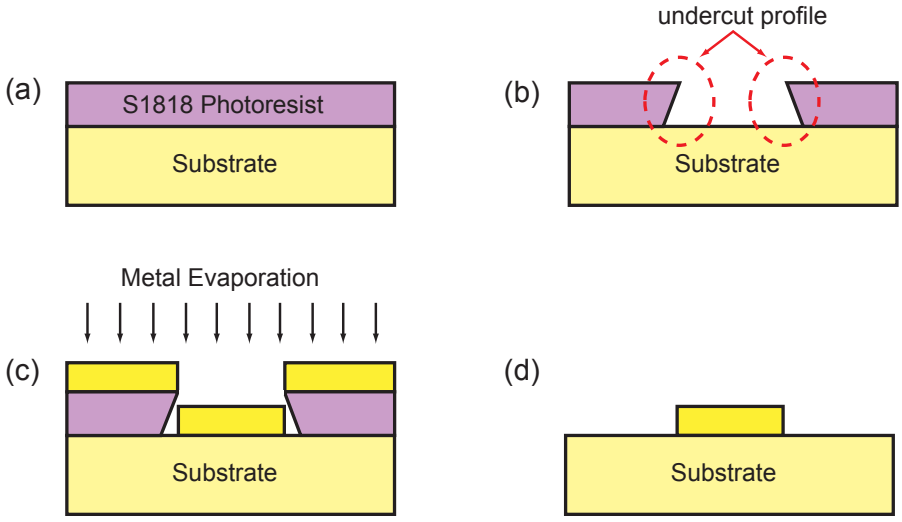


FIGURE 2.5: S1818 photoresist liftoff technique processing summary: (a) S1818 layer coating, pre-bake and soak in the developer solution, (b) After S1818 development, (c) Metal evaporation, and (d) Metal liftoff.

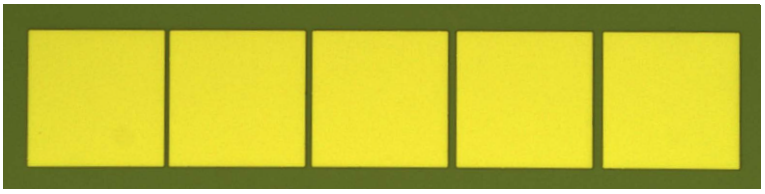


FIGURE 2.6: Optical microscope picture after the metal liftoff process.

2.6.2 Liftoff technique using PMMA e-beam resist

On this project, the poly methyl methacrylates (PMMA) was used as a electron-beam (e-beam) resist for the ohmic and gate metal liftoff processes during submicron device fabrication. PMMA is a positive resist. The two standard molecular weights of PMMA used in the JWNC are 2041 molecular weight (MW) = 345k and 2010 MW = 90k [85]. PMMA is supplied as powders which are dissolved in solvents (mainly ethyl lactate) to provide different concentrations. The developer solution for PMMA is a 4-methylpentan-2-one (methyl isobutyl ketone or MIBK, $C_6H_{12}O$) and IPA. For a liftoff process, bilayers of PMMA are used. The bottom

layer has lower MW and higher concentration, in this case PMMA 2010 is used and for the top layer PMMA 2041, which has higher MW and lower concentration. To produce good liftoff, an under-cut resist profile is needed to avoid coating the sidewall of the resist during the metal evaporation step. This is particularly true for such high beam energies (100 kV) which used in VB6 machine tool during the patterning where the sidewall profile is normally extremely vertical.

The liftoff process starts with first layer coating with PMMA 2010 on the clean wafer surface. Once coated the sample is placed in oven at 180 °C for 30 mins. After baking, the second layer of PMMA 2041 is spun on the same sample, followed with the second baking in oven at 180 °C for 90 mins. The baking step is needed to evaporate the solvent from the resist film. To avoid electron charging effect on sapphire substrate (for transparent substrate), a very thin layer of aluminium, $\sim$30 nm, is deposited on top of the wafer sample before submitting to the VB6. After the exposure, the thin conductive layer Al is etched by CD-26 for 5 mins, followed by rinsing with the DI water, and drying with the N_2 gun. Then, the wafer sample is developed using 2MIBK:IPA solution for 45 secs at 23 °C. The exposed regions (the short chain molecules) are dissolved during the development process.

After the development, the sample is ashed in the Oxygen Barrel Asher at 40 W for 30 secs to remove resist residues. The de-oxidation process is done on the wafer sample using HCl:4H_2O prior to gate metal deposition. Gate metal contacts are formed by evaporation of Ni/Au. After the metal evaporation, the sample is placed in a beaker which is filled with warm acetone. The liftoff process is done in warm water bath at 50 °C. Fig. 2.7 shows the process summary of PMMA bilayers used for the liftoff process and an example of a pattern design in L-Edit with the scanning electron microscope (SEM) of gate metallisation after the liftoff proses is shown in Fig. 2.8.

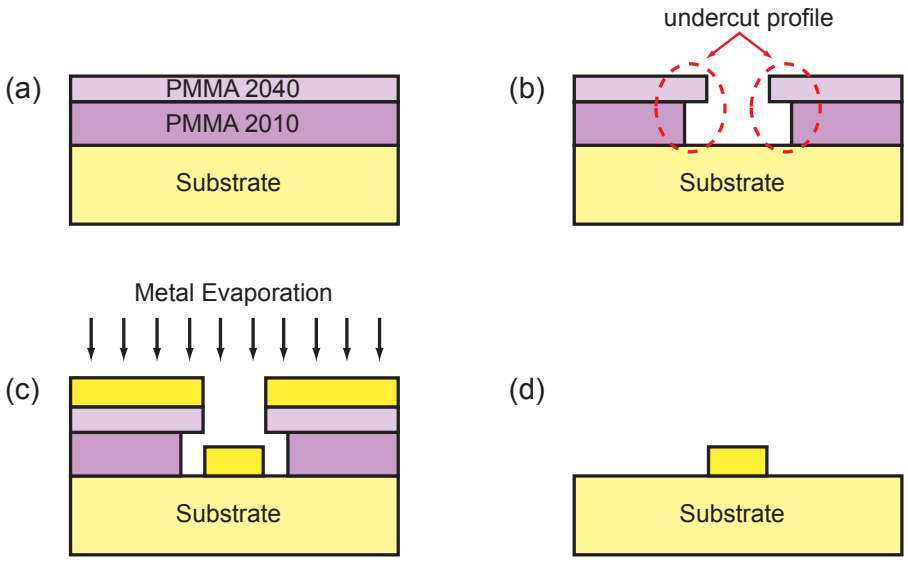


FIGURE 2.7: PMMA bilayers liftoff process summary: (a) First and second layers of PMMA coating, (b) E-beam resists development, (c) Metal evaporation, and (d) Metal liftoff.

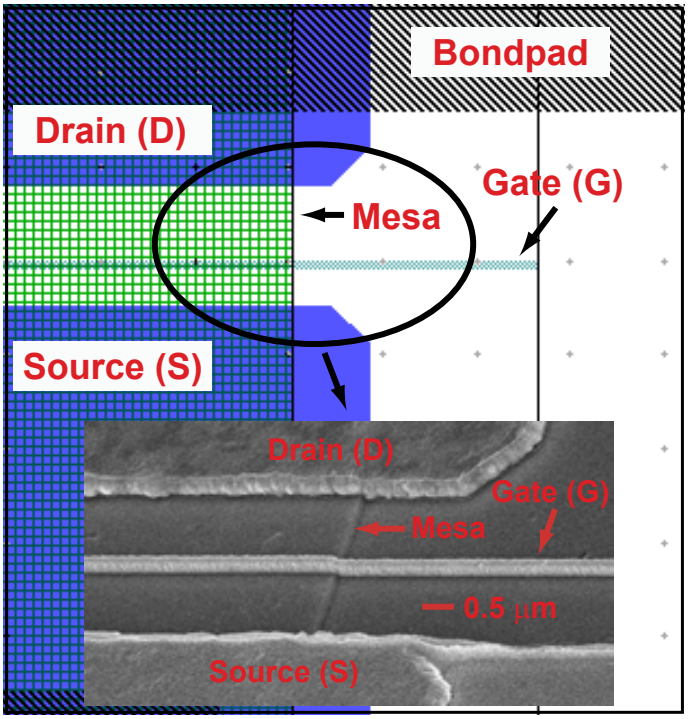


FIGURE 2.8: An example of pattern design in L-Edit. (Inset) Gate metallisation after the liftoff process.

2.7 Device Isolation

In processing HEMT devices, device isolation is an important step to isolate individual devices from each other. In order to obtain a good electrical isolation, the semiconductor should be etched down to the semi-insulating buffer layer, which typically is around 150 - 200 nm etch depth. In the case of GaN-based HEMTs, the etch is performed mostly to the insulating GaN buffer layer as shown in Fig. 2.9-the inset diagram. Due to the chemical stability of group III-nitride semiconductors, it is difficult to etch the materials using wet etch techniques and so dry etching is the dominant technique especially for the mesa structure process. Reactive ion etch (RIE) and inductively coupled plasma (ICP) etching have been widely used and studied to etch the III-nitride materials. ICP etching offers low damage etch compared to the RIE. The most common gas used is chlorine-based or chlorine based mixture gas such as Cl_2/Ar, Cl_2/BCl_3/Ar, $SiCl_4$/Ar, CH_4/H_2. High etch rates, anisotropic profiles, and low damage etching have been achieved if the etching conditions such as radio-frequency (RF) power, direct-current (DC) bias, pressure, gas mixtures, and flow rate are precisely controlled [86],[87].

In this project, the etch optimisations on AlGaN/GaN and AlN/GaN HEMTs were conducted for the mesa structure to produce the accurate condition recipes for both heterostructures. The fabrication starts with the sample cleaning as discussed in Section 2.3. The S1818 photoresist is spun on the sample surface. After the resist spinning step, the sample is baked at 65 °C for 2 mins. Then, the sample is exposed to UV light using MA6. The exposed sample is developed for 75 secs to form the desired pattern. The sample is then rinsed with DI water and dried with N_2 gun. The sample is ashed using the oxygen barrel asher in an O_2 environment. Post baking at 90 °C for 3 mins on the hotplate is done on the sample prior to dry etching step. When the sample is ready, it is etched with given condition parameters such as gases type, gas flow, RF power, and pressure. After the etching, the resist is removed and followed with the etch depth measurement using Dektak profilometer.

Table 2.3 summarises the dry etching process. At first, the etching tests were done using ET430 RIE with gas mixtures of $CH_4/H_2 = 5/25$ sccm, but very low etched rate and poor etched surfaces have been obtained. It seems there was an interaction between CH_4/H_2 with AlGaN and GaN, resulting in very poor etched surfaces. Then, $SiCl_4$ was chosen for the etching optimisation. The System 100 RIE (T-Gate) machine was used since it has faster etch rate as compared to other dry etch machines which are available in JWNC. The optimised chamber conditions is RF power of 75 W, gas flow rate of 30 sccm, pressure of 30 mT and DC bias of 295 V. This results in etch rate of $\sim$4 nm/min and $\sim$3.5 nm/min for AlGaN/GaN and AlN/GaN structures respectively. Fig. 2.9 shows the SEM images of the etched AlN/GaN surfaces with an S1818 mask.

TABLE 2.3: Results summary of the dry etching process

Dry Etch Machine	Conditions Parameters	Etch Rate/Remarks
ET430 RIE	$CH_4/H_2 = 5/25$ sccm 200 W, 40 mT DC bias 900 V	very low etch rate poor etched surfaces
S100 RIE	$SiCl_4 = 10$ sccm 200 W, 40 mT DC bias 900 V	1.4 - 1.7 nm/min good etched surfaces
S100 (T-Gate)	$SiCl_4 = 10$ sccm 200 W, 40 mT DC bias 900 V	40 nm/min good etched surfaces
S100 (T-Gate)	$SiCl_4 = 30$ sccm 75 W, 30 mT DC bias 295 V	AlGaN/GaN HEMT $\sim$ 4 nm/min AlN/GaN HEMT $\sim$ 3.5 nm/min good etched surfaces

2.8 Annealing

Rapid Thermal Anneal (RTA) is used not only for the formation of Ohmic contacts but also for recovering the electrical properties of the devices damaged by etching process (e.g. during the mesa isolation step). For Ohmic contacts, the annealing is carried out in N_2/H_2 environment for 30 - 60 secs. For the annealed Ohmic contacts

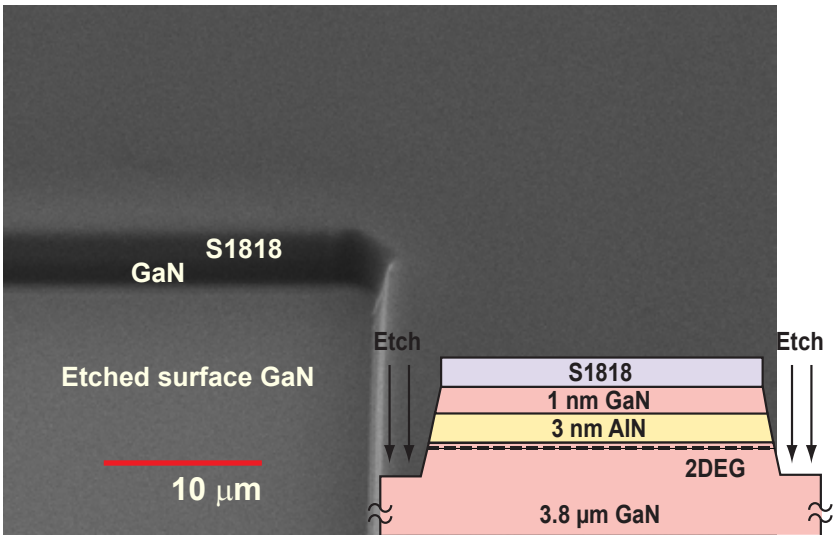


FIGURE 2.9: SEM micrograph of the etched AlN/GaN HEMT surface with S1818 etch mask. (Inset) Schematic cross-section view.

under the optimised conditions in RTA chamber, the contact resistance can be reduced due to alloying. In this project, the equipment used for the annealing was the Joint Industrial Processors for Electronics (JIP ELEC) JetFirst system and the temperature used was 800 °C. Details of the Ohmic contact formation for GaN-based HEMTs are discussed in Chapter 4.

2.9 Summary

The material structures used in this project have been described. The fabrication techniques for both AlGaN/GaN HEMTs and AlN/GaN HEMTs also have been described and discussed. In general, the developed techniques for the conventional AlGaN/GaN HEMTs can be used for the new barrier AlN/GaN HEMTs with the exception of the sample preparation. This is attributed to surface sensitivity of AlN/GaN epilayers which will be discussed in Chapters 4 and 5.

Chapter 3

Ohmic Contact Formation

3.1 Introduction

Optimal performance of GaN-based HEMT devices requires the use of low-resistance, thermally stable Ohmic contacts with smooth surface morphology. This is required for the following reasons: (1) to obtain the maximum value of drain current, I_{DSmax}, (2) to reduce the On-resistance, (3) to minimise the power dissipation in the Ohmic contacts because of the high current densities, and (4) to obtain the maximum value of extrinsic transconductance, G_m, which results in the enhancement of the current gain cut-off frequency, f_T, as well as maximum frequency of oscillation, f_{MAX}, of the devices. For these reasons, Ohmic contact optimisation processing for HEMT and MOS-HEMT in the GaN-based material systems is crucial to achieving good device performance. This chapter describes metal to semiconductor contact formation in the III-nitrides heterostructures. The transmission line method (TLM) for characterising Ohmic contacts will be described and discussed. Finally, a review of Ohmic contacts for both AlGaN/GaN HEMTs and AlN/GaN HEMTs will be presented, and the Ohmic contact processing for these structures will be described and discussed.

3.2 Metal/Semiconductor Contact Formation

When a metal makes intimate contact with an n-type semiconductor, the Fermi levels (E_F) in the two materials must be equal at thermal equilibrium. In addition, the vacuum level must be continuous. These two requirements determine a unique energy band diagram for the ideal metal-semiconductor contact, as shown in Fig. 3.1. For this ideal case, the Schottky barrier height (SBH) $q\phi_{bn}$ and is given by [2]

$$q\phi_{bn} = q\phi_m - q\chi \tag{3.1}$$

where $q\phi_m$ is the metal work function and $q\chi$ is the electron affinity. Electrons start to flow from the semiconductor into the metal until the Fermi energies of both solids are equal (equilibrium condition). In the semiconductor, a space charge region is formed due to ionized donors. In contrast, the electrons for a negative surface charge in the metal layer creating an electric field associated with an electric potential gradient which gives rise to a bending of the bands. The amount of band bending is called the built-in potential qV_{bi} i.e. the built-in potential that is seen by electrons in the conduction band trying to move into the metal, and is given by [2]

$$qV_{bi} = q\phi_{bn} - qV \tag{3.2}$$

where qV is the distance between the bottom of the conduction band (E_C) and the Fermi level (E_F).

There are several ways in which carriers can be transported across a metal-semiconductor junction [88].

i. Thermionic emission (TE), i.e. transport of carriers from the semiconductor over the top of the SBH into the metal.

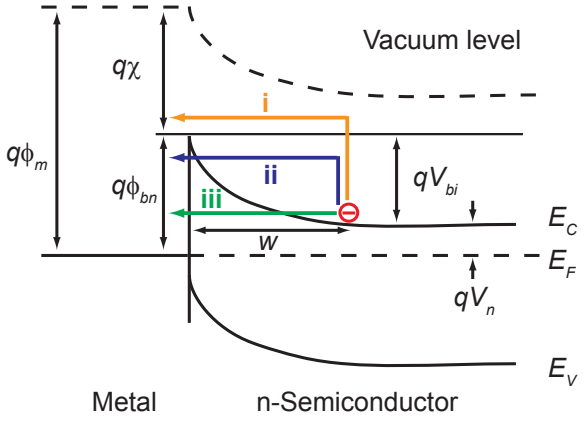


FIGURE 3.1: Energy band diagram of a metal-semiconductor (n-type) contact in thermal equilibrium.

ii. Thermionic field emission (TFE), i.e. the tunneling of hot carriers through the top of the SBH (when high doping levels narrow the depletion layer (w)).

iii. Field Emission (FE), i.e. carrier tunneling through the whole SBH, which is the preferred mode of current transport in Ohmic contacts.

In practical rectifying Schottky diodes with moderately doped semiconductors and moderate operating temperatures, TE is the dominant process of current transport. If a very high doping concentration of the semiconductor material drastically increases the tunneling probability, TFE will become the dominant mechanism of the electron flow. This special kind of current transport is fundamental for Ohmic contacts. The current density-voltage (J-V) characteristics given by the thermionic emission theory [2]:

$$J = J_S(e^{\frac{qV}{nk_BT}} - 1) \tag{3.3}$$

where J_S is the saturation current density, q is the electron charge, V is the applied voltage i.e. positive for forward bias and negative for reverse bias, T is the temperature and k_B the Boltzmann constant. The ideality factor n is approximately independent of V and greater than unity. The saturation current density J_S is

given by Eqn. 3.4 [2]

$$J_S = A^* T^2 e^{-\frac{q\phi_{bn}V}{k_B T}} \tag{3.4}$$

where A^* is the effective Richardson constant. For bias greater than $3k_BT/q$, the J-V characteristics can be approximately written in a simpler form:

$$J = J_S(e^{\frac{qV}{nk_BT}}) \tag{3.5}$$

According to this analysis, the reverse current density of an ideal metal-semiconductor contact should saturate at the value J_S. However, practical diodes normally show great deviations from this ideal behavior.

On the other hand, the electrical properties of the non-rectifying contacts i.e. Ohmic contacts, are characterised by their specific contact resistance ρ_C, defined as [2]

$$\rho_C = \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0} \Omega - cm^2 \tag{3.6}$$

For metal-semiconductor contacts with low doping concentrations, the thermionic emission current dominates the current transport, as given by Eqn. 3.4. Therefore,

$$\rho_C = \frac{k}{qA^*T} exp\left(\frac{q\phi_{bn}}{kT}\right) \tag{3.7}$$

Hence, the formation of low-resistance Ohmic contacts can be achieved by lowering the SBH. Ohmic contacts to wide bandgap materials (e.g. III-nitrides) are generally more difficult to obtain compared to conventional semiconductors, because there are no metals with low-enough work function to yield a low barrier height. Therefore the practical way to obtain a low resistance Ohmic contact is to increase the doping level near the metal-semiconductor interface to a very

high level. So in some cases a highly doped GaN layer is placed at the top of AlGaN/GaN heterostructure in an effort to lower the barrier height.

3.3 Transmission Line Model

Transmission Line Model (TLM) is the commonly used method to assess the electrical properties as well as the quality of the Ohmic contacts [89]. The method was proposed by Reeves and Harrison [90]. In this work, the Ohmic contact resistance was measured on the linear TLM test structures using Agilent's B1500A Semiconductor Parameter Analyzer at room temperature. A schematic diagram of the TLM test structure is shown in Fig. 3.2. It consists of rectangular metal contact pads with increasing spacing between them, L, while W is the contact pad width, d is the contact pad length and Z is the semiconductor mesa width.

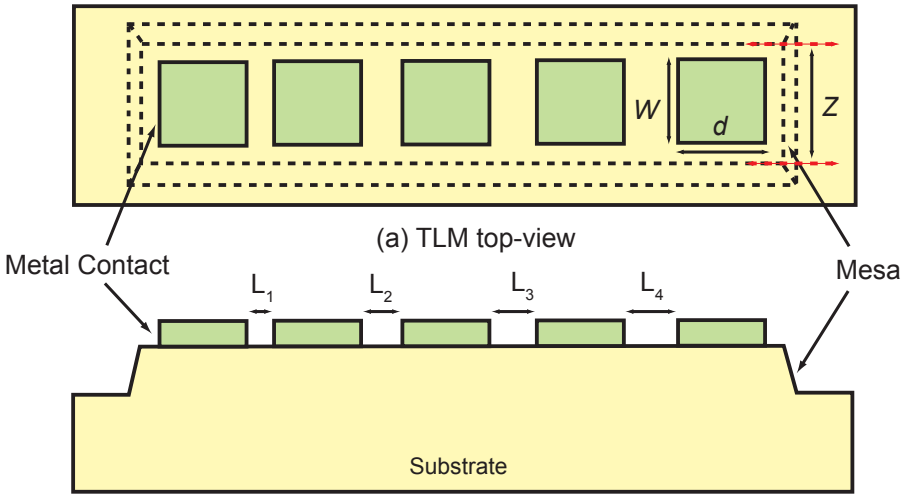


FIGURE 3.2: Schematic of TLM test structure

The four point probe method, where a constant current is supplied by two probes and a second set of probes are used to measure the voltage drop, is used to measure the total resistance, R_T, between two neighbouring pads separated by a distance L and is given by Eqn. 3.8

$$R_T = \frac{2R_{sk}L_T}{W} + \frac{R_{sh}L}{W} \tag{3.8}$$

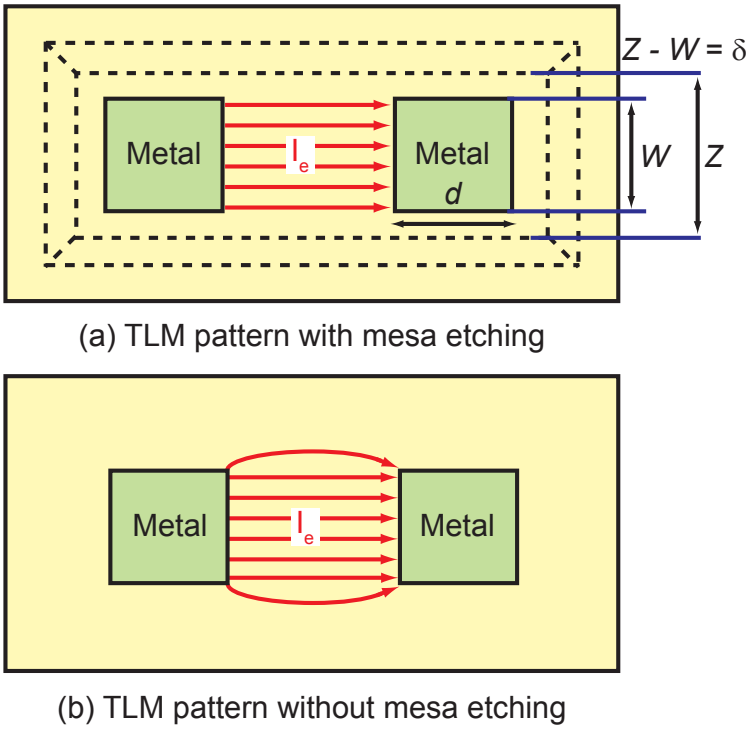


FIGURE 3.3: Current flow in TLM pattern structure (a) with and (b) without having a mesa etch.

where R_{sh} and R_{sk} are the semiconductor sheet resistance between the contact pads and under the contact pads respectively, L_T is the transfer length, and ρ_c is the specific contact resistivity at the metal-semiconductor interface. L_T refers to the distance across which most of the current transfers into the contact pads from the semiconductor and vice versa. All voltage-drops in the horizontal direction are attributed to the current flow in R_{sh} while the voltage drop in the vertical direction, perpendicular to the plane of the current is due to ρ_c.

By plotting R_T as a function of L, a linear fit to the data as shown in Fig. 3.4 can be made. Eqn. 3.8 can also be written as

$$R_T = 2R_C + R_{sh}\frac{L}{W} \tag{3.9}$$

where R_C is the contact resistance. The slope of the line in Fig. 3.4 gives the value of R_{sh}/W and the intercept with y-axis gives the value of $2R_C$. The intercept with

x-axis is called L_x and it is related to the transfer length L_T as:

$$L_x = \frac{2R_C W}{R_{sk}} = 2L_T \tag{3.10}$$

If the pad contact length d is much greater than the transfer length, L_T, ($d \gg L_T$) the effective contact area is approximately WL_T instead of Wd. Thus, the specific contact resistivity from the above expression becomes:

$$\rho_c = R_C W L_T = \frac{(R_C W)^2}{R_{sk}} \tag{3.11}$$

Since in practice ρ_c can be measured for semiconductors then the contact resistance can be calculated. It is to be noted that the value of R_C is independent of the contact length d, and only depends on its width i.e. only on the dimension perpendicular to the current flow. In order to normalise the contact resistance, the value of R_C is multiplied with W to obtain a value in Ω.mm.

For TLM measurements accuracy, the rectangular TLM test patterns should sit on the mesa-isolated structure. This is because the mesa structure confines the current flow within one mesa and the current direction perpendicular to the edge of the metal contacts. In other words, the current flows laterally from one contact to the other contact as shown in Fig. 3.3(a).

It is important to note that, the Eqn. 3.8 is only valid for the one-dimensional transmission line model (1D-TLM). The 1D-TLM is based on the assumption that the current only flows laterally from one contact to the other contact, assuming the contact metal width (W) is identical with the semiconductor mesa width (Z), i.e. $W = Z$. Practically, these conditions are not verified as there is always lithography alignment tolerance that need to be considered during processing.

In the case of W smaller than Z, i.e. Z- $W = \delta$, the lateral current crowding occurs in the gap (δ) between the contact edge and the semiconductor mesa, producing parasitic effects. To provide more accurate extraction of the specific contact resistivity (ρ_c), the two-dimensional transmission line model (2D-TLM)

approach which includes lateral current crowding in the δ region around the contact should be adopted in the TLM analysis.

According to previous works by Loh et al [91] and Chor et al [92], the 1D-TLM analysis is applicable if $\delta \ll W$, in which the effects of lateral current crowding can be neglected. However, for a larger δ/W ratio, the lateral current crowding effects becomes significant and should be included in the TLM analysis to give more accurate ρ_c extraction. If the mesa structure is to be avoided to simplify processing, the circular TLM can be employed [93].

On this project, linear TLM without mesa was used to provide quick turnaround results in the optimisation of the processing, since Ohmic contacts on wide-bandgap GaN are high ($\sim > 0.4\,\Omega$.mm). For final device evaluation (detail in section 4.3), mesa isolation was also used with linear TLM. Comparing results of linear TLM with and without mesa isolation, the contact resistances for the mesa-isolated structures were $0.95 \pm 0.07\,\Omega$.mm (wafer A) and $0.76 \pm 0.26\,\Omega$.mm (wafer B), two times higher than the optimised contact resistance of the un-isolated structures ($0.49 \pm 0.01\,\Omega$.mm). Therefore note that the extracted results from linear TLM described in this section are therefore only indicative and were only useful for process development and optimisation.

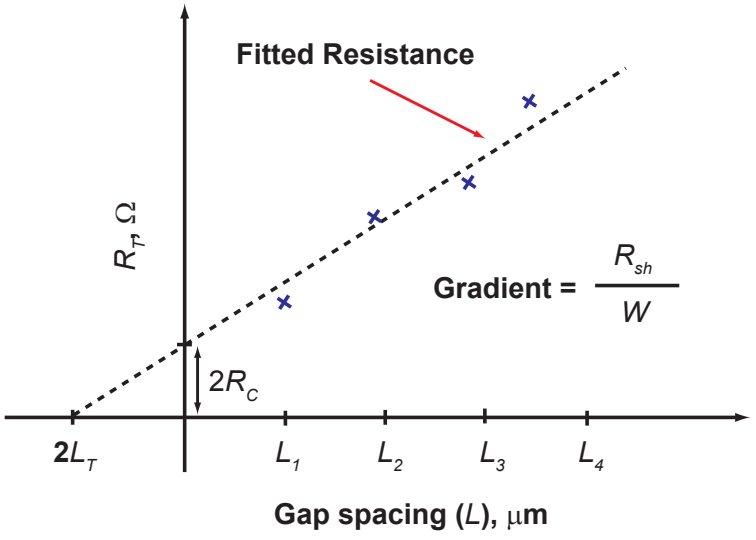


FIGURE 3.4: An example of a plot of total resistance as a function of TLM pad spacing.

3.3.1 A Review of Ohmics on AlGaN/GaN HEMT

For the last decade, research for obtaining low resistance Ohmic contacts to the AlGaN/GaN heterostructures has received great attention and studied intensively by universities and industries. As a wide bandgap material, formation of low resistance Ohmic contacts to AlGaN/GaN is challenging. Various efforts have been reported in forming good Ohmic contacts to these heterostructures. Generally, the metallisation schemes used for making Ohmic contacts on AlGaN/GaN are originally taken from the optimised Ohmic contact processing used for GaN or n-type GaN. The earliest metals used for Ohmic studies for n-type GaN were Al [94], [95], Ti [96], and Ti/Al [94]. Both Ti and Al have relatively low work functions (Al = 4.28 eV and Ti = 4.33 eV) and react with the n-type GaN material to form low Ohmic resistances at high annealing temperature.

With further research on Ohmic contacts on n-type GaN, Fan et al. [97] introduced a new metallisation stack, Ti/Al/Ni/Au, in which two more additional metal layers (Ni/Au) are added on top of Ti/Al layers. This new metal stack produced very low resistance with specific resistivity values of $\rho_c \approx 8.9 \times 10^{-8}\,\Omega.\text{cm}^2$ at the optimal annealing temperature. Since then, a standard Ti/Al/X/Au metallisation scheme (e.g. X is Pt, Ni, Mo) such as Ti/Al/Pt/Au [98], Ti/Al/Ni/Au [99], Ti/Al/Mo/Au [100], and other variants as reported in Table 3.1 is used for n-type GaN and AlGaN/GaN heterostructures. Each of these metal stacks has their own specific role in obtaining the Ohmic behaviour and this is described below;

Titanium To react with N in AlGaN barrier layer to form TiN which has a lower work function, lowering the SBH and therefore helping in contact formation. It also creates N vacancies so that the AlGaN material underneath the contact becomes highly n-doped, enabling electrons to tunnel through the remaining thin potential barrier which separates them from the 2DEG [96],[101].

Al To react with Ti to form an Al_3Ti layer that prevents oxidation of the underlying Ti layer [96] and helps in contact formation [101]. It also reacts with the

semiconductor to form AlN, resulting in N vacancies, which yields a heavily doped interface underneath the contact, enabling electrons to tunnel easily to the 2DEG [94].

Pt, Ni, Ti or Mo To prevent the indiffusion Au and outdiffusion of Al, and the intermixing of Al and Au. The metal layer also plays an important role in forming good contact resistance as well as good surface morphology of the Ohmic contacts after annealed at high temperature [100].

Au To prevent oxidation for Ti and Al metals during high annealing temperature and to improve the Ohmic contacts conductivity [102].

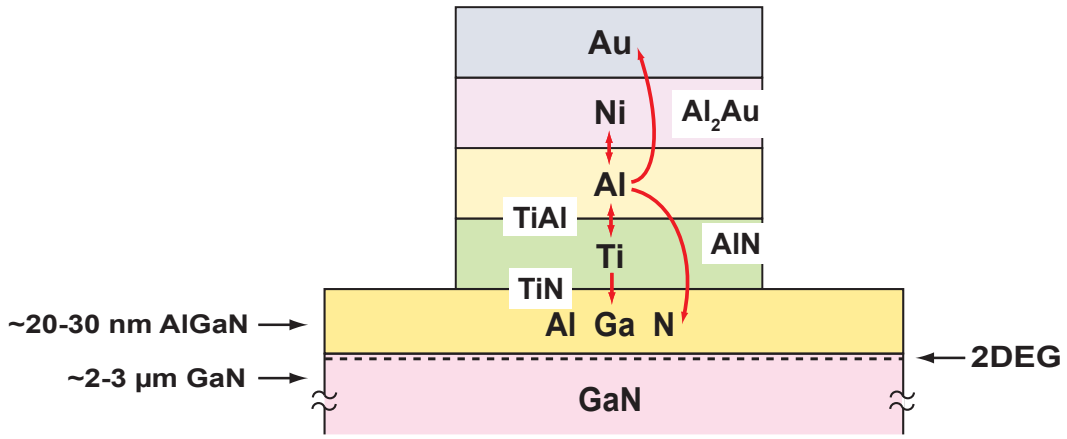


FIGURE 3.5: Reactions among different metals (Ti/Al/Ni/Au) and the semiconductor at high annealing temperature.

Fig. 3.5 shows the reactions among different metals for Ti/Al/Ni/Au metallisation stacks, after high annealing temperature as reported in [101],[103]. It was concluded that the formation of TiN, TiAl, AlN and Al_2Au alloys due to both in- and out-diffusion of Ti and Al are responsible for the formation of Ohmic behaviour in the AlGaN/GaN heterostructures. In addition, the formation of the alloys also creates N vacancies that are known to act as a n-type dopants underneath the contact and therefore help the electrons to easily tunnel through the remaining thin AlGaN layer [94],[96],[101].

A summary of the state of the art Ohmic contacts on AlGaN/GaN heterostructures is shown in Table 3.1. As can be seen, the optimal values of R_C or ρ_c reported

in the literature are varied because of the various factors affecting the contact resistivity such as the type of metallisation stacks used as well as their thicknesses, semiconductor quality (e.g. 2DEG and mobility), Ohmic recessing i.e. etching the AlGaN layer, n-type dopant in the semiconductors, surface pre-treatments prior to Ohmic metallisation, and thermal annealing conditions (e.g. time and temperature).

3.3.2 A Review of Ohmics on AlN/GaN HEMT

In general, formation of good Ohmic contact to AlN/GaN-based devices is difficult, due to having a wide bandgap AlN (6.2 eV) as a barrier layer, as compared to conventional AlGaN/GaN-based devices. This difficulty has been one of the major obstacles in fabricating high performance AlN/GaN HEMTs, and is yet to be completely overcome. In the earlier research of Ohmic contacts on AlN/GaN structures, Xing et al. [61] reported that Ohmic contact formation to AlN/GaN heterostuctures depends on its 2DEG mobility. Contact resistance as low as $\sim 0.36\,\Omega$.mm was obtained on a 3 nm AlN/GaN sample with mobility of $300\,\mathrm{cm^2/V.s}$ at 860 °C, while sample with mobility of $1000\,\mathrm{cm^2/V.s}$ resulted in an open circuit after annealing at 860 °C. Zimmermann et al. [112] suggested that the nonuniformity of the AlN layer, having thin and thick areas of AlN across a sample, gave low R_C value for the low mobility heterostructures. This thin AlN allows the metals to penetrate easily to the semiconductor and forming contact to the 2DEG during annealing.

With improvement in material growth, formation of low contact resistances on the high quality AlN/GaN heterostructures becomes challenging. This means, in low defects/dislocations area it is difficult for electrons to tunnel through the 2DEG. The first study on formation of Ohmic contacts to high quality AlN/GaN heterostructures with $n_s > 1 \times 10^{13}\,\mathrm{cm^{-2}}$ and $\mu > 900\,\mathrm{cm^2/V.s}$ was carried out by Zimmermann et al. [112]. The authors found a dependence of contact resistance with the annealing temperatures, AlN thickness and 2DEG mobility. Similar observations were also reported by Deen et al. [115] who concluded that varying

the AlN thickness has an impact on Ohmic contact formation to AlN/GaN heterostructres.

Optimisation of the Ohmic contact processing on AlN/GaN-based MOS-HEMTs and/or MIS-HEMT structures also has been reported. Due to surface sensitivity of AlN/GaN epilayers, protection layers such as Si_3N_4 and Al_2O_3 are needed to protect the structure during processing [78],[79]. However, in the presence of these protective/passivation layers covering the AlN surface structure, formation of low Ohmic resistance source and drain contacts can be challenging. These protective/-passivation layers need to be removed or etched prior to Ohmic metallisation. The etching of Al_2O_3 is difficult and only very well optimised processes such as using a timed low-power inductively coupled plasma (ICP) to etch the atomic layer deposited (ALD) Al_2O_3 layer prior to Ohmic metallisation produces low resistance Ohmic contacts [78]. On the other hand, for patterning of Si_3N_4, either HF acid or buffered oxide etch (BOE) may be used, or dry etching with SF_6. Both HF and BOE easily attack AlN [79] and therefore because of this, many reports using Si_3N_4, the Ohmic metallisation is deposited directly on the Si_3N_4 thereby resulting in high contact resistances [68],[77]. Summary of the Ohmic contacts on AlN/GaN heterostructures is shown in Table 3.2.

3.4 Ohmic Contact Optimisation

3.4.1 Experiments on AlGaN/GaN HEMT

Optimisation of the Ohmic contacts was first conducted on conventional AlGaN/-GaN HEMT structure since its technology is well established as compared to the AlN/GaN HEMT structure. The details of the heterostructures and its properties used was described in Section 2.2.

Processing steps for the linear TLM test structure are shown in Fig. 3.6. The liftoff technique using S1818 as described in sub-section 2.6.1 was used for TLM contact pads. Ohmic metal contacts were formed by evaporation with metal stacks

of Ti/Al/Ni/Au with 30/180/40/100 nm thicknesses respectively. A de-oxidation process was done with HCl:4H_20 prior to ohmic metal deposition. The reason for this is, gallium oxide, Ga_2O_3 (or often called as a native oxide) is formed on AlGaN or GaN surfaces when the epilayers are exposed to ambient atmosphere. This native oxide acts as a thin insulating layer over the epilayer. Metal contacts deposited on such semiconductors with surface oxides form a metal-insulator-semiconductor structure instead of a metal-semiconductor junction. Hence, it is an important step to remove the native oxide prior to metal deposition on the semiconductor if low resistance Ohmic contacts are to be achieved.

After the metal liftoff, the Ohmic contacts are annealed in a RTA in a N_2 atmosphere. The annealing temperature was varied from 750 °C to 900 °C and the annealing time from 30 secs to 120 secs to determine the optimum process conditions for low resistance Ohmic contacts.

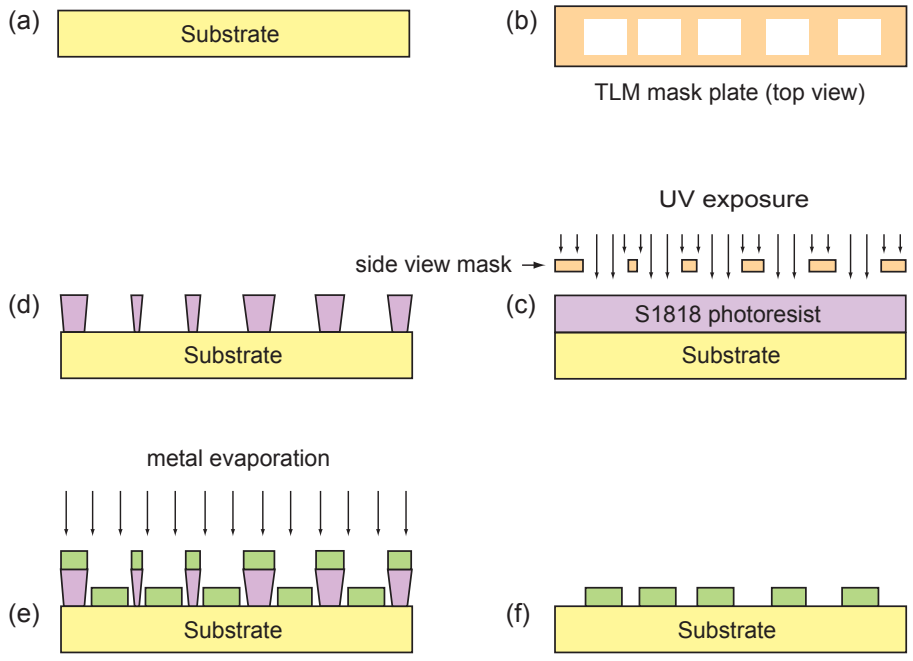


FIGURE 3.6: TLM processing summary: (a) Substrate cleaning, (b) TLM photomask, (c) UV light exposure, (d) Resist development, (e) Metal deposition, and (f) Metal liftoff, followed by annealing and TLM measurements.

Electrical characterisation was performed using the TLM method on 150 × 150 μm pads with the spacing of 5, 7, 9 and 11 μm. Fig. 3.7 shows a SEM micrograph of

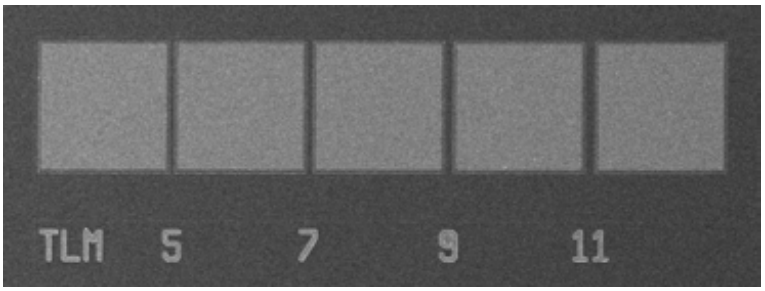


FIGURE 3.7: SEM micrograph of TLM test structures $150 \times 150\,\mu$m pads with the spacing of 5, 7, 9 and 11 μm.

TLM test structure used for the extraction of the contact resistance, R_C, as well as the sheet resistance, R_{sh}, values.

The average total resistance of TLM data was plotted as a function of the varied gap spacing as shown in Fig. 3.8. The gap spacing on the samples was measured using SEM. The linear fit was performed using the least-squares method. Analysing the TLM data for Ohmic contacts annealed at 800 °C for 30 secs the average total resistance can be modeled using Eqn. 3.9. R_C was determined from the Y intercept of the linear fit and R_{sh} was calculated from the slope of the linear fit. This is an example how both R_C and R_{sh} values were extracted from the TLM measurements.

Fig. 3.9 shows the summary of the extracted R_C and R_{sh} values from TLM test structures for Ohmic contacts annealed at different annealing temperature, 750 °C to 825 °C for 30 secs, and at different annealing times, 30 to 120 secs. Details of TLM measurements are given in Tables 3.3,3.4,3.5 and 3.6.

The contact resistances were improved when the samples were annealed between temperature 750 °C to 825 °C, with the optimal R_C and R_{sh} values of 0.32 Ω.mm with a standard deviation of 0.04 Ω.mm (or 12.10 %) and 260.67 Ω/□ with a standard deviation of 3.54 Ω/□ (or 1.36 %), respectively at 800 °C. The average correlation coefficient of 0.9982 showed a good homogeneity of Ohmic contacts annealed at this temperature.

It was difficult to measure the current-voltage (IV) characteristics for the samples which were annealed at 850 °C to 900 °C due to the very poor surfaces on the metal

contacts. Note that all the TLM processing was done without mesa etching, thus both R_C and R_{sh} values were not accurate. However, the extraction values were shown to have small standard deviation and also good correlation coefficient.

As mentioned previously, the R_{sh} is the semiconductor sheet resistance between the contact pads, and supposedly should not change with the annealing temperature. However, the slope (Rsh/W) of the line plotted in Fig. 3.4 often changes after annealing. Large deviation of R_{sh} among the TLM data at different annealing temperature indicates problems during processing.

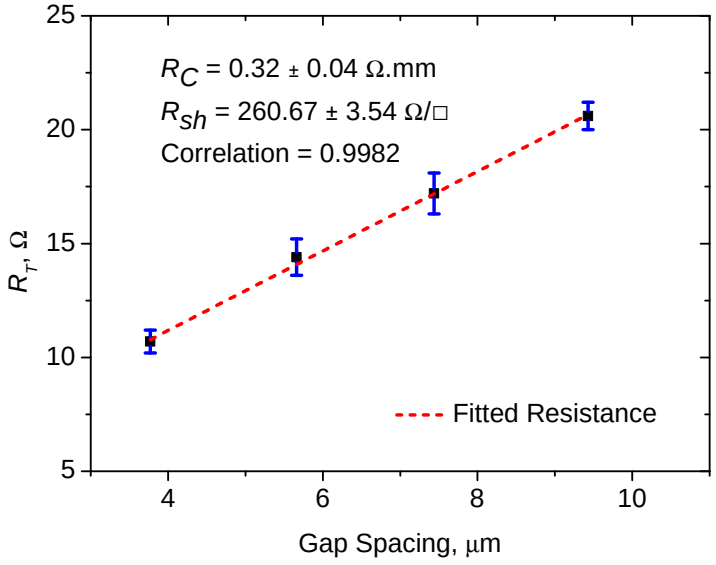
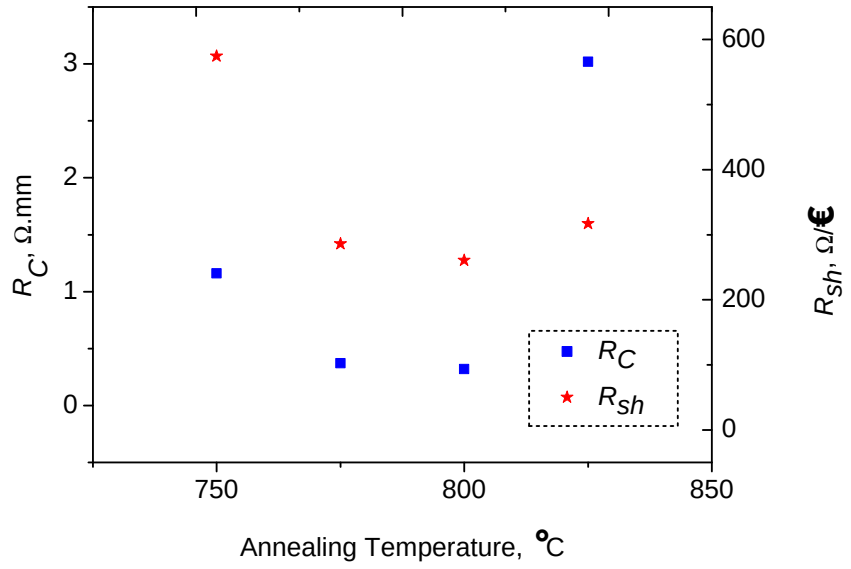
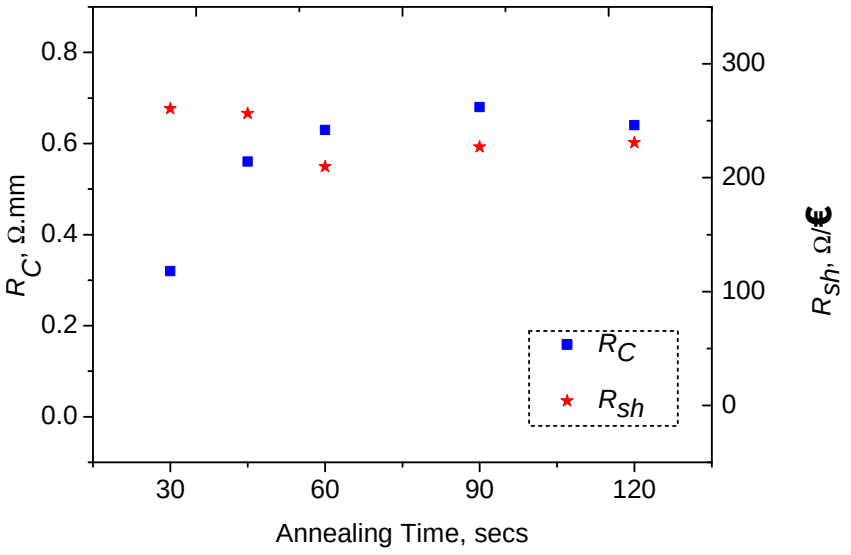


FIGURE 3.8: Extracted R_C and R_{sh} values from TLMs on non-mesa isolated AlGaN/GaN HEMT structures for Ohmic contacts annealed at 800 °C for 30 secs.

Using the optimised annealing temperature of 800 °C, the annealing time was varied from 30 secs to 120 secs in order to investigate the effects of annealing time on AlGaN/GaN contacts. Low resistance Ohmic contacts were obtained when the sample was annealed at 800 °C for 30 secs as shown in Fig. 3.9(b). The contacts started to degrade (higher of R_C value) when the samples were annealed for longer times.



(a)



(b)

FIGURE 3.9: Extracted R_C and R_{sh} values from TLMs on non-mesa isolated structures for Ohmic contacts annealed (a) at different annealing temperatures, 750 to 825 °C for 30 secs, and (b) at different annealing times, 30 to 120 secs.

The optimised measured contact resistance R_C was comparable to the state of the art with other published work for Ohmic contacts on AlGaN/GaN-based devices as shown in Fig. 3.10.

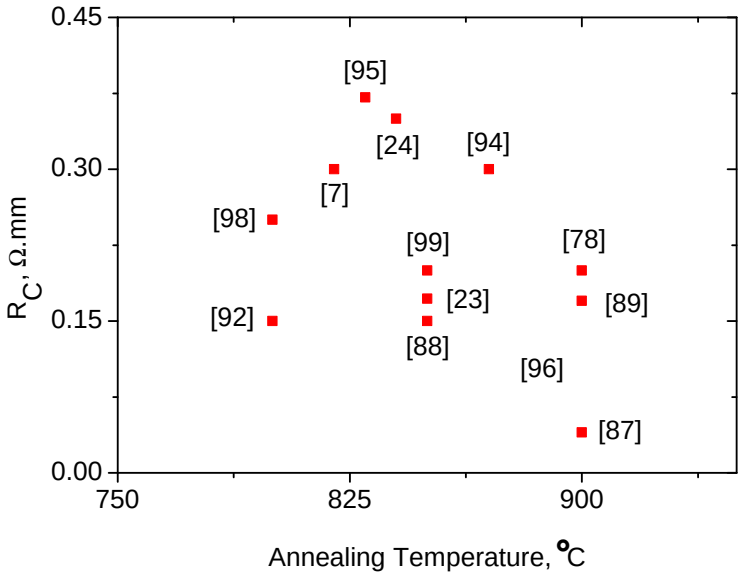


FIGURE 3.10: Comparison of Ohmic contact resistance, R_C, on AlGaN/GaN-based devices as a function of annealing temperatures from various publications.

3.5 Experiments on AlN/GaN HEMT

Initial work on optimising device processing for AlN/GaN HEMTs (or unprotected AlN/GaN devices) revealed that this structure was very sensitive to processing liquids such as acetone and IPA. Having a very thin AlN barrier layer, $\sim 3\,\text{nm}$, makes the epilayers very sensitive to liquids coming in contact with the surface. Exposure to some chemical solutions during device processing degrades the surface properties, resulting in poor device performance.

Although, TLM experimental results of unprotected AlN/GaN HEMTs exhibited low resistance Ohmic contacts, $\sim 0.3\,\Omega.\text{mm}$, devices made on the same structure exhibited very high leakage currents, did not pinch-off, and drain current was very low. The detailed results on unprotected AlN/GaN devices are presented and discussed in sub-section 4.2.2. A new process for Ohmic contact processing on AlN/GaN MOS-HEMTs (or protected AlN/GaN devices) was therefore developed. These results have been published in Ref. [82]. Details of the process optimisation on Ohmic contacts are provided in the following section, including comparative results from unprotected samples.

3.5.1 Unprotected AlN/GaN HEMT

The AlN/GaN HEMT structure used in this work was/is shown in Fig. 2.1(b), and its properties are given in Table 2.1. Due to surface sensitivity of AlN/GaN epilayers [82], the optimisation of Ohmic contacts was divided into two parts. The first part was involved with Ohmic contacts processing without the Al layer (unprotected samples), while the second part was involved with the Al (which was thermally oxidised to form Al_2O_3) layer (protected samples).

Three unprotected bare samples 1, 2 and 3, were processed to determine the optimum annealing temperature. These experiments were also meant to provide comparative performance data for protected epilayers during processing. Another two different samples were prepared, samples 4 and 5, to investigate the effects of liquid chemicals such acetone, isopropanol and developer solutions on the Ohmic contacts. Both samples were prepared using the same processes from (i) to (vi), except that during the sample cleaning the samples were only cleaned with DI water.

Sample 5 was pre-annealed at 800 °C for 30 secs in N_2 ambient to remove the native oxide on top of the sample while sample 4 had no surface treatment. The motivation for employing pre-annealed technique was based on works by Hashim et al [116], where the authors reported that the RTA treatment i.e. annealing at 800 °C for 60 secs in N_2 ambient was effective to remove the native oxide. Details of the fabrication steps were described in Table 3.7. The cross-section of completed TLM structure for unprotected AlN/GaN HEMT sample is illustrated in Fig. 3.11(a).

TLM measurements for samples 2 and 3 are shown in Fig. 3.12. The extracted contact and sheet resistances for the other samples (1, 4 and 5) were too high and are not shown. The results of these experiments are tabulated in Table 3.9, from which it is clear that the process for sample 3 resulted in the lowest contact and sheet resistance, i.e annealing at 800 °C for 30 secs. Even though, samples 2 and 3

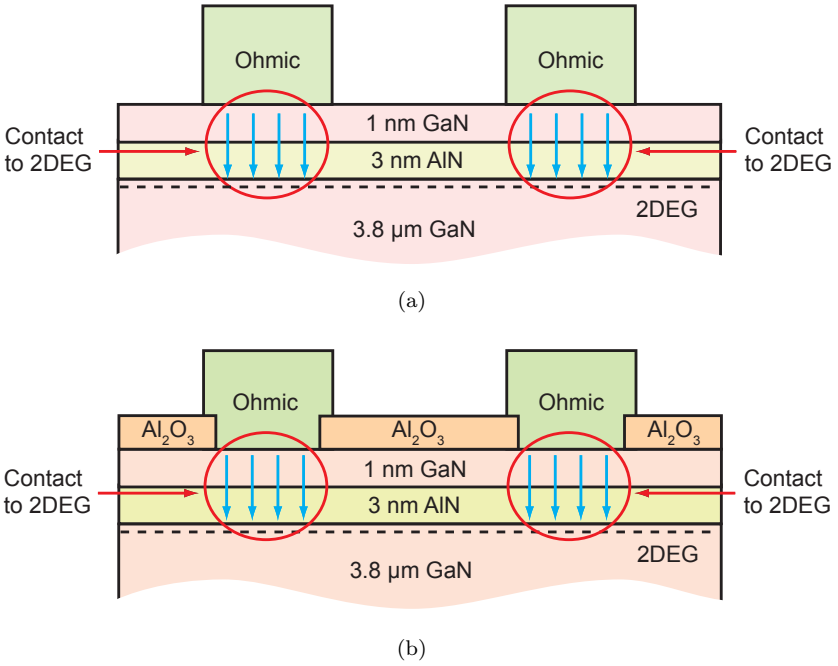


FIGURE 3.11: Cross-section of completed TLM structure for (a) unprotected and (b) protected AlN/GaN HEMT samples.

had measurable contact resistances, the sheet resistance was far higher than one would expect from the 2DEG carrier concentration and mobility of the samples.

3.5.2 Protected AlN/GaN MOS-HEMT

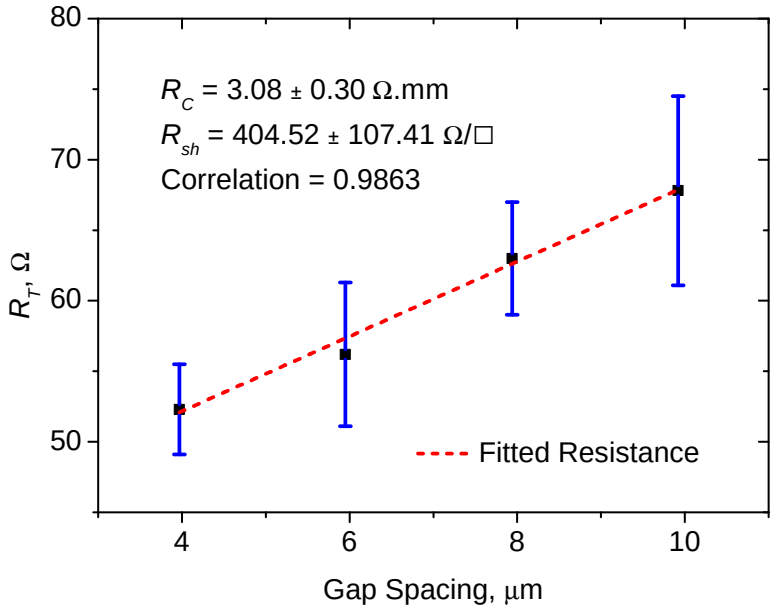
In this part, five samples 6 - 10 were processed to determine the optimum TLM process steps for Ohmic contacts on protected AlN/GaN HEMT. All samples were protected with e-beam evaporated Al which on oxidation formed Al_2O_3. Fabrication involved the following steps:

i. Sample cleaning: only rinsing with DI water (no exposure to liquid chemicals)

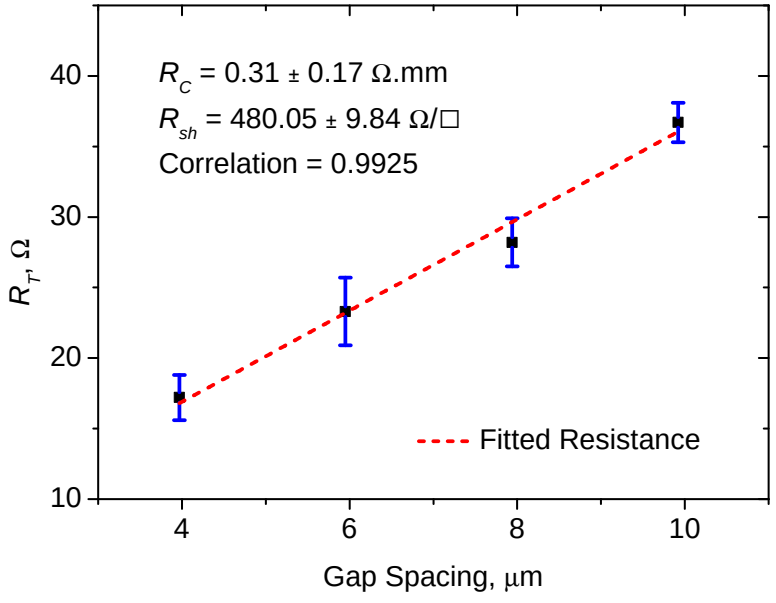
ii. Deoxidation using HCl:$4H_2O$ solution

iii. 2 nm Al deposition using e-beam evaporation

iv. S1818 resist coating and mask exposure



(a)



(b)

FIGURE 3.12: Extracted R_C and R_{sh} values from TLMs on non-mesa isolated structures for Ohmic contacts annealed at different annealing temperatures for 30 secs (a) 700 °C and (b) 800 °C.

v. Resist development and O_2 ashing

vi. Etch Al in the Ohmic regions using $16H_3PO_4$:HNO_3:$2H_2O$ solution (with five different etching time, 10 secs, 20 secs, 40 secs, 60 secs and 120 secs)

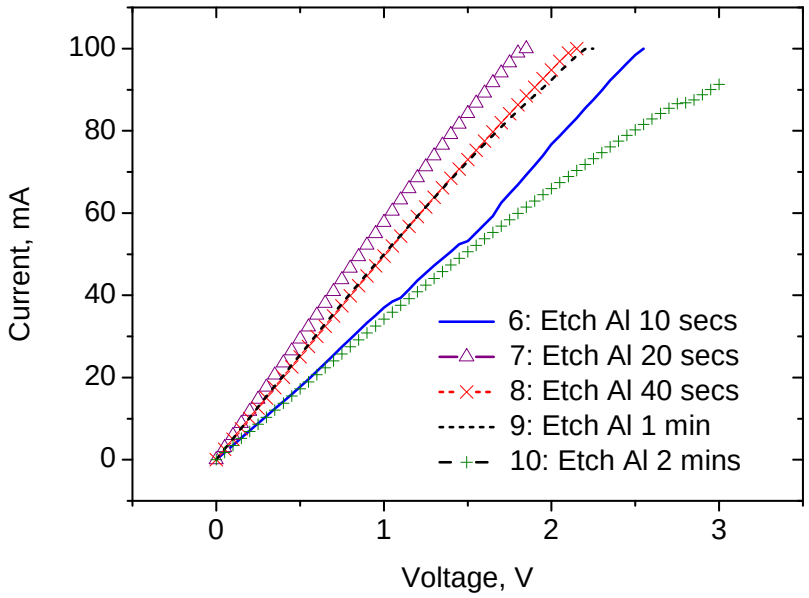
vii. Thermal oxidation of the remaining Al layer using RTA at 550 °C for 10 mins in O_2 environment

viii. Ohmic metal stack deposition and liftoff

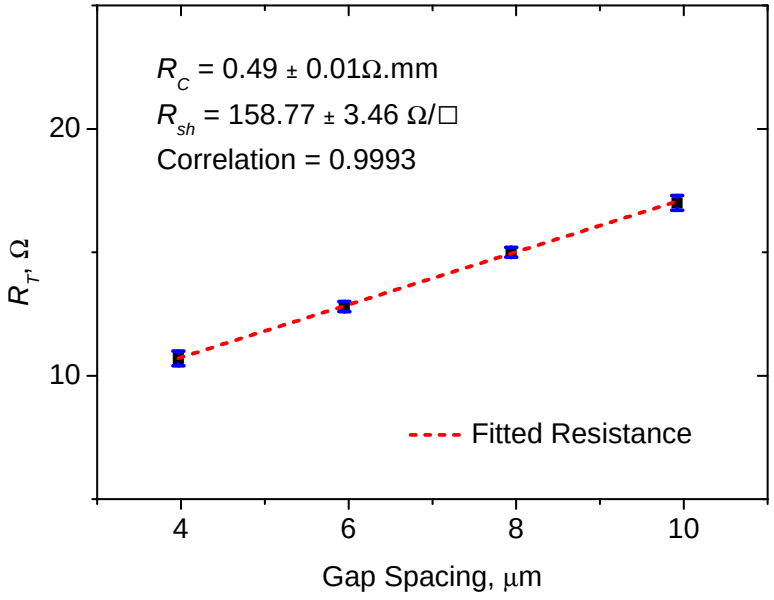
ix. Ohmic contacts annealing at 800 °C for 30 secs

The cross-section of completed TLM structure for protected AlN/GaN HEMT sample is illustrated in Fig. 3.5.2. For the Al-protected samples, the Al in the Ohmic contact regions is etched with $16H_3PO_4$:HNO_3:$2H_2O$ solution prior to oxidation of the Al covering the rest of the device. The Al etching time was optimised and Fig. 3.13(a) shows the measured I-V characteristics on 5 μm TLM gap spacing of annealed Ohmic contacts for different Al etch times. A 20 secs etch resulted in the lowest contact resistance of 0.49 Ω.mm with a standard deviation of 0.01 Ω.mm (or 1.49 %), which is also one of the lowest contact resistance values for this material system. The average correlation coefficient of 0.9993 showed a good homogeneity of Ohmic contacts for the process recipe. If the sample was left longer in the etchant the contact resistance rose indicating that further undesirable reactions may be taking place. Fig. 3.13(b) shows the TLM measurements for protected samples annealed at 800 °C for 30 secs . The extraction values of R_C and R_{sh} for both protected and unprotected samples are shown in Table 3.11.

The results of the optimised processing on Ohmic contacts experiments were reported in Ref. [83]. Unprotected samples had a lower Ohmic contact resistance of 0.31 ± 0.17 Ω.mm compared to 0.49 ± 0.01 Ω.mm for the protected samples. A possible explanation to this reduced contact resistance is that the chemicals have thinned the AlN layer and so the Ohmic contact is formed closer to the 2DEG, resulting in a lower contact resistance. Unlike other techniques for AlN epilayer protection, the thermally grown Al_2O_3 technique described here allows for a simple and effective wet etching optimisation technique for the Ohmic contact resistance. For the comparable ALD grown Al_2O_3, a more complicated, expensive dry etch



(a)



(b)

FIGURE 3.13: (a) Current-Voltage (I-V) characteristics on 5 μm TLM gap spacing of annealed Ohmic contacts for different Al etch times, and (b) TLMs for the optimised Ohmic contact processing for protected on non-mesa isolated Al-N/GaN heterostructures.

is required to optimise the Ohmic contacts [78]. Similar or better results are expected for devices protected with thermally grown Al_2O_3 samples after further optimisation.

So far, all the R_C and R_{sh} values were extracted from the TLM patterns on the non-mesa isolated structure. To provide more accurate R_C and R_{sh} values, the TLM patterns on the mesa-isolated structure were also investigated. These TLM test patterns were actually fabricated along with the devices in order to evaluate the quality of Ohmic contacts made from the complete device level process. The optimised Ohmic contact processing for protected MOS-HEMTs as described in sub-section 3.5.2 was used, with an additional mesa etching step prior to Ohmic regions definition. There are two different TLM results as shown in Fig. 3.14. Details of TLM data for both wafers are tabulated in Table 3.12. Both TLMs test patterns are on the mesa-isolated structures but were processed at different wafers. However, both wafers were processed using same procedures as described in sub-section 3.5.2. To differentiate between these two wafers, the first wafer is labeled as a 'wafer A' and the second wafer is labeled as a 'wafer B'.

Processing for wafer A involves fabrication of large devices i.e., 3 μm gate length while processing for wafer B involves fabrication of small devices i.e., 0.2 μm and 0.5 μm gate lengths. As can be seen, values of R_C and R_{sh} for both wafers are different. For wafer A, the R_C and R_{sh} values were $0.95 \pm 0.07\,\Omega$.mm (or with deviation of 6.97 %) and $257.35 \pm 10.60\,\Omega/\square$ (or with deviation of 4.12 %) respectively. The extraction of R_{sh} gave reasonable value with the as-grown R_{sh} ($227\,\Omega/\square$) for AlN/GaN HEMTs. The increased R_{sh} value was probably caused by the thermally grown Al_2O_3 on the sample surfaces between two metal contacts. Similar observations were also reported by Zimmermann et al [74], where both R_C and R_{sh} values were increased from 0.9 to 1.5 Ω.mm and 165 to $243\,\Omega/\square$ after deposition of 5 nm SiNx on top of a 4 nm thin AlN barrier.

For wafer B, the R_C value was reduced to $0.76 \pm 0.26\,\Omega$.mm (or with deviation of 33.99 %) and the R_{sh} value was increased to $318.00 \pm 59.73\,\Omega$.mm (or with deviation of 18.78 %). These results indicate that there are always variation from wafer

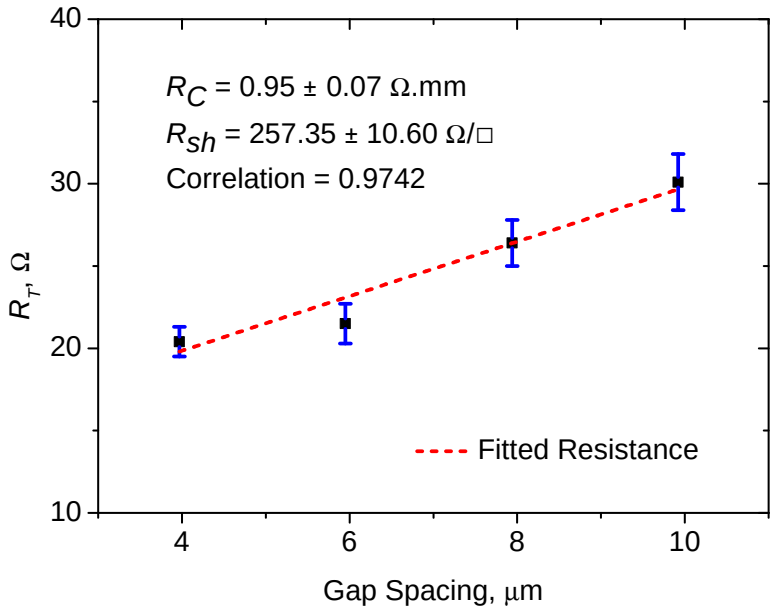
to wafer although similar processing or technique were used for both wafers. More research is needed to investigate the problem.

By comparing the TLMs results between the un-isolated and the mesa-isolated structures, clearly, the extracted values of R_C and R_{sh} on the un-isolated structures were not accurate. However, the use of un-isolated TLM structures provide a simple and effective solution for developing and optimising processes/recipes for forming good Ohmic contacts on GaN-based structures. This is very important especially for investigation/evaluating new material structures such as AlN/GaN HEMTs. It is important to note here that the circular TLM structures should have employed for process development as there do not require a mesa [93].

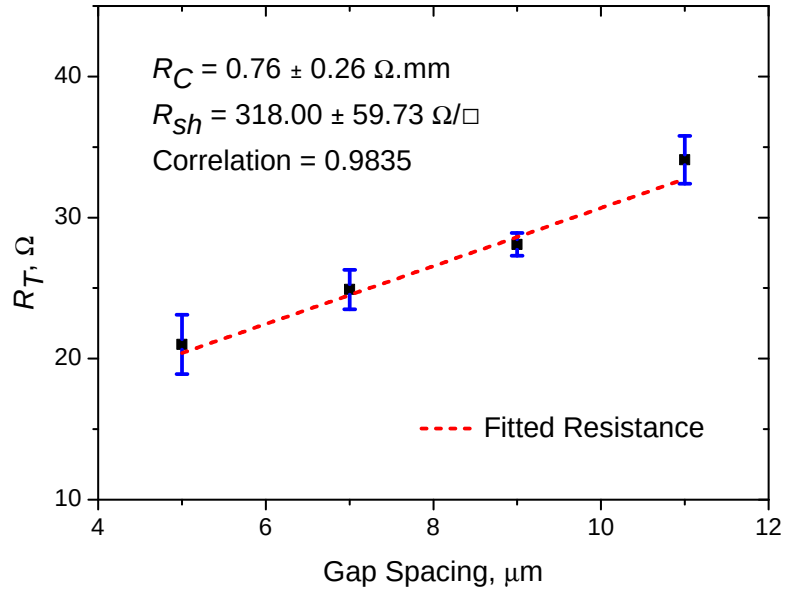
A comparison between the measured contact resistance R_C which was obtained in this work with other published work for AlN/GaN-based devices is shown in Fig. 3.15. As can be seen, the optimised values for Ohmic contact resistances for this material system, 0.95 Ω.mm [83] and 0.76 Ω.mm [81], still needs to be further reduced in order to take fully advantage of the superior properties of AlN/GaN HEMTs.

3.6 Summary

The optimisation of Ohmic contacts on conventional AlGaN/GaN HEMT structures has been described. In the case of Ohmic contacts on AlN/GaN-based devices, an alternative approach in forming low resistance Ohmic contacts has been developed to overcome the surface sensitivity of its barrier epilayer. The method employs Al for protection of the epilayers, but which is removed from the Ohmic contact areas via wet etching. The wet etching can be optimised to reduce the contact resistance. The remaining Al is oxidised to form Al_2O_3. By using this approach, very low contact and sheet resistance have been achieved on AlN/GaN MOS-HEMT structures.



(a)



(b)

FIGURE 3.14: Extracted R_C and R_{sh} values from TLM test patterns on mesa-isolated AlN/GaN MOS-HEMT structure for Ohmic contacts annealed at 800 °C for 30 secs (a) TLMs on wafer A and (b) TLMs on wafer B.

TABLE 3.1: Ohmic contacts to AlGaN/GaN HEMT structures

Metal Schemes	Al mole fraction, %	RTA Conditions	R_C, Ω.mm	ρ_c, $\Omega.cm^2$	Ref.
Ti/Al/Pt/Au	-	900 °C, 35 secs, N_2	0.039	5.38×10^{-8}	[98]
Ti/Al/Ni/Au	25	900 °C, 30 secs, N_2	0.2	7.30×10^{-7}	[99]
Ti/Al/Ni/Au	20 - 30	800 °C, 45 secs, N_2	~ 0.15	-	[104]
Ti/Al/Mo/Au	30	850 °C, 30 secs	0.172	2.96×10^{-7}	[100]
Ti/Al/Ni/Au	27	900 °C, 30 secs, N_2	0.17	7.70×10^{-8}	[101]
Ti/Al/Ni/Au	23	850 °C, 30 secs	0.21	6.17×10^{-7}	[105]
Ti/Al/Mo/Au	25	850 °C, 30 secs, N_2	~ 0.15	-	[40]
Ti/Al/Ni/Au	40	820 °C	0.3	-	[18]
Ti/Al/Ni/Au	30	870 °C, 30 secs	0.3	-	[106]
Ti/Al/Mo/Au	25	840 °C, 30 secs	0.35	-	[41]
Ti/Al/Ni/Au	-	830 °C, 15 secs	0.371	-	[107]
Si/Ti/Al/Mo/Au	30	800 °C, 30 secs	0.31	-	[108]
Mo/Al/Mo/Au	20	650 - 800 °C, N_2	$\sim 0.22 \pm 0.02$	$\sim 9 \times 10^{-7}$	[109]
Pd/Al/Ti/Au	-	800 °C, 120 secs	0.25 ± 0.02	5.95×10^{-7}	[110]
Ti/Al/Mo/Au	20	850 °C, 30 secs, N_2	0.2	4.5×10^{-7}	[111]

TABLE 3.2: Ohmic contacts to AlN/GaN HEMT structures

Metal Schemes	2DEG, cm^{-2}	μ, $cm^2/V.s$	RTA Conditions	R_C, $\Omega.mm$	ρ_c, $\Omega.cm^2$	R_{sh}, $\Omega/\square$	Ref.
Ti/Al/Au	1.5×10^{13}	340	900 °C, 30 secs, N_2	-	2×10^{-6}	-	[72]
Ti/Al/Pt/Au	8.25×10^{13}	150	600 °C, N_2	0.72	8.25×10^{-6}	-	[73]
Ti/Al/Ni/Au	2.33×10^{13}	365	840 °C	-	3.3×10^{-7}	-	[68]
Ti/Al/Mo/Au	$\sim 2.7 \times 10^{13}$	~ 1370	875 °C, 30 secs	~ 1.1	-	165	[66]
Ti/Al/Ni/Au	$> 1 \times 10^{13}$	> 900	400 - 860 °C	0.8 - 2	-	-	[112]
Ti/Al/Ti/Au	6.8×10^{12}	948	850 °C, 30 secs, N_2	0.64	1.15×10^{-5}	709	[77]
Ti/Al/Ti/Au	0.98×10^{13}	900	850 °C, 30 secs, N_2	1.75	1.14×10^{-4}	569	[76]
Ti/Al/Mo/Au	-	-	800 °C, 30 secs	0.455	1.01×10^{-5}	-	[113]
Si/Ti/Al/Ti/Au	1.5×10^{13}	1100	820 °C, 60 secs, N_2	-	1.70×10^{-6}	388	[114]
Ti/Al/Ti/Au	$> 10^{13}$	-	800 °C, 30 secs	$\sim 0.22 \pm 0.02$	$\sim 9 \times 10^{-7}$	-	[60]
Ti/Al/Ni/Au	2.5×10^{12}	700	800 °C, 30 secs	0.8 - 1.1	-	-	[115]
Ti/Al/Ni/Au	3.6×10^{13}	~ 1200	-	0.93	-	144	[69]
Ti/Al/Ni/Au	3.25×10^{13}	> 1000	N_2	0.457	-	161	[78]
Ti/Al/Ni/Au	2.8×10^{13}	> 1800	850 °C, 30 secs	-	-	167	[79]

Table 3.3: Results of TLMs on non-mesa isolated AlGaN/GaN HEMT structure at annealing temperature 750 °C and 775 °C for 30 secs

Temp., °C	750			Temp., °C	775		
	TLM1	TLM2	TLM3		TLM1	TLM2	TLM3
R_C, Ω.mm	1.17	1.13	1.17	R_C, Ω.mm	0.37	0.37	0.36
R_{sh}, Ω/□	593.27	581.21	548.87	R_{sh}, Ω/□	284.71	284.65	287.89
Correlation	0.9957	0.9949	0.9769	Correlation	0.9987	0.9993	0.9991
		SD	SD %			SD	SD %
R_C (ave)	1.16	0.02	2.11	R_C (ave)	0.37	0.00	1.12
R_{sh} (ave)	574.45	22.96	4.00	R_{sh} (ave)	285.75	1.86	0.65

Table 3.4: Results of TLMs on non-mesa isolated AlGaN/GaN HEMT structure at annealing temperature 800 °C and 825 °C for 30 secs

Temp., °C	800			Temp., °C	825		
	TLM1	TLM2	TLM3		TLM1	TLM2	TLM3
R_C, Ω.mm	0.31	0.37	0.29	R_C, Ω.mm	3.00	3.02	3.05
R_{sh}, Ω/□	259.75	264.58	257.68	R_{sh}, Ω/□	319.09	316.95	314.69
Correlation	0.9995	0.9968	0.9983	Correlation	0.6630	0.6670	0.6650
		SD	SD %			SD	SD %
R_C (ave)	0.32	0.04	12.10	R_C (ave)	3.02	0.02	0.74
R_{sh} (ave)	260.67	3.54	1.36	R_{sh} (ave)	316.91	2.20	0.70

Table 3.5: Results of TLMs on non-mesa isolated AlGaN/GaN HEMT structure at annealing time 45 secs and 60 secs for 800 °C

Time, secs	45			Time, secs	60		
	TLM1	TLM2	TLM3		TLM1	TLM2	TLM3
R_C, Ω.mm	0.60	0.59	0.50	R_C, Ω.mm	0.63	0.61	0.64
R_{sh}, Ω/□	235.00	238.41	295.54	R_{sh}, Ω/□	207.19	226.85	195.07
Correlation	0.9991	0.9912	0.9933	Correlation	0.9988	0.9916	0.9994
		SD	SD %			SD	SD %
R_C (ave)	0.56	0.05	9.02	R_C (ave)	0.63	0.02	2.51
R_{sh} (ave)	256.32	34.01	13.27	R_{sh} (ave)	209.70	16.04	7.65

TABLE 3.6: Results of TLMs on non-mesa isolated AlGaN/GaN HEMT structure at annealing time 90 secs and 120 secs for 800 °C

Time, secs	90			Time, secs	120		
	TLM1	TLM2	TLM3		TLM1	TLM2	TLM3
R_C, Ω.mm	0.71	0.61	0.72	R_C, Ω.mm	0.71	0.61	0.61
R_{sh}, Ω/□	218.36	243.82	218.36	R_{sh}, Ω/□	218.36	243.82	230.02
Correlation	0.9997	0.9975	0.9997	Correlation	0.9997	0.9975	0.9927
		SD	SD %			SD	SD %
R_C (ave)	0.68	0.06	8.73	R_C (ave)	0.64	0.06	9.03
R_{sh} (ave)	226.85	14.70	6.48	R_{sh} (ave)	230.73	12.74	5.52

TABLE 3.7: Fabrication steps for the unprotected TLMs on AlN/GaN HEMT structure

Sample	Fabrication Steps
1, 2, 3	(i) Sample cleaning using acetone, isopropanol and rinsing with DI water (ii) S1818 resist coating and mask exposure (iii) Resist development and O_2 ashing (iv) De-oxidation using HCl:4H_2O solution (v) Deposition of Ti/Al/Ni/Au metal stack and liftoff (vi) Ohmic contacts annealing using RTA at 600 °C 700 °C and 800 °C for 30 secs in N_2 environment
4	(i) Sample cleaning with only DI water. Then, sample was prepared using the same processes from (ii) to (vi)
5	(i) Sample cleaning with only DI water, and followed by pre-annealed at 800 °C for 30 secs in N_2 ambient. Then, sample was prepared using the same processes from (ii) to (vi)

TABLE 3.8: Results of TLMs on non-mesa isolated AlN/GaN HEMT structure at annealing temperature 700 °C and 800 °C for 30 secs

Temp., °C	700			Temp., °C	800		
	TLM1	TLM2	TLM3		TLM1	TLM2	TLM3
R_C, Ω.mm	2.74	4.15	3.26	R_C, Ω.mm	0.31	0.14	0.47
R_{sh}, Ω/□	464.32	206.80	280.52	R_{sh}, Ω/□	480.06	489.89	470.21
Correlation	0.9697	0.4399	0.9921	Correlation	0.9933	0.9924	0.9920
		SD	SD %			SD	SD %
R_C (ave)	3.38	0.72	21.15	R_C (ave)	0.31	0.17	53.38
R_{sh} (ave)	317.21	132.62	41.81	R_{sh} (ave)	480.05	9.84	2.05

TABLE 3.9: Results of TLMs for unprotected on non-mesa isolated AlN/GaN HEMT samples

Sample	Annealing Temperature, °C	R_C, Ω.mm	R_{sh}, Ω/□
1	600	very high	very high
2	700	3.38 ± 0.72	317.21 ± 132.62
3	800	0.31 ± 0.17	480.05 ± 9.84
4	800	high	high
5	800	high	high

TABLE 3.10: Results of TLMs on non-mesa isolated AlN/GaN MOS-HEMT structure at annealing temperature 800 °C for 30 secs.

Temperature, °C	800		
	TLM1	TLM2	TLM3
R_C, Ω.mm	0.48	0.49	0.49
R_{sh}, Ω/□	158.01	155.75	162.55
Correlation	0.9994	0.9993	0.9993
		SD	SD %
R_C (average)	0.49	0.01	1.49
R_{sh} (average)	158.77	3.46	2.18

TABLE 3.11: Summary of results of the TLMs for the unprotected (HEMT) and protected on non-mesa isolated (MOS-HEMT) AlN/GaN samples

Sample	Description,	$R_C, \Omega.mm$	$R_{sh}, \Omega/\square$
3	Unprotected (HEMT)	0.31 ± 0.17	480.05 ± 9.84
7	Protected (MOS-HEMT)	0.49 ± 0.01	158.77 ± 3.46

TABLE 3.12: Results of TLMs on mesa-isolated AlN/GaN MOS-HEMT structure at annealing temperature 800 °C for 30 secs.

Sample	Wafer A			Sample	Wafer B		
	TLM1	TLM2	TLM3		TLM1	TLM2	TLM3
R_C, Ω.mm	0.99	0.99	0.88	R_C, Ω.mm	0.56	0.66	1.05
R_{sh}, Ω/□	248.78	269.20	254.07	R_{sh}, Ω/□	343.50	360.75	249.75
Correlation	0.9784	0.9781	0.9662	Correlation	0.9946	0.9811	0.9748
		SD	SD %			SD	SD %
R_C (ave)	0.95	0.07	6.97	R_C (ave)	0.76	0.26	33.99
R_{sh} (ave)	257.35	10.60	4.12	R_{sh} (ave)	318.00	59.73	18.78

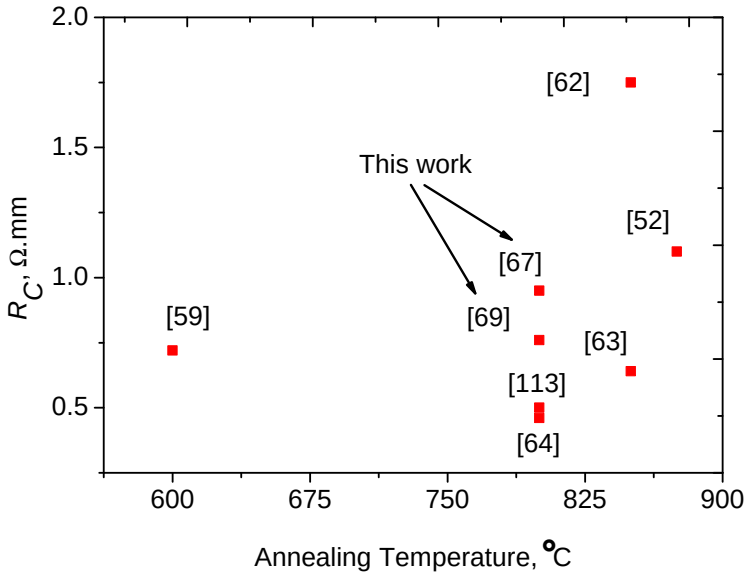


FIGURE 3.15: Comparison of the R_C as a function of annealing temperatures on AlN/GaN-based heterostructures from various publications.

Chapter 4

Device Fabrication and Characterisation

4.1 Introduction

This chapter focuses on the processing and characterisation of high-power, high-frequency AlN/GaN MOS-HEMT devices which employ thermally grown Al_2O_3 as a gate dielectric, and for surface protection and passivation. Initial work is carried out on gate wrap-around large area devices which require only 2 - 3 lithography steps to establish basic processing steps. Thereafter processing of 0.2 μm and 0.5 μm long gate AlN/GaN RF devices is described and the achieved results discussed.

4.2 Gate Wrap-Around MOS-HEMT Optimisation

Processing of GaN-based HEMTs typically requires 8 photolithography steps [117] and this can therefore be time consuming when assessing new HEMT material

structures. The RoundHEMT [118] and gate wrap-around [119] concepts, requiring just 2 - 3 process steps, have been reported and have successfully been used to evaluate and characterise the quality of HEMT structures.

In this work, a gate wrap-around layout technique [119], where the gate electrode encircles the drain as shown in 4.1, was employed for process development and optimisation on AlN/GaN HEMT structures. This technique consists only of Ohmic and gate metallisation, eliminating the mesa isolation step. During process development, $10 \times 10\,\text{mm}$ samples cleaved from a 2-inch were used.

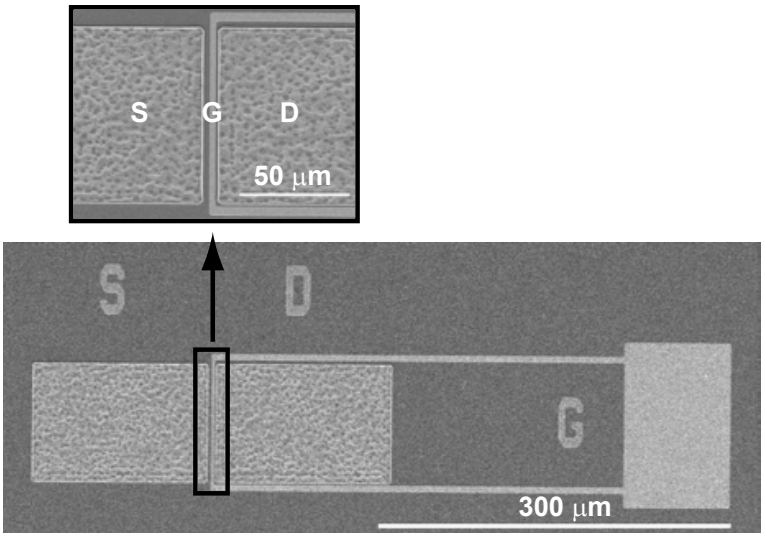


FIGURE 4.1: SEM micrograph of completed gate wrap-around AlN/GaN HEMT layout. Inset: Device with $L_{SD} = 6\,\mu$m and $L_G = 3\,\mu$m.

4.2.1 Unprotected AlGaN/GaN HEMT

AlGaN/GaN HEMTs were first fabricated to establish the processing steps for making devices. During process development, $10\,\text{mm} \times 10\,\text{mm}$ samples cleaved from a 2-inch wafer were used. Fig. 4.2 shows the complete process flow for fabrication of unprotected AlGaN/GaN HEMT using the gate wrap-around technique. Device fabrication starts with standard sample cleaning using acetone, isopropanol and DI water.

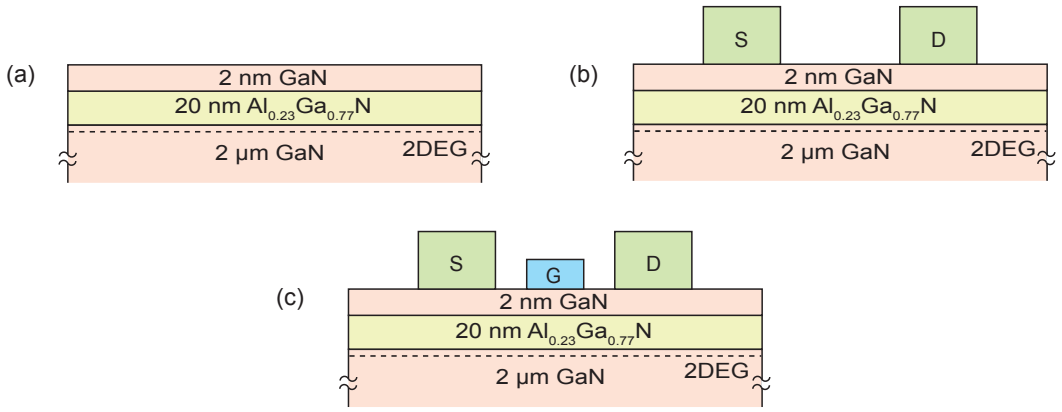


FIGURE 4.2: Process flow for fabrication of unprotected AlGaN/GaN HEMTs using the gate wrap-around technique. Processing includes: (a) Sample cleaning and de-oxidation, (b) Ohmic metallisation and annealing, and (c) Gate metallisation and device measurements.

The optimised Ohmic contact processing in sub-section 3.4.1 was employed for fabrication of unprotected AlGaN/GaN HEMT devices. De-oxidation was done on the Ohmic contact regions by HCl:4H_2O solution prior to Ohmic metal deposition. Ohmic metal contacts were formed by evaporation of Ti/Al/Ni/Au, followed by a lift-off process and then annealing at 800 °C for 30 s. Thereafter, gate metal contacts were formed by evaporation of Ni/Au and followed by liftoff process.

DC measurements were done by contacting the probe needles directly on top of the source (S), drain (D) and gate (G) structures. All measurements were made at room temperature using Agilent's B1500A Semiconductor Parameter Analyzer. Fig. 4.3(a) shows the I_{DS} - V_{DS} characteristics of fabricated unprotected 3 μm × 100 μm device on AlGaN/GaN HEMT structure. Devices made on this material system exhibited good gate control of drain currents up to a gate bias of 1 V and achieved a maximum drain current of ∼800 mA/mm. The devices also showed both good pinch-off and good saturation characteristics.

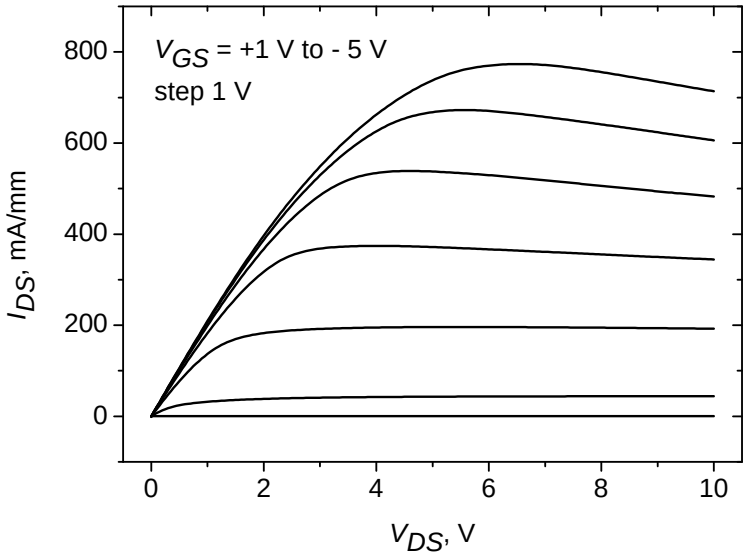
4.2.2 Unprotected AlN/GaN HEMT

By using the developed device processing for AlGaN/GaN HEMTs, unprotected AlN/GaN HEMTs were then fabricated. Ohmic contact processing in subsection 3.11(a) was employed for the source and drain contact regions. Fig. 4.3(b) shows the I_{DS} - V_{DS} characteristics of fabricated unprotected $3\,\mu\text{m} \times 100\,\mu\text{m}$ device on AlN/GaN HEMT structure. In contrast to I_{DS} - V_{DS} characteristics of unprotected AlGaN/GaN HEMTs, devices made on AlN/GaN HEMT structure exhibited very high leakage currents, did not pinch-off and the drain current was very low.

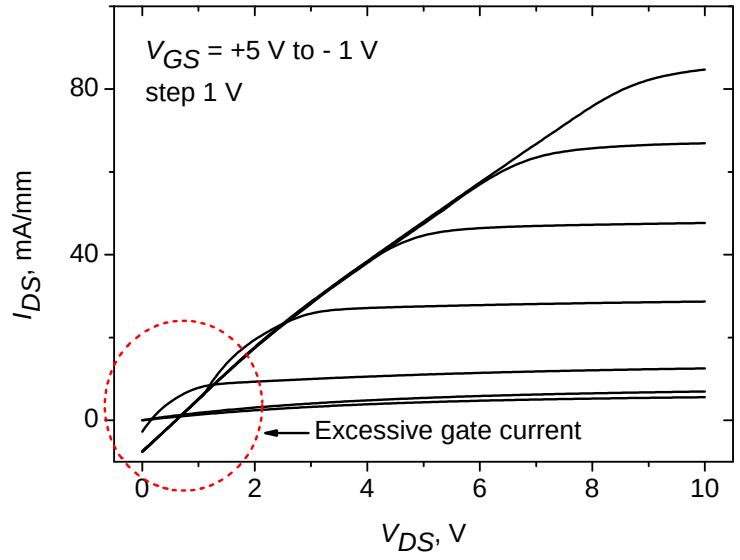
These results, together with the TLM results described in Section 3.11(a), showed that there were some issues with processing of AlN/GaN HEMT structure which are not seen in AlGaN/GaN HEMTs. Exposure to different processing chemicals such as resist developer and solvents solutions could help reduce the Ohmic contact resistance but at the same time this may have led to the degradation of the quality of the AlN/GaN epilayer structures. Similar observations were made by Fan et al. [97] on the formation of low Ohmic contact on n-GaN materials, where reduced Ohmic contact resistance was caused by the damage of the RIE process employed prior to deposition of the Ohmic contact metallisation. The AlN/GaN HEMT devices suffered from surface sensitivity and high leakage currents, confirming earlier reports [78], [79], and it is therefore necessary to protect the AlN/GaN epitaxial layers during device processing.

4.2.3 Protected AlN/GaN MOS-HEMT

Based on earlier problems as described in Section 4.2.2, a new process for the fabrication AlN/GaN-based devices was therefore developed. It involved employing thermally grown Al_2O_3 for protection of the very sensitive AlN epilayer from exposure to liquid chemicals during processing [82] as earlier described for TLM experiments in Section 3.5.2. This Al_2O_3, which is formed by thermal oxidation



(a)



(b)

FIGURE 4.3: I_{DS}-V_{DS} characteristics of fabricated unprotected with $3\,\mu\text{m} \times 100\,\mu\text{m}$ devices, (a) AlGaN/GaN HEMT, and (b) AlN/GaN HEMT.

of evaporated Al, acts as a surface protection and as a gate dielectric for the transistors. Al_2O_3 is also expected to act as a passivation layer [21].

The optimised Ohmic contacts processing as described in Section 3.5.2 was used in the fabrication of the MOS-HEMT devices. Fig. 4.4 shows the process flow for

the fabrication of protected AlN/GaN MOS-HEMTs using the gate wrap-around technique. Device fabrication starts with sample cleaning (only rinsing with DI water, no exposure to liquid chemicals such acetone and isopropanol). Prior to 2 nm Al deposition, deoxidation using HCl:4H_2O solution was done on the samples.

A 2 nm Al layer was then deposited on the sample surface using electron beam evaporation. Low deposition rate $\sim$0.05 nm/s was chosen to ensure the uniformity of the Al deposition on the sample surfaces. Next, the Al in the source and drain regions was etched using 16H_3PO_4:HNO_3:2H_2O solution for 20 secs, followed by oxidation of the remaining Al layer using RTA at 550 °C for 10 mins in an O_2 environment to form the Al_2O_3 [120].

Ohmic metal contacts were formed by evaporation of Ti/Al/Ni/Au, followed by liftoff process then annealed at 800 °C for 30 secs. Gate metal contacts were formed by evaporation of Ni/Au. TLM and metal-oxide-semiconductor (MOS) test structures were also fabricated on the same epilayer structure in order to evaluate the quality of Ohmic contacts as well as the quality of the oxide layer made from this complete wrap-around device level process.

Fig. 4.4 shows the process flow for the fabrication of protected AlN/GaN MOS-HEMT using the gate wrap-around technique. MOS diodes were fabricated at the same time to evaluate the quality of the oxide. Fig. 4.5 shows the SEM micrograph of MOS structure and its schematic used in this work. DC and capacitance-voltage (CV) measurements were made at room temperature. For CV measurements, the test MOS structures were characterised using Agilent N1301A-100 SCUU (SMU CMU unify unit) (this unit is integrated with the B1500A semiconductor device analyzer) which is capable of performing automatic switching of the measurement resource connected to the device under test (DUT). The measurement resource can be capacitance measurement unit (CMU) or one of two source measurement units (SMUs) connected to the SCUU [121].

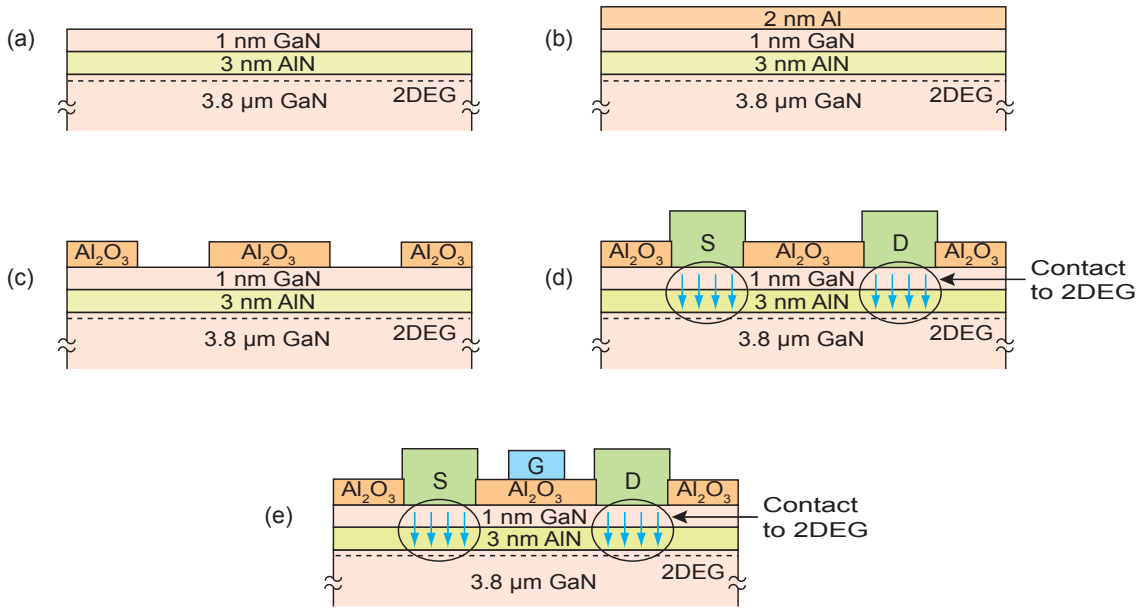


FIGURE 4.4: Process flow for fabrication of protected AlN/GaN MOS-HEMTs using the gate wrap-around technique. Processing includes: (a) Sample cleaning and de-oxidation, (b) 2 nm Al deposition, (c) Etching Ohmic regions and thermal oxidation of Al, (d) Ohmic metallisation and annealing, and (e) Gate metallisation and device measurements.

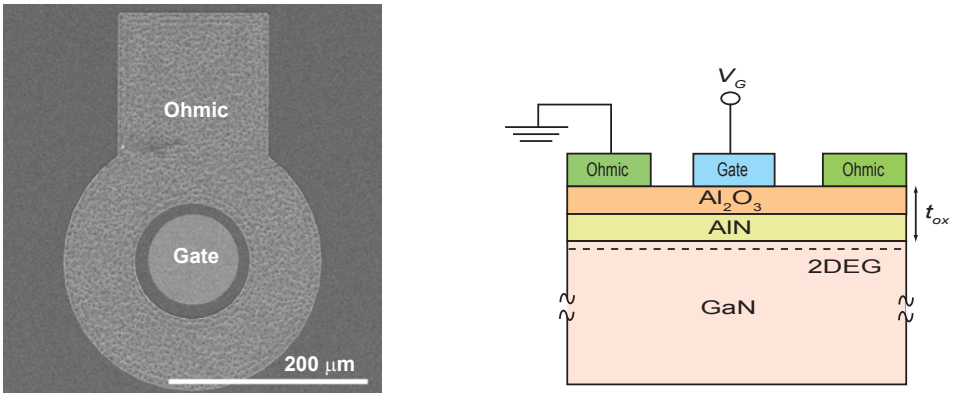
4.2.4 Device Results and Discussion

4.2.4.1 GaN MOS Diode

Fig. 4.6(a) shows the CV characteristics of Al_2O_3/AlN/GaN circular test MOS structures with a 90 μm diameter. The CV characteristics were measured at 1 MHz with a voltage amplitude of 50 mV. The curve clearly shows deep depletion behaviour for reverse gate voltages with no hysteresis being observed, attesting to the good quality of the oxide. The sharp capacitance transition from depletion to 2DEG accumulation is in good agreement with published data for thermally grown Al_2O_3 on AlGaN in Ref. [120]. Assuming that the total thickness of thermally grown Al_2O_3 and AlN barrier layer is t_{ox}, (since the AlN barrier layer is very thin, $\sim$3 nm) can be extracted from the measured oxide capacitance, C_{ox}, using the Eq. 4.1

$$t_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} A}{C_{ox}} \tag{4.1}$$

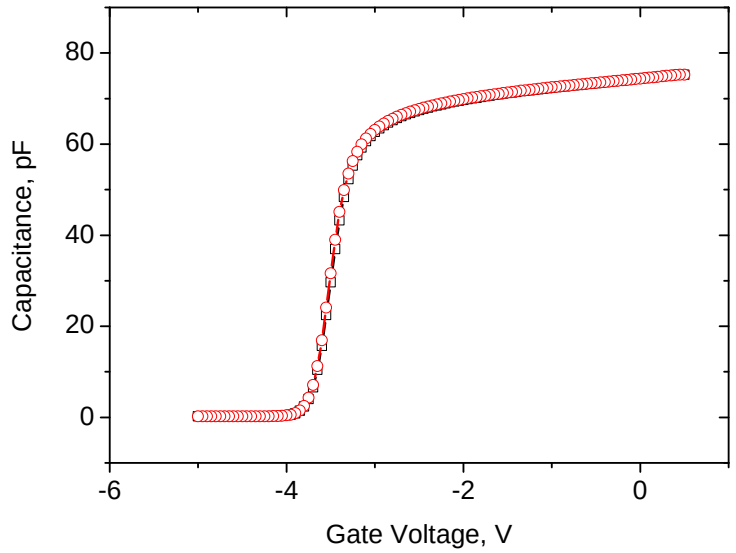
where ε_0 is the permittivity of free space, ε_{ox} is the average relative permittivity of Al_2O_3 and AlN, where the permittivity of Al_2O_3 [122] and AlN [123] is ~ 8 and ~ 8.5, respectively, and A is the capacitor area. The calculated t_{ox} is $\sim 6\,\text{nm}$, which gave the oxide thickness of $\sim 3\,\text{nm}$. The leakage currents characteristics of the test MOS structures were also measured and is shown in Fig. 4.6(b). The gate leakage current was $\sim 10^{-5}\,\text{A}$ at $V_{GS} = -2\text{V}$ which is at least one order of magnitude lower than the gate current of the AlN/GaN HEMTs treated with the oxygen plasma in Ref. [80].



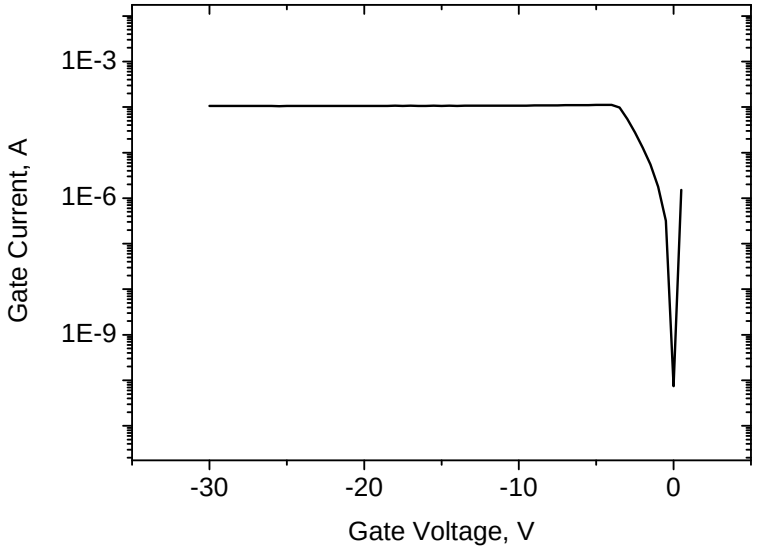
(a) (b)

FIGURE 4.5: (a) SEM micrograph of MOS structure and (b) Schematic cross-section.

Fig. 4.7 shows the atomic force microscope (AFM) measurement of the surface roughness before and after thermally grown Al_2O_3 on AlN/GaN HEMT. After Al_2O_3 formation, the measured surface roughness (scan area is $25\,\mu\text{m}^2$ slightly increased from 1.186 nm (as-grown) to 1.207 nm, which indicates the thermally grown Al_2O_3 has good step coverage and thickness uniformity. This also verifies that only a very thin layer of oxide has formed after the thermal oxidation process on AlN/GaN structure. Temperature dependent C-V measurements were not made and so no comments will be made on how the structure may have behaved. However, results published in Ref. [124] for SiO_x/GaN diode showed that as the measuring temperature increases, the flatband voltage shift to higher values.

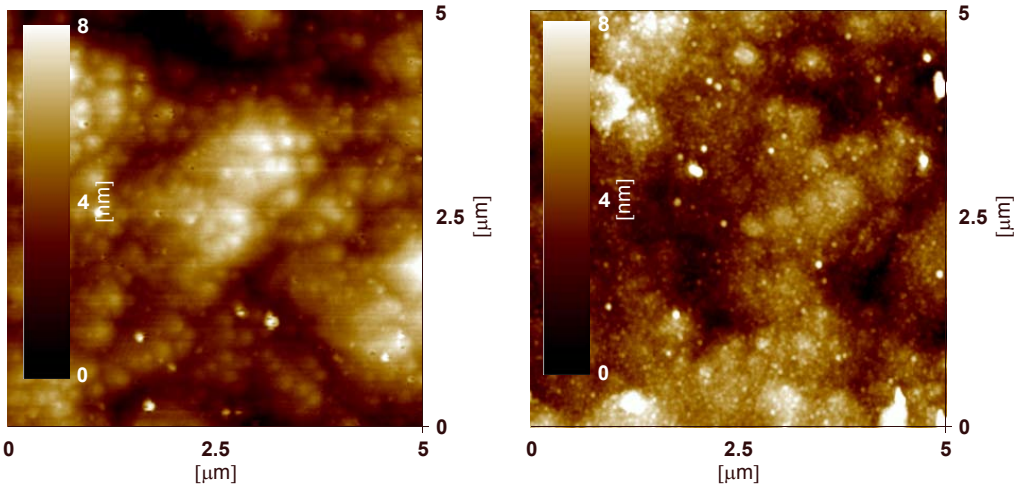


(a)



(b)

FIGURE 4.6: (a) C-V characteristics of Al_2O_3/AlN/GaN circular test MOS structures with diameter of 90 μm. Trace with circular data markers is for gate voltage sweep of -5 V to +0.5 V; trace with square data markers is for reverse measurement, +0.5 V to -5 V, and (b) Gate leakage current characteristics.



(a) (b)

FIGURE 4.7: AFM measurement of the surface roughness (a) as-grown AlN/-GaN HEMT, (b) after thermal growth of Al_2O_3 on AlN/GaN MOS-HEMT.

4.2.4.2 AlN/GaN MOS-HEMTs

Typical I_{DS}-V_{DS} characteristics of the fabricated $3\,\mu\text{m} \times 100\,\mu\text{m}$ gate AlN/GaN MOS-HEMT devices for two different etching times prior to Ohmic metallisation are shown in Fig. 4.8. It is clear that a 20 secs Al etch has a significant impact on the device performance with the drain current at zero gate voltage (I_{DSS}) more than double that of a device in which the etching time was 10 secs, corroborating the TLM results given earlier in Fig. 3.13(a).

Summary of $I_{DS,max}$ and $G_{m,max}$ of gate wrap-around AlN/GaN MOS-HEMT devices for these two different etching times prior to Ohmic metallisation are tabulated in Tables 4.1 and 4.2. The measured drain current and the transconductance characteristics of the devices were observed to decrease for the larger gate width devices. This is attributed to more pronounced self-heating effects in the wider devices. The variation in device performance on a sample was under 10 %, indicates good wafer uniformity.

The devices (using optimised processes) exhibited excellent DC characteristics and so based on this, the process was extended to realise RF devices employing mesa isolation and thermally grown Al_2O_3 passivation.

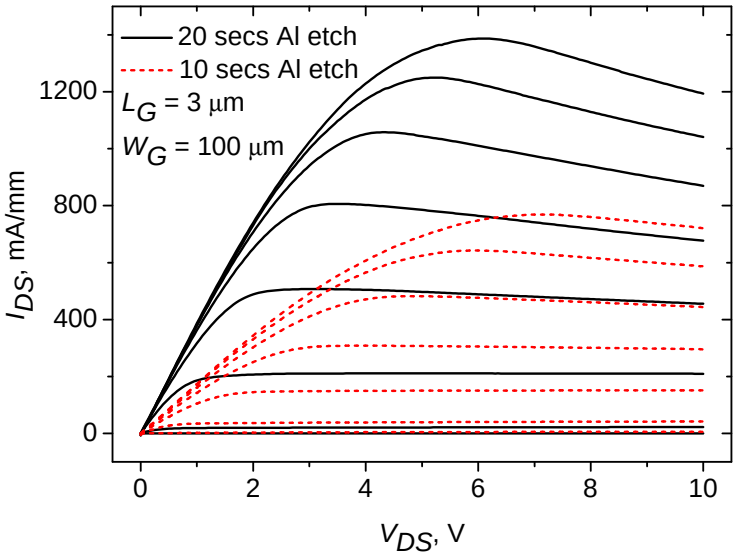


FIGURE 4.8: I_{DS}-V_{DS} characteristics of fabricated AlN/GaN MOS-HEMT devices with different etching times using the simplified gate wrap-around method. The devices are biased from $V_{GS} = +3$ V to -4 V with step size of 1 V.

4.3 Mesa AlN/GaN MOS-HEMT Optimisation

To be able to realise the full potential of AlN/GaN MOS-HEMTs technology for high power and high frequency applications, RF characteristics have to be examined. Hence, the next step towards the realisation of this technology was to design an appropriate device layout using conventional HEMT processing employing the mesa isolation step. In this section, process development and device characteristics for both the large (3 μm gate length) and small (0.2 μm and 0.5 μm gate lengths) two-finger AlN/GaN MOS-HEMT devices are presented and discussed. A summary of the completed optimised processes for both large and small two-finger devices is given in Appendix A.

4.3.1 DC Characteristics

Initially, RF devices with longer gate length, 3 μm, were fabricated using optical lithography to produce fast feedback for process development and optimisation on

TABLE 4.1: Summary of $I_{DS,max}$ and $G_{m,max}$ of gate wrap-around AlN/GaN MOS-HEMTs with different gate width sizes. All devices are etched for 10 secs prior to Al thermal oxidation. The measured $I_{DS,max}$ values are biased at $V_{GS} = +3$ V, while $G_{m,max}$ values are biased at $V_{DS} = +4$ V.

	L_G, W_G, μm	$I_{DS,max}$, mA/mm	$G_{m,max}$, mS/mm
	3, 100	$I_{DS,max1} = 818.6$ $I_{DS,max2} = 703.5$ $I_{DS,max3} = 785.5$ $I_{DS,max4} = 768.9$	$G_{m,max1} = 127.7$ $G_{m,max2} = 105.9$ $G_{m,max3} = 121.6$ $G_{m,max4} = 119.3$
		SD	SD %
$I_{DS,max}$(ave)	769.1	48.4	6.3
$G_{m,max}$(ave)	118.6	9.2	7.8
	3, 200	$I_{DS,max1} = 759.9$ $I_{DS,max2} = 713.6$ $I_{DS,max3} = 721.1$ $I_{DS,max4} = 700.2$	$G_{m,max1} = 116.8$ $G_{m,max2} = 108.9$ $G_{m,max3} = 111.5$ $G_{m,max4} = 101.2$
		SD	SD %
$I_{DS,max}$(ave)	723.7	25.6	3.5
$G_{m,max}$(ave)	109.6	6.5	5.9
	3, 300	$I_{DS,max1} = 709.5$ $I_{DS,max2} = 702.2$ $I_{DS,max3} = 683.9$ $I_{DS,max4} = 714.4$	$G_{m,max1} = 109.4$ $G_{m,max2} = 104.3$ $G_{m,max3} = 99.5$ $G_{m,max4} = 110.0$
		SD	SD %
$I_{DS,max}$(ave)	702.5	26.8	3.8
$G_{m,max}$(ave)	105.8	4.9	4.6
	3, 400	$I_{DS,max1} = 688.4$ $I_{DS,max2} = 672.2$ $I_{DS,max3} = 659.1$ $I_{DS,max4} = 626.5$	$G_{m,max1} = 101.9$ $G_{m,max2} = 96.0$ $G_{m,max3} = 92.7$ $G_{m,max4} = 89.8$
		SD	SD %
$I_{DS,max}$(ave)	661.6	26.3	4.0
$G_{m,max}$(ave)	95.1	5.2	5.5

AlN/GaN MOS-HEMTs. These devices were fabricated without the mesa sidewall protection, see Fig. 4.11 - Device process (a). The processing includes:

i. Mesa etch for device isolation

TABLE 4.2: Summary of $I_{DS,max}$ and $G_{m,max}$ of gate wrap-around AlN/GaN MOS-HEMTs with different gate width sizes. All devices are etched for 20 secs prior to Al thermal oxidation. The measured $I_{DS,max}$ values are biased at $V_{GS} = +3$ V, while $G_{m,max}$ values are biased at $V_{DS} = +4$ V.

	L_G, W_G, μm	$I_{DS,max}$, mA/mm	$G_{m,max}$, mS/mm
	3, 100	$I_{DS,max1} = 1321.2$ $I_{DS,max2} = 1359.3$ $I_{DS,max3} = 1182.5$ $I_{DS,max4} = 1387.2$	$G_{m,max1} = 285.8$ $G_{m,max2} = 297.3$ $G_{m,max3} = 293.3$ $G_{m,max4} = 308.4$
		SD	SD %
$I_{DS,max}$(ave)	1312.6	90.8	6.9
$G_{m,max}$(ave)	296.2	9.4	3.2
	3, 200	$I_{DS,max1} = 1026.7$ $I_{DS,max2} = 1052.8$ $I_{DS,max3} = 1074.6$ $I_{DS,max4} = 1070.2$	$G_{m,max1} = 236.2$ $G_{m,max2} = 245.2$ $G_{m,max3} = 251.7$ $G_{m,max4} = 251.3$
		SD	SD %
$I_{DS,max}$(ave)	1056.1	21.7	2.1
$G_{m,max}$(ave)	246.1	7.2	2.9
	3, 300	$I_{DS,max1} = 958.9$ $I_{DS,max2} = 941.8$ $I_{DS,max3} = 958.4$ $I_{DS,max4} = 914.9$	$G_{m,max1} = 234.7$ $G_{m,max2} = 225.8$ $G_{m,max3} = 234.6$ $G_{m,max4} = 217.9$
		SD	SD %
$I_{DS,max}$(ave)	943.5	20.7	2.2
$G_{m,max}$(ave)	228.3	8.1	3.5
	3, 400	$I_{DS,max1} = 861.6$ $I_{DS,max2} = 787.4$ $I_{DS,max3} = 869.7$ $I_{DS,max4} = 879.1$	$G_{m,max1} = 213.5$ $G_{m,max2} = 185.6$ $G_{m,max3} = 204.4$ $G_{m,max4} = 216.7$
		SD	SD %
$I_{DS,max}$(ave)	849.5	42.0	4.9
$G_{m,max}$(ave)	205.05	14.0	6.8

ii. Etch Ohmic regions and thermal oxidation of Al

iii. Ohmic metallisation and annealing, followed by gate metallisation

iv. Bondpad metal i.e. NiCr/Au, deposition

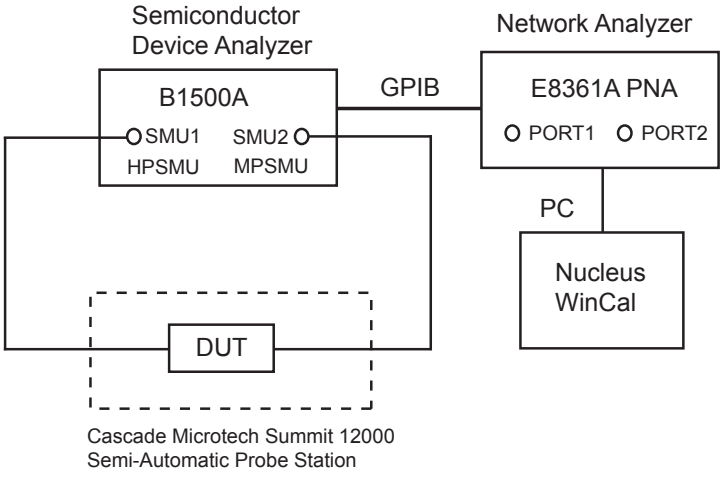


FIGURE 4.9: DC and RF measurement set-up.

An un-optimised Ohmic contact process was employed during the device fabrication. The aluminium etch was done for only 10 secs prior to Ohmic contacts metallisation [82].

On-wafer DC characterisation is performed by using the measurement set-up as illustrated in Fig. 4.9. The set-up also includes with the E8361A PNA network analyzer for RF measurements. It consists of a B1500A semiconductor device analyzer and a Cascade Microtech summit 12000 semi-automatic probe station. DC biases are provided by Agilent's B1500A, which runs Agilent EasyEXPERT measurement software. The device is connected to the semiconductor device analyzer with ground-signal-ground (GSG) RF probes. DC measurements include the output characteristics I_{DS} - V_{DS}, the gate leakage characteristic I_{GS} - V_{DS} and the transconductance characteristic G_m - V_{GS}. These are basic DC performances of the devices and provide fast feedback after the fabrication of the devices.

Fig. 4.12(a) shows I_{DS}-V_{DS} characteristics for both unprotected and protected mesa sidewall devices. The device with unprotected mesa sidewall exhibited high knee voltages (high Ohmic contact resistance) and did not fully pinch-off. The reason for the high leakage currents seemed to be the contact between the gate metal and the exposed mesa sidewalls. Devices were therefore insulated with an additional layer of thermally grown Al_2O_3 on the mesa sidewall edge as shown in Fig. 4.11 - Device process (b). The new processing includes:

i. Mesa etch for device isolation

ii. 2 nm Al deposition on mesa sidewall edge

iii. 2 nm of Al covers the sample surface

iv. Etch Ohmic regions and thermal oxidation of Al, then Ohmic metallisation and annealing, followed by gate metallisation

v. Bondpad metal i.e. NiCr/Au, deposition

The processing summary for both unprotected and protected RF AlN/GaN MOS-HEMTs are shown in Fig. 4.11. The leakage current at $V_{GS} = 4\,\text{V}$ and $V_{DS} = 10\,\text{V}$ was 0.3 mA/mm and 0.06 mA/mm for unprotected and protected devices, respectively. The protected device suppresses the leakage current by about one order of magnitude better as compared to devices without mesa sidewall protection as shown in Fig. 4.12(b). Summary of $I_{DS,max}$ and $G_{m,max}$ for both unprotected and protected RF AlN/GaN MOS-HEMT devices are tabulated in Tables 4.3 and 4.4. Good uniformity (i.e. under 10 % of variations) were also observed for both unprotected and protected RF AlN/GaN MOS-HEMT devices across the samples.

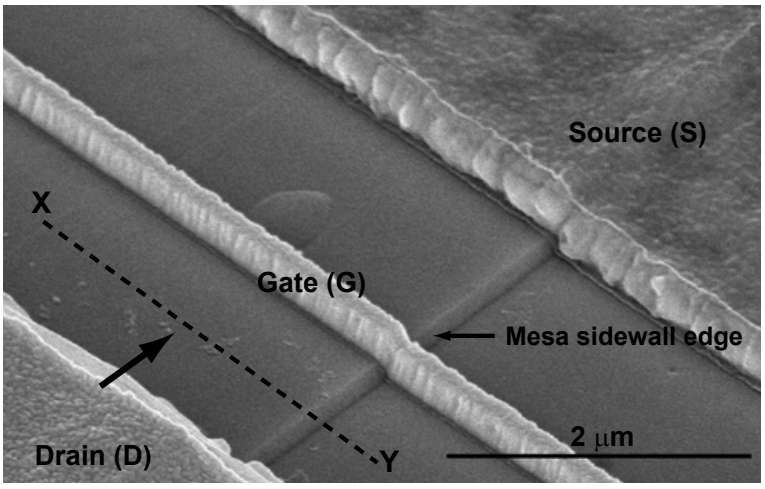


FIGURE 4.10: Top-view SEM micrograph of completed device with mesa sidewall edge. Device with vertical gate structure and the gate length is 0.2 μm.

Devices with a shorter gate length of 0.2 μm and 0.5 μm with different gate widths, 100 μm and 200 μm, were also fabricated using the process with mesa sidewall

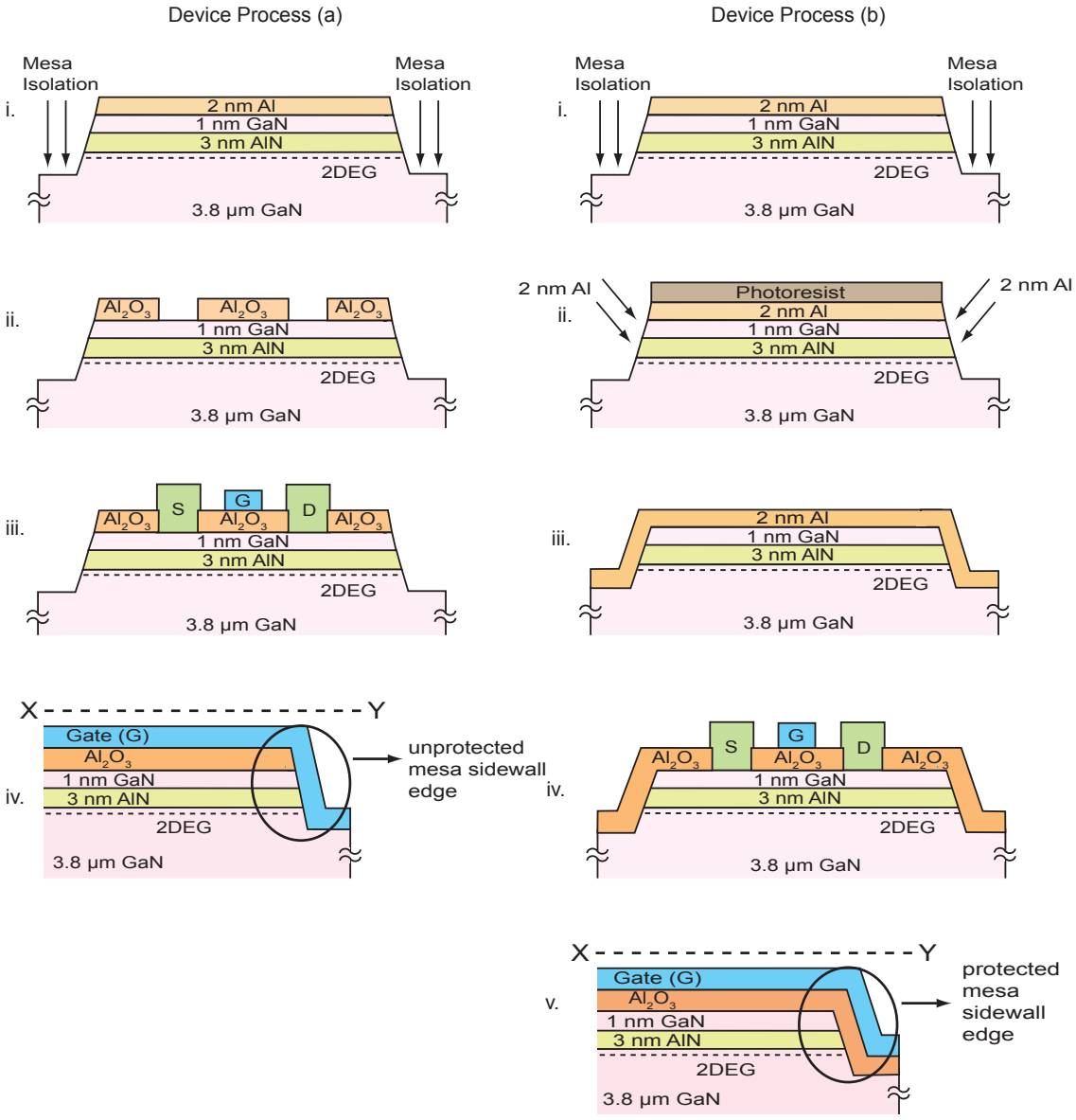
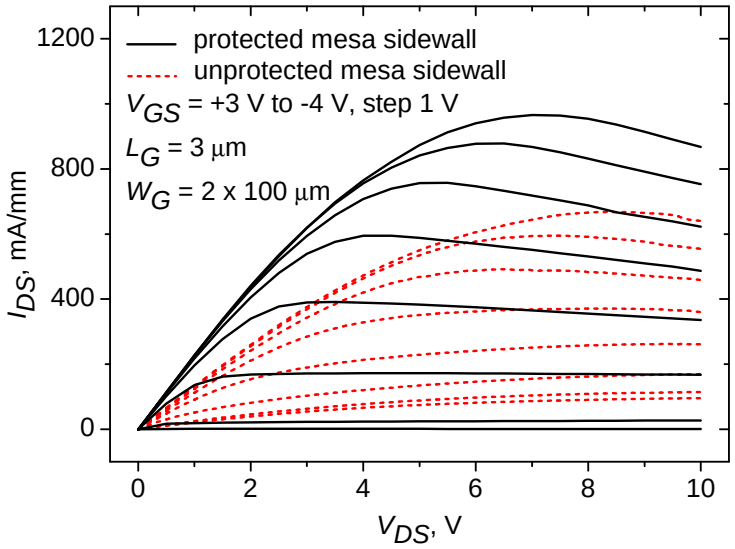
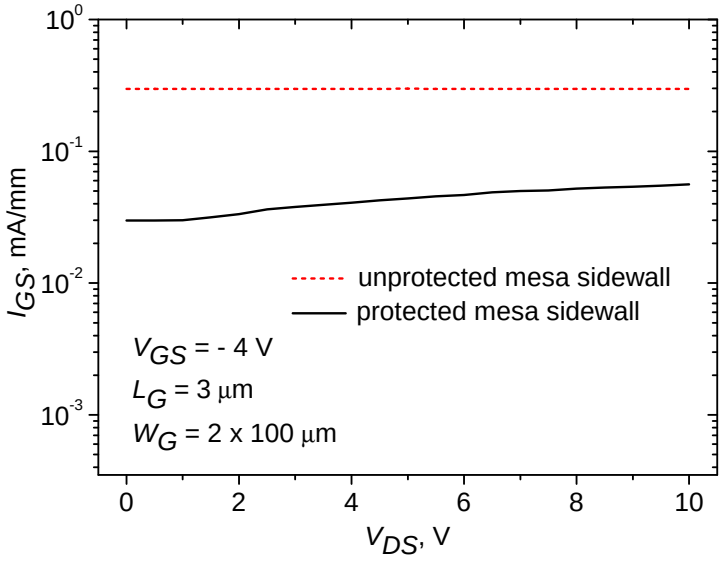


FIGURE 4.11: Process flow for fabrication of protected RF AlN/GaN MOS-HEMTs. Device process (a):(i) Mesa etch for device isolation, (ii) Etch Ohmic regions and thermal oxidation of Al, (iii) Ohmic metallisation and annealing, followed by gate metallisation, and (iv) Cross-section of completed device with unprotected mesa sidewall edge. Device process (b):(i) Mesa etch for device isolation, (ii) 2 nm Al deposition on mesa sidewall edge, (iii) 2 nm of Al covers the sample surface, (iv) Etch Ohmic regions and thermal oxidation of Al, then Ohmic metallisation and annealing, followed by gate metallisation, and (v) Cross-section (X-Y) of completed device with protected mesa sidewall edge (picture from completed device shows in Fig. 4.10).

protection. Ohmic and gate contacts steps were defined using e-beam lithography for patterning accuracy. The bilayer PMMA liftoff process was used for both Ohmic and gate metallisation (the detailed process was given earlier in Section 2.7).



(a)



(b)

FIGURE 4.12: (a) I_{DS} - V_{DS} characteristics of fabricated two-finger 3 μm gate length AlN/GaN MOS-HEMT devices with unprotected mesa sidewall and unoptimised etching time (10 secs). Also shown is a device with protected mesa sidewall and with an optimised etching time (20 secs). The devices are biased from V_{GS} = +3 V to -4 V with step size of 1 V, and (b) Measured leakage current of unprotected and protected devices.

All other fabrication steps were defined using optical lithography. To simplify the

TABLE 4.3: Summary of $I_{DS,max}$ and $G_{m,max}$ of unprotected mesa sidewall RF AlN/GaN MOS-HEMT devices with different gate width sizes. All devices are etched for 10 secs prior to Al thermal oxidation. The measured $I_{DS,max}$ values are biased at $V_{GS} = +3$ V, while $G_{m,max}$ values are biased at $V_{DS} = +4$ V.

	L_G, W_G, μm	$I_{DS,max}$, mA/mm	$G_{m,max}$, mS/mm
	3, 2 x 100	$I_{DS,max1} = 667.9$ $I_{DS,max2} = 621.3$ $I_{DS,max3} = 556.6$ $I_{DS,max4} = 587.2$	$G_{m,max1} = 145.1$ $G_{m,max2} = 139.8$ $G_{m,max3} = 134.2$ $G_{m,max4} = 137.6$
		SD	SD %
$I_{DS,max}$(ave)	608.3	47.7	7.8
$G_{m,max}$(ave)	139.2	4.6	3.3
	3, 2 x 200	$I_{DS,max1} = 504.1$ $I_{DS,max2} = 483.1$ $I_{DS,max3} = 464.6$ $I_{DS,max4} = 452.8$	$G_{m,max1} = 122.6$ $G_{m,max2} = 111.3$ $G_{m,max3} = 107.6$ $G_{m,max4} = 102.3$
		SD	SD %
$I_{DS,max}$(ave)	476.2	22.4	4.7
$G_{m,max}$(ave)	111.0	8.6	7.8

processing steps for shorter RF devices, a vertical gate structure was employed for fabrication two-finger AlN/GaN MOS-HEMTs as shown in Fig. 4.10. Fig. 4.13 shows a SEM micrograph of completed two-finger gate AlN/GaN MOS-HEMT after the bondpad metallisation step.

From the TLM measurements of metal pads fabricated on the same sample, the average value of R_C and R_{sh} is 0.76 Ω.mm and ∼318 Ω/□, respectively. The value of R_{sh} is twice as compared to the previous work on Ohmic contact optimisation as described in Section 3.5.2 [83]. Based on this result, it seemed that the R_{sh} can vary depending on the device process steps used during the fabrication. More research is needed to investigate this problem.

Figs. 4.14 and 4.15 give a summary of typical I_{DS} - V_{DS} and G_m - V_{GS} characteristics of fabricated 0.2 μm and 0.5 μm gate length AlN/GaN MOS-HEMTs with gate width, W_G, of 100 μm and 200 μm respectively. All fabricated devices exhibit good gate control of drain currents up to a gate bias of +3 V. A maximum drain current

TABLE 4.4: Summary of $I_{DS,max}$ and $G_{m,max}$ of protected mesa sidewall RF AlN/GaN MOS-HEMT devices with different gate width sizes. All devices are etched for 20 secs prior to Al thermal oxidation. The measured $I_{DS,max}$ values are biased at $V_{GS} = +3\,\text{V}$, while $G_{m,max}$ values are biased at $V_{DS} = +4\,\text{V}$.

	L_G, W_G, μm	$I_{DS,max}$, mA/mm	$G_{m,max}$, mS/mm
	3, 2 x 100	$I_{DS,max1} = 753.3$ $I_{DS,max2} = 859.5$ $I_{DS,max3} = 925.3$ $I_{DS,max4} = 882.0$	$G_{m,max1} = 209.2$ $G_{m,max2} = 216.6$ $G_{m,max3} = 241.1$ $G_{m,max4} = 227.8$
		SD	SD %
$I_{DS,max}$(ave)	855.2	73.2	8.6
$G_{m,max}$(ave)	223.7	16.6	7.4
	3, 2 x 200	$I_{DS,max1} = 737.4$ $I_{DS,max2} = 766.1$ $I_{DS,max3} = 655.4$ $I_{DS,max4} = 689.9$	$G_{m,max1} = 178.9$ $G_{m,max2} = 207.4$ $G_{m,max3} = 169.3$ $G_{m,max4} = 183.3$
		SD	SD %
$I_{DS,max}$(ave)	712.2	49.2	6.9
$G_{m,max}$(ave)	184.7	16.2	8.8

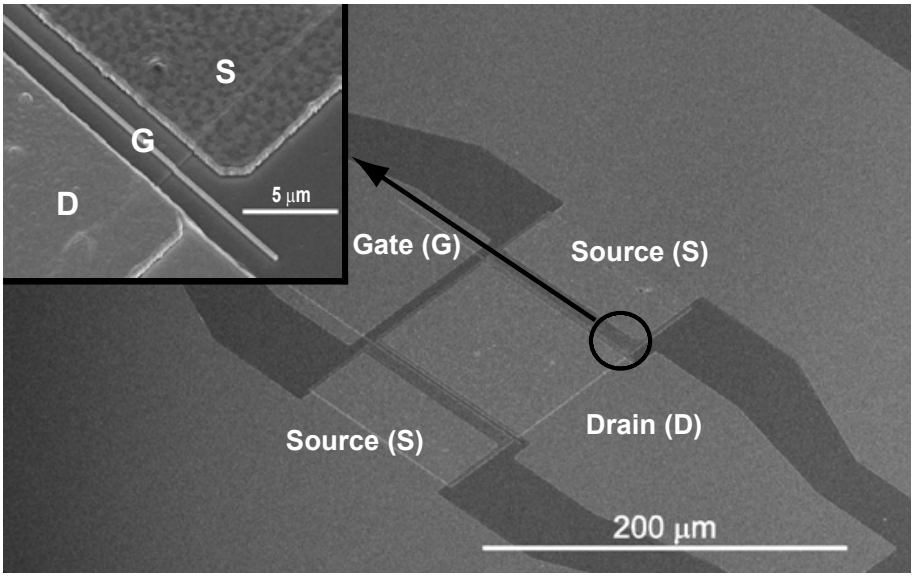


FIGURE 4.13: SEM micrograph of completed two-finger gate AlN/GaN MOS-HEMT layout. Inset: Device with $L_{SD} = 3.2\,\mu$m and $L_G = 0.2\,\mu$m.

of $1457.0 \pm 99.0\,\text{mA/mm}$ (or deviation of 7.4 %) and $1314.6 \pm 49.9\,\text{mA/mm}$ (or deviation of 7.1 %) was observed for $L_G = 0.2\,\mu$m and $L_G = 0.5\,\mu$m, respectively,

with gate width of 100 μm. However, the maximum drain current decreased to 1111.0 ± 60.7 mA/mm (or deviation of 5.9 %) and 1017.6 ± 41.9 mA/mm (or deviation of 4.3 %) for $L_G = 0.2\,\mu$m and $L_G = 0.5\,\mu$m, respectively, with gate width of 200 μm.

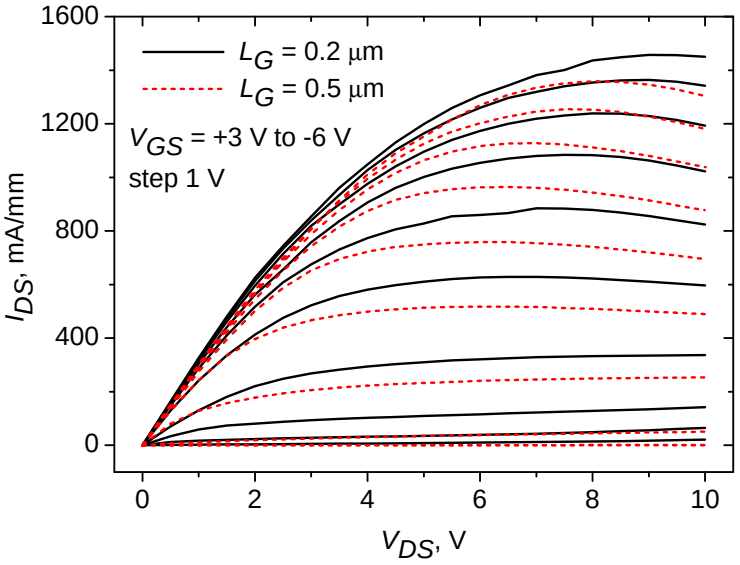
A maximum peak transconductance of 303.1 ± 22.0 mS/mm (or deviation of 7.9 %) and 268.4 ± 16.1 mS/mm (or deviation of 6.5 %) was measured for $L_G = 0.2\,\mu$m and $L_G = 0.5\,\mu$m with gate width of 100 μm. While for the larger gate width, 200 μm, the peak transconductance is decreased to 221.4 ± 6.0 mS/mm (or deviation of 2.8 %) and 215.1 ± 13.0 mS/mm (or deviation of 6.5 %) for $L_G = 0.2\,\mu$m and $L_G = 0.5\,\mu$m, respectively.

Good pinch-off and saturation characteristics were also observed for measured devices. Note that the open channel currents (at $V_{GS} = 0$ V) for the gate width of 100 μm devices with $L_G = 0.2\,\mu$m and $L_G = 0.5\,\mu$m are 1084.0 ± 99.0 mA/mm (or deviation of 7.4 %) and 964.0 ± 49.9 mA/mm (or deviation of 7.1 %), respectively. Summary of $I_{DS,max}$ and $G_{m,max}$ of sub-micron RF AlN/GaN MOS-HEMT devices are tabulated in Table 4.5.

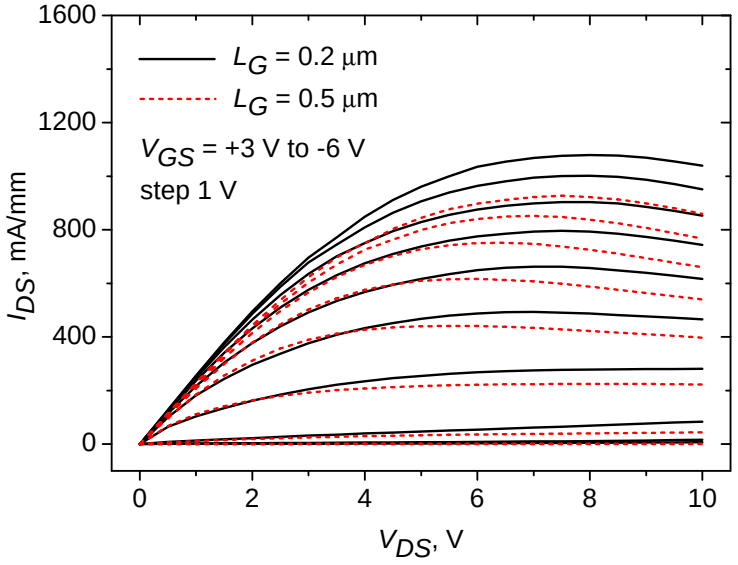
AlGaN/GaN MOS-HEMTs were also fabricated using the optimised process in Fig. 4.11 - Device process (b). Fig. 4.16 gives a summary of I_{DS}-V_{DS} and G_m-V_{GS} characteristics of fabricated 0.2 μm and 0.5 μm gate length AlGaN/GaN MOS-HEMTs with gate width, W_G, of 200 μm. All fabricated devices exhibit good gate control of drain currents up to a gate bias of +2 V. Summary of $I_{DS,max}$ and $G_{m,max}$ of sub-micron RF AlGaN/GaN MOS-HEMT devices are tabulated in Table 4.6.

Clearly from Figs. 4.14(b),4.16(a),4.15(b) and 4.16(b), the measured drain current and the transconductance characteristics of AlGaN/GaN devices were lower than AlN/GaN devices.

For AlGaN/GaN devices, the open channel currents (at $V_{GS} = 0$ V) for the gate width of 200 μm devices with $L_G = 0.2\,\mu$m and $L_G = 0.5\,\mu$m were 605.3 ± 56.1-mA/mm (or deviation of 7.0 %) and 521.9 ± 55.9 mA/mm (or deviation of 8.2 %), respectively (Fig. 4.16(a)). While for AlN/GaN devices, the open channel currents



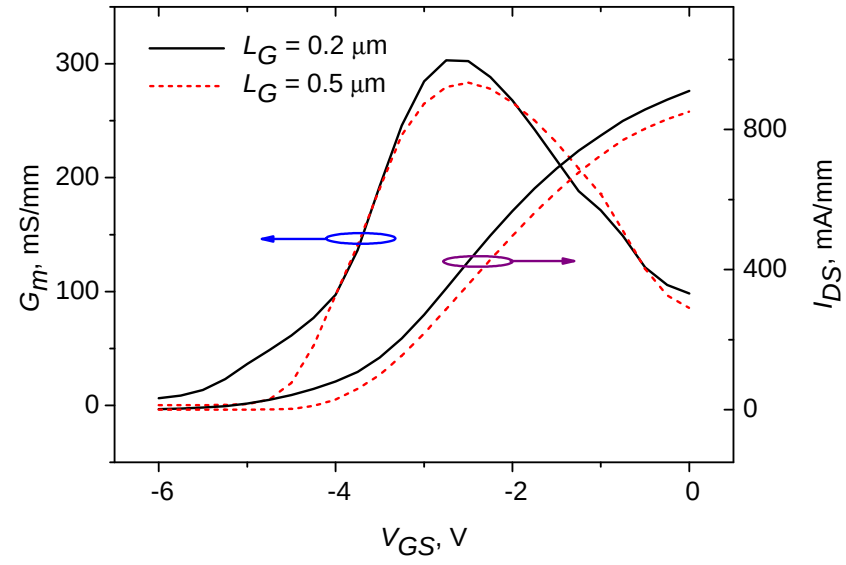
(a)



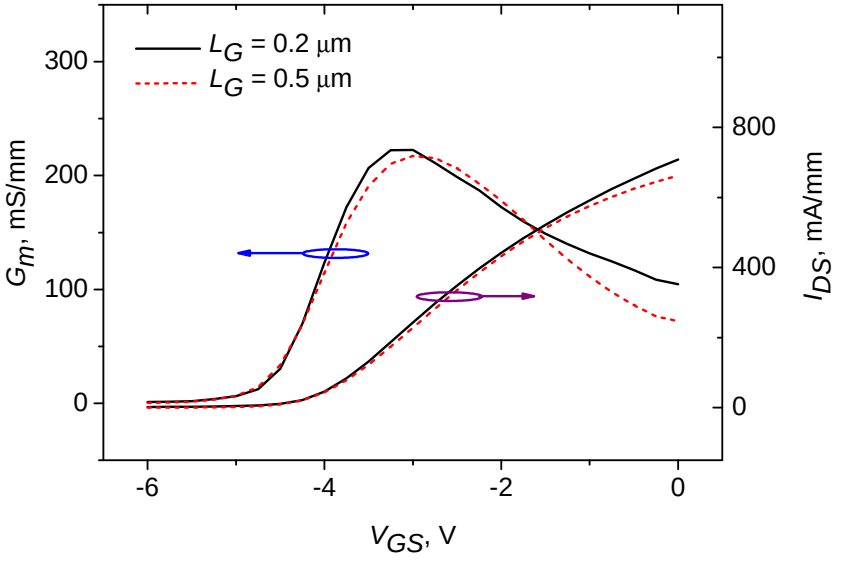
(b)

FIGURE 4.14: Summary of I_{DS} against V_{DS} characteristics of fabricated 0.2 μm and 0.5 μm gate length AlN/GaN MOS-HEMT with different gate width sizes. (a) $W_G = 100\,\mu$m, and (b) $W_G = 200\,\mu$m.

were 795.7 ± 60.7 mA/mm (or deviation of 5.9 %) and 751.8 ± 41.9 mA/mm (or deviation of 4.3 %) for $L_G = 0.2\,\mu$m and $L_G = 0.5\,\mu$m, respectively (Fig. 4.14(b)). The higher current in AlN/GaN MOS-HEMTs is attributed to its higher $n_s\mu$ product



(a)



(b)

FIGURE 4.15: Summary of G_m against V_{GS} characteristics of fabricated 0.2 μm and 0.5 μm gate length AlN/GaN MOS-HEMT with different gate width sizes. (a) $W_G = 100\,\mu$m, and (b) $W_G = 200\,\mu$m at $V_{DS} = 4$ V.

(2.75×10^{16}/V.s) as compared to AlGaN/GaN MOS-HEMTs (1.57×10^{16}/V.s).

TABLE 4.5: Summary of $I_{DS,max}$ and $G_{m,max}$ of fabricated 0.5 μm and 0.2 μm gate length AlN/GaN MOS-HEMTs with different gate width sizes. All devices are etched for 20 secs prior to Al thermal oxidation. The measured $I_{DS,max}$ values are biased at $V_{GS} = +3$ V, while $G_{m,max}$ values are biased at $V_{DS} = +4$ V.

	L_G, W_G, μm	$I_{DS,max}$, mA/mm	$G_{m,max}$, mS/mm
	0.5, 2 x 100	$I_{DS,max1} = 1273.5$ $I_{DS,max2} = 1198.6$ $I_{DS,max3} = 1234.9$ $I_{DS,max4} = 1314.6$	$G_{m,max1} = 249.8$ $G_{m,max2} = 230.2$ $G_{m,max3} = 241.5$ $G_{m,max4} = 268.4$
		SD	SD %
$I_{DS,max}$(ave)	1255.4	49.9	7.1
$G_{m,max}$(ave)	247.5	16.1	6.5
	0.2, 2 x 100	$I_{DS,max1} = 1359.9$ $I_{DS,max2} = 1233.2$ $I_{DS,max3} = 1274.9$ $I_{DS,max4} = 1457.0$	$G_{m,max1} = 289.9$ $G_{m,max2} = 255.8$ $G_{m,max3} = 264.3$ $G_{m,max4} = 303.1$
		SD	SD %
$I_{DS,max}$(ave)	1331.3	99.0	7.4
$G_{m,max}$(ave)	278.3	22.0	7.9
	0.5, 2 x 200	$I_{DS,max1} = 976.9$ $I_{DS,max2} = 915.8$ $I_{DS,max3} = 964.0$ $I_{DS,max4} = 1017.6$	$G_{m,max1} = 201.1$ $G_{m,max2} = 183.5$ $G_{m,max3} = 198.2$ $G_{m,max4} = 215.1$
		SD	SD %
$I_{DS,max}$(ave)	968.6	41.9	4.3
$G_{m,max}$(ave)	199.5	13.0	6.5
	0.2, 2 x 200	$I_{DS,max1} = 1111.0$ $I_{DS,max2} = 972.1$ $I_{DS,max3} = 1036.9$ $I_{DS,max4} = 997.0$	$G_{m,max1} = 221.4$ $G_{m,max2} = 208.1$ $G_{m,max3} = 217.8$ $G_{m,max4} = 211.5$
		SD	SD %
$I_{DS,max}$(ave)	1029.3	60.7	5.9
$G_{m,max}$(ave)	214.7	6.0	2.8

The maximum peak transconductance of 174.5 ± 10.6 mS/mm (or deviation of 6.4 %) and 146.8 ± 8.2 mS/mm (or deviation of 5.9 %) for $L_G = 0.2$ μm and $L_G = 0.5$-μm, respectively, with 200 μm gate width of AlGaN/GaN devices (Fig. 4.16(b)). While for AlN/GaN devices, the peak transconductance was 221.4 ± 6.0 mS/mm

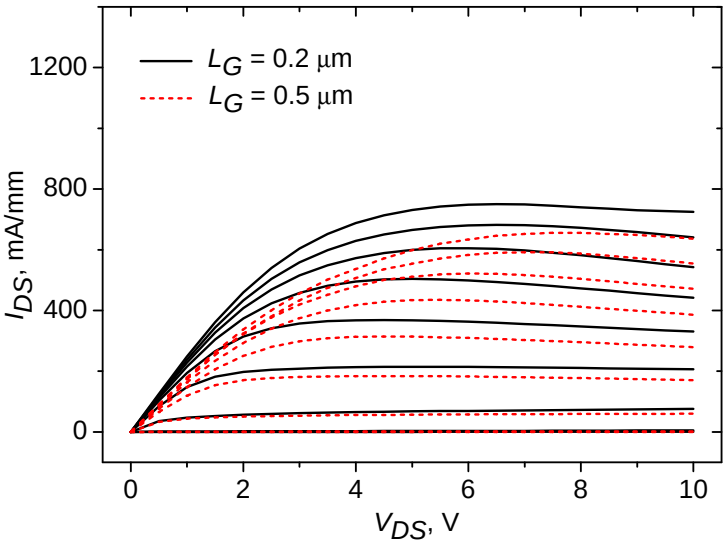
TABLE 4.6: Summary of $I_{DS,max}$ and $G_{m,max}$ of fabricated 0.5 μm and 0.2 μm gate length AlGaN/GaN MOS-HEMTs with different gate width sizes. All devices are etched for 20 secs prior to Al thermal oxidation. The measured $I_{DS,max}$ values are biased at $V_{GS} = +2$ V, while $G_{m,max}$ values are biased at $V_{DS} = +4$ V.

	L_G, W_G, μm	$I_{DS,max}$, mA/mm	$G_{m,max}$, mS/mm
	0.5, 2 x 200	$I_{DS,max1} = 738.8$ $I_{DS,max2} = 718.6$ $I_{DS,max3} = 657.2$ $I_{DS,max4} = 617.1$	$G_{m,max1} = 146.8$ $G_{m,max2} = 141.5$ $G_{m,max3} = 133.7$ $G_{m,max4} = 128.4$
		SD	SD %
$I_{DS,max}$(ave)	682.9	55.9	8.2
$G_{m,max}$(ave)	137.6	8.2	5.9
	0.2, 2 x 200	$I_{DS,max1} = 829.8$ $I_{DS,max2} = 755.4$ $I_{DS,max3} = 857.0$ $I_{DS,max4} = 741.9$	$G_{m,max1} = 171.8$ $G_{m,max2} = 159.7$ $G_{m,max3} = 174.5$ $G_{m,max4} = 151.9$
		SD	SD %
$I_{DS,max}$(ave)	796.0	56.1	7.0
$G_{m,max}$(ave)	164.5	10.6	6.4

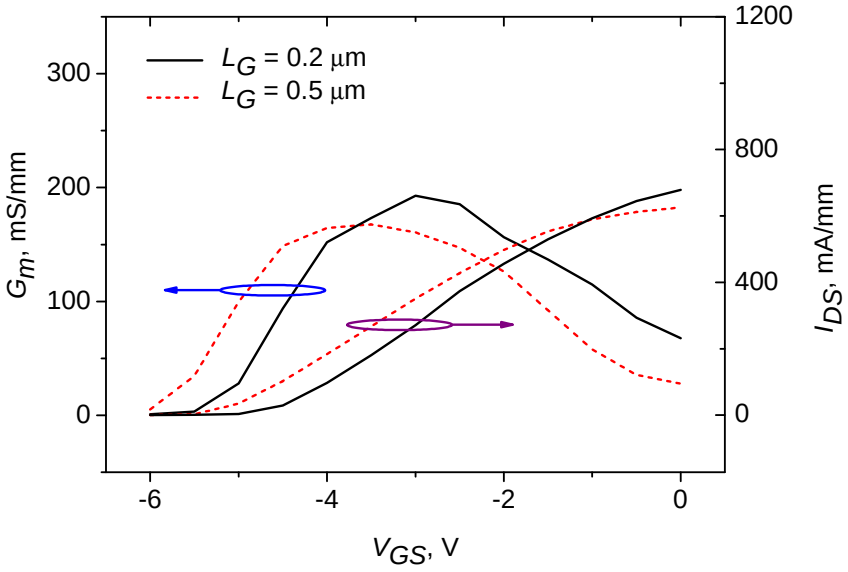
(or deviation of 2.8 %) and 215.1 ± 13.0 mA/mm (or deviation of 6.5 %) for $L_G = 0.2$-μm and $L_G = 0.5\,\mu$m, respectively (Fig. 4.15(b)). The higher transconductance in AlN/GaN MOS-HEMTs is attributed to shorter distance between the gate to the channel (i.e. thinner barrier layer) as compared to AlGaN/GaN MOS-HEMTs.

4.3.2 Pulse Characteristics

In DC measurements, IV characteristics are measured by increasing the drain source voltage from zero to the maximum value for each of gate source voltage. For pulse IV measurements, the gate and drain terminals are pulsed and the drain current is measured during the on-period of the pulse. The pulses are initiated from a static quiescent bias point, which can be chosen on the IV plane. The width of the drain pulse is smaller than that of the gate pulse. To prevent the flow of excessive drain current, the drain pulse is applied after the gate pulse. Provided



(a)



(b)

FIGURE 4.16: Fabricated 0.2 μm and 0.5 μm gate length AlGaN/GaN MOS-HEMT with gate width of $W_G = 200\,\mu$m. (a) I_{DS} against V_{DS} characteristics with gate bias from +2 V to -6 V (step size of 1 V) and (b) G_m against V_{GS} characteristics at $V_{DS} = 4$ V.

the applied pulse width is short and the pulse period to be long, the effects of device self-heating can be minimised. The ratio between the pulse width and the pulse period is called duty cycle.

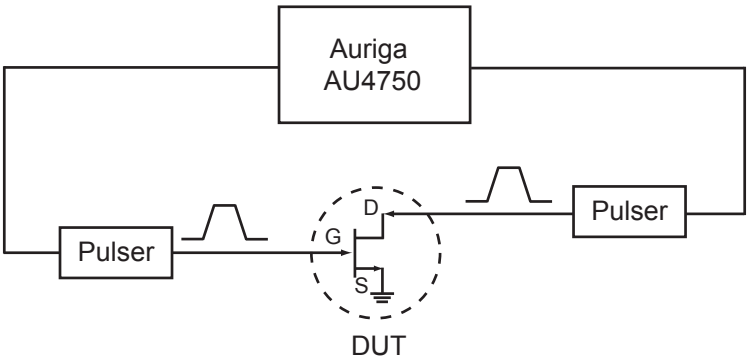


FIGURE 4.17: Pulsed IV measurement set-up.

Pulse IV measurements were carried out at NXP Semiconductors, Amsterdam, to investigate self-heating as well as trapping effects in the devices. The Auriga AU4550 Pulsed IV measurement system was used. It is an integrated system that can deliver pulses up to 200 V and 600 W. Pulse heads are easily interchangeable and have different power rating to suit the device size. Pulse traces can be viewed live for the all pulses, that is V_{GS}, I_{GS}, V_{DS} and I_{DS} during typical FET measurements. The pulse shapes are also affected by the measurement system that they feed, hence for a stable system an oscillation free setup is required [125]. The pulsed IV measurement set-up is illustrated in Fig. 4.17.

In this measurements, two pulses are used, one at the gate and one at the drain; pulses are synchronized and measurements done using two different pulse widths, 1 μs and 200 ns, with duty cycle of 0.1 %. When performing a pulsed IV measurement, each set of IV curves is generated by pulsing voltages away from a quiescent bias point. The quiescent bias point, consisting of the drain and gate voltages, will determine the type of electric field state is present in the HEMT in between pulses.

Fig. 4.18(a) shows the pulse IV characteristics of a two-finger 0.5 μm gate length AlN/GaN MOS-HEMT with different pulse width conditions at a zero electric field quiescent bias point ($V_{GS} = 0$, $V_{DS} = 0$). Self-heating effects were observed during the 1 μs pulses and were suppressed by shortening the pulse width to 200 ns. However, the currents were observed to decrease for the shorter pulse width. More

research is required in order to investigate this unknown behaviour of AlN/GaN MOS-HEMTs.

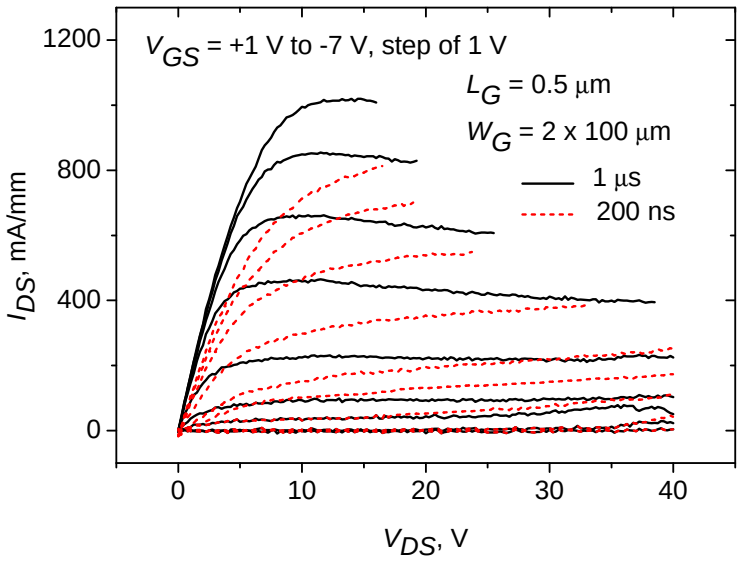
In contrast, an AlGaN/GaN MOS-HEMT showed an increase of 5 % in drain current when the pulse width was shortened from 1 μs to 200 ns as shown in Fig. 4.18(b). This is attributed to suppression of self-heating effect which results in improvement in current density.

4.3.3 Breakdown Voltage Characteristics

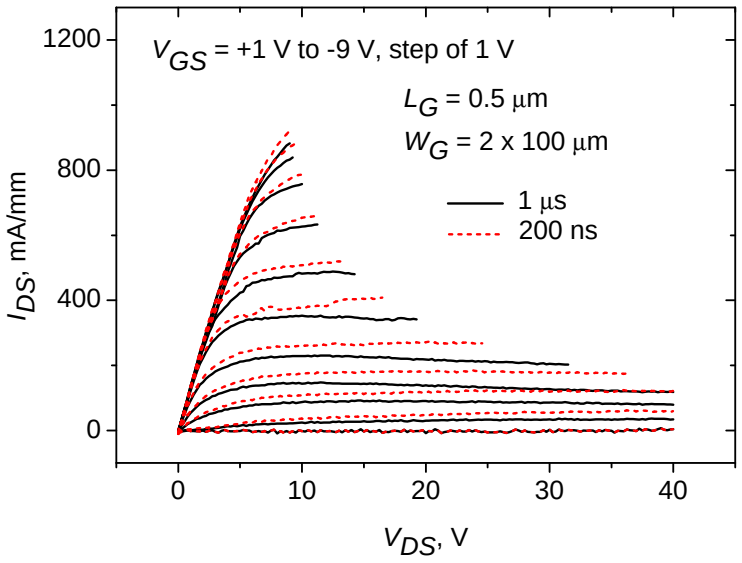
One of the most important features for GaN-based devices is its breakdown voltage. Several off-state breakdown mechanisms have been proposed and discussed for AlGaN/GaN HEMTs. In general, impact ionisation near the gate edge on the drain side (high-field region) of the channel is regarded as source that results in the off-state breakdown in AlGaN/GaN HEMTs [126] ,[127]. Ohno et al [128] reported that the breakdown mechanism was caused by the impact ionization in the channel which was triggered by electrons tunneling from the gate to the channel at a large gate-reverse bias. Nakao et al [129] and Kim et al [130] proposed that the gate leakage current injection was the source of electrons/carriers which initiate the impact ionization process.

For Schottky HEMTs with large reverse gate current, the gate leakage current injection through the Schottky gate leads to premature the off-state breakdown. Techniques such as post-gate annealing [130] and thermal oxidation treatment [131] were employed to suppress the gate leakage, resulting in remarkable improvement in the breakdown performance. This may also explain the reason why the MOS-HEMT and/or MIS-HEMT structures have higher breakdown voltage as compared to Schottky HEMT structures. In the case of MOS-HEMT structures, the gate leakage which contributes to the drain breakdown is suppressed by the insertion of this oxide layer, thus enhancing the breakdown performances [132].

The mechanism of off-state breakdown mechanism in AlGaN/GaN HEMTs can be described as follows: (1) leakage electrons tunnel from the gate metal to the



(a)



(b)

FIGURE 4.18: Pulse I-V characteristics of two-finger (a) AlN/GaN MOS-HEMT and (b) AlGaN/GaN MOS-HEMT (quiescent bias point: $V_{DS} = 0\,V$, $V_{GS} = 0\,V$).

channel, (2) with increasing positive drain bias, more and more electron and holes pairs are generated by the impact ionization avalanche, resulting in an abrupt increase in the drain current triggered by the injected electrons and finally leading

to device breakdown. Xie et al [133] proposed that the abrupt increase of the gate to drain leakage suggests that an irreversible electron current was developed from the gate directly to the 2DEG region after onset of device degradation. The relatively high current flowing through the gate metal may have caused the thermal damage of the device. The off-state breakdown voltage of GaN-based HEMTs is determined by the sub-threshold drain current of 1 mA/mm.

To alleviate the electric field crowding at the drain-side of the gate edge and to increase the breakdown voltage, overlapping gate/field plate structures which are effective in modulating the electric field distribution along a channel are widely used [52].

In this project, the off-state breakdown was carried out using the Auriga's AU4550 Pulsed IV measurement system. The off-state breakdown voltage characteristics are shown in Fig. 4.19, measured at gate voltage V_{GS} of -9 V. The breakdown voltage, V_{BR}, of a two-finger MOS-HEMT with 0.5 μm gate length was 58 V. When the voltage approaches breakdown, the leakage current increases rapidly and it is therefore destructive for the device. More research is required to ivestigate the mechanism of off-state breakdown for this material.

Fig. 4.20 shows the SEM micrograph of AlN/GaN MOS-HEMT before and after the breakdown measurements. The gate to drain distance of the device was 1.5 μm, resulting in an associated electric field of 38.7 V/μm (387 kV/cm).

Further improvement in V_{BR} can be achieved by (1) employing field plate structure, (2) optimising the thickness of the insulator used for the field plate, (3) optimising the gate to drain distance as well as the field plate length, and (4) employing an insulator which has high dielectric constant. According to works by Karmalkar et al [134] using 2-D simulation in ATLAS, all these parameters should be optimised in order to achieved maximum V_{BR} while minimise degradation in frequency response and on-resistance of GaN-based HEMTs when employing field plate.

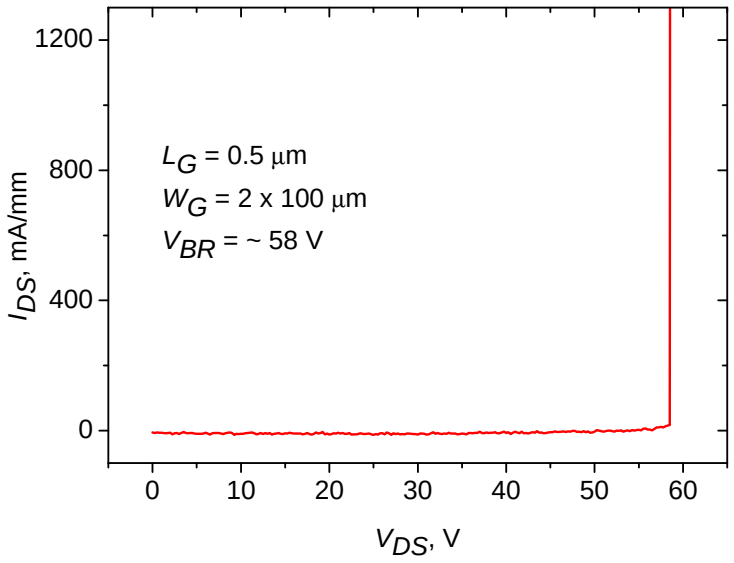


FIGURE 4.19: Off-state breakdown voltage characteristics of two-finger AlN/-GaN MOS-HEMT

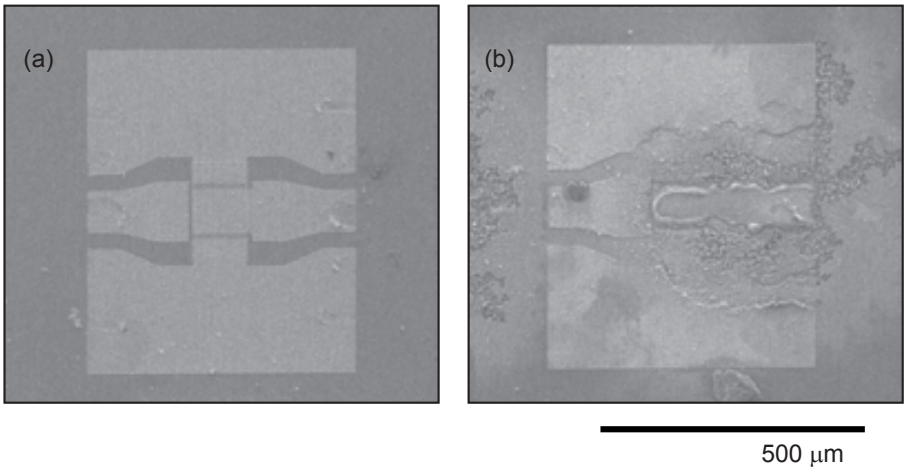


FIGURE 4.20: AlN/GaN MOS-HEMT (a) before and (b) after the breakdown measurement.

4.3.4 RF Characteristics

The small-signal characterisation of transistors is carried out by measuring the small-signal S-parameters measured at their input and output terminals (ports) while considering the actual component as a "black box". The scattering-parameters

(S-parameters) [135] are widely used for the characterisation of transistors at microwave frequencies because S-parameters can easily be determined from the measured ratios of the incident (a_i) and reflected (b_i) power waves using a network analyzer.

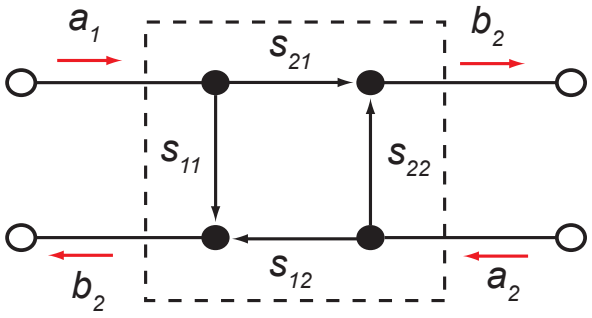


FIGURE 4.21: Graph representation of a two-port component showing the relations between the incident (a_i) and reflected (b_i) power waves and the individual S-parameters.

Fig. 4.21 shows these power waves and the individual S-parameters in the case of a two-port component, e.g. a transistor where the gate-source and the drain-source terminals are considered as the input and output ports, respectively. The relations between the input and the output of the two-port can be represented as

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

where the S-parameters S_{11}, S_{12}, S_{21}, and S_{22}, represent reflection and transmission coefficients. The measurement of these coefficients only requires termination of the DUT with the characteristic impedance of the measurement system, which is equal to $50\,\Omega$. The additional advantage of terminating the DUTs with this characteristic impedance is that they are stable at microwave frequencies [136]. In order to perform accurate RF characterisation of on-wafer devices, the impedance standard substrate (ISS) provided by Cascade Microtech is used for calibration. This is to remove the effect of connecting cables, define the measurement reference plane to the probe tips and remove measurement errors from, for instance, coupling between the ports.

The short-open-load-thru (SOLT) calibration technique was used in this work, where the following structures were used: (a) an open circuit, where the probes are usually elevated in the air above the substrate ($\sim 200\,\mu$m), (b) a short circuit, where a vertical metallised line shorts the three probes together, (c) a load structure, which is matched to the $50\,\Omega$ characteristic impedance of the system, and (d) a thru structure, which is essentially a $50\,\Omega$ short line connecting the two probes directly and a line of a given length. Fig. 4.22 shows "on-wafer" a set of microstrip calibration standards for the SOLT technique. With a calibrated network analyzer, accurate and precise small-signal S-parameter measurements can be easily carried out.

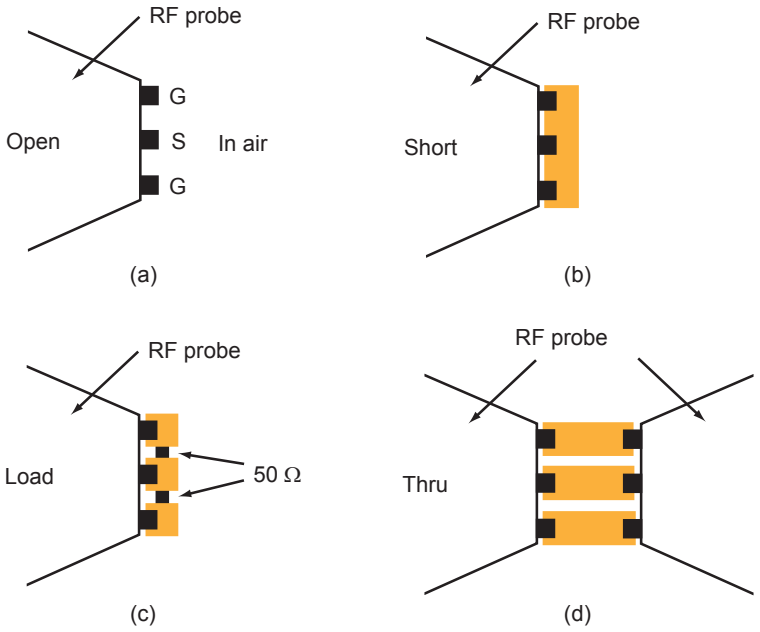


FIGURE 4.22: On-wafer calibration standards for the SOLT technique. (a) open, (b) short, (c) load, and (d) thru line.

All of the fabricated RF devices, long and short gate devices, were characterised on-wafer using GSG RF probes contacting the NiCr/Au bondpads. The configuration of the S-parameters measurements was shown in Fig. 4.9, and consists of a two-port E8361A PNA network analyzer, B1500A semiconductor device analyzer and Cascade Microtech Summit 12000 semi-automatic probe station. The system is connected to a control computer running Cascade Microtech Nucleus software.

This computer also runs the Cascade Microtech WinCal software which allows the configuration and management for small-signal S-parameters measurements.

At any given bias point and under small-signal conditions (at an input power of -20 dBm), the magnitude and phase of the S-parameters of a transistor are measured as a function of frequency. With this data, values for the unity current gain f_T, and the unity power gain frequency f_{MAX} can be determined. The frequency at which the magnitude of the current gain (h_{21}), which expressed in S-parameters is given by Eqn. 4.2 [137], equals one is defined as f_T, and the frequency at which Masons unilateral power gain (U), which expressed in S-parameters is given by Eqn. 4.3 [16], equals one is defined as f_{MAX}.

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \tag{4.2}$$

$$U = \frac{\left|\frac{S_{21}}{S_{12}}-1\right|^2}{2\left[K\left|\frac{S_{21}}{S_{12}}\right|-Re\left(\frac{S_{21}}{S_{12}}\right)\right]} \tag{4.3}$$

where K is the Rollet stability factor, which expressed in S-parameters, is given by Eqn. 4.4 [138]

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2\,|S_{12}S_{21}|} \tag{4.4}$$

where $\Delta = S_{11}S_{22}$ - $S_{12}S_{21}$, and can give an indication to whether a device is likely to oscillate or not or whether it is conditionally/unconditionally stable. The parameter must satisfy $K>1$ and $|\Delta|<1$ for a device to be unconditionally stable.

The small-signal RF performances of the AlN/GaN MOS-HEMTs for two-finger $3\,\mu m \times 100\,\mu m$ devices biased at $V_{DS} = 4$ V and $V_{GS} =$ -1 V exhibited a unity current-gain cut off frequency, f_T, and power gain cutoff frequency, f_{MAX}, of 2.8 and 7.9 GHz, respectively, as shown in Fig. 4.23 which is a good RF performance for these long gate devices. $K=1$ at approximately 2.3 GHz and $|\Delta|<1$ for all frequencies.

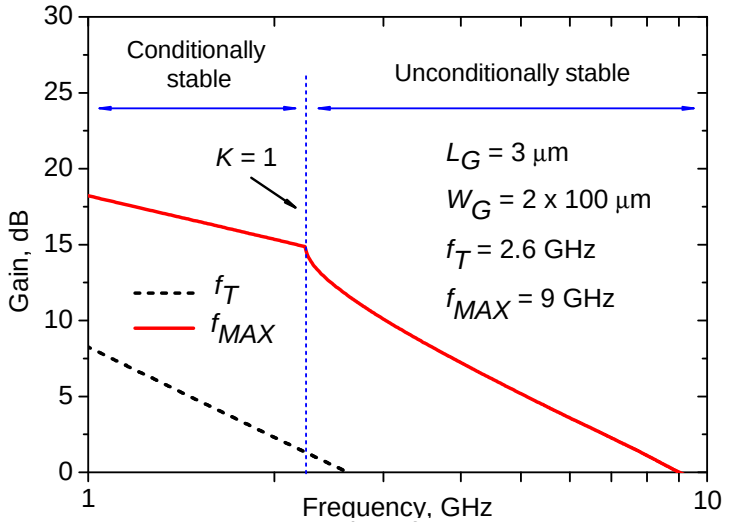


FIGURE 4.23: RF performance of two-finger $3 \times 100\,\mu$m AlN/GaN MOS-HEMT device at $V_{GS} = $-1 V and $V_{DS} = 4$ V.

For the shorter gate lengths, the small-signal RF performances of the AlN/GaN MOS-HEMTs for $W_G = 2 \times 100\,\mu$m and $W_G = 2 \times 200\,\mu$m are shown in Fig. 4.24. An improvement in RF performances is observed for smaller gate lengths although not much difference is observed in DC performances between $L_G = 0.2\,\mu$m and $L_G = 0.5\,\mu$m devices. For $W_G = 2 \times 100\,\mu$m, the average values of f_T are ~ 20 GHz and 50 GHz for $L_G = 0.5\,\mu$m and $L_G = 0.2\,\mu$m, respectively.

For $W_G = 2 \times 200\,\mu$m, the average values of f_T are ~ 19 GHz and 40 GHz for $L_G = 0.5\,\mu$m and $L_G = 0.2\,\mu$m, respectively. The f_{MAX} is 40 GHz and ~ 30 GHz for $L_G = 0.2\,\mu$m and $L_G = 0.5\,\mu$m with total gate width $200\,\mu$m. For the larger gate width, the average value of f_{MAX} is ~ 21 GHz for both gate lengths. The value of f_{MAX} should be higher for $L_G = 0.2\,\mu$m, however the reason for the similarity to $L_G = 0.5\,\mu$m is most probably due to processing errors on the smaller device. For $W_G = 2 \times 200\,\mu$m, $K = 1$ at approximately 4 GHz and 3.3 GHz for $L_G = 0.2\,\mu$m and $L_G = 0.5\,\mu$m, respectively. While for $W_G = 2 \times 100\,\mu$m, $K = 1$ at approximately 11 GHz and 9 GHz for $L_G = 0.2\,\mu$m and $L_G = 0.5\,\mu$m, respectively. $|\Delta| < 1$ for all frequencies for both devices. These RF results are far better than reported

in Ref. [78] for similar gate lengths. In Ref. [78], for fabricated T-Gate AlN/-GaN MOSHEMT device with $L_G = 0.15\,\mu$m, the average f_T and f_{MAX} were only 25 GHz and 22 GHz although the material was having excellent properties such as, $\mu > 1100\,\text{cm}^2/\text{V.s}$, $n_s > 3.25 \times 10^{13}\,\text{cm}^{-2}$, $R_{sh} < 165\,\Omega/\square$, and $R_C < 0.5\,\Omega.\text{mm}$. This indicates that there is still some issues related to this material that prevents the device from reaching record-breaking device performance.

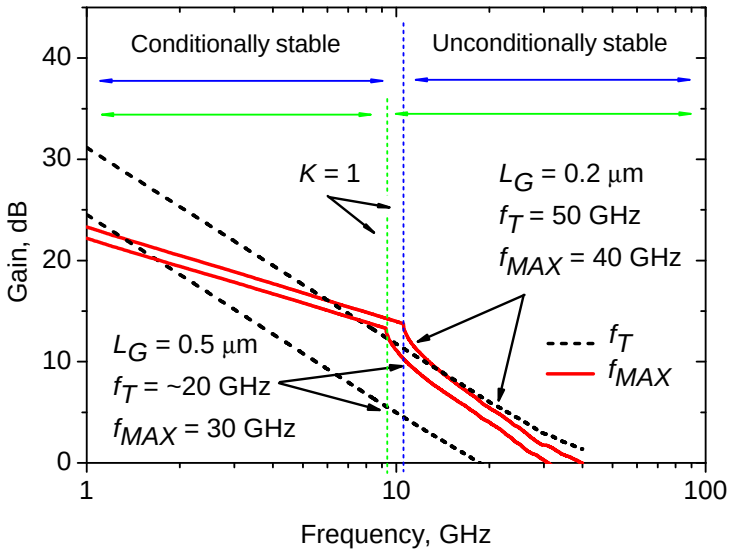
Fig. 4.25 shows the small-signal performance for two-finger AlGaN/GaN MOS-HEMT with gate length of $0.2\,\mu$m and total gate width of $400\,\mu$m. The values of f_T and f_{MAX} are 40 GHz and $\sim$29 GHz, respectively. $K = 1$ at approximately 6.5 GHz and $|\,\Delta\,| < 1$ for all frequencies. These values are not much different from those of an AlN/GaN MOS-HEMT for the same dimension device. Summary of RF performance of fabricated two-finger devices is shown in Fig. 4.7. Significant improvement in DC and RF performance of AlN/GaN MOS-HEMTs is expected by employing T-Gate and Field-plate technology on the devices.

TABLE 4.7: Summary of RF performance of fabricated devices.

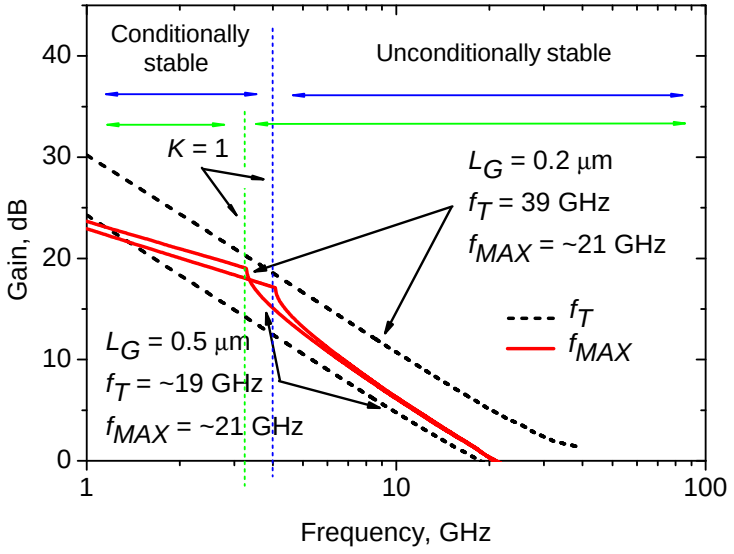
Wafer Structure	L_G, W_G, μm	f_T, GHz	f_{MAX}, GHz	Bias Point (V_{GS}, V_{DS})
AlN/GaN MOS-HEMT	3, 2 x 100	2.8	7.9	-1 V, 4 V
AlN/GaN MOS-HEMT	0.2, 2 x 200	40	21	-3 V, 10 V
	0.5, 2 x 200	$\sim$19	21	-3 V, 10 V
	0.2, 2 x 100	$\sim$50	40	-3 V, 10 V
	0.5, 2 x 100	$\sim$20	$\sim$30	-3 V, 10 V
AlGaN/GaN MOS-HEMT	0.2, 2 x 200	40	29	-3.5 V, 10 V

4.4 Summary

The use of thermally grown Al_2O_3 as a gate dielectric and device passivation for AlN/GaN MOS-HEMTs has been described and discussed. The approach provides an opportunity to define the Ohmic contact areas by wet etching of Al (and optimisation of this processing step) prior to the formation of Al_2O_3 and



(a)



(b)

FIGURE 4.24: Summary of RF performance of fabricated 0.2 μm and 0.5 μm gate length AlN/GaN MOS-HEMT with different gate width sizes at V_{GS} = -3 V and V_{DS} = 10 V. (a) $W_G = 2 \times 100\,\mu$m, (b) $W_G = 2 \times 200\,\mu$m.

Ohmic metal deposition. The present devices demonstrate higher breakdown voltage, comparable cut off frequency and drain current capabilities to AlGaN/GaN

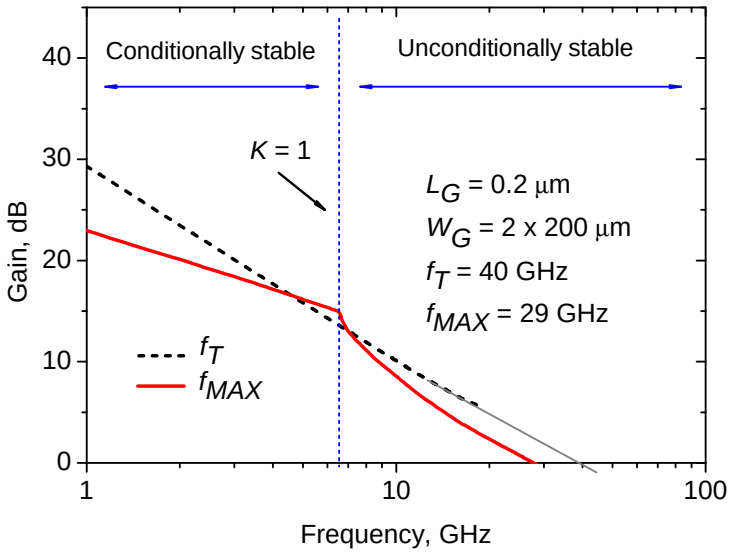


FIGURE 4.25: RF performance of fabricated two-finger gate AlGaN/GaN MOS-HEMT.

HEMT technology for similar gate lengths. This clearly demonstrates the potential of ultra-thin AlN/GaN-based devices for high power frequency applications. However, there are several aspects yet to be developed/improved in order to fully exploit advantages offered by the ultra-thin AlN barrier such as: (1) lower resistance Ohmic contacts, (2) lower gate leakage, and (3) improved passivation. The preliminary results of pulsed IV characterisations also indicate there is a fairly high density of defects/traps in this material system which needs to be solved. It is well known that surface passivation is essential for high efficiency large signal power applications so the effect of surface passivation using thermally grown Al_2O_3 on the devices need to be investigated further.

Chapter 5

Small-Signal Equivalent Circuit Extraction

5.1 Introduction

This chapter describes the determination of the small-signal equivalent circuit model values for fabricated AlN/GaN MOS-HEMTs. It relies on intimate process knowledge and device geometry to determine equivalent circuit elements of the fabricated AlN/GaN MOS HEMTs. An accurate small-signal modelling technique will be crucial to the continuing development and optimisation of the AlN/GaN MOS-HEMT technology by providing valuable feedback for process optimisation. It is also essential for reliable circuit design. In addition, the small-signal equivalent circuit model values for conventional AlGaN/GaN MOS-HEMTs are also described to provide comparative data.

5.2 HEMT Small-Signal Model

In this work, the extraction of a physically realistic small-signal equivalent circuit of the fabricated two-finger AlN/GaN MOS-HEMT and AlGaN/GaN MOS-HEMT with gate length of 0.2 μm and total gate width of 400 μm is presented. The

device had 3.2 μm source-drain spacing, gate-to-source and gate-to-drain distance of 1.5 μm each respectively. Summary of devices used for small-signal extraction model elements is shown in Table 5.1.

The small-signal equivalent circuit model used in this work is shown in Fig. 5.1 and is based on that used in previous GaN-based HEMT small-signal models [139]. This is a physically based small-signal equivalent circuit model. The extrinsic elements include the pad capacitances C_{pg}, C_{pgd} and C_{pd}, the pad inductances L_g, L_d, and L_s, and the gate and access resistances R_g, R_d, and R_s. They are bias independent except for the source resistance R_s [140]. The other parameters are intrinsic elements and are bias dependent.

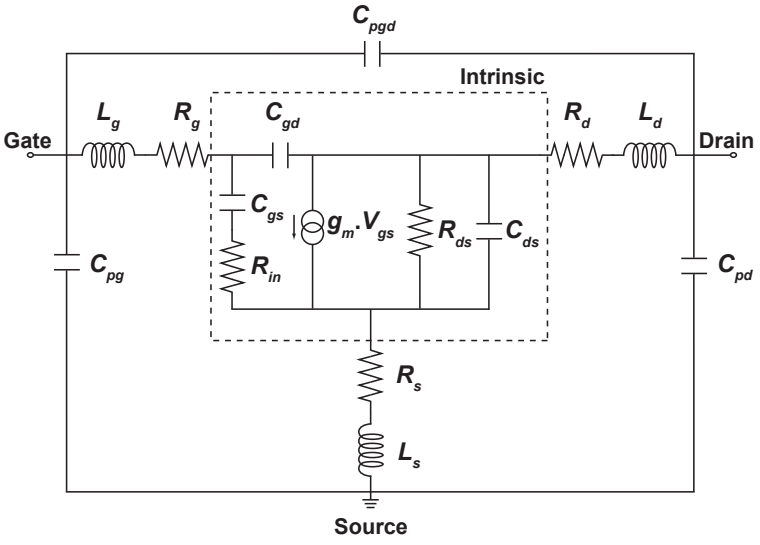


FIGURE 5.1: HEMT small-signal equivalent circuit model.

TABLE 5.1: Devices used for small-signal extraction model elements.

Wafer Structure	L_G, W_G μm	f_T, GHz	f_{MAX}, GHz
AlN/GaN MOS-HEMT	0.2, 2×200	$\cong 39$	$\cong 21$
AlGaN/GaN MOS-HEMT	0.2, 2×200	40	29

The extraction approach requires an intimate knowledge of the device layout from which the pad capacitances and inductances are estimated using 3D electromagnetic numerical simulations. The source and drain access resistances are estimated

from the TLM test structures, while the gate resistance is estimated from the gate geometry. Knowledge of the estimated values of these (extrinsic) elements allows all the intrinsic elements to be estimated analytically [141]. With good estimates of all the equivalent circuit known, optimisation of these now follows to determine the actual element values. This approach is based on the fact that in multi-variable optimisation, a starting vector close to the actual solution leads to quick convergence and determination of the correct optimised solution [142].

Small-signal modelling approaches of Schottky-gate GaN-based devices have generally followed that on the work of Dambrine et al. [143] to some extent, which requires forward biasing of the gate Schottky diode for the extraction of the bias independent extrinsic components including pad capacitances C_{pg}, C_{pd} and C_{pgd}, pad inductances L_g, L_s, L_d, and gate and access resistances R_g, R_s and R_d. For devices with an insulator or oxide underneath the gate metal, this technique does not work. For such devices, the lead inductances and gate and access resistances are usually determined at zero bias conditions [139], but the intrinsic device capacitances reduce the accuracy of this extraction approach.

5.3 Extrinsic Parameters Extraction

5.3.1 Parasitic Capacitances

The parasitic capacitances C_{pg}, C_{pd} and C_{pgd} are initially estimated from the test structure used to connect the co-planar waveguide (CPW) probes to the device. The test structure is simulated in Agilent's Momentum software and includes information about the epilayer geometry and relative dielectric constants. Here, the pads lie on the GaN buffer layer which has a dielectric constant of 10.4 [144]. *Momentum* is a 3D electromagnetic simulator within Agilent's Advanced Design System (ADS) software used for passive circuit modelling and analysis. It uses a technique called method of moments to solve Maxwell's electromagnetic equations

for planar structures embedded in a multilayered dielectric substrate [145]. Simulations produce S-parameter results of the structures which can be transformed to Y- and Z-parameters for further analysis.

For parasitic capacitances, the test structure is open-circuited in the region where the DUT would sit. Fig. 5.2(a) shows the 3D open test structure along with its equivalent circuit. Fig. 5.3 shows the imaginary part of the simulated Y-parameter data of the open test structure. It clearly shows a capacitive behaviour. The Y-parameters are then calculated from simulations from which the capacitance values are estimated based on the Eqns. 5.1, 5.2 and 5.3. A linear fit of the curves gives $C_{pg} = 38.66\,\text{fF}$, $C_{pd} = 39.31\,\text{fF}$, and $C_{pgd} = 1.36\,\text{fF}$. Fig. 5.4 shows plots of the extracted extrinsic/pad capacitances as a function of frequency. The capacitance values are constant with frequency as would be expected.

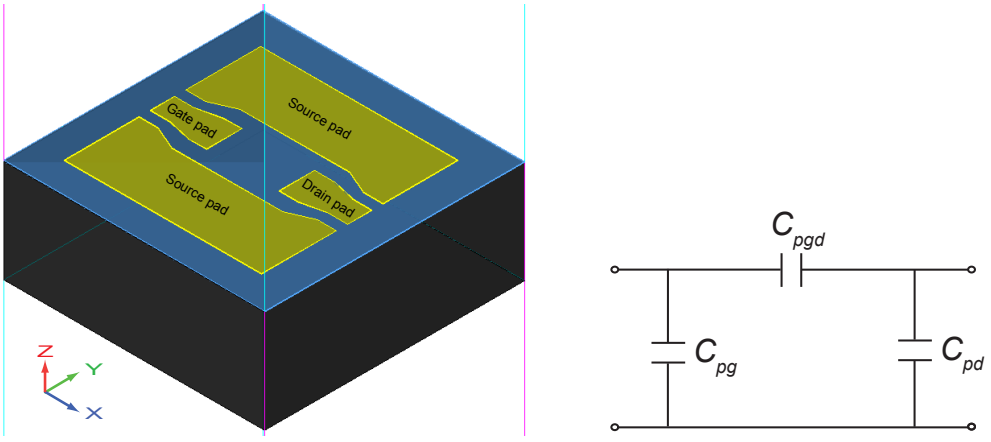


FIGURE 5.2: (a) Open test structure, and (b) Its equivalent circuit.

$$Y_{11} = j\omega\,(C_{pg} + C_{pgd}) \tag{5.1}$$

$$Y_{12} = Y_{21} = -j\omega\,(C_{pgd}) \tag{5.2}$$

$$Y_{22} = j\omega\,(C_{pd} + C_{pgd}) \tag{5.3}$$

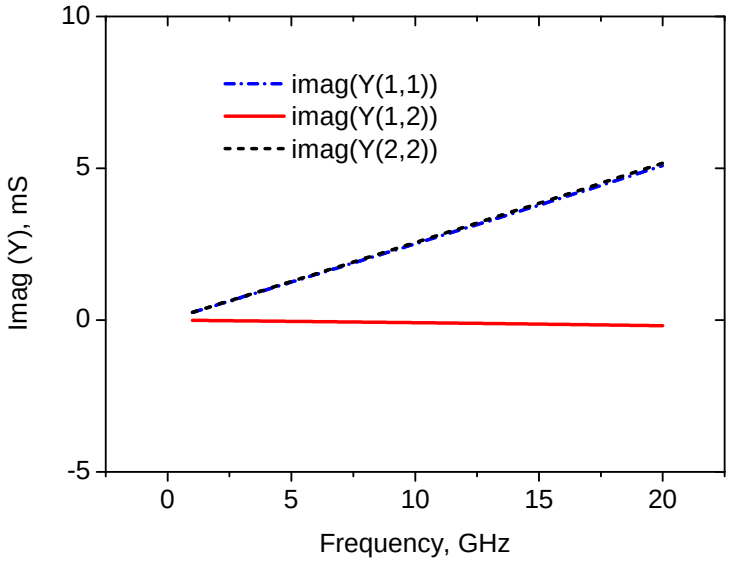


FIGURE 5.3: Imaginary part of the simulated Y-parameter data of the open test structure versus frequency.

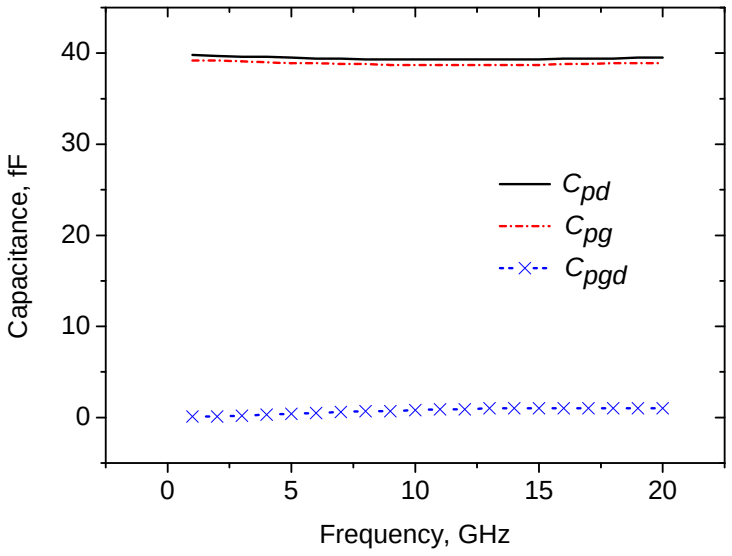
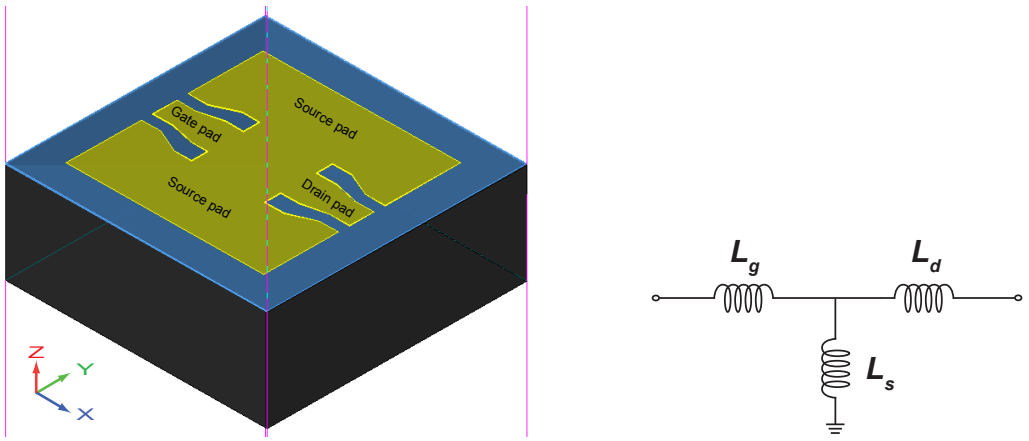


FIGURE 5.4: Parasitic capacitances versus frequency.

5.3.2 Pad Inductances

Pad inductances L_g, L_s and L_d are then estimated by a similar method, except a short circuit is placed where the DUT would sit. An illustration of the short test

structure, as well as its equivalent circuit is shown in Fig. 5.5(a).



(a) (b)

FIGURE 5.5: (a) Short test structure, and (b) Its equivalent circuit.

Z-parameters from this test structure are calculated from S-parameter simulations from which the values of inductances can be estimated from the following expressions:

$$Z_{11} = j\omega\,(L_g + L_s) \tag{5.4}$$

$$Z_{12} = j\omega\,(L_s) \tag{5.5}$$

$$Z_{22} = j\omega\,(L_d + L_s) \tag{5.6}$$

The test structure is not symmetrical and hence values of L_g and L_d differ slightly. Fig. 5.6 shows the imaginary part of the simulated Y-parameter data of the short test structure. It clearly shows a inductive behaviour. The Z-parameters are then calculated from simulations from which the capacitance values are estimated based on the Eqns. 5.4, 5.5 and 5.6. The linear fit of the curve gives $L_d = 100.30\,\text{pH}$, $L_g = 97.76\,\text{pH}$, and $L_s = 1.58\,\text{pH}$.Fig. 5.7 shows the pad inductances as a function of frequency. Again, as expected, inductance values do not change with frequency.

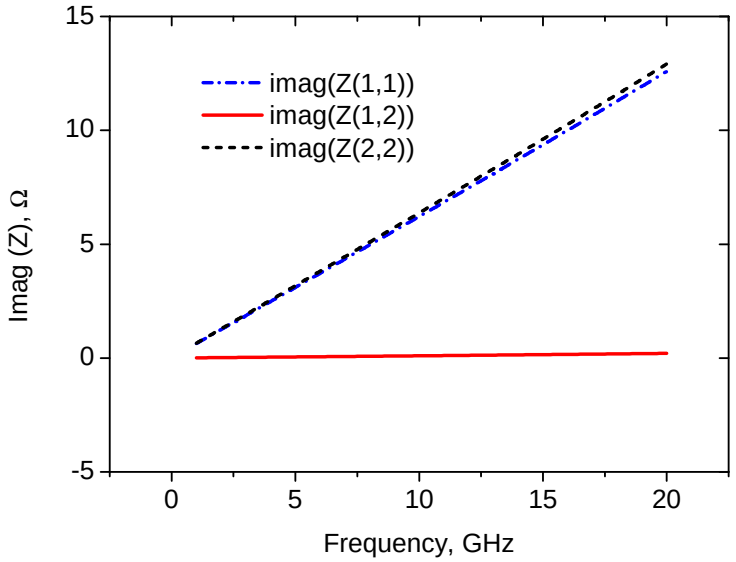


FIGURE 5.6: Imaginary part of the simulated Z-parameter data of the short test structure versus frequency.

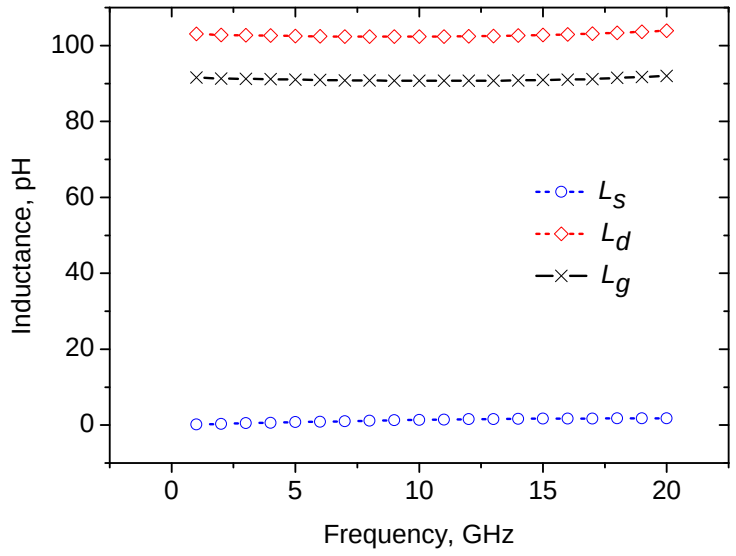


FIGURE 5.7: Parasitic capacitances versus frequency.

5.3.3 Gate and Access Resistances

The access resistances to the source and drain are now estimated using knowledge of the HEMT's layout, contact resistance and sheet resistance characteristics

(extracted from TLM measurements). The contact and sheet resistances were $0.76\,\Omega$.mm and $\sim 318\,\Omega/\square$ respectively. Device geometries were used as follows: $W_G = 2 \times 200\,\mu$m, $L_G = 0.2\,\mu$m, $L_{SD} = 3.2\,\mu$m, $L_{GS} = 1.5\,\mu$m, and $L_{GD} = 1.5\,\mu$m. Using the following equation an initial estimate for the contact resistance for the device can be made:

$$R_C \approx R_{d/s}.W \tag{5.7}$$

where W is the width of the source/drain and R_C is the contact resistance (in Ω.mm) extracted from the TLM measurements. The calculated value for R_d and R_s is $3.8\,\Omega$ $(\frac{R_C}{W})$ each. The effect of the sheet resistance should also be included, which again depends on the knowledge of the geometry of the device i.e. the separation between source-gate and gate-drain. The value of R_{sh} can be calculated using $R_{sh}\frac{L}{W}$, and gave $2.34\,\Omega$. Combining this with the initial estimate we get R_s and R_d to be approximately $6.19\,\Omega$ each (total access resistance $R_d = R_s = 3.8 + 2.385 = 6.19\,\Omega$). The DC gate resistance, R_g, is estimated by knowing the dimensions of the gate and applying the following expression [146]:

$$R_g = \frac{W_G}{nL_G h}.\rho \tag{5.8}$$

where W_G is the width of the gate, n is the number of gate fingers, L_G is the length of the gate, h is the thickness of the gate metal and ρ is the resistivity of the gate metals. In this case the gate metals are Ni (20 nm) and Au (300 nm). The resistivity of Au is used in the calculation since it is >10x thicker than the Ni. Clearly there will be some margin of error associated with this calculation due to the fabrication process i.e. the dimensions will vary slightly from those in the calculations. The calculated value for DC R_g is $75.70\,\Omega$, so for RF R_g, the value is equal to $\frac{1}{3}$ of its DC R_g [146], which is $25.22\,\Omega$. A factor of $\frac{1}{3}$ is introduced to Eqn. 5.8 to account for the distributed RC effects at RF [146]. The R_g value ($\sim 25\,\Omega$) is fairly large, however, it should be noted that a relatively thin layer of gold was used for the contact and so we would expect a lower resistance with thicker and broader gate metal (e.g. T-gate).

This approach was adopted since it is usually difficult to extract R_g directly from S-parameter measurements [142].

5.4 Intrinsic Parameters Extraction

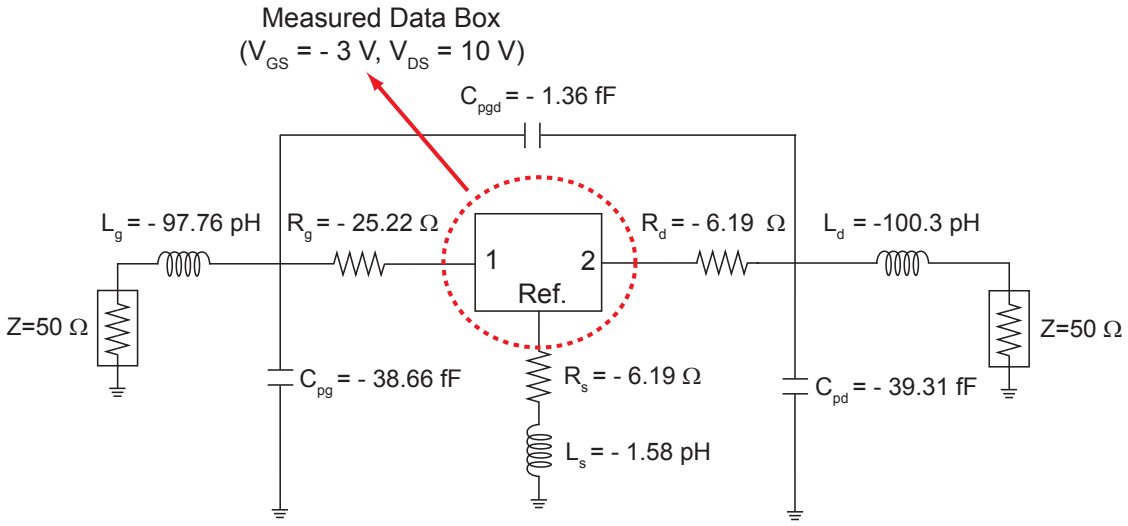


FIGURE 5.8: Agilent ADS schematic topology for the intrinsic parameter extraction with extrinsic elements subtracted using negative values at V_{GS} = -3 V and V_{DS} = 10 V.

Now that all extrinsic components of the small-signal model are known, they can be de-embedded from the measured S-parameter data as shown in Fig. 5.8. The parasitic de-embedding is equivalent to substracting impedances of L_g, L_d and L_s from the Z-parameters of the device, the admittances of C_{pg}, C_{pd} and C_{pgd} from the resultant parameters after conversion into Y-parameters, etc. [143]. The resulting parameters can be expressed as Y-parameters which are uniquely related to the intrinsic elements which can be estimated analytically as follows [141]:

$$C_{gd} = -\frac{Im\left(Y_{12}\right)}{\omega} \tag{5.9}$$

$$C_{gs} = \frac{Im\left(Y_{11}\right)-\omega C_{gd}}{\omega}\left(1+\frac{\left(Re\left(Y_{11}\right)\right)^2}{\left(Im\left(Y_{11}\right)-\omega C_{gd}\right)^2}\right) \tag{5.10}$$

$$R_{in} = \frac{Re\left(Y_{11}\right)}{\left(Im\left(Y_{11}\right)-\omega C_{gd}\right)^2+\left(Re\left(Y_{11}\right)\right)^2} \tag{5.11}$$

$$g_m = \sqrt{\left(\left(Re\left(Y_{21}\right)\right)^2+\left(Im\left(Y_{21}\right)+\omega C_{gd}\right)^2\right)\left(1+\omega^2 {C_{gs}}^2 {R_{in}}^2\right)} \tag{5.12}$$

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{-\omega C_{gd}-Im\left(Y_{21}\right)-\omega C_{gs}R_{in}Re\left(Y_{21}\right)}{g_m}\right) \tag{5.13}$$

$$C_{ds} = \frac{Im\left(Y_{22}\right)-\omega C_{gd}}{\omega} \tag{5.14}$$

$$g_{ds} = Re\left(Y_{22}\right) \tag{5.15}$$

Once the intrinsic element values were determined, the S-parameters of the model were then simulated and compared to the measured S-parameters values. Optimisation is necessary since uncertainties such as fabrication tolerances (line widths, spacing) and probe tip placement mean that the computed extrinsic (and therefore also intrinsic element values) are only estimates i.e. the extracted elements include errors. A gradient-based optimisation approach in ADS [147] was used to eliminate/minimise errors for small-signal modeling of AlN/GaN MOS-HEMT. Gradient optimiser uses the Gradient search method to arrive at new parameter values using the gradient information of the network's error function. The gradient of the error function indicates the direction to move a set of parameter values in order to reduce the error function. In the gradient optimisation, a Least-Squares fit procedure is executed to minimise the error between the measured and modelled S-parameters [147].

Maximum number of iterative optimisation was set in ADS to better fit the modelled S-parameter data to the measured S-parameter data. Optimisation goals, such as the magnitude and phase error targets for the S-parameters were defined in the simulator. The optimisation goals were:

$$Mag(S_{ij})_{modelled} - Mag(S_{ij})_{measured} \approx 0 \tag{5.16}$$

$$Phase(S_{ij})_{modelled} - Phase(S_{ij})_{measured} \approx 0 \tag{5.17}$$

The range of values that each element can take was also defined. To ensure that the optimisation procedure yields reasonable element values, user need to set tight ranges for most of the elements. Only the elements that exhibited a large variation in the calculated values over frequency were allowed wide ranges in the optimisation procedure (i.e. R_g, g_m, C_{gs}, C_{ds}, C_{gd} and R_{ds}). The optimisation program was then executed and it results in a better fit between the simulated and measured S-parameters by varying the element values. Since there is more than one way for the optimisation procedure to converge, the elements values obtained from one run and next vary slightly.

The optimised values were obtained by searching for a minimum in the error function. If the starting values for the gradient search method were close enough to the actual physical parameters of the device, the search method converged to the absolute minimum, which represents the real parameter values. Also if the modelled S-parameters are good fit with the measured S-parameters, it could be stated that the values for the parasitic parameters determined by the optimiser correspond to their real values. The optimisation goals were satisfied when the difference between the measured and modelled S-parameters equaled or approached zero.

The percentage of error between the measured and modelled S-parameters is calculated using the following equation;

$$Error(\%) = \frac{((S_{ij}Measured) - (S_{ij}Modelled))}{S_{ij}Measured} \times (100) \tag{5.18}$$

Tables 5.3 and 5.4 give details on the values of the extracted model elements. All elements values required some degree of optimisation, however, it should be noted that the values do not vary so much that initial estimations could be disregarded completely. From the optimisation, the parameters such as R_g, g_m, C_{gs}, C_{ds}, C_{gd} and R_{ds} play an important role to improve fitting of S-parameters. A wide range of values was set for these parameters during the optimisation. While tight range

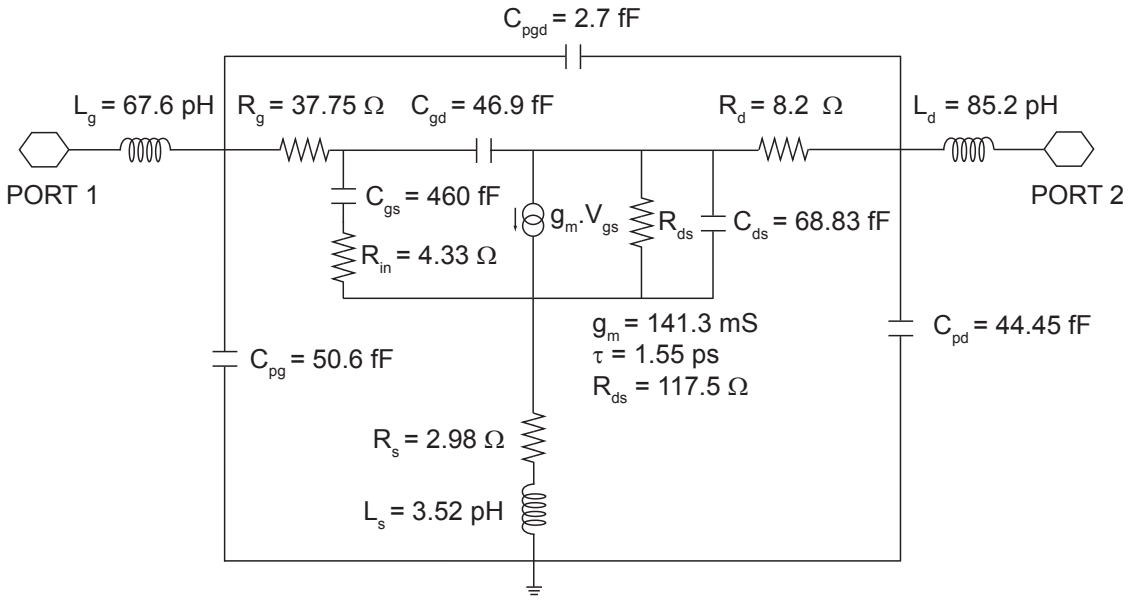
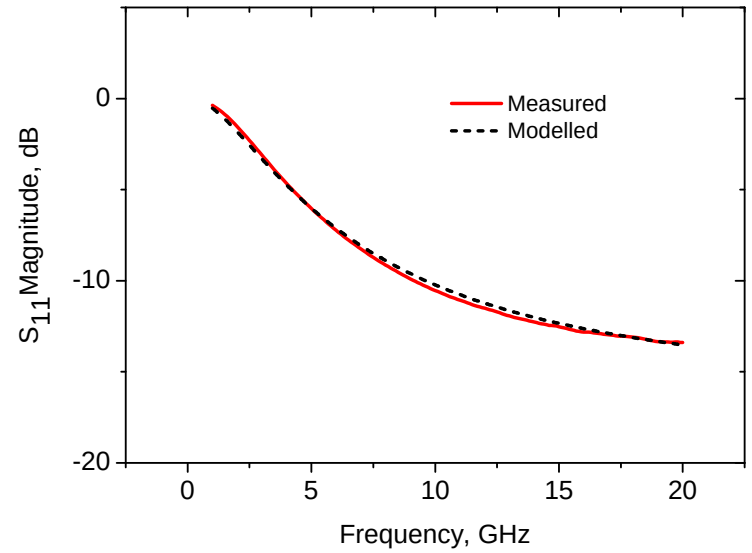


FIGURE 5.9: Modelled AlN/GaN MOS-HEMT after optimisation at V_{GS} = -3 V and V_{DS} = 10 V.

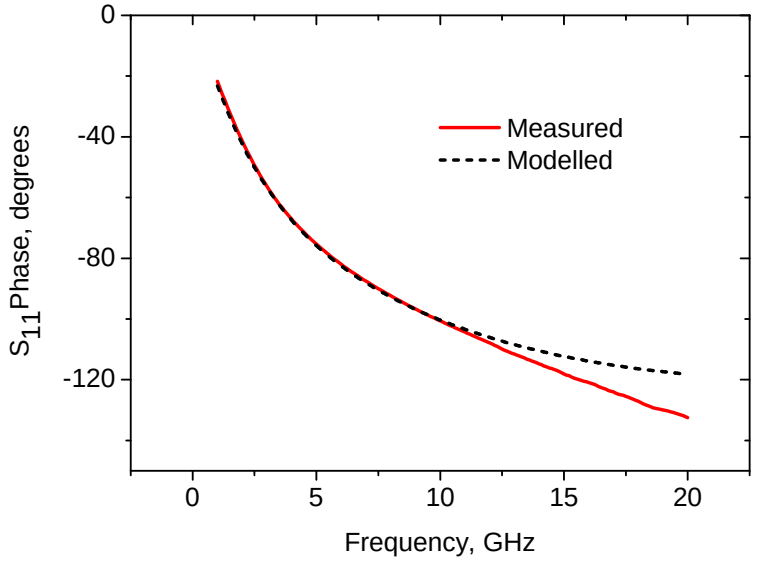
of values was set for the rest of parameters. It is important to note that all the optimised values for extrinsic elements do not vary much with their estimated/initial values (except for L_g) which indicate the validity of the method used for extraction of the extrinsic elements. Since these estimates/initials are closely related to the actual devices, they form a starting vector (of equivalent circuit elements) which is close to the actual solution. This leads to quick convergence and determination of the correct optimised solution.

Figs. 5.10,5.11,5.12 and 5.13 and shows a good fit between measured and modelled S-parameters from 1 - 20 GHz, suggesting that the model topology and approach for determining element values is justified. The error was less than 5 % for all S-parameters as shown in Table 5.2. The extrinsic $G_{m,ext}$ was calculated from the extracted intrinsic transconductance ($g_{m,int}$) using Eqn. 1.8 (given in section 1.2.3), and gave value of 248.57 mS/mm for small-signal model AlN/GaN MOS-HEMT. The measured DC extrinsic G_m was 280.70 mS/mm (refer to Fig. 4.14(b)) which indicates that there was a DC to RF dispersion in transconductance for this device.

The extracted gate resistance is very high i.e. 38 Ω probably explaining the lower value of f_{MAX} compared to f_T in Section 4.3.4. This high resistance is due to the



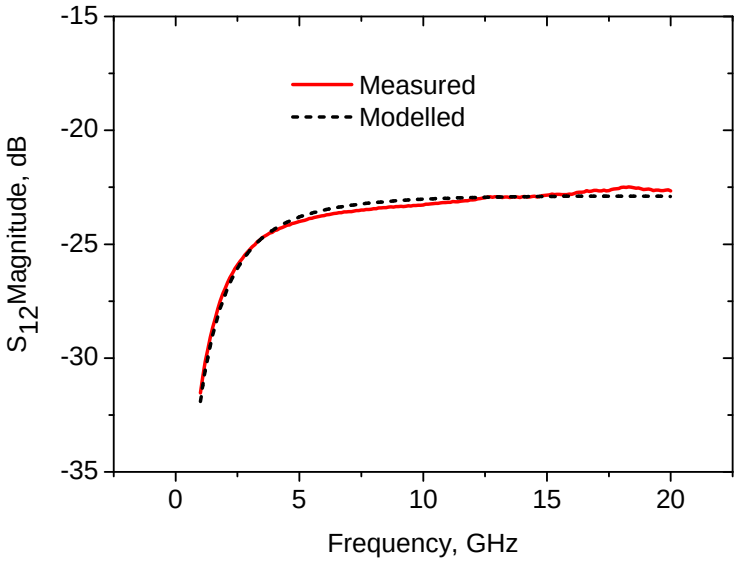
(a)



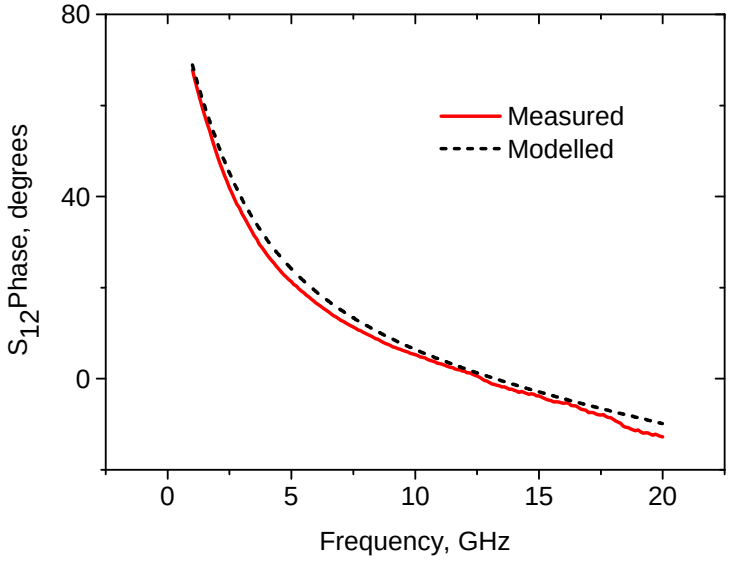
(b)

FIGURE 5.10: Modelled and Measured S_{11} of AlN/GaN MOS-HEMTs at the frequency range of 1 - 20 GHz, (a) dB versus Frequency, and (b) Phase versus Frequency at V_{GS} = -3 V and V_{DS} = 10 V.

gate having a vertical structure (adopted because of simpler processing). Therefore, a T-gate structure should be used in future devices. Contact resistances also need further reducing.



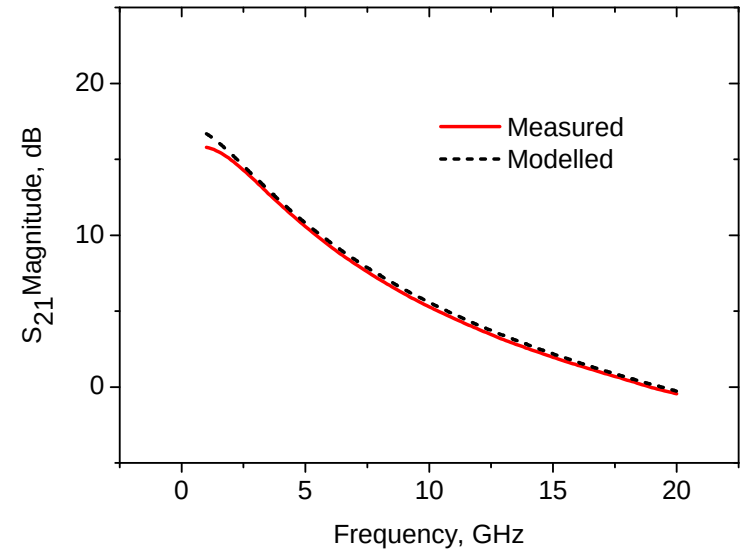
(a)



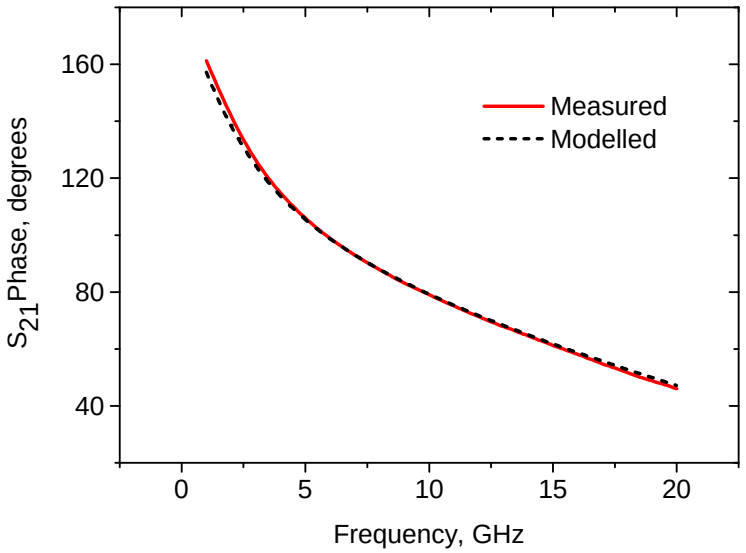
(b)

FIGURE 5.11: Modelled and Measured S_{12} of AlN/GaN MOS-HEMTs at the frequency range of 1 - 20 GHz, (a) dB versus Frequency, and (b) Phase versus Frequency at V_{GS} = -3 V and V_{DS} = 10 V.

By using the same procedure, the small-signal equivalent circuit model values for conventional two-finger AlGaN/GaN MOS-HEMT with gate length of 0.2 μm and total gate width of 400 μm (same device dimension as AlN/GaN MOS-HEMT)



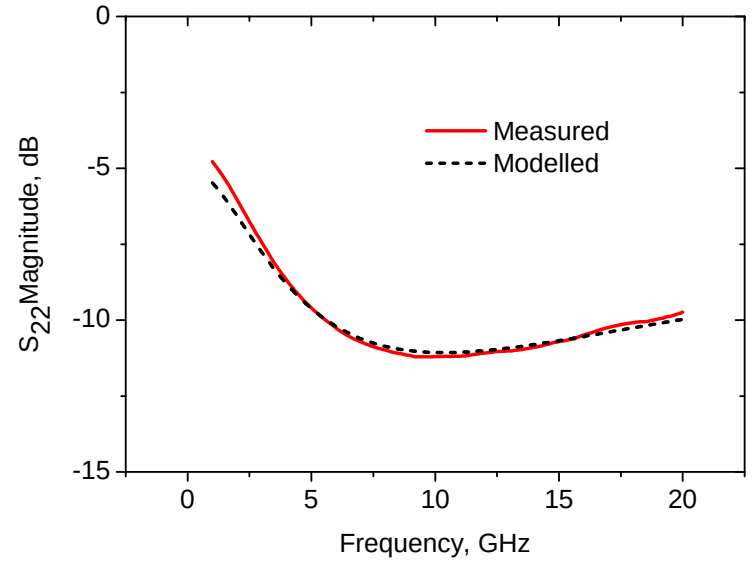
(a)



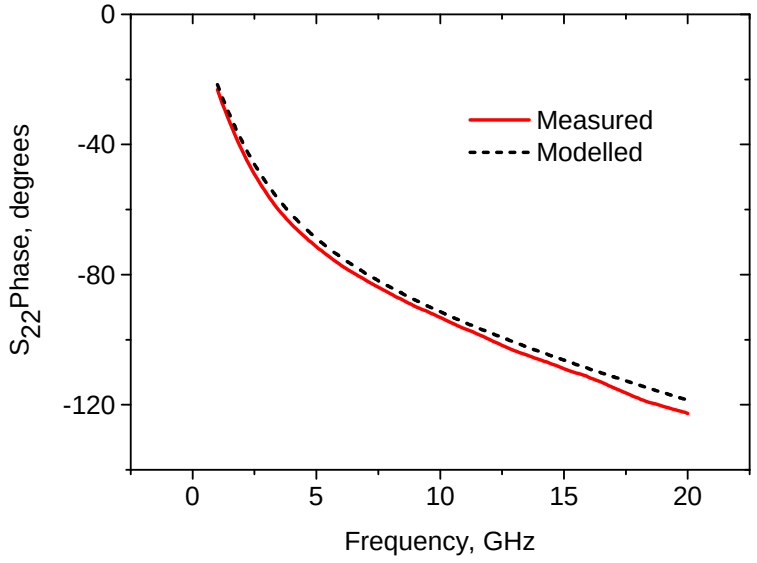
(b)

FIGURE 5.12: Modelled and Measured S_{21} of AlN/GaN MOS-HEMTs at the frequency range of 1 - 20 GHz, (a) dB versus Frequency, and (b) Phase versus Frequency at V_{GS} = -3 V and V_{DS} = 10 V.

was also extracted. Tables 5.5 and 5.6 give details on the values of the extracted model elements of AlGaN/GaN MOS-HEMT. These values are not much different from those of an AlN/GaN MOS-HEMT except for the intrinsic transconductance



(a)



(b)

FIGURE 5.13: Modelled and Measured S_{22} of AlN/GaN MOS-HEMTs at the frequency range of 1 - 20 GHz, (a) dB versus Frequency, and (b) Phase versus Frequency, at V_{GS} = -3 V and V_{DS} = 10 V.

(g_m), gate-to-source capacitance (C_{gs}) and output resistance (R_{ds}). There was a slightly different for R_d and R_s due to values of $\sim 0.5\,\Omega$.mm and $\sim 500\,\Omega/\square$ were used for AlGaN/GaN MOS-HEMT.

DC to RF dispersion in transconductance was also observed for AlGaN/GaN MOS-HEMT since its calculated extrinsic $g_{m,ext}$ value, 135.90 mS/mm smaller than the measured DC G_m, 206.10 mS/mm (refer to Fig. 4.16(a)).

The lower g_m in AlGaN/GaN MOS-HEMT is attributed to larger distance between the gate to the channel (i.e. thicker barrier layer) as compared to AlN/GaN MOS-HEMT. This also leads to decreased gate-to-source capacitance (C_{gs}) in AlGaN/GaN MOS-HEMT. A good fit between measured and modeled S-parameters was achieved as shown in Figs. 5.14,5.15,5.16 and 5.17. The error was less than 7 % for all S-parameters as shown in Table 5.2. The extrapolated values of f_T and f_{MAX} (shown in Figs. 5.18 and 5.19) were similar to the extrapolated measured f_T and f_{MAX} values for both structrures. K =1 at approximately 3 GHz and 8 GHz for AlN/GaN MOS-HEMT and AlGaN/GaN MOS-HEMT, respectively. $|\Delta| < 1$ for all frequencies for both modelled devices. This indicates that the small-signal modeling method, which utilises optimisation, can be successfully applied for both on AlN/GaN MOS-HEMTs and AlGaN/GaN MOS-HEMTs.

TABLE 5.2: Error percentage (%) of measured and modelled S-parameters for both AlN/GaN MOS-HEMT and AlGaN/GaN MOS-HEMT.

	Error percentage (%)	
S-Parameters	AlN/GaN MOS-HEMT	AlGaN/GaN MOS-HEMT
S_{11}(dB)	1.00	6.50
S_{11}(Phase)	2.00	1.40
S_{12}(dB)	0.02	0.20
S_{12}(Phase)	3.40	5.70
S_{21}(dB)	1.40	0.37
S_{21}(Phase)	0.20	3.20
S_{22}(dB)	0.90	0.10
S_{22}(Phase)	3.20	0.05

TABLE 5.3: Small-Signal Equivalent Circuit Extrinsic Elements of AlN/GaN MOS-HEMTs at V_{GS} = -3 V and V_{DS} = 10 V.

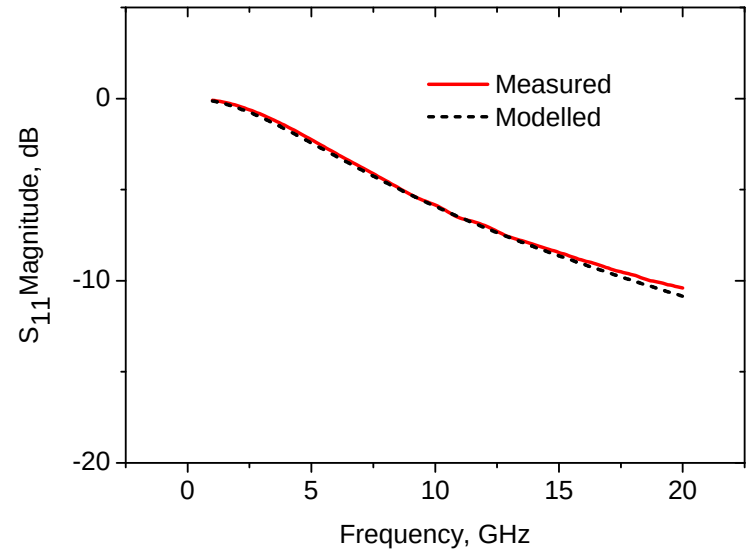
Extrinsic Parameters	Estimated	Optimised
L_g	97.76 pH	67.60 pH
L_s	1.58 pH	3.52 pH
L_d	100.30 pH	85.20 pH
R_g	25.22 Ω	37.75 Ω
R_s	6.19 Ω	2.98 Ω
R_d	6.19 Ω	8.20 Ω
C_{pg}	38.66 fF	50.60 fF
C_{pd}	39.31 fF	44.45 fF
C_{pgd}	1.36 fF	2.70 fF

TABLE 5.4: Small-Signal Equivalent Circuit Intrinsic Elements of AlN/GaN MOS-HEMTs at V_{GS} = -3 V and V_{DS} = 10 V.

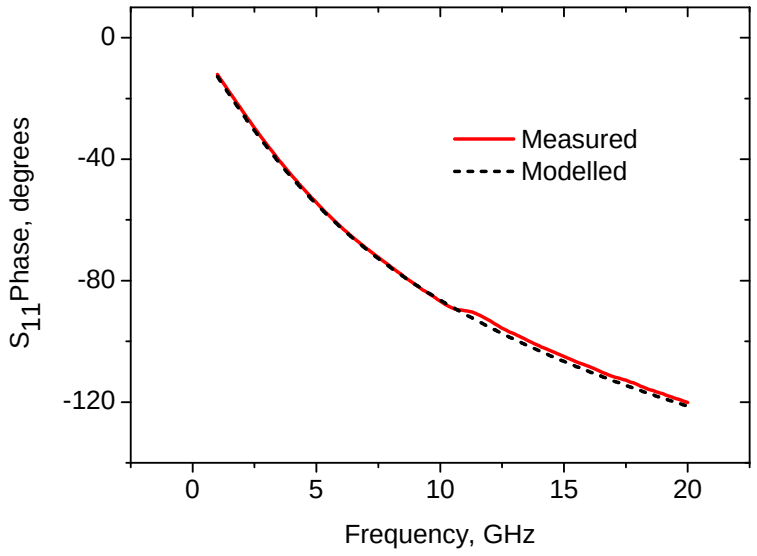
Intrinsic Parameters	Estimated	Optimised
g_m	164.2 mS	141.30 mS
C_{gs}	523.2 fF	460.00 fF
C_{gd}	22.09 fF	46.90 fF
C_{ds}	84.8 fF	68.83 fF
R_{in}	6.35 Ω	4.33 Ω
R_{ds}	91.55 Ω	117.50 Ω
τ	1.05 ps	1.55 ps

5.5 Summary

The small-signal equivalent circuit model extraction for fabricated AlN/GaN MOS-HEMT and AlGaN/GaN MOS-HEMT has been desribed and discussed. The extraction approach is based on an accurate estimate of all the equivalent circuit elements followed by optimisation of these to get the actual element values. Good fit between measured and modelled S-parameters as well as the physically realistic extracted equivalent circuit elements demonstrate the validity of the approach. The optimised element values were not markedly different from the estimated ones showing the robustness of the developed extraction approach. The extracted element values provide feedback for further device process optimisation.

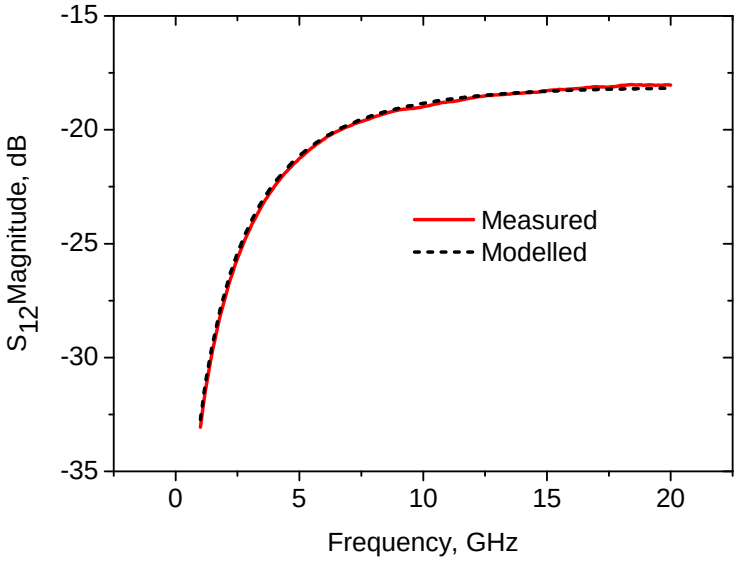


(a)

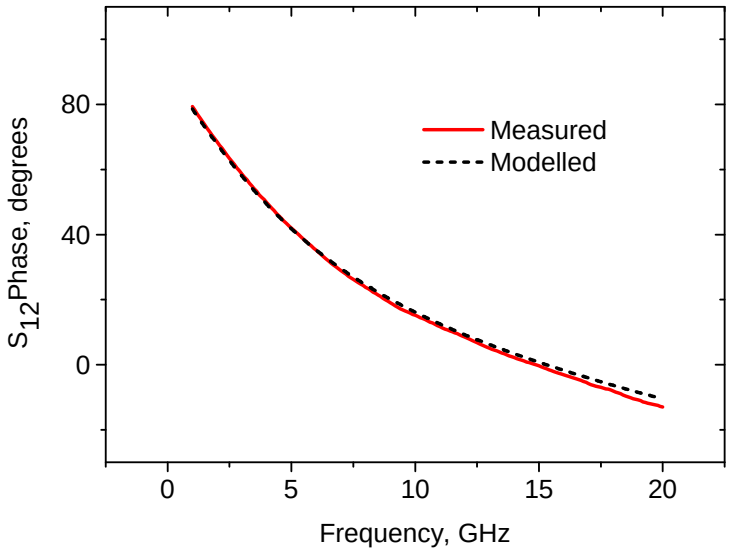


(b)

FIGURE 5.14: Modelled and Measured S_{11} of AlGaN/GaN MOS-HEMTs at the frequency range of 1 - 20 GHz, (a) dB versus Frequency, and (b) Phase versus Frequency at V_{GS} = -3.5 V and V_{DS} = 10 V.

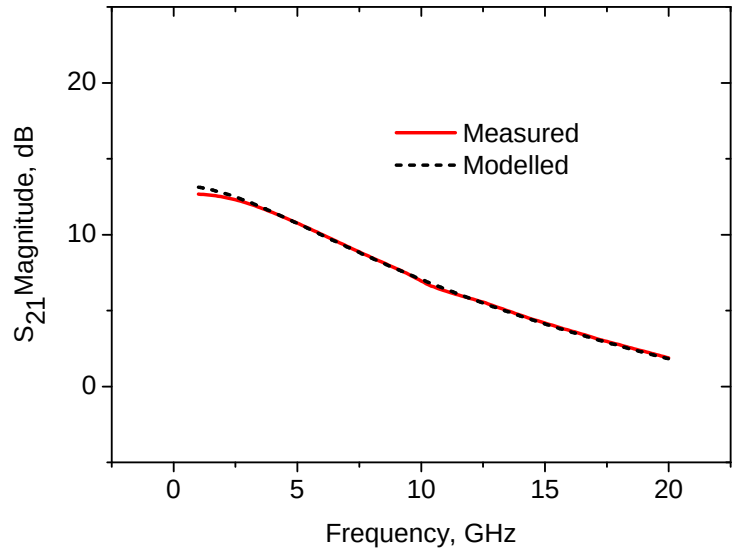


(a)

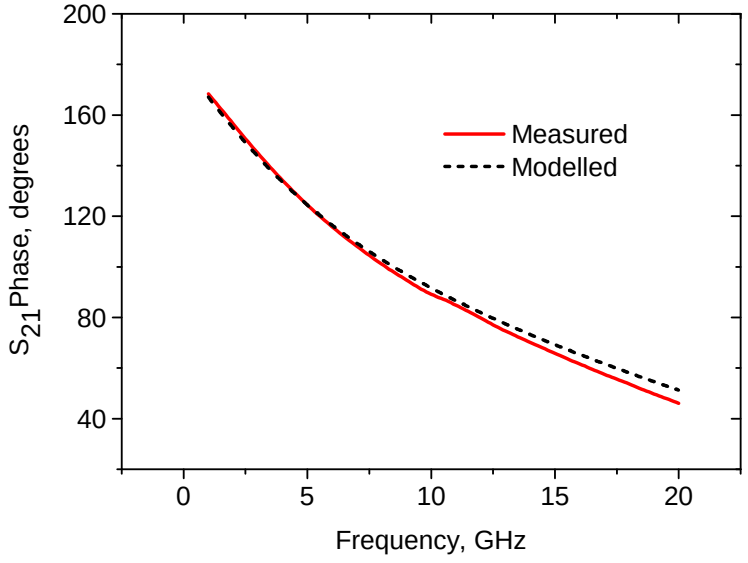


(b)

FIGURE 5.15: Modelled and Measured S_{12} of AlGaN/GaN MOS-HEMTs at the frequency range of 1 - 20 GHz, (a) dB versus Frequency, and (b) Phase versus Frequency at V_{GS} = -3.5 V and V_{DS} = 10 V.

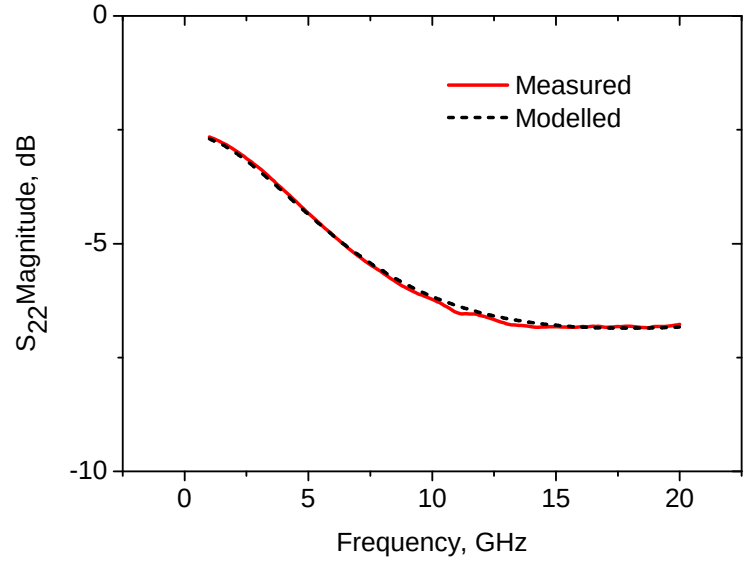


(a)

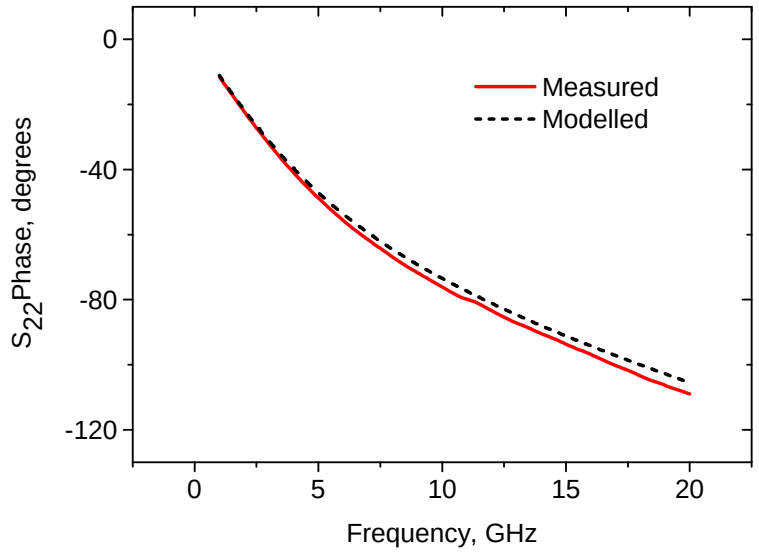


(b)

FIGURE 5.16: Modelled and Measured S_{21} of AlGaN/GaN MOS-HEMTs at the frequency range of 1 - 20 GHz, (a) dB versus Frequency, and (b) Phase versus Frequency at V_{GS} = -3.5 V and V_{DS} = 10 V.



(a)



(b)

FIGURE 5.17: Modelled and Measured S_{22} of AlGaN/GaN MOS-HEMTs at the frequency range of 1 - 20 GHz, (a) dB versus Frequency, and (b) Phase versus Frequency at V_{GS} = -3.5 V and V_{DS} = 10 V.

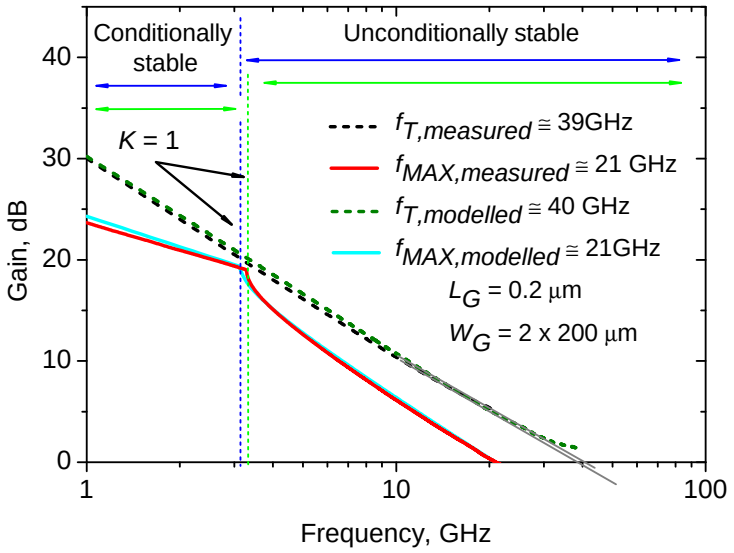


FIGURE 5.18: Extrapolated f_T and f_{MAX} of modelled AlN/GaN MOS-HEMT after optimisation at V_{GS} = -3 V and V_{DS} = 10 V.

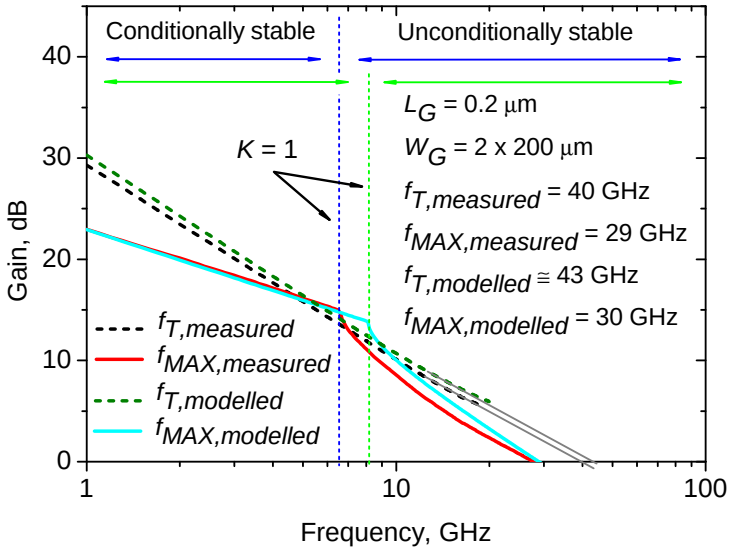


FIGURE 5.19: Extrapolated f_T and f_{MAX} of modelled AlGaN/GaN MOS-HEMT after optimisation at V_{GS} = -3.5 V and V_{DS} = 10 V.

TABLE 5.5: Small-Signal Equivalent Circuit Extrinsic Elements of AlGaN/GaN MOS-HEMTs at V_{GS} = -3.5 V and V_{DS} = 10 V.

Extrinsic Parameters	Estimated	Optimised
L_g	97.76 pH	112.00 pH
L_s	1.58 pH	3.34 pH
L_d	100.30 pH	86.00 pH
R_g	25.22 Ω	32.50 Ω
R_s	6.25 Ω	5.77 Ω
R_d	6.25 Ω	3.40 Ω
C_{pg}	38.66 fF	41.60 fF
C_{pd}	39.31 fF	39.71 fF
C_{pgd}	1.36 fF	2.10 fF

TABLE 5.6: Small-Signal Equivalent Circuit Intrinsic Elements of AlGaN/GaN MOS-HEMTs at V_{GS} = -3.5 V and V_{DS} = 10 V.

Intrinsic Parameters	Estimated	Optimised
g_m	77.43 mS	79.20 mS
C_{gs}	252.10 fF	245.00 fF
C_{gd}	37.37 fF	37.00 fF
C_{ds}	129.80 fF	64.84 fF
R_{in}	1.55 Ω	1.09 Ω
R_{ds}	276.70 Ω	225.00 Ω
τ	0.07 ps	0.25 ps

Chapter 6

Summary and Future Work

6.1 Summary and Conclusions

Having key properties such as high 2DEG sheet carrier density, high 2DEG mobility, high breakdown fields and low sheet resistances makes the AlN/GaN-based HEMTs technology very promising for future microwave power devices. Despite being an immature technology as compared to conventional AlGaN/GaN HEMTs, AlN/GaN-based devices already demonstrated comparable DC and RF performances. With the expected very high power density with this material system, extremely compact AlN/GaN power transistors with high output powers at high frequencies can be realised.

At the beginning, the difficulty to grow high quality material i.e. high 2DEG sheet carrier density and high 2DEG mobility, was one of main problems in developing the technology. As research continues, a few of groups have reported very impressive results in the material growth, leading to tremendous progress in the current capabilities and frequency performances (as summarised in Table 1.5). Having very thin AlN barrier layer $\sim$3 - 4 nm (i.e. the 2DEG channel is very near to the surface), makes the epilayers very sensitive to liquids coming in contact with the surface. Exposure to any chemical solutions during device processing degrades the

surface properties, resulting in poor device performance. To overcome the problems, a protective layer is employed during fabrication of AlN/GaN-based devices. However, in the presence of the protective/passivation layers, formation of low Ohmic resistance source and drain contacts is difficult. A very delicate and well optimised processing is required to remove/etch this layer.

In this work, thermally grown Al_2O_3 was used as a gate dielectric and surface passivation for AlN/GaN MOS-HEMTs. Most importantly, the Al_2O_3 acts as a protection layer during device processing. Good DC and RF performances was achieved in the fabricated devices. The main results of the research described in this thesis are summarised below:

1. **Thermally grown Al_2O_3** This is an alternative approach to form Al_2O_3 layer. The technique is simple, less expensive (compared for instance to ALD), and also effective in protecting the AlN/GaN epilayer structure. The developed technique employs $\sim 2\,nm$ layer of Al to protect the surface, and after thermal oxidation forms Al_2O_3 which is also acts as a surface passivation and gate dielectric for AlN/GaN MOS-HEMTs.

2. **Ohmic contact optimisation using Al wet etch** The developed thermally grown Al_2O_3 technique as mentioned in (1) allows for a simple and effective wet etching optimisation technique for the Ohmic contact resistances on AlN/GaN MOS-HEMT structures. The Al in the Ohmic regions is etched by $16H_3PO_4$:HNO_3:$2H_2O$ solution (and optimisation of this processing step) prior to the formation of Al_2O_3 and Ohmic metallisation. Low Ohmic contact resistance ($0.76\,\Omega$.mm) as well as low sheet resistance ($318\,\Omega/\square$) were obtained after optimisation. The achieved results are comparable to the lowest reported in the literature for this material system [78].

3. **Mesa sidewall protection** For RF devices (i.e. which employ the mesa isolation step), an additional layer of thermally grown was deposited on the mesa side wall. Significant reduction in the gate leakage current was observed when employing an additional layer of thermally grown Al_2O_3 on the mesa sidewalls.

4. **Small-signal equivalent circuit model extraction** An approach based on an accurate estimate of all the equivalent circuit elements followed by optimisation of these to get the actual element values was developed. This way, element variations due to fabrication tolerances, measurement uncertainties such as probe tip placement accuracy and variations in material across a wafer are accounted for. The extracted element values provide feedback for further device process optimisation.

The achieved results indicate the suitability of thermally grown Al_2O_3 for AlN/GaN MOS-HEMT technology for future high frequency power applications. Further improvement in DC and RF performances will be achieved with scaling the transistor dimensions, reducing the parasitic resistances and capacitances, and employing the field plate technology. Further analysis and characterisation of thermally grown Al_2O_3 used as a surface passivation on AlN/GaN-based devices needs to be conducted so problems such as surface trapping can be eliminated. Surface preparation prior to Al deposition may be the key. Apart from D-mode AlN/GaN MOS-HEMTs, there is potential to develop E-mode type devices based on AlN/-GaN MOS-HEMTs [80],[148]. E-mode devices offer many important advantages in circuit design such as simpler circuit configuration (only single polarity power supply needed) and offer fail-safe operation.

The following section will discuss potential research for future work.

6.2 Future Work

6.2.1 *In-situ* Al

A thin GaN cap layer is known to protect the surface from the oxidation and to promote low resistance Ohmic contact on AlN/GaN epilayers [60]. Based on experience in processing this structure, deposition of thin (2 - 3 nm) *in-situ* Al is another eficient way to protect the surface from oxidation and/or contamination

by air exposure and subsequent processes. This is illustrated in Fig. 6.1a. The AlN surface is protected in this case right upon growth and is not therefore directly exposed to the atmosphere. Low resistance Ohmic contact can be realised using the Ohmic recess technique by optimised the wet etching both for Al and AlN [76],[83]. After the Ohmic recess, the remaining Al layer will be oxidised to form Al_2O_3 and gate metal will be deposited directly on top of the Al_2O_3. The proposed D-mode device structure is illustrated in Fig. 6.1b.

In addition, E-mode or normally off AlN/GaN devices may be also realised using oxidation of the barrier layer as in Ref. [80],[149],[150]. Parameters such as annealing temperature and annealing time during thermal oxidation need to be optimised in order to shift the threshold voltage, V_{th} from negative to positive. By oxidizing the exposed AlN in the gate region/foot, the AlN barrier layer thickness is decreased and the V_{th} can be shifted to positive. The proposed E-mode device structure is illustrated in Fig. 6.1c.

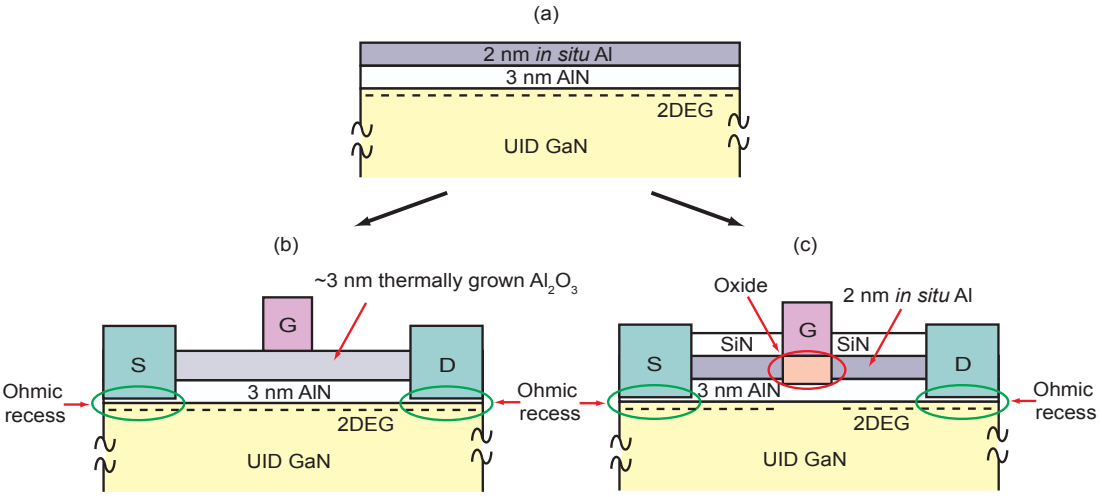


FIGURE 6.1: (a) Proposed AlN/GaN HEMT with 2 nm of *in situ* Al, (b) Proposed D-mode type device, and (c) Proposed E-mode type device.

6.2.2 Thermal Management in AlN/GaN HEMTs

The GaN-based heterostructures grown on SiC substrates have demonstrated power density up to 41 W/mm at 4 GHz [32] due to good thermal conductivity

of SiC (4 W/Kcm) [3]. Despite some excellent results, SiC substrates suffer from high cost so sapphire is the commonly used substrates to III-nitrides. However, sapphire has low thermal conductivity, 0.25 W/Kcm [151], as compared to SiC. Therefore, devices on sapphire substrates suffer from self-heating effects leading to poor power performance [152]. This effect is clearly observed in the DC characteristics of I_{DS} versus V_{DS} for AlN/GaN HEMTs, when the drain current I_{DS} decreases with increasing drain voltage V_{DS}. Increased drain current results in more power that leads to higher channel temperature, causing reduction in electron mobility which in turn decreases drain current [153]. Thus, accurate modeling of self-heating effects in this material system and device structure optimisation for better thermal management becomes important for further development of AlN/GaN-based HEMTs technology.

6.2.3 Traps in AlN/GaN HEMTs

Current collapse is a trap-related phenomenon that severely limits the output power of FETs, and has been observed in AlGaN/GaN HEMTs. It causes the output power achieved from a device at microwave frequency to be considerably smaller than that expected based on DC charaterisation. The presence of surface or epitaxial layer related defects and traps in the device structure are responsible for this. Intensive research work and studies have been reported on this topic to understand and analyse this problem in AlGaN/GaN HEMTs [154],[155]. To date, there is no study that has been reported for defects or traps in AlN/GaN HEMTs. Thus, an understanding of defects and traps in this structure is essential for improving material quality and consequently device performances.

Appendix A

AlN/GaN MOS-HEMT Device Processing

A1. RF Device with 3 μm Gate Length

Note: All the fabrication steps were defined using optical lithography.
*Sample cleaning is done with only de-ionised (DI) water. Standard sample cleaning is done with acetone, isopropanol and DI water.

1. **2 nm Al deposition**
   - Clean sample*
   - De-oxidise in $4H_2O$:HCl for 1 min
   - Rinse with DI water for 15 secs
   - Blow dry with N_2
   - Deposit 2 nm using electron beam metal evaporator
2. **Alignment Marker**
   - Clean sample
   - Spin Microposit S1818 resist at 4000 rpm for 120 secs
   - Bake on hotplate at 65 °C for 120 secs

- Soak in Microposit Concentrate:H_2O for 1 min
- Rinse in DI water
- Blow dry with N_2
- Expose using MA6 for 5 secs
- Develop with Microposit Concentrate:H_2O for 75 secs
- Rinse in DI water
- Blow dry with N_2
- Oxygen ash at 40 W for 3 mins
- Deposit Ti/Au = 50/100 nm using electron beam metal evaporator
- Soak in acetone at 50 °C for 15 mins
- Rinse in IPA for 15 secs
- Blow dry with N_2

3. Mesa Isolation

- Clean sample
- Spin Microposit S1818 resist at 4000 rpm for 120 secs
- Bake on hotplate at 65 °C for 120 secs
- Expose using MA6 for 5 secs
- Develop with Microposit Concentrate:H_2O for 75 secs
- Rinse in DI water
- Blow dry with N_2
- Oxygen ash at 40 W for 3 mins
- Bake resist on hotplate at 90 °C for 3 mins
- Submit to System 100 RIE (T-gate) with recipe $SiCl_4$ = 30 sccm, 30 mT, 75 W, etch for 40 mins
- Soak in acetone at 50 °C for 15 mins
- Rinse in IPA for 15 secs

- Blow dry with N_2

4. Side Mesa Protection Layer

- Clean sample
- Spin Microposit S1818 resist at 4000 rpm for 120 secs
- Bake on hotplate at 65 °C for 120 secs
- Soak in Microposit Concentrate:H_2O for 1 min
- Rinse in DI water
- Blow dry with N_2
- Expose using MA6 for 5 secs
- Develop with Microposit Concentrate:H_2O for 75 secs
- Rinse in DI water
- Blow dry with N_2
- Oxygen ash at 40 W for 3 mins
- Deposit 2 nm Al using electron beam metal evaporator
- Soak in acetone at 50 °C for 15 mins
- Rinse in IPA for 15 secs
- Blow dry with N_2

5. Etch 2 nm Al in the source and drain region

- Clean sample
- Spin Microposit S1818 resist at 4000 rpm for 120 secs
- Bake on hotplate at 65 °C for 120 secs
- Expose using MA6 for 5 secs
- Develop with Microposit Concentrate:H_2O for 75 secs
- Rinse in DI water
- Blow dry with N_2

- Oxygen ash at 40 W for 3 mins
- Bake resist on hotplate at 90 °C for 3 mins
- Etch 2 nm Al with $16H_3PO_4$:HNO_3:$2H_2O$ for 20 secs
- Rinse in DI water for 5 mins
- Soak in acetone at 50 °C for 15 mins
- Rinse in IPA for 15 secs
- Blow dry with N_2

6. Thermal oxidation of evaporated 2 nm Al

- Clean sample
- Anneal at 550 °C for 10 mins using RTA in an O_2 environment to form the Al_2O_3

7. Ohmic Metallisation

- Clean sample
- Spin Microposit S1818 resist at 4000 rpm for 120 secs
- Bake on hotplate at 65 °C for 120 secs
- Soak in Microposit Concentrate:H_2O for 1 min
- Rinse in DI water
- Blow dry with N_2
- Expose using MA6 for 5 secs
- Develop with Microposit Concentrate:H_2O for 75 secs
- Rinse in DI water
- Blow dry with N_2
- Oxygen ash at 40 W for 3 mins
- De-oxidise in $4H_2O$:HCl for 1 min
- Deposit Ti/Al/Ni/Au = 30/180/40/100 nm using electron beam metal evaporator

- Soak in acetone at 50 °C for 15 mins
- Rinse in IPA for 15 secs
- Blow dry with N_2
- Anneal at 800 °C for 60 secs using RTA in an N_2 environment

8. Gate Metallisation

- Clean sample
- Spin Microposit S1805 resist at 4000 rpm for 120 secs
- Bake on hotplate at 65 °C for 120 secs
- Soak in Microposit Concentrate:H_2O for 1 min
- Rinse in DI water
- Blow dry with N_2
- Expose using MA6 for 3 secs
- Develop with Microposit Concentrate:H_2O for 75 secs
- Rinse in DI water
- Blow dry with N_2
- Oxygen ash at 40 W for 3 mins
- De-oxidise in $4H_2O$:HCl for 1 min
- Deposit Ni/Au = 20/200 nm Al using electron beam metal evaporator
- Soak in acetone at 50 °C for 15 mins
- Rinse in IPA for 15 secs
- Blow dry with N_2

9. Contact/Bondpad Metallisation

- Clean sample
- Spin Microposit S1818 resist at 4000 rpm for 120 secs
- Bake on hotplate at 65 °C for 120 secs

- Soak in Microposit Concentrate:H_2O for 1 min
- Rinse in DI water
- Blow dry with N_2
- Expose using MA6 for 5 secs
- Develop with Microposit Concentrate:H_2O for 75 secs
- Rinse in DI water
- Blow dry with N_2
- Oxygen ash at 40 W for 3 mins
- Deposit NiCr/Au = 20/200 nm Al using electron beam metal evaporator
- Soak in acetone at 50 °C for 15 mins
- Rinse in IPA for 15 secs
- Blow dry with N_2

A2. RF Devices with 0.2 and 0.5 μm Gate Length

Note: Ohmic and gate contacts steps were defined using e-beam lithography for patterning accuracy. All other fabrication steps were defined using optical lithography. Processing from step 1 *to* 6*, and the last step* 9 *are the same as previously described in A*1*.*

7. Ohmic Metallisation

- Clean sample
- Spin 12% PMMA 2010 at 5000 rpm ($\sim$ 535 nm) for 60 secs
- Bake in oven at 180 °C for 30 mins
- Spin 4% PMMA 2041 at 2000 rpm ($\sim$ 215 nm) for 60 secs
- Bake in oven at 180 °C for 90 mins
- Deposit 30 nm Al using electron beam metal evaporator

- Submit to Leica VB6 UHR EWF with a dose of 960 μCcm^{-2}, a beam current of 32 nA and a beam step size of 24 nm, variable resolution unit (VRU) of 22
- Soak in CD-26 for 5 mins
- Rinse with DI water 5 mins
- Blow dry with N_2
- Develop with 2MIBK:IPA for 45 secs at 23 °C
- Rinse in IPA for 15 secs
- Blow dry with N_2
- Oxygen ash at 40 W for 30 secs
- De-oxidise in $4H_2O$:HCl for 1 min
- Rinse with DI water for 15 secs
- Blow dry with N_2
- Deposit Ti/Al/Ni/Au = 30/180/40/100 nm using electron beam metal evaporator
- Soak in acetone at 50 °C for 15 mins
- Rinse in IPA for 15 secs
- Blow dry with N_2
- Anneal at 800 °C for 60 secs using RTA in an N_2 environment

8. Gate Metallisation

- Spin 8% PMMA 2010 at 2000 rpm ($\sim$375 nm) for 60 secs
- Bake in oven at 180 °C for 30 mins
- Spin 4% PMMA 2041 at 4000 rpm ($\sim$152 nm) for 60 secs
- Bake in oven at 180 °C for 90 mins
- Deposit 30 nm Al using electron beam metal evaporator
- Submit to Leica VB6 UHR EWF with a dose of 1426 μCcm^{-2}, a beam current of 2 nA and a beam step size of 6 nm, VRU of 2

- Soak in CD-26 for 5 mins
- Rinse with DI water for 5 mins
- Blow dry with N_2
- Develop with 2MIBK:IPA for 45 secs at 23 °C
- Rinse in IPA for 15 secs
- Blow dry with N_2
- Oxygen ash at 40 W for 30 secs
- De-oxidise in $4H_2O$:HCl for 1 min
- Rinse with DI water for 15 secs
- Blow dry with N_2
- Deposit Ni/Au = 20/200 nm using electron beam metal evaporator
- Soak in acetone at 50 °C for 15 mins
- Rinse in IPA for 15 secs
- Blow dry with N_2

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