Inherent SM Voltage Balance for Multilevel Circulant Modulation in Modular Multilevel DC-DC Converters

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***Abstract*- The modularity of a modular multilevel dc converter (MMDC) makes it attractive for medium voltage distribution systems. Inherent balance of submodule (SM) capacitor voltages is considered as an ideal property which avoids a complex sorting process based on many measurements thereby reducing costs and enhancing reliability. This paper extends the inherent balance concept previously shown for square-wave modulation to a multilevel version for MMDCs. A switching duty matrix d_U is introduced: it is a circulant matrix of preset multi-level switching patterns with multiple stages and multiple durations. Inherent voltage balance is ensured with a full-rank d_U. Circulant matrix theory shows that this is equivalent to a simplified common factor criterion. A non-full rank d_U causes clusters of SM voltage rather than a single common value, with the clusters indicated by the kernel of the matrix. A generalized co-prime criterion is developed into several deductions that serve as practical guidance for design of multilevel circulant modulation. The theoretical development is verified through full-scale simulations and down-scaled experiments. The effectiveness of the proposed circulant modulation in achieving SM voltage balance in an MMDC is demonstrated.**

***Index Terms*- Multilevel circulant modulation, inherent balance, submodule capacitor voltage, modular multilevel dc converter (MMDC)**

I. Introduction

Medium voltage dc (MVdc) technology is a promising solution that can supplement and enhance existing AC grids and thereby enable integration of greater volumes of distributed renewable energy sources, energy storage and large industrial loads. MVdc is also a way to link and coordinate existing low voltage dc (LVdc) distribution [1]-[3]. The modular multilevel dc converter (MMDC) has already become a competitive candidate among various options for dc-dc transformers that interface between the dc systems with different voltages because of its superior flexibility, scalability, and reliability [4], [5]. As an extension from an isolated dual-active bridge (DAB) or an LLC structure, the MMDC contains a medium frequency transformer as part of internal ac stage that provides isolation and facilitates high step-down ratios with enhanced power density[6], [7]. The primary, MV, side of the MMDC comprises series submodules (SMs) whereas the secondary, LV, side is either a controllable active full-bridge or a diode-based uncontrolled rectifier bridge. Therefore, the MMDC inherits the merits of both the modular multilevel converter (MMC) and the DAB (or LLC) topologies including high modularity and high efficiency.

A fundamental requirement for stable operation for an MMDC, and indeed a whole dc system, is that the SM capacitor voltages are well balanced at all times [8]. This can be achieved by allocating the SM insertion based on their position when ranked by voltage as is typically the case in MMC dc-ac conversion [9]. However, the sampling and switching frequency should be higher than the ac stage frequency to obtain a positive or negative arm current within an ac fundamental period for charging or discharging the SM capacitors, which would limit the internal ac stage frequency and decrease the power density of MMDCs. In recent studies, the SM capacitor voltages in MMDCs are regulated by the reassignment of gating signals according to the double-sorting process for both the SM capacitor voltages and their net increments during last period [10]-[13]. The ac frequency could reach the switching frequency, but it is still strictly limited by the time of sensor data communication and complex sorting computation. For both methods, the central controller should be equipped with high computing performance to realize the real-time SM capacitor voltages sampling, storing and sorting. Besides the dilemma between operating frequency and computational complexity, on the other hand, the sorting and reassigning process makes it unpredictable for the SM switching actions. Switching frequency and current stress are different for each SM, which indicates the lack of operating uniformity and leads to deviation of lifespans.

Inherent balance capability for the SM capacitor voltages is expected as an ideal characteristic to improve the operating frequency and reduce the control burden, which helps to curtail the converter implementation costs with enhanced reliability [14]. Compared with the aforementioned balance scheme basing on common sorting algorithms, the computational complexity of the inherent balance modulation significantly reduces from $O(n^2)$ to $O(1)$ where n is the SM number in one arm, which allows decentralized control with much cheaper local controllers and simplifies the expansion of SM for higher voltage application. High-speed communications, real-time SM voltage feedback and sorting-reassigning process would be unnecessary since the SM capacitor voltages are self-balanced and self-regulated. The fast but expensive field programmable gate arrays (FPGAs) can be avoided, that is always equipped in typical MMCs as the part of central controller for satisfying the high computational complexity of sorting process [15]. Further, a high ac stage frequency can be achieved without increasing any computational burden for control system and the converter could even keep working in open-loop control if some of the SM voltage sensors fail.

The balanced SM voltages under open-loop control have been observed in both MMCs [16]-[19] and MMDCs [20], [21]

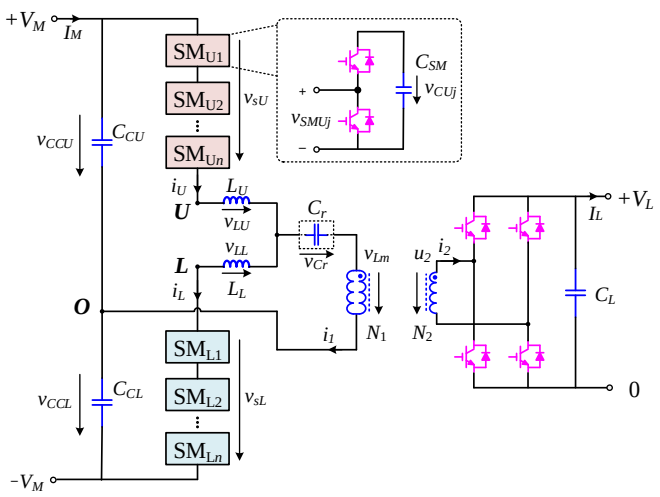

Fig. 1 Schematics of the MMDC

with rotated switching patterns. Firstly, by analyzing the steady-state operation under the pure sinusoidal ac output, the arm current of MMC is considered as the superposition of fundamental component and dc component, then SM voltages could be estimated step-by-step. The switching patterns of each SM is then decided to keep SM voltages stable with additional demands on fundamental switching frequency operation for each SM [16] or reducing the SM capacitor voltage ripple by adding switching actions [17]. However, these works could not explain the dynamic phenomena that the SMs initially with different voltages could converge to balance with switching pattern rotation [18] and the SM voltage balance would not be affected by changing operating condition or circuit parameter variation [16], [17]. Moreover, unbalanced cases have appeared in MMDC operation [22] since the waveform of arm voltage is more flexible in MMDCs aiming at soft-switching or increasing dc voltage utilization rather than simply tracing a sinewave like MMCs, which leads the harmonics in arm current non-negligible and the SM voltage estimation very complex.

Capturing the circulant feature of switching patterns, the circulant modulation is specified in [23] that each SM circularly repeats the preset switching patterns every circulant cycle, and the later SM refers the former one with a fundamental cycle lagging. The circulant matrix is then introduced to deduce the steady-state inherent balance criterion [23] and clarify the inherent converging dynamics [24] for square-wave operation. The matrix allows a more generalized and theoretical way to analyze the circulant modulation regardless of the operation condition, which effectively simplifies the SM voltage balance prediction.

However, the square-wave modulation is hardly applied in practice, for the voltage with high dv/dt is generated as the input of the internal passive ac stage. The arm inductors and the primary winding of the transformer share dv/dt stress when several SMs are simultaneously inserted or bypassed, which would shorten the lifespans of magnetic elements. Thicker insulation materials are demanded that decrease the power density and limit the heat dissipation [25]. The power losses of the transformer increase due to high-frequency harmonics, which lowers the total efficiency and further complicates the thermal design at the same time [26]. Electromagnetic interference (EMI) performance tends to deteriorate, that is also the crucial issue for the reliability and safety of MMDCs [27]. To reduce dv/dt stress for the transformer, modulation with more voltage levels is expected for the primary winding. Trapezoidal, sinusoidal and quasi-square modulation are proposed in literature for MMDCs to realize multi-level stack output [28]-[30].

So far, few studies have discussed the inherent SM voltage balance for MMDCs with multi-level operation. In this paper, a generalized multilevel circulant modulation is presented for MMDCs and proven to possess inherent balance capability under certain criteria. The preset stack switching patterns over a fundamental cycle are described state by state for a three-level circulant modulation as the simplest case, and then abstracted as a switching duty matrix $\boldsymbol{d}_U$ for a full circulant cycle. A full-rank $\boldsymbol{d}_U$ is revealed to promise the inherent balance capability, and a simplified common factor criterion is deduced through circulant matrix theory to make the condition more applicable. A non-full rank $\boldsymbol{d}_U$ is indicated causing clusters of SM voltage rather than a single common value, with the clusters identified by the kernel of the matrix. A generalized coprime criterion with several deductions is further illustrated as practical guidance for multilevel circulant modulation. Full-scale simulations and down-scaled experiments are presented for both inherently balanced cases and unbalanced cases, that validate the theoretical analysis and deduced criterion.

II. Basic Description for Modular Multilevel DC-DC Converter

As shown in Fig.1, two dc systems with different voltage levels of $\pm V_M$ and $+V_L$ are linked by the MMDC. The MVdc side of the MMDC is a single-phase MMC bridge, which contains an arm inductor and a stack with n half-bridge SMs in both the upper and the lower arm. The LVdc side is a full-bridge with a smoothing capacitor C_L connected to the LVdc bus. An ac passive stage including a medium-frequency transformer with a step-down ratio of $r_T=N_1/N_2$ is applied to link and isolate between the MVdc side and the LVdc side. The primary winding of the internal transformer is connected between the midpoint of the MMC arms and the neutral point created by the dc-link capacitor C_{CU} and C_{CL}, while the secondary winding is connected to the full bridge in the LV side. L_U and L_L are the equivalent arm inductors of the MMC arm inductor and the transformer leakage inductor, that act as the phase-shift inductor in DAB-based MMDC, while act as the resonant inductor in LLC-based MMDC. An additional resonant capacitor C_r is equipped between the midpoint of the MMC part and the transformer for the LLC-based MMDC to form the resonant tank with the equivalent arm inductors and the magnetizing inductor, that is shown in dashed box in Fig.1.

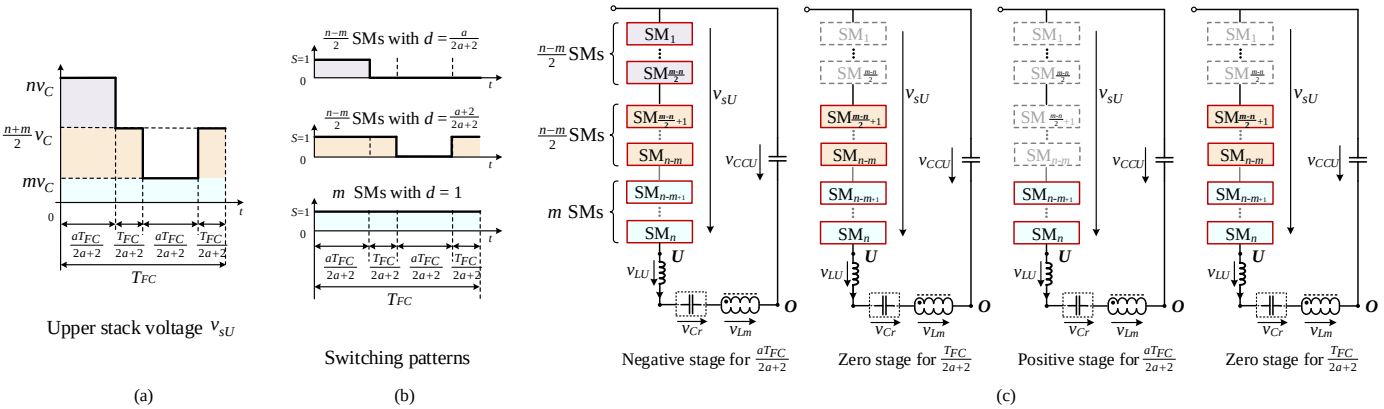

Fig. 2 Three-level voltage generation within one fundamental cycle. (a) Three-level stack voltage output (b) SM switching patterns (For each SM, S=1 means inserting the SM capacitor into the circuit, while S=0 means bypassing it from the circuit). (c) Circuits of the voltage loop of upper arm (Colored SMs means being inserted, while grey SMs means being bypassed).

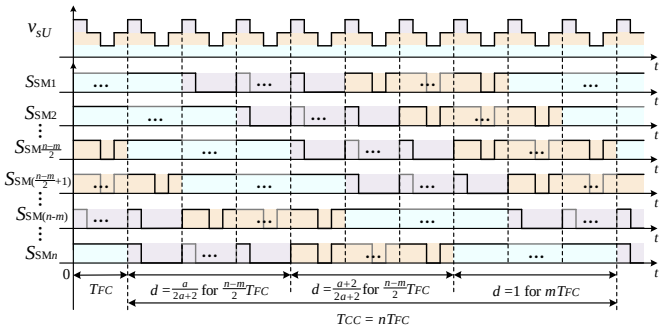

Fig. 3 Switching patterns with circulant modulation.

The ac voltage for exciting the internal ac passive stage is generated by the MMC part according to the variation of the inserted SMs in the upper and the lower arms. The ac current is equally distributed in both arms, which leads the potential of point U and point L to be the same, v_U=v_L. The upper and lower arm inductors can be considered as parallel connected from the ac side's point of view. For the DAB-based MMDC, the MMC bridge and the active full bridge should operate at the same frequency and the power flow is controlled by the phase-shift angle φ, which is the lagging angle between the primary winding voltage v_{Lm} and the stack midpoint voltage v_{UO} (or v_{LO}). For the LLC-based MMDC, the MMC bridge should work around the resonant frequency of the resonant tank to control the output power.

III. Three-level Circulant Modulation

As the simplest case of the multilevel modulation, the three-level circulant modulation is firstly illustrated as a clear example as follow. The three-level ac voltage is generated by the MMC stacks and applied to the passive stage of the MMDC. It halves dv/dt stress for the ac passive components compared with the square-wave voltage, since the maximum voltage step is less than half of dc bus voltage.

The upper stack operation within an ac fundamental cycle is shown in Fig. 2. One fundamental cycle, denoted as T_{FC}, can be divided into four stages with different inserted SM numbers. Firstly, all the n SMs are inserted in the upper arm, the stack voltage is higher than the clamping capacitor voltage. The negative stage is hence defined for v_{UO} being negative. Then, the zero stage is defined as (n+m)/2 SMs being inserted [1≤m<n-1, (n+m)/2∈$\boldsymbol{N}$*] in both the upper and lower stack. The stack voltage equals the dc-link capacitor voltage, which leads v_{UO} to be zero. After that, in the positive stage, n-m SMs are bypassed and the remaining m SMs are inserted in the upper stack, resulting the stack voltage being lower than the dc-link capacitor voltage and v_{UO} being positive. Finally, another zero stage is added to form a symmetrical voltage wave. The summation of the inserted SMs in both arms is a constant to keep the dc bus voltage and the SM capacitor voltages stable. It means that when m SMs are inserted in the upper arm during the positive stage, n SMs are inserted in the lower arm. Conversely, n SMs are inserted in the upper arm and m SMs are inserted in the lower arm during the negative stage.

Different time durations are designed for stages considering the generalization and symmetry. The length of the negative stage and the positive stage are the same, which are a times the zero stage length, where a can be an arbitrary positive value. With a larger a under a given n, m value set, the fundamental component of the MMC generated three-level voltage is magnified to improve the dc voltage utilization. According to the switching pattern and the insertion duration within one fundamental period, n SMs within one stack can be divided into 3 groups. The switching duty of the ith (i≤n) SM is known as the ratio between its inserted-state duration and the whole fundamental period, that is denoted by d_i. As shown in Fig. 2(b) and Fig. 2(c), (n-m)/2 SMs in purple are only inserted during negative stages, thus d=a/(2a+2). Another (n-m)/2 SMs in orange are bypassed during positive stages with d=(a+2)/(2a+2). The remaining m SMs in blue are inserted for the whole T_{FC}, and their switching duties are d=1.

Circulant modulation is applied to evenly distribute power losses and uniform all SMs. As shown in Fig. 3, the driving signal for each SM circularly lags behind the former SM for T_{FC}. In other words, the driving signal of the ith (i=2,3,⋯,n)

SM for the jth (j=2,3,⋯,n) fundamental cycle respects to that of the (i-1)th SM for the (j-1)th fundamental cycle, and the first SM follows the last SM. For a specific SM, the driving signal of the (j+n)th fundamental cycle is same as the jth one, which shows the circularity of the circulant modulation. Full circulant cycle is hence defined as T_{CC}=nT_{FC}, which is the cycle for a SM rotating back to the initial switching state.

For the n SMs in one stack within each fundamental cycle, m SMs keep inserted and the other n-m SMs should switch once. Thus the average switching period for the SM is defined as $T_{SW}=\frac{n}{n-m}T_{FC}$, which means that the switching frequency is lower than the fundamental frequency.

Take the upper arm as an example for detailed analysis. According to the Kirchoff voltage law (KVL), the voltage loop of the upper arm can be expressed as (1) during each of the stages for the first fundamental cycle

$$v_{UO}=v_{CCU}-v_{sU}=v_{CCU}-\boldsymbol{S}_{x1U}\cdot\boldsymbol{v}_{CU}^{T}\ \ (x=n,z,p) \tag{1}$$

where v_{CCU}, v_{sU} and v_{UO} are the instantaneous voltage of the upper dc-link capacitor, the upper stack and the ac passive stage. Considering that the ac passive stage consists of the equivalent arm inductors and the transformer for the DAB-based MMDC, v_{UO}=v_{LU}+v_{Lm}. For the LLC-based MMDC, v_{UO}=v_{LU}+v_{Lm}+v_{Cr} with an additional resonant capacitor included. $\boldsymbol{v}_{CU}$=[v_{CU1} v_{CU2} ⋯ v_{CUn}] and $\boldsymbol{S}_{x1U}$=[S_{x11} S_{x12} ⋯ S_{x1n}] are both n-dimensional vector, whose elements indicate the instantaneous capacitor voltages and the switching states of each SM in the upper stack, respectively. $\boldsymbol{S}_{n1U}$, $\boldsymbol{S}_{z1U}$ and $\boldsymbol{S}_{p1U}$ are defined as the switching vector of the upper stack for the negative stage, the zero stage and the positive stage for the first fundamental cycle, respectively.

The voltage loop of the upper arm is show in Fig. 2(c) for each stage of the first fundamental cycle. The corresponding switching vector is shown in (2) respectively as

$$\begin{aligned}\boldsymbol{S}_{n1U}&=[\overbrace{1\,1\cdots1\,1}^{(n-m)/2}\ \overbrace{1\,1\cdots1\,1}^{(n-m)/2}\ \overbrace{11\cdots11}^{m}]\\ \boldsymbol{S}_{z1U}&=[\overbrace{00\cdots00}^{(n-m)/2}\ \overbrace{1\,1\cdots1\,1}^{(n-m)/2}\ \overbrace{11\cdots11}^{m}]\\ \boldsymbol{S}_{p1U}&=[\overbrace{00\cdots00}^{(n-m)/2}\ \overbrace{00\cdots00}^{(n-m)/2}\ \overbrace{11\cdots11}^{m}]\end{aligned} \tag{2}$$

The element of 1 or 0 in $\boldsymbol{S}_{x1U}$ denotes that the SM capacitor is inserted into or bypassed from the conducting circuit, respectively. For the first fundamental cycle, $\boldsymbol{S}_{n1U}$ denotes that all the n SMs are inserted for the negative stage. $\boldsymbol{S}_{z1U}$ indicates that the first (n-m)/2 SMs are bypassed for the following zero stage, while the last (n+m)/2 SM keep their inserted state. $\boldsymbol{S}_{p1U}$ represents that another (n-m)/2 SMs are bypassed for the positive stage, while the remaining last m SMs are inserted. For the final zero stage, the switching vector is back to $\boldsymbol{S}_{z1U}$.

According to the definition of SM's switching duty mentioned above, the switching duty vector of the upper stack for the first fundamental cycle can be derived as

$$\begin{aligned}\boldsymbol{d}_{1U}&=\frac{a}{2a+2}\boldsymbol{S}_{n1U}+\frac{2}{2a+2}\boldsymbol{S}_{z1U}+\frac{a}{2a+2}\boldsymbol{S}_{p1U}\\&=[\overbrace{D_1\,D_1\cdots D_1\,D_1}^{(n-m)/2}\ \overbrace{D_2\,D_2\cdots D_2\,D_2}^{(n-m)/2}\ \overbrace{D_3\,D_3\cdots D_3\,D_3}^{m}]\end{aligned} \tag{3}$$

where D_1=a/(2a+2), D_2=(a+2)/(2a+2) and D_3=1. It should be emphasized that with the proposed modulation method, the switching duty vector can not only indicate the SMs' insertion duration but also fully represent the switching patterns of the stack, since SMs with same switching duty share the completely identical switching actions within the fundamental cycle.

For the following n fundamental cycles within a full circulation cycle, the voltage relationship for the upper arm can be always expressed as (1) but with different switching vectors denoted as $\boldsymbol{S}_{xiU}$ (i=1,2,⋯,n). The preset switching sequence is determined by the circulant modulation as illustrated in Fig. 3.

For the second fundamental cycle, the switching vectors $\boldsymbol{S}_{x2U}$ can be derived from $\boldsymbol{S}_{x1U}$ with a circular shift of each element, which means that the switching state (1 or 0) of the former SM in $\boldsymbol{S}_{x1U}$ is assigned to the later SM in $\boldsymbol{S}_{x2U}$, and the first element in $\boldsymbol{S}_{x2U}$ is same with the last element in $\boldsymbol{S}_{x1U}$, i.e., $\boldsymbol{S}_{n2U}$ is still an all-one vector, $\boldsymbol{S}_{p2U}=[\overbrace{10\cdots00}^{(n-m)/2}\ \overbrace{00\cdots00}^{(n-m)/2}\ \overbrace{01\cdots11}^{m}]$ and $\boldsymbol{S}_{z2U}=[\overbrace{10\cdots00}^{(n-m)/2}\ \overbrace{01\cdots11}^{(n-m)/2}\ \overbrace{11\cdots11}^{m}]$. The switching duty vector for the second fundamental cycle can be calculated according to its definition, or it can be also derived by rotating the elements in $\boldsymbol{d}_{1U}$, that is

$$\boldsymbol{d}_{2U}=[\overbrace{D_3\,D_1\cdots D_1\,D_1}^{(n-m)/2}\ \overbrace{D_1\,D_2\cdots D_2\,D_2}^{(n-m)/2}\ \overbrace{D_2\,D_3\cdots D_3\,D_3}^{m}] \tag{4}$$

Since the stack contains n SMs and correspondingly, switching vectors contain n elements, the nth fundamental cycle is the last one within a full circulation. The switching vectors of it can be obtained by shifting the elements in $\boldsymbol{S}_{x1U}$ for n-1 times, that can be written as $\boldsymbol{S}_{nnU}=[\overbrace{1\,1\cdots1\,1}^{n}]$ for the negative stage, $\boldsymbol{S}_{pnU}=[\overbrace{00\cdots00}^{(n-m)/2}\ \overbrace{00\cdots01}^{(n-m)/2}\ \overbrace{11\cdots10}^{m}]$ for the positive stage and $\boldsymbol{S}_{znU}=[\overbrace{00\cdots01}^{(n-m)/2}\ \overbrace{11\cdots11}^{(n-m)/2}\ \overbrace{11\cdots10}^{m}]$ for the zero stage. Thus, the switching duty vector of the last fundamental cycle is obtained as $\boldsymbol{d}_{nU}=[\overbrace{D_1\,D_1\cdots D_1\,D_2}^{(n-m)/2}\ \overbrace{D_2\,D_2\cdots D_2\,D_3}^{(n-m)/2}\ \overbrace{D_3\,D_3\cdots D_3\,D_1}^{m}]$. With another shift, the switching vectors and the switching duty vector will be back to the initial state as $\boldsymbol{S}_{x1U}$ and $\boldsymbol{d}_{1U}$, and a new circulation starts then.

In steady-state operation, the fundamental cycle is the operating cycle for the internal ac stage, thus the integral of v_{UO} over T_{FC} is zero. Furthermore, compared with their normal value, the voltage fluctuation is fairly small for the dc-link capacitor C_{CU} and C_{CL}, thus the instantaneous voltage values v_{CCU} in (1) can be approximated by the average value V_{CCU}=V_M at any time. The SM capacitor voltage difference between stages within one fundamental cycle can be also neglected since the stage periods are quite short. Thus, it can

be derived from (1) that SM capacitor voltages are regulated by the switching patterns and the bus voltage, which is written as

$$\begin{aligned} V_M &= \frac{1}{T_{FC}}\int_0^{T_{FC}} \boldsymbol{S}_{\boldsymbol{x1U}} \cdot \bar{\boldsymbol{v}}_{\boldsymbol{C1U}}^{\boldsymbol{T}} dt \\ &= (\frac{a}{2a+2}\boldsymbol{S}_{\boldsymbol{n1U}} + \frac{2}{2a+2}\boldsymbol{S}_{\boldsymbol{z1U}} + \frac{a}{2a+2}\boldsymbol{S}_{\boldsymbol{p1U}}) \cdot \bar{\boldsymbol{v}}_{\boldsymbol{C1U}}^{\boldsymbol{T}} = \boldsymbol{d}_{\boldsymbol{1U}} \cdot \bar{\boldsymbol{v}}_{\boldsymbol{C1U}}^{\boldsymbol{T}} \end{aligned} \tag{5}$$

where $\bar{\boldsymbol{v}}_{\boldsymbol{C1U}} = [\bar{v}_{C1U1}\ \bar{v}_{C1U2} \cdots \bar{v}_{C1Un}]$ is the vector of average SM capacitor voltages for the first fundamental cycle. For the following fundamental cycles, similar voltage equations can be obtained with a corresponding switching duty vector.

The circulant cycle is the operation cycle for the SM capacitors. The average SM capacitor voltages over each circulant cycle, denoted as $\bar{\boldsymbol{v}}_{\boldsymbol{CU}} = [\bar{v}_{CU1}\ \bar{v}_{CU2} \cdots \bar{v}_{CUn}]$, keep constant in steady state. Considering that the fundamental frequency of the MMDC reaches several kilohertz and the number of the total SMs in a stack are usually no more than dozens, the circulant cycle is short and the SM capacitor voltage ripple within T_{CC} is also small, $\bar{\boldsymbol{v}}_{\boldsymbol{C1U}}$ in (5) can be further approximated by $\bar{\boldsymbol{v}}_{\boldsymbol{CU}}$. Thus, all the voltage equations for each fundamental cycle can be integrated by a linear equation set as

$$\boldsymbol{d}_{\boldsymbol{U}} \cdot \bar{\boldsymbol{v}}_{\boldsymbol{CU}}^{\boldsymbol{T}} = [V_M\ \ V_M \cdots V_M]^T \tag{6}$$

where $\boldsymbol{d}_{\boldsymbol{U}}$ is the switching duty matrix for the circulant cycle, which fully represents the stack switching patterns determined by the circulant modulation and is written as

$$\boldsymbol{d}_{\boldsymbol{U}} = \begin{bmatrix} \boldsymbol{d}_{\boldsymbol{1U}} \\ \boldsymbol{d}_{\boldsymbol{2U}} \\ \vdots \\ \boldsymbol{d}_{\boldsymbol{nU}} \end{bmatrix} = \begin{bmatrix} \overbrace{D_1\ D_1 \cdots D_1\ D_1}^{(n-m)/2} & \overbrace{D_2\ D_2 \cdots D_2\ D_2}^{(n-m)/2} & \overbrace{D_3\ D_3 \cdots D_3\ D_3}^{m} \\ D_3\ D_1 \cdots D_1\ D_1 & D_1\ D_2 \cdots D_2\ D_2 & D_2\ D_3 \cdots D_3\ D_3 \\ \vdots & \vdots & \vdots \\ D_1\ D_1 \cdots D_1\ D_2 & D_2\ D_2 \cdots D_2\ D_3 & D_3\ D_3 \cdots D_3\ D_1 \end{bmatrix} \tag{7}$$

$\bar{\boldsymbol{v}}_{\boldsymbol{CU}}$ can be calculated by the linear equation set in (6). The solution of $\bar{\boldsymbol{v}}_{\boldsymbol{CU}}$ represents the steady state average voltage of each SM capacitor. If the elements in $\bar{\boldsymbol{v}}_{\boldsymbol{CU}}$ are the same, it means that the capacitor voltages are inherently balanced relying on the preset circulant modulation. Otherwise, capacitor voltages stand at different values and additional feedback control is demanded at any time to keep SM voltage balanced.

IV. Inherent Balance Capability

The switching patterns for the circulant modulation and the steady-state SM capacitor voltages are abstracted by the set of linear equations in (6). According to the theory of linear algebra, the solution of variable vector is determined by the coefficient matrix, which means that $\bar{\boldsymbol{v}}_{\boldsymbol{CU}}$ is decided by the switching duty matrix $\boldsymbol{d}_{\boldsymbol{U}}$ here. If the solution is unique with equal elements, the MMDC is said to have inherent balance capability. By investigating the rank of $\boldsymbol{d}_{\boldsymbol{U}}$, the condition of inherent balance capability for the circulant modulation is revealed as follow.

A. Full Rank and Complete Circulation

For a n-dimensional linear equations set expressed as $\boldsymbol{Ax}=\boldsymbol{b}$, where $\boldsymbol{A}$ is an $n \times n$ coefficient matrix, $\boldsymbol{x}$ is a column vector involving n variables and $\boldsymbol{b}$ is a given column vector, the unique solution can be gotten if and only if the coefficient matrix $\boldsymbol{A}$ is full rank [31]. This full-rank condition promises the linear independence for all the n row vectors in $\boldsymbol{A}$, which gives a complete constraint for the n variables.

For the voltage equation set in (6), the sufficient and necessary condition for the n-dimensional variable vector $\bar{\boldsymbol{v}}_{\boldsymbol{CU}}$ to get a unique solution is that the rank of the switching duty matrix equals n, which can be expressed as

$$\mathrm{rank}(\boldsymbol{d}_{\boldsymbol{U}}) = n \tag{8}$$

Since each row vector of $\boldsymbol{d}_{\boldsymbol{U}}$ represents the switching pattern for one fundamental cycle, a full-rank $\boldsymbol{d}_{\boldsymbol{U}}$ indicates that n switching patterns for n fundamental cycles within one full circulation cycle are linearly independent and irreplaceable. None of them is the repetition or linear combination of each other, which guarantees the steady-state SM capacitor voltages are fully constrained by the switching actions.

Furthermore, noting that $\boldsymbol{d}_{\boldsymbol{U}}$ determined by circulant modulation is a circulant matrix, whose elements of each row are identical to those of the previous row but are moved one position to the right and wrapped around, the solution of SM capacitor voltages should be rotationally symmetrical. Thus, as long as the unique solution exists, elements in the capacitor voltage vector $\bar{\boldsymbol{v}}_{\boldsymbol{CU}}$ should be the same

$$\bar{v}_{CU1} = \bar{v}_{CU2} = \cdots = \bar{v}_{CUn} = \frac{2V_M}{m+n} \tag{9}$$

It means that the inherent balance of average capacitor voltages is realized. The full-rank $\boldsymbol{d}_{\boldsymbol{U}}$ provides a complete rotation of the SMs, thus the SM voltages would be inherently balanced by the circulant modulation if the balance criterion is satisfied, which could be considered that the SM capacitors are equally and separately clamped by the dc bus capacitor. The circulant modulation directly and strongly constrains the SM voltages with open-loop control, while voltage feedback, sorting and choosing are unnecessary.

On the contrary, if $\mathrm{rank}(\boldsymbol{d}_{\boldsymbol{U}}) \neq n$, precisely $\mathrm{rank}(\boldsymbol{d}_{\boldsymbol{U}}) < n$, $\boldsymbol{d}_{\boldsymbol{U}}$ has linearly dependent row vectors. Although there are still n switching patterns within a circulation cycle, one or some of them can be replaced by others. The rotation is not complete and the energy cannot be evenly shared between SMs. The SM capacitor voltages in steady state are decided by the initial state and hardware parameters, that will not be well balanced by circulant modulation.

B. Simplified Mathematical Criterion

The inherent balance condition based on the circulant modulation is theoretically described by (8), but a simpler criterion is expected to guide the practical design. Since $\boldsymbol{d}_{\boldsymbol{U}}$ is determined by n and m, the full-rank property can be reclarified by the relationship between n and m.

According to the circulant matrix theory [32], an n-dimensional circulant matrix $\boldsymbol{C}$ can be expressed by the full-rank Vandermonde matrix $\boldsymbol{V}$ as

$$\begin{aligned}\boldsymbol{C} &= \begin{bmatrix} a_1 & a_2 & a_3 & \cdots & a_{n-1} & a_n \\ a_n & a_1 & a_2 & \cdots & a_{n-2} & a_{n-1} \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ a_2 & a_3 & a_4 & \cdots & a_n & a_1 \end{bmatrix} \\ &= \begin{bmatrix} 1 & 1 & \dots & 1 \\ \omega_0 & \omega_1 & \dots & \omega_{n-1} \\ \omega_0^2 & \omega_1^2 & \cdots & \omega_{n-1}^2 \\ \vdots & \vdots & \ddots & \vdots \\ \omega_0^{n-1} & \omega_1^{n-1} & \cdots & \omega_{n-1}^{n-1} \end{bmatrix} \cdot \begin{bmatrix} \lambda_0 & 0 & 0 & \cdots & 0 \\ 0 & \lambda_1 & 0 & \cdots & 0 \\ 0 & 0 & \lambda_2 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & \lambda_{n-1} \end{bmatrix} \cdot \begin{bmatrix} 1 & 1 & \dots & 1 \\ \omega_0 & \omega_1 & \dots & \omega_{n-1} \\ \omega_0^2 & \omega_1^2 & \cdots & \omega_{n-1}^2 \\ \vdots & \vdots & \ddots & \vdots \\ \omega_0^{n-1} & \omega_1^{n-1} & \cdots & \omega_{n-1}^{n-1} \end{bmatrix}^{-1} \\ &= \boldsymbol{V} \cdot \mathrm{diag}(\lambda_0, \lambda_1, \lambda_2, \cdots, \lambda_{n-1}) \cdot \boldsymbol{V}^{-1} \end{aligned} \tag{10}$$

where $\lambda_k = \sum_{q=1}^{n} a_q \omega_k^{q-1}$, $k = 0,1,\cdots,n-1$, which are n eigenvalues of $\boldsymbol{C}$; $\omega_k = e^{i2\pi\cdot\frac{k}{n}}$, which are the nth roots of unity ($\omega_k^n = 1$) and i is the imaginary unit ($i^2=-1$). Since $\boldsymbol{V}$ is a full-rank matrix, $\boldsymbol{C}$ is similar to diag(λ_0, λ_1,$\cdots$, λ_{n-1}) and has the same rank with this diagonal matrix. Thus, $\boldsymbol{C}$ will be a full-rank matrix if and only if all eigenvalues are nonzero, otherwise, the rank of $\boldsymbol{C}$ equals the number of nonzero eigenvalues among λ_0, λ_1, $\cdots$, λ_{n-1}.

For the circulant matrix $\boldsymbol{d}_U$, the eigenvalues can be expressed as

$$\begin{aligned}\lambda_k &= a_1 + a_2\omega_k + a_3\omega_k^2 + \cdots + a_n\omega_k^{n-1} \\ &= D_1 + D_1\omega_k + \cdots + D_1\omega_k^{\frac{n-m}{2}-1} + D_2\omega_k^{\frac{n-m}{2}} + \cdots + D_2\omega_k^{n-m-1} + D_3\omega_k^{n-m} + \cdots + D_3\omega_k^{n-1} \end{aligned} \tag{11}$$

For the first eigenvalue, it can be always calculated that $\omega_k = e^{i2\pi\cdot\frac{k}{n}} = e^0 = 1$, then $\lambda_0 = (m+n)/2 \neq 0$, which is a nonzero eigenvalue. When $k\neq 0$, $\omega_k \neq 1$, other eigenvalues can be calculated as

$$\begin{aligned}\lambda_k &= D_1 + D_1\omega_k + \cdots + D_1\omega_k^{\frac{n-m}{2}-1} + D_2\omega_k^{\frac{n-m}{2}} + \cdots + D_2\omega_k^{n-m-1} + D_3\omega_k^{n-m} + \cdots + D_3\omega_k^{n-1} \\ &= D_1\frac{1-\omega_k^n}{1-\omega_k} + (D_2 - D_1)\cdot\frac{1-\omega_k^{\frac{n+m}{2}}}{1-\omega_k} + (D_3 - D_2 - D_1)\cdot\frac{1-\omega_k^m}{1-\omega_k} \\ &= \frac{1}{2(a+1)}\cdot\frac{1-e^{i2\pi\cdot\frac{n+m}{2n}k}}{1-\omega_k} + \frac{a}{2(a+1)}\cdot\frac{1-e^{i2\pi\cdot\frac{m}{n}k}}{1-\omega_k} \qquad (k = 1,2,3,\cdots,n-1) \end{aligned} \tag{12}$$

If a k can be found to make $\frac{n+m}{2n}k$ and $\frac{m}{n}k$ being integer at the same time, the corresponding eigenvalue λ_k could be zero, and the rank of switching duty matrix is less than n. The inherent balance capability is absent with this circulant modulation.

The greatest common divisor of n, m and $\frac{n+m}{2}$, denoted as g=gcd(n, m, $\frac{n+m}{2}$), is introduced here to identify the existence of zero eigenvalue. If g>1, the eigenvalue $\lambda_{n/g}$ equals 0 since $\frac{n+m}{2n}k = \frac{(n+m)/2}{g}$ and $\frac{m}{n}k = \frac{m}{g}$ are integers together, which leads rank($\boldsymbol{d}_U$)<n. On the contrary, if g=1, although k_1 can be found as gcd(n, $\frac{n+m}{2}$) or its prime factors and k_2 can be found as gcd(n, m) or its prime factors to let the former or latter part in (12) to be zero separately, k_1 and k_2 have no intersection set to get a zero eigenvalue.

Therefore, the full-rank condition in (8) of inherent balance can be simplified as

$$\gcd(n, m, \frac{n+m}{2}) = 1 \tag{13}$$

Since the condition in (13) only relates to n and m, while a is irrelevant to the matrix rank, it indicates that the specific switching duty length has no effect on the balance feature. As long as the number of the inserted SMs during each of the stages have no common factor larger than 1, n independent switching patterns are completely circulated and energy equally flows among each SM. The circulant modulation guarantees the inherent balance capability of SM capacitor voltages. It promises a self-regulated open-loop control instead of feedback and sorting processes by the central controller.

C. Kernel and Cluster

The inherent balance property is lost for the circulant modulation with a non-full rank switching duty matrix. To obtain the whole picture of the circulant modulation, how the capacitor voltages splitting in steady state for these unbalanced cases is revealed as follow by further exploring the kernel of switching duty matrix.

Generally, the complete solution of a linear equation set $\boldsymbol{Ax}=\boldsymbol{b}$ can be expressed as $\boldsymbol{x}=\boldsymbol{x}^g+\boldsymbol{x}^*$, where $\boldsymbol{x}^g$ is the general solution satisfying the corresponding homogeneous equation set $\boldsymbol{Ax}=\boldsymbol{0}$, while $\boldsymbol{x}^*$ is the particular solution satisfying $\boldsymbol{Ax}=\boldsymbol{b}$. The set of all the general solutions is defined as the kernel of $\boldsymbol{A}$, which can be expressed as ker($\boldsymbol{A}$)={$\boldsymbol{x}$: $\boldsymbol{Ax}=\boldsymbol{0}$}. The rank-nullity theorem [33] is introduced here to clarify the relationship between the rank of $\boldsymbol{A}$ and the dimension of its kernel, which is

$$\mathrm{rank}(\boldsymbol{A}) + \mathrm{nullity}(\boldsymbol{A}) = n \tag{14}$$

where nullity($\boldsymbol{A}$)=dim(ker($\boldsymbol{A}$)), i.e., the nullity of $\boldsymbol{A}$ is the dimension of ker($\boldsymbol{A}$).

Therefore, for the equation set with a full-rank coefficient matrix, nullity($\boldsymbol{A}$) equals 0. The general solution can be only the zero vector, namely, $\boldsymbol{x}^g=\boldsymbol{0}$, hence the particular solution $\boldsymbol{x}^*$ is the single solution to $\boldsymbol{Ax}=\boldsymbol{b}$. For rank($\boldsymbol{A}$)<$n$ and nullity($\boldsymbol{A}$)>0, numerous nonzero general solution vectors exist for $\boldsymbol{Ax}=\boldsymbol{0}$. Then the complete solution losses the uniqueness and numerous solutions can be found for this equation set with the constrain of $\boldsymbol{A}$.

Focus back on the SM capacitor voltages solved by the linear equations in (6). If the switching duty matrix is full-rank, the voltages are fully regulated by the switching patterns and the dc bus. From the equation set's point of view, the general solution to $\boldsymbol{d}_U \cdot \bar{\boldsymbol{v}}_{CU}^T = \boldsymbol{0}$ only contains the zero vector. The particular solution can be always obtained as (9), which is also the complete solution that indicates the inherent balance capability. On the contrary, with g=gcd(n, m, $\frac{n+m}{2}$)>1, (g-1)

zero eigenvalues can be found as $\lambda_{n/g}$, $\lambda_{2n/g}$, ⋯, $\lambda_{(g-1)n/g}$ for $\boldsymbol{d}_U$, while other eigenvalues are nonzero. Thus, rank($\boldsymbol{d}_U$)=n-(g-1) and nullity($\boldsymbol{d}_U$)=g-1≠0, the switching patterns expressed by $\boldsymbol{d}_U$ can only provide n-(g-1) independent constraints for n SM in one stack, which implies that (g-1) independent solution vectors can be found for $\bar{\boldsymbol{v}}_{CU}^T$ satisfying $\boldsymbol{d}_U \cdot \bar{\boldsymbol{v}}_{CU}^T = \boldsymbol{0}$. The switching patterns provide incomplete constrains for the SM capacitor voltages, which leads to the SM voltages clustering.

A group of independent general solution vectors can be readily obtained for (6) according to the circulant feature of the switching duty matrix and the rotational symmetry of the solution, that are expressed by the kernel of $\boldsymbol{d}_U$ in (15) as an n×(g-1) matrix. Since the nullity of $\boldsymbol{d}_U$ is (g-1), all of other possible solution vectors can be represented by the linear combination of the column vectors in ker($\boldsymbol{d}_U$), that indicate the same relation of the voltage variables.

$$\ker(\boldsymbol{d}_U) = \begin{bmatrix} \boldsymbol{Z}_1 \\ \boldsymbol{Z}_2 \\ \vdots \\ \boldsymbol{Z}_{n/g} \end{bmatrix}_{n\times(g-1)} \tag{15}$$

$$\text{where } \boldsymbol{Z}_1 = \boldsymbol{Z}_2 = \cdots = \boldsymbol{Z}_{n/g} = \begin{bmatrix} z_1 & 0 & 0 & 0 \\ 0 & z_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & z_{g-1} \\ -z_1 & -z_2 & \cdots & -z_{g-1} \end{bmatrix}_{g\times(g-1)},$$

z_1, z_2, ⋯, z_{g-1} are independent constants. The general solution to $\boldsymbol{d}_U \cdot \bar{\boldsymbol{v}}_{CU}^T = \boldsymbol{0}$ is obtained according to the column vectors of the kernel in (15) as

$$\begin{cases} \bar{v}_{CU1}^g = \bar{v}_{CU(g+1)}^g = \bar{v}_{CU(2g+1)}^g = \cdots = \bar{v}_{CU(n-g+1)}^g = z_1 \\ \bar{v}_{CU2}^g = \bar{v}_{CU(g+2)}^g = \bar{v}_{CU(2g+2)}^g = \cdots = \bar{v}_{CU(n-g+2)}^g = z_2 \\ \cdots \\ \bar{v}_{g-1}^g = \bar{v}_{CU(2g-1)}^g = \bar{v}_{CU(3g-1)}^g = \cdots = \bar{v}_{CU(n-1)}^g = z_{g-1} \\ \bar{v}_{CUg}^g = \bar{v}_{CU(2g)}^g = \bar{v}_{CU(3g)}^g = \cdots = \bar{v}_{CUn}^g = -\sum_{i=1}^{g-1} z_i \end{cases} \tag{16}$$

Finally, the complete solution of the voltage equation set in (6) is shown in (17), that has a similar structure with its general solution but is amended by the particular solution correlated with the bus voltage.

$$\begin{cases} \bar{v}_{CU1} = \bar{v}_{CU(g+1)} = \bar{v}_{CU(2g+1)} = \cdots = \bar{v}_{CU(n-g+1)} = v_1 \\ \bar{v}_{CU2} = \bar{v}_{CU(g+2)} = \bar{v}_{CU(2g+2)} = \cdots = \bar{v}_{CU(n-g+2)} = v_2 \\ \cdots \\ \bar{v}_{CUg-1} = \bar{v}_{CU(2g-1)} = \bar{v}_{CU(3g-1)} = \cdots = \bar{v}_{CU(n-1)} = v_{g-1} \\ \bar{v}_{CUg} = \bar{v}_{CU(2g)} = \bar{v}_{CU(3g)} = \cdots = \bar{v}_{CUn} = \frac{2g}{n+m} V_M - \sum_{i=1}^{g-1} v_i \end{cases} \tag{17}$$

where v_1, v_2, ⋯, v_{g-1} are also a group of independent constants. $v_i = z_i + \frac{2}{n+m} V_M$ (i=1, 2, ⋯ , g-1), which is the summation of the general solution z_i and the particular solution $\frac{2}{n+m} V_M$. Although these independent constants could be v_1=v_2=⋯=v_{g-1} = $\frac{2}{n+m} V_M$ by chance indicating that the SM voltages are balanced at the same value, theoretically, v_1, v_2, ⋯, v_{g-1} could be arbitrary value only with the limit of DC bus voltage if the inherent balance criteria are unsatisfied. The steady-state SM voltages of each cluster would vary, which are affected by their initial voltages, the SM capacitance variation and the operating point including switching frequency and load condition, et. al. The lack of uniformity of SMs would lead to over-voltage for the SM with a higher voltage and shorten the lifespan of the whole converter.

Therefore, for the number of inserted SMs in the positive stage, the zero stage and the negative stage being m, $\frac{n+m}{2}$ and n, as long as the greatest common devisor g of m, $\frac{n+m}{2}$ and n is larger than 1, the g-1 dimensional kernel of $\boldsymbol{d}_U$ indicates that (g-1) independent solution vectors can be found for the steady-state capacitor voltages. Considering the circulant switching patterns and the practical circuits, the SM would evenly split into g clusters. Only the n/g SMs included in one cluster are fully circulated and equally share the energy flow, which leads the voltages of them to be the same. The SMs in different clusters may have different voltages and the inherent balance capability is absent in steady state with these preset circulant switching patterns.

D. Examples

According to the previous analysis, by introducing the circulant switching duty matrix $\boldsymbol{d}_U$ to describe the circulant switching patterns, a series of inherent balance criteria are derived for arbitrary total SM number or operating condition by analyzing the rank of $\boldsymbol{d}_U$, and the clustering feature is also clarified for unbalanced cases by the matrix kernel. The switching patterns of all the SMs in one stack for a circulant cycle could be considered as a whole to generate the desired voltage with the inherent balance capability identified, which avoids complicated arm current estimation and switching pattern calculation one-by-one for each SM and case-by-case for each operating point.

For example, the inherent balance feature of the SM capacitor voltages can be predicted in the specific cases as follow. For an upper stack with 6 SMs, the number of inserted SM in the positive stage can be assigned as m=2 or m=4 to obtain an integer for (m+n)/2.

If n=6, m=4 and (n+m)/2=5, the SM capacitor voltage equation set for a circulant cycle can be written as (18). The switching duty matrix is calculated with a=4 in this specific case as a representative, while the value of a has no effect on the inherent balance feature as analysis above.

$$\begin{bmatrix} 1 & 1 & 1 & 1 & 3/5 & 2/5 \\ 2/5 & 1 & 1 & 1 & 1 & 3/5 \\ 3/5 & 2/5 & 1 & 1 & 1 & 1 \\ 1 & 3/5 & 2/5 & 1 & 1 & 1 \\ 1 & 1 & 3/5 & 2/5 & 1 & 1 \\ 1 & 1 & 1 & 3/5 & 2/5 & 1 \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{CU1} \\ \bar{v}_{CU2} \\ \bar{v}_{CU3} \\ \bar{v}_{CU4} \\ \bar{v}_{CU5} \\ \bar{v}_{CU6} \end{bmatrix} = \begin{bmatrix} V_M \\ V_M \\ V_M \\ V_M \\ V_M \\ V_M \end{bmatrix} \tag{18}$$

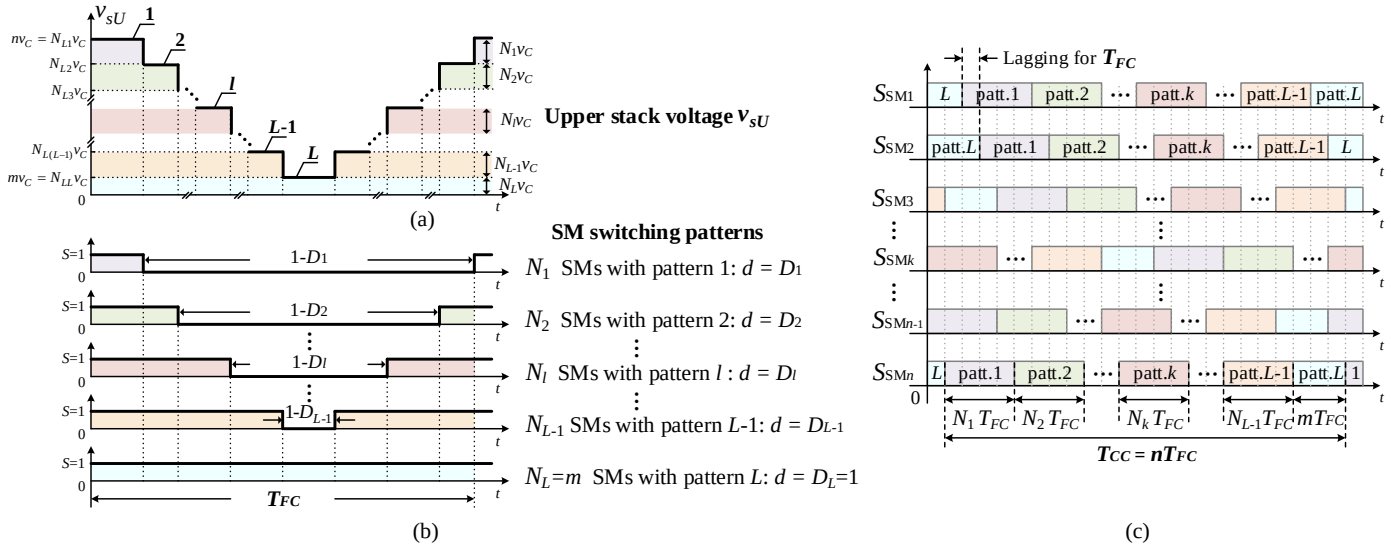

Fig. 4 Multilevel circulant modulation. (a) Multilevel stack voltage within one fundamental cycle. (b) Switching patterns of SMs within one fundamental cycle. (c) Switching patterns of SMs with switching state circulation within one circulant cycle

Since no common factor other than 1 can be found for n, m and $(n+m)/2$, all the n eigenvalues of $\boldsymbol{d}_U$ are nonzero, hence rank($\boldsymbol{d}_U$)=6. The switching patterns for each fundamental cycle within one circulant cycle are linearly independent. Thus, the SM capacitor voltages are inherently balanced by the circulant modulation. Clamped by the upper capacitor C_{CU} and calculated from (9), the steady-state average voltages of upper stack SM capacitors equally settle at the value of

$$\overline{v}_{CU1} = \overline{v}_{CU2} = \cdots = \overline{v}_{CU6} = \frac{1}{5}V_M \tag{19}$$

However, with n=6, m=2, $(n+m)/2$=4 and a=4, the voltage equation set for a circulant cycle can be given as

$$\begin{bmatrix} 1 & 1 & \frac{3}{5} & \frac{3}{5} & \frac{2}{5} & \frac{2}{5} \\ \frac{2}{5} & 1 & 1 & \frac{3}{5} & \frac{3}{5} & \frac{2}{5} \\ \frac{2}{5} & \frac{2}{5} & 1 & 1 & \frac{3}{5} & \frac{3}{5} \\ \frac{3}{5} & \frac{2}{5} & \frac{2}{5} & 1 & 1 & \frac{3}{5} \\ \frac{3}{5} & \frac{3}{5} & \frac{2}{5} & \frac{2}{5} & 1 & 1 \\ 1 & \frac{3}{5} & \frac{3}{5} & \frac{2}{5} & \frac{2}{5} & 1 \end{bmatrix} \cdot \begin{bmatrix} \overline{v}_{CU1} \\ \overline{v}_{CU2} \\ \overline{v}_{CU3} \\ \overline{v}_{CU4} \\ \overline{v}_{CU5} \\ \overline{v}_{CU6} \end{bmatrix} = \begin{bmatrix} V_M \\ V_M \\ V_M \\ V_M \\ V_M \\ V_M \end{bmatrix} \tag{20}$$

The greatest common devisor of n, m and $(n+m)/2$ is 2. The eigenvalue λ_3 of the switching duty matrix equals 0 and thus rank($\boldsymbol{d}_U$)=5<n, nullity($\boldsymbol{d}_U$)=1. Linear dependent switching patterns exist in the circulant modulation and the energy circulates incompletely between SMs. The steady-state voltages of SM capacitors vary according to different initial states or circuit parameters, but it can be concluded that the SM capacitor voltages will split into 2 clusters with 3 SMs in each cluster as

$$\begin{cases} \overline{v}_{CU1} = \overline{v}_{CU3} = \overline{v}_{CU5} = v_1 \\ \overline{v}_{CU2} = \overline{v}_{CU4} = \overline{v}_{CU6} = \frac{1}{2}V_M - v_1 \end{cases} \tag{21}$$

where v_1 is an arbitrary value within the range of 0 to $\frac{1}{2}V_M$. Although v_1 could be $\frac{1}{4}V_M$ to make all SM capacitor voltages settling at the same value, the balance relies on the equal initial state of each SM and the perfectly consistent circuit parameters. The SM capacitor voltages cannot converge automatically with the circulant modulation. The inherent balance capability should be also considered as absence.

V. Multilevel Circulant Modulation and Generalized Coprime Criterion

The L-level ($1<L\le n+1$) circulant modulation is illustrated in Fig. 4. For a fundamental cycle T_{FC}, the stack voltage and the corresponding SM switching patterns are shown in Fig. 4(a) and Fig. 4(b), respectively. For a full circulant cycle T_{CC} including n fundamental cycles, the circulant switching patterns for each SM are shown in Fig. 4(c). Colors are used for identifying the specific switching patterns within the fundamental cycle in each subgraph.

Taking the upper stack as an example, the stack generates the L-level voltage within one fundamental cycle. For the first level, all the n SMs in the upper arm are inserted into the circuit. For the second level, N_1 SMs are bypassed from the circuit, and for the following lth ($2<l<L$) level, another N_{l-1} SMs are bypassed successively. Finally, for the Lth level, after N_{L-1} SMs are bypassed, the remaining m SMs ($m\ge1$) are still inserted while n-m SMs are bypassed. The lower stack works complementarily with the upper stack to keep the summation of inserted SMs in both arm being a constant.

To generate the L-level stack voltage, n SMs in the upper arm operate with L kinds of switching patterns within a fundamental cycle. N_1 SMs sharing the switching pattern 1 in purple are only inserted during the first level with the switching duty d=D_1. For the another N_2, N_3, ⋯, N_{L-1} SMs respectively sharing the identical switching pattern 2, pattern 3,

…, pattern L-1, they are bypassed from the circuit at the end of the 2nd, 3rd, …, (L-1)th level and inserted back into the circuit at the beginning of corresponding level within one fundamental cycle. Thus, the switching duty of them are D_2, D_3, …, $D_{L\text{-}1}$, respectively. The remaining N_L=m SMs in blue are inserted for the whole fundamental cycle, namely their switching duty d=D_L=1. It should be noted that the switching duty d here can fully represent the switching pattern, since the SM with the same d shares the same switching pattern. Although it can be set that $N_1 \neq N_2 \neq \cdots \neq N_{L\text{-}1}$ and $D_1 \neq D_2 \neq \cdots \neq D_{L\text{-}1}$ to generate an arbitrary L-level wave, considering the symmetry of the voltage output, the first and the (L-1)th level, the second and the (L-2)th level and so on usually share the same SM number and have the complementary switching duty, namely, $N_l = N_{L\text{-}l}$, $D_l + D_{L\text{-}l} = 1$ (l =1,2, …, L-1).

The presented multilevel circulant modulation shows its generality that the preset switching patterns are generated only according to the stack voltage command. This feature well adapts to MMDCs that the internal ac stage voltage could be more flexible than that in MMCs. Typical operation mode of MMDC including quasi-square-wave, trapezoidal, triangle and sinusoidal operation can be freely implemented with self-regulated SM voltage under open-loop control. According to the driving signal allocation of each SM in Fig.4, for example, adding the following constraints to the patterns can realize trapezoidal operation for the MMDC: $N_1 = N_2 = \cdots = N_{L\text{-}1}$, D_1=1-$D_{L\text{-}1}$, $D_l - D_{l\text{-}1} = D_{l+1} - D_l$ (l =2, …, L-2) and the mid-point of bypassed (or inserted) duration for each SM are the same. Moreover, if further restrict that $D_{l+1} - D_l$ (l =1, …, L-2) is much shorter than D_1 or 1-$D_{L\text{-}1}$, it can be viewed as quasi-square-wave operation. Then, the following analyses and criteria can be applied to identify that the SM capacitor voltages would be inherently balanced or not under the circulant modulation.

As shown in Fig. 4(c), circulant modulation is applied to allocate the stack switching patterns for fundamental cycles. For each fundamental cycle, the stack keeps generating this L-level voltage as long as there are N_1 SMs operating with switching pattern 1, N_2 SMs operating with switching pattern 2, …, $N_{L\text{-}1}$ SMs operating with switching pattern L-1 and m SM operating with switching pattern L. In the first fundamental cycle T_{FC1}, the first N_1 SMs colored in purple operate with switching pattern 1, the (N_1+1)th to the (N_1+N_2)th SM colored in green operate with switching pattern 2, and the $(\sum_{i=1}^{l-1} N_i + 1)$ th to the $(\sum_{i=1}^{l} N_i)$ th SM colored in red operate with switching pattern l and so on. The last m SMs are colored in blue, which represents that they operate with switching pattern L and d=1. Thus, similar to the analysis for three-level modulation, the switching duty vector of the upper stack for the first fundamental cycle can be written as

$$\boldsymbol{d}_{1U} = [\overbrace{D_1 \cdots D_1}^{N_1} \ \overbrace{D_2 \cdots D_2}^{N_2} \ \cdots \ \overbrace{D_l \cdots D_l}^{N_l} \ \cdots \ \overbrace{1 \cdots 1}^{m}] \tag{22}$$

The driving signal of the later SM refers the former SM with one T_{FC} lagging according to the circulant modulation. The switching duty vectors for each following fundamental cycle can be obtained by shifting the line elements of that of the former T_{FC}. Since there are n SMs in one stack and n elements in one switching duty vector, the full circulant cycle contains n fundamental cycles, namely T_{CC}=nT_{FC}. Within one circulant cycle, each SM operates with pattern L for mT_{FC} and operates with other patterns for (n-m)T_{FC}. Thus, the SM switch n-m time within T_{CC}, namely $T_{SW} = \frac{n}{n-m} T_{FC}$. It means that the SM switching frequency is $f_{SW} = \frac{n-m}{n} f_{FC}$, which is always lower than (or equal to, if and only if m=0) the fundamental frequency. All the switching actions are necessary for stack voltage shaping and balancing without any ineffective actions. Considering that the internal stage frequency in MMDCs is much higher than that in MMCs, the reduced switching frequency would contribute a lot to improve the efficiency.

The switching duty matrix of the L-level modulation for the full circulant cycle can be obtained as an n×n matrix as

$$\boldsymbol{d}_U = \begin{bmatrix} \boldsymbol{d}_{1U} \\ \boldsymbol{d}_{2U} \\ \vdots \\ \boldsymbol{d}_{nU} \end{bmatrix} = \begin{bmatrix} \overbrace{D_1\ D_1 \cdots D_1\ D_1}^{N_1} & \overbrace{D_2\ D_2 \cdots D_2\ D_2}^{N_2} & \cdots & \overbrace{D_l\ D_l \cdots D_l\ D_l}^{N_l} & \cdots & \overbrace{1\,1 \cdots 1\,1}^{m} \\ 1\ D_1 \cdots D_1\ D_1 & D_1\ D_2 \cdots D_2\ D_2 & \cdots & D_{l-1}\ D_l \cdots D_l\ D_l & \cdots & D_l\ 1 \cdots 1\,1 \\ \vdots & \vdots & & \vdots & & \vdots \\ D_1\ D_1 \cdots D_1\ D_2 & D_2\ D_2 \cdots D_2\ D_3 & \cdots & D_l\ D_l \cdots D_l\ D_{l+1} & \cdots & 1\,1 \cdots 1\ D_1 \end{bmatrix} \tag{23}$$

With the rational simplification of neglecting the voltage ripple of dc-link capacitors and SM capacitors within one circulant cycle, the average SM capacitor voltage $\bar{\boldsymbol{v}}_{\boldsymbol{CU}}$ is constrained by the linear voltage equation set in (6). The inherent balance capability is still guaranteed by the circulant modulation with a full-rank switching duty matrix $\boldsymbol{d}_U$ as clarified in (8), and the balanced capacitor voltages keep $\frac{2V_M}{n+m}$ as (9).

To obtain the inherent balance capability for the L-level circulant modulation, namely a full-rank $\boldsymbol{d}_U$, n non-zero eigenvalues are expected. Simplification and practical guidance can be derived basing on the circulant matrix theories. The eigenvalues of the circulant matrix $\boldsymbol{d}_U$ can be calculated as

$$\begin{aligned} \lambda_k = {} & D_1(1 + \omega_k + \cdots + \omega_k^{N_1-1}) + D_2(\omega_k^{N_1} + \cdots + \omega_k^{N_1+N_2-1}) + \cdots \\ & + D_l(\omega_k^{N_1+\cdots+N_{l-1}} + \cdots + \omega_k^{N_1+\cdots+N_l-1}) + \cdots + (\omega_k^{N_1+\cdots+N_{L-1}} + \cdots + \omega_k^{n-1}) \\ & (k = 0,1,2\cdots,n-1) \end{aligned} \tag{24}$$

The first eigenvalue must a non-zero eigenvalue since ω_0=1, $\lambda_0 = \sum_{i=1}^{L} D_i N_i \neq 0$. Regardless of the specific value of D_1, D_2, …, D_L, it can be always obtained that D_1<D_2<…<D_L according to the modulation design. Therefore, when k≠0, ω_k≠1, other eigenvalues can be calculated as

$$\begin{aligned} \lambda_k = {} & D_1 \frac{1-\omega_k^n}{1-\omega_k} + (D_2 - D_1) \cdot \frac{1-\omega_k^{n-N_1}}{1-\omega_k} + \cdots + (D_{l+1} - \textstyle\sum_{i=1}^{l} D_i) \cdot \frac{1-\omega_k^{n-\sum_{i=1}^{l} N_i}}{1-\omega_k} \\ & + \cdots + (1 - \textstyle\sum_{i=1}^{L-1} D_i) \cdot \frac{1-\omega_k^{n-\sum_{i=1}^{L-1} N_i}}{1-\omega_k} \qquad (k = 1,2,3,\cdots,n-1) \end{aligned} \tag{25}$$

Similar to the analysis for the three-level circulant modulation, it can be derived from (25) that if the greatest common divisor of n, n-N_1, …, $n - \sum_{i=1}^{L-1} N_i$ is 1, no zero eigenvalue exists and the switching duty matrix is full-rank, then the SM capacitor voltages are inherently balanced.

TABLE I
EXAMPLE CASES OF INHERENT BALANCE CAPABILITY FOR MULTILEVEL CIRCULANT MODULATION

Case	n	m	L	N_h	(N_{L1}, N_{L2}, ⋯, N_{LL})	Rank of $\boldsymbol{d}_U$	Balanced or not	Description
1	5	1	4	N/A	(5,4,2,1)	5	Balanced	Example of (26), gcd(N_{L1}, N_{L2}, ⋯, N_{LL})=1
2	10	2	4	N/A	(10,8,4,2)	9	Unbalanced	Contrasting example of (26), gcd(N_{L1}, N_{L2}, ⋯, N_{LL})=2
3	6	4	3	1	(6,5,4)	6	Balanced	Example of (28), gcd(n,N_h)=1, N_h=1
4	6	2	3	2	(6,4,2)	5	Unbalanced	Contrasting example of (28), gcd(n,N_h)=2
5	6	0	7	1	(6,5,4,3,2,1,0)	6	Balanced	Example of N_h=1, m=0
6	6	0	3	3	(6,3,0)	4	Unbalanced	Example of N_h≠1, m=0

Considering the practical meaning of above values, the inherent balance criterion of the L-level circulant modulation can be concluded that the numbers of inserted SMs in each stack voltage level have no common factor larger than 1, and is expressed as

$$\gcd(N_{L1}, N_{L2}, \cdots, N_{LL}) = 1 \tag{26}$$

where N_{L1}, N_{L2}, ⋯, N_{LL} are the number of inserted SMs in the first, second, ⋯, Lth voltage level, and $N_{L1}=n>0$, $N_{L2}=n-N_1>0$, ⋯, $N_{LL}= n-\sum_{i=1}^{L-1} N_i =m>0$. Since the criterion is only related to the inserted numbers rather than the switching duty D_1, D_2, ⋯, D_L, the duration of each level have no effect on the inherent balance capability.

On the contrary, if the greatest common divisor g=gcd(N_{L1},N_{L2},⋯,N_{LL}) is larger than 1, (g-1) zero eigenvalues can be found as $\lambda_{n/g}$, $\lambda_{2n/g}$, ⋯, $\lambda_{(g-1)n/g}$ for $\boldsymbol{d}_U$. Thus, $\boldsymbol{d}_U$ would be a non-full rank matrix with rank($\boldsymbol{d}_U$)=n-(g-1) and nullity($\boldsymbol{d}_U$)=g-1. The voltage equation set for multilevel modulation would get the same solution with three-level modulation as (17), which illustrates that the SMs would split into g clusters with different average capacitor voltages in steady state. Specifically, only the ith, (g+i)th, (2g+i)th, ⋯, (n-g+i)th (i=1,2,⋯,g) SM in the same cluster would be fully circulated and equally share the energy flow to promise the same capacitor voltage, while the SMs in different clusters may have different voltages. That is to say, the circulant modulation losses its inherent balance capability in these cases.

According to (26), balanced example and unbalanced contrasting example are listed as case 1 and case 2 in TABLE I, respectively. With the equal dc bus voltage, the stack output voltages are identical for case 1 and case 2. But for case 1, the inserted SM numbers of each level have no common factor other than 1, the rank of the switching duty matrix is equal to the total SM number of the stack. Thus, the SM capacitor voltages are inherently balanced. For case 2, 2 is the greatest common divisor of each voltage level, thus rank($\boldsymbol{d}_U$)=9<n. The SM capacitor voltages tend to split into 2 clusters with the 1st, 3rd,5th, 7th and 9th SM in the same cluster while other SMs in another cluster with different steady-state voltage. The inherent balance capability of the circulant modulation is absent.

As the analysis for the three-level modulation above, the height of each voltage level usually sets to be identical to keep the symmetry, namely, $N_1=N_2=\cdots=N_{L-1}=N_h$, where N_h is the height of the voltage level. N_h can be represented by n, m and L as

$$N_h = \frac{n-m}{L-1}, \quad N_h \in \boldsymbol{N}^* \tag{27}$$

Then, the inserted SM numbers of each level are $N_{L1}=n$, $N_{L2}=n-N_h$, ⋯, $N_{LL}=n-(L-1)N_h=m$, that are an arithmetic progression with common difference of $-N_h$. Thus, the greatest common divisor of N_{L1}, N_{L2}, ⋯, N_{LL} equals that of n and N_h. The L-level inherent balance criterion in (26) can be further simplified as a generalized coprime criterion

$$\gcd(n, N_h) = 1 \tag{28}$$

As long as the height of voltage level and the total SM number are coprime, the inherent balance capability is obtained for the L-level circulant modulation. This criterion concludes the solutions in [23] and (13) for two-level and three-level circulant modulation. In [23], n and m should be coprime, where n and m are the inserted SM number of negative stage and positive stage for the square-wave stack voltage, respectively. The height of the voltage level is n-m. Since gcd(n, n-m)=gcd(n, m), if n and n-m are coprime, the inherent balance capability is guaranteed. In (13), n, (n+m)/2 and m are the inserted SM numbers of each stage, and the height of voltage level is (n-m)/2. The inherent balance capability or the voltage clustering characteristic can be also predicted by gcd(n, $\frac{n-m}{2}$), since it is equal to gcd(n, $\frac{n+m}{2}$,m). Balanced example and unbalanced contrasting example of (28) are listed as case 3 and case 4 in TABLE I, respectively. The detailed analyses from the rank's point of view have been conducted in Part D, Section IV. The same conclusion can be drawn according to this coprime criterion.

If only one SM is inserted into or bypassed from the circuit at the same time, namely N_h=1, the dv/dt stress of the passive stage is minimized and the MMC part fully takes its advantage of multilevel voltage output ability. For this specific case, the SM capacitor voltages are inherently balanced with the circulant modulation, since the height of voltage level is 1, and gcd(n, N_h)=gcd(n,1)=1 with any D_1, D_2, ⋯, D_L, or m. Case 3 in TABLE I can be also considered as an balanced example of this conclusion.

Another special case is that all the n SMs in the stack are bypassed during the Lth level. Although there are still L levels for the stack voltage, only (L-1) switching patterns exist while the pattern L is lost. $N_{LL}=m$ can be considered as 0, which makes it inapplicable for (26) to identify the inherent balance capability, since 0 is not coprime with any value. In fact, it should be back to (25), and the final term of the right polynomial is zero. The inherent balance capability is

identified by the inserted SM number of other levels. For the heights of each level are identical, (28) is still applicable with the missing pattern L. In fact, it can be concluded that for cases of m=0, the inherent balance capability only exists when N_h=1. Otherwise, gcd(N_{L1},N_{L2},⋯,N_{LL})=gcd(n,N_h)=N_h>1, which leads to unbalancing and clustering. For the case 5 and case 6 in TABLE I, they shares the same n and m=0. When N_h=1 in case 5, the switching duty matrix is full-rank and the SM capacitor voltages are fully regulated by the circulant switching patterns. The inherent balance capability of the circulant modulation is present. When N_h=3 in case 6, gcd(N_{L1},N_{L2})=gcd(n,N_h)=N_h=3, rank($\boldsymbol{d}_U$)=4, which leads to the SM capacitor voltages splitting into 3 clusters. The inherent balance capability of the circulant modulation is lost.

In conclusion, a series of criteria are exposed to identify the inherent balance capability of the multilevel circulant modulation for MMDC in this section. Beginning with the full-rank criterion in (8), it is applied to any circulant modulation since the switching duty matrix $\boldsymbol{d}_U$ is directly derived from the voltage equations. Then, the full-rank feature of $\boldsymbol{d}_U$ is specified as (26) by calculating the matrix eigenvalues that the inserted SM number in each voltage level have the common factor larger than 1. This criterion is more intuitive for guiding design than relying on the rank, but it specifies the SM inserting sequence as Fig. 4. Finally, The generalized coprime criterion in (28) may provide the direction of optimal design with both practicability and flexibility. For the cases with equal magnitude of each voltage level, so long as the number of inserted SMs in each voltage step is coprime with the total SM number in one stack, the circulant modulation promises the inherent balance of all SM voltages. Two deductions are also provided for N_h=1 and m=0 cases as a more specified footnote. Considering from the converter design, another approach is to choose a prime number as the total SM number in an arm. The inherent balance criteria in (8), (26) or (28) will be always satisfied regardless of the inserted SM number of each voltage level.

VI. Simulation Results

Both the LLC-based and DAB-based MMDC simulation models are built in the MATLAB/Simulink environment with the parameters listed in TABLE II to verify the multilevel circulant modulation and the inherent balance criterion. To indicate the balancing capability that is independent to the circuit topology, hardware parameters or initial state, the SM capacitances are set with 10% variation and the initial voltages of each SM capacitor are set to be unbalanced for all cases in both models. The theoretical predictions of case 3 to case 6 in TABLE I are respectively validated by simulation results in Fig. 5 to Fig. 8 with LLC-based MMDC and Fig. 9(a) to (d) with DAB-based MMDC.

Simulation results of operating with n=6, m=4, L=3 and N_h=1 are presented in Fig. 5. The upper stack voltage and the 6 SM driving signals are shown in Fig. 5(a). All SMs equally switch with a preset circular pattern yet the latter SM action lags behind the former one for one fundamental cycle T_{FC}. For each T_{FC}, only 2 SMs switch once while the remaining 4 SMs keep inserted in the circuit. Within one circulant cycle T_{CC}=6T_{FC}, each SM is bypassed twice. Thus the switching frequency f_{sw} of each SM equals $\frac{1}{3} f_{FC}$, where f_{sw} equals 1/T_{sw}. The upper stack voltage in Fig. 5(b) is generated according to this preset switching patterns. For the positive stage, two SMs are bypassed from the circuit and for the zero stage, one SM is bypassed. The lower stack operates complimentarily with half fundamental cycle shift of SM switching patterns. In Fig. 5(c), it shows that a three-level voltage is generated by the MMC part as the excitation of ac passive stage. Each voltage step is half of the peak-to-peak value of stack voltage. The resonant current flows through the transformer and will be rectified by the diode bridge in LVdc side. As shown in Fig. 5 (d), the proposed circulant modulation shows its robustness that the SM voltages can converge to balance even if the SM voltages begin with the severe unbalance. The inherent balance capability for SM capacitor voltages is obtained since the inserted SM numbers of each voltage level, i.e., n, m, (n+m)/2 have no common factor other than 1 in this case, or it can be directly decided by N_h=1. Although the SM voltages are different at the beginning, they all equally settle at 1.1kV as VM/5 in steady-state due to the circulant modulation, which verifies the prediction in (19). The LV side output dc voltage can be controlled by adjusting the fundamental frequency as typical LLC convertors or changing the stage length ratio a in this three-level modulation. The inherent balance capability will not be affected by these operating parameters. In this case, the fundamental frequency is set as 4kHz that is near the resonant frequency, and a is set as 4.

Simulation results of operating with n=6, m=2, L=3, N_h=2 and n=6, m=0, L=3, N_h=3 are respectively presented in Fig. 6 and Fig. 7 as unbalanced cases but with different clustering characters. It illustrates in Fig. 6(a) that for the case of m=2, 4 SMs switch once within one fundamental cycle. Each SM switches 4 times within one circulant cycle and the SM switching frequency can be calculated as $\frac{2}{3} f_{FC}$. For the m=0 case, all SM switch once within each T_{FC} as shown in Fig. 7(a), thus f_{SW}=f_{FC}. The upper and lower stack voltages and currents are shown in Fig. 6(b) and Fig. 7(b), and the three-level voltage in Fig. 6(c) and Fig. 7(c) excites the ac passive stage

TABLE II
Simulation parameters of MMDCs

Parameters	Descriptions	Values
n	SM number per stack	6
$2V_M$	MV side bus voltage	11kV
V_L	Minimum LV side bus voltage	300V
C_{CU}, C_{CL}	Medium-side dc-link capacitance	550μF
C_L	Low-side output capacitance	5mF
L_P,L_L	Equivalent arm inductance	3.2mH
C_r	Resonant capacitance	1μF
L_m	Magnetizing inductance	60.8mH
C_{SM}	SM capacitance	500μF (±10% variation)
r_T	Transformer turns-ratio	3:1
f_{ac}	AC stage frequency	4kHz
S	Power devices	FF450R33T3E3

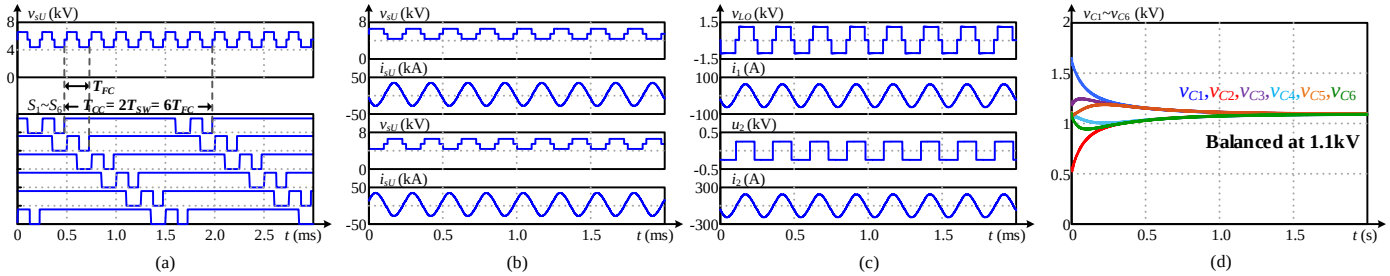

Fig. 5 Simulation results of n=6, m=4, L=3, N_h=1 as a balanced case for LLC-based MMDC. (a) Steady-state upper stack voltage and upper stack SM driving signals. (b) Steady-state voltages and currents of upper and lower stack. (c) Steady-state voltages and currents of input and output side of ac passive stage. (d) Dynamic SM capacitor voltages of upper stack.

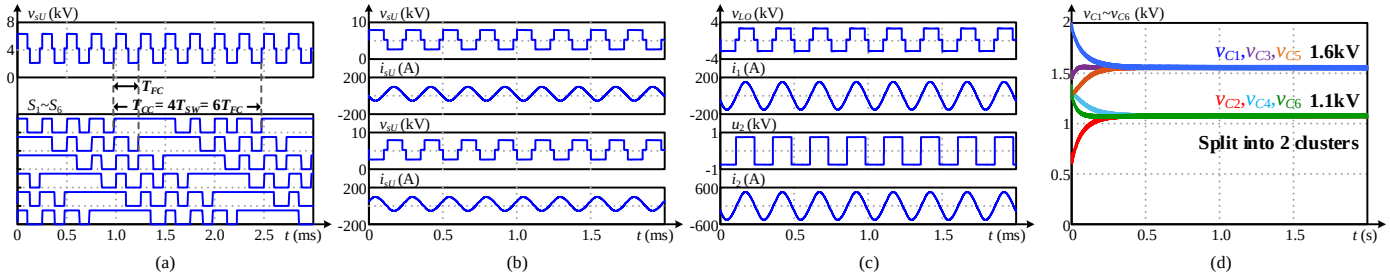

Fig. 6 Simulation results of n=6, m=2, L=3, N_h=2 as an unbalanced case with SM capacitor voltages splitting into 2 clusters for LLC-based MMDC. (a) Steady-state upper stack voltage and upper stack SM driving signals. (b) Steady-state voltages and currents of upper and lower stack. (c) Steady-state voltages and currents of input and output side of ac passive stage. (d) Dynamic SM capacitor voltages of upper stack.

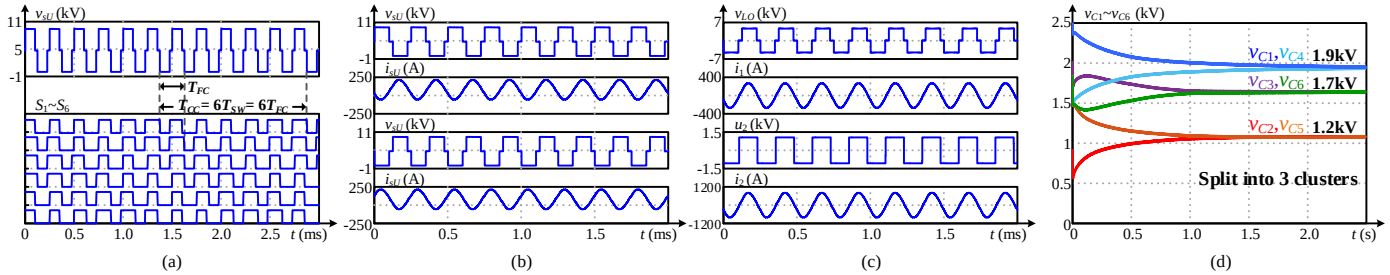

Fig. 7 Simulation results of n=6, m=0, L=3, N_h=3 as an unbalanced case with SM capacitor voltages splitting into 3 clusters for LLC-based MMDC. (a) Steady-state upper stack voltage and upper stack SM driving signals. (b) Steady-state voltages and currents of upper and lower stack. (c) Steady-state voltages and currents of input and output side of ac passive stage. (d) Dynamic SM capacitor voltages of upper stack.

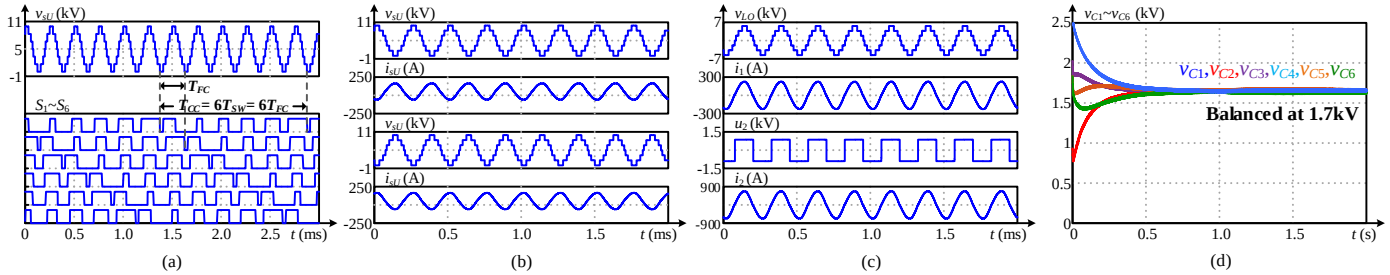

Fig. 8 Simulation results of n=6, m=0, L=7, N_h=1 as a balanced case for LLC-based MMDC. (a) Steady-state upper stack voltage and upper stack SM driving signals. (b) Steady-state voltages and currents of upper and lower stack. (c) Steady-state voltages and currents of input and output side of ac passive stage. (d) Dynamic SM capacitor voltages of upper stack.

as the former case. However, because gcd(m, $\frac{n+m}{2}$,n)>1 for these two cases, SM capacitor voltages cannot be inherently balanced by the preset circulant modulation. For the m=2 case, the greatest common factor equals N_h as 2. Fig. 6(d) illustrates that the SM capacitor voltages split into 2 clusters as the theoretical prediction in (21). The voltage difference among SM capacitors is about 30% of their average reference value. For the m=0 case, Fig. 7(d) indicates that the SM capacitor voltages split into 3 clusters since N_h=3. The highest SM capacitor voltage is 60% higher than that of the lowest one.

Simulation results of operating with n=6, m=0, L=7, N_h=1 are shown in Fig. 8. Each SM is inserted and bypassed one by

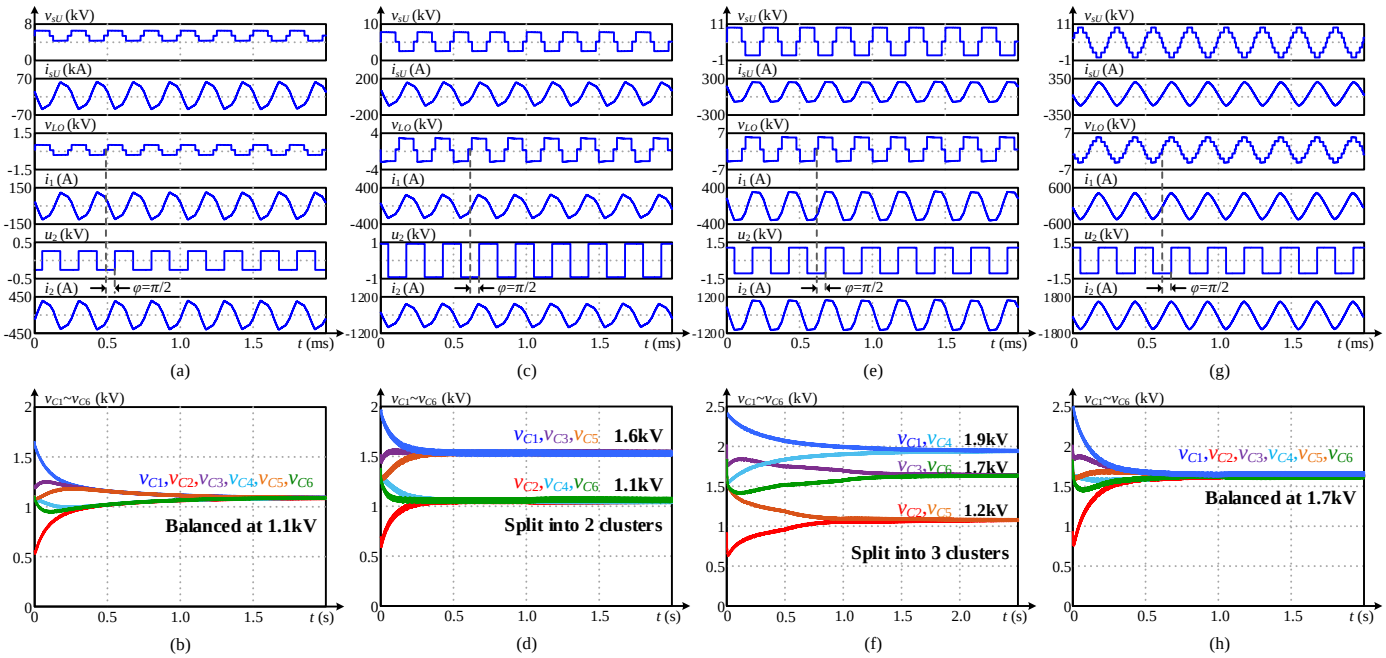

Fig. 9 Simulation results of DAB-based MMDC. (a) and (b) with n=6, m=4, L=3, N_h=1. (c) and (d) with n=6, m=2, L=3, N_h=2. (e) and (f) with n=6, m=0, L=3, N_h=3. (g) and (h) with n=6, m=0, L=7, N_h=1. (a), (c), (e) and (g) shows the steady-state voltages and currents of upper stack, and input and output side of ac passive stage. (b), (d), (f) and (h) shows the dynamic upper stack SM capacitor voltages.

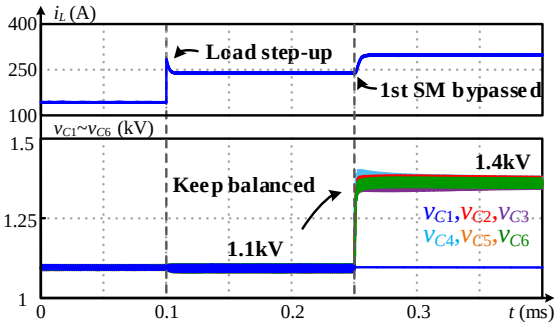

Fig. 10 Simulation results of dynamic robustness with load step-up and single faulty SM bypassed.

one within a fundamental cycle, thus f_{SW}=f_{FC}. A seven-level voltage is generated by the stacks to excite the passive ac stage, and the dv/dt stress is minimized. Since the height of the voltage level equals 1, namely N_h=1, all the SM capacitor voltages are inherently balanced by the circulant modulation, that shares the voltage of 1.7kV. The length of each voltage level are different in this simulation, which has no effect on the inherent balance capability.

The same cases are conducted on the DAB-based MMDC model as shown in Fig. 9. The phase-shift angle, that is the lagging angle of the transformer voltage u_2 and stack output voltage v_{LO}, can be adjusted to control the power flow as typical DABs, is set as φ=π/2 to reach the maximum power output in this system. Same switching patterns are respectively allocated to the SMs for each case on this DAB-based MMDC, and the stack voltages are the same for the both topologies. However, the stack currents and the ac stage currents vary for different circuit topology. It slightly effects the dynamic response of SM capacitor voltages from the initial state, but it has no effect on the convergence or the clustering characters of their steady-state average values. As illustrated in Fig. 9(b), (d) and (f), the SM capacitor voltages converge to the balanced value for N_h=1 case, split into 2 clusters for N_h=2 case and split into 3 clusters for N_h=3 case, respectively. For the seven-level modulation with N_h=1 in Fig. 9(h), the inherent balance capability is also guaranteed.

To provide a broader validation of the dynamic robustness for the inherently balanced circulant modulation, simulation results of the SM voltage response after load step-up on LVdc side and single SM bypassed for fault are shown in Fig. 10. An LLC-based MMDC begins operating with n=6, m=4, L=3, N_h=1 as the balanced case in Fig. 5. The load steps at t=0.1ms and it can be observed that the LV side output current increases with a transient process, while all the SM capacitor voltages keep well balanced for the whole period. The SM voltage ripple tends to enlarge after the load step-up since it is proportional to load current. But all the SMs evenly share the energy fluctuation regardless of the load condition, which keeps limiting the capacitor voltage ripple within a reasonable range. Considering the fault-tolerant design of MMDC, the converter could keep operating with a single bypassed SM for fault. As shown in Fig. 10 at t=0.25ms, the first SM in stack is bypassed and the remaining 5 SMs could keep operation with the circulant modulation. The converter would operate with n=5, m=3, L=3, N_h=1 that is still a balanced case. Since there are less SM sharing the dc bus voltage, the capacitor voltages of working SM tend to increase together from 1.1kV to 1.4kV while the bypassed faulty SM keeps the capacitor voltage

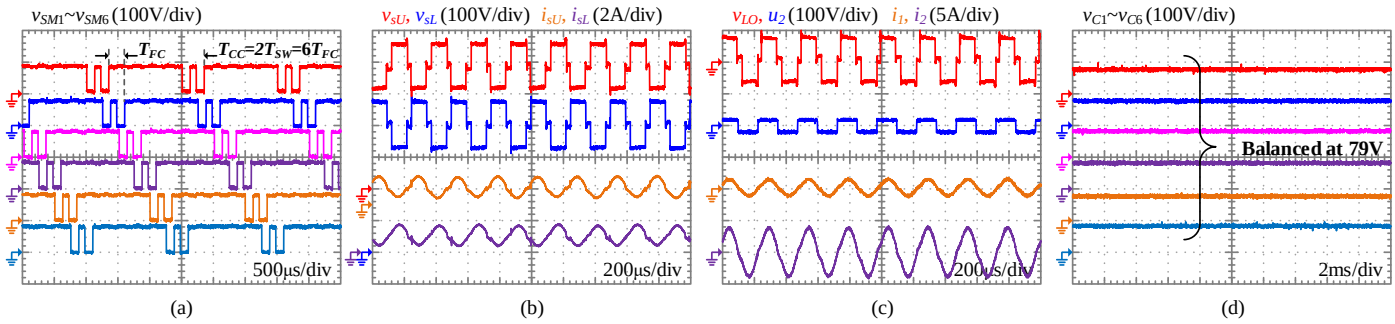

Fig. 11 Experimental results with n=6, m=4, L=3, N_h=1 as an inherently balanced case (a) SM output voltages in upper stack. (b) Voltages and currents of upper and lower stack. (c) Voltages and currents of input and output side of ac passive stage. (d) SM capacitor voltages of upper stack.

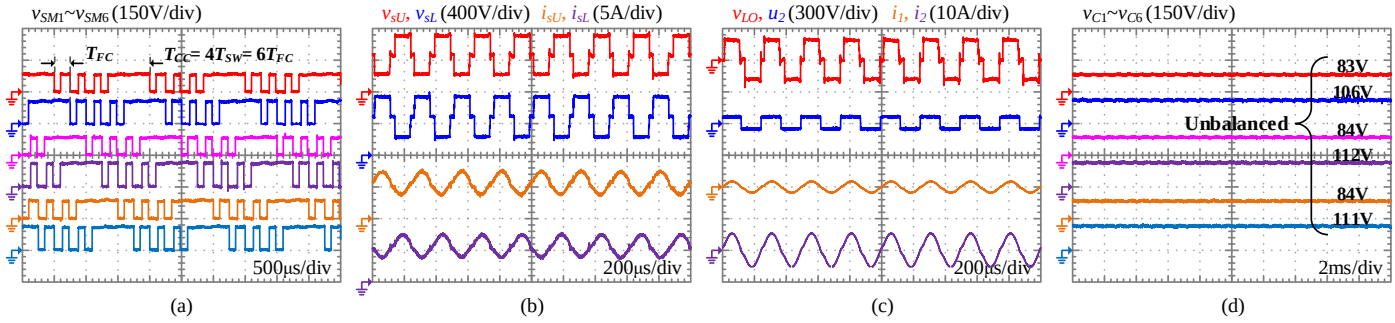

Fig. 12 Experimental results with n=6, m=2, L=3, N_h=2 as an unbalanced case (a) SM output voltages in upper stack. (b) Voltages and currents of upper and lower stack. (c) Voltages and currents of input and output side of ac passive stage. (d) SM capacitor voltages of upper stack.

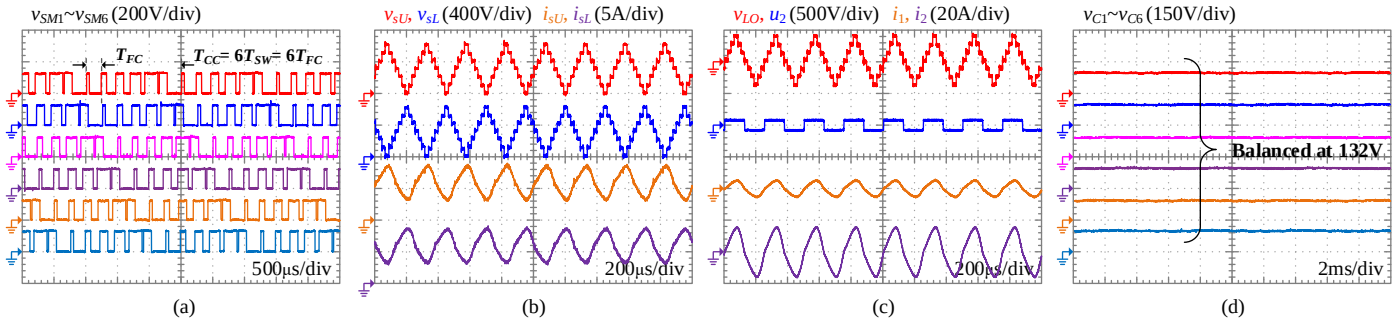

Fig. 13 Experimental results with n=6, m=0, L=7, N_h=1 as a balanced case (a) SM output voltages in upper stack. (b) Voltages and currents of upper and lower stack. (c) Voltages and currents of input and output side of ac passive stage. (d) SM capacitor voltages of upper stack.

TABLE III
EXPERIMENTAL PARAMETERS OF LLC-BASED MMDC

Parameters	Descriptions	Values
n	SM number per stack	6
$2V_M$	MV side bus voltage	800V
V_L	Minimum LV side bus voltage	20V
C_{CU}, C_{CL}	Medium-side dc-link capacitance	20μF
C_L	Low-side output capacitance	2.4mF
L_P,L_L	Equivalent arm inductance	4mH
C_r	Resonant capacitance	0.33μF
L_m	Magnetizing inductance	60.8mH
C_{SM}	SM capacitance	60μF (±10% variation)
r_T	Transformer turns-ratio	3:1
f_{ac}	AC stage frequency	4kHz
S	Power devices	IKW40N65H5

unchanged, which illustrates the great robustness of the proposed circulant modulation.

VII. EXPERIMENT RESULTS

In order to further validate the theoretical analysis for the multilevel circulant modulation and the inherent balance criterion, experiments are conducted on a down-scaled LLC-based MMDC prototype. The detailed parameters are listed in TABLE III. The control frequency is set as 4kHz, that is also the as stage fundamental frequency.

Experimental results with n=6, m=4, L=3, N_h=1 and a=4 are shown in Fig. 11 as an inherently balanced case. The SM output voltages in Fig. 11(a) show the preset circular patterns. The upper and lower stack voltage in Fig. 11(b) generate a three-level voltage in Fig. 11(c) to excite the ac passive stage.

Since there is no common factor other than 1 for n, m and$(n+m)/2$, SM capacitor voltage are inherently balanced at 79V in this system as shown in Fig. 11(d), which verifies the prediction in (19).

Experimental results with n=6, m=2, L=3, N_h=2 and a=4 are shown in Fig. 12 as an unbalanced case. The SM output voltages also show the circulant switching patterns in Fig. 12 (a). The stack and ac stage voltage and current are shown in Fig. 12(b) and (c). The SM capacitor voltages are illustrated in Fig. 12(d). It shows that the inherent balance capability is lost and capacitor voltages tend to split into 2 clusters with the maximum deviation of 30% of their reference voltage.

Finally, experimental results with n=6, m=0, L=7 and N_h=1 are shown in Fig. 13. Seven-level voltage is generated by the stacks with the SMs inserting and bypassing one by one. The SM capacitor voltages all settle at 132V, that identifies the inherent balance capability of the circulant modulation with N_h=1.

VIII. Conclusion

A circulant modulation method for multi-level operation of MMDCs has been proposed and proven to possess inherent balance of SM capacitor voltages if certain criteria are met. The stack switching patterns over a circulant cycle are composited into a switching duty matrix $\boldsymbol{d}_U$. If $\boldsymbol{d}_U$ is full-rank, inherent balance is guaranteed. In practical terms it means that each SM capacitor is clamped by the dc-link capacitor to an equal extent. A simplified criterion has also been deduced through circulant matrix theory and provides practical design guidance. So long as the numbers of inserted SMs in each voltage level have no common factor other than 1, the SM capacitor voltages can be inherently balanced. Otherwise, the SM capacitor voltages divide into several clusters and the circulant modulation loses its inherent balance feature. These clusters can be identified from the kernel of $\boldsymbol{d}_U$. Furthermore, a generalized co-prime criterion is identified for multilevel circulant modulation for the cases with equal magnitude of each voltage level. The validity of the theoretical analysis and of the deduced criterion have been confirmed through simulation and an experimental prototype.

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