An Implantable ENG Detector with In-System Velocity Selective Recording (VSR) Capability

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***Abstract*—Detection and classification of *electroneurogram* (ENG) signals in the peripheral nervous system can be achieved by *velocity selective recording* (VSR) using multi-electrode arrays. This paper describes an implantable VSR-based ENG recording system representing a significant development in the field since it is the first system of its type that can record naturally-evoked ENG and be interfaced wirelessly using a low data rate trans-cutaneous link. The system consists of two CMOS ASICs one of which is placed close to the multielectrode cuff array (MEC) while the other is mounted close to the wireless link. The digital ASIC provides the signal processing required to detect selectively ENG signals based on *velocity*. The design makes use of an original architecture that is suitable for implantation and reduces the required data rate for transmission to units placed outside the body. Complete measured electrical data from samples of the ASICs are presented that show that the system has the capability to record signals of amplitude as low as 0.5 μV, which is adequate for the recording of naturally evoked ENG. In addition, measurements of electrically evoked ENG from the explanted sciatic nerves of *Xenopus Laevis* frogs are presented.**

***Index Terms (keywords)*— Biomedical signal processing, Biomedical transducers, Microelectronic implants, Neural prosthesis**

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Introduction

Velocity selective recording (VSR) of ENG signals has the ability to extract more information from implanted electrodes than is possible using current methods. VSR is therefore a very promising technology for use in applications requiring sensory feedback. Potential applications include a variety of neuroprostheses [1], [2]. Neural recording generally requires chronically implanted electrodes and nerve cuffs, typically fitted with three electrodes configured as *tripoles*, have been implanted successfully for several decades [2]. However a single tripolar nerve cuff records only one signal and a recording method based on it is very restricted in its information acquisition capability. VSR solves this problem by providing a velocity spectral analysis of neural traffic (*afferent* and *efferent*) that can be related to fibre diameter and hence to the organs from which the signals originated [3], [4]. Furthermore, the summation of multiple correlated signal sources, which is fundamental to VSR, significantly improves signal-to-noise ratio (SNR). A very powerful method for implementing VSR using multi-electrode cuffs (MECs) has been described recently [3], [4]. In addition refs [5] – [8] and describe, respectively, current VSR methods and their limitations theoretically and experimentally. The current paper describes very significant improvements to current practices in neural recording allowing the recording of natural (physiological) ENG (see e.g. [8], [9]). These improvements include an interleaved analogue to digital conversion system providing increased sampling rate and improved digital processing creating the opportunity to incorporate the signal processing required for VSR into the implantable system. An important consequence of these enhancements is that the required transcutaneous data rate, which was previously a barrier to chronic implantation, is significantly reduced.

A practical VSR system should have the capability to make measurements from several nerves and this has been allowed for in the overall system design described here although testing has been carried out so far with only a single active recording site. Each ENG recording site (which might be in the arm or leg) is fitted with an ASIC that we refer to as an *electrode unit* (EU). An EU contains a complete analogue front end and a set of analogue-to-digital converters with multiplexed and serialized digital outputs that are linked to a second ASIC, called the *monitoring unit* (MU). The MU can be placed together with power control circuitry in a less space constrained part of the body such as the abdominal cavity. It can be connected to the EU by a multicore implantable cable that allows commands and power to be provided to the EU at the same time as providing a data path from the converters on the EU back to the MU. The (single) MU is a digital de-multiplexing system that can also implement a signal processor to perform the operations (delay, add, bandpass filtering) required in VSR to compute the velocity spectrum. Since the spectrum is essentially stationary (or slowly time-varying), the spectral parameters can be extracted for transmission at a conveniently reduced rate to an external logging system *via* an RF transcutaneous link (which is not described in this paper).

This paper describes new and original methods for the design of the analogue front end preamplifiers (realized in 0.8 μm CMOS), the cable interface unit (focusing on the mode of failure present in earlier designs and its resolution) and the digital signal processing module (realized in 0.35 μm CMOS) of the circuit. Detailed bench testing of the complete system is described including a measurement of the smallest detectable input signal level. This minimum level was found to be 0.5 μV at 1 kHz and demonstrates that the system is well suited to the recording of *natural* ENG (although this remains to be demonstrated *in vivo*). In addition, the system was employed to demonstrate VSR using electrically evoked *compound action potentials* (CAPs) recorded in an explanted sciatic nerve from a *Xenopus Laevis* frog. These results, described in section 3.4, show that signals with velocities of 14, 20 and 40 $m.s^{-1}$ were present in the excited CAP.

2. Methods

2.1 System description

Fig 1 is a block diagram of a single EU, MU and cable interface. The purpose is to implement VSR in a form capable of chronic implantation. Artificial delays are created to cancel the naturally-occurring delays between the signal samples appearing at the electrodes of the MEC. The delays are adjusted over a range to match velocities of interest and the delayed signals are summed, a process called delay and add [4]. The resulting plot of peak output power as a function of delay matched velocity is termed the *intrinsic velocity spectrum* (IVS) [4]. The selectivity obtainable using this method is quite low and it has been shown more recently that placing a bandpass filter at the output of each adder results in significant improvement [5].

2.1.1 Signal acquisition (front end) system, digitization

As shown in Fig 2, the MEC electrodes are connected in pairs to an array of low noise, low power differential amplifiers. These are referred to as 'nerve signal amplifiers' in Fig 1. Since the recorded signals are very small (typically about 1 – 10μV) voltage gain of about 10^4 (80 dB) is required to drive the analogue-to-digital converter (ADC) in a bandwidth of approximately 300 Hz – 10 kHz. Each amplifier in the array is a cascade connection of two stages each with a gain of about 100: a first-rank differential amplifier (low power, low noise preamplifier) *ac* coupled to a much less tightly-specified second-rank stage [9]. The *ac* coupling stage also provides the low frequency cut-off point (300 Hz), the upper cut-off frequency (10 kHz) being defined by the second-rank stages. These stages are grouped in the first stage symbol 'Dipole Amp' in Fig 2 and are followed by a unity gain 'Tripole Amp' stage that can be switched in and out of the signal path using the 'Tri/Dipole Mux' arrangement. This provides the option to digitize

and send either *dipole* (single differential) or *tripole* (double differential) versions of the recorded signals. As already noted, the EU is realized in a 0.8 μm CMOS, 5V technology. The main reason for this choice of process was its very low noise specification. Smaller CMOS processes tend to be noisier, especially in the production of flicker (1/*f*) noise, which is very significant in this application given the need to process low frequencies. Additional reasons for our choice included (1) the robustness of the technology to voltage transients at the input (this is important here as the front-end amplifiers are *dc* coupled to the recording electrodes) and (2) the excellent signal-handling capacity provided by the 5 V power supplies.

2.1.2 Cable interface and system communication

The communication between the MU and an EU is bidirectional and employs an implantable 4-core silicone-insulated steel cable providing separate cores for consisting of clock, sync and data signals), backward channel (from EU to MU consisting of measured data) and two power rails (+/-2.5V). The characteristics of this cable are shown in Table I. The forward data flow is in the form of frames and a summary of these features is given in section 2.3. A four-level signaling system is employed and results in a data rate of 6 Mbits /second.

2.1.3 Digital signal processing

The MU is a digital signal processing system that (a) de-multiplexes the digitized dipolar or tripolar signals from the EUs and (b) performs signal processing operations (delay, add, filtering) to calculate the velocity spectrum. These operations are located on a separate FPGA that is initially placed outside the body in the 'external signal processing unit' (SPU) as shown in Fig 1. The intention is that ultimately these parts of the system will be integrated in the MU. Finally, the parameters of the measured velocity spectra are extracted and transmitted across for logging although the telemetric aspects of the system are not dealt with in the present paper. The MU was realized in 0.35 μm technology. The low noise and other advantages of the 0.8 μm CMOS process are not relevant here and so a smaller process was used to reduce the size and power consumption of this all-digital chip. An even smaller process could have been used but the 0.35 μm technology was chosen because, although it is basically a 3 V process, it has a 5 V I/O option that allows very convenient interfacing with the EU.

2.2 Electrode unit

2.2.1 Front end amplifier array

Each first rank differential amplifier employs a transconductance amplifier of the type described in reference [11]. The input differential pair employs lateral pnp bipolar transistors (BJTs) as a viable, cheap and convenient substitute for conventional vertical BJTs in this application [11], [12]. Unfortunately

lateral transistor parameters degrade with collector currents of more than a few microamperes which conflicts with the need to provide adequate transconductance gain (g_m) and to suppress white noise to appropriate levels both of which require fairly high collector currents (typically about 100 μA). To compensate for this, a parallel combination of several lateral pnp cells was used so that the collector current in each individual cell is low (a level of forward current gain (β) of 100 was adopted as a reasonable rule-of-thumb) [11].

The design described in [11] was based entirely on the CADENCE model parameters and in preparation for the new design presented in this paper these results were compared with the measured characteristics of three lateral pnp transistors chosen from a batch of 10 fabricated devices, each consisting of 6 cells connected in parallel. The data indicates that β declines more slowly with I_b than the model predicts and that in fact 12 parallel cells (rather than 36) are sufficient to provide the required current gain, occupying an area of 6,525 μm^2 rather than 18,900 μm^2 in the earlier version. Each complete nerve amplifier in the original design measured 1,315 x 425 μm, which as a result of the DC characterization presented in this paper, has been revised down to 1,035 x 395 μm, representing a saving of approximately 1.5 mm^2 for the whole 10-channel array. The space saved has enabled double guard rings (i.e. one connected to each power supply rail) to be employed around each amplifier and has also influenced the design of the ADC system (see section 2.2.2).

In addition, in the design presented in this paper, the total tail (common emitter) current was reduced to 100 μA, approximately halving the power consumption of each preamplifier. The effect of this was to reduce gm to about 1 mA/V, the voltage gain of 100 being achieved by increasing the load resistance (R_L) to 105 kΩ and to increase noise slightly. However, the input referred *rms* voltage noise level is still within the specification (500 nV *rms*) and so this modification is entirely beneficial.

2.2.2 Analogue to digital conversion (ADC)

This function is carried out by five interleaved 10-bit ADCs operating at a sampling rate of slightly over 66 kSamples/s each, providing an effective sampling rate per channel in excess of 33 kSamples/s. This satisfies both the sampling requirement for an analogue bandwidth of 10 kHz and also the additional requirement in VSR that the sampling interval is less than the minimum delay offset between two adjacent tripolar outputs. These converters are taken from the Austriamicrosystems library for the process. Each unit measured 675 μm x 619 μm (0.417 mm^2) and in order to accommodate 5 of them on the die, it was necessary to use some of the space freed by the redesign of the preamplifiers described above. The 10 dipole signals at the outputs of the second-rank amplifiers are converted by the ADCs and serialised into a packet for the entire sample set. This packet consists simply of a start bit followed by the

LSB first ordered data samples (each with its own parity bit) as a 110-bit data frame. In order to cope with the required data rate, a data bit is transmitted on each half of the clock cycle giving an effective *double data rate* (DDR) transmission rate of 6 Mbit/s. This allows a sample rate in excess of 33 kSamples/s (3.6 Mbit/s) to be achieved for all ten dipole channels without the potential noise associated with transmitting data at the same time as the data conversion is occurring.

2.2.3 Control Logic

A digital control system is required within the EU but this is kept to a minimum in order to reduce switching noise. The EU operates in a low power and noise mode by clocking registers from a token shift register rather than directly from a global clock. It is connected to the MU *via* a four core cable carrying two power (+/-2.5V), and two unidirectional data lines. The control logic uses the +/-2.5V power rails as an effective 5V supply suitable for the logic in this process. The clock and control commands are recovered from a four level MU to EU signal using a triple threshold input buffer and a set of re-synchronization registers [9]. The data channel from the EU to the MU uses standard binary DDR. The use of two unidirectional communications signals and a four level MU to EU link permits the continuous reception of a clock signal by the EU without any need to re-construct missing edges. Hence, voltage controlled oscillators and other clock recovery circuitry is not needed in the EU.

2.3 *Monitoring Unit*

The essential functions of the MU are to configure the EUs on start-up, control the data acquisition from the EUs, and to provide conversion of the data into a form that it can be logged outside the body *via* an transcutaneous RF link. The first two of these functions were described in [9] and will not be repeated here. However, as already noted, the output data rate from an EU is in excess of 3 Mbit/s, which is too high for transmission *via* the transcutaneous link employed in this system and so the VSR signal processing has to be implemented in the MU. Since the resulting velocity spectra are stationary or slowly time-varying, a much lower data rate (typically a few kb/s) is possible. The VSR signal processing system, which is currently implemented in an FPGA, is shown by a single block in Fig 1 and in more detail in Fig 3. The following functionality is required in order to be able to achieve the appropriate level of data reduction:

1. Sample Delay Lines to provide velocity matched delays;
2. Digital filtering to increase velocity selectivity and permit envelope smoothing;
3. Rectification to permit signal envelope detection;
4. Thresholding to reduce a single velocity channel from a multi-bit waveform to a single bit detection signal;

5. Sub-Sampled data output to reduce the output data rate.

A signal processing unit (SPU) based on a sequential state machine has been designed to perform these functions. The state machine effectively implements a customized processor that can perform all the required signal processing operations in a linear execution model. The system is shown in block form in Fig 3. The state machine executes a fixed sequence of instructions each time a sample is received from the EU. The instructions implemented represent a very compact instruction set for efficient fixed point signal processing with most of the instructions performing more than one operation in comparison to a typical microprocessor instruction set. The SPU instruction set is very compact using just 9 instructions operating on a single local register (the 32 bit accumulator) with no branching. Instructions all have the format of a 3 bit opcode, a 16 bit constant and a 10 bit data address / second constant. The instructions implemented are:

- READ. Read from a memory location, multiply by a constant and add it to the accumulator;
- MAX. Read from a memory location, multiply by a constant and replace the accumulator if the multiplication result is larger than the current accumulator value;
- WRITE. The accumulator value is stored at the indicated memory location;
- ABS. The accumulator is replaced by its unsigned equivalent;
- CMP. The accumulator is replaced by the second constant or zero depending upon a comparison of the accumulator with the 16 bit constant field of the instruction;
- OUTPUT: The value in the accumulator is truncated and written to the output port. Output masking permits down-sampling by a factor of 2, 4, 8 or 16;
- HALT: Processing stalls until the next sample when the code restarts;
- NOP: No operation is performed. Required to pre-load the two stage pipeline.

Sample inputs to the MU are automatically loaded into consecutive addresses of memory from a base address determined by the address offsetting system. Once the samples from all 10 channels have been received, processing is initiated with the base address for data updated to the location of the sample set just loaded. Addressing of data by the instruction set is automatically offset by this base address so that a given address in the memory as seen by the programmer always contains the same sample or previously calculated variable relative to the current sample. For example, in a system with 32 words per sample block (as is the case in the present design) The most recent sample received from channel 0 can be accessed at address 0 and the previous sample from channel 0 is always accessed at address 32. When a new sample is received the offsetting system changes the base address such that the memory location that was seen as address 0 is now seen as address 32 (i.e. the sample effectively moves to the location of the previous sample). In this manner, the addressing in the instructions is relative to the current sample. This

mode of addressing can be described as *sample relative addressing*. In order that this addressing mode can operate continuously, addresses are permitted to overflow the maximum address in the memory space by simply ignoring any overflow bits. Hence the data memory becomes the equivalent of a circular buffer.

The provision of output gating allows a wide range of sub-sampling operations to be performed without the need for conditional branch instructions in the processor architecture. This is achieved by incorporating a one-hot 16 bit ring counter into the processor that is updated each time a complete sample set is received. The constant field in the OUTPUT instruction is used as a mask and the output only occurs if the single '1' bit in the ring counter corresponds to a '1' bit in the constant field in the instruction. Hence an OUTPUT with a constant value of 0001000100010001_2 would produce an output only every 4 sample periods. In addition, the overall output data rate can be smoothed by causing different computations to output on different samples. For example, an OUTPUT with a constant value of 0100010001000100_2 would output data at the same rate but at a different time to the previous example. These architectural decisions have the benefit of constraining the process to operate in constant time for each sample even in the case of subsampled outputs.

3. Results

The modified EU has been fabricated as shown in Fig 4, and tested with an existing MU integrated circuit and a 0.5m length of bio-compatible four-core cable whose characteristics are compared with Cooper Cable (using helical Pt/Ir wires) [9], [13] in Table 1. In addition, extra test points placed on the EUs enabled the new amplifiers to be tested separately. The analogue front-end tests are described below as are communication and system level tests. Simulated processing using the proposed VSR signal processor based on previously recorded data also presented.

3.1 Nerve signal acquisition and amplification (front-end)

The frequency responses of the ten dipole channels of five fabricated chips were tested individually and showed a very satisfactory level of consistency. The results are similar to those reported in [11], the reduction in the number of lateral *pnp* transistors in the front-end having, as predicted, little effect on the performance of the circuit. Fig 5 shows the measured frequency response of one complete channel for a sinusoidal input signal level of 100 μV. This is plotted on the same axes as the simulated and measured analogue outputs for the purposes of comparison. As noted in Section II (a), the mid-band gain of a complete nerve amplifier channel is about 79 dB with lower and upper cutoff frequencies of 300 Hz and 10 kHz. Note that the simulated and measured responses correspond very closely, the slight additional attenuation at higher frequencies being attributable to the effect of the sample and hold stage. Note also

that the frequency range of the digitized version is limited by sampling effects to about 17 kHz (i.e. the Nyquist frequency of the test environment which runs at 34 kSamples/s).

3.2 Communication interface

The multi-level MU to EU communication system operated correctly over the implantable cable. However, the DDR communication system from EU to MU combined with the implantable cable produces troublesome artefact on the MU to EU 4-level link when the returned data transitions in the opposite direction to the clock signal. The reason for this is that the current required to drive the data connection from one logic level to another is drawn from the power supply at the EU end of the implantable cable. Because of the resistance and reactance of the cores in the implantable cable, the power or ground line under load exhibits a short *bounce*. The frequency of this power line signal is well out of band of the analogue circuitry, but because the 4-level signal is driven by the MU, it appears to the EU circuitry to bounce in the opposite direction to the power line. This can cause an apparent glitch on the clock signal fed to the EU. This can be addressed in future versions of the EU by delaying output switching by around 50-80ns. This in turn shifts the time at which the (relatively small) glitches on the clock input will be induced to a point where the internal clock signal is stable and voltage noise immunity is at its peak. An alternative strategy would be to create a Schmitt trigger on the Clock input to the EU by adding a fourth threshold detector on the MU to EU connection input.

3.3 Complete system (excluding VSR signal processing)

For this test, an EU and an MU were interconnected by a 50 cm length of biocompatible four core cable. The analogue inputs were driven by a specially designed programmable signal source generating synthesized SFAPs with 10 bit resolution. The magnitude of the LSB is approximately 5 nV, although in practice such tiny increments are invisible due to the noise floor of the system. Typical SFAP signals used for testing are in the range 10 μV to 100 μV peak-to-peak. The signal generator produces a variable inter-channel delay to emulate the propagation velocity of an SFAP passing through an MEC in the range of 10m/s to 100m/s and the outputs of the channels were captured using a logic analyzer. Captured data from the MU are shown in Fig 6 for synthesized SFAPs with velocities of 10, 20 and 30 m/s. Data from all ten channels were captured but only two channels are shown for each velocity. Fig 7 shows the impact of summing the signals from all ten channels using the delay-and-add technique [4], [5] with a matched velocity of 20m/s. The results clearly show the ability of the system to differentiate between action potentials travelling at different velocities.

Finally, the smallest detectable signal level was determined by connecting a single sinewave source to the input of one channel. At a frequency of 1 kHz, it was possible to detect an intelligible output for an input of amplitude about 0.5 μV, which accords well with the measured *rms* noise floor of 420 nV. It should be

noted that this lower limit can, in theory at least, be significantly improved by the use of an *N*-channel array, since the signal-to-noise ratio will increase in proportion to $\sqrt{N}$.

3.4 Measured results from frogs

Data recorded during experiments with 80 to 90 mm long sections of sciatic nerves explanted from decapitated Xenopus Laevis frogs [6] was used to evaluate the effectiveness of the proposed signal processing. The signals were obtained from the nerve immersed in amphibian Ringer's solution at room temperature and stimulated electrically at their distal end, resulting in the production of CAPs propagating towards the proximal stump. The MEC recording cuffs were constructed using polyimide technology with sputtered platinum electrodes and were of the self-spiralling type [3]. The eleven electrode cuffs were 1.5 mm in diameter, about 40 mm long with an electrode centre-to-centre spacing of 3.5 mm. Each electrode was of 500 μm wide.

The MECs were connected directly to the 10-channel amplifier array described in section 2.1 (i.e. the front-end of the EU) and two types of data acquisition and analysis were employed. Firstly, as reported in [6], the outputs of the front-end amplifiers were captured and digitized by a commercial data acquisition card (DAQ-National Instruments 6062E) and subsequently processed (delay-and-add) in MATLAB. Secondly, the recorded signals were allowed to propagate through the proposed digital signal processing chain and VSR signal processing was carried out in a simulation of the FPGA connected to the output of the MU as described in Section 2.1.3. Fig 8 shows the intrinsic velocity spectra (IVS) of the resulting data, i.e. the plots obtained by applying the delay-and-add algorithm directly to the captured data, without applying any velocity selectivity enhancing techniques such as bandpass filtering [5]. Three excited populations, at 14, 20 & 42 m/s respectively are clearly visible.

In Fig 8 the spectrum of the externally-captured signal (dashed line) is shown together with that of the signal passed through the MU (solid line). The small differences between the two spectra are due to memory restrictions in the MU processor. For example, whereas the velocity spectrum of the externally-captured signal has a range of 10 – 100 m/s with a step of 1 m/s, the MU signal has a range of 15 – 75 m/s and a step of 4 m/s. An increase in range and/or resolution would require more memory and hence die size and power consumption.

3.5 Power consumption and area

The EUs consume 43 mW each at maximum sample rate (30 kSamples/s per channel). The majority of the power consumption is in the analogue sections of the design so slower sampling rates do not significantly reduce the total budget. The MU consumes 37 mW in a basic configuration, and the addition of the signal-processing module described in Section 2.3 is estimated to add a further 70mW. This

estimate is based on equivalent gate counts combined with power data for the Austriamicrosystems 0.35 μm CMOS library based on reasonable assumptions for signal activity. An MU constructed using 0.8μm technology is estimated to consume 300mW showing the importance of moving this device to a smaller process geometry whilst maintaining compatibility with the 0.8μm EU.

The EU die measured 6.4 x 2.5mm. Without the additional VSR signal processing, the MU is much smaller measuring 1.3 x 1.3 mm and is severely pad limited. Using the same basis as used for the power consumption estimate described above, the area of the MU including the signal processing system is estimated at 3 x 3 mm. In this configuration the design is core limited. Approximately 0.6 mm^2 of the core is taken up with the processor, 0.2 mm^2 is program memory and 2 mm^2 is the delay line memory. In a 0.8μm process the MU would measure approximately than 9 x 9 mm.

4. Discussion

4.1 Application of the method

So far VSR has been demonstrated as a means of discriminating electrically-evoked ENG waveforms (CAPs) such as the *in vitro* experiments in *frog* described above. In this application it has shown itself to be a powerful and useful tool, and has many potential applications in neuroscience. In order to be of practical value in clinical applications such as neuroprostheses it is necessary to solve two further sets of problems. Firstly, the amplitude of natural (physiological) ENG is about an order of magnitude less than the electrically evoked CAPs described above. Secondly, information is transferred by means of the rate of neural transmission in velocity bands and so it is not sufficient simply to know the velocities present in the recording. Recently, new methods have been described that demonstrate that VSR can be extended to determine the rate of neural firing at particular velocities. This is referred to as the method of *velocity spectral density* (VSD) [14].

In clinical applications such as neuroprosthesis, we envisage the method being used in one of two possible ways. If the relevant single fibre action potentials are distinct spikes that stand out above the noise, then the system can be used with our recently-published method, called *velocity spectral density* (VSD) [14]. In this method, spikes are sorted by velocity and the output could be the number of spikes per unit time in a defined band. If the SFAPs are not so large, then the system would not be used to count but would integrate over a period to find the power in the velocity band above the background noise. During set-up, it will be interesting to see the whole velocity spectrum of the signal but in the application, one would take just the signal for the velocity of the relevant fibres. Whether the SFAPs were large or small, the output would represent the number of spikes over the period of counting or integration.

4.2 Analogue front end section

As noted this consists of a low noise preamplifier with a midband voltage gain of 100, *dc* coupled to the MEC. The devices in the input stage are parasitic *lateral bipolar transistors* (BJTs), which are available as standard cells in most standard CMOS processes. For biomedical applications where the required bandwidth is low, these devices can be used to provide a better trade-off between noise and power consumption than would be possible with a comparable FET-based stage. However, BJTs require base current to be supplied and BJT-based amplifiers tend to have much higher levels of input-referred current noise than their FET-based counterparts (e.g. about 1 pA /√Hz for the amplifier described in this paper). For low source impedances such as are provided by cuff-based systems (about 100 Ω - 1 kΩ at 1 kHz) this does not cause a problem, but some types of electrodes (e.g. *microchannels* [15]) have impedances as high as 100 kΩ and in such cases the resulting noise would be at least an order of magnitude larger than the input referred voltage noise. Current noise would dominate in this case and FET-based approaches would probably be preferable. Another issue results from the *dc* coupling itself.

4.3 Digital Signal processing section

The provision of signal processing using *sample relative addressing* enables entirely deterministic throughput for a processor and the silicon area required to create the digital delay lines dominates the device cost. In this configuration, the processor can create 30 independent VSR outputs each using an interpolated delay and add to accumulate the individual channel information. Depending on the application this may be far more processing than is required but reducing capability results in almost no area saving in the MU due to the small relative size of the processor. However, since the processing does dominate the MU power consumption (70%), it would be entirely possible to scale processing activity by adjusting clock frequency with a resultant near linear reduction in power consumption of the MU.

4.4 Statement on the welfare of animals

The nerve experiments were done by researchers trained according the *Guiding Principles in the Care and Use of Animals*. Specific approval for these experiments was not required from the Committee for Animal Experiments because the nerves were taken from the bodies of frogs that had been killed for other experiments that were already approved.

5. Conclusions

An integrated system for velocity-selective recording (VSR) based on two ASICs fabricated using different CMOS technologies has been described and tested. A 0.8μm technology was used for the low noise front end data capture system whilst a 0.35μm process was used to create a digital only de-serialiser

with enough spare area to implement a VSR signal processing system using the delay-and-add algorithm. Interconnection between the ASICs is via a 4-core implantable cable using stainless steel cores. In this version of the system, additional discrete components were necessary at the data capture end of the implantable cable because of the influence of the cable impedance on apparent signal levels. The ability to digitize ENG data directly at the recording site provides considerable opportunities for improving the detection, recording and classification of nerve signals.

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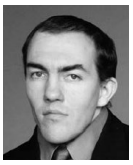
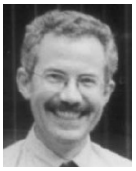


Christopher T. Clarke (M'13) received a B.Eng.degree in Engineering Electronics and a Ph.D. degree in Computer Science from the University of Warwick in 1989 and 1994, respectively. He joined the University of Bath in March 2003.

Robert Rieger (S'01−M'04−SM'08) received the B.Eng. degree from the University of Kent, Canterbury, U.K., in 2000, and the Ph.D. degree in electrical and electronic engineering from University College London (UCL) in 2004.



Nick Donaldson studied Engineering and Electrical Sciences at Cambridge University. Since 1992, he has been Head of the Implanted Devices Group at University College London, UK.

Martin Schuettler studied Electrical Engineering at the Technical University of Braunschweig, Germany, and received his PhD on peripheral nerve stimulation electrodes from Saarland University (Germany) in 2002.

John Taylor received the BSc and PhD degrees from Imperial College, London University, London, UK, in 1973 and 1984, respectively. He joined the Department of Electronic and Electrical Engineering at the University of Bath, UK in 2002.

TABLE I
ELECTRICAL CHARACTERISTICS OF THE FOUR-CORE IMPLANTABLE CABLE PER CENTIMETRE OF CORE LENGTH COMPARED TO COOPER CABLE

Parameter	Cooper Cable [9]	Steel core cable
Resistance	2 Ω	0.1 Ω
Inductance	15 nH	16 nH
Capacitance[1]	80 pF	5 pF

[1] total to other cores and body tissue

TABLE II
ANALOGUE SYSTEM SPECIFICATION AND MEASURED RESULTS

Parameter	Specification	Previous system [9]	Measured	Units
Dimensions	12	12	11.6	mm^2
System power consumption	300	238	196	mW
Midband gain	80	80	79	dB
–3 dB frequencies:				
lower	300	310	320	Hz
upper	10	3.3①	10	kHz
Total input-referred voltage noise density				
@ 1Hz	< 20	11.5	18	nV/√Hz
@ 1kHz	< 4	3.8	4.1	nV/√Hz
Total input-referred current noise density				
@ 1Hz	< 20	17	0.35	pA/√Hz
@ 1kHz	< 2	1.5	0.12	pA/√Hz
Total input-referred *rms* voltage noise 300 Hz-10 kHz	< 500	291②	420	nV
Residual input DC current	< 100	20.25	<< 100	nA

These measured results were achieved without changing the power supply rails or the number of dipole channels.
①In the design described in [7], the specification was 3.5kHz
②This measurement was for the range 1kHz – 5kHz

List of Figure Captions

Figure 1. System Architecture Overview showing a single EU, the MU (including the proposed VSR signal processing) and the cable interface. The signal processing unit (SPU) is currently implemented externally but could also be located inside the MU.

Figure 2. The Electrode Unit (EU). This is a more detailed version of the block diagram on the left of Fig 1.

Figure 3. The SPU proposed for incorporation into the Monitoring Unit to provide VSR signal processing. This is a more detailed version of the blocks marked 'proposed VSR signal processing' and 'External Signal Processing System (SPU) on the right of Fig 1 and simulated in an FPGA environment as described in section IV.

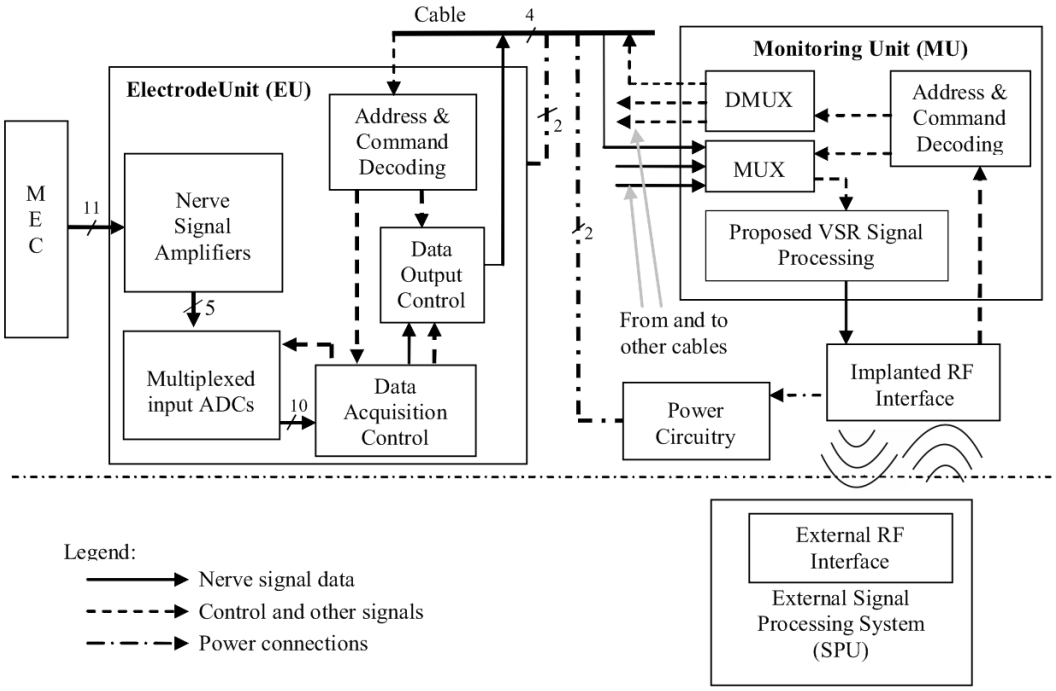
Figure 4. Chip microphotograph of the redesigned EU. The 10 analogue front end stages are in a single row at the bottom left of the die. Above those are the 10 *ac* coupling stages and 2nd rank amplifiers. Finally at the top, also in a row are the 5 analogue-to-digital converters and serialization stages.

Figure 5. Comparison of measured and simulated frequency responses of a single channel of the EU front end amplifier system with the measured overall system frequency response. The slight extra attenuation of the system response at higher frequencies is attributable the effect of the sample-and-hold stage. Note also that the system response terminates at 15 kHz, which approaches the Nyquist frequency (17.5 kHz)

Figure 6. Pairs of recorded tripolar signals for adjacent channels to illustrate the relationship between delay and propagation velocity. Three action potentials are employed with velocities of 10, 20 and 30 m/s. The signal amplitudes are referred to the inputs.

Figure 7. Unfiltered tripolar outputs of the delay matched addition process for an SFAP of propagation velocity 20 m/s. The middle plot shows the output when the delays are tuned for 20m/s, whilst the upper and lower show the outputs when the delays are tuned to 10 m/s and 30 m/s respectively. The signal amplitudes are referred to the input signal voltages.

Figure 8. Intrinsic velocity spectrum (IVS) of electrically evoked compound action potentials (CAPs) recorded from Xenopus Laevis frogs (nine tripole channels). Three excited populations are visible, at 14, 20 & 42 m/s respectively. The dashed line is the output from the analogue front end section of the EU captured using an external DAQ card and processed in MATLAB. The solid line is the reconstructed output from the SPU after hardware VSR signal processing. Both the velocity step and overall range are limited by available processor memory.



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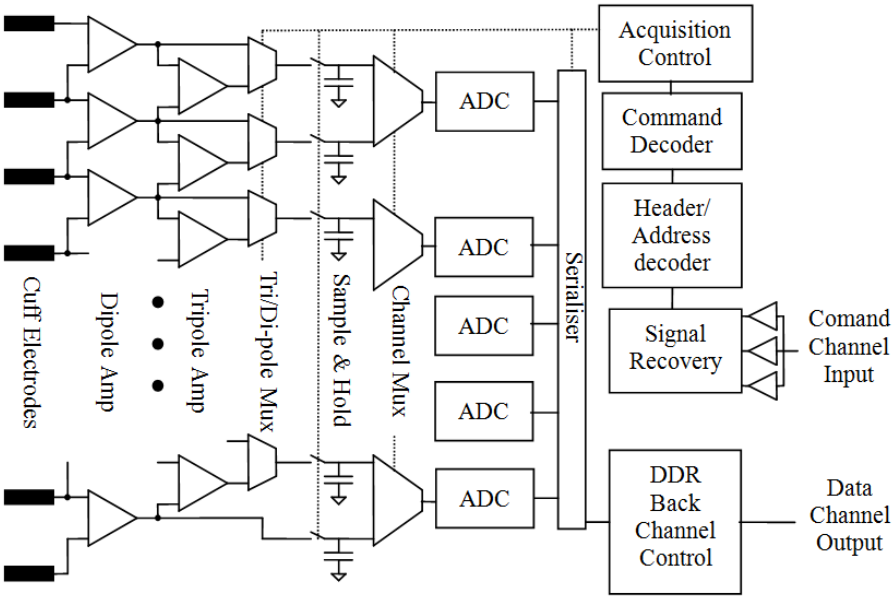

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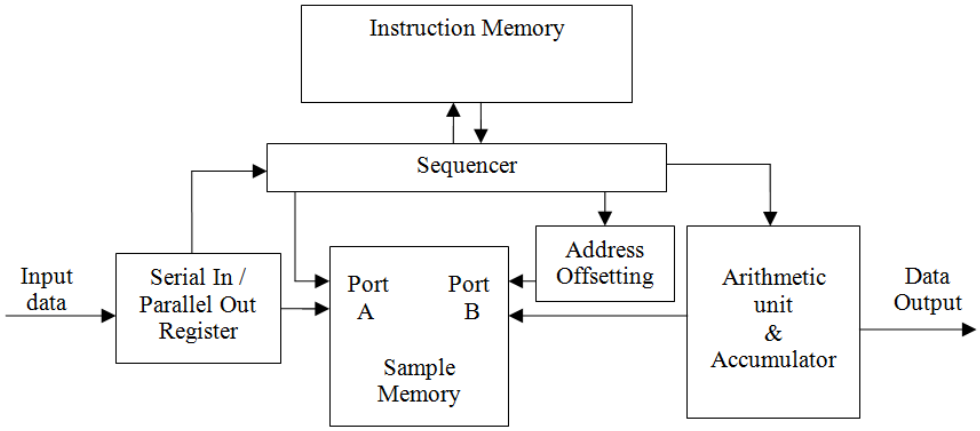

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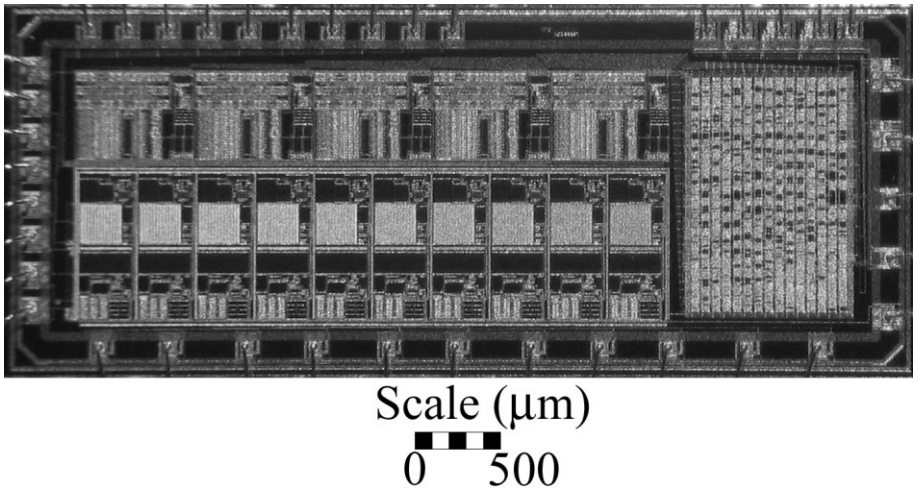

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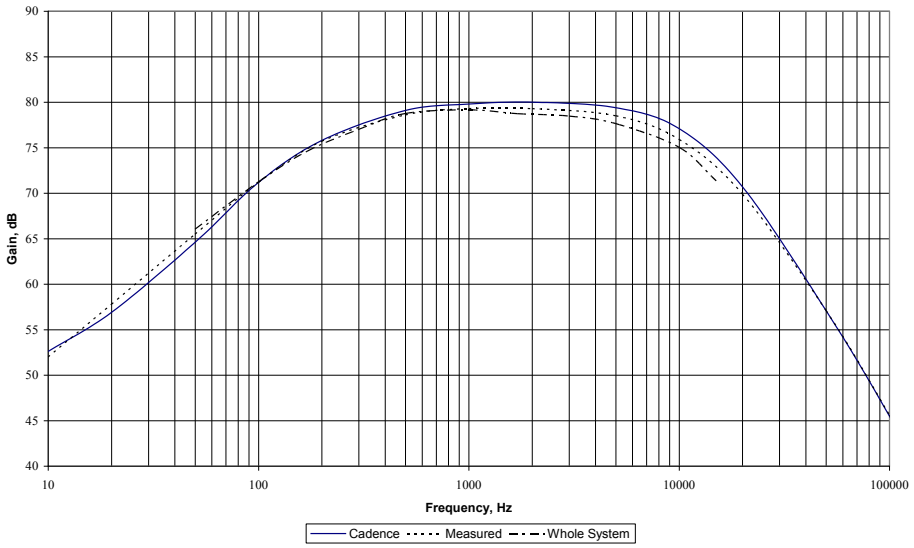

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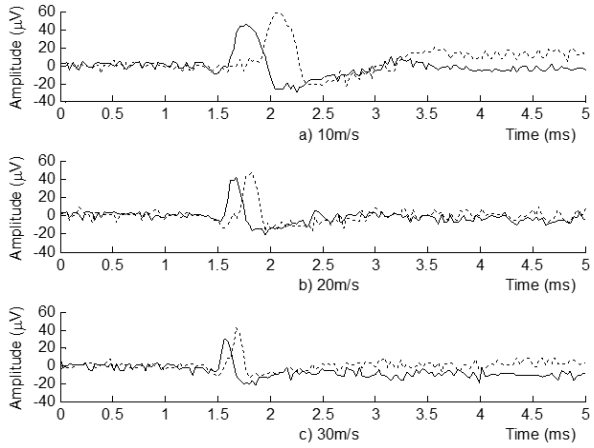

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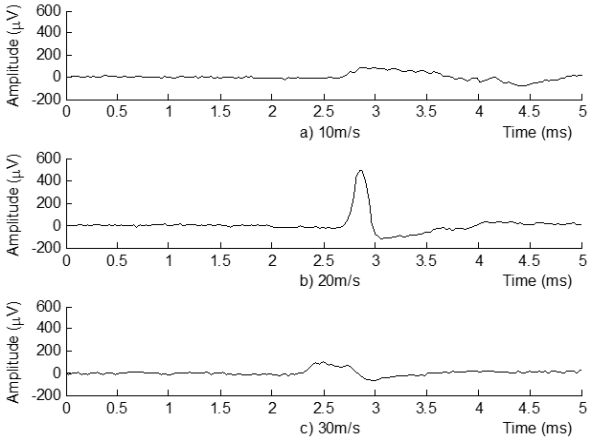

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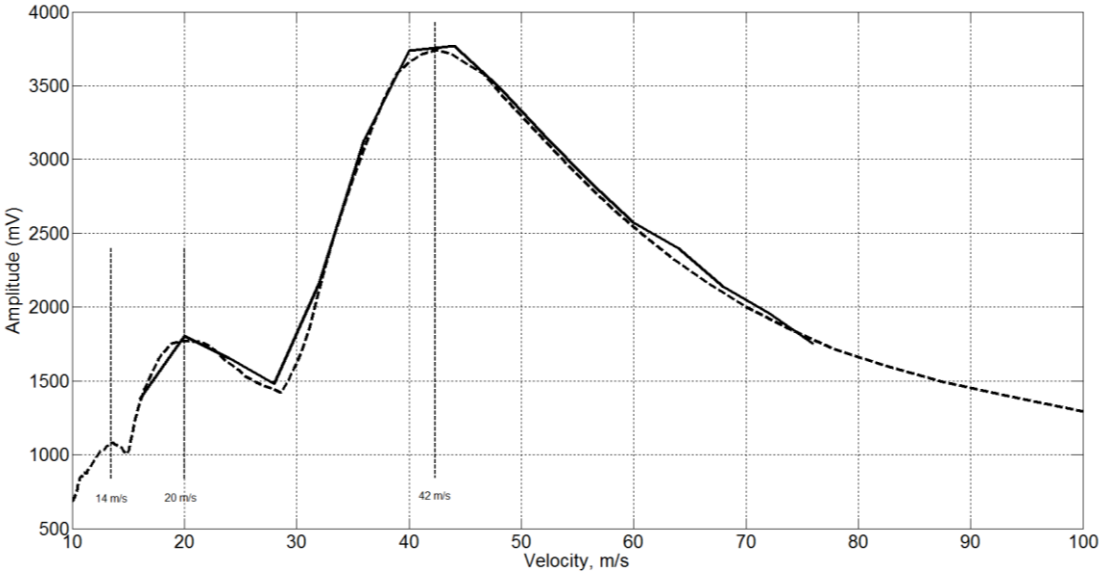

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