MAXIMISING DEVICE CURRENT UTILISATION IN INVERTER DRIVES

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ABSTRACT

A considerable improvement in power-semiconductor-device utilisation seems possible if the output current of power-stages is actively limited by thermal feedback from the power-converter. To illustrate the potential utilisation benefit in main switching devices, the variation in usable current with operating conditions is examined for several devices used in a constant-frequency-PWM VVVF inverter, and operated under conditions to keep their junction-temperature constant.

INTRODUCTION

Despite the high volume contributed to overall power converter size by the heatsink, fans and air circulation space, power electronics specialists have been much less attracted to optimising heatsink configuration and use, and getting the best use out of devices, than, say, optimising the type or configuration of semiconductors, magnetic components, connection hardware and control systems.

The typical error that exists in heatsink design calculations is often not precisely known or empirically tested. The likely reasons for this include: the difficulty in accurately predicting or even bracketing device power-loss, given the existence of production-spread and temperature variation in conduction and switching characteristics; the complexity of practical power-loss waveforms; the imprecision in estimated thermal impedance and resistance seen by power devices distributed on a heatsink; and the difficulty in measuring the chip-area-averaged junction-temperature of switched power-devices. As a result, the safety margins built into power-stage and heatsink designs must often be far from optimum.

Some improvement in verifying the operating junction-temperature of devices and achieving tighter designs will inevitably result from better loss prediction and thermal-design verification as simulation tools become more widely tested and developed. However, a greater improvement seems possible using more sophisticated active current-limiting, which limits the maximum output current or power of systems to maintain the junction-temperature (or power dissipation) of the main devices below a pre-set level, say 125°C, on a pulse-by-pulse basis. The effects of changes in device heating and cooling characteristics due to dynamic load changes, variation in operating conditions etc. would, thus, be directly measured and safeguarded against.

There would be significant practical difficulties to overcome in implementing temperature-regulated active-current-limiting. But prior to tackling these, it is necessary to consider the potential increase in device utilisation. This has been investigated by notionally applying a range of medium-power devices in a constant-frequency PWM three-phase inverter application and estimating the maximum usable current that gives a specific junction temperature for a range of modulating and switching frequencies.

ESTIMATING INVERTER POWER-LOSS

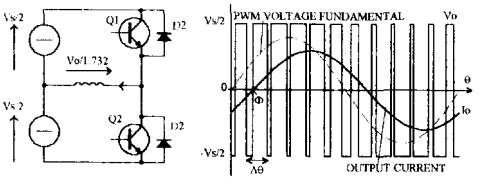

Fig.1 Equivalent circuit for loss estimation. PWM voltage, its fundamental component and lagging output current.

In inverters, device current and duty-cycle vary sinusoidally, and the variation in all loss components with current level must be determined and averaged over an output-frequency, *fo*, period. This becomes relatively simple with high carrier-frequency ratio, *p*, [i.e. *p* or $fsw/fo \geq 10$], provided conduction power-loss and switching energy-loss equations can be expressed as continuous functions of current, as discrete-equation averages may then be approximated by closed-form continuous-equation averages.

The power-loss in each bridge-leg of a 3-phase inverter is about the same, assuming balanced steady-state machine operation, and it is only necessary to examine the equivalent circuit for one bridge-leg and load-phase (Fig.1). Also, the inductive load, i.e. the machine-winding, is assumed to draw a pure sinusoidal current since inverter switching period is usually chosen to be far less than the winding time-constant for low ripple.

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The calculation of average bridge-leg power-loss in asynchronous regular-sampled-PWM inverters has been the subject of previous investigations. Generally, these either involve the numerical solution of discrete loss equations, or the use of approximate closed-form solutions to discrete equations [1-4]. The latter method of solution, although inherently less flexible and accurate, avoids the need to generate such complex algorithms for numerical solution by computer, and has been shown [3] to give surprisingly low error for regular-sampled-PWM, provided p is at least 10.

CONDUCTION POWER-LOSS

Switch and diode on-state voltages are approximated using conventional piece-wise linear models [Eqs.(1a) and (1b)], but may be specified as a more precise function of current if greater accuracy is desired.

$$v_Q(i) = V_{QO} + i\,r_Q \qquad (1a) \qquad v_D(i) = V_{DO} + i\,r_D \qquad (1b)$$

Bridge-leg current at any instant, θ, of the fundamental output-period is given by Eq.(2), where $\theta = \omega t$ and ϕ is the phase difference between the load-current and PWM voltage-waveform fundamental [see Fig.1].

$$i(\theta) = \hat{I}_O \sin(\theta - \phi) \qquad (2)$$

Transistor and diode normalised conduction periods at any θ are given by Eqs.(3a) and (3b), where M is the modulation index and $\Delta\theta$ is $2\pi/p$.

$$\Delta\theta_Q = \frac{1}{2}[1 + M\sin\theta]\Delta\theta \qquad (3a) \qquad \Delta\theta_D = \frac{1}{2}[1 - M\sin\theta]\Delta\theta \qquad (3b)$$

Therefore, net average conduction power-loss over 2π is given by Eqs.(4a) and (4b).

$$P_{QCON} = \frac{1}{2\pi}\sum_{s=\phi/\Delta\theta}^{(\pi+\phi)/\Delta\theta}\left[V_{QO}\,i(s\Delta\theta) + r_Q i^2(s\Delta\theta)\right]\Delta\theta_Q \qquad (4a)$$

$$P_{DCON} = \frac{1}{2\pi}\sum_{s=\phi/\Delta\theta}^{(\pi+\phi)/\Delta\theta}\left[V_{DO}\,i(s\Delta\theta) + r_D i^2(s\Delta\theta)\right]\Delta\theta_D \qquad (4b)$$

Approximate closed-form solutions are obtained by assuming $\Delta\theta$ tends to zero and using continuous system averages given by Eqs.(5a) and (5b).

$$P_{QCON} \approx \frac{1}{2\pi}\int_{\phi}^{\pi+\phi}\left[V_{QO}\,i(\theta) + r_Q i^2(\theta)\right]\frac{[1 + M\sin\theta]}{2}\,d\theta \qquad (5a)$$

$$P_{DCON} \approx \frac{1}{2\pi}\int_{\phi}^{\pi+\phi}\left[V_{DO}\,i(\theta) + r_D i^2(\theta)\right]\frac{[1 - M\sin\theta]}{2}\,d\theta \qquad (5b)$$

These, when solved, give the following diode and switch average conduction power-loss equations.

$$P_{QCON} \approx \frac{\hat{I}_O V_{QO}}{2}\left(\frac{1}{\pi} + \frac{M}{4}\cos\phi\right) + \hat{I}_O^{\,2} r_Q\left(\frac{1}{8} + \frac{M}{3\pi}\cos\phi\right) \qquad (6a)$$

$$P_{DCON} \approx \frac{\hat{I}_O V_{DO}}{2}\left(\frac{1}{\pi} - \frac{M}{4}\cos\phi\right) + \hat{I}_O^{\,2} r_D\left(\frac{1}{8} - \frac{M}{3\pi}\cos\phi\right) \qquad (6b)$$

These equations do not incorporate the effects of third-harmonic addition but the difference in loss is small.

SWITCHING POWER-LOSS

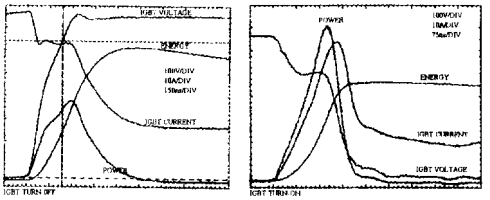

Fig.2 Switching waveforms with power and energy.

Switching loss arising from crossover in device voltage and current waveforms. The heat energy added at each switching interval is now readily measurable with high-bandwidth digital oscilloscopes, which perform waveform multiplication and integration to give instantaneous power and energy change [see Fig.2]. Wherever possible, manufacturers' direct loss measurements are used. For those devices for which loss data is unavailable, switching energy is estimated.

Turn-Off Switching Energy

Turn-off switching loss is often estimated from current fall, tFI. However, experimental waveforms generally show that 50% or more of the turn-off loss occurs during the voltage rise. Therefore Eq.(7) is used.

$$W_{QSW(off)}(\theta) = V_S I(\theta)\frac{t_{FI}}{0.8} \qquad (7) \qquad W_{QSW(off)}(\theta) = \left(\frac{I(\theta)}{I_{QR}}\right)^n W_{QR} \qquad (8)$$

Where switching energy-loss measurements do exist, the relationship between $WQSW(off)$ and switched current may be approximated by Eq.(8), where WQR is the turn-off energy-loss at a reference current, IQR, and n is the gradient of the loss graph plotted on logarithmic axes. Curve fits to published loss graphs for the devices considered later are plotted in Fig.3.

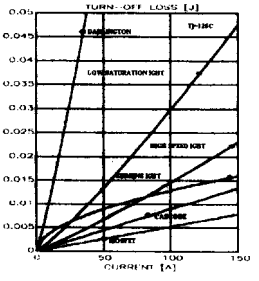

Fig.3 Turn-off energy-loss versus switched-current graphs for various devices after parabolic curve fit

$$W_{QSW(off)}(\theta) = \left(\frac{\hat{I}_O}{I_{QR}} \sin\theta \right)^n W_{QR} \qquad (9)$$

$$P_{QSW(off)}(\theta) = \frac{f_{SW}}{2\pi} \left(\frac{\hat{I}_O}{I_{QR}} \sin\theta \right)^n W_{QR} \int_0^{\pi} \sin^n \theta \, d\theta \qquad (10)$$

With sinusoidally modulated current, $W_{QSW(off)}$ is given by Eq.(9); and Eq.(10) gives the total average loss. The remaining integration in Eq.(10) cannot be solved explicitly and must be approximated by numerical solution. The evaluation of average power-loss relies on specifying switching energy-loss as a continuous function of current which is then easily integrated.

Turn-On Switching Energy

The variation in turn-on energy-loss with current may also be approximated by Eq.(8), or $W_{QSW(on)}$ may be estimated using Q_{RR} data and Eq.(11).

$$W_{QSW(on)}(\theta) = \int_0^{t_{rr}+t_{fs}} v_Q i_Q dt = V_S \left(Q_{RR} + I(\theta) \sqrt{\frac{2Q_{RR}}{di/dt} + \frac{I(\theta)^2}{2di/dt}} \right) \qquad (11)$$

$$Q_{RR}(\theta) = \frac{I(\theta)}{I_{DR}} Q_{RRR} \qquad (12a) \qquad Q_{RR}(\theta) = \frac{\hat{I}_O}{I_{DR}} Q_{RRR} \sin\theta \qquad (12b)$$

With modulated current $W_{QSW(on)}(6)$ must be averaged over an output frequency period. Recovery di/dt is assumed sufficiently high (>400 A/μs), such that Q_{RR} approaches the total stored charge in the diode, and is approximately proportional to forward current. Q_{RR} is then given at any current by Eq.(12a), where Q_{RRR} is the recovered charge at a reference current I_{DR}, and, for sine-weighted PWM, Eq.(12b) gives Q_{RR} at each switching instant, *6*.

With sinusoidal load-current, $P_{QSW(on)}$ at any switching instant is given by Eq.(13), which gives Eq.(14) when averaged over 2π.

$$P_{QSW(on)}(\theta) = f_{SW} V_S \left(\frac{\hat{I}_O}{I_{DR}} Q_{RRR} \sin\theta + \hat{I}_O \sin^{\frac{1}{2}}\theta \sqrt{\frac{2\hat{I}_O t_{rr}}{di/dt} + \frac{\hat{I}_O^2}{2di/dt}} \sin\theta \right) \qquad (13)$$

$$P_{QSW(on)} \approx \frac{f_{SW} V_S}{2\pi} \left(2 \frac{\hat{I}_O}{I_{DR}} Q_{RRR} + 2.472 \hat{I}_O \sqrt{\frac{Q_{RRR} \hat{I}_O / I_{DR}}{di/dt} + \frac{\pi \hat{I}_O^2}{4di/dt}} \right) \qquad (14)$$

When a graph of $W_{QSW(on)}$ measurements is available, $P_{QSW(on)}$ is obtained by averaging Eq.(15) over 2π to give Eq.(16), as previously performed for $P_{QSW(off)}$.

$$W_{QSW(on)}(\theta) = \left(\frac{\hat{I}_O}{I_{DR}} \sin\theta \right)^m W_{DR} \qquad (15)$$

$$P_{QSW(on)} \approx \frac{f_{SW} V_S}{2\pi} \left(\frac{\hat{I}_O}{I_{DR}} \right)^m W_{DR} \int_0^{\pi} \sin^m \theta \, d\theta \qquad (16)$$

Total Power-Loss

The total conduction and switching loss in a bridge-leg switch-diode pair, P_{QD}, is now given by Eq.(17). Note, that diode switching loss is assumed negligible. Where parabolic switching-loss equations are appropriate, P_Q and P_D are given by Eqs.(18a) and (18b).

$$P_{QD} = P_Q + P_D = \left(P_{QCON} + P_{QSW(on)} + P_{QSW(off)} \right) + P_{DCON} \qquad (17)$$

$$P_Q \approx \frac{\hat{I}_O V_{QO}}{2} \left(\frac{1}{\pi} + \frac{M}{4} \cos\phi \right) + \hat{I}_O^2 r_Q \left(\frac{1}{8} + \frac{M}{3\pi} \cos\phi \right) + \frac{f_{SW}}{2\pi} \left\{ \left(\frac{\hat{I}_O}{I_{QR}} \right)^n W_{QR} \int_0^{\pi} \sin^n \theta \, d\theta + \left(\frac{\hat{I}_O}{I_{DR}} \right)^m W_{DR} \int_0^{\pi} \sin^m \theta \, d\theta \right\} \qquad (18a)$$

$$P_D \approx \frac{\hat{I}_O V_{DO}}{2} \left(\frac{1}{\pi} - \frac{M}{4} \cos\phi \right) + \hat{I}_O^2 r_D \left(\frac{1}{8} - \frac{M}{3\pi} \cos\phi \right) \qquad (18b)$$

Net inverter power-stage efficiency, η_{INV} is then given by Eq.(19), where S_O is inverter apparent output power.

$$\eta_{INV} \approx \frac{S_O \cos\phi}{S_O \cos\phi + 6 P_Q} \qquad (19)$$

DERATING POWER DEVICES

Power devices must be operated below their absolute maximum ratings in most applications for an acceptable service life [13,14]. Current, voltage and power, or junction-temperature, derating must also be performed to allow for production spread in device characteristics, tolerance in design calculations, line-voltage surges, and cost effective heatsink design.

Current Derating

The most significant current derating arises from the impracticality of maintaining device case temperature, T_C, at 25°C, i.e. the case temperature for which rated device-current is often specified [i.e. T_{CS}]. Power devices are normally operated with $T_{C(max)}$ at 70-80°C at maximum ambient temperature with practical heatsinks. For case temperatures above 25°C, power-loss must be linearly derated from the maximum allowable value at T_{CS}, P_{QS}, according to Eq.(24), to keep junction temperature, T_J, at or below $T_{J(max)}$.

$$P_Q(T_C) = \left(\frac{T_J - T_C}{T_{J(max)} - T_{CS}} \right) P_Q(T_{CS}) \qquad (24)$$

A stress-ratio derating is then applied by reducing operating TJ below 150°C to give reasonable equipment service life. A value of 110°C will be used as the maximum working junction temperature, $TJ(wmx)$, based on recommendations for non hermetically sealed packages [12].

TRANSIENT THERMAL IMPEDANCE ASPECTS

From the maximum permissible average device power-loss at $TJ(wmx)$, $PQ\ (TJ(wmx))$, the maximum permissible switch current is readily obtained for rectangular current pulses of width tP and duty-cycle ratio D from Eq.(25) by solving for $\hat{I}_O$.

$$\frac{P_Q(\hat{I}_O)}{D} = \frac{(T_{J(wmx)} - T_{C(max)})}{Z(t_P, D) R_{\theta JC}} \qquad (25)$$

Modifying Eq.(25) to include diode loss and $R\theta CH$, thus rendering it usable with bridge-leg modules, gives Eq.(26). This is now used to determine maximum $\hat{I}_O$ by assuming heatsink surface, TH, rather than case, TC, temperature is limited to 70°C.

$$\frac{P_Q(\hat{I}_O)}{D} = \frac{T_{J(wmx)} - \left\{ \left[P_Q(\hat{I}_O) + P_D(\hat{I}_O) \right] R_{\theta CH} + T_{H(max)} \right\}}{Z(t_P, D) R_{\theta JC}} \qquad (26)$$

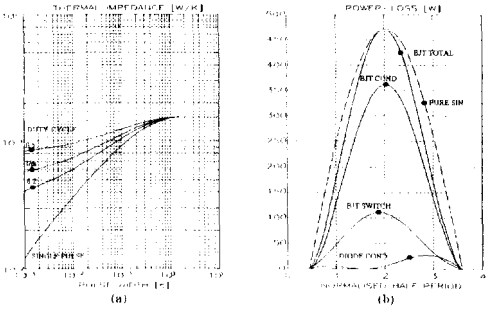

Fig.4 Darlington BJT (a) single-pulse and repetitive transient thermal-impedance characteristics and (b) quasi-instantaneous conduction and switching loss components for f_{SW} 5kHz, f_O 50Hz and T_J 110°C

In sine-weighted PWM inverters, device quasi-instantaneous power pulses, obtained by averaging instantaneous power-loss over each fSW period, approximate to sine pulses [Figs.4 and 5], and an equivalent rectangular power-pulse with the same amplitude and area may be used to give a conservative estimate of heating effect [14,15]. Solving for $\hat{I}_O$ that gives TJ=110°C, or any other T_J for given f_{SW} and f_O values, therefore, proceeds by putting total average transistor and diode loss, PQ and PD, expressed in terms of $\hat{I}_O$, in Eq.(26), and solving for $\hat{I}_O$, assuming PQ originates in a rectangular pulse of amplitude πPQ and width and duty-cycle $tP = 1/\pi fo$ and $D = 1/\pi$,

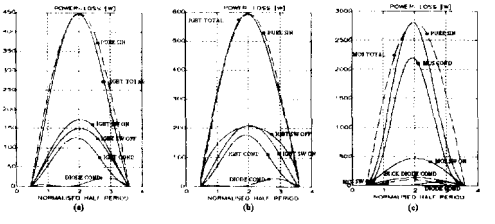

Fig.5 (a) High-speed IGBT, (b) IGBT, and (c) MOSFET, quasi-instantaneous conduction and switching loss components for f_{SW}=20kHz, f_O=50Hz and T_J=110°C operation at peak output current.

EVALUATION OF USABLE DEVICE CURRENT

The evaluation of usable current is most simply determined by calculating device loss and TJ for each fsw or fo value over a range of operating conditions as inverter IO is increased, [Fig.6], and collecting all the $\hat{I}_{O(max)}$ values giving the required $TJ(wmx)$.

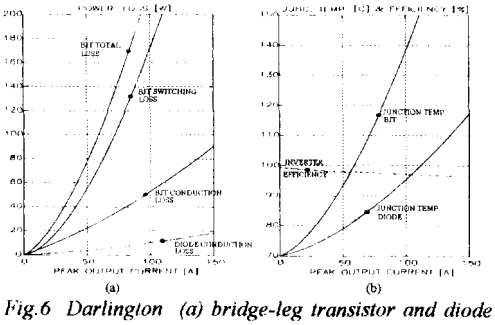

Fig.6 Darlington (a) bridge-leg transistor and diode loss components and (b) junction temperature and inverter efficiency versus peak inverter output current

This is exemplified for the Darlington BJT module in Fig.7 where $\hat{I}_{O(max)}$ variation with f_O and f_{SW} are given. The corresponding net inverter efficiency values may be similarly collected and plotted. The increase in $\hat{I}_{O(max)}$ with fo, seen in Fig.7a, results from the improved filtering effect of package thermal inertia and reduced TJ ripple. Usable $\hat{I}_{O(max)}$ is at least 50%

higher at *fo =50Hz* than *fo=0.5Hz*, making adaptable current limiting of considerable benefit in VVVF applications to enable full device utilisation.

The rapid decrease in $\hat{I}_{O(max)}$ with *fsw*, seen in Fig 7b, results from increasing switching-loss. A simple relationship between $\hat{I}_{O(max)}$ and *fsw* is not specifiable because conduction and switching loss vary faster than proportionately with current. Hence $\hat{I}_{O(max)}$ decreases more slowly than in inverse proportion to *fsw*.

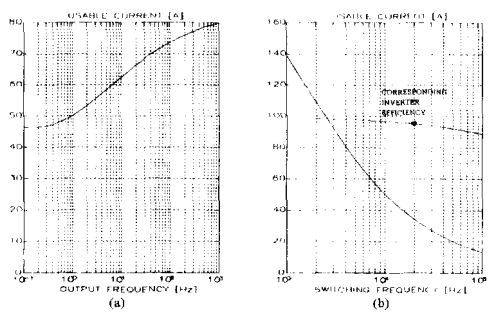

Fig.7 Darlington BJT peak usable inverter output current $I_{O(max)}$ versus (a) inverter f_O with f_{SW}=5kHz and (b) inverter f_{SW} with f_O=50Hz for $T_J \leq 110°C$

From Fig.7 it is seen that, for operation at *fsw=5kHz* and *fo=50Hz*, $\hat{I}_{O(max)}$ is limited to 71A for the Darlington BJT. This is confirmed by practical experience because the device is recommended for and applied in 33kVA, 415V AC inverters [8,11] with a maximum continuous r.m.s. output-current capability of 49.5A [i.e. with 110% continuous current overload because the nominal rated output is 45A r.m.s.], which corresponds to an $\hat{I}_{O(max)}$ of 70A.

Maximum on-state voltage and typical switching parameters are often specified and were used, whenever available, in determining the presented device usable current values [5-12]. Generally, 125°C conduction and switching loss data is used for utilisation prediction and comparison at 110°C. Similarly, 125°C freewheel-diode conduction and reverse-recovery data is used.

VARIATION IN DEVICE UTILISATION

Maximum usable peak inverter current, $\hat{I}_{O(max)}$, is evaluated for a range of 1000-1200V, 150A devices, when operated with *TJ* at 110°C in a 415V inverter. Power loss graphs are given in Fig.8 for the devices when operated in an inverter at the same, $\hat{I}_O$, and illustrates differences in conduction and switching power-loss and their temperature sensitivity.

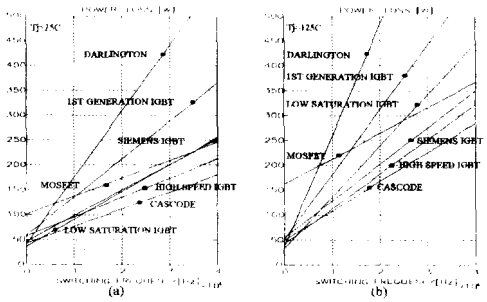

Fig.8 Half bridge-leg conduction and switching loss versus f_{SW} for several 1000V, 150A devices at 20kHz

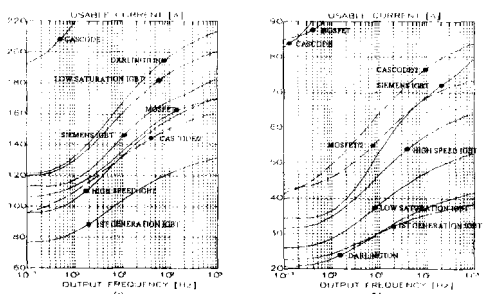

Fig.9 Peak usable current $\hat{I}_O$ versus f_O for devices with T_J = 110°C and f_{SW}= 20kHz (a) if only conduction loss existed (b) with conduction and switching loss

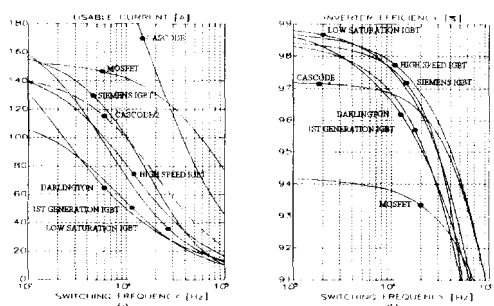

Fig.10 (a) Peak usable current $\hat{I}_O$ versus f_{SW} for devices with T_J = 110°C and with f_O=50Hz (b) corresponding inverter efficiency η_{INV} versus f_{SW}

Usable Switch Current at High Frequency

The variation in usable $\hat{I}_{O(max)}$ and inverter power-stage efficiency, η_{INV}, with *fO* and *fSW* is shown in Figs.9 and 10. The low *RθJC* of the cascode-switch, 150A, single-BJT, compression-capsule package allows

its use at about twice the $\hat{I}_{O(max)}$ of all other devices except the MOSFET switch, as seen in Figs.9b and 10a.

High MOSFET $\hat{I}_{O(max)}$ arises because a 1000V, 150A rating is achievable using five parallel 1000V, 28A modules which give very low $R\omega JC$ and $R\omega CH$ values.

The higher $\hat{I}_{O(max)}$ of the Siemens IGBT, [Fig.10a] over the high-speed IGBT, similarly, arises despite lower efficiency [Fig.8] due to lower $R\omega JC$. The general increase in $\hat{I}_{O(max)}$ with fO seen in Fig.9 arises because of improved thermal filtering, and shows that adaptive active-current-limiting would optimise device utilisation, irrespective of device type.

Fig.9a gives usable $\hat{I}_{O(max)}$ assuming all switching loss is eliminated, and shows that for most devices a factor of three improvement appears possible at 20kHz. This is of interest because it gives an indication of the potential gain in utilisation obtainable using snubber networks or soft switching

The ordering of devices in Fig.9a is determined by on-state voltage and package thermal performance. The higher $\hat{I}_{O(max)}$ is obtained with the single stage BJT in the cascode configuration, the low-saturation-voltage IGBT has the higher $\hat{I}_{O(max)}$ of all IGBTs, and the MOSFET with its high $R_{DS(on)}$ has a relatively low $\hat{I}_{O(max)}$ compared with the faster IGBTs, despite good package thermal performance, because of its significantly higher on-state voltage.

If fO is held constant at 50Hz and fSW varied, $\hat{I}_{O(max)}$ varies for the devices varies as shown in Fig.10a. Corresponding ηINV graphs are given in Fig.10b. Fig.10a illustrates the penalty associated with high fSW inverter operation because, except for MOSFETs, the fall off in usable $\hat{I}_{O(max)}$ is very rapid with increasing fSW, even for the high-speed IGBT.

CONCLUSIONS

The data presented in Figs.8 to 10 is not intended for comparison between manufacturers devices, since some aspects of device performance are not well specified and variability exists in the way in which device data is collected. The intention has been to demonstrate how usable device current varies with modulating signal frequency [Fig.9b], switching frequency [Fig.10], and the level of soft switching employed.

Predicting usable current does not only require knowledge of device conduction and switching loss but also device thermal conditions, such as thermal impedance, equivalent power pulses for steady-state operation, and in the case of transient load changes thermal response to power waveform transients. With wide variation in power-electronics system input and/or output quantities and modulating and switching frequency possible [e.g. VVVF inverters using hysteresis current control] determining usable current in the presence of tolerance in device characteristics and operating conditions is a complex matter. Temperature-regulated active current limiting would ease this by ensuring that power-stages are always usable up to their full capability under transient, as well as steady-state, conditions.

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