Monolithically integrated SiON photonic circuit and silicon single-photon detectors for NIR-range operation

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***Abstract*— The integration of quantum functionalities in photonic integrated circuits (PICs) is attracting intense research efforts nowadays. Many solutions have been proposed for generation, processing and detection of single photons in such quantum PICs. A significant breakthrough would be the monolithic integration of all the three functionalities in a compact, CMOS compatible silicon chip. In this paper we present a solution to integrate monolithically photonic architectures with photon detectors on the same chip. In our device, the light (850 nm photons) propagates within a SiON waveguide, integrated on top of a silicon chip where we realized the single photon avalanche diodes (SPADs). The light is coupled from the waveguide to the detector with a novel and efficient top-down evanescent-transfer approach. The proposed solution for a monolithic integration is fully CMOS compatible. In this contribution, we characterized the performance of the photonic integrated chip, containing several waveguides coupled to SPADs. We detail the functional performance of the fabricated SPADs, as well as the system performance when the injected photons are manipulated and detected within the same chip.**

***Index Terms*— Quantum photonics, photon, silicon, photonics, single-photon detector, SiON, waveguide, SPAD.**

I. Introduction

TODAY quantum photonics represents one of the most fascinating and discussed fields of research, with many efforts directed towards enabling novel applications. A generic quantum photonic system consists of three different parts, corresponding to the generation, manipulation and detection of quantum states of light carried by single photons [1]-[3].

In such systems, a very important and hot-topic nowadays is the integration of single-photon detectors within the quantum PICs. Among the technologies that are exploited for the implementation of single-photon detectors, an important class of devices is the one based on superconducting materials. Superconducting nanowire single-photon detectors (SNSPDs) are now an established technology. They can achieve photon detection efficiency (PDE) close to 90%, dark count rate (DCR) <0.1 cps (counts per second) and good timing jitter [4]-[7]. However, they typically have a relatively large active area (e.g., 100 μm diameter), a PDE dependent on the polarization of light [6] and they are not able to resolve the number of impinging photons (unless used in arrays, but limited to few elements). Another detector, whose operation is based on superconducting materials, is the transition-edge sensor (TES). This device has a very high detection efficiency (>90%) [8], very low noise <1 cps, and has the ability of distinguishing the number of photons impinging on the detector at the same time. However, being calorimetric devices, they are affected by a trade-off between sensitivity and timing performance, and a recovery time in the order of 1 μs.

Although integration of these detectors with waveguides has been demonstrated [9][10], both types of devices require a cryostat to operate at temperatures <4 K. This requirement increases the cost and the complexity of the experimental setup, questioning thus their compatibility with a vision of full integration of the quantum system. Moreover, going towards a fully integrated approach, CMOS compatibility is of prime importance. In literature, few solutions have been proposed, for example, working in the short-wave infrared (SWIR) range (e.g. at 1310 nm or 1550 nm) using a Silicon-on-Insulator (SOI) photonic platform with Ge-on-Si based single-photon avalanche diodes (SPADs) [11]. However, Ge-based SPADs typically have a very high DCR, even when cooled down to 80K÷160K and a PDE of few percent [11].

A different solution, with a better CMOS compatibility, is the use of silicon nitride (SiNx) based PIC platforms. This can be realized on the top of a silicon chip, including silicon detectors, having all the ancillary electronics in the same chip, thanks to the CMOS process. In such kind of solutions, the main research topic nowadays is the efficient coupling between the optically

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transparent waveguide, where the light propagates inside the PIC, and the light-absorbing waveguide (or generically light-absorbing silicon region), where it is photo-detected [3]. As an example, a simple butt coupling of the two waveguides has been proposed in ref. [12], whereas another possible approach is the evanescent coupling between the two waveguides [3]. While in these approaches the detector (e.g. SPAD) is realized in a waveguide shaped form to aid the light propagation, the drawback is that this geometry causes a silicon SPAD to suffer a poor performance and high DCR due to the very small dimensions. In addition, the waveguide shape of the SPAD prevents from the implementation of proper guard-ring structures (implanted or virtual guard-ring), the proper isolation by the Si/SiO2 (or generally silicon-dielectric) interface layers and, generally, a proper electric field "shaping".

In this paper, with the aim to develop a more efficient and CMOS compatible solution, we present a monolithically integrated approach of silicon-oxynitride (SiON) PICs fabricated on top of a silicon substrate. Here, the single-photon avalanche diodes, which will be used as the single photon detectors for an integrated photonic platform, have been fabricated directly within the Si substrate. The light coupling is based on the top-down convergence approach, where we shape the geometry of both the waveguide and the bottom cladding material. This approach has been described in [13] where it has been used to couple a SiON waveguide with a linear mode photodiode. In this paper, we detail the implementation of the integrated photonic structures with single-photon detectors, and characterize the functional performance of the implemented SPADs, fabricated in the same photonic chip, with a modified process compatible with the subsequent waveguide fabrication in the back-end-of-line (BEOL) part.

The approach presented here has several advantages: i) the material used and the fabrication processes are all CMOS compatible (already used in the standard CMOS technologies), ii) it does not require alignments, butt coupling or generally the use of two waveguides made in different materials, iii) it operates at room temperature and iv) the design of the SPADs does not have particular constraints.

In the following sections, we first describe the implemented test chip layout and describe our top-down approach. Then, we describe the performance of the implemented SPADs in terms of noise and detection efficiency. We also describe some preliminary performance characterization of the complete detector and photonic integrated circuit (DPIC), e.g. the variation of the detection count rate when modulating the driving signal of the preceding Mach–Zehnder interferometer (MZI). Finally, we describe the performance characterization of the SPADs when gated and quenching with an external CMOS fast-gater circuit.

II. PHOTONIC INTEGRATED PLATFORM

A. *Top-down photon coupling details*

The electronic-photonic integration approach implemented in this work enables a direct integration of a SiON photonic circuit with silicon single-photon detectors, realized within the same CMOS-compatible fabrication process. The waveguide-detector coupling is achieved by means of a 3D structuring of the waveguide and of the bottom cladding of the PIC through an efficient single lithography and a wet-etching step [14]. We note that while this study uses SiON as the waveguiding material, our approach can be readily extended to others, for example to Si_3N_4 (silicon nitride) PICs.

Fig. 1 shows the schematic representation of the waveguide (WG) and the photodetector structure (SPAD in this case), within the light-transfer region. The photonic-electronic coupling is realized by shaping: i) the waveguide dimensions laterally (PIC plane) and ii) the bottom cladding thickness of the photonic waveguide in the vertical direction. At the

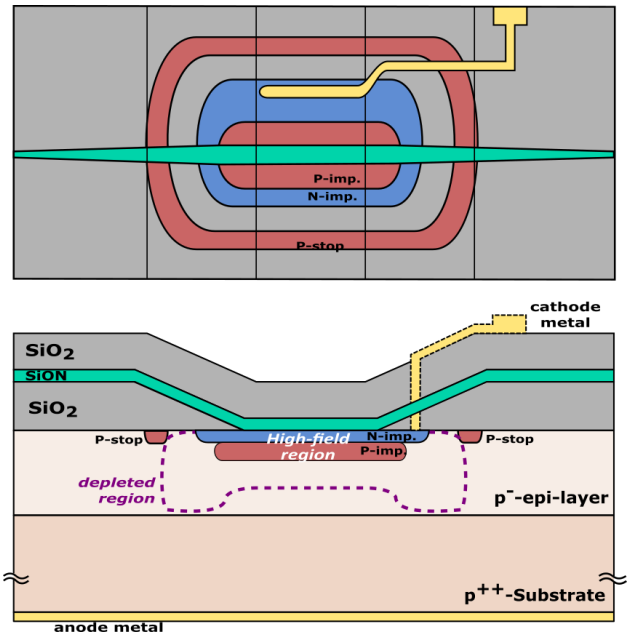

Fig. 1 Schematic representation of the implemented photonic-electronic integration approach. The waveguide is made with SiON within SiO2 cladding, all within the BEOL of the silicon chip including the silicon SPAD detectors (made within a p-type epi/substrate with a n-on-p junction).

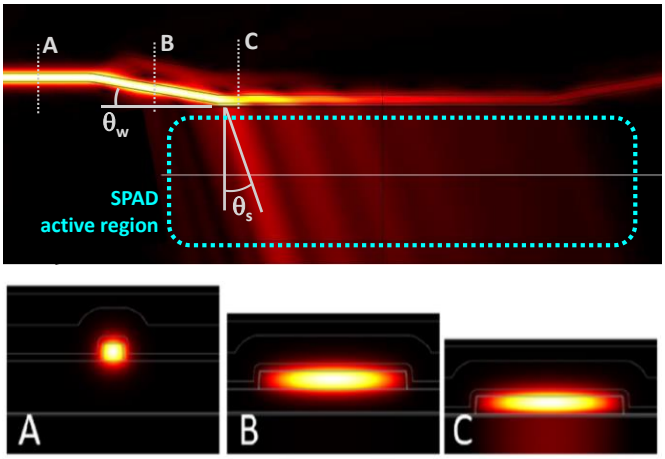

Fig. 2 Simulations of the field distribution in various regions of the waveguide: lateral view of the transition from the PIC to the detector region (top) and cross-sections in different regions of interest, as indicated in the top lateral view (bottom).

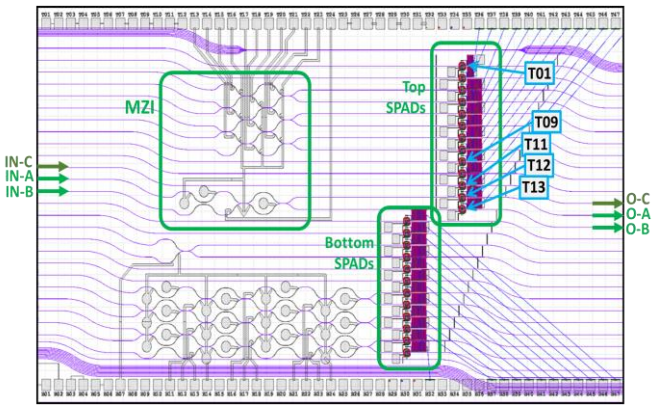

Fig. 3 Layout of the test chip, containing several waveguides, MZIs, and SPADs. The relevant SPADs and waveguides mentioned in the paper have been indicated (waveguides have input on the left and output on the right of the chip).

photodetector location, the waveguide follows the cladding's profile and approaches the substrate adiabatically. Here the optical mode leaks into the silicon epitaxial-layer and the substrate, thus transferring light into the active region of the photodetector. In this first implementation, the substrates are hundreds of micrometers thick, thus the back metal is not contributing in any light reflection, whereas we avoided any top metal on the SPAD region to be able to perform detection efficiency measurement with external light.

The light coupling efficiency from a SiON waveguide to the detector has been numerically simulated using the finite element method. An example of the obtained results is shown in Fig. 2, where it can be seen a lateral view (top) and three cross-sections of the optical modes electrical filed distribution in three noteworthy points (bottom). In particular, in the cross-section (A) it can be seen the lossless propagation (full cladding height) within the PIC architecture. Section (B) represents the region where the waveguide is widened and it also starts to follow a shallow descent toward the substrate. In section (C) the waveguide is in close proximity of the silicon epitaxial-layer, where the light refracts from the PIC into silicon at an angle θ_s of about 26°. This angle is given by the Snell's law as:

$$sin(\theta_s) = \frac{n_{eff}}{n_{Si}}$$

where n_{eff} = 1.594 and n_{Si}=3.673 are the effective index of the waveguide mode and of the silicon substrate at the wavelength of 850 nm, respectively. The choice of the operating wavelength, being here 850 nm, is based on a tradeoff between two aspects: the detectors would be much more efficient towards the visible range, but, on the other side, decreasing the wavelength is challenging for the scattering and material losses of the guiding part of the photonic circuit.

The amount of light transferred and absorbed within the epi layer depends on the transmission (T) at the waveguide-to-Si interface, the epi layer thickness (t_{epi}) and the absorption depth (L_{abs}) of photons at the given wavelength. As an example, a coupling efficiency of 46% at a wavelength of 850 nm has been estimated from the fraction of the optical power absorbed within a 10 µm thick epi-layer [13]. However, when calculating the photon detection efficiency (*PDE*) of the SPAD, additional factors must be considered: the effective collection region (t_{abs}) might be different from the epitaxial layer thickness (as a first approximation we can consider them equivalent) and photo-generated carriers have a certain probability to trigger a self-sustaining detectable avalanche pulse, i.e. the avalanche triggering probability (P_{trig}):

$$PDE = QE \cdot P_{trig} = T \cdot \left(1 - exp\left(-\frac{t_{abs}}{L_{abs}(\lambda)}\right)\right) \cdot P_{trig}$$

As reported in [15][16], the triggering probability depends on the type of carriers triggering the avalanche and it increases with excess bias (i.e. the difference between applied reverse bias to the SPAD and its breakdown voltage). As shown in Fig. 2, it is possible to engineer the amount of the coupling of the waveguide with the underneath detector. Indeed, in our case a small fraction of light intensity is not transferred but transmitted and could be used for referencing. For this reason, we designed uninterrupted waveguides that reach the opposite edge of the chips, allowing thus to measure the light power exiting the PIC.

B. SPAD layout

The SPADs are based on a technology derived from FBK RGB SiPMs [17]. The nominal breakdown voltage, noise and detection efficiency are similar to what reported in [17] (but being single elements, the fill-factor is not included in the PDE). Moreover, the overall manufacturing process has been slightly modified because of the different BEOL procedures (e.g. by removing the polysilicon resistor and employing different BEOL dielectric thicknesses).

As shown in Fig. 1, the SPADs are based on a deep p implant, a shallow n+ implant and a guard ring structure, which is mostly composed by a p+ shallow implantation (not reported here the other additional steps).

Concerning the SPAD layout, contrary to the Silicon Photo-Multiplier (SiPM) microcell layout philosophy, where the fill factor (FF) needs to be maximized, here we implemented an oval oblong shape for the shallow implant and the deep (enrichment) implant, surrounded by a guard ring with the same shape. This is because, on contrary to typical applications of SPAD detectors, here the light is injected from the waveguide mainly along only one direction.

The pitch between SPADs in the implemented chip is 150 µm and their nominal active area is about 860 µm^2. Because of the virtual guard ring structure, as discussed in [16], the "effective FF" is smaller, but this is not an issue in this application: indeed the SPAD active area has been made slightly bigger than the area where the waveguide lays on the Si substrate, along the light propagation direction.

C. PIC layout and fabrication

Fig. 3 shows the layout of the implemented 0.5 × 1 cm^2 chip, containing both photonic components and photo-detectors (SPADs). There are several waveguides with inputs and outputs on opposite sides of the chips. In some of them, there are photonic elements such as MZI's or a network of MZIs, which can be reconfigured using thermo-optical phase shifters (heaters) on one of the MZI arms. The SPADs are organized in

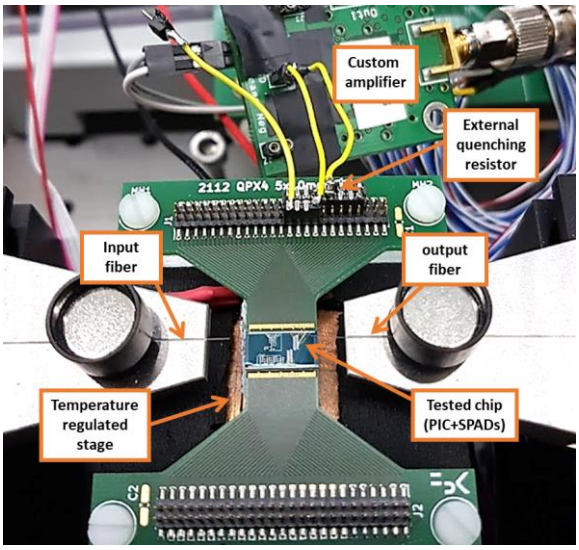

Fig. 4 Picture of the custom carrier board, placed in the temperature controlled setup. The heaters of the MZI and the SPAD anodes of the PIC are wire bonded to the high-connection-density PCB.

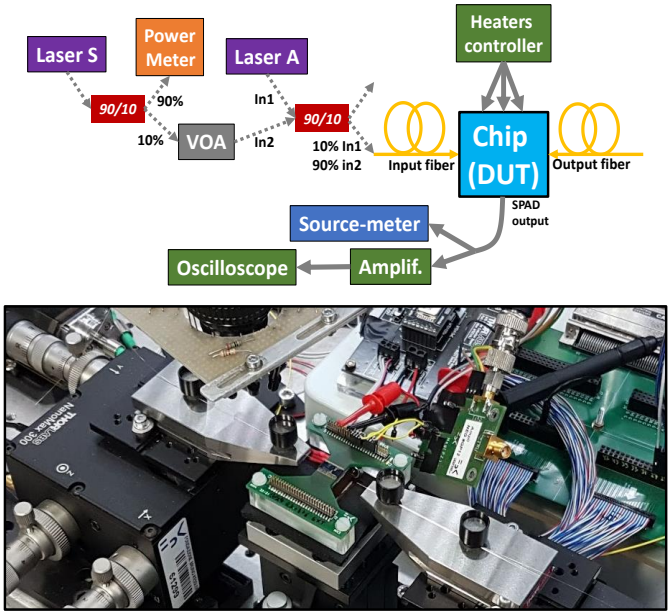

Fig. 5 Schemtatic representation of the measurement setup used for the functional performance evaluation of the integrated SPADs+WGs (top) and picture of the chip and fibers micro-positioning stages (bottom).

two arrays of 12 and 13 devices, one on the top waveguides and one on the bottom waveguides. The chips have been fabricated in several replicas on a 6" silicon wafer, but with many layout and process splits, eventually having a total of about 36 nominally identical chips per wafer. In this paper we report the performance of only the most promising process split.

In our process, the devices are fabricated starting from p-doped epitaxial Si substrates. Then the SPADs are realized by means of three different lithographic and ion implantation steps. After SPAD fabrication, the substrates were covered with a thin SiN layer, which acts as a wet etch-stop film during the definition of the 3D structured SiO_2 cladding. Then, a 1.5-µm thick SiO_2 film is deposited, in which the shallow-angled triangular wedge structures are realized at the detector locations using wet etching in buffered hydrofluoric (BHF) acid (more details on the fabrication can be found in [13] and [14]). The PIC layer is realized by depositing a Si_3N_4 film, followed by a PECVD SiON film on top of the structured cladding, patterned and defined by reactive ion etching (RIE). Next, after dopant activation a second deposition of a thin Si_3N_4 and a top SiO_2 cladding is performed. Finally, two different metal layers are sputtered, patterned, and etched to allow the connection of the SPADs and the thermo-optical control of the photonic elements in the PIC [18].

III. Measurement Results

A. *Wafer level measurements*

The SPADs contained in the manufactured chips have been tested with automatic probers. In particular we employed a customized probe-card which include an external high value quenching resistor (1 Mohm) to properly bias the SPADs and be able to measure the reverse leakage current (below the breakdown voltage), as well as the dark current (above breakdown voltage) [19]. Good devices have been selected based on the breakdown voltage value and dark current (below a certain threshold, corresponding to an estimated DCR of about 5 kcps). The yield in this first production was limited, due to some manufacturing-process related issues, which have been identified and will be fixed in the next production run. However, the uniformity in breakdown voltage is good (around 0.7 V maximum variation among working devices) and the spread in the dark current (proportional to the spread in the primary dark count rate) was generally within 1 up to 2 orders of magnitude.

B. *Functional performance characterization*

The functional performance of the SPADs, such as the noise and the detection efficiency, have been measured on some of the produced chips. One SPAD at a time has been tested by connecting it to an external 1 Mohm quenching resistor. The current signal from the quenching resistor was amplified by a trans-impedance amplifier with a gain of 1000 V/A.

We produced a custom high-connection-density PCB to host the chip and to wire-bond all the photonic components and the SPADs (cathodes and common anode), as shown in Fig. 4. The PCB has a peculiar hourglass shape, because of the need to have direct access to the right and left side with optical fibers (to inject and collect the light from the waveguides) while having the electrical signals from the chip on the top and bottom sides.

For the functional characterization of the noise of the SPADs, the chip and the amplifier board have been placed in a climatic chamber, in dark condition. The pulse signal from the amplifier has been digitized with an oscilloscope (Agilent DSO9104A, with 1GHz bandwidth) and periodically transferred to the PC running a LabVIEW software for the pulse identification and analysis, following the method described in [15], which has been developed for SiPMs but that can be adapted for SPADs. In particular, we collect long time-windows of pulses, e.g. 200 ms long, with a high time resolution, e.g. 8 ns time step (this

numbers can be adapted depending on the count rate). Then with the software, we filter the signal, we identify the pulses and we plot their amplitude and inter-time (i.e. time after the previous pulse). By creating a scatter plot and a histogram of the inter-times (with logarithmic axis and logarithmic binning), we can distinguish the primary dark events (exponentially distributed, because of the Poisson statistics) and the correlated noise, e.g. afterpulsing, happening at lower inter-times and with variable amplitude.

The detection efficiency of the SPADs has been measured both with top external illumination (i.e. the PDE of the SPADs alone) and with laser light injected in the waveguide and detected by the SPADs thanks to the electronic-photonic integration approach. The latter is the direct measurement of the detection efficiency of the system (waveguide and detector), including the light coupling efficiency of the waveguide-to-silicon interface.

For the measurement of the PDE with external illumination, we used a dark box and we illuminated the SPADs with perpendicular light coming from an integrating sphere, to have uniform and calibrated illumination. The setup and method are the ones described in [20]. We used pulsed light and calculated the PDE based on Poisson statistics, using the probability of no-detection in a fixed synchronous time window.

For the measurement of the PDE with laser light injected in the waveguide, as well as for other measurements of SPAD count rate we used the setup reported in Fig. 5. The chip and the hosting board are mounted on temperature-regulated stage (based on thermoelectric cooler, TEC). Two fibers are precisely aligned on left and on the right (typically light is injected from the left side and residual light collected from the right, unless otherwise specified). Light from an 850 nm pigtailed laser is fed into a 90/10 power splitter: 90% of the power is sent to a Power Meter for monitoring, while the remaining 10% is coupled to a series of Variable Optical Attenuators (VOA). The VOA output is then sent to a 90/10 mixer, with the 10% output injected into a polarization control stage and finally coupled into the chip with lensed inverse-taper fibers actuated with piezo controllers. On the other input of the mixer, another laser is injected for alignment purposes (turned on only during initial alignment, off during the measurement).

C. *SPAD noise*

We report the noise as a function of excess bias for some of the tested SPADs, measured at 20°C. The primary DCR and afterpulsing are extracted from the inter-times histogram (corrected for the pulse amplitudes). An example is reported in Fig. 6 for the SPAD T12 of the tested chip. It can be seen that afterpulsing is lower limited in time at about 1.5 µs. This is due to the external quenching used for these SPADs, and due to the large capacitance of the SPAD and external interconnections. This non-optimal quenching mechanism was used because of its simplicity and was necessary to operate the SPADs implemented in the PIC, which were fabricated bare, without any integrated quenching circuit.

The comparison of the DCR of some of the tested SPADs is reported in Fig. 7. The DCR is in the order of few tens of counts per second (cps) at near room temperature. This is in line with state-of-the-art commercial products [21][22]. It can be seen that there is a spread of less than one order of magnitude (for SPADs in the same chip). This is mainly due to the intrinsic variability of noise level in the fabrication process, but also because of the preliminary and non-optimized manufacturing process, which has led not only to a non-optimal yield but also to a spread in the noise level.

The variation of noise (primary DCR) with temperature has also been measured, and an example of DCR at 10°C, 20°C and 30°C, as a function of excess bias is reported in Fig. 8, for the

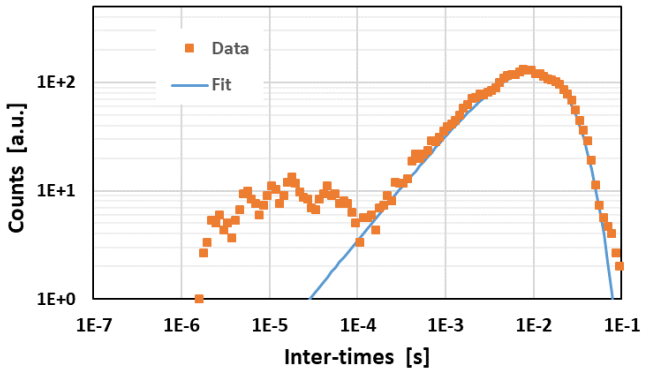

Fig. 6 Example of measured inter-time histogram, for SPAD T12, with exponential fit on the primary events used to extract primary DCR and afterpulsing, at 20°C, at 6V of excess bias.

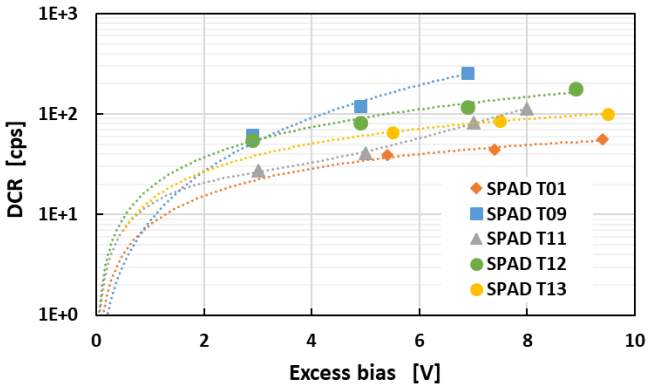

Fig. 7 Measured primary DCR of different tested SPADs, at 20°C, as a function of excess bias. Dashed lines are polynomial fits.

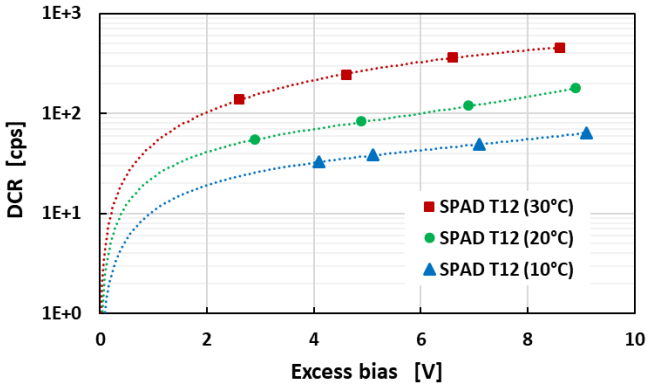

Fig. 8 Example of primary DCR dependence on temperature, as a function of excess bias, for tested SPAD T12. Dashed lines are polynomial fits.

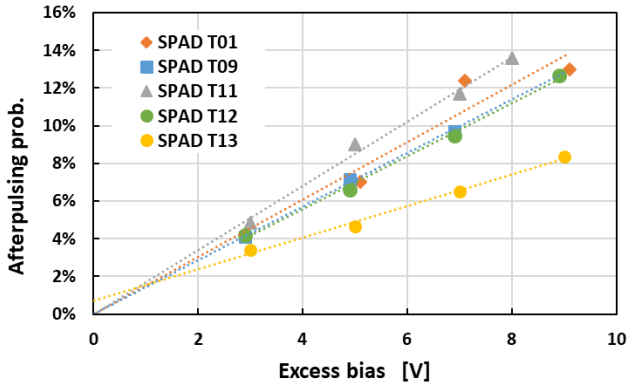

Fig. 9 Measured afterpulsing probability of same SPADs in the tested chip, with external passive quenching circuit.

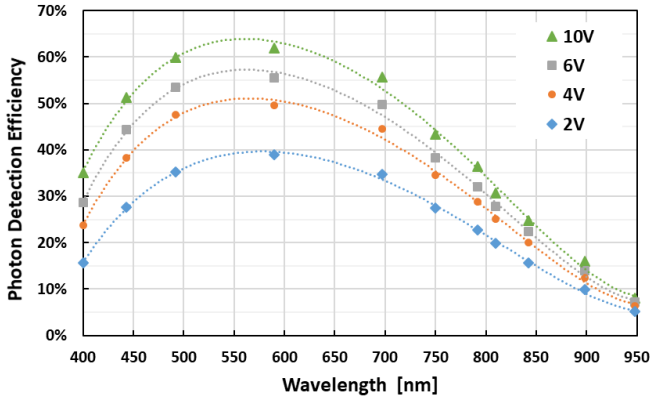

Fig. 10 Measured photon detection efficiency (PDE) of one of the tested SPADs, as a function of wavelength at different excess biases. Points represent the measured wavelengths, dashed lines are polynomial fits.

SPAD T12. The dependence is compatible with what reported for FBK RGB and NIR SiPM and SPAD technologies [15][17], i.e. approximatively DCR increase of a factor 2 every 10°C.

We also characterized the afterpulsing probability of these SPADs (estimated from inter-times plots). Results are reported in Fig. 9. The values are high with respect to the state-of-the-art and with respect to typical values of corresponding SiPM technology [17]. As discussed above, this is because of the external quenching circuit, producing an avalanche charge much higher than what is typically flowing with integrated passive quenching or what can be obtained with a proper and faster active quenching circuit [23]. We measured a gain (i.e. avalanche charge divided the elementary electron charge) of more than one order of magnitude higher than what reported in [17]. For these reasons we tested these SPADs, integrated in the PIC, also with a faster SPAD-"gater" (and quenching) circuit, as detailed in the last section. Both the maximum count rate and the afterpulsing performance are expected to be improved with the use of such fast quenching and reset circuit, matching the performance needed for typical photonic circuit applications.

D. SPAD detection efficiency

We characterized the PDE of the SPADs with external perpendicular illumination and operated at room temperature. We used several pulsed LEDs, at different wavelengths and fitted the results with polynomial lines. The results are reported in Fig. 10. In this case, the PDE was estimated considering for the photon flux, the nominal active area of the SPAD, thus not compensating for any border effect [15]. Therefore, the PDE in the very center of the SPAD area could be higher than the reported values.

The PDE peaks at about 570 nm, as expected for this type of silicon detector [17], and it shows values around 65% in the peak, and of about 25% at 850 nm, at 10 V excess bias. These values reduce to about 50% in the peak and 20% at 850 nm at 4 V excess bias, just because of the lower triggering probability of the avalanche (despite maintaining the same quantum efficiency). The wavelength of 850 nm is the one used for the tests of the photonic chip, as reported in the next section.

E. Photon rate modulation with MZI

The photonic chip has been operated with external laser-light illumination (850 nm). The injected light was modulated and detected within the PIC. We used inversely-tapered fibers coupled to the SiON waveguides in the PIC (Fig. 4) and ensured proper alignment by using the alignment laser and the value of the power at referencing output.

The light was injected into the waveguide marked as "IN-B" in Fig. 3, fed to the MZI and split into two output waveguides, coupled to SPADs T12 and T13, where the respective count rates were measured. The injected light power in the photonic circuit was monitored by means of the power meter, as visible in the schematic of the setup in Fig. 5. With such configuration, we measured the count rate in the two SPADs: i) in dark condition, with laser off, and ii) with laser light on. The count rate in the two SPADs have been measured separately, by connecting one or the other device, but always monitoring the input light power before the fixed VOAs on the power meter. The "net count rate" (NCR) in the two SPADs has been calculated subtracting the dark count rate to the light count rate.

To estimate the best working condition for the photon flux we evaluated the response of the SPADs when changing the light intensity, to find a proper level for these measurements (not saturating the detector). The resulting net count rate (of SPAD T12) as a function of the power detected in the power meter, i.e. before attenuators (VOA and splitter) is shown in Fig. 11. It can be seen that with NCRs higher than about 900 cps, the dead-time of the SPAD starts to limit the linearity in the count rate vs photon flux. As discussed above, this is due to the external passive quenching (and recharge) circuit, which is a non-optimal configuration, leading to a very long recharge time constants. The main reason for this is the high capacitance of the bonding pads and of the connectors, which have to be discharged and recharged during every avalanche pulse. This does not represent a critical issue as it can be avoided with the use of active quenching or integration of the resistance before the bonding pad.

To limit the saturation, we operated with a light power of around 3 µW, thus net count rates in the order of few hundreds of counts per second.

In such conditions, we modulated the MZI by changing the heater current (thus heating power) on one of the arms and we

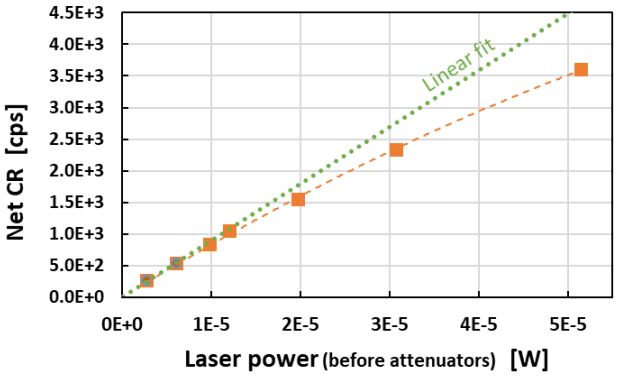

Fig. 11 Measured net count rate (CR) of SPAD T12 as a function of the measured light power on the power-meter (before attenuation stages). The linear fit on the first points is represented, i.e. without count rate saturation.

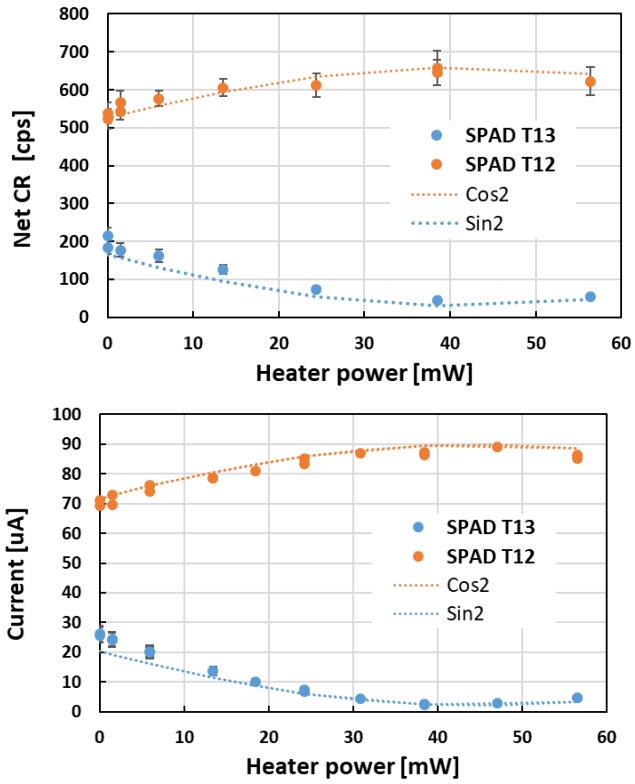

Fig. 12 Measured net count rate of SPAD T12 and T13, as a function of the MZI driving heater power (top) and measured photocurrent of the same two SPADs when operated well below the breakdown voltage, in linear photodiode mode, as a function of the MZI driving heater power (bottom). The dashed lines are polynomial fits of measured data.

measured the NCR on the two SPADs. The results are shown in Fig. 12 (top). It can be seen that the light power is exchanged between the two waveguides and this is properly detected in terms of photon rate in the two SPADs. Unfortunately, in this first implementation of the photonic chip the single-arm thermo-optic actuators on the MZIs could not achieve a full π-shift within the power limit of the heater itself, and the MZI is close to the [1 0] condition (i.e. full open on one arm and closed to the other one). Most of the power remains in the top waveguide even when spanning the driving signal on the whole power sweep of the heater. This limitation will be removed in the next implementations. To verify these results, we also

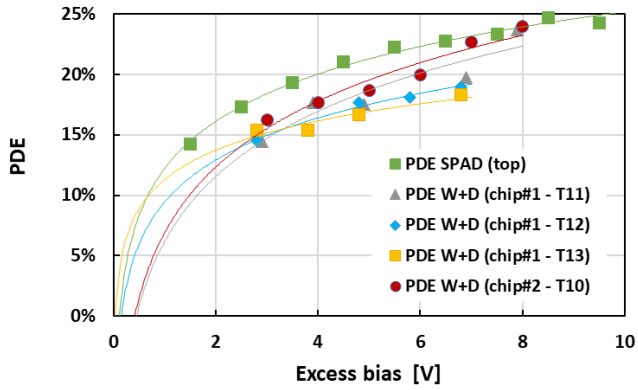

Fig. 13 Measured PDE of SPAD T13 (light from the top), and PDE of the waveguide+detector (W+D), of SPAD T11, T12, T13 of chip #1 and of SPAD T10 of another chip #2, as a function of excess bias.

measured the light power within the two waveguides with the two SPADs operated as linear photodiodes, i.e. biased well below the breakdown voltage. To do this, the input light power has been significantly increased, and the photodetectors were operated without quenching resistor, measuring their photocurrent with a source-and-measurement unit. As reported in Fig. 12 (bottom), the variation in photocurrent reflects the variation in the measured count rates. The measurements in photon-counting mode and in linear mode have been both fitted with $\sin^2$ and $\cos^2$ functions, changing amplitudes but keeping the same frequency and initial phase shift. The results are shown in the figures as dotted lines. It can be seen a good agreement, indicating the same behavior of the MZI with high light power and in single-photon regime. In our case we added also a fixed amplitude to the fit, to take into account the non-zero minimum, which might be likely due to a non-perfect modulation of the MZI, related to the non-pure polarization of input light.

F. System detection efficiency

With the same setup used in the previous section, we estimated the "system detection efficiency". In our case, since we aim to a future complete integration of the single-photon source, the photonic components and of the detectors all on the same chip, we measured the detection efficiency as the ability of the integrated SPADs in detecting the photons that are propagating inside the waveguides of the PIC. Thus, this include the PDE of the SPAD itself, and the coupling efficiency of the photons from the waveguide to the detector.

First, we estimated the losses of the photonic part of the chip, assessed by Beer-Lambert fitting the transmitted optical power of waveguides of different length, placed on dedicated test chips fabricated on the same wafer. We estimated about insertion losses of 6 dB per facet and a propagation loss of around 1.4 dB/cm. These insertion losses can be considered relevant for a quantum experiments but in our specific case this can be neglected as a first approximation since the PIC has been designed with the aim of integrating the light source on the same chip, thus no fiber injection.

For the measurement of the detection efficiency, the precise

estimation of the light intensity at the SPAD location is not straightforward. The light losses in the setup and in the PIC can be estimated with high light power (e.g. by means of power meters and measuring the photocurrent), but then when including attenuators, approaching the single-photon level, thus photon-counting mode, this method cannot be used. Therefore, in our case, we characterized all losses, including the injection losses from optical fibers to waveguides, and the propagation loss of the integrated waveguides, with high light power, and we characterized the overall attenuations of the external optical-fiber based system. Eventually, we combined the two together to estimate the power (photon rate) at the SPAD location, for the detection efficiency estimation.

As a first measurement, we used the SPADs T12 and T13 as in the previous section. The total light intensity injected in the PIC has been estimated to be about 4100 photons per second. Due to the MZI, thse photons are divided between the two waveguides associated with the two SPADs, where we measured net count rates of 441÷560 for SPAD T13 and 287÷185 for SPAD T12, at 3 V of excess bias. These count rates are measured with the minimum and maximum MZI driving signal intensities. Given these numbers, we estimated a PDE of the two SPADs combined (i.e. summing the NCR, divided the number of injected photons in the PIC, considering waveguide and injection losses) to be in the order of about 17%.

Secondly, as a more direct measurement, we also measured the PDE of SPAD T11 (which does not have any MZI, thus light is going directly towards the SPAD), and of SPADs T12 and T13 but with light injected from the right side of the chip, thus not having any MZI in the light path between injection point and SPADs. The different light attenuation with injection from the left side or the right side have been estimated and taken into account. In this case, we performed the measurements at different excess biases. The results are shown in Fig. 13. We measured also another SPAD (T10) from a second chip (chip #2), to check possible variations in the waveguide and in the coupling efficiency of the fibers to the PIC.

From this second set of measurements, the average waveguide-and-detector (W+D) PDE is in the order of 17% at 4 V of excess bias, increasing towards almost 20% at 7 V excess bias. By comparing these results with the PDE measured with external illumination, on SPAD T13, we can estimate a light coupling efficiency (from the waveguide to the SPAD) between 76% and 85%.

Both the PDE of the SPAD and the coupling efficiency can be considered promising results, even though the PDE can be further improved within the new production runs, for example by means of thicker epitaxial layers (see simulations in [19]).

G. Stray-light estimation

We preliminary evaluated also the effect of stray light in the PIC, i.e. light not-properly coupled to the main waveguide and travelling in the cladding, or light scattered from neighboring waveguides and ending being detected by the SPAD under analysis. We performed a preliminary evaluation of the sensitivity of SPADs to the stray light generated when injecting

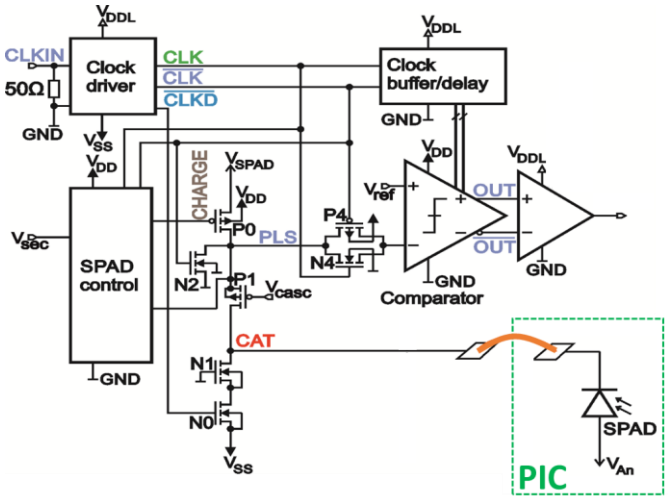

Fig. 14 Schematic representation of the gater internal circuit and external connections to the SPAD in the PIC.

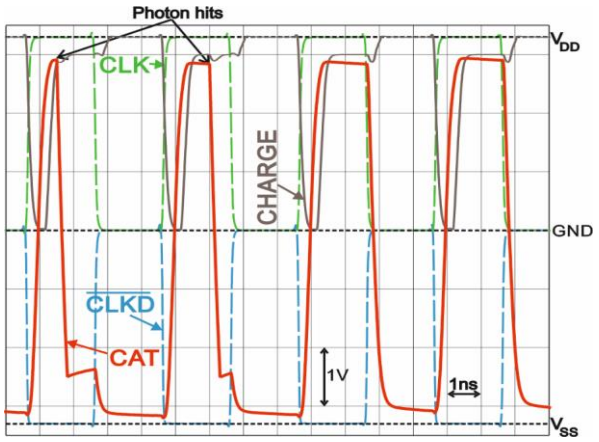

Fig. 15 Simulated signals at the important nodes of the gater circuit, in case of triggering or no-triggering of the SPAD avalanche pulse.

the photon flux into a neighboring waveguide.

As an example, we injected the light from the right side of the chip #1, in the waveguide associated to SPAD T13 (i.e. from the point indicated as “O-B” in Fig. 3), while monitoring the count rate in SPAD T12. With a procedure similar to the one used in the previous section, we estimated a detection efficiency of about 0.04%.

In a second test, we monitored the count rate in SPAD T13, when injecting the light first from the left and then from the right side in the waveguide associated to SPAD T11 (i.e. from points marked as “IN-C” and “O-C” in Fig. 3, which is two waveguides above the one associated to T13). In the former case, we estimated a detection efficiency around 0.03%, whereas in the latter approximately 0.16%.

Such results indicate a good isolation between adjacent waveguides and neighboring SPADs. This is due to a proper light confinement in the waveguides and to the presence of dedicated light-blocking structures in the BEOL (but outside the waveguide region) around each SPAD and near the edge of the chip. Among such structures we implemented for example deep trenches within the oxide layers all the way to the silicon and filled with aluminum, acting as barriers for the light propagating in the oxide cladding.

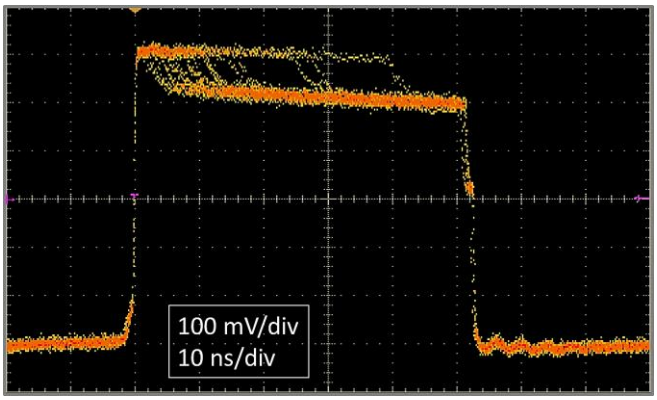

Fig. 16 Example of measured signal at the CAT node of the gater, with SPAD connected and biased at about 1 V excess bias (waveform collected with 10x attenuation).

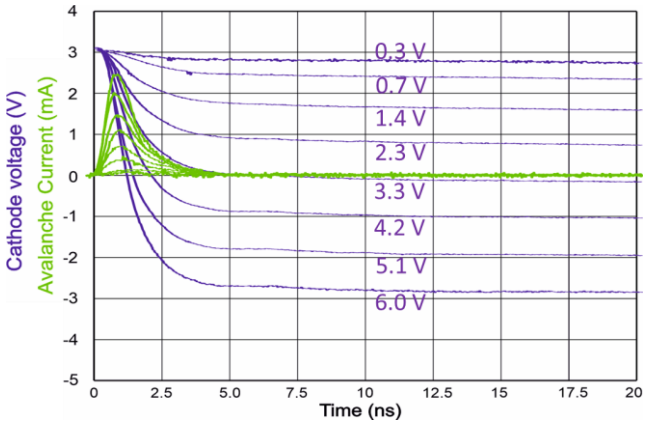

Fig. 17 Measured cathode voltage signals drop (blue curves: excess bias increasing from top to bottom), at the avalanche build-up, for different excess biases, and estimated associated SPAD avalanche-pulse current, based on the measured overall node capacitance (green curves: excess bias increasing from bottom to top).

IV. SPAD WITH FAST GATING CIRCUIT

Up to now, we described the SPADs while working with a non-optimal external quenching and reset circuit, introducing long dead-time. Here instead, some of the produced SPADs have also been tested when wire-bonded to a fast external gating circuit (developed by TUW) [24]. This is important to assess the overall photonic circuit performance in application where, for example, a high repetition-rate laser source is used to inject the photons. When gated, a SPAD has defined, mostly periodic time slots, where it is set to active and ready for photon detection, until a photon is detected or until the end of the active period.

The "gater" circuit schematic is shown in Fig. 14, and described in detail in [24]. It operates by driving the cathode node above and below the breakdown voltage (for active avalanche quenching), while the anode bias is fixed. The circuit has been fabricated in a CMOS 0.35 µm technology, with a nominal bias supply voltage of 3.3 V. Thanks to a cascoding topology, the SPAD cathode can be driven up to a swing of about 6.6 V. Thus, the excess bias of the SPAD could be adjusted between 0V to max. 6.6V in changing the anode voltage V_{An}. During the positive gating pulse the cathode of the SPAD is left floating (i. e. the quenching switch consisting of N0 and N1 and the charging switch formed by P0 and P1 are open, see Fig. 14) and the SPAD is ready for photon detection. An example of the cathode voltage and of the simulated signals is shown in Fig. 15. If a photon is absorbed and triggers a self-sustaining avalanche, the avalanche current discharges the capacitance of the SPAD and the cathode potential (CAT) drops earlier (1st and 2nd red pulse in Fig. 15), i. e. before the quenching switch discharges the SPAD (at the end of the gating pulse, like in 3rd and 4th red pulse). Here V_{SPAD}, V_{DD} and V_{DDL} are +3.3V, whereas V_{SS} is -3.3V.

In our measurements the driving signal was at 10 MHz (CLKIN). The driving voltage swing has been kept fixed, while changing the anode voltage (V_{An}). The cathode voltage was monitored via a pico-probe 35 from GGB Industries with a bandwidth of 26 GHz and an attenuation of 10. Fig. 16 shows a superposition of the cathode signals (for absorption of randomly distributed photons at different times after the start of the gating pulse), when the excess bias is about 1V. It can be seen that the avalanche current discharges the capacitance of the floating cathode of the SPAD to the breakdown voltage during the gating pulse (on-time) of 50 ns.

The avalanche quenching time, as well as the active gating slopes, are in the order of a few nanoseconds. When increasing the excess bias, the amplitude of the avalanche pulses increases, while the positive (raising) gating pulse swing stays the same. More precisely, the avalanche duration, calculated as 80%-to-20% fall times of the measured pulses, are between 3 ns (at low excess bias) and 1.5 ns (at high excess biases).

A. SPAD capacitance and avalanche current estimation

To be able to extract the actual current flowing within the SPAD, we estimated the SPAD capacitance. Measurements of several SPAD samples wire-bonded to gating chips resulted in an average overall cathode node capacitance of 630 fF. When excluding from such measurements the active probe contribution and the input capacitance of the gating circuit, we estimate a SPAD+PAD capacitance of about 402 fF average value, with 19 fF standard deviation between the samples.

When considering the total capacitance (C_{Cat} = 630 fF), the avalanche current as a function of time is obtained (see Fig. 17) when applying the method described in [24].

$$I(t) = C_{Cat} \cdot \frac{dV_{Cat}(t)}{dt}$$

The maximum avalanche current increases with the excess bias and the maximum of the avalanche current is reached earlier due to higher electric field strength and stronger impact ionization. The SPADs developed here are characterized by an avalanche build-up time of about 1 ns, which is a factor of 2 to 3 faster (shorter) than that of the SPADs integrated in 0.35 µm CMOS and characterized in [24].

V. CONCLUSIONS

We presented a new efficient and CMOS compatible approach to implement a monolithic electronic-photonic integration of a PIC based on SiON waveguides and silicon single-photon avalanche diodes (SPADs) as NIR single photon detector. The light coupling is based on a novel top-down

convergence approach, based on the shaping of both the waveguide and of the bottom cladding material. This realizes an evanescent light coupling between the waveguide and the SPAD underneath. This approach has several advantages: i) the material used and the fabrication processes are all CMOS compatible, ii) it does not require alignments, butt coupling or the use of two waveguides made in different materials, iii) it can be operated at room temperature and iv) the design of the SPADs does not have particular restrictions.

We fabricated the first, to our knowledge, PIC based on SiON waveguide and with integrated silicon SPADs. We characterized the SPAD performance, both when operated with external light and when detecting the light propagating in the integrated waveguides. The SPADs implemented in the electronic-photonic integrated chip are characterized by a moderately low dark count rate (in the order of 100 cps at room temperature), a high photon detection probability (>50% in the green wavelength region and >20% at 850nm) and a short avalanche build-up time. Such performance makes these SPADs well appropriate for short gating pulses in a photonic quantum simulator.

We also operated the PIC with integrated detectors in linear mode with external laser light injected into the waveguides, modulating the photon propagation in the PIC by means of MZI, and then detecting the photons with the integrated SPADs, all close to room temperature. We were able to modulate the photon propagation between two adjacent waveguides and detect them by two different single-photon detectors, and we also measured the system detection efficiency (i.e. PIC+SPAD), being between 17% and 20% (depending on the excess bias of the SPADs). This indicates a coupling efficiency between the waveguide and the detectors in the order of 80%.

Such performances are very promising and are the baseline for future developments at FBK, aiming to more efficient detectors and complex electronic-photonic integrated platforms.

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