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Original scientific paper

Four-Leg Inverter Based on Three-Dimensional Space Vector Modulation Method for Desired Output Frequency

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Abstract: Conventional six-switch inverters, designed for balanced three-phase systems, face challenges in low-voltage networks with mixed single-phase and three-phase loads, leading to voltage imbalances. This imbalance adversely affects equipment, especially protection devices and power electronic converters. The increasing use of power electronic devices in industries with nonlinear loads has driven the adoption of four-leg inverters to handle neutral currents during unbalanced load connections in three-phase networks. This shift introduces challenges in pulse width modulation, particularly in the application of Space Vector Modulation (SVM). This work proposes a novel control strategy using a direct 3D-SVM approach, effectively determining switch states for voltage capacitor balancing and precise output current control. The study's main focus is presenting an advanced control strategy for a four-leg inverter utilizing the 3D-SVM technique to operate efficiently under highly unbalanced loads in distribution networks. The goal is to achieve balanced output voltages and currents under varying load conditions while maintaining the desired variable output frequency. Simulation results validate the proposed control strategy, showing a Total Harmonic Distortion (THD) of output current is 2.06% at 50 Hz and 2.55% at 25 Hz under balanced load, same thing in second case under unbalanced load, the THD is 1.65% at 50 Hz and 2.10% at 25 Hz. with similar under nonlinear load, the THD is 1.94% at 50 Hz and 2.46% at 25 Hz. Importantly, all outcomes fall within IEEE Standard 519-1992 for harmonic limits, highlighting the robustness and reliability of the proposed control approach.

Keywords: balanced load; four-leg inverter; output frequency; performances analysis; power quality improvement; 3D-SVM technique

1 INTRODUCTION

Many electrical power conversion systems, including distributed power generation and uninterruptible power supply [1, 2], require three-phase, four-wire systems to create a path that compensates for the zero-sequence component and prevents the distortion of the output voltage wave. Nonlinear and unbalanced loads generate zero-sequence components in the voltage and current waveform. Therefore, three-phase inverters should be designed to be suitable for four-wire systems and maintain the symmetry of the output voltage wave [3, 4].

For this purpose, the research on the topology of three-phase inverters presents two solutions which do not use a three-phase transformer. The first involves a three-leg inverter with four wires where the neutral load point is connected to the voltage midpoint of the DC bus capacitors using a fourth wire [5, 6]. The second solution consists of a four-limb inverter where the fourth wire connects the neutral point of the loads to the midpoint of the fourth branch [7, 8]. Even if the first solution constitutes the simplest way of connecting the neutral point, practical problems limit its use: the zero sequence components of the neutral current increase the current of the capacitors of the intermediate circuit, often electrolytic, and have a detrimental effect on the ripples voltage and their longevity. The three phase inverters have several disadvantages: insufficient use of the intermediate circuit voltage, large ripples in the intermediate circuit voltage, and intense voltage oscillations on the intermediate circuit capacitors. On the other hand regardless of the higher number of power switches, four-leg inverters are best suited for four-wire networks and industrial applications where the load is unbalanced or nonlinear [9, 10].

Additionally, they have none of the problems of standard neutral point inverters. On the other hand, adding a fourth branch to the inverter complicates the control strategy. Thus, techniques of more elaborate modulation schemes are necessary for this type of inverter [11, 12].

The first use of this topology is developed for a power generation application in an aircraft system to provide a neutral connection and manage neutral current [13, 14]. This is why it is commonly used in distribution networks, due to its good ability to operate in grid-connected mode and islanded mode, a line to provide a current path to unbalanced loads in a three-phase system at four sons. It is therefore important to use an appropriate inverter topology to balance the output voltages of critical loads.

This topology plays an important role in the smooth operation of three-phase distribution networks due to its superior performance characteristics in handling unbalanced load conditions. Providing the fourth stage of the four-leg inverter can result in independent control of the phase voltage [15, 16]. Recently, various control methods have been applied to balance the output voltage and current of a four leg three-phase inverter. The use of three-dimensional space vector modulation (3D-SVM) has become a popular control technique because it provides superior harmonic performance and output waveform quality.

This paper presents a comprehensive analysis of four-leg inverters controlled by 3D-SVM, including the theory of operation, mathematical model, simulation results, and potential applications. The results demonstrate that the 3D-SVM strategy provides a unity power factor, sinusoidal waveforms of output voltages and currents, and lower total harmonic distortion, making it an ideal solution for designing power systems, specifically for DC/AC conversion in various frequency inverter applications. The simulation results can be used to validate the proposed system and make necessary adjustments to optimize its performance.

This manuscript is organized as follow: In Section 1, we made a brief introduction on the necessity of the four leg inverter applications. Section 2 presents the methodology, the modelling and strategy control based on 3D-SVM technique. In section 3 simulation results are presented and interpreted, followed by the conclusion.

2 METHODOLOGY

This article provides a comprehensive study of the four-leg inverter, covering its topological structure, its LC passive filter, its mathematical model and its control strategy. A simulation model has been developed. The 3D-SVM control strategy was proposed to generate the control signals of the switches. The three-phase four-leg inverter topology can realize higher AC voltage utilization and lower harmonic distortion under unbalanced and nonlinear load conditions. Although the reference space vector can be synthesized either in $\alpha\beta\gamma$ coordinates or in (abc) coordinates [17, 18], the former is more favourable due to the ease of analysis and control of the neutral component. In this work the three-dimensional vector space modulation method in $\alpha\beta\gamma$ coordinates is detailed. The paper analyzes the operating principles of a four-leg inverter to produce output AC voltages and currents at 25 and 50 Hz output frequency under varying load conditions.

The four- leg inverter can be widely used in industry to control the speed and torque of electric motors. These devices can be used in a variety of applications, including pumps, fans, conveyors and even machine tools. They are popular because they provide precise control of motor speed, which can result in increased efficiency, reduced energy consumption and improved process control.

The four-leg inverter topology comprises eight bidirectional power switches, each consisting of transistors and fast diodes connected anti-parallel. This allows for power distribution through three phases, enabling the supply of balanced and/or unbalanced linear or nonlinear loads [19, 20]. The working principles of the four-leg inverter using three-dimensional vector space modulation were validated in compliance with IEEE 519-standars to control harmonic distortion in electrical systems [21, 22]. Fig. 1 shows the circuit configuration of the four-leg inverter.

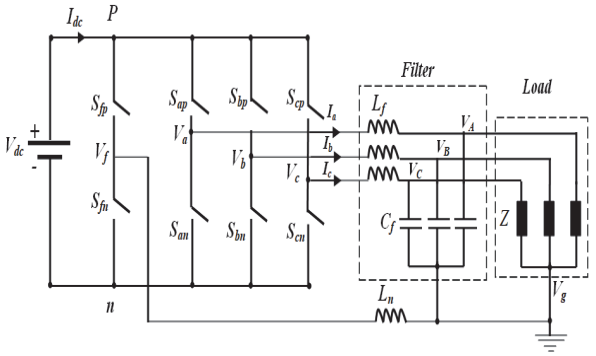

Figure 1 Circuit of a Four-leg inverter

2.1 Modelling of a 4-leg Inverter

The three phase output voltage is dependent on the function S_{if} can be defined as [23, 24].

$$S_{if} = \begin{cases} 1 & \text{if} \quad S_{ip} \text{ is closed} \\ 0 & \text{if} \quad S_{ip} \text{ is open} \end{cases} \tag{1}$$

with: $i = a, b, c$

A simple relationship between the output voltage and DC input voltage (V_{dc}) may be written as:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} S_{af} \\ S_{bf} \\ S_{cf} \end{bmatrix} \tag{2}$$

And the Eq. (3) represents the DC current:

$$i_{dc} = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix} \cdot \begin{bmatrix} S_{af} \\ S_{bf} \\ S_{cf} \end{bmatrix} \tag{3}$$

Three-phase AC voltage (V_{af}, V_{bf}, and V_{cf}) is a surge voltage with constant switching time T_s. To get the average voltage for each switching period, we write:

$$\bar{\hat{X}} = \frac{1}{T_s} \int_0^{T_s} X(t) \mathrm{d}t \tag{4}$$

Using the average cycle-by-cycle calculation method, the average AC and DC voltages are:

$$\begin{bmatrix} \bar{V}_a \\ \bar{V}_b \\ \bar{V}_c \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} D_{af} \\ D_{bf} \\ D_{cf} \end{bmatrix} \tag{5}$$

and,

$$i_{dc} = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix} \cdot \begin{bmatrix} D_{af} \\ D_{bf} \\ D_{cf} \end{bmatrix} \tag{6}$$

where D_{af}, D_{bf}, D_{cf} are line-to-neutral duty ratio.

2.2 Three-Dimensional Space Vector Modulation Method (3D-SVM)

2.2.1 Switching Vectors

Richard et al. proposed a new approach for 3D-SVM to control output voltage of four- leg inverter supplying three phase unbalance or non-linear loads [20]. According to this approach after adding the fourth leg to the three-leg inverter, the switching states increase from eight states in three-leg inverter to sixteen switching states in four-leg inverter [28, 29].

Table 1 Switching state and the corresponding voltage vectors in (*abc*) coordinates

	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8
	0000	0001	1001	1101	0101	0111	0011	1011
V_{fa}	0	$-V_{dc}$	0	0	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0
V_{fb}	0	$-V_{dc}$	$-V_{dc}$	0	0	0	$-V_{dc}$	$-V_{dc}$
V_{fc}	0	$-V_{dc}$	V_{dc}	$-V_{dc}$	$-V_{dc}$	0	0	0
	V_9	V_{10}	V_{11}	V_{12}	V_{13}	V_{14}	V_{15}	V_{16}
	1110	1111	1000	1100	0100	0110	0010	1010
V_{fa}	V_{dc}	0	V_{dc}	V_{dc}	0	0	0	V_{dc}
V_{fb}	V_{dc}	0	0	V_{dc}	V_{dc}	V_{dc}	0	0
V_{fc}	V_{dc}	0	0	0	0	V_{dc}	V_{dc}	V_{dc}

They are represented in order according to the combinations of the switches [S_a, S_b, S_c, S_f], the terminal voltages [$V_{fa}V_{fb}V_{fc}$] listed in Tab. 1.

2.2.2 Prisms Detection

There is a total of fourteen vectors in three-dimensional space, with the combinations (1111) and (0000) always resulting in zero vectors [30, 31]. Fig.2 provides a graphical representation of these vectors. The voltage space vectors depicted in Fig. 3 are divided into six prisms, and at any given moment, the vector voltage is situated within one of these prisms [32, 33]. Fig. 4 illustrates the cases in which the reference voltage vector falls within each prism [20]. The prism can be divided into four tetrahedrons, resulting in a total of Twenty-four tetrahedrons.

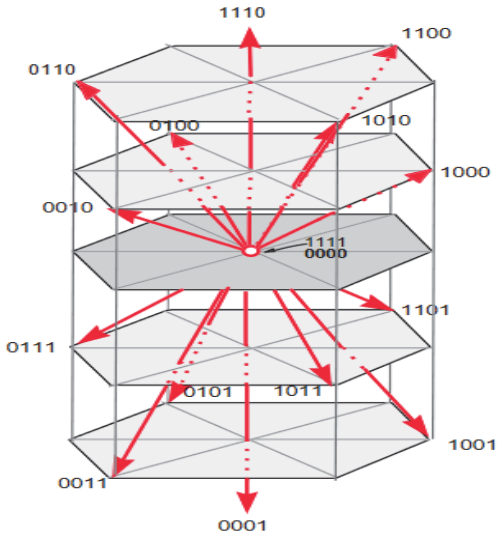

Figure 2 Switching vectors in (α, β, λ) coordinates

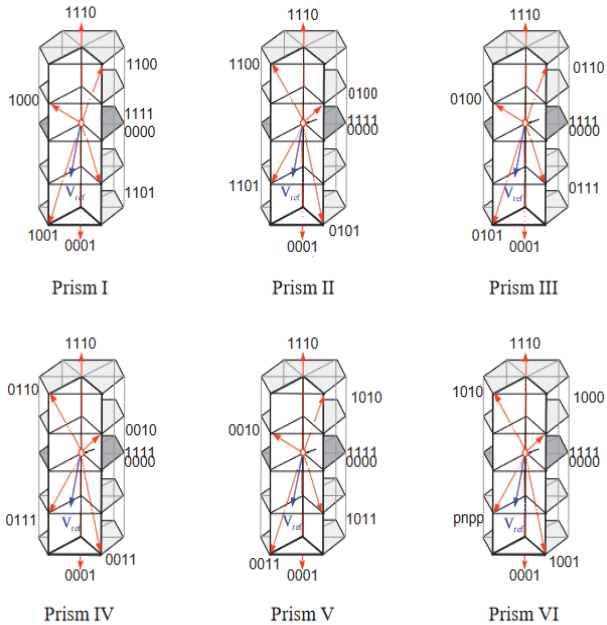

Figure 3 Representation of the reference vector in the different prisms

2.2.3 Reference Vector Projection

The Eq. (7) represents the reference vector is in prism I and tetrahedron 1.

$$v_{ref} = \begin{bmatrix} V_{a-ref} \\ V_{b-ref} \\ V_{c-ref} \end{bmatrix} \tag{7}$$

where, the available switching vectors are: $V_1 = [1000]$, $V_2 = [1001]$, $V_3 = [1101]$, $V_0 = [1111, 0000]$.

The corresponding duty cycle for each switching vector is given in [20].

$$v_{ref} = D_1 \cdot V_1 + D_2 \cdot V_2 + D_3 \cdot V_3 \tag{8}$$

So,

$$\begin{bmatrix} D_1 \\ D_2 \\ D_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ 0 & \sqrt{3} & 0 \end{bmatrix} \begin{bmatrix} v_{ref-a} \\ v_{ref-b} \\ v_{ref-c} \end{bmatrix} \tag{9}$$

where: $D_0 = 1 - (D_1 - D_2 - D_3)$ (10)

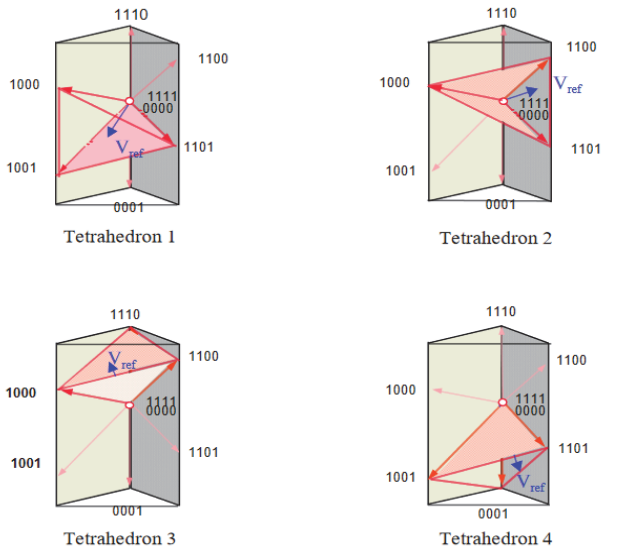

Figure 4 Representation of tetrahedrons in prism I

2.2.4 Design of the Input Filter

In order to stop the propagation of harmonic currents created by four leg inverter connected to balanced load, an LC filter is used. It is a series resonant circuit tuned to the frequency of the harmonics and mounted as a shunt across the terminals of the AC terminals voltage, [34]. This filtering system behaves like a reactive power compensator. It is seen that if the filter parameters are correctly calculated, the output voltages will be similar to its references.

3 SIMULATION RESULTS

The schematic diagram of a four-leg inverter is presented in Fig. 5. This topology is formed by eight power switching devices coupled to free-wheeling diodes and a DC capacitor voltage (V_{dc}), LC passive filter and three phase balanced load, the neutral conductor connected to the

star point of the load to the mid-point of the fourth arm of the inverter. The four-leg inverter is connected in parallel with respectively unbalanced load and nonlinear load.

Tab. 4 shows the parameters chosen in the simulation test. The waveforms of the four-leg inverter are validated by comparing them with the THD imposed by IEEE 519 standard norms [36]. Different simulation tests under various load scenarios such as balanced load, unbalanced load and nonlinear load are carried out to validate the performances and effectiveness of the proposed control strategy.

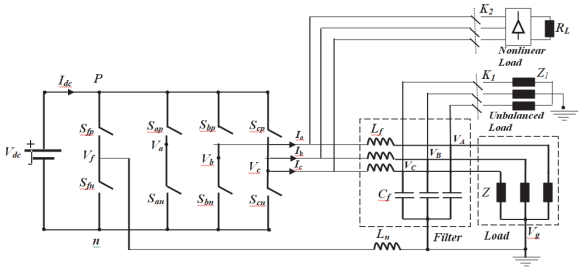

Figure 5 Block diagram of four-leg inverter

Table 4 Simulation parameters

DC voltage	200 V
LC Filter	160 µF, 1.2 mH
Neutral inductor	0.6 mH
Switching frequency	5 KHz
load resistance	10 Ω
Unbalanced load	100 Ω, 10 Ω, 5 Ω
R_L Load	10 Ω
Imposed output frequency,	25 Hz and 50 Hz

a) Balanced load

Figs. 6 and 7 represent the line to line output voltages at 50 and 25 Hz respectively. It is observed that there is a high quality voltage; the control system presents an excellent dynamic response.

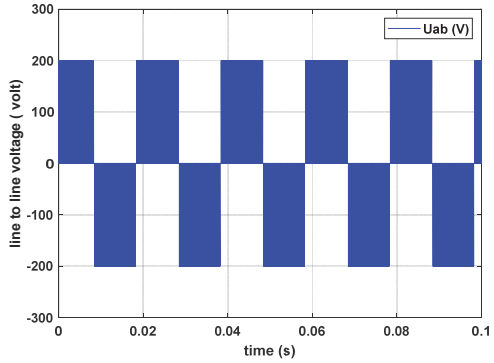

Figure 6 Line to line output voltage at 50 Hz

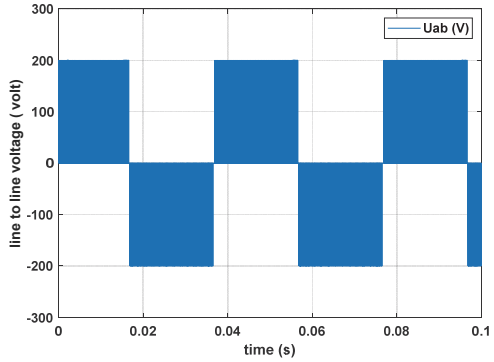

Figure 7 Line to line output voltage at 25 Hz

Figs. 8 and 9 show the simple voltage with respect to the load neutral point at 50 and 25 Hz. These figures show the capability of this model to produce pure sinusoidal waveform when frequency of 50 Hz is used and idem case when frequency of 25 Hz is used.

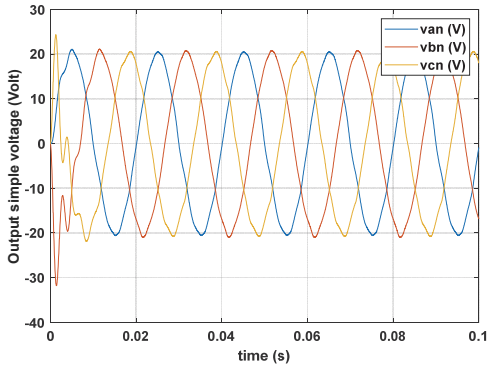

Figure 8 Simple output voltages at 50 Hz

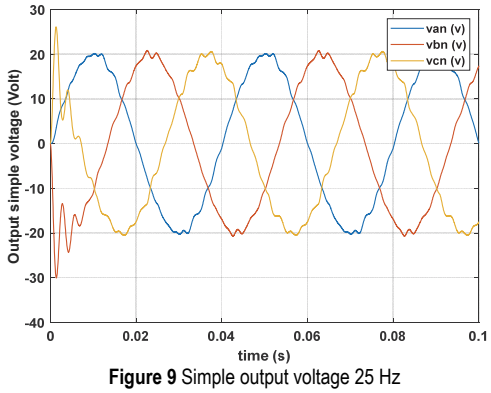

Figure 9 Simple output voltage 25 Hz

From Figs. 10 and 11, it can be clearly seen that the output currents at 50 Hz and 25 Hz are pure sinusoidal waveforms.

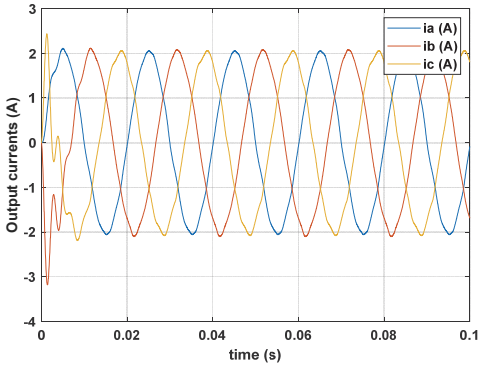

Figure 10 Output current at 50 Hz

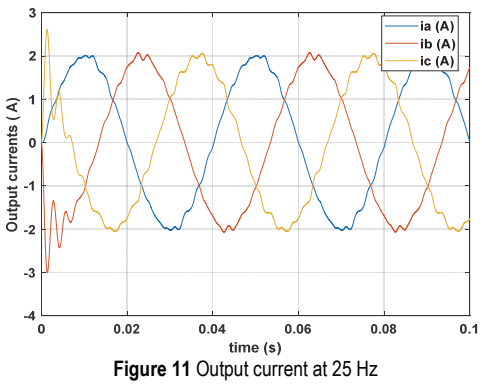

Figure 11 Output current at 25 Hz

In Figs. 12 and 13, the THD of output current is 2.06% at 50 Hz, while frequency of 25 Hz produces THD of 2.55%. In this case THD is observed at both inverter output voltage and current as per IEEE standard norms the maximum THD allowed is 5% [35].

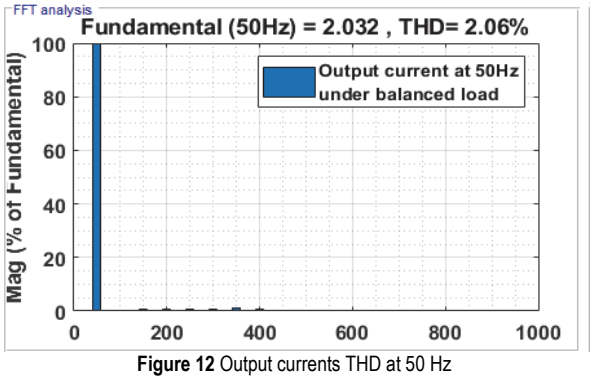

Figure 12 Output currents THD at 50 Hz

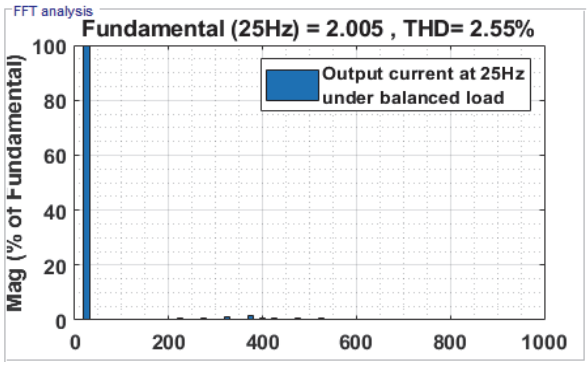

Figure 13 Output currents THD at 25 Hz

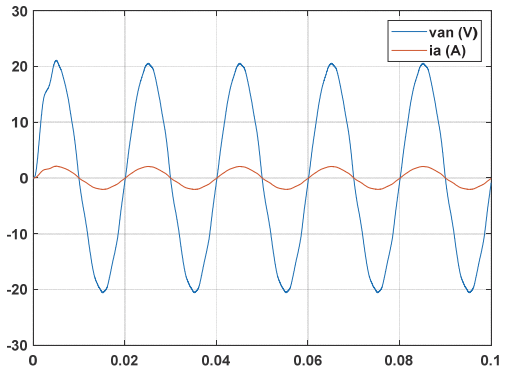

Figure 14 Output voltage and current: at 50 Hz

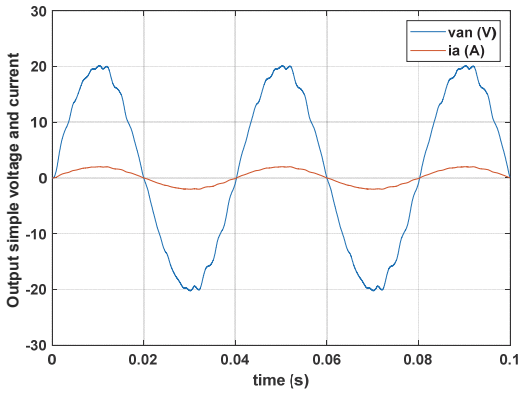

Figure 15 Output voltage and current: at 25 Hz

In Figs. 14 and 15 we can see that the single voltage and output current are in phase at 50 Hz and 25 Hz respectively. These results show that an inverter can inject current into the load with unity power factor with zero power reactive consumption. The neutral voltage is shown in Fig. 16.

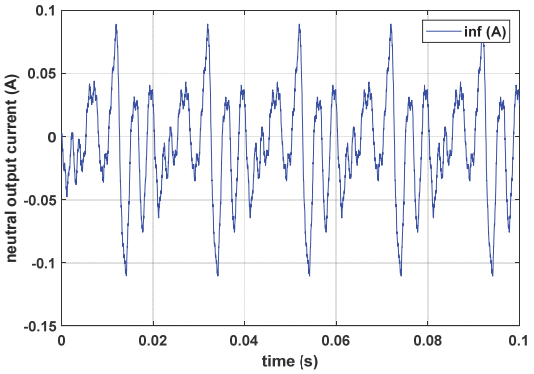

Figure 16 Neutral current waveforms

b) Unbalanced load

When the four-leg inverter fed an unbalanced load, the output currents with a desired output frequency are illustrated in Figs. 17 and 18. These figures show the capability of this model to produce sinsoidal wavorfmes. The spectrum of the corresponding currents is shown in

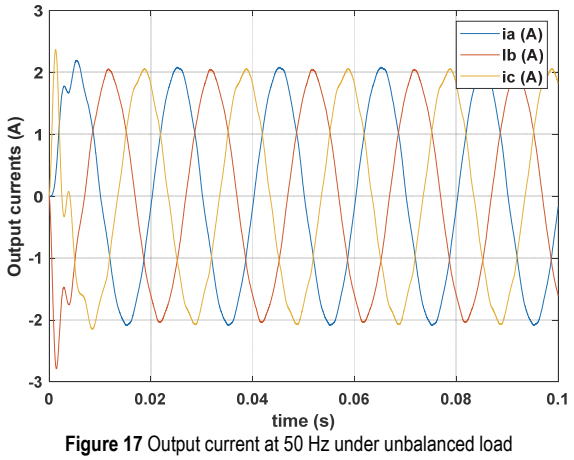

Figure 17 Output current at 50 Hz under unbalanced load

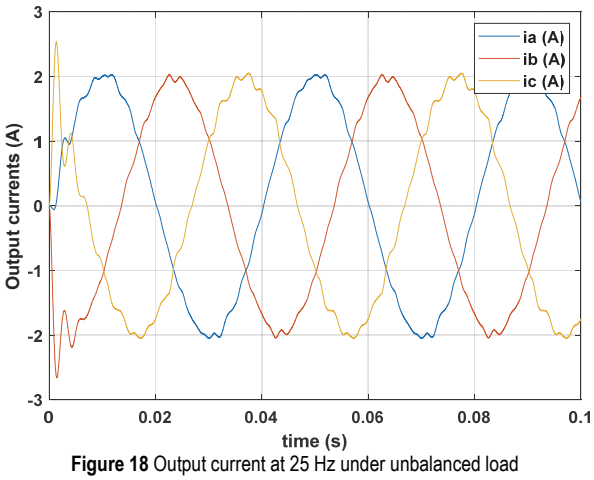

Figure 18 Output current at 25 Hz under unbalanced load

Fig. 19 and Fig. 20. It can be observed that the THD is 1.65% at 50 Hz and 2.10% at 25 Hz. These figures indicate that the THD value of the load currents is very small in this loading condition.

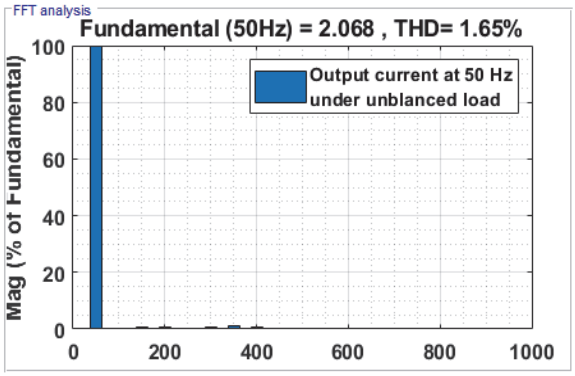

Figure 19 Output currents THD at 50 Hz under unbalanced load

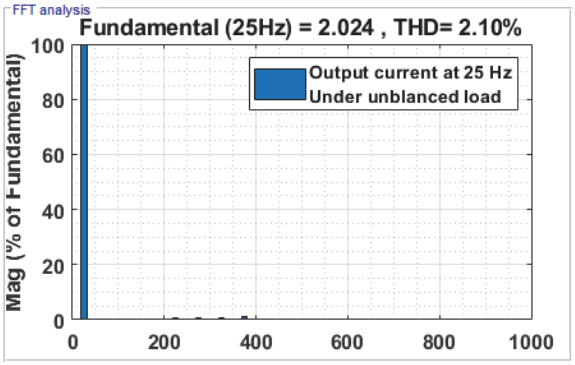

Figure 20 Output currents THD at 25 Hz under unbalanced load

c) Nonlinear Load

In this case, a nonlinear load, consisting of three Rectifiers Bridge that supply $R_l = 10\ \Omega$ resistors, has been connected to the Linear Load. As observed in Figs. 21 and 22, the output currents are sinusoidal waveforms. These results are due to proper configuration of the inverter and appropriate strategy control and effectiveness filter.

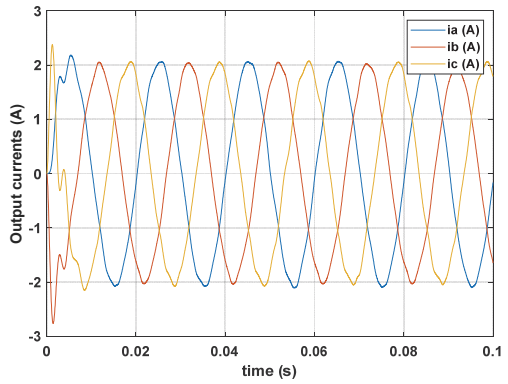

Figure 21 Output currents THD at 50 Hz under nonlinear load

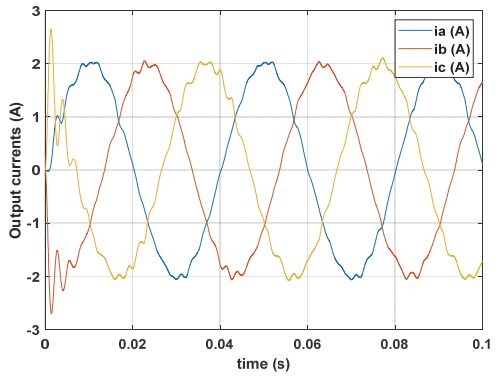

Figure 22 Output currents THD at 25 Hz under non linear load

Figs. 23 and 24 show spectrums harmonic analysis of the output currents. It is clear that distortion harmonics are effectively attenuated at a satisfying level seen that the THD decreased to 1.94% at 50 Hz and to 2.46 at 25 Hz.

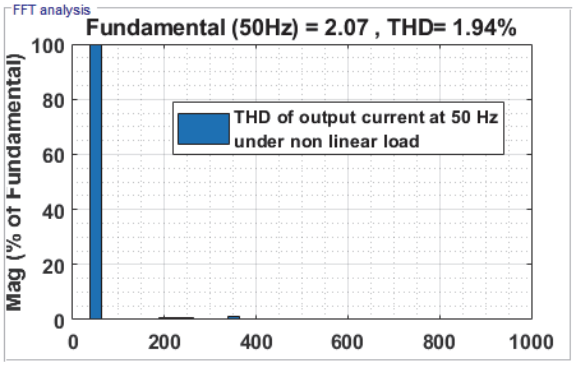

Figure 23 Output currents THD at 50 Hz under nonlinear load

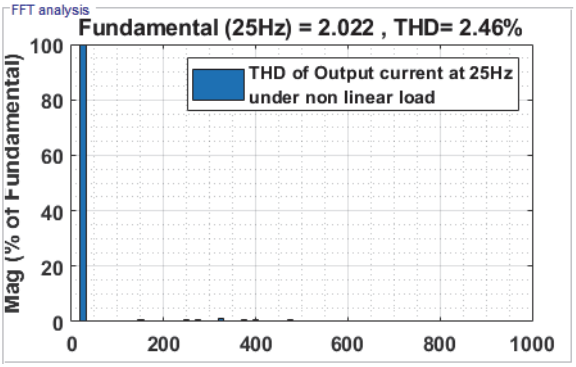

Figure 24 Output currents THD at 25 Hz under non linear load

4 CONCLUSION

In this study, a 3D-SVM-based four-leg inverter was proposed, and its theory of operation and analysis were presented. The mathematical model of the four-leg inverter was explained in detail. Simulation results demonstrated that the proposed modulation strategy can achieve a unity power factor, sinusoidal waveforms of output voltages and currents with lower Total harmonic distortion. Therefore, it can be confidently used in designing DC/AC conversion for operating variable frequency. The THD values of the output currents are 2.06% at 50 Hz and 2.55% at 25 Hz in the case of balanced load. It is similar 1.65% at 50 Hz and 2.10% at 25 in the case of unbalanced load; same thing in the presence of nonlinear load the THD is 1.94% at 50 Hz and 2.64% at 25 Hz, complying with IEEE 519-standards. These values are under the maximum limits allowed by the IEEE 519 standards with maximum THD allowed of 5%. According to the standards norms our work is reasonable. Future research includes developing a simplified 3D-SVM methodology, integrating intelligent controller for system-level stability assessment, and implementing control design in the Z-source domain.

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