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Thermal annealing and temperature dependences of memory effect in organic memory transistor

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We investigate the annealing and thermal effects of organic non-volatile memory with floating silver nanoparticles by real-time transfer curve measurements. During annealing, the memory window shows shrinkage of 23% due to structural variation of the nanoparticles. However, by increasing the device operating temperature from 20 to 90 °C after annealing, the memory window demonstrates an enlargement up to 100%. The differences in the thermal responses are explained and confirmed by the co-existence of electron and hole traps. Our findings provide a better understanding of organic memory performances under various operating temperatures and validate their applications for temperature sensing or thermal memories. © *2011 American Institute of Physics*. [doi:10.1063/1.3617477]

Organic electronic devices have drawn much attention due to their low fabrication temperature, compatible with flexible substrates, large fabrication area, and low production costs.[1,2] Among different organic devices, transistors play a very important role as they are the key element of various types of integrated circuits including memories. Organic non-volatile memories (ONVM) based on organic thin film transistors (OTFT) have been demonstrated in different structures such as floating gate, charge trapping dielectric, and ferroelectric gate dielectric.[3–5] Recently, we demonstrated an ONVM structure by applying floating silver nano particles (NPs) into the semiconductor layers of OTFT.[6] Such structure can maintain the relatively high mobility of the device and simplify the fabrication steps as no floating gate layer is needed.

The environmental and thermal instability of organic materials is one of the reasons why the commercialization of organic electronic devices has not been fully achieved. Although the ambient environment induced degradation of pentacene-based OTFT at room temperature has been reported,[7] more investigation is still needed for the thermal instability of the thin film transistors structure devices, especially the ONVM. For the OTFT, multiple trapping and releasing (MTR) model is commonly adapted to explain the Arrhenius relationship,[8–10] but this model fails at elevated temperatures where scattering of charges become important.[9,10] In contrast to OTFT, the thermal effects on the performance of the ONVM have not been investigated in detail, and the relationship between memory window and the operating temperature remains unclear. Since the metal NPs embedded into the organic materials are thermally unstable and aggregation may occur in room ambient under high temperature,[11] the memory effect (hysteresis loop) in the floating nanopartice ONVM would be strongly dependent on the temperature and annealing process. A detailed study on the thermal response of ONVM would be very useful for understanding the charge trapping and transporting mechanisms under various temperatures.

In the current work, we separately study the annealing and temperature effects in the floating Ag NPs ONVM devices by monitoring the real-time transfer output curves. We found the memory window (ΔV_{th}) decreases by 14.8 V ($\sim$23% of the original value) during the annealing process; after annealing, the device became stabilized and sensitive only to variations of the operating temperature. The memory window shows a 100% increase from 24.1 to 48.3 V when the temperature rises from 20 to 90 °C. Such trend is similar to the TANOS memory[12] but different from the silicon ferroelectric memory devices where memory window decreases with temperature.[13] The nature of the trap states in the ONVM device is studied by transmission electronic microscopy (TEM) analysis and time-domain drain-source current (I_{DS}) measurements. The potential applications of the observed bipolar trap states in the ONVM devices are also discussed.

Similar to the previous devices,[6] the thicknesses of the active region layers in order are pentacene (15 nm), Ag NPs (3 nm), and pentacene (25 nm). The channel length and width of the device are 50 and 1000 μm, respectively. The detailed fabrication process has been reported elsewhere[6] and will not be repeated here. The current-voltage characteristics of the transistor memory devices were measured using an Agilent 4156C Semiconductor Parameter Analyzer. Peltier heater connected with a Newport 350A temperature controller was applied to control the temperature of the device, and the surface temperature of the sample was monitored by a microthermocouple (30 μm). All measurements were performed in dark and room ambient conditions.

To separate the annealing and temperature effects, the heating processes were divided into three stages: (1) initial heating, (2) constant temperature annealing, and (3) periodic cycling as shown in Fig. 1(b) and are represented by the numbers (1)–(13). Throughout the process, the temperature

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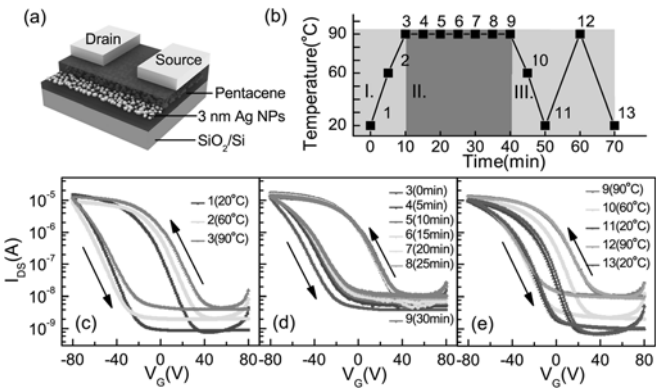

FIG. 1. (Color online) (a) Schematic diagram of ONVM device. (b) Temperature profile applied on the device as a function of time. The transfer I-V characteristics for ONVM device under different thermal process are shown in (c) stage 1, (d) stage 2 and (e) stage 3, respectively.

controller maintained the heating and cooling rate at 10 °C/min. Fig. 1 show the transfer curves of the ONVM at different regions, with the drain-source voltage (V_{DS}) maintained at −80 V. In the transfer curves, V_{th1} is defined as the threshold voltage when gate voltage (V_G) is sweeping from +80 to −80 V (off-to-on), and V_{th2} is defined as the threshold voltage when V_G is sweeping from −80 to +80 V (on-to-off). The memory window (ΔV_{th}) is given by the difference between the two threshold voltages due to different sweeping directions, i.e., $\Delta V_{th} = V_{th1} - V_{th2}$. As shown in Fig. 1(c), during the initial temperature rising stage, V_{th1} is right shifted when temperature increases from 20 to 90 °C while the V_{th2} remains relatively stable. As a result, the memory window of the device increases from 50 V at 20 °C to 64.1 V at 90 °C during the initial 10 min heating process in stage 1. In stage 2 (Fig. 1(d)), when the device is annealed at a constant temperature of 90 °C, V_{th2} drops continuously to a steady value but V_{th1} remains constant. By comparing the results in Figs. 1(c) and 1(d), one can notice that V_{th1} appears to be temperature dependent while, on the other hand, the temperature dependence of V_{th2} is less explicit but shows a stronger time dependent behavior. After the annealing process (stage 3), the device became stabilized, and the transfer curves of the ONVM devices only show temperature dependence as shown in Fig. 1(e). The values of V_{th1} and V_{th2} for point 1-13 are listed in Table I (see Supplementary material). It is worthy to mention that V_{th1} is close to zero and V_{th2} is −20.6 V after annealing; it suggests hole traps are dominant at room temperature and agrees with our previous observation.[6] A detailed discussion about the variation of threshold voltages will be presented in the following section.

Different from the temperature dependence V_{th1}, the right shift of V_{th2} during annealing is irreversible, and it is attributed to the permanent structural change in the device during the annealing. Silver NPs between two pentacene layers before (point 1) and after (point 13) annealing are observed in top view TEM images as shown in Figs. 2(a) and 2(b), respectively. It can be noticed that the silver nanoparticles aggregate and the size of the NPs increases after annealing at 90 °C. By performing image processing in MATLAB, the silver nanoparticles density in Figs. 2(a) and 2(b) are evaluated to be 6.7×10^{11} cm^{-2} and 4.2×10^{11} cm^{-2}, respectively. The trap density (Δn) is proportional to the shift of the threshold voltage ΔV_{th} by[14] $\Delta n = \frac{\Delta V_{th} C_i}{e}$, where C_i is the unit area capacitance of dielectric layer. By comparing the reduction of the trap density obtained from the equation and areal density of the Ag NPs, the average trapped charges per silver nanoparticle decrease from 5.4 to 3.8 after annealing. A possible explanation for the reduction of the trapping efficiency of the nanoparticles is the growing and crystallization of the Ag NPs which would reduce the hole trap states within the nanoparicles or at the interface between the NP and pentacene. More detailed investigations at the interface between the nanoparticles and the pentance are needed to verify the exact location of traps and the formation mechanism.

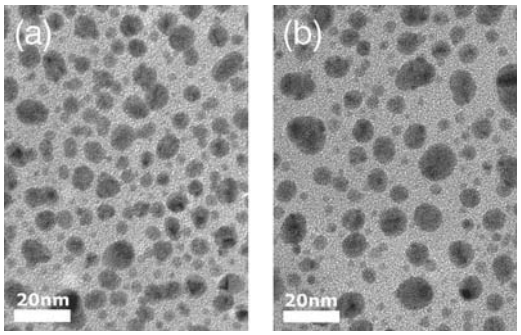

FIG. 2. TEM images of silver NPs in pentacene layer before (a) and after (b) annealing. The dark spots represent the silver nanoparticles.

For the V_{th1}, the strong temperature dependence and reversible shift of V_{th1} suggest a different voltage shifting mechanism from V_{th2}. The hole traps dominate the hysteresis effect of ONVM device at room temperature, and the increase in temperature only causes variation of V_{th1}, but not V_{th2}. We speculate the right shift of V_{th1} with temperature is due to the generation and filling of negative charges (electron) traps in the active region. To verify that, we applied time-domain drain-source current measurements[7] under different temperatures by keeping V_G at +40 V for the first 100 s and then switched to +60 V for another 100 s. If the

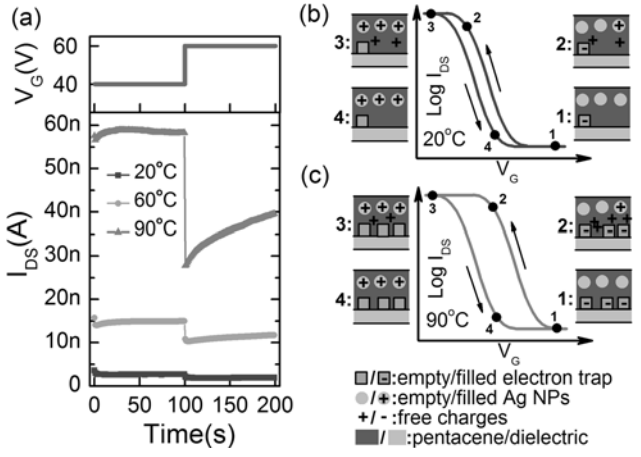

FIG. 3. (Color online) (a) Time-domain measurement data for ONVM device at 20, 60, and 90°C. Upper panel shows the applied V_G waveform during the experiment. (b) Schematic diagram of electron traps formation and transfer curve at 20°C, suggesting negligible electron traps at this temperature; (c) schematic diagram of electron traps formation and transfer curve at 90°C, suggesting more electron traps at this temperature and right shift of V_{th1}.

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electron traps exist, certain amount of electron traps are filled at the first 100 s; after V_G is switched to +60 V, more electrons will be further trapped and more holes are required to balance the trapped electrons; hence, the drain-source current increases with time and right shift of V_{th1}. On the other hand, if there is no electron traps, a more positive V_G will not fill the traps, so the drain-source current remains constant after the switching of V_G. From the results shown in Fig. 3(a), the I_{DS} remains constant after $t = 100$ s at 20 °C, suggesting hole traps is dominating in the device and the electron trap density is negligible at room temperature. However, when the temperature is at 90 °C, the I_{DS} increases significantly after $t = 100$ s and the rising rate also goes up with temperature due to the presence of electron traps. By comparing the ONVM results with the pentacene OTFT without silver NPs layer,[15] the increase of V_{th1} in OTFT is similar to the ONVM while the V_{th2} remains constant. It suggests the shift of V_{th1} in ONVM is independent of the Ag NPs. These thermal induced electron trap states are reversible and highly sensitive to temperature. It is different from the traps induced by illumination and oxygen environment observed by Ogawa *et al.*, where the charges can maintain for tens of hours.[16] Furthermore, the thermal induced traps are also different from the bias-stress induced traps; in the bias-stress test of a p-type OTFT, a continuous negative gate bias would induce immobile trapped holes at the dielectric and causes left (negative) shift of V_{th}, but not the right shift as observed at the elevated temperature.[17] We believe the extra electron traps in the ONVM device are due to the SiOH silanol groups[18] and oxygen anion[19] formed when the device is under room ambient condition, and the formation of these electron traps is temperature sensitive. The schematic diagram of hysteresis loop of the ONVM devices after annealing at 20 and 90 °C are shown in Figs. 3, respectively. At 20 °C, Fig. 3(b) shows that only little electron traps are located in the channel. Sweeping the gate bias from +80 V will fill these traps and induce holes to balance the trapped electrons. However, due to the low density of the electron traps, the induced holes affect shows very little enhance to the I_{DS}, and the V_{th1} is close to zero. When V_G is at −80 V, all the hole traps will be filled and cause screening effect when V_G is sweeping from −80 to +80 V; hence, the V_{th2} is a negative value and shows the hysteresis effect. At 90 °C, more electron traps are induced by high temperature and filled at a +80 V V_G bias. The I_{DS} will increase and cause the right shift of V_{th1}. All the electron traps are empty at −80 V starting V_G bias, so the V_{th2} has no significant changes.

In summary, we studied the annealing and thermal effects in ONVM devices and provide explanation to the memory responses at different temperatures. Depending on the operating temperature of the ONVM device, we find that other than the hole traps, electron traps would also contribute to the hysteresis loop and enlarge the memory window of the device at the elevated temperatures. In the floating NP ONVM devices, one can make use of the shifting of the threshold voltages and enlargement of the memory window for the storage levels of Boolean states "0" and "1". By placing the array of the ONVM devices on the object, the temperature profile of the object can be measured and stored by the ONVM array. Our finding can not only provide better understanding on the relationship between hysteresis effect and operating temperature in floating Ag NP ONVM devices but also demonstrate their potentials applications as temperature sensors and thermal memories arrays.

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