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Unification of bulk and interface electroresistive switching in oxide systems

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We demonstrate that the physical mechanism behind electroresistive switching in oxide Schottky systems is electroformation, as in insulating oxides. Negative resistance shown by the hysteretic current-voltage curves proves that impact ionization is at the origin of the switching. Analyses of the capacitance-voltage and conductance-voltage curves through a simple model show that an atomic rearrangement is involved in the process. Switching in these systems is a bulk effect, not strictly confined at the interface but at the charge space region.

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A reversible electroresistive (ER) switching effect in oxide Schottky junctions has been widely reported in the last years.[1–3] In the effort to claim potentiality for nonvolatile memory applications, it has been sustained that, unlike ER switching in insulating oxides,[4] the effect is electronic and hence very fast. As recently pointed out by Waser and Aono,[5] unambiguously experimental evidence was not provided in this direction. Moreover, the papers often lack in details on fabrication processes and measurement setups. As a consequence, it is difficult to draw boundaries for possible applications.

The proposed scenario is the charging effect at the Schottky interface[3] through Fowler-Nordheim tunneling to defect states: acceptor trapping states are present in the Schottky barrier because of impurities and structural defects. In the high resistance state these traps are occupied with electrons. When a sufficiently high forward bias voltage is applied, electrons are detrapped, leaving resonant tunneling paths in the Schottky barrier; as a consequence, the resistance drops. A negative reverse bias voltage is able to produce retrapping, hence to switch back the device to the previous state. In other words, resonantly tunneling paths into the Schottky barrier would play the same role as filamentary percolative paths created by electroformation in insulating oxides.[6]

In this Brief Report we give experimental evidences sustaining electroformation at the origin of the effect, as in bulk undoped oxides.[5,6] The trapping states are not due to impurities or structural defects but are created by avalanche injection breakdown. Ionic motion is involved, although the atomic rearrangement remains confined below the interface over a length scale of the space charge.

The system $La_{0.7}Sr_{0.3}MnO_3/SrTi_{0.98}Nb_{0.02}O_3$ (LSMO/NSTO) was chosen for the present investigation. A full characterization of the interface transport properties of this system has been already reported.[7] To avoid any possible additional capacitance contribution from patterned wiring when measuring at high frequency, for the present study, we chose a capacitorlike geometry. A 100-nm-thick LSMO film was deposited on a 0.5-mm-thick NSTO substrate through a 500×500 μm^2 shadow mask and, subsequently, a platinum film was evaporated on the LSMO for the electrical contact. In the following, the positive voltage bias is defined by the current flowing from LSMO to NSTO.

The junctions could be switched between two stable states (Fig. 1). Switching toward the low resistance state (LRS) can be achieved by either scanning the negative voltage (reverse bias) or by applying a short negative voltage pulse. The application of a subsequent train of pulses of the same sign does not change the state of the device. Switching back toward the high resistance state (HRS) can be achieved by either scanning the positive voltage (forward bias) or by applying a positive voltage pulse. Like for the LRS, the HRS is

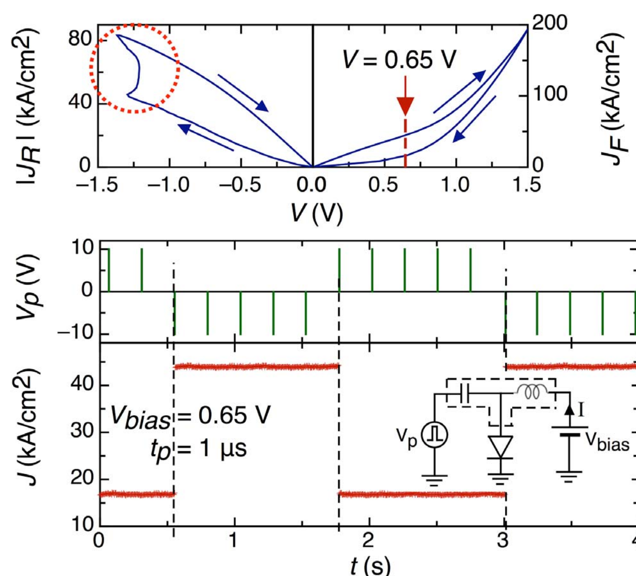

FIG. 1. (Color online) Top: Hysteretic current density-voltage (J-V) characteristic. The forward bias current (J_F) and the absolute value of the reverse bias current (J_R) are reported on two different scales. The J-V shows negative resistance when reverse switching occurs. Bottom: ER switching induced by voltage pulses with a duration of $t_p=1$ μs. The ER ratio measured in the pulsed working mode is the same as that evaluated from the J-V, at the same bias. Inset shows the measurement setup.

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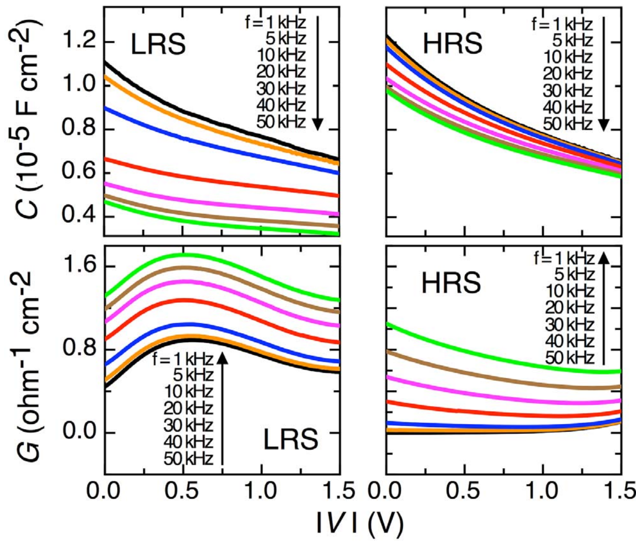

FIG. 2. (Color online) C-V and G-V curves in the two resistance states recorded in reverse bias at different values of f: 1, 5, 10, 20, 30, 40, and 50 kHz from top to bottom in the C-V's and bottom to top in the G-V's.

stable over the application of further positive pulses. In the pulsed working mode, the ER switching was detected by reading the current at a fixed voltage. A standard bias tee was used to supply simultaneously the pulses and the bias voltage to the junction. The dc current was measured as the current flowing through the dc power supplier. The ER ratio was the same as that evaluated from the hysteretic current-voltage (I-V) curve, at the same bias. The dipolar characteristic of the effect, together with the large compliance current of the voltage suppliers (~ 100 mA), rules out Joule heating as the dominant mechanism.[5]

The presence of trapping states at the interface of a Schottky junction can be detected by measuring the capacitance (C) and the conductance (G) as a function of V with frequency (f) as a parameter.[8] Figure 2 shows the C-V's and the G-V's taken at various f in reverse bias (superimposed oscillating voltage of 25 mV) and in both the resistance states. Such a combination of C-V's and G-V's is peculiar in the framework of standard semiconducting Schottky junctions. A shift of the C-V's with f is typically detected in metal-insulating oxide-semiconductor (MIS) systems and can have several origins. The most common is the presence of interface states at the I-S interface, where the periodic lattice structure is interrupted.[9] We do not have an insulating oxide in our system. Yet, the semiconductor is itself an oxide, therefore one could imagine that dangling Ti bonds at the interface act as acceptor states. As a matter of fact, when increasing f, the C-V shifts toward less negative (more positive) voltage, as expected for acceptor states at the interface.[8] In the LRS, the overlapping between Ti acceptor states results in the formation of a conducting band in the midgap. When a voltage is applied, the peak in the G-V curve corresponds to the Fermi level crossing the interface state band in the gap.

This simple scenario is ruled out by the weak shift of the peak position with f in the G-V's. In the case of interface trapped charge, the position of the peak in the G-V is expected to shift accordingly with the shift of the C-V because both are a function of the surface (interface) potential. In Fig. 2 (bottom left) the peak position is weakly sensitive to the frequency. If trapping states exist, they are not strictly confined at the interface.

Another possibility is the presence of trapping centers in the depletion layer due to impurities or crystal defects. This can also be excluded with a simple calculation. When the ac voltage swings, at high frequency, trapped charges cannot follow it; thus, when f increases, the C-V approaches the ideal curve, free of capacitance due to traps. Choosing a fixed value of $C = 6.6 \times 10^{-6}$ F/cm^2, a change of f from 1–20 kHz produces a shift of about 1.5 V in the LRS. This means that the trapping density per unit area Q_{tot} is larger than $\Delta Q = (6.6 \times 10^{-6}) \times 1.5 = 10^{-5}$ C/cm$^2 = 6.25 \times 10^{13}$ charges/cm^2. The built-in depletion width $W_{D0} = W_D(V=0)$ of a Schottky junction can be calculated from,[8]

$$W_D = \sqrt{\frac{2\epsilon_S (V_{B0} - V)}{qN_S}}, \tag{1}$$

where q is the electron charge, V_{B0} is the built-in potential, N_S is the doping concentration, and ϵ_S is the permittivity in the depletion layer. In our as-grown junctions,[7] where $N_S = 3.3 \times 10^{20}$ cm^{-3}, $V_{B0} = 0.83 \pm 0.05$ V, and $\epsilon_S = 54.4$ at room temperature, and $W_{D0} = 3.9$ nm. This implies that a concentration of defects larger than $N_d = \Delta Q / W_{D0} = 1.6 \times 10^{20}$ cm^{-3} should exist in the original crystal, which is absolutely unlikely. Notice how N_d is suspiciously very close to N_S. If there were no overlapping between defect states (fixed charges), the shift of the C-V from LRS to HRS should be rigid and no peak should be detected in the G-V in either state.

We can simply conclude that the ER effect is not due to any kind of structural defects of the original semiconducting crystal, neither at the interface nor in the depletion layer. It must be the application of a voltage above a certain threshold that creates trapping states and possibly fixed charge in the crystal.

In Fig. 1, when the reverse threshold voltage ($V_{sw,r}$) is reached, the I-V shows S-type negative differential resistance.[10] Only after that a negative resistance is recorded, the I-V becomes hysteretic. The appearance of an S-type negative differential resistance is a common observation in Schottky contacts and it is due to avalanche injection under the application of a large negative electric field.[11] In standard semiconductors, avalanche ionization begins when the electric field reaches values of the order of 10^5 V cm^{-1},[12] i.e., large voltage bias is required. In our junctions, the built-in electric field at the interface is already $E_{\mathrm{max}} = 2(V_{B0}/W_{D0}) = 4.1 \times 10^6$ V cm^{-1}. As a consequence, the avalanche ionization has a very low threshold voltage. In MIS diodes, avalanche injection causes a flat-band shift in the C-V toward a more positive voltage, the appearance of a peak in the G-V and a reversible change in the I-V.[8] The shift indicates an increase in negative trapped charge in the insulating oxide and the appearance of the peak indicates that the charge is mainly trapped close to the I-S interface, where the plasma is

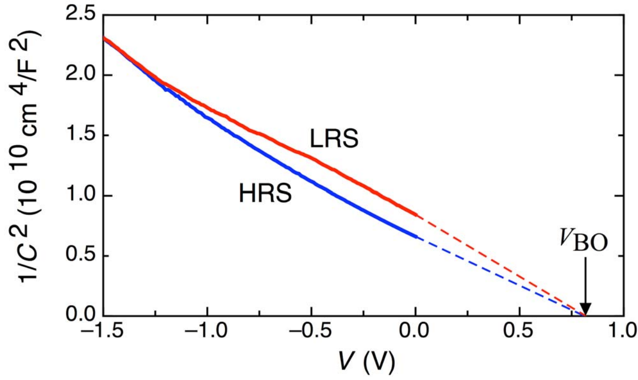

FIG. 3. (Color online) $1/C^2-V$ curves at $f=1$ kHz. The built-in potential is the same in both states.

confined. Some of the electrons have enough energy to surmount the *I-S* interfacial energy barrier and enter the insulating oxide where they remain trapped and form a midgap band. In our system, we do not have an insulating oxide where electrons can be trapped. Therefore, the negative charge or acceptor states must be created by impact ionization. This can happen in only one way: break of bondings and atomic rearrangement.

When a negative voltage is applied, the electric field close to the interface reaches a value at which carriers have enough energy to ionize some of the valence bonds of the lattice and to liberate one, or more than one, mobile electron-hole pair. The new carriers can cause further ionization that would lead to irreversible breakdown if any feedback mechanism intervened to switch off the plasma. The avalanche ionization must be stopped because of a sudden drop of the electric field. A drop of electric field can occur because of a change in the barrier height and/or in the barrier width. If we plot (Fig. 3), $1/C^2-V$ at low frequency in the LRS and HRS, the curves are linear at low reverse bias voltage and V_{B0} can be determined as the intercept with the V axis,[8]

$$\frac{1}{C^2}=2\frac{V_{B0}-V}{q\epsilon_S N_S}. \quad (2)$$

V_{B0} is the same in the two states (and equals to that measured in as-grown junctions). When increasing the reverse bias voltage, the curves deviate from the linear behavior. For the HRS this deviation is of the same type of that commonly recorded in as-grown all-oxide Schottky junctions[7,13] and can be attributed to reduced measurement accuracy due to the increase in the reverse leakage current. Instead, the behavior in the case of LRS is peculiar and indicative of an anomalous nonuniform distribution of space charge. The curve in this case goes through an *S*-type bending to join the HRS curve at a voltage that corresponds to $V_{sw,r}$. This suggests that the semiconductor is affected by the switching only over a distance from the interface $W_{sw,r}=W(V_{sw,r}=-1.3\ \text{V})=6.3$ nm, as calculated from Eq. (1).

Impact ionization produces negative charge in the depletion layer. If the built-in potential is not affected, the presence of extranegative charge is compensated by spontaneous ionization of a larger number of donors, i.e., an increase in W_D. An increase in W_D implies a reduction in C, consistently with the *C-V* shift observed when switching from HRS to LRS. When W_D increases, the electric field decreases until the plasma switches off preventing breakdown. In these systems, avalanche injection is self-feedbacked.

Notice that in the LRS $W_{D,\text{LRS}}$ cannot be calculated by evaluating the permittivity from the slope of $1/C^2-V$ at $V=0$ and applying Eq. (1) as is. The slope is larger at $V=0$ but much smaller at higher reverse bias voltage, as compared to that in the HRS. Instead, in the HRS the permittivity and the built-in depletion width were evaluated to be $\epsilon_{S,\text{HRS}}=54.1$ and $W_{D,\text{HRS}}=3.9$ nm.

$W_{D,\text{LRS}}$ must be larger than $W_{D,\text{HRS}}$ but of the same order of magnitude, if the semiconductor is affected only over a distance $W_{sw,r}=6.3$ nm. On the other hand, since all the negative charge created during ionization must be compensated by spontaneous ionization of Nb, $W_{D,\text{LRS}}$ being of the same order of $W_{D,\text{HRS}}$ is consistent with the previously calculated trap density N_d being of the same order of the doping level N_S.

It remains to understand which bondings are broken during ionization. Any uniform change of stoichiometry into the compound can only produce a rigid shift of the Fermi energy. A conducting band can appear in the midgap in only one case: if clustering of oxygen vacancies occurs.[14] The scenario must be the following: Ti-O bonds are broken during ionization. The negative electric field exerts its force on the negative O ions in such a way as to displace them far from the interface [not further than $W(V_{sw,r})$] and leave Ti acceptor states close to the interface. When the external reverse voltage is brought back to zero, the (still) negative built-in electric field acts against the oxygen gradient force, hence inhibiting the diffusion of O ions in the opposite direction. In these states, overlapping between neighbor Ti acceptor states results in a conducting band in the midgap. The *G-V* detects only the surface states,[9] with the result that the shift in the *G-V* with f is small while the large shift of the *C-V* reveals the presence of a large concentration of oxygen ions deep into the depletion layer.

In order to switch the device back, a positive voltage must be applied to compensate (at least) the negative internal electric field. As a matter of fact, a voltage larger than V_{B0} (see Fig. 1) must be applied to induce hysteresis in the *I-V*. Compensation gives to the oxygen the possibility to slowly diffuse back. This is consistent with the absence of a well-defined forward threshold voltage when slowly sweeping the *I-V*. The switching is bursted up by applying fast voltage pulses larger than V_{B0}. In our system the application of a voltage larger than V_{B0} (that would produce irreversible breakdown in a standard diode) is possible because of the presence of the conducting paths formed along the oxygen dislocations. The space charge region can be seen as a three-dimensional network of diodes and metallic resistors.[6,15]

Notice that the device never goes back to the as-grown state. If the device switched back to the as-grown state suddenly, a voltage much larger than the barrier height would be applied to an as-grown diode, which would completely destroy it. From a microscopical point of view, this means that when the device is switched back to the HRS, the previously formed oxygen vacancies are not completely refilled but con-

ducting paths are all interrupted, exactly in the same way as it occurs in filamentary type switching in undoped STO.[6] Dislocations are still present in the depletion layer although conduction is inhibited. This explains why in Fig. 2 a shift of the C-V with f is still observed in the HRS, but no peaks are detected in the corresponding G-V's.

We can now draw some boundaries on the size and the time-scale limitations of these devices for nonvolatile memory applications. The semiconductor is affected by the switching only over a distance below the interface $W_{sw,r}$. As an upper limit, we can assume that the plasma does not extend outside the interface area further than $W_{sw,r}$ along the interface plane.[8] For a doping level of the order of that used in this Brief Report, the minimum distance between two nearest-neighbor bit cells can be of the order of a few nanometers. Large values of N_S imply small values of depletion width and large built-in electric fields. As a consequence, the bit density increases and, at the same time, the switching threshold decreases. This explains the large increase in reverse threshold voltage reported in Ref. 3 when reducing N_S. On the other hand, the ER ratio decreases with N_S (Ref. 3). This can be explained with a smaller built-in electric field, and hence a smaller gradient of charge distribution in the depletion layer, i.e., a smaller number of dislocations.

As far as the switching time is concerned, determining the mobility of the O ions along the conducting paths is mandatory. We can only observe here that the avalanche multiplication is a very fast process ($\sim$10 ps in standard semiconductors[12]) and that, once the bondings have been broken, O ions are accelerated by a very large electric field to be displaced over the length scale of the depletion width, i.e., a few nanometers. It is not unreasonable to believe that these devices can reach, or even overcome, the working frequency of the current nonvolatile memories.

In conclusion, we have demonstrated that the ER switching in Schottky contacts is due to electroformation, as in bulk insulating oxides. Yet, the high electric field at the Schottky interface confines the plasma, and hence the effect, to a specific volume below the junction area, opening up the path to high density integration of resistive random access memories. Moreover, the presence of a built-in electric field reduces the switching voltage and makes the LRS stable over a very long retaining time.

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