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Ni–Al diffusion barrier layer for integrating ferroelectric capacitors on Si

B. T. Liu,[a] C. S. Cheng, F. Li, L. Ma, Q. X. Zhao, Z. Yan, and D. Q. Wu
College of Physics Science & Technology, Hebei University, Hebei 071002, China

C. R. Li
Institute of Physics, Chinese Academy of Sciences, Beijing 100080, China

Y. Wang
Department of Applied Physics, The Hong Kong Polytechnic University, Hong Kong, China

X. H. Li and X. Y. Zhang
Key Laboratory of Metastable Materials Science and Technology, Yanshan University, Hebei 066004, China

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We report on the use of amorphous Ni–Al film (*a*-Ni–Al) as conductive diffusion barrier layer to integrate $La_{0.5}Sr_{0.5}CoO_3/PbZr_{0.4}Ti_{0.6}O_3/La_{0.5}Sr_{0.5}CoO_3$ capacitors on silicon. Cross-sectional observation by transmission electron microscope reveals clean and sharp interfaces without any discernible interdiffusion/reaction in the sample. The physical properties of the capacitors are vertically characterized as the parameters of memory elements. Excellent ferroelectric properties, e.g., large remnant polarization of $\sim 22\ \mu C/cm^2$, small coercive voltage of ~ 1.15 V, being fatigue-free, good retention characteristic, imply that amorphous Ni–Al is an ideal candidate for diffusion barrier for the high-density ferroelectric random access memories integrated with silicon transistor technology. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2214142]

$Pb(Zr,Ti)O_3$ (PZT) thin films, which possess favorable characteristics such as low operation voltage, large remnant polarization, and piezoelectric constant, have been extensively investigated due to their potential applications for ferroelectric nonvolatile memory,[1–4] field effect devices,[5,6] microelectromechanical systems (MEMS),[7–9] and pyroelectric sensors.[10] Currently, great efforts have been intensively made to integrate PZT based ferroelectric capacitors with modern silicon transistor technology to yield one-transistor–one-capacitor (1T-1C) based memory architectures[2] in order to realize high-density ferroelectric random access memories. In such a memory cell, the drain must be electrically in contact with the bottom electrode of ferroelectric capacitor stack. If the PZT ferroelectric capacitor stack is directly integrated on Si, however, the chemical reactions and interdiffusion between the bottom electrode and silicon may generate a nonconducting layer, resulting in the failure of the memory cell due to the deterioration of the electric contact between the bottom electrode and silicon. To solve this problem, an extra layer, usually called "diffusion barrier layer," is interposed between PZT capacitor stack and Si wafer to separate them from direct contact. Ideally the diffusion barrier should possess a nature of good oxidation resistance, high thermal and chemical stabilities and large electrical conductivity (so as to function as a bridge to conduct electric current between its bordering layers). In literature, several intermetallic systems such as Pt–(Ti,Al)N and Ir–TiN were investigated for the use of barriers.[7,11–13] While these materials possess very high electrical and thermal conductivities, there are still some concerns such as the formation of Pt hillock structure due to the stress release in the processing, the difficulty in developing a reliable reactive ion etching process for the refractory metals, and the inherently high cost.[14] To find alternative material systems is thus an active topic in recent years. Among several candidates, amorphous Ni–Al seems to be a good choice because it is highly resistant to oxidation, low cost, and ready to be patterned by conventional etching techniques.

In this letter, we report the integration and characterization of a ferroelectric heterostructure $La_{0.5}Sr_{0.5}CoO_3/PbZr_{0.4}Ti_{0.6}O_3/La_{0.5}Sr_{0.5}CoO_3$ on highly doped silicon using amorphous Ni–Al thin film as the conductive diffusion barrier layer (the whole structure is abbreviated as LSCO/PZT/LSCO/*a*-Ni–Al/*c*-Si), mainly aiming to demonstrate the suitability of *a*-Ni–Al for this application. The heterostructure LSCO/PZT/LSCO has been extensively studied in literature. LSCO has a very good electrical conductivity both in its amorphous and crystalline states and the bottom LSCO layer can also serve as a template to achieve fatigue-free PZT capacitors.[15,16] The preparation of PZT by sol-gel technique has been well established in literature and in our laboratory and the properties of PZT are well known, giving us a good reference for assessing the quality of our samples.

The samples were prepared by a multistep procedure. (Step 1) Amorphous Ni–Al thin film (5–50 nm thick) was deposited on highly doped silicon [with resistivity of $(1-3)\times 10^{-3}\ \Omega$ cm] by means of radio frequency (rf) magnetron sputtering. As crystallinity of sputtered Ni–Al film greatly depends on the deposition conditions (e.g., deposition power density and deposition pressure), the deposition parameters were carefully optimized in order to avoid the crystallization of Ni–Al film. We found that the sputtering, using power of 7 W, at room temperature and in an atmosphere of high-purity argon with a pressure of 3 Pa could yield high quality amorphous Ni–Al films. (Step 2) LSCO thin films (70 nm) were deposited on *a*-Ni–Al/Si substrates by magnetron sputtering under the following conditions: temperature= $\sim 25\ ^\circ$C, $Ar:O_2=3:1$, and power=50 W. Postannealing was conducted at 500–550 °C in a tube furnace with flowing

[a]Electronic mail: btliu@mail.hbu.edu.cn

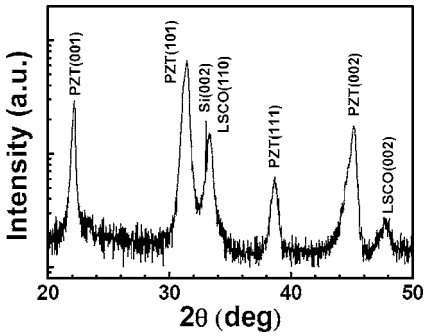

FIG. 1. XRD spectrum of the LSCO/PZT/LSCO/*a*-Ni–Al/Si heterostructure.

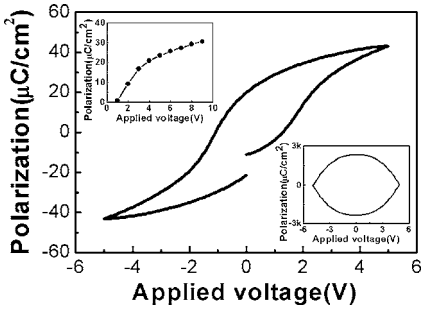

FIG. 3. A typical hysteresis loop of the LSCO/PZT/LSCO capacitors integrated on *a*-Ni–Al/*c*-Si. The insets show the switchable polarization as a function of applied voltage (left, top) and hysteresis loop of the LSCO/PZT/LSCO capacitor integrated on *c*-Ni–Al/*c*-Si (right, bottom).

oxygen. (Step 3) PZT thin films were prepared by the spin coating technique using a modified PZT sol-gel solution followed by annealing at the same temperatures as for LSCO films. (Step 4) On PZT, another LSCO layer was prepared as mentioned in step 2. (Step 5) Pt circular pads with an area of 1.16×10^{-3} cm^2 were defined as the top electrodes for LSCO/PZT/LSCO capacitors through standard photolithography, Pt deposition, and wet chemical etching techniques. (Step 6) The back side of the silicon wafer was cleaned, on which a 100 nm thick aluminum film was deposited to facilitate Ohmic contact for vertical measurements. The phase and crystallinity of the samples were characterized by x-ray diffraction (XRD), and the interfaces were studied using transmission electron microscopy (TEM) and high-resolution TEM (HRTEM). The ferroelectric properties of the samples were vertically determined using a precision *LC* unit from Radiant Technologies.

Figure 1 shows a typical XRD spectrum of the LSCO/PZT/LSCO/*a*-Ni–Al/*c*-Si heterostructure. PZT is found to have been well crystallized with a random crystallographic orientation. No evident peaks of impurities are found, indicating that no reaction occurred between the Ni–Al layer and its adjacent layers. The TEM image of the cross-sectional LSCO/PZT/LSCO/*a*-Ni–Al/*c*-Si heterostructure [Fig. 2(a)] shows that the interfaces related to Ni–Al layer are clear, sharp, and free of inter-reaction and diffusion. HRTEM images of the cross-sectional LSCO/*a*-Ni–Al/Si shown in Figs. 2(b)–2(d) were further employed

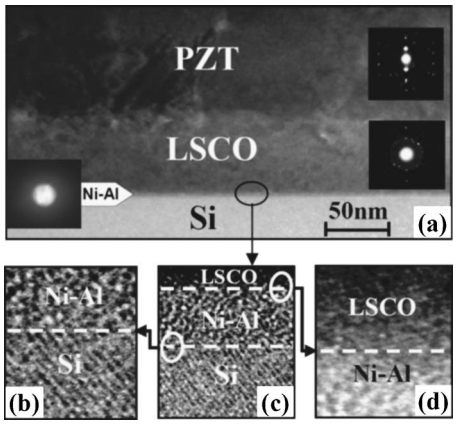

FIG. 2. (a) Cross-sectional structure of the LSCO/PZT/LSCO/*a*-Ni–Al/*c*-Si under transmission electron microscope (TEM). The corresponding SAED patterns are shown in the inset. (b)–(d) present interfaces from various layers under high-resolution TEM. No chemical reaction or interdiffusion between different layers was observed.

to characterize the interfaces and crystallinity. Notice that Ni–Al film is ~5 nm and still amorphous after high temperature process. The absence of grain boundaries makes amorphous diffusion barriers suitable to overcome this type of failure mechanism. The interfaces between Ni–Al and its adjacent layers, i.e., Si/LSCO, are sharp, indicating no reaction at the interfaces. Also, stripes can be found in LSCO image from Fig. 2(d), implying that LSCO is crystallized. The crystallinity of each layer of the heterostructure can also be confirmed by the selected-area electron diffraction (SAED) patterns as shown in the inset of Fig. 2(a). These results are analogous to the recent report of Aggarwal *et al.* on LSCO/Nb-PZT/LSCO/*a*-Ti–Al heterostructure integrated on polycrystalline-Si/Si substrates,[14] suggesting that *a*-Ni–Al is chemically stable under the thermal treatments described above. The oxidation processes and correlation of crystallinity with deposition parameters for *a*-Ti–Al film have been well studied;[17] *a*-Ni–Al film needs to be further investigated.

Ferroelectric properties were characterized using polarization hysteresis and pulsed polarization measurements. Figure 3 shows a typical ferroelectric hysteresis loop measured at 5 V for the LSCO/PZT/LSCO capacitor. The remnant polarization (P_r) and coercive voltage (V_c) are ~22 μC/cm^2 and ~1.15 V, respectively. The dependence of the switchable polarization (ΔP) on the applied voltage is shown in the inset of Fig. 3.[18] Taking into account that the typical P_r values of PZT prepared at higher temperatures (600–650 °C) are also around 15–40 μC/cm^2 and the minimum requirement of P_r for ferroelectric memory is ~10 μC/cm^2, we can conclude that the ferroelectric polarization (20–25 μC/cm^2) of our samples is sufficiently high for memory applications. For comparison, also shown in the inset is the hysteresis loop of the LSCO/PZT/LSCO capacitor fabricated on crystalline Ni–Al/*c*-Si (*c*-Ni–Al/*c*-Si) substrate; we can see that the capacitor is leaky, indicating that crystalline Ni–Al cannot be used as a barrier layer for integrating ferroelectric capacitor stack on Si. Also note that the electrical response of ferroelectric capacitors measured via the underlying silicon substrate is identical to the measurements made using conventional capacitive coupling method, indicating the viability of this approach.

Ferroelectric capacitors used for memory applications should be subjected to a large number of read/write cycles in order to retrieve and store information, and thus a good fatigue resistance is critically important. Fatigue tests were conducted on our samples. In the test, bipolar-pulsed cycles

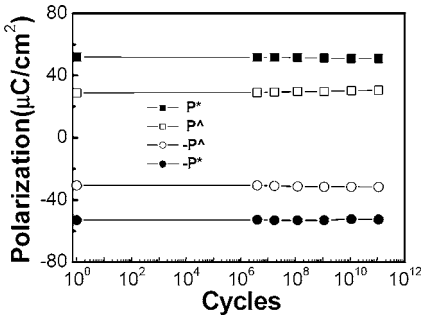

FIG. 4. Fatigue characteristic of the LSCO/PZT/LSCO capacitor as a function of switching cycles.

of 5 V in amplitude and at a frequency of 1.0 MHz were applied on the LSCO/PZT/LSCO capacitors. The switched (P^*) and nonswitched ($P^\wedge$) polarizations were measured through pulsed polarization tests as a function of fatigue cycles as shown in Fig. 4, from which we know that the test capacitors are fatigue-free up to 10^{11} switching cycles. Figure 5 demonstrates the retention characteristic, one of the most important concerns for the ferroelectric random access memory. The test capacitors were applied with write pulse of −5 V in order to write logic state 1 and read pulse of 4 V. The difference between switched (P^*) and nonswitched ($P^\wedge$) polarizations is maintained at about 22 $\mu C/cm^2$ throughout the retention measurement time of 10^5 s without any obvious degradation of the polarization. These physical properties further confirm that the ferroelectric behaviors of the LSCO/PZT/LSCO stack were not influenced by the introduction of Ni–Al in the samples.

In summary, amorphous Ni–Al intermetallic film was demonstrated first as a conductive diffusion barrier layer for integrating LSCO/PZT/LSCO ferroelectric capacitors on Si. Robust physical properties of LSCO/PZT/LSCO capacitors, coupled with the XRD and TEM/HRTEM results, demonstrate that the simple, inexpensive amorphous Ni–Al film can be used as a barrier layer for fabricating high-density ferroelectric random access memories.

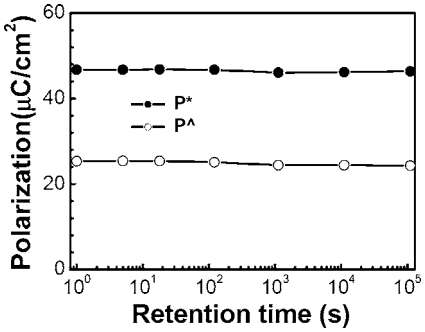

FIG. 5. Polarization of the LSCO/PZT/LSCO capacitor as a function of retention time.

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[18]The switchable polarization ΔP, a parameter that can be directly read on Radiant ferroelectric tester, is defined as the difference between the switched (P^*) and nonswitched ($P^\wedge$) polarizations. Compared with the conventional P_r, ΔP is regarded to reflect the ferroelectric properties more accurately because the interference coming from the leakage current is removed. The larger the ΔP value is, the more "ferroelectric" the material is.