Nonvolatile organic transistor-memory devices using various thicknesses of silver nanoparticle layers

S. M. Wang,[1,2] C. W. Leung,[1] and P. K. L. Chan[2,a)]
[1]Department of Applied Physics, The Hong Kong Polytechnic University, Kowloon, Hong Kong
[2]Department of Mechanical Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong

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We demonstrate the modification of the memory effect in organic memory devices by adjusting the thickness of silver nanoparticles (NPs) layer embedded into the organic semiconductor. The memory window widens with increasing Ag NPs layer thickness, a maximum window of 90 V is achieved for 5 nm Ag NPs and the on/off current ratio decreases from 10^5 to 10 when the Ag NPs layer thickness increases from 1 to 10 nm. We also compare the charge retention properties of the devices with different Ag NPs thicknesses. Our investigation presents a direct approach to optimize the performance of organic memory with the current structure. *© 2010 American Institute of Physics*.
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The advent of the nonvolatile flash memory has provided remarkable benefits for data storage in computers and other portable electronic devices. Due to the advantages of organic electronic devices over their inorganic counterparts such as the low fabrication costs, suitable for large area fabrication, and compatible with flexible substrates,[1,2] organic memory devices fabricated on flexible substrates have great potential for the next generation of nonvolatile flash memory. They can be further integrated with other electronic devices and form a flexible circuit. Recently a 26×26 array of organic flash memory transistors based on floating gate structure was demonstrated on flexible plastic sheets, and the operating voltage was as low as 6 V.[3] Currently, different approaches have been adopted to fabricate organic nonvolatile memory devices, such as using ferroelectric polymer dielectric materials[4,5] and chargeable gate dielectric in the organic field-effect transistors (OFETs).[6] In these devices, the memory effect arises from the field effect modulation by either the spontaneous polarization that occurs in ferroelectric, or through the trapping of charges in a chargeable layer of the dielectric.[7] Usually, the charge-trapping elements in the chargeable gate dielectric are nanoparticles (NPs) of metals such as Cr,[8] Au,[6] and Ag.[9] Compared with ferroelectric polymer-based memory, devices using metal NPs as charge traps have an advantage that the trap density and distribution can be controlled by adjusting the density and location of the NPs during the NP formation process, by using ultrathin metallic films deposition or ion implantation techniques.[10,11]

Recently, we reported a different structure of transistor memory device with remarkable memory window performance by placing silver NPs in between two pentacene layers.[12] A significant advantage of the structure is that it can eliminate the extra fabrication steps for the insulator layers as in the case of floating gate transistor memory structure, making it suitable for integrating with other electronic devices on the same substrate to form a circuit. In the current work, we focused on investigating the performance variation in the pentacene OFET-based memory with different silver NP layer thickness. We also compared the memory window, on/off current ratio, and charge retention properties of the devices. The experimental results suggest a guideline for optimizing the thicknesses of the NP layer in the device for different application criteria.

The bottom-gate transistor memory devices were fabricated on highly doped *n*-type Si substrates with 300 nm SiO_2, and the device configuration was in the form of pentacene/Ag NPs/pentacene [schematic diagram shown in Fig. 2(a)]. Pentacene thin films and silver NPs were thermally evaporated at a base pressure of 1×10^{-7} Torr. The thickness of the first and second pentacene layers were 15 nm and 25 nm, respectively. The Ag layer varied with a nominal thickness of 1, 5, and 10 nm, and the corresponding devices were named as devices A1, A5, and A10. The 50 nm thick silver source and drain electrodes were patterned by shadow mask, and the channel lengths (L) and widths (W) were 50 μm and 1000 μm, respectively. The output and double-sweep transfer characteristics of the transistors were measured by two Keithley 2400 sourcemeters. All the measurements were performed in dark and ambient conditions, immediately after the devices were taken out of the thermal evaporation chamber.

The output characteristics for devices A1, A5, and A10 are shown in Figs. 1(a)–1(c). The gate voltage (V_g) was varied from 0 to -60 V with a 10 V step. It can be noticed that for devices A1 and A5, the output curves exhibit a typical p-channel field-effect transistor behavior, with the hole accumulation mode at negative V_g and hole depletion mode at positive V_g. The calculated carrier mobility in the saturation region is about 0.34 $cm^2\ V^{-1}\ s^{-1}$ for device A1, three times larger than that of device A5 (0.10 $cm^2\ V^{-1}\ s^{-1}$). However, device A10 does not show obvious saturation in the output curves and the drain source current is large (about 2×10^{-6} A) even at a positive gate bias of 60 V, which suggests the off state of device A10 cannot be achieved.

The hysteresis properties of these three devices were investigated by cyclic sweeping of V_g (i.e., from positive to negative and then back to positive). The memory window of a device is defined as the difference of the threshold voltages in the two V_g sweeping directions, i.e., $\Delta V_{th}=V_{th1}-V_{th2}$. As shown in Fig. 1(d), the memory window shows a remarkable

a)Author to whom correspondence should be addressed. Tel.: +852 27666664. Electronic mail: mmklchan@polyu.edu.hk.

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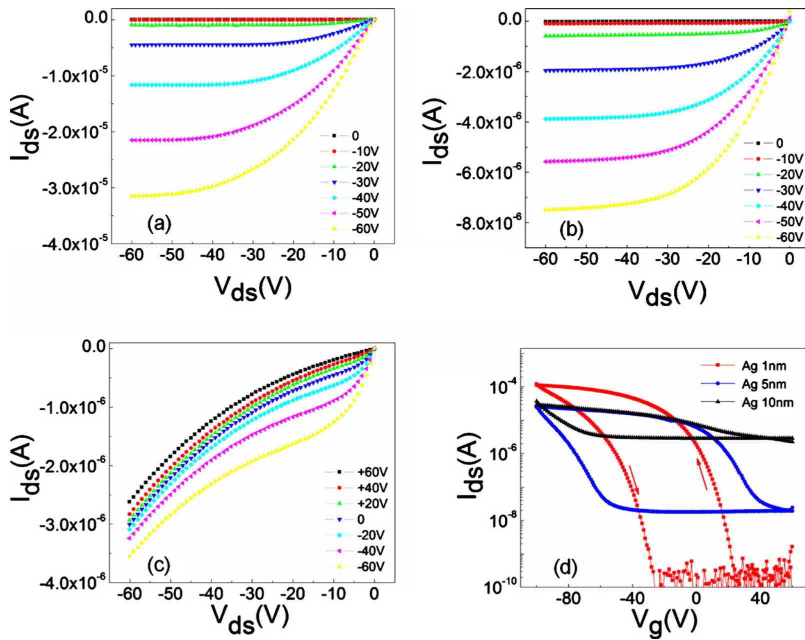

FIG. 1. (Color online) The output characteristics of the transistor memory with Ag NPs thickness of (a) 1 nm, (b) 5 nm, and (c) 10 nm. (d) The transfer characteristics of the transistor memory with Ag NPs thickness 1–10 nm.

dependence on the silver NP layer thickness. When the Ag NPs thickness is 1 nm, the memory window is about 60 V, with a large on/off current ratio of 10^5. When the NP layer thickness increases to 5 nm, the memory windows increase to 90 V, and the on/off current ratio drops to 10^3 due to the larger off current. For the device with 10 nm thick Ag NPs, although the off state is difficult to be defined from the output characteristic curves, a significant memory window can still be observed in the transfer characteristic curve with a small on/off current ratio of 10. The decrease in on/off current ratio from device A1 to A10 is believed to be due to the gradual size increase and partially connected silver NPs, which are likely to create low resistance current paths and hence increases the off-current.

As the physical origin of the memory effect in the devices is due to the thermal evaporated Ag atom diffusing and penetrating into the pentacene layer and forming dopant-like traps,[13,14] the enhancement of the memory window is attributed to the larger trap density induced by the NPs. Scanning electron microscopy (SEM) images of Ag NPs on 15 nm pentacene layer are shown in Figs. 2(b)–2(d). For 1 nm Ag NPs, the NPs cannot be clearly observed in the SEM image and it is possibly due to the resolution limit of the SEM. On the other hand, for 5 and 10 nm thick Ag layers deposited on pentacene, NPs with different size can be clearly observed as shown in Figs. 2(c) and 2(d). The areal densities of Ag NPs are evaluated by the image processing function in MATLAB as 3.3×10^{11} cm^{-2} and 1.9×10^{11} cm^{-2} in device A5 and A10, respectively, one order of magnitude higher than that of gold NPs formed on SiO_2 insulating layer by solution immersion method ($2-5\times10^{10}$ cm^{-2}) with the memory window of 22 V.[15] Practically, the large memory window and small on/off ratio of 10^3 of device A5 allow us to design devices with multilevel storage despite compromised on/off current ratio,[16] while device A1 can satisfy applications which re-

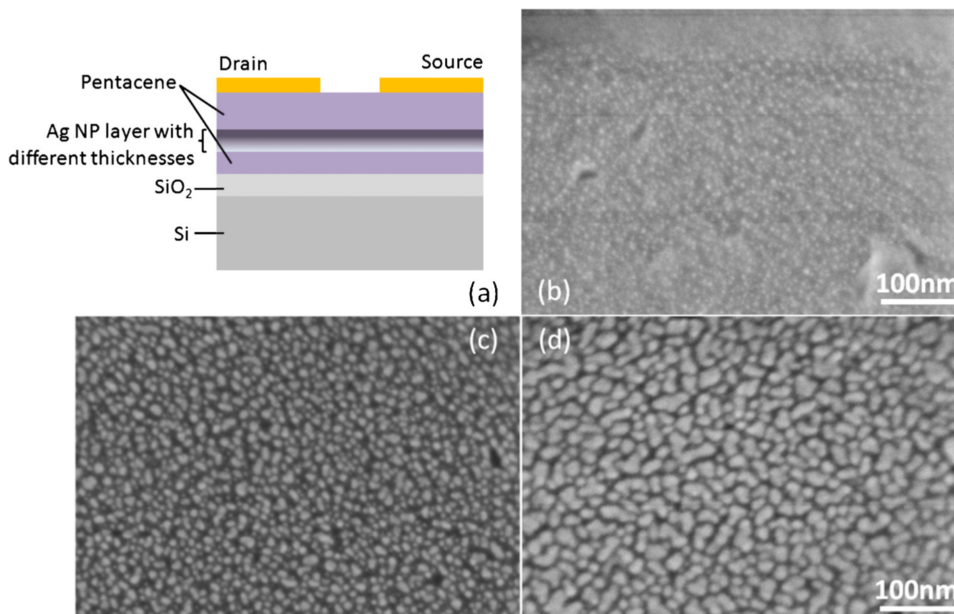

FIG. 2. (Color online) (a) The schematic structure of pentacene/Ag/pentacene configuration devices; SEM images of Ag NPs on 15 nm bottom pentacene layer, the nominal thickness for Ag NPs are (b) 1 nm, (c) 5 nm, and (d) 10 nm.

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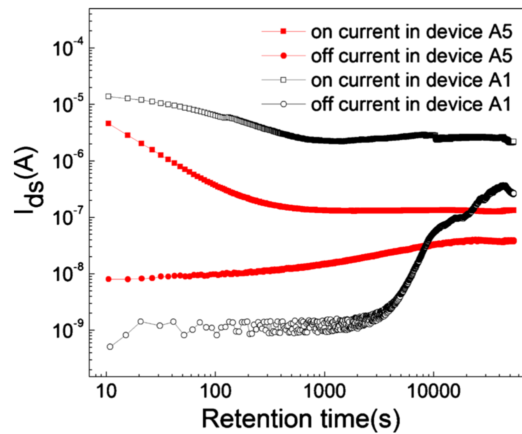

FIG. 3. (Color online) Retention time measurement for devices A1 and A5.

quire a moderate memory window but a large on/off current ratio.

Retention time of charge carriers is another important parameter for the operation of nonvolatile memory devices. Figure 3 shows the retention time of on- and off-currents of device A1 and A5. After applying a writing pulse of −100 V (erasing pulse of +100 V) with a pulse width of 5 s, we measured the off- (on-) current with time intervals of 5 s at $V_g=0$ V and $V_{ds}=-60$ V. To eliminate the aging effect in ambient conditions and to ensure identical starting conditions, the samples were stored under vacuum for about 10 h after finishing the on-current measurement and before the off-current measurement was performed. The on-current of both devices show an obvious decay at initial stage and then keep constant for both devices. This initial decrease is related to the trap filling process by the applied drain source voltage as the traps are emptied after positive gate bias of 100 V. During the trap filling process, the number of free charge carriers decreases hence the on-current decreases. For device A5, the on-current decays faster than that of device A1 and it could be due to its larger trap density in device A5. The off-current, on the contrary, shows a remarkable difference for the two devices; in device A5, the off-current increases slowly during the whole measurement time of 12 h, demonstrating a long trap lifetime and a relatively stable charge retention behavior; the on/off current ratio decreases from 500 at the beginning to 3.5 after 12 h. However, in device A1, the off-current maintains constant at the first one hour then rises sharply by two orders of magnitude, indicating a poor charge retention capability of the trap states in this device. Thus, the initial high on/off current ratio of 10^4 decreased to 10 after 12 h. It is also important to notice that the off-current of device A1 is larger than A5 after 12 h of measurement. Such an increase in the off-current is related to the charges releasing process from the trap centers, and the difference in charge retention behavior may be ascribed to the difference trap states level in 1 and 5 nm Ag NPs. As discussed by other groups,[17–19] the work function of metal increases with decreasing size of NPs, hence the 1 nm Ag NPs has a Fermi level closer to highest occupied molecular orbital level of pentacene while comparing with the 5 nm Ag NPs. As a result the shallower trapped charges in device A1 were released more easily from the trap centers and resulting in a fast increase in the off-current in the retention time measurement. On the contrast, the deeper traps level in 5 nm Ag NPs device are beneficial for the stored charges, therefore reducing the charges loss rate and enhancing the charge retention property. Similar mechanism has been observed in silicon based metal-oxide-semiconductor memory where deep traps density in the floating gate governs the charge retention of the device.[20–22]

In conclusion, OFET-based memory devices with different memory properties were demonstrated by controlling the Ag NPs layer thickness. The 1 nm Ag NP device shows a moderate memory window with 60 V and large on/off current ratio at about 10^5. The 5 nm device exhibits larger memory window of 90 V but the on/off current ratio decrease to 10^3. The charge retention behaviors of the devices were also studied and 5 nm Ag NP device show a longer retention time comparing with the 1 nm Ag NP device. The variation in the retention time is due to different trap states level similar to the silicon based memory device. Our finding suggests a way to optimize the organic memory performance for different application criteria.

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