Performance Considerations of PFC Switching Regulators Based on Non-Cascading Structures

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***Abstract*— This paper discusses the characteristics of power-factor-correction (PFC) switching regulators of non-cascading structures in terms of efficiency, input current harmonic distortion, and load transient response. The discussion begins with simplified power flow diagrams of the non-cascading PFC switching regulators and describes their essential features for achieving power factor correction and tight voltage regulation. Based on these diagrams, the various configurations of switching regulators can be classified into three categories, each offering a different possibility of performance tradeoffs. The first category permits tradeoff between efficiency and input current harmonic contents, the second permits tradeoff between efficiency and load transient response, and the third allows tradeoffs among all performance areas. The paper briefly reviews the non-cascading structures of PFC switching regulators in terms of the three categories. Simulation and experimental results are provided to illustrate the performance tradeoffs in these PFC switching regulators.**

***Index Terms*— Ac-dc converter, efficiency, harmonic distortion, load transient, power factor correction, voltage regulation.**

I. Introduction

Power factor correction (PFC) is becoming a mandatory functional requirement for ac-dc switching regulators [1]–[2], in addition to fast load transient response and highly efficient power conversion. Switching regulators, in general, achieve their function by using two basic converters together with a low-frequency (100 Hz or 120 Hz) energy storage element which acts as an energy buffer to maintain power balance between the instantaneous input power and the output power [3]. The usual construction involves cascading a PFC pre-regulator and a voltage regulator. Recently, motivated by an efficiency concern, non-cascading structures have been considered for constructing PFC switching regulators. Essentially, non-cascading structures prevent double processing of power by the two essential stages and hence reduce the overall power loss [4]–[17]. While such non-cascading structures allow efficiency to be improved, they present several unsolved design problems relating to the optimization among a few basic performances, namely, power factor, load transient response, and efficiency.

Our objective in this paper is to investigate the effects of the choice of non-cascading topologies on the performances of PFC switching regulators. We begin with some descriptions of the non-cascading topologies in terms of simplified power flow diagrams [18]–[19]. Using these diagrams, we classify the PFC switching regulators of non-cascading structures into three categories, each of which has a different possibility of performance tradeoff. The first category permits tradeoff between efficiency and input current harmonic contents, the second permits tradeoff between efficiency and load transient response, and the third allows tradeoffs among all performance areas. We will take a brief literature survey of the non-cascading PFC switching regulators [4]–[17] and then focus on the performance analysis of the the various categories of structures. Finally, we present simulation experimental results to illustrate the performance tradeoffs in these PFC switching regulators.

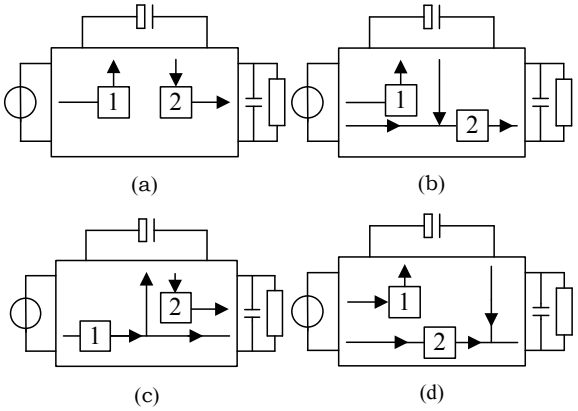

Fig. 1. Power flow graphs for describing PFC switching regulators. (a) Classical (cascade), (b) Category 1, (c) Category 2, and (d) Category 3.

II. Power Flow Diagrams

The power flow diagrams describing several PFC switching regulators are shown in Fig. 1. The branches in the power flow diagrams denote the paths through which power is being transferred, and the arrows on the branches indicate the direction of the power flow. Square boxes 1 and 2 represent the PFC pre-regulator and the voltage regulator, respectively. Suppose that the regulators allow power to be transferred in only one direction, and that the storage element is a capacitor and allows a bi-directional power flow.

Fig. 1 (a) presents the power flow diagram of the classical PFC switching regulator which adopts a cascade structure. The total input power is transferred from the input power source to the storage element through the pre-regulator and then to the load through the voltage regulator. In this case, the input

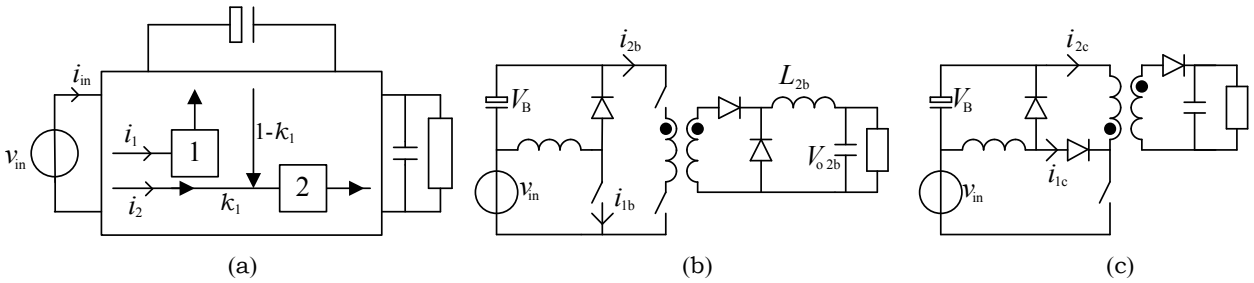

Fig. 2. (a) Power flow diagram of Category 1 switching regulators, (b) a simple example proposed by [5]; and (c) another one from [6].

power and the output power is fully controllable by the pre-regulator and the voltage regulator, thus achieving PFC and fast load transient response. The efficiency is degraded as a result of the serial power processing. The overall efficiency of this kind of PFC regulators is

$$\eta_{\text{classical}} = \eta_1\eta_2, \tag{1}$$

where η_1 and η_2 are the efficiencies of the pre-regulator and the voltage regulator, respectively.

The power flow diagrams of the non-cascading PFC switching regulators are shown in Figs. 1 (b) to (d). Fig. 1 (b) presents Category 1 switching regulators [4]–[8]. In this category, the output power is completely controlled by the voltage regulator (converter 2). Thus, the load transient response can be independently controlled. On the other hand, the input power is split into two parts, one going into the PFC pre-regulator and the other going to the storage, and both to the load eventually. The overall efficiency of the switching regulators in this category is

$$\begin{aligned}\eta_{\text{Category1}} &= k_1\eta_2 + (1-k_1)\eta_1\eta_2 \\ &= \eta_1\eta_2 + \eta_2 k_1(1-\eta_1),\end{aligned} \tag{2}$$

where k_1 is the ratio at which the input power is split between the pre-regulator and the storage. Clearly, *tradeoff is mainly possible between the efficiency improvement and the attainable power factor.* In this category, k_1 is the parameter that controls the tradeoff.

The non-cascading PFC switching regulators proposed in some earlier publications [9]–[14] belong to Category 2 and the power flow diagram is given in Fig. 1 (c). All of the input power in this category of switching regulators goes to the PFC pre-regulator. Thus, the input current can be independently shaped by the PFC pre-regulator. The output from the PFC pre-regulator is split between the storage (then voltage regulator) and a direct path to the load. The efficiency of this category of switching regulators is

$$\begin{aligned}\eta_{\text{Category2}} &= k_2\eta_1 + (1-k_2)\eta_1\eta_2 \\ &= \eta_1\eta_2 + \eta_1 k_2(1-\eta_2),\end{aligned} \tag{3}$$

where k_2 is the ratio at which the output of the pre-regulator is split between the storage and a direct path to the load. Clearly, *the transient response of the switching regulator can be traded off for some efficiency improvement*, i.e., the load transient response is impaired by large value of k_2 [12]–[13].

Fig. 1 (d) represents Category 3 switching regulators [15]–[17]. The efficiency of this category of PFC regulators is

$$\eta_{\text{Category3}} = k_3\eta_1 + (1-k_3)\eta_2, \tag{4}$$

where k_3 is the ratio at which the input power is split between the pre-regulator and the storage. Clearly, *both the power factor and the load transient response of the switching regulators cannot be independently controlled.* Thus, the power split ratio represents tradeoff between efficiency, power factor and load transient response. While this arrangement provides some flexibility for engineers to optimize performance, the analysis can be rather complicated.

III. Performance Analysis

We make several assumptions about PFC switching regulators with non-cascading structures prior to our analysis. First, each PFC switching regulator is composed of a pre-regulator and a voltage regulator, which have two clearly separated pre-regulator and voltage regulator allowing independent control of the individual duty cycles. The independent control circuitries are the key to achieving low current harmonic and fast load transient response simultaneously in the switching regulator. Also, the input voltage of the switching regulator is a rectified sinusoid, and then the input current of the pre-regulator is also a rectified sinusoid. Finally the output voltage of the voltage regulator is the desired dc voltage.

A. Category 1 PFC switching regulators

Referring to (2) and Fig. 2 (a), the output power of Category 1 PFC switching regulators can be defined by

$$P_{\text{Category1}} = \eta_2(P_{\text{in}}k_1 + \overline{P_{\text{in}}(1-k_1)}\eta_1). \tag{5}$$

$\overline{P_{\text{in}}(1-k_1)}$ is the averaged input power of the pre-regulator and is given by

$$\begin{aligned}P_{\text{in}}(1-k_1) &= \hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|\ \hat{i}_1|\sin 2\pi f_{\text{m}}t| \\ &= \frac{\hat{v}_{\text{in}}\hat{i}_1}{2}(1-\cos 4\pi f_{\text{m}}t). \\ \overline{P_{\text{in}}(1-k_1)} &= \frac{\hat{v}_{\text{in}}\hat{i}_1}{2},\end{aligned} \tag{6}$$

where $\hat{v}_{\text{in}}$ and $\hat{i}_1$ are the peak input voltage and the peak input current of the pre-regulator respectively; f_{m} is the ac mains frequency. The power stored in the storage element is $\frac{\hat{v}_{\text{in}}\hat{i}_1}{2}\eta_1$.

Also, $P_{\text{in}}k_1$ is the power directly transferred from the ac mains to the input port of the voltage regulator and is given by

$$P_{\text{in}}k_1 = \hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|\ i_2. \tag{7}$$

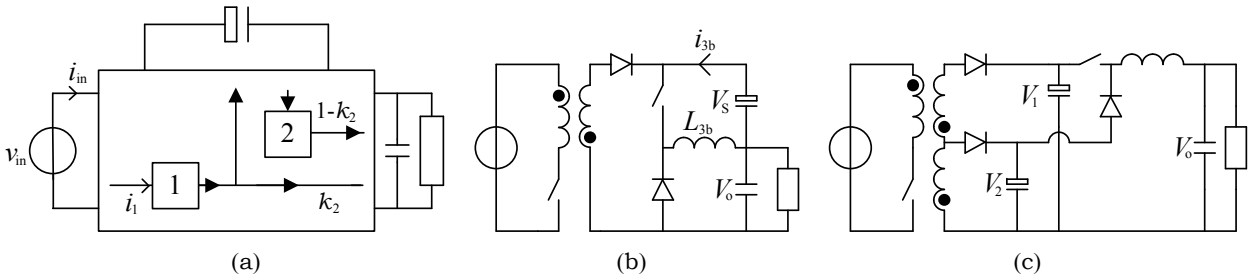

Fig. 3. (a) Power flow diagram of Category 2 switching regulators, (b) a simple example proposed by [10], and (c) another one from [13].

Putting (6) and (7) in (5), we get

$$P_{\text{Category1}} = \eta_2(\hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|\ i_2 + \frac{\hat{v}_{\text{in}}\hat{i}_1}{2}\eta_1). \quad (8)$$

$$i_2 = \frac{P_{\text{Category1}}}{\eta_2\hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|} - \frac{\hat{i}_1\eta_1}{2|\sin 2\pi f_{\text{m}}t|}, \quad (9)$$

where i_2 is a part of the input current of the switching regulator. This current directly goes to the voltage regulator. Thus, the total input current of this category switching regulator is

$$i_{\text{in}} = \frac{P_{\text{Category 1}}}{\eta_2\hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|} - \frac{\hat{i}_1\eta_1}{2|\sin 2\pi f_{\text{m}}t|} + \hat{i}_1|\sin 2\pi f_{\text{m}}t|. \quad (10)$$

Examples: Based on the foregoing analysis, we apply (5)–(10) in the switching regulators proposed earlier [5], [6] to calculate the input current harmonic distortion. Figs. 2 (b) and (c) show the simplified circuits of the proposed switching regulators. For the circuits of Figs. 2 (b) and (c), k_1 is

$$k_1 = \frac{\hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|}{V_{\text{B}} + \hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|}, \quad (11)$$

where V_{B} is the voltage of the storage element. From Fig. 2 (b), $i_{2\text{b}}$ can be given by

$$i_{2\text{b}} = \frac{P_{\text{Category1}}}{\eta_2(V_{\text{B}} + \hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|)}. \quad (12)$$

Putting (8) and (11) in (12), we have the input current of Fig. 2 (b), as

$$i_{\text{in}} = \frac{\hat{v}_{\text{in}}\hat{i}_{1\text{b}}\eta_1}{2(1-k_1)(V_{\text{B}} + \hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|)} + \hat{i}_{1\text{b}}|\sin 2\pi f_{\text{m}}t|. \quad (13)$$

where η_1 and η_2 are the efficiencies of the buck-boost converter and the two-switch forward converter, respectively, shown in Fig. 2 (b).

The input voltage value of voltage regulators is one of important parameters that affects the transient response time of the switching regulators. In the classical PFC switching regulators, this value is fixed and controlled by a PFC controller, therefore the transient response time affected by input voltage is also fixed. However in these two examples, this value is changing and is depended by k_1. Referring to Fig. 2 (b), the minimum transient response time affected by the input voltage of the voltage regulator can be evaluated by

$$\frac{\Delta i_{2\text{b}}}{\Delta t_{2\text{b}}} = \frac{(V_{\text{B}} + \hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|) - V_{\text{o2b}}}{L_{2\text{b}}}. \quad (14)$$

where $\Delta i_{2\text{b}}$ is the change in input current of the voltage regulator at load transient period, V_{o2b} is the output voltage, and $L_{2\text{b}}$ is inductance of the output inductor. Assuming that the transformer turn ratio is $1:1$, the duty cycle is unity in the transient period, and the output power is changed from 10% of full load condition to 90%, we can show that,

$$\Delta i_{2\text{b}} = \frac{(0.9P_{\text{Category1}} - 0.1P_{\text{Category1}})}{(V_{\text{B}} + \hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|)\eta_2}, \quad (15)$$

where η_2 is the efficiency of the two-switch forward converter in Fig. 2 (b). By using (11), then (15) & (14) give the minimum transient response time affected by the input voltage of the voltage regulator for Fig. 2 (b), as

$$\Delta t_{2\text{b}} = \frac{(0.9P_{\text{Category1}} - 0.1P_{\text{Category1}})L_{2\text{b}}}{\eta_2((\frac{\hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|}{k_1})^2 - V_{\text{o2b}}\frac{\hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}}t|}{k_1})}. \quad (16)$$

Clearly, the current harmonic distortion and the efficiency of Category 1 switching regulators are directly affected by k_1. The transient response time of this category switching regulators is influenced by the circuit parameters of the voltage regulator including k_1.

B. Category 2 PFC switching regulators

Fig. 3 shows the power flow diagram of the switching regulators under Category 2. The input current of the switching regulators is completely processed by the pre-regulator. Suppose that the current is a rectified sinusoid. The output power is represented by

$$P_{\text{Category2}} = \eta_1(P_{\text{out}}k_2 + \overline{P_{\text{out}}}(1-k_2)\eta_2), \quad (17)$$

where $\overline{P_{\text{out}}}$ is the averaged output power of pre-regulator. Thus, (17) can be extended to

$$P_{\text{Category2}} = \eta_1(k_2\frac{\hat{v}_{\text{in}}\hat{i}_1}{2}(1-\cos 4\pi f_{\text{m}}t) + (1-k_2)\frac{\hat{v}_{\text{in}}\hat{i}_1}{2}\eta_2), \quad (18)$$

and k_2 becomes

$$k_2 = \frac{P_{\text{Category2}} - \overline{P_{\text{out}}}\eta_1\eta_2}{P_{\text{out}}\eta_1 - \overline{P_{\text{out}}}\eta_1\eta_2}. \quad (19)$$

Obviously, k_2 is equal to zero, when $P_{\text{Category2}}$ is equal to $\overline{P_{\text{out}}}\eta_1\eta_2$. This means that the input power is processed by the PFC pre-regulator and the voltage regulator serially. This is the least efficient power conversion. When k_2 is equal to one, the total output power of the PFC pre-regulator is directly transferred to the load and the output voltage without a tight voltage regulation. Therefore, the maximum value of k_2 should be less than 1 for a tight voltage regulation.

Examples: We use two examples to explain the relationship between the dynamic response of Category 2 switching regulators and the value of k_2. The two example circuits were proposed in [10] and [13]. Figs. 3 (b) and (c) show the proposed circuits. In Fig. 3 (b), k_2 can be defined by $k_{2\mathrm{b}} = \frac{V_\mathrm{o}}{V_\mathrm{S}+V_\mathrm{o}}$. The output voltage of the PFC pre-regulator contains low frequency (100 Hz or 120 Hz) ripple voltage. Thus, the output voltage of the PFC pre-regulator must contain a dc voltage which is larger or equal to the output voltage to fulfil the output voltage regulation. In Fig. 3 (c), moreover, k_2 is represented by $k_{2\mathrm{c}} = \frac{V_2}{V_1}$. In order to provide tight voltage regulation, it must satisfy $V_2 < V_\mathrm{o} < V_1$, i.e., $k_{2\mathrm{b}}$ should be smaller than 1. Furthermore, k_2 controls the input voltage value of the voltage regulator and has an impact on the transient response time, from Fig. 3(b)

$$\frac{\Delta i_{3\mathrm{b}}}{\Delta t_{3\mathrm{b}}} = \frac{V_\mathrm{s}}{L_{3\mathrm{b}}}, \tag{20}$$

where $\Delta i_{3\mathrm{b}}$ is the change in input current at load transient period, V_s is the input voltage of the buck-boost converter, and $L_{3\mathrm{b}}$ is an inductance of the converter. Assuming that again, the duty cycle is unity in the transient period and the load is changed from 10% of the full load condition to 90%, we can get

$$\Delta i_{3\mathrm{b}} = \frac{(0.9P_{\mathrm{Category2}} - 0.1P_{\mathrm{Category2}})}{\eta_2 V_\mathrm{s}}. \tag{21}$$

where η_2 is the efficiency of the buck-boost converter in Fig. 3 (b). Therefore, the minimum transient response time affected by the input voltage is

$$\Delta t_{3\mathrm{b}} = \frac{(0.9P_{\mathrm{Category2}} - 0.1P_{\mathrm{Category2}})L_{3\mathrm{b}}}{\eta_2 V_\mathrm{s}^2}. \tag{22}$$

For maintaining a high power factor, the pre-regulators can only provide a slow power transient response and the bandwidth of this response is about one-fifth of the ac mains frequency [20], therefore the buffer energy stored in the storage element becomes a critical parameter in the load transient view point. The energy stored in the storage elements is presented by

$$\text{Energy} = \text{Power} \times \text{Time} = \frac{1}{2}CV^2. \tag{23}$$

To ensure that the transient response of PFC switching regulators will not be affected by its slow power transient response of the pre-regulators, the energy stored in the storage elements must support all the output power in one-fifth of the ac mains period time. Since k_2 is a ratio between the input voltage and output voltage of this category switching regulators and the voltage level of this category switching regulator is relatively lower than the classical one, the capacitance of this category regulators must be larger than that of the classical counters part for saving the same energy.

From these two examples, we can also observe that the duty cycle of the voltage regulator of the circuits is large, when $k_{2\mathrm{b}}$ and $k_{2\mathrm{c}}$ are kept high. Thus, the headroom for changing the duty cycle becomes quite small, and the dynamic response of the voltage regulators is restrained by this narrow margin.

Eventually, k_2 not only affects the transient response and the gain of efficiency of this category switching regulators, but also gives a penalty in the cost of the energy storage element.

C. Category 3 PFC switching regulators

The non-cascading PFC switching regulators proposed earlier by [15]–[17] belong to Category 3. The output voltage of these switching regulators contains low-frequency ripples because of the connection between the storage element and the two converters. The only way to reduce this ripple voltage is to use a bigger output capacitor.

In fact, this category of switching regulators can be represented by several different power flow diagrams [18]. One of the power flow diagrams of this category is shown in Fig. 4. First, (4) can be extended to

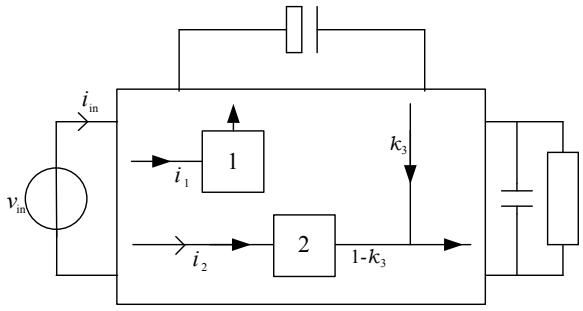

Fig. 4. A power flow diagram of Category 3 switching regulators.

$$\begin{aligned} P_{\mathrm{Category3}} &= \eta_1 \hat{v}_{\mathrm{in}} \hat{i}_1 |\sin 2\pi f_\mathrm{m} t|^2 \\ &\quad + \eta_2 \hat{v}_{\mathrm{in}} |\sin 2\pi f_\mathrm{m} t| i_2, \end{aligned} \tag{24}$$

where the input current of the PFC pre-regulator is a rectified sinusoidal current, $\hat{i}_1|\sin 2\pi f_\mathrm{m} t|$ and the input current of the switching regulator is equal to $i_1 + i_2$. Also, i_2 can be derived by

$$i_2 = \frac{P_{\mathrm{Category3}}}{\eta_2 \hat{v}_{\mathrm{in}} |\sin 2\pi f_\mathrm{m} t|} - \frac{\eta_1}{\eta_2} \hat{i}_1 |\sin 2\pi f_\mathrm{m} t|, \tag{25}$$

Thus, i_{in} is equal to

$$\begin{aligned} i_{\mathrm{in}} &= \frac{P_{\mathrm{Category3}}}{\eta_2 \hat{v}_{\mathrm{in}} |\sin 2\pi f_\mathrm{m} t|} - \frac{\eta_1}{\eta_2} \hat{i}_1 |\sin 2\pi f_\mathrm{m} t| \\ &\quad + \hat{i}_1 |\sin 2\pi f_\mathrm{m} t|. \end{aligned} \tag{26}$$

In this power flow diagram, k_3 can be written as

$$\begin{aligned} k_3 &= \frac{P_{\mathrm{preregulator}}}{P_{\mathrm{in}}} \\ &= \frac{\hat{i}_1 |\sin 2\pi f_\mathrm{m} t|}{i_2 + \hat{i}_1 |\sin 2\pi f_\mathrm{m} t|}, \end{aligned} \tag{27}$$

where $P_{\mathrm{preregulator}}$ is the input power of the pre-regulator which is transferred to the load via the storage element, and P_{in} is the input power of the switching regulator. Putting (27) into (26), we get

$$i_{\mathrm{in}} = \frac{P_{\mathrm{Category3}}}{(\eta_2 + \eta_1 k_3) \hat{v}_{\mathrm{in}} |\sin 2\pi f_\mathrm{m} t|} + \frac{\eta_2 \hat{i}_1 |\sin 2\pi f_\mathrm{m} t|}{\eta_2 + \eta_1 k_3}. \tag{28}$$

Clearly, k_3 is an important parameter which affects the input current harmonic distortion and the dynamic response of Category 3 switching regulators.

IV. Simulation Results

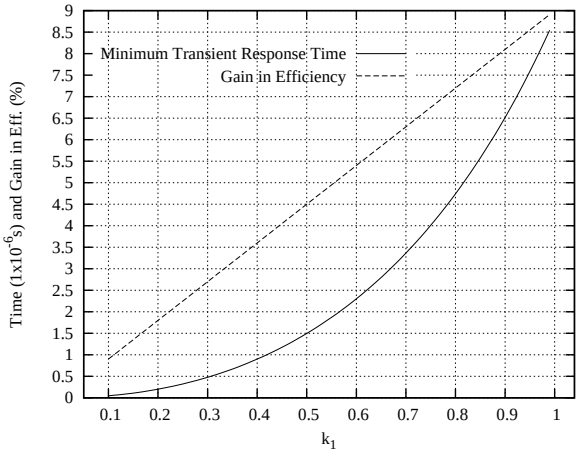

Fig. 5. The relationship for Fig. 2(b) switching regulator between k_1, the minimum transient response time (μs), and the gain in efficiency (%).

Some simulation results of Category 1 PFC regulators and Category 2 PFC regulators are presented here. In the simulation, the specifications of switching regulators are defined as follows: the output voltage is $48\ V_{\rm dc}$, the input voltage of the switching regulator is $110\ V_{\rm ac}$ and the ac mains frequency is 50 Hz, the efficiency of the pre-regulator and the voltage regulator are 90 %, the output power of the switching regulator is 100 W, and the output inductor of the voltage regulator is $500\ \mu$H. By using (2), (11), and (16), the relationship between k_1, transient response time and gain in efficiency is given in Fig. 5. Fig. 6 shows minimum transient response time, input voltage of voltage regulator, and gain in efficiency in Category 2 PFC regulators at the different value of k_2. Using (23), the capacitance of the energy storage element is also shown in Fig. 6. The storage time is set for 0.1 s, which is time for one-fifth in 50 Hz ac mains voltage, at 100 W output power.

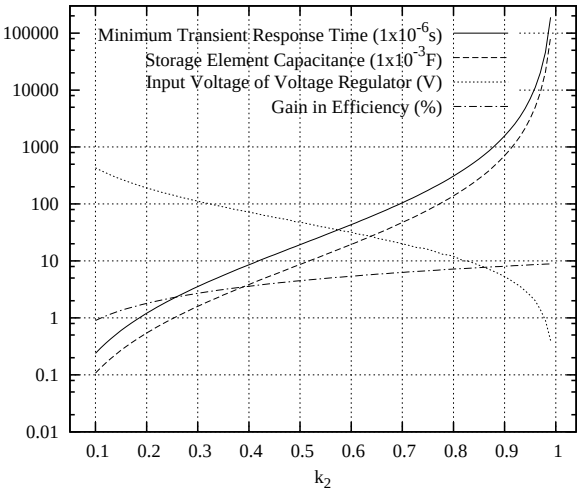

Fig. 6. The relationship for Fig. 3(b) switching regulator between k_2 and its parameters.

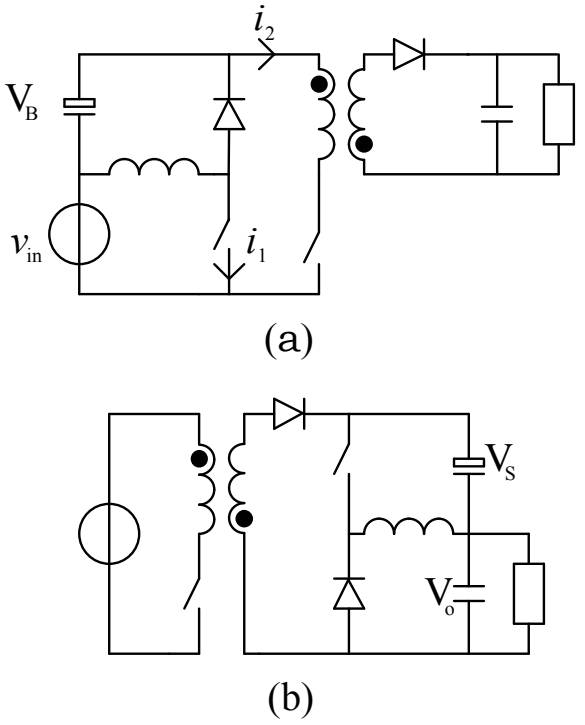

Fig. 7. The simplified circuit diagram of the prototypes. (a) Category 1 PFC regulator and (b) Category 2 PFC regulator.

V. Experimental Results

Two laboratory prototypes are built to demonstrate the performances of Category 1 PFC regulators and Category 2 PFC regulators experimentally. Figs. 7 (a) and (b) show the simplified circuit diagram of Category 1 PFC regulators and Category 2 PFC regulators, respectively. In the prototype of Category 1 PFC regulator, the pre-regulator is a buck-boost converter and the voltage regulator is a flyback converter. In the prototype of Category 2 PFC regulator, the pre-regulator and the voltage regulator are a flyback converter and a buck-boost converter, respectively. Those converters are controlled by their own control circuitries. The major specifications of the prototypes are as follows: the input voltage is $110\ V_{\rm ac}$, the output voltage is 48 V, the maximum output power is 100 W, and the switching frequency for both regulators are 100 kHz. Fig. 8 shows the total current harmonic distortion of Category 1 PFC regulator for different k_1 conditions. Figs. 9 (a) to (c) show the gain in efficiency of Category 1 PFC regulator compared with the cascading structure for different values of k_1. Figs. 10 (a) to (c) show the waveforms of this category PFC regulator: input voltage of the voltage regulator (upper trace), input voltage (middle trace) and input current (lower trace) of the PFC regulator. The decreased k_1 leads the gain in the efficiency is decreasing, but the total current harmonic distortion of this category PFC regulator is improved by lower k_1.

Figs. 11 (a) to (c) show the waveforms of Category 2 PFC regulator: output voltage of the pre-regulator (upper trace), input voltage (middle trace) and input current (lower trace) of the PFC regulator. Fig. 12 shows the overall efficiency of this category PFC regulator for different values of k_2. Fig. 13

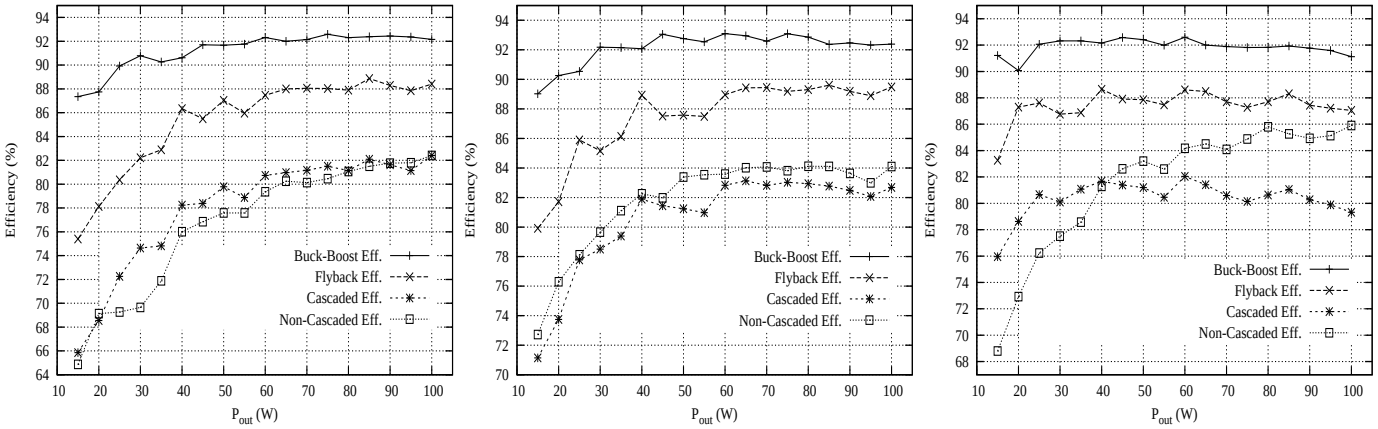

Fig. 9. Efficiency comparison of Category 1 PFC regulator [Fig. 7(a)], showing the non-cascading structure efficiency and the cascading structure efficiency for different values of k_1: (a) k_1 = 0.3, (b) k_1 = 0.4, and (c) k_1 = 0.5.

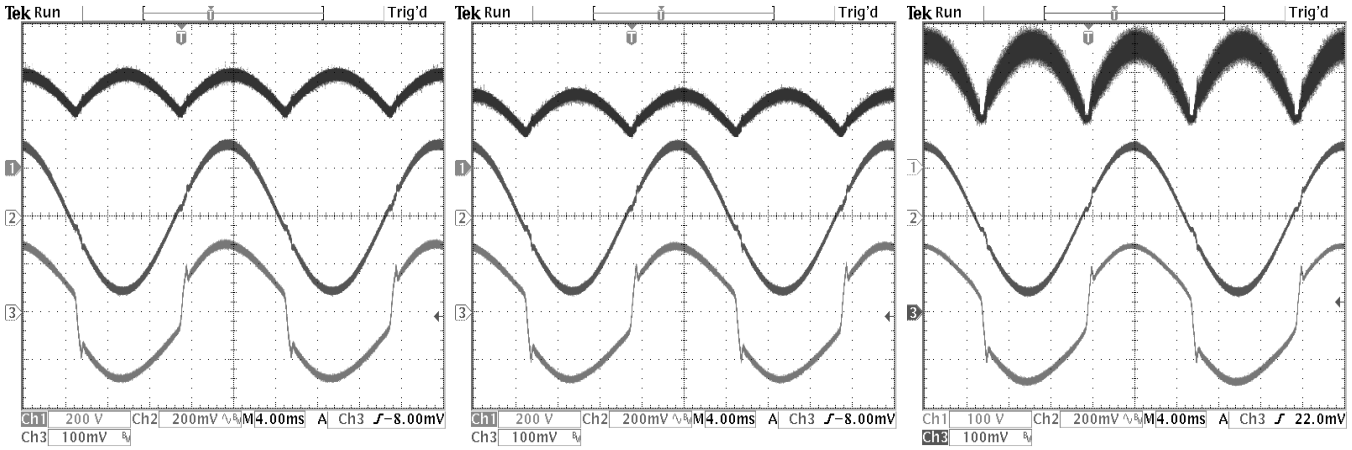

Fig. 10. The measured waveforms of Category 1 PFC regulator [Fig. 7(a)]: input voltage of voltage regulator (upper trace), input voltage (middle trace) and filtered input current (lower trace) of the regulator for different values of k_1: (a) k_1 = 0.3, (Ch1: 200 V/div, Ch2: 100 V/div, and Ch3: 1 A/div) (b) k_1 = 0.4, (Ch1: 200 V/div, Ch2: 100 V/div, and Ch3: 1 A/div) and (c) k_1 = 0.5, (Ch1: 100 V/div, Ch2: 100 V/div, and Ch3: 1 A/div).

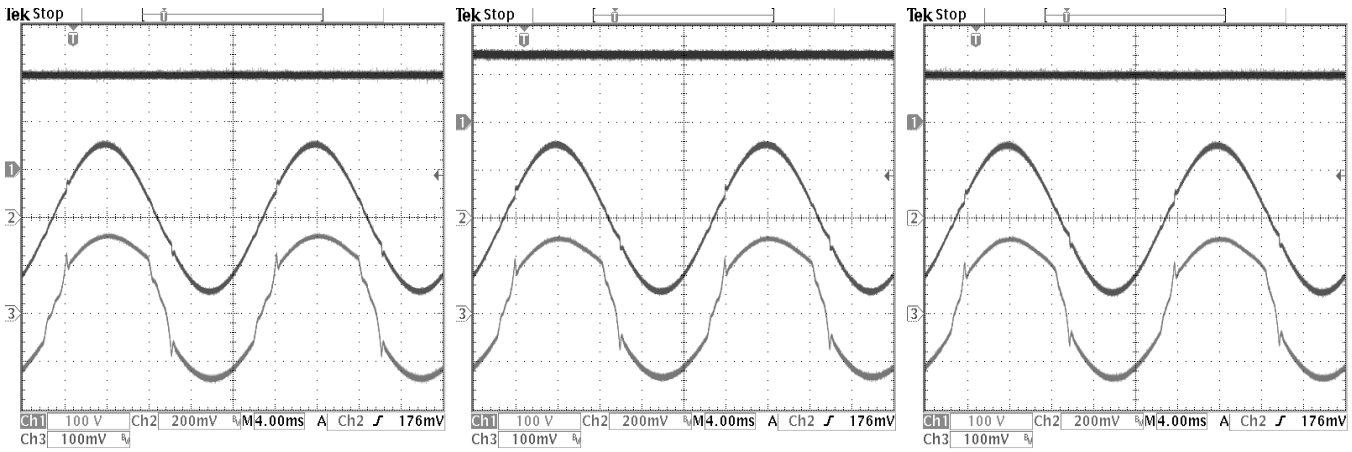

Fig. 11. The measured waveforms of Category 2 PFC regulator [Fig. 7(b)]: output voltage of pre-regulator (upper trace), input voltage (middle trace) and filtered input current (lower trace) of the regulator for different values of k_2: (a) k_2=0.25, (b) k_2=0.35, (c) k_2=0.5. (Ch1: 100 V/div, Ch2: 100 V/div, and Ch3: 1 A/div).

shows the current harmonic distortion of the PFC regulator for different k_2 conditions. Based on the measured results, the input current harmonic is independent of the value of k_2, but the overall efficiency is reduced by lower k_2.

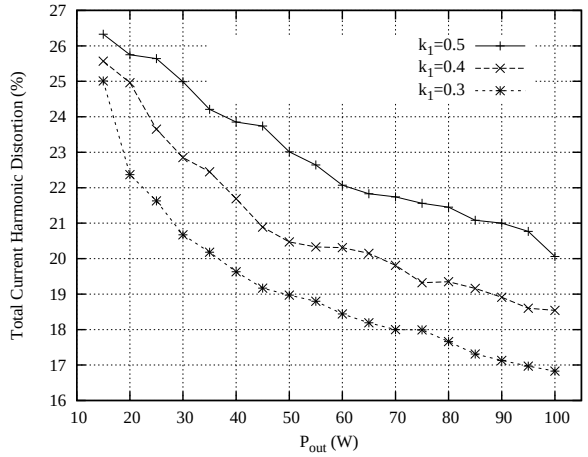

Fig. 8. The total current harmonic distortion of Category 1 PFC regulator [Fig. 7(a)] for different values of k_1.

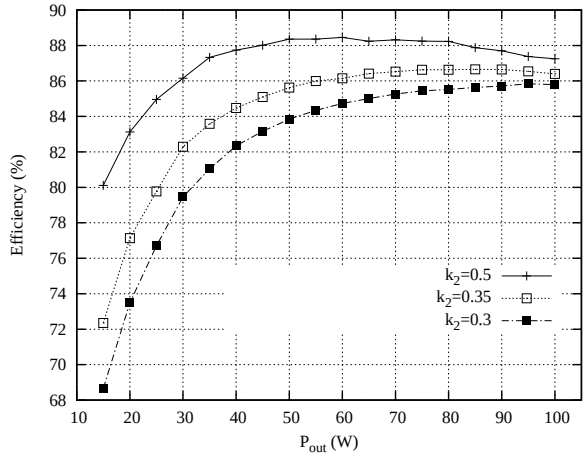

Fig. 12. The overall efficiency of Category 2 PFC regulator [Fig. 7(b)] for k_2 equal to 0.25, 0.35, and 0.5, respectively.

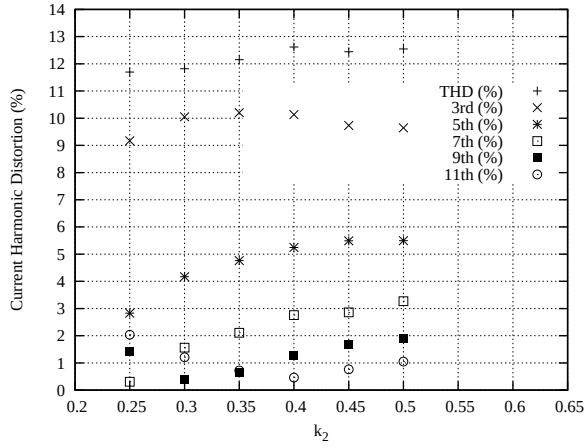

Fig. 13. The measured current harmonic distortion of Category 2 PFC regulator [Fig. 7(b)] for different values of k_2.

VI. Conclusion

In view of the large number of PFC switching regulators reported recently, we have presented a systematic study of their characteristics with an aim to understanding the various design tradeoff possibilities. In this paper we focus on those PFC switching regulators having a non-cascading structure, i.e., the pre-regulator and the post voltage regulator are not connected in cascade. Efficiency is generally improved, but often at a price. Here, we have considered the relationship between the type of structure and the possible tradeoff it offers to engineers. Specifically we have considered efficiency, power factor and load transient response, and described how different structures affect the optimization of the different performance areas. Basically we have used the power flow diagram as a tool for analyzing the non-cascading switching regulators and their performance tradeoffs. Three categories of structures are considered here. Some simulation and experimental results are shown to illustrate the basic phenomena.

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References

[1] European Standard EN 61000-3-2 Ed. 2:2001. Electromagnetic Compatibility (EMC), Part 3. Section 2. Limits for Harmonic Current Emission (Equipment Input up to and Including 16 A Per-Phase).

[2] IEEE Industry Applications Society/Power Enginnering Society. IEEE Std 519-1992 IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Sytem. Revision of IEEE Std 519-1992. Recognized as an American National Standard (ANSI).

[3] C. K. Tse, "Circuit Theory of Power Factor Correction in Switching Converters," in *Int. J. of Circuit Theory and Applications*, Vol. 31, No. 2, pp. 157-198, 2003.

[4] M. H. Kheraluwala, R. L. Steigerwald, and R. Gurumoorthy, "A Fast-Response High Power Factor Converter with a Single Power Stage," in *IEEE PESC Rec.*, pp. 769-779, 1991.

[5] M. H. L. Chow, C. K. Tse, and Y. S. Lee, "An Efficient PFC Voltage Regulator with Reduced Redundant Power Processing,"in *IEEE PESC Rec.*, pp. 87-92, 1999.

[6] J. L. Lin, M. Z. Chang, and S. P. Yang, "Synthesis and Analysis for a Novel Single-Stage Isolated High Power Factor Correction Converter," in *IEEE Trans. Circuits Syst. I*, Vol. 52, pp.1928-1939, September 2005.

[7] H. Wei and I. Bataresh, "Comparison of Basic Converter Topologies for Power Factor Correction," in *IEEE Southeastcon 98 Proceedings,*, pp. 348-353, April 1998.

[8] D. C. Martins, F. D. S. Campos, and I. Barbi, "Zeta Converter with High Power Factor Operating in Continuous Conduction Mode," in *IEEE IECON Rec.*, Vol. 3, pp. 1802-1807, 1996.

[9] Y. Jiang, F. C. Lee, G. Hua, and W. Tang, "A Novel Single-Phase Power Factor Correction Scheme," in *Proc. IEEE APEC*, pp. 287-292, 1993.

[10] O. García, J. A. Cobos, R. Prieto, J. Uceda, and S. Ollero, "A New Family of Single Stage AC/DC Power Factor Correction Converters with Fast Output Voltage Regulation," in *IEEE PESC Rec.*, pp. 536-542, 1997.

[11] M. Madigan, R. Erickson, and E. Ismail, "Integrated High Quality Rectifier-Regulators," in *IEEE Trans. Industrial Electronics*, Vol. 46, No. 4 pp. 749-758, 1999.

[12] J. Sebastián, P. Villegas, M. M. Hernando, and S. Ollero, "Improving Dynamic Response of Power Factor Correctors by Using Series-Switching Post-Regulator," in *Proc. IEEE APEC*, pp. 441-446 1998.

[13] J. Sebastián, P. J. Villegas, F. Nuño, O. García, and J. Arau, "Improving Dynamic Response of Power-Factor Preregulators by Using Two-Input High-Efficient Postregulators," in *IEEE Trans. Power Electron.*, Vol. 12, No. 6, November 1997.

[14] S. Luo, W. Qiu, W. Wu, and I. Batarseh, "Flyboost Power Factor Correction Cell and a New Family of Single-Stage AC/DC Converters," in *IEEE Trans. Power Electron.*, Vol. 20, No. 1, January 2005.

[15] R. Srinivasan and R. Oruganti, "Single-Phase Parallel Power Processing Scheme with Power Factor Control," in *Int. J. Electronics*, Vol. 80, No. 2, pp. 291-306, 1996.

[16] J. Y. Lee and M. J. Youn, "A Single-Stage Power-Factor-Correction Converter with Simple Link Voltage Suppressing Circuit (LVSC)," in *IEEE Trans. Industrial Electronics*, Vol. 48, No. 3 June 2001.

[17] S. Kim and P. N. Enjeti, "A Parallel-Connected Single Phase Power Factor Correction Approach with Improved Efficiency," in *IEEE Trans. Power Electron.*, Vol. 19, No. 1 January 2004.

[18] C. K. Tse, M. H. L. Chow, and M. K. H. Cheung, "A Family of PFC Voltage Regulator Configurations with Reduced Redundant Power Processing," in *IEEE Trans. Power Electron.*, Vol. 16, No. 6, pp. 825-830, November 2001.

[19] C. K. Tse and M. H. L. Chow, "Theoretical Study of Switching Converters with Power Factor Correction and Output Regulation," in *IEEE Trans. Circuits Syst. I*, Vol. 47, pp. 1047-1055, July 2000.

[20] A. Fernádez, J. Sebastián, P. Villegas, M. M. Hernondo, and D. G. Lamar, "Dynamic Limits a Power-Factor Preregulator," in *IEEE Trans. Industrial Electronics*, Vol. 52, No. 1, February 2005.