Shunt Active Power Filter – SIMULINK Simulation and DSP-based Hardware Realization

Che Yanbo Zhou Fudan
School of Electrical Engineering & Automation
Tianjin University, Tianjin
China
ybche@tju.edu.cn blankbei@163.com

K.W. Eric Cheng
Department of Electrical Engineering
Hong Kong Polytechnic University
Hong Kong
eeecheng@polyu.edu.hk

ABSTRACT: Active Power Filter (APF) is one of the effective means for harmonic current compensation in power grid. This paper focuses theoretical topics on a three-phase four-wire Shunt Active Power Filter (SAPF) system, covers operation principle, harmonic current detection, structure of main circuit, control of the DC voltage and compensating current. The overall system has been modeled using MATLAB/Simulink, and simulation results have shown that the structure is reasonable. Besides, the SAPF control system's hardware is realized based on DSP and MCU.

Keywords: **Shunt Active Power Filter, Harmonic Current Compensation**

Ⅰ INTRODUCTION

With the development of power electronics technology, a sharply increasing number of power electronics equipments have been widely used nowadays. Although these power electronic equipments make our life convenient, they inject much harmonic current to the power grid for their nonlinear characteristics. Active Power Filter (APF) is one of the effective means for harmonic current compensation.

A number of three-phase three-wire APF have been successfully applied in industrial products. But for three-phase four-wire APF, since the existence of neutral line, its main circuit topology and compensating current control strategy are more complex. Due to the three-phase four-wire APF compensates both harmonic current and zero-sequence current, it become a difficult issue, which is studied by many researchers, in recent years. [1]

This paper mainly studies on the three-phase four-wire SAPF system, analyses the principle, simulates the overall system. Finally, the hardware of SAPF control system is realized based on DSP and MCU.

Ⅱ SAPF THEORY ANALYSES

A. SAPF system structure and work principle

The structure of SAPF system is shown in Fig.1 and can be divided into four parts: optimal reference compensation current calculator, compensation current control, gate driver and main circuit.

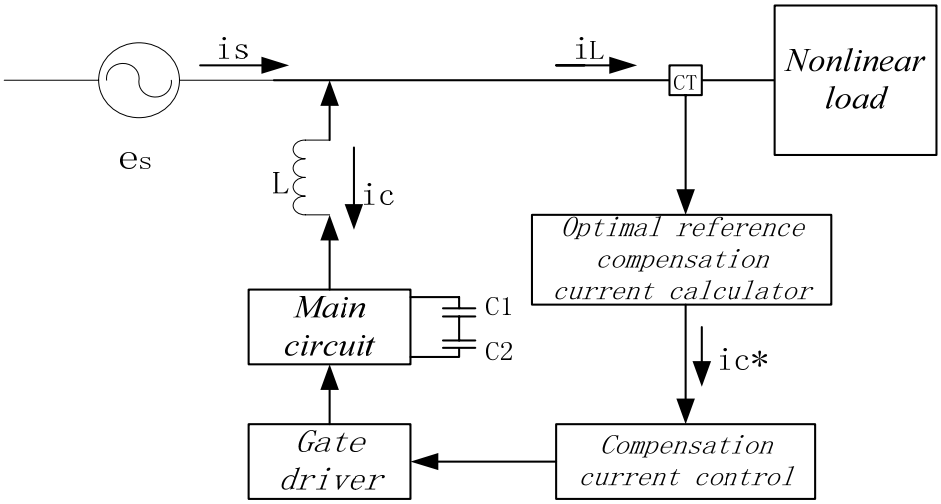

Fig.1. The structure of SAPF system

From fig.1 we get the following equation:

$$\begin{cases} i_S = i_L + i_C \\ i_L = i_f + i_h \end{cases} \quad (1)$$

Where i_S is power grid current; current i_L is load current; i_f is fundamental current. i_h is the harmonic current in i_L, current i_C is the compensating current generated by APF.

From equation (1) when the APF compensating current $i_c = -i_h$, we get that $i_S = i_f$, hence the harmonic current which is generated by nonlinear load can completely be eliminated by the APF system.

B. The main circuit structure of three-phase four-wire SAPF

The difference between the three-phase three-wire SAPF and the three-phase four-wire SAPF is that there's zero-sequence current on the neutral line of three-phase four-wire SAPF. According to the different zero-sequence current compensating method there are two main current topologies—three-leg voltage source inverter (VSI) topology [2] and four-leg VSI topology. [3] In order to reduce the cost of SAPF, the paper uses the three-leg VSI main current topology, for it needs fewer electronic elements.

The three-leg VSI main current topology studied in this paper is given in Fig.2. The DC bus uses two capacitors common to all three phases, with the center-tap connected to the line neutral. The AC side of the converter is connected to the main via by a synchronous link reactor L which is shown in Fig.2.

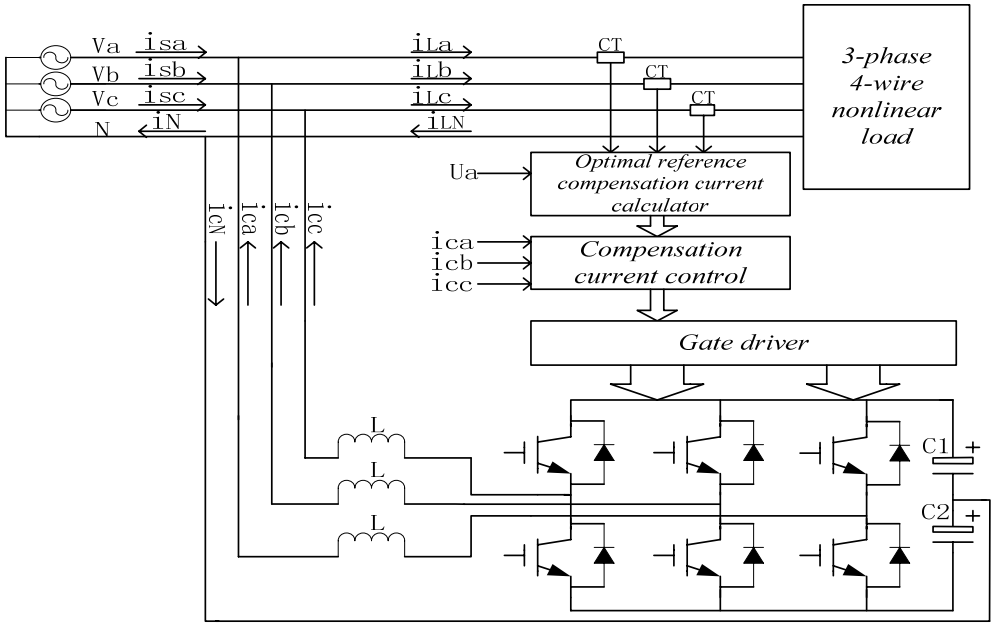

Fig.2. The three-leg VSI topology of three-phase four-wire SAPF

In Fig.2, the functions of the four parts in three-phase four-wire SAPF system are covered as following:

1) The function of optimal reference compensation current calculator is to sample the three-phase currents, which contain harmonic current, from the load side in the above system; separate zero-sequence current from three-phase currents which have been sampled. Based on the instantaneous reactive power theory [4,5] and after a series of calculations, the optimal compensation current would be got.

2) The function of compensation current control is to make sure that the actual compensation currents ic_a, ic_b, ic_c follow the optimal compensation currents ic_a*,ic_b*,ic_c*. It generates the IGBT control signal based on the value of Δic_i ($\Delta ic_i = ic_i$*- ic_i; i=a, b, c)

3) The function of gate driver is to drive the IGBT turn on or turn off according to the IGBT control signals. It is made up of IGBT drive modules and their protective circuit.

4) Main circuit contains IGBT modules, in series capacitances, filter circuit etc. Its main function is to realize the harmonic current compensation.

C. The method of harmonic current detecting

The method of harmonic current detecting is based on the instantaneous reactive power theory. Fist, separate the

zero-sequence current from three-phase currents which have been sampled, and then in order to get the optimal compensation current, a series of calculation would be carried out based on the i_p--i_q detecting method.[6] The principle of harmonic current detecting method is shown in Fig.3.

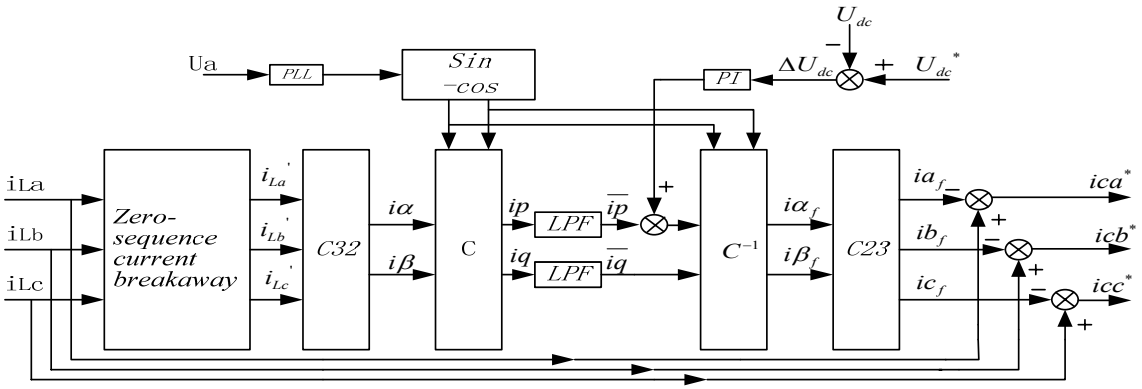

Fig.3. The principle of harmonic current detecting method

In fig.3 iLa、iLb、iLc are the load side currents which contain harmonic current. First, break the zero-sequence current away.

$$\begin{cases} i_{La}' = i_{La} - (i_{La} + i_{Lb} + i_{Lc})/3 \\ i_{Lb}' = i_{Lb} - (i_{La} + i_{Lb} + i_{Lc})/3 \\ i_{Lc}' = i_{Lc} - (i_{La} + i_{Lb} + i_{Lc})/3 \end{cases} \quad (2)$$

The three-phase currents iLa', iLb', iLc' with no zero-sequence current can be gotten.

In fig.3 definitions of C_{32}, C_{23}, C and C^{-1} are as follows

$$C = C^{-1} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ -\cos\omega t & -\sin\omega t \end{bmatrix} \quad (3)$$

$$C_{32} = \sqrt{2/3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \quad (4)$$

$$C_{32} = C_{32}^{\ T} \quad (5)$$

According to i_p--i_q detecting method the three-phase currents iLa', iLb', iLc' were done C_{32} and C transform, and through the LPF we get $\bar{i}_p$ & $\bar{i}_q$ which have been just determined by fundamental currents. And then after the C^{-1} and C_{23} transform we get the fundamental currents: ia_f, ib_f, ic_f. The optimal compensation currents ica^*, icb^*, icc^* can get from equation (6) which contains harmonic and zero-sequence compensating components.

$$\begin{cases} ica^* = i_{La} - ia_f \\ icb^* = i_{Lb} - ib_f \\ icc^* = i_{Lc} - ic_f \end{cases} \quad (6)$$

D. The control of the DC voltage and compensating current

1) The control of the DC voltage

In the system of three-phase four-wire SAPF with three-leg voltage source inverter (VSI) topology, DC voltage control should have two functions: first maintaining the DC voltage U_d at a certain value to satisfy the demand of compensating currents tracking capacity; second making balance of the voltage between C1 and C2.

In order to control the voltage of U_d, we add DC voltage feedback control loop to the harmonic current detecting circuit as shown in Fig.3. $\Delta U = U_d^* - U_d$, ΔU is modulated by PI adjustor and then add up to current i_p. Hence there's an additional fundamental current in the compensating current. The additional fundamental current can control the energy exchange between the power grid and SAPF system, so that the DC voltage can be maintained at a certain value.

In the balance control of C1 and C2 voltages, first detect their voltages separately, according to the difference we add zero-sequence compensating current to the optimal compensation current to balance the voltage on C1 and C2.

2) The control of the compensating current

In this system we use hysteresis comparison as the

compensating current control method. Let Δic_i ($\Delta ic_i = ic_i^* - ic_i$; i=a, b, c) go through the hysteresis comparator, according to the comparing results turn on or turn off IGBT. By doing so we can make the actual compensation currents ic_a, ic_b, ic_c follow the optimal compensation currents ic_a^*, ic_b^*, ic_c^*.

III. SAPF SYSTEM'S SIMULATION WITH MATLAB/SIMULINK

A. Simulation building

The simulation construction of three-phase four-wire SAPF system with matlab\simulink is shown as Fig.4. Unbalanced nonlinear load contains a three-phase rectifier and a one-phase rectifier. Main circuit uses voltage source inverters，and when simulating we use ideal switches instead of real semiconductor switches. DC capacitor value: C1=C2=0.1F, three-phase AC inductances: $L_A=L_B=L_c=0.005H$

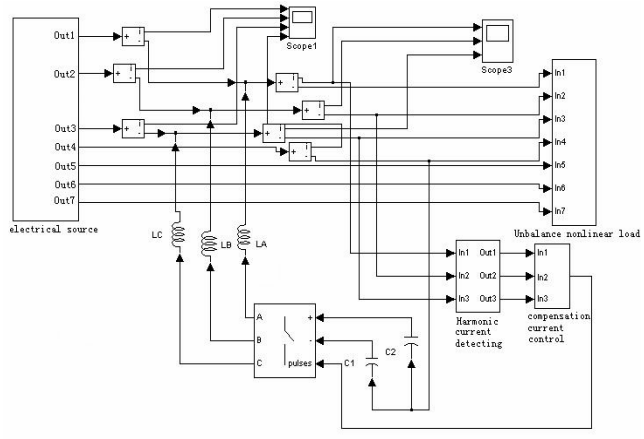

Fig.4. SAPF system simulation construction

In Fig.5 harmonic current detecting module is built according to the principle of harmonic current detecting method.

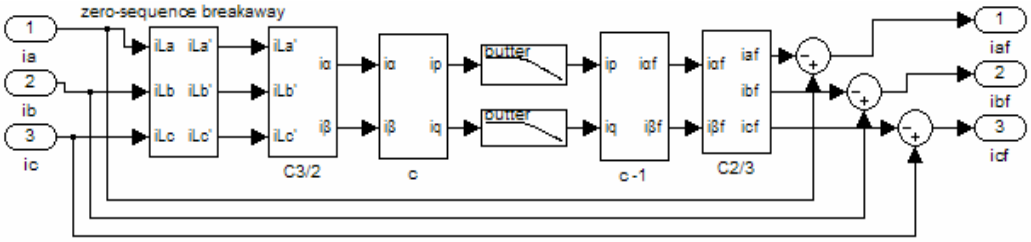

Fig5. Harmonic current detecting module

In Fig.6 compensating current control module is built based on the hysteresis comparison current tracing control method. The part of IGBT gate driver is not considered in the simulation. Three pairs of driving signals 1-2, 3-4, 5-6 separately control a, b, c phase of three-phase rectifier. In order to prevent the two switches of one leg turn on at the same time, the pass band width of the two hysteresis comparators in one leg is set in different value, so that there's a dead time when the two switches alternately turn on.

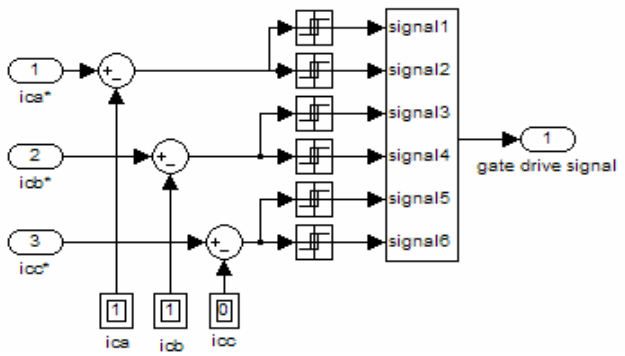

Fig6. Compensating current control module

Simulation parameters set up:

Stop time t=0.06s; Solver options: Variable-step, Besides,stiff/TR-BDF2]. The currents before compensating are shown in Fig.7. Harmonic currents detecting are shown in Fig.8 The currents after compensating are shown in Fig.9.

B. Simulation results analysis

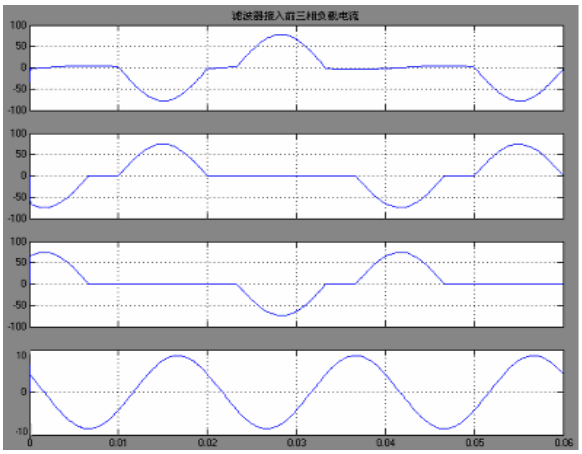

Fig.7. Currents before compensating

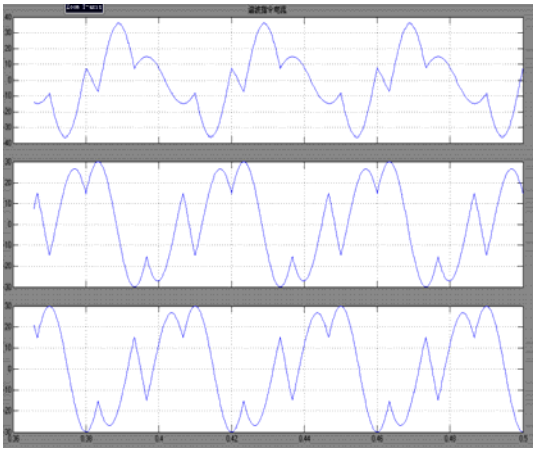

Fig.8. Harmonic currents detecting

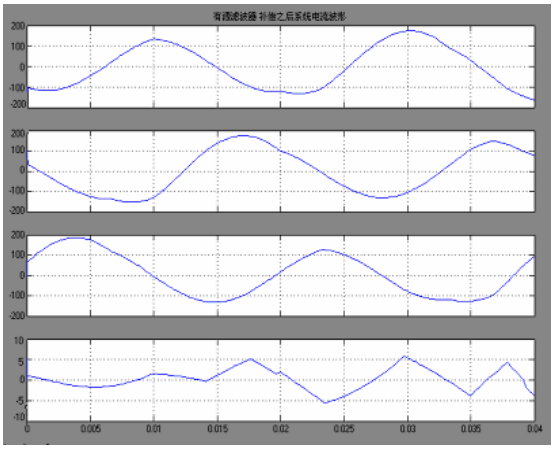

Fig.9. Currents after compensating

Simulation waveforms shown in fig.7 to fig.9 indicate that the three-phase four-wire SAPF can not only effectively eliminate the harmonic currents in power grid which is caused by unbalanced nonlinear load, but restrain the neutral current as well.

IV. SAPF SYSTEM'S HARDWARE ACTUALIZE

Fig.10 shows the three-phase four-wire SAPF control system's hardware actualized based on DSP and MCU.

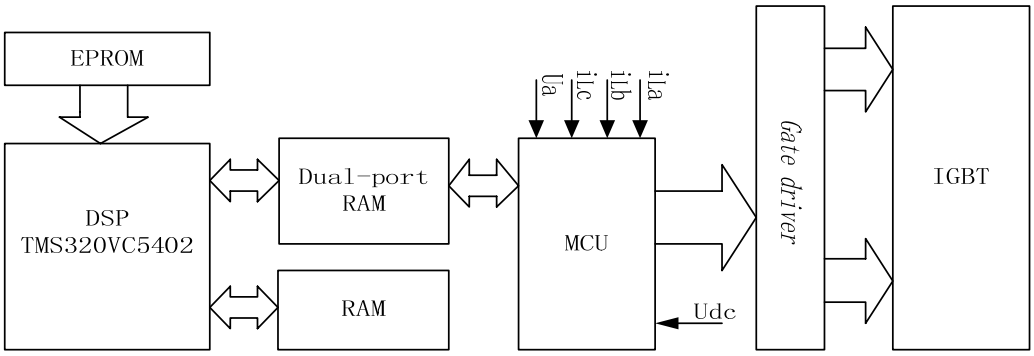

Fig.10. SAPF control system's hardware actualize based on DSP and MCU

The main control processor of SAPF contains a TMS320c5402 DSP, which is produced by TI company, and a Mitsubishi MCU. They exchange data through the dual-port RAM. DSP has an external EPROM for user's programs because TMS320c5402 has no available internal ROM for its users. Also DSP has a RAM expansion.

In SAPF control system the MCU is in charge of sampling currents, A/D converting and output PWM wave, according to the fundamental currents data. DSP is in charge of computing the fundamental currents, according to the sampled currents, including 3/2 transforming, C transforming and LPF etc. Dual-port RAM is in charge of the exchange of data between DSP and MCU.

MCU converts the sampled currents which are analog signals into digital signals by its internal A/D converter. Then it writes the digital data into dual-port RAM and changes the state of the BIO port on DSP. DSP reads the date in dual-port RAM written by MCU according to the state of BIO port. Through a series of computations the fundamental currents data is finally returned to the dual-port RAM. MCU gets the fundamental currents data from dual-port RAM and outputs PWM signals to generate compensating currents.

V. CONCLUSION

Simulation results show that the 3-phase 4-wire SAPF system in this structure can effectively reduce the undesired effect of the harmonic current to the power grid, thus, that structure is proved to be reasonable. DSP and MCU have powerful computing speed, the realized control system hardware based on DSP and MCU has a rapid and good capability on harmonic currents compensation to meet the SAPF system's requirements.

VI. REFERENCES

[1] Mauricio Aredes and Edson H.Watanabel, 'New Control Algorithms For Series And Shunt Three-phase Four-wire Active Power Filters' IEEE Trans. on Power Delivery, Vol. 10, No. 3, pp. 1649-1656, July 1995.

[2] Kdvork Haddad, Thierry Thomas, GCza JoOs, Alain Jaafari 'Dynamic Performance Of Three Phase Four Wire Active Filters', in Conf. Rec. IEEE/APEC, pp. 206-212, 1997.

[3] C.B Jacobinal, R.F. Pinheiro, M.B. de R. Correa1, A.M.N. Limal and E.R.C. da Silval 'Control of a three-phase four-wire active filter operating with an open phase' in Conf. Rec. IEEE/IAS, pp. 561-568, 2001.

[4] H. Akagi, Y. Kanazawa, and A. Nabae, 'Generalized Theory of the Instantaneous Reactive Power in Three-phase Circuits', in Conf. Rec. IEEE/APEC, pp. 1375-1386, 1983.

[5] H. Akagi, Y. Kanazawa, and A. Nabae, 'Instantaneous Reactive Power Compensators Comprising Switching Devices Without Energy Storage Components' IEEE Trans. on IA, Vol. IA-20, No. 3, pp. 625-630, May 1984.

[6] Zhou Lin, Shen Xiaoli 'Active power filter based on ip-iq detecting method and One-cycle control' in Conf. Rec. IEEE/IES, pp.564-569, 2004.