The Control of Switching dc-dc Converters—A General LQR Problem

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Abstract—**The control of switching dc-dc converters is reviewed. Regarding it as a general linear quadratic regulator (LQR) problem, an innovative optimal and robust digital controller is proposed. The control strategy adopted can achieve good regulation, rejection of modest disturbances, and more significantly, the ability to cater to switching converters with RHP zeroes. This controller design is a general approach that is applicable to all PWM-type dc-dc converters with their circuit topologies known or unknown. Modern CAD techniques are used to reach the final control law. Application to a published Ćuk converter is illustrated as an example, and the performance evaluation is given.**

I. Introduction

SINCE the past two decades, switch-mode power regulators have been developed into lightweight, highly efficient dc power sources, and the switching dc-dc converters have raised an upsurge of research interest in the area of their modeling, analysis, and the search of an optimal topology. Among the various types of dc-dc converters, the pulse-width modulated (PWM) ones constitute by far the largest group and will be considered in this paper.

Despite the great effort delivered to the researches on switch-mode power supplies, the control aspect of dc-dc converters has received intensive investigation only in recent years. There are two main reasons: First, the problem of control usually requires good modeling and analysis for the converters, and time is needed to let this research reach maturity; second, the wide range of circuit topologies of switching converters makes the problem of control, using conventional design, complicated and somewhat topology dependent. In particular, the problem will become more difficult when the switching converters have open-loop zeroes in the right-hand side of the s plane (i.e., the converters are nonminimum phase plants).

This paper aims to tackle the problem of controlling PWM-type switching dc-dc converters with emphasis on generality. A general approach to designing digital controllers for switching converters, independent of circuit topologies and locations of their open-loop poles and zeroes, will be proposed. Based on this approach, one even need not know the actual circuits or their ways of operation. The problem will be considered systematically from the control engineering point of view. Thanks to the techniques of state feedback and the theory of linear quadratic optimal regulator (LQR), the controller proposed will result in a switching regulator with good dynamic response, rejection to modest disturbances, and robustness.

In Section II, a review of some previously published work and the inadequacies on the control of switching dc-dc converters will be given. In Section III, the problem of control will be defined clearly, and the proposed design procedure of the controller will be given. The proposed control algorithm will be elaborated upon in Section IV. In Section V, an application example for a published Ćuk converter, which may have RHP zeroes, will be illustrated, and simulation results will be presented.

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II. Review

Investigations of basic switching converters commenced in the mid-1960's. Over the next two decades, Middlebrook and Ćuk made significant contributions on modeling, analysis, and generalization of the basic topologies [1] [2], developments on the Ćuk converter [3], and research on integrated magnetics [4]. With the maturity in modeling and analysis, the control of switching regulators began to motivate many studies. Contributions were made by Chetty [5] and Thau [6] on the design of analog controllers to improve the transient response of some particular converters. Peracaula *et al.* [7] suggested the use of digital controllers and gave a performance comparison with the analog alternatives. A three-term controller was proposed by Daly and Tymerski [8]. In the mid-1980's, two significant advancements in the closed-loop control of switching power converters were consolidated by the improvements on regulations and dynamic responses. They are, namely, the voltage-feedforward control and the current-mode (or current-programmed) control [9]. In 1989, compensation using an analog-amplitude, discrete-time recursive filter was proposed [15].

Despite the many publications on the control of the switching converters, the studies were limited to certain specific topologies from which a proper model (represented by differential equations, transfer functions, state equations, or whatever) could be found. These previous design approaches suffer from one or more of the following weaknesses:

1) The models always involve complicated mathematical expressions, and different topologies of switching converters will have different model representations. Thus, the modeling of the switching converter concerned becomes a specific, complicated, and time-consuming task, which has to be performed prior to designing the controller.
2) The common control methods rely very much on accurate modeling of dc-dc converters. However, the parameters of the converter models will vary due to many factors, and the sensitivity of the controller to parameter changes of the model is an important factor for consideration. In particular, the problem of sensitivity to the possible migration of open-loop zeroes from the left-half s plane (LHP) to the right-half s plane (RHP) is generally not adequately addressed.

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3) Most of the controllers published were analog controllers that would be implemented using active filters and other analog components. The lack of flexibility, the complexity, and the cost of the controller will become significant problems when complicated control laws are implemented.

In view of these weaknesses, this paper proposes a systematic and general duty-ratio control approach to PWM-type switching dc-dc converters that is independent of their circuit topologies. Special attention is delivered to situations when the switching converters have open-loop zeroes in the RHP. The theory of LQ optimal control provides a means to achieve improved transient response, robustness to topology changes, parameter variations, or modeling errors in the converter. Nowadays, with the availability of fast DSP chips, it becomes possible to implement a digital controller for a switching converter that has the advantages of cost effectiveness, flexibility, and simplicity on implementation.

III. Design Consideration

A. Problem Definition

A switching dc-dc converter can be regarded as a multiple-input single-output (MISO) plant [6]. The output is the output voltage V_o of the switching regulator. The control input is the signal represented by the PWM duty ratio D, where D is defined as the ratio of the power switch ON time to the switching period ($D \equiv T_{ON}/T_s$). The converter parameters are affected by the input line voltage V_{in} and output load R_L, which in conjunction with other minor variations such as EMI and stray effects, constitute the external disturbance inputs to the system. The steady-state values of D, V_o, V_{in}, and R_L constitute the operating point of the switching converter. As far as control is concerned, switching converters can be regarded as highly nonlinear plants. Nonlinearities can be classified into three groups: 1) topology changes due to, perhaps, high temperature or component failure, 2) nonlinear characteristics of the electronic switches (fast dynamics), and 3) nonlinear plant parameter variations due to external disturbances (slow dynamics). To cater to these nonlinearities, two approaches can be adopted.

Approach 1: Use an approximate linearized model to average out the effects of fast dynamics. This linearized model is usually accurate enough within the bandwidth of interest. However, owing to nonlinearities 1) and 3) mentioned above, the following assumptions have to be made:

1) The switching regulator has only one operating point.
2) The variations in line voltage and load current are infrequent and small enough to be tackled.
3) Other disturbances or the effects of topology changes are small and lie within the sensitivity tolerance of the controller (i.e., the controller is adequately robust).

Approach 2: Design a high-quality adaptive controller that is capable of adapting significant nonlinearities as well as catering to multioperating point situations.

Comparing the above two approaches, *Approach 1* is obviously less general. The area of application using *Approach 1* is narrower due to the constraints that validities of assumptions 1) to 3) have to be assured. *Approach 2*,on the other hand, is more general, but the design and implementation of such a controller requires a more advanced control theory, which is not as mature as *Approach 1*. A tradeoff has to be done between these two approaches. In practice, *Approach 1* is found to be sufficient in many cases, and we limit the scope of this paper by considering *Approach 1* only.

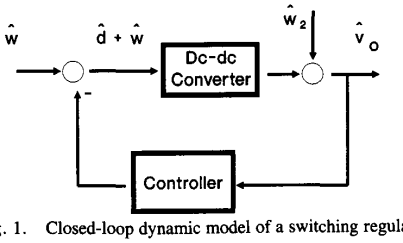


Fig. 1. Closed-loop dynamic model of a switching regulator.

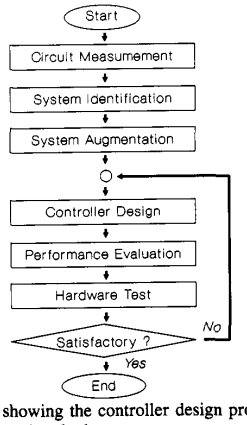


Fig. 2. Flow diagram showing the controller design procedure for switching dc-dc converters.

Under *Approach 1*, a linearized ac small-signal model has to be considered. The converter can be represented by the block diagram shown in Fig. 1, where the '^' sign is used to represent small ac variations about the steady-state operating point. Based on the linearized small-signal model, a controller will be designed to close the loop. "Small signal" is emphasized here, meaning that the highly nonlinear plant switching converter is modeled as a linear system working around its operating point. Perturbations to the system are assumed to be small signals such that the linearization can still be a valid approximation and will not affect overall system stability. Perturbations to the systems are modeled as the disturbance inputs $\hat{\omega}$ and $\hat{\omega}_2$ in the input and output sides of the plant, respectively. The controller is designed to drive the output $\hat{v}_o$ to zero in the presence of these perturbations with good transient dynamics. Due to the inevitable external disturbances and unmeasured factors (such as topology changes or modeling errors) mentioned previously, the controller must be robust enough to handle variations in the plant parameters.

B. Design Procedure

The proposed design procedure can be represented by the flow diagram shown in Fig. 2. The first phase of circuit measurement shown is used to provide data for the second phase of system identification, and either actual data from hardware or simulated data from a circuit analysis package may be used. In this way, the dc-dc converter can be regarded as a black box, and only the open-loop control-to-output response data, but no other information, are necessary for modeling the plant. As discussed in Section II-A, since a small signal linearized model is assumed, the input data to this identification scheme ought to have small amplitude. Because of the nonlinearities, a large input amplitude will give different coefficients of the model, but this model is no longer a small signal linearized model.

After the second phase of system identification, an open-loop control-to-output transfer function is obtained. The system is then augmented to suit the controller design. Much work on small signal linearization and large signal control has been published [18], [19]. In this paper, with concerns about the nonlinearities, the controller design is regarded as a general LQR problem. The details of these phases will be elaborated upon in Section IV. After the controller has been designed, its performance may be evaluated first by software simulation and then by actual hardware implementation. Whenever necessary, further fine adjustments to the controller parameters are introduced.

It can be seen that the whole design procedure is a general procedure independent of the topologies of switching converters. With the sophisticated computing power available today, it is possible to merge the first five phases shown in Fig. 2 into a standalone automatic CAD package.

IV. Optimal Controller Design

A. Observer-Controller Compensator

The switching dc-dc converter open-loop plant can readily be represented by the linearized state-space model

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}(\hat{d} + \hat{\omega}) \tag{1}$$

$$\hat{v}_o = \boldsymbol{C}\boldsymbol{x} + D(\hat{d} + \hat{\omega}) + \hat{\omega}_2. \tag{2}$$

As far as a digital controller is concerned, the plant can be modelled by its discrete-time representation

$$\boldsymbol{x}(k+1) = \boldsymbol{\Phi}\boldsymbol{x}(k) + \boldsymbol{\Gamma}(\hat{d}(k) + \hat{\omega}(k)) \tag{3}$$

$$\hat{v}_o(k) = \boldsymbol{C}\boldsymbol{x}(k) + D(\hat{d}(k) + \hat{\omega}(k)) + \hat{\omega}_2 \tag{4}$$

where $\boldsymbol{x}$ represents the state vector of the linearized nth-order system, $\hat{d}$, $\hat{v}_o$, $\hat{\omega}$, and $\hat{\omega}_2$ are scalar quantities representing the perturbed duty cycle, perturbed output voltage, input disturbance, and output disturbance, respectively. The scalar D accounts for the possible link between input and output, e.g., the effects caused by parasitics of the energy storage components [16]. For the sake of generality and the fact that not all states of the plant are easily measurable, an observer-controller compensator is suggested [10], assuming that the plant is controllable and observable. The asymptotic state observer can be represented by the following expression:

$$\hat{\boldsymbol{x}}(k+1) = \boldsymbol{\Phi}\hat{\boldsymbol{x}}(k) + \boldsymbol{\Gamma}\hat{d}(k) + \boldsymbol{L}(\hat{v}_o(k) - \boldsymbol{C}\hat{\boldsymbol{x}}(k)) \tag{5}$$

where $\hat{\boldsymbol{x}}$ denotes the observed state variables. The block diagram of the observer-controller compensator is given in Fig. 3. The design involves the determination of the gain vector $\boldsymbol{L}$ of the observer and the feedback gain vector $\boldsymbol{k}^T$ of the controller.

B. Disturbances and Integral Feedback

As mentioned in Section III-A, the switching dc-dc converter is inevitably subjected to perturbations for a lot of reasons. As long as the disturbances are sustained and slowly varying ones (i.e., $\hat{\omega}(k+1) \approx \hat{\omega}(k)$), the inclusion of a feedback path containing an integration can be used so that the closed-loop steady-state error is zero. To implement the integral feedback, the system represented by (3) and (4) has to be augmented to a new system as followed:

$$\boldsymbol{x}_1(k+1) = \boldsymbol{\Phi}_1\boldsymbol{x}_1(k) + \boldsymbol{\Gamma}_1 u_1(k) \tag{6}$$

$$\hat{v}_o(k) = [\boldsymbol{C} \quad D]\,\boldsymbol{x}_1(k) \tag{7}$$

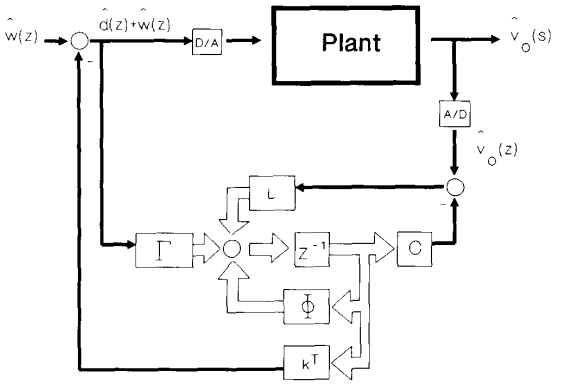


Fig. 3. Observer-controller compensator for switching dc-dc converter.

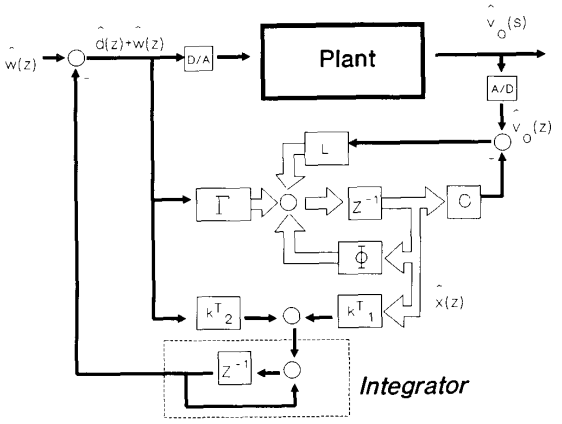


Fig. 4. Final control scheme for a dc-dc converter.

where

$$\boldsymbol{x}_1(k) = \begin{bmatrix} \boldsymbol{x}(k) \\ \hat{d}(k) + \hat{\omega}(k) \end{bmatrix}$$

$$u_1(k) = \hat{d}(k+1) - \hat{d}(k)$$

$$\boldsymbol{\Phi}_1 = \begin{bmatrix} \boldsymbol{\Phi} & \boldsymbol{\Gamma} \\ \boldsymbol{0} & 1 \end{bmatrix}, \qquad \boldsymbol{\Gamma}_1 = \begin{bmatrix} \boldsymbol{0} \\ 1 \end{bmatrix}.$$

Here, it is assumed that the effects of all disturbance inputs will cause the state variables to deviate from the desired operating point, and the controller output will bring the perturbed states back to its equilibrium condition. Rejection of disturbances is related to the robustness of the controller. However, as far as the controller design is concerned, all these disturbance inputs do not contribute to a direct effect (thus, $\hat{\omega}_2$ does not appear in (6) and (7)). A complete control scheme with the addition of integral feedback is shown in Fig. 4. Notice that the feedback gain vector $\boldsymbol{k}^T$ is now replaced by $\boldsymbol{k}_1^T$ and $\boldsymbol{k}_2^T$.

C. Linear Optimal Control

By state-feedback techniques, the closed-loop poles can be allocated to any position. However, perturbations in input voltage and load current, modeling errors, and many other factors constitute the variations of system parameters. In view of these parameter variations, a simple pole-allocation method using state-feedback techniques will usually lead to unsatisfactory system performance.

To guarantee that the regulator have good closed-loop behavior and to be relatively insensitive to system parameter variations and/or external disturbances (which implies good line and load regulations), the controller feedback gain vector has to be determined optimally. The key to optimality is the choice of an appropriate performance index. By linear optimal control theory, the closed-loop poles can be assigned such that the dominant poles are close to the desired locations and that the remaining poles be nondominant, i.e., far from the origin of the s plane and in a Butterworth pattern. Such an optimal controller provides a guaranteed reduction in sensitivity to plant parameter variations when compared with an equivalent open-loop system [11]. In this problem, a suitable quadratic performance index for the digital controller can be determined using the design steps of the following algorithm (adapted from [12], [13], [17]).

Algorithm 1:

Step 1) Form a polynomial $m(z)$ such that it has the desired dominant poles p_i as its roots:

$$m(z) = \prod_{i=1}^{n'} (z - p_i) \tag{8}$$

where n' is the number of dominant poles.

Step 2) Solve for the vector $\boldsymbol{d}$ according to:

$$\boldsymbol{d}'(zI - \boldsymbol{\Phi})\boldsymbol{\Gamma} = m(z)/\det(zI - \boldsymbol{\Phi}) \tag{9}$$

$$\boldsymbol{Q} = \boldsymbol{d}\boldsymbol{d}'. \tag{10}$$

Step 3) Check that $[\boldsymbol{\Phi}, \boldsymbol{d}]$ is completely observable.

Step 4) Define the performance index

$$J = \sum_{k=0}^{\infty} \left(u_1(k)^2\sigma + \boldsymbol{x}_1(k)'\boldsymbol{Q}_1\boldsymbol{x}_1(k)\right) \tag{11}$$

where

$$\boldsymbol{Q}_1 = \begin{bmatrix} \boldsymbol{Q} & \boldsymbol{0} \\ \boldsymbol{0} & R \end{bmatrix} \tag{12}$$

and where $\boldsymbol{Q}$ is symmetric, nonnegative definite and of order n (order of the open-loop unaugmented system). R and σ are positive scalars. R is chosen to be sufficiently small so that it gives a more significant weight to the state error weighing matrix $\boldsymbol{Q}$. σ is chosen to be between the value of R and the largest eigenvalue of $\boldsymbol{Q}$.

Step 5) Determine the optimal feedback gain vector

$$\boldsymbol{k}^{\mathrm{T}} = \begin{bmatrix} \boldsymbol{k}_1^T & \boldsymbol{k}_2^T \end{bmatrix}. \tag{13}$$

Using the CAD tools, this design methodology promises to be a simple task.

D. Plant with RHP Zeroes

For a system with all zeroes in the LHP of the s plane, the quadratic performance index can be determined with dominant poles close to the zeroes of the system. However, when the zeroes are in the RHP of the s plane or outside the unit circle in the z plane (this is quite common for some kinds of dc-dc converters), the dominant poles cannot be chosen to be close to the "unstable" zeroes. Our approach to cater to this situation is as follows

Algorithm 2

For any RHP zero $s_i = \sigma_i + j\omega_i$ in the s plane, choose the corresponding dominant pole to be located near the position $s = -\sigma_i + j\omega_i$. Correspondingly, when discrete-time domain is considered, for any "unstable" zero z_i in the z plane, choose the corresponding dominant pole to be located near the position $z = 1/z_i$. If necessary, modify the location of the dominant pole to make it sufficiently far from the stability boundary.

TABLE I
COMPARISON OF DIFFERENT COMBINATIONS OF CONTROLLER AND OBSERVER ALGORITHMS FOR PLANT WITH POSSIBLE MIGRATIONS OF ZEROES FROM LHP TO RHP AND VICE VERSA

Choice	Algorithm for Designing $\boldsymbol{k}^T$	Algorithm for Designing $\boldsymbol{L}$	Performance
1	LH	LH	Very poor
2	LH	RH	Satisfactory
3	RH	LH	Poor
4	RH	RH	Satisfactory

Table I. Leung et al, IE-38, Feb 1991

Special attention has to be paid to the situations in which the perturbations to the system will cause the system zeroes to drift from the LHP to RHP and vice versa. In this case, as far as the controller design is concerned, two factors have to be considered: 1) The model for designing the feedback gain vector $\boldsymbol{k}^T$ may be invalid; 2) the model for designing the observer gain vector $\boldsymbol{L}$ may be invalid. The control scheme has to be determined by considering different combinations of the above two factors. This can be summarized in Table I.

In Table I, LH and RH refer to the algorithm that assumes that the system zeroes are in the LHP and RHP, respectively (therefore, RH in the second column corresponds to *Algorithm 2* stated above). Investigations on these combinations give the results shown in Table I, which can be explained as follows:

1) When the locations of zeroes are actually in the RHP, both algorithms for determining $\boldsymbol{k}^T$ and $\boldsymbol{L}$ refer to invalid models in Choice 1, and the closed-loop system performance becomes very poor, whereas in the other choices, at least one model is valid, resulting in a better performance.
2) Among Choices 2, 3, and 4, Choice 3 gives a poorer response and stability margin. This shows that the invalidity of the model for observer gain design plays a major role for performance degradation.
3) Both Choices 2 and 4 give satisfactory results. Choice 2 gives a better performance when the system zeroes are more often in the LHP. When the zeroes are more often in the RHP, Choice 4 is better. The final choice somewhat depends on how frequent the zeroes may be in the RHP.

The next section gives an example to illustrate this control scheme.

V. APPLICATION EXAMPLE

In this section, a dc-dc converter topology will be chosen as the plant to illustrate how the design methodology discussed in the Section IV can be carried out. This plant is a published Ćuk converter circuit by Middlebrook [14] and has a topology that is shown in Fig. 5. The advantage of using a published plant is that the intermediate results can be compared and checked with the published results as a reference. In addition, this circuit has the interesting property that under the desired operating point, the system will have two complex zeroes in the LHP,[1] but when the operating condition alters due to load changes, the zeroes may shift to the RHP. The design procedure has been summarized in Fig. 2. The materials discussed hereafter are the procedures

[1]More generally, it has 4 zeroes if scalar D in equ. (7) is not equal to 0

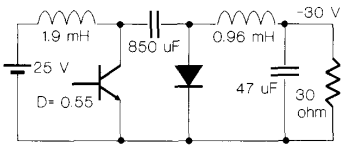
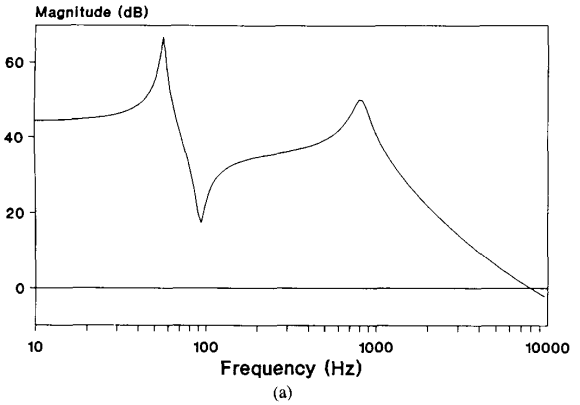
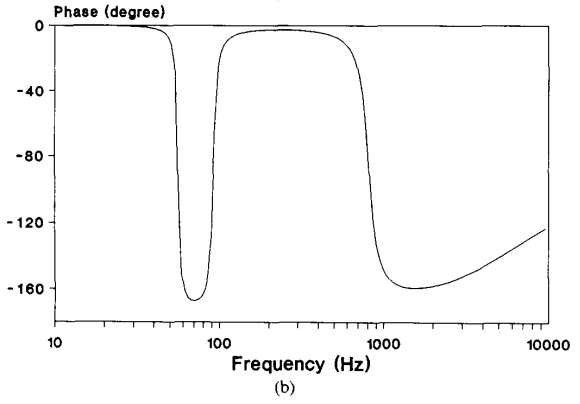


Fig. 5. 30-V, 1-A Ćuk converter circuit.



(a)



(b)

Fig. 6. Bode diagram for the open-loop control-to-output transfer function ($\hat{v}_o/\hat{d}$) of the 30-V, 1-A Ćuk converter.

adopted after the open-loop control-to-output transfer function of the Ćuk converter has been obtained.

The identified open-loop system has frequency and phase response, as is shown in Fig. 6. Notice that besides the two complex zeroes, one more zero is identified, and it is located in the high-frequency region. However, within the bandwidth concerned, this zero does not contribute a significant effect. Under the criterion that the sampling time is at least 10 times smaller than the effective time constant of the system, a sampling frequency of 10 kHz is selected. The control-to-output transfer function found can then be transformed into the following discrete-time state equation:

$$x(k+1) = \begin{bmatrix} 3.6662 & -5.2431 & 3.4865 & -0.9099 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} x(k) + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{d}(k) \tag{14}$$

$$\hat{v}_o(k) = \begin{bmatrix} 10.9239 & -18.1095 & 3.5938 & 3.6405 \end{bmatrix} x(k). \tag{15}$$

It is found that when the load changes from 30 to 32 Ω or higher, two zeroes will shift outside the unit circle in the z plane. The specifications assume a load variation from 25 to 34 Ω and input voltage variations from 21 to 29 V. Due to the significant shifts of zeroes, a compromise is adopted in that the controller is designed based on the model with $R_L = 30$ Ω, but for the observer, the model with $R_L = 34$ Ω is used (Choice 2 of Table I). The model with $R_L = 34$ Ω is given by

$$x(k+1) = \begin{bmatrix} 3.6336 & -5.1196 & 3.3375 & -0.8517 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} x(k) + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{d}(k) \tag{16}$$

$$\hat{v}_o(k) = \begin{bmatrix} 13.0378 & -27.8917 & 16.4579 & -1.5617 \end{bmatrix} x(k). \tag{17}$$

The design involves the determinations of the feedback gain vector $\boldsymbol{k}^T$ and the observer gain vector $\boldsymbol{L}$. The eigenvalues of the observer are chosen to correspond to 1500, 2500, 3500, and 4500 rad/s in the s domain. Three dominant poles of the closed-loop system are chosen in such a way that two complex poles are close to the two complex zeroes in the s plane, and one dominant real pole is around 1000 Hz in the frequency domain (*Algorithm 1*). Based on the discussion of Section IV-C, the performance index can be determined:

$$J = \sum_{k=0}^{\infty} \left(u_1(k)^2 \sigma + \boldsymbol{x}_1(k)' \boldsymbol{Q}_1 \boldsymbol{x}_1(k) \right). \tag{11}$$

Choosing R to be 0.01 and σ to be 0.1, the digital observer-controller compensator consists of the following vectors:

$$\boldsymbol{k}_1^T = \begin{bmatrix} 0.7438 & -2.2930 & 2.3604 & -0.8106 \end{bmatrix} \tag{18}$$

$$\boldsymbol{k}_2^T = 1.8291 \tag{19}$$

$$\boldsymbol{L} = \begin{bmatrix} 11.0622 \\ 10.7393 \\ 10.4412 \\ 10.1667 \end{bmatrix}. \tag{20}$$

Thus, every block in Fig. 4 is well defined, and an optimal digital controller for the Ćuk converter is designed.

The closed-loop response for a unit-step disturbance input to the system at the desired operating point ($V_{\text{in}} = 25$ V, $R_L = 30$ Ω) is shown in Fig. 7. It can be seen that the responses are good in terms of overshoot, settling time, and fall time. The same responses for loads of 34 and 25 Ω are shown in Fig. 8, and those for input voltages of 29 and 21 V are shown in Fig. 9. It can be seen that overall system stability can be retained, and the transient dynamics remain to be satisfactory.

VI. Conclusion

A new and general approach for controlling PWM-type switching dc-dc converters has been presented. Full understanding of the converter topologies and their ways of operation are not prerequisites for designing such a controller. The whole

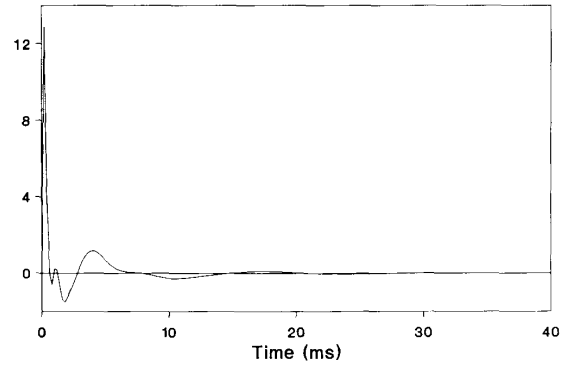


Fig. 7. Step disturbance-to-output response ($\hat{v}_o/\hat{\omega}$) in the normal operating point of 30-Ω load and 25-V input voltage.

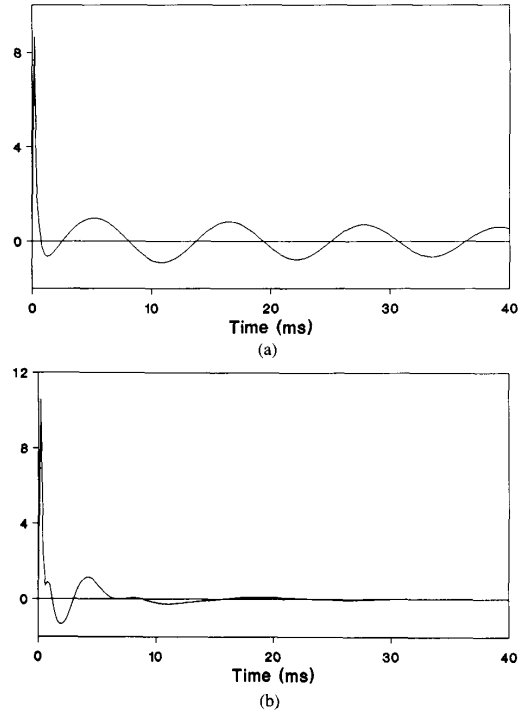


Fig. 8. Step disturbance-to-output response ($\hat{v}_o/\hat{\omega}$) with an input voltage of 25 V but with loads of (a) 34 Ω and (b) 25 Ω.

design procedure can be carried out automatically by a standalone CAD package. Based on linear optimal control theory, a strategy for designing an optimal and robust digital controller for switching regulators has been described. Regarding the inherent system parameter variations, in particular, the shifts of system zeroes, special attention is given to the robustness of the controller to these perturbations.

To highlight the direction of further development, first, it is noted that disturbances, including effects caused by possible links between inputs, are assumed to be adequately modeled as state perturbations, and improvements through the introduction of feedforward compensations may be investigated: second, it is noted that the work is mainly applicable to dc-dc converters of single operating point with small parameter variations. Therefore, further work should be directed to multioperating point switching regulators with large variations in line voltage and output current.

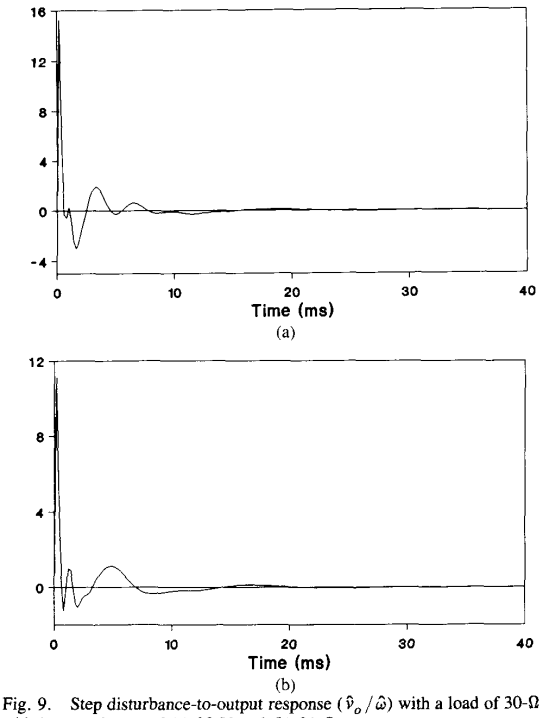


Fig. 9. Step disturbance-to-output response ($\hat{v}_o/\hat{\omega}$) with a load of 30-Ω but with input voltages of (a) 29 V and (b) 21 Ω.

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